11-Bit, 200MSPS/9-Bit, 250MSPS, Ultralow-Power ADCs with Analog Buffer

Check for Samples: ADS58B18, ADS58B19

FEATURES

- **ADS58B18: 11-Bit, 200MSPS**
- **ADS58B19: 9-Bit, 250MSPS**
- **Integrated High-Impedance Analog Input Buffer**
- **Ultralow Power:**
  - **Analog Power: 258mW at 200MSPS**
  - **I/O Power: 69mW (DDR LVDS, low LVDS swing)**
- **High Dynamic Performance:**
  - **ADS58B18: 66dBFS SNR and 81dBc SFDR at 150MHz**
  - **ADS58B19: 55.7dBFS SNR and 76dBc SFDR at 150MHz**
- **Enhanced SNR Using TI-Proprietary SNRBoost Technology (ADS58B18 Only)**
  - **–77.7dBFS SNR in 20MHz Bandwidth**
- **Dynamic Power Scaling with Sample Rate**
- **Output Interface:**
  - **Double Data Rate (DDR) LVDS with Programmable Swing and Strength**
    - **Standard Swing: 350mV**
    - **Low Swing: 200mV**
    - **Default Strength: 100Ω Termination**
    - **2x Strength: 50Ω Termination**
  - **1.8V Parallel CMOS Interface Also Supported**
- **Programmable Gain for SNR/SFDR Trade-Off**
- **DC Offset Correction**
- **Supports Low Input Clock Amplitude**
- **Package: QFN-48 (7mm × 7mm)**

DESCRIPTION

The ADS58B18/B19 are members of the ultralow power ADS4xxx analog-to-digital converter (ADC) family that features integrated analog buffers and SNRBoost technology. The ADS58B18 and ADS58B19 are 11-bit and 9-bit ADCs with sampling rates up to 200MSPS and 250MSPS, respectively. Innovative design techniques are used to achieve high dynamic performance while consuming extremely low power. The analog input pins have buffers with constant performance and input impedance across a wide frequency range. This architecture makes these parts well-suited for multi-carrier, wide bandwidth communications applications such as PA linearization.

The ADS58B18 uses TI-proprietary SNRBoost technology that can be used to overcome SNR limitation as a result of quantization noise for bandwidths less than Nyquist ($f_S/2$).

Both devices have gain options that can be used to improve SFDR performance at lower full-scale input ranges, especially at very high input frequencies. They also include a dc offset correction loop that can be used to cancel the ADC offset. At lower sampling rates, the ADC automatically operates at scaled-down power with no loss in performance.

These devices support both double data rate (DDR) low-voltage differential signaling (LVDS) and parallel CMOS digital output interfaces. The low data rate of the DDR LVDS interface (maximum 500Mbps) makes it possible to use low-cost field-programmable gate array (FPGA)-based receivers. They have a low-swing LVDS mode that can be used to further reduce the power consumption. The strength of the LVDS output buffers can also be increased to support 50Ω differential termination.

The ADS58B18/B19 are both available in a compact QFN-48 package and specified over the industrial temperature range (–40°C to +85°C).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
ADS58B18	QFN-48	RGZ	–40°C to +85°C	GREEN (RoHS, no Sb/Br)	Cu/NiPdAu	AZ58B18	ADS58B18IRGZR	Tape and reel
							ADS58B18IRGZT	Tape and reel
ADS58B19	QFN-48	RGZ	–40°C to +85°C	GREEN (RoHS, no Sb/Br)	Cu/NiPdAu	AZ58B19	ADS58B19IRGZR	Tape and reel
							ADS58B19IRGZT	Tape and reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Eco Plan is the planned eco-friendly classification. Green (RoHS, no Sb/Br): TI defines *Green* to mean Pb-Free (RoHS compatible) and free of Bromine- (Br) and Antimony- (Sb) based flame retardants. Refer to the Quality and Lead-Free (Pb-Free) Data web site for more information.

ABSOLUTE MAXIMUM RATINGS(1)

		ADS58B18, ADS58B19		UNIT
		MIN	MAX	
Supply voltage range, AVDD		–0.3	2.1	V
Supply voltage range, AVDD_BUF		–0.3	3.9	V
Supply voltage range, DRVDD		–0.3	2.1	V
Voltage between AGND and DRGND		–0.3	0.3	V
Voltage between AVDD to DRVDD (when AVDD leads DRVDD)		–2.4	2.4	V
Voltage between DRVDD to AVDD (when DRVDD leads AVDD)		–2.4	2.4	V
Voltage between AVDD_BUF to DRVDD/AVDD		–4.2	4.2	V
Voltage applied to input pins	INP, INM	–0.3	minimum (1.9, AVDD + 0.3)	V
	CLKP, CLKM(2), RESET, SCLK, SDATA, SEN, DFS, SNRBoost_En	–0.3	AVDD + 0.3	V
Operating free-air temperature range, T_A		–40	+85	°C
Operating junction temperature range, T_J			+125	°C
Storage temperature range, T_{stg}		–65	+150	°C
ESD, human body model (HBM)			2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3V|. Doing so prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS58B18 RGZ 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	29	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	n/a	
θ_{JB}	Junction-to-board thermal resistance	10	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.13	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		ADS58B18, ADS58B19			UNIT
		MIN	TYP	MAX	
SUPPLIES					
AVDD	Analog supply voltage	1.7	1.8	1.9	V
AVDD_BUF	Analog buffer supply voltage	3	3.3	3.6	V
DRVDD	Digital supply voltage	1.7	1.8	1.9	V
ANALOG INPUTS					
Differential input voltage range			1.5		V_{PP}
Input common-mode voltage			1.7 ± 0.05		V
Maximum analog input frequency with $1.5V_{PP}$ input amplitude(1)			400		MHz
Maximum analog input frequency with $1V_{PP}$ input amplitude(1)			600		MHz
CLOCK INPUT					
Input clock sample rate: ADS58B18					
Enable low speed mode(2)		30		80	MSPS
Low speed mode disabled (default mode after reset)		> 80		200	MSPS
Input clock sample rate: ADS58B19					
Enable low speed mode(2)		30		80	MSPS
Low speed mode disabled (default mode after reset)		> 80		250	MSPS
Input clock amplitude differential ($V_{CLKP} – V_{CLKM}$)					
	Sine wave, ac-coupled	0.2	1.5		V_{PP}
	LVPECL, ac-coupled		1.6		V_{PP}
	LVDS, ac-coupled		0.7		V_{PP}
	LVCMOS, single-ended, ac-coupled		1.8		V
Input clock duty cycle		35	50	65	%
DIGITAL OUTPUTS					
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND		5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)		100		Ω
T_A	Operating free-air temperature	–40		+85	°C

(1) See the *Theory of Operation* section in the *Application Information*.
(2) See the *Serial Interface* section for details on the low-speed mode.

ELECTRICAL CHARACTERISTICS: ADS58B18/ADS58B19

Typical values are at +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range:
T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, and DRVDD = 1.8V.

PARAMETER	TEST CONDITIONS	ADS58B18			ADS58B19			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				11			9	Bits
SNR (signal-to-noise ratio), LVDS	f_{IN} = 10MHz		66.3			55.8		dBFS
	f_{IN} = 70MHz		66.2			55.8		dBFS
	f_{IN} = 100MHz		66.1			55.8		dBFS
	f_{IN} = 170MHz	64.5	66		54.7	55.8		dBFS
	f_{IN} = 300MHz		65.3			55.8		dBFS
SINAD (signal-to-noise and distortion ratio), LVDS	f_{IN} = 10MHz		66.2			55.8		dBFS
	f_{IN} = 70MHz		66.1			55.8		dBFS
	f_{IN} = 100MHz		66			55.8		dBFS
	f_{IN} = 170MHz	64	65.8		54.2	55.8		dBFS
	f_{IN} = 300MHz		64.8			55.7		dBFS
Spurious-free dynamic range SFDR	f_{IN} = 10MHz		87.5			76.5		dBc
	f_{IN} = 70MHz		87			76.2		dBc
	f_{IN} = 100MHz		87			76.1		dBc
	f_{IN} = 170MHz	71	81		68.5	76		dBc
	f_{IN} = 300MHz		75			75.7		dBc
Total harmonic distortion THD	f_{IN} = 10MHz		86.5			85		dBc
	f_{IN} = 70MHz		85			80		dBc
	f_{IN} = 100MHz		84			79		dBc
	f_{IN} = 170MHz	70	81		67.5	80.5		dBc
	f_{IN} = 300MHz		74.5			71.5		dBc
Second-harmonic distortion HD2	f_{IN} = 10MHz		90			88		dBc
	f_{IN} = 70MHz		91			89		dBc
	f_{IN} = 100MHz		92			85		dBc
	f_{IN} = 170MHz	71	87		68.5	85		dBc
	f_{IN} = 300MHz		79			75		dBc
Third-harmonic distortion HD3	f_{IN} = 10MHz		87.5			89		dBc
	f_{IN} = 70MHz		87			90		dBc
	f_{IN} = 100MHz		87			82		dBc
	f_{IN} = 170MHz	76	81		68.5	85		dBc
	f_{IN} = 300MHz		75			75		dBc
Worst spur (other than second and third harmonics)	f_{IN} = 10MHz		91			76.5		dBc
	f_{IN} = 70MHz		91			76.2		dBc
	f_{IN} = 100MHz		90			76.1		dBc
	f_{IN} = 170MHz	76	89		68.5	76		dBc
	f_{IN} = 300MHz		88			76		dBc
Two-tone intermodulation distortion IMD	f_1 = 185MHz, f_2 = 190MHz, each tone at –7dBFS		–86			–86		dBFS
Input overload recovery	Recovery to within 1% (of final value) for 6dB overload with sine-wave input		1			1		Clock cycles
AC power-supply rejection ratio PSRR	For 100mV_{PP} signal on AVDD supply, up to 10MHz		> 30			> 30		dB
Effective number of bits ENOB	f_{IN} = 170MHz		10.6			9		LSBs
Differential nonlinearity DNL	f_{IN} = 170MHz	–0.7	±0.25	2	–0.6	±0.15	0.85	LSBs
Integral nonlinearity INL	f_{IN} = 170MHz		±0.5	±2.5		±0.25	±1.2	LSBs

ELECTRICAL CHARACTERISTICS: GENERAL

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, 50% clock duty cycle, and 0dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, and DRVDD = 1.8V.

PARAMETER		ADS58B18			ADS58B19			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUTS								
Differential input voltage range			1.5			1.5		V_{PP}
Differential input resistance (at dc); see Figure 59			4			4		kΩ
Differential input capacitance; see Figure 60			2.1			2.1		pF
Analog input bandwidth			550			550		MHz
Analog input common-mode current (per input pin)			< 2			< 2		µA
Common-mode output voltage	VCM		1.7			1.7		V
VCM output current capability			4			4		mA
DC ACCURACY								
Offset error		–15	2	15	–15	2	15	mV
Temperature coefficient of offset error			0.003			0.003		mV/°C
Gain error as a result of internal reference inaccuracy alone	E_{GREF}	–2		2	–2		2	%FS
Gain error of channel alone	E_{GCHAN}		–0.2	–1		–0.2	–1	%FS
Temperature coefficient of E_{GCHAN}			0.001			0.001		Δ%/°C
POWER SUPPLY								
IAVDD Analog supply current			88	105		103	113	mA
IAVDD_BUF Input buffer supply current			30	40		31	42	mA
IDRVDD(1) Output buffer supply current LVDS interface with 100Ω external termination Low LVDS swing (200mV)			38			47		mA
IDRVDD Output buffer supply current LVDS interface with 100Ω external termination Standard LVDS swing (350mV)			62	75		64	82	mA
IDRVDD output buffer supply current(1)(2) CMOS interface(2) 8pF external load capacitance f_{IN} = 2.5MHz			26			35		mA
Analog power: AVDD + AVDD_BUF supplies			260			287		mW
Digital power: LVDS interface, low LVDS swing			68.7			84.6		mW
Digital power: CMOS interface(2) 8pF external load capacitance f_{IN} = 2.5MHz			47			63		mW
Global power-down			10	35		10	35	mW
Standby			185			185		mW

(1) The maximum DRVDD current with CMOS interface depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance on each digital output line is 10pF.

(2) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see the *CMOS Interface Power Dissipation* section in the *Application Information*).

DIGITAL CHARACTERISTICS

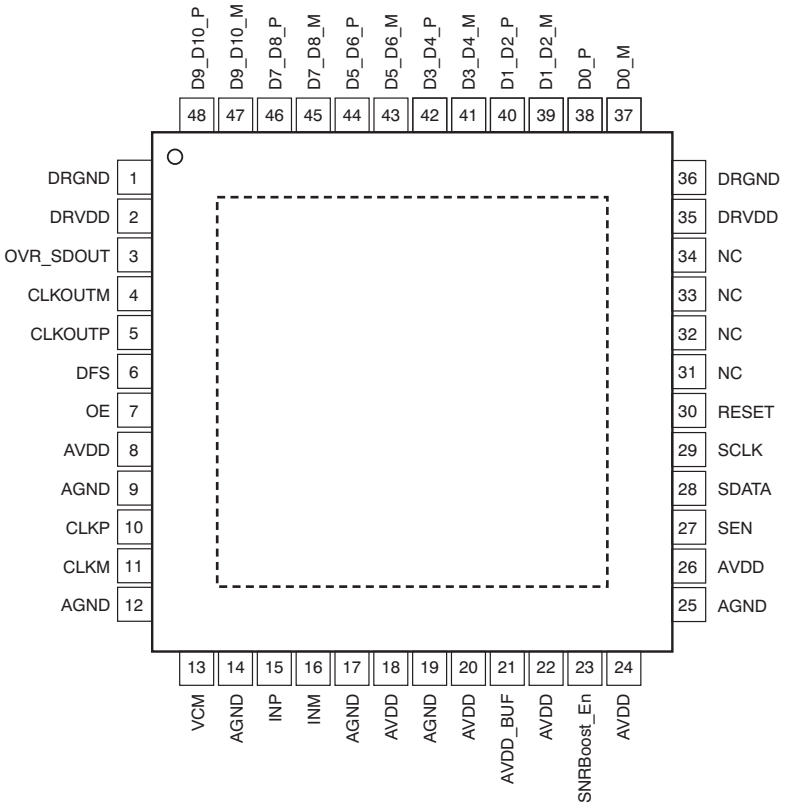
The dc specifications refer to the condition where the digital outputs are not switching but are permanently at a valid logic level '0' or '1'. AVDD = 1.8V and DRVDD = 1.8V.

PARAMETER		TEST CONDITIONS	ADS58B18, ADS58B19			UNIT
			MIN	TYP	MAX	
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, OE, SNRBoost_En)						
High-level input voltage		RESET, SCLK, SDATA, SNRBoost_En, and SEN support 1.8V and 3.3V CMOS logic levels	1.3			V
Low-level input voltage					0.4	V
High-level input voltage		OE only supports 1.8V CMOS logic levels	1.3			V
Low-level input voltage					0.4	V
High-level input current: SDATA, SCLK(1)		V_{HIGH} = 1.8V		10		µA
High-level input current: SEN(2)		V_{HIGH} = 1.8V		0		µA
Low-level input current: SDATA, SCLK		V_{LOW} = 0V		0		µA
Low-level input current: SEN		V_{LOW} = 0V		–10		µA
DIGITAL OUTPUTS (CMOS INTERFACE: D0 TO D13, OVR_SDOUT)						
High-level output voltage			DRVDD – 0.1	DRVDD		V
Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS (LVDS INTERFACE: D0P/M TO D9_10_P/M, CLKOUTP/M)						
High-level output voltage(3)	V_{ODH}	Standard swing LVDS	270	+350	430	mV
Low-level output voltage(3)	V_{ODL}	Standard swing LVDS	–430	–350	–270	mV
High-level output voltage(3)	V_{ODH}	Low swing LVDS		+200		mV
Low-level output voltage(3)	V_{ODL}	Low swing LVDS		–200		mV
Output common-mode voltage	V_{OCM}		0.85	1.05	1.25	V

(1) SDATA and SCLK have an internal 180kΩ pull-down resistor.
(2) SEN has an internal 180kΩ pull-up resistor to AVDD.
(3) With an external 100Ω termination.

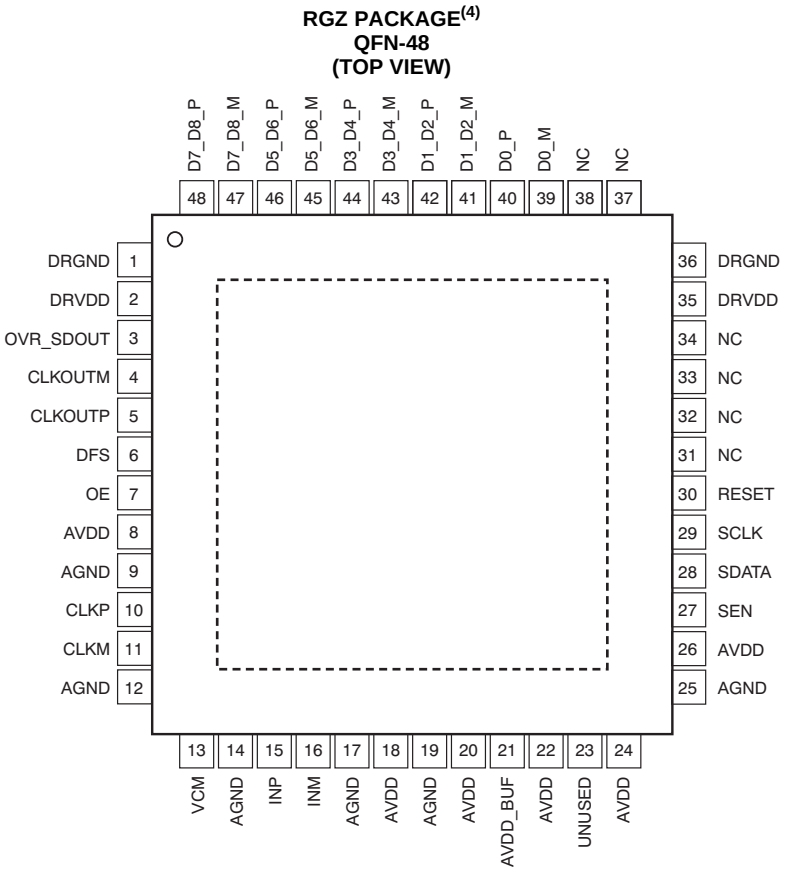
PIN CONFIGURATION (LVDS MODE)

RGZ PACKAGE(3)
QFN-48
(TOP VIEW)



(1) The PowerPAD™ is connected to DRGND.

Figure 1. ADS58B18 LVDS Pinout



(2) The PowerPAD is connected to DRGND.

Figure 2. ADS58B19 LVDS Pinout

ADS58B18, ADS58B19 Pin Assignments (LVDS Mode)

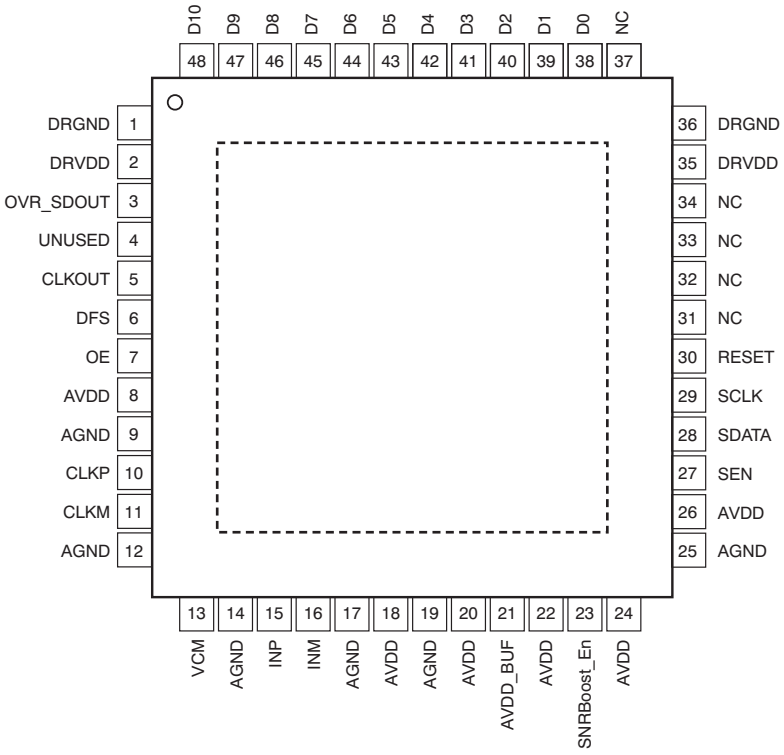
PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
AVDD	8, 18, 20, 22, 24, 26	6	I	1.8V analog power supply
AVDD_BUF	21	1	I	3.3V input buffer supply
AGND	9, 12, 14, 17, 19, 25	6	I	Analog ground
CLKP	10	1	I	Differential clock input, positive
CLKM	11	1	I	Differential clock input, negative
INP	15	1	I	Differential analog input, positive
INM	16	1	I	Differential analog input, negative
VCM	13	1	O	Outputs the common-mode voltage that can be used externally to bias the analog input pins.
RESET	30	1	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface* section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 180kΩ pull-down resistor.
SCLK	29	1	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and should be tied to ground. This pin has an internal 180kΩ pull-down resistor.
SDATA	28	1	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 7). This pin has an internal 180kΩ pull-down resistor.
SEN	27	1	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and should be tied to AVDD. This pin has an internal 180kΩ pull-up resistor to AVDD.

ADS58B18, ADS58B19 Pin Assignments (LVDS Mode) (continued)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
OE	7	1	I	Output buffer enable input, active high; this pin has an internal 180kΩ pull-up resistor to DRVDD.
DFS	6	1	I	Data format select input. This pin sets the DATA FORMAT (twos compliment or offset binary) and the LVDS/CMOS output interface type. See Table 4 for detailed information.
SNRBoost_En	23	1	I	ADS58B18: Digital control pin for SNRBoost mode, active high. ADS58B19: Unused.
CLKOUTP	5	1	O	Differential output clock, true
CLKOUTM	4	1	O	Differential output clock, complement
D0_P	Refer to Figure 1 and Figure 2	1	O	Differential output data D0 and logic low multiplexed, true
D0_M	Refer to Figure 1 and Figure 2	1	O	Differential output data D0 and logic low multiplexed, complement
D1_D2_P	Refer to Figure 1 and Figure 2	1	O	Differential output data D1 and D2 multiplexed, true
D1_D2_M	Refer to Figure 1 and Figure 2	1	O	Differential output data D1 and D2 multiplexed, complement
D3_D4_P	Refer to Figure 1 and Figure 2	1	O	Differential output data D3 and D4 multiplexed, true
D3_D4_M	Refer to Figure 1 and Figure 2	1	O	Differential output data D3 and D4 multiplexed, complement
D5_D6_P	Refer to Figure 1 and Figure 2	1	O	Differential output data D5 and D6 multiplexed, true
D5_D6_M	Refer to Figure 1 and Figure 2	1	O	Differential output data D5 and D6 multiplexed, complement
D7_D8_P	Refer to Figure 1 and Figure 2	1	O	Differential output data D7 and D8 multiplexed, true
D7_D8_M	Refer to Figure 1 and Figure 2	1	O	Differential output data D7 and D8 multiplexed, complement
D9_D10_P	Refer to Figure 1 and Figure 2	1	O	Differential output data D9 and D10 multiplexed, true
D9_D10_M	Refer to Figure 1 and Figure 2	1	O	Differential output data D9 and D10 multiplexed, complement
OVR_SDOUT	3	1	O	This pin functions as an out-of-range indicator after reset, when register bit SERIAL READOUT = 0, and functions as a serial register readout pin when SERIAL READOUT = 1. This pin is a CMOS output level that runs off DRVDD supply.
DRVDD	2, 35	2	I	1.8V digital and output buffer supply
DRGND	1, 36, PAD	2	I	Digital and output buffer ground
NC	Refer to Figure 1 and Figure 2	—	—	Do not connect

PIN CONFIGURATION (CMOS MODE)

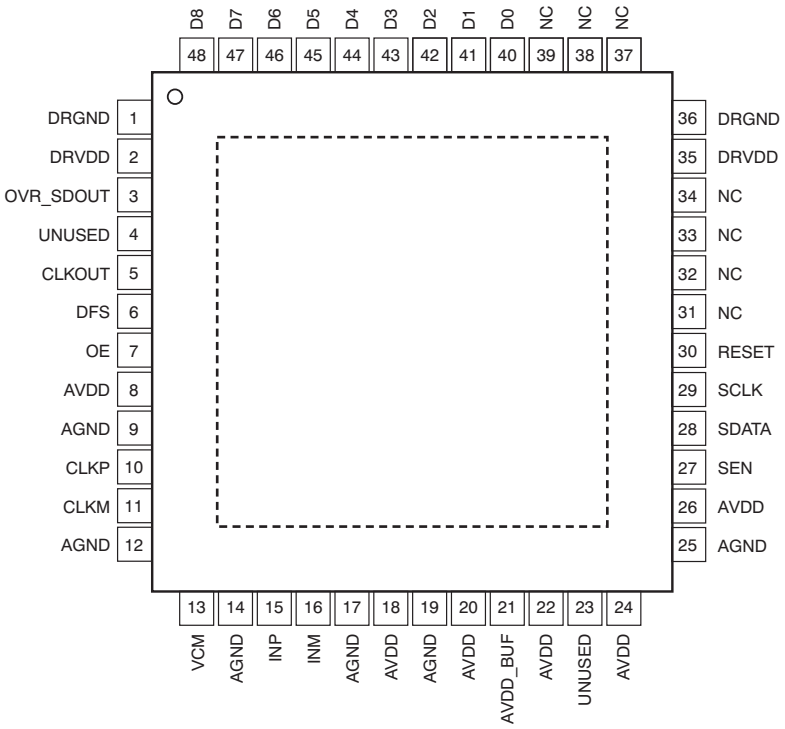
RGZ PACKAGE(5)
QFN-48
(TOP VIEW)



(3) The PowerPAD is connected to DRGND.

Figure 3. ADS58B18 CMOS Pinout

RGZ PACKAGE(6)
QFN-48
(TOP VIEW)



(4) The PowerPAD is connected to DRGND.

Figure 4. ADS58B19 CMOS Pinout

ADS58B18, ADS58B19 Pin Assignments (CMOS Mode)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
AVDD	8, 18, 20, 22, 24, 26	6	I	1.8V analog power supply
AVDD_BUF	21	1	I	3.3V input buffer supply
AGND	9, 12, 14, 17, 19, 25	6	I	Analog ground
CLKP	10	1	I	Differential clock input, positive
CLKM	11	1	I	Differential clock input, negative
INP	15	1	I	Differential analog input, positive
INM	16	1	I	Differential analog input, negative
VCM	13	1	O	Outputs the common-mode voltage that can be used externally to bias the analog input pins.
RESET	30	1	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface* section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 180kΩ pull-down resistor.
SCLK	29	1	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and should be tied to ground. This pin has an internal 180kΩ pull-down resistor.
SDATA	28	1	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 7). This pin has an internal 180kΩ pull-down resistor.
SEN	27	1	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and should be tied to AVDD. This pin has an internal 180kΩ pull-up resistor to AVDD.

ADS58B18, ADS58B19 Pin Assignments (CMOS Mode) (continued)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
DFS	6	1	I	Data format select input. This pin sets the DATA FORMAT (twos compliment or offset binary) and the LVDS/CMOS output interface type. See Table 4 for detailed information.
SNRBoost_En	23	1	I	ADS58B18: Digital control pin for SNRBoost mode, active high. ADS58B19: Unused.
CLKOUT	5	1	O	Differential output clock, true
OE	7	1	I	Output buffer enable input, active high; this pin has an internal 180kΩ pull-up resistor to DRVDD.
D0	Refer to Figure 1 and Figure 2	1	O	Differential output data D0 and logic low multiplexed, true
D1	Refer to Figure 1 and Figure 2	1	O	Differential output data D1 and D2 multiplexed, true
D2	Refer to Figure 1 and Figure 2	1	O	Differential output data D1 and D2 multiplexed, complement
D3	Refer to Figure 1 and Figure 2	1	O	Differential output data D3 and D4 multiplexed, true
D4	Refer to Figure 1 and Figure 2	1	O	Differential output data D3 and D4 multiplexed, complement
D5	Refer to Figure 1 and Figure 2	1	O	Differential output data D5 and D6 multiplexed, true
D6	Refer to Figure 1 and Figure 2	1	O	Differential output data D5 and D6 multiplexed, complement
D7	Refer to Figure 1 and Figure 2	1	O	Differential output data D7 and D8 multiplexed, true
D8	Refer to Figure 1 and Figure 2	1	O	Differential output data D7 and D8 multiplexed, complement
D9	Refer to Figure 1 and Figure 2	1	O	Differential output data D9 and D10 multiplexed, true
D10	Refer to Figure 1 and Figure 2	1	O	Differential output data D9 and D10 multiplexed, complement
OVR_SDOUT	3	1	O	This pin functions as an out-of-range indicator after reset, when register bit SERIAL READOUT = 0, and functions as a serial register readout pin when SERIAL READOUT = 1. This pin is a CMOS output level that runs off DRVDD supply.
DRVDD	2, 35	2	I	1.8V digital and output buffer supply
DRGND	1, 36, PAD	2	I	Digital and output buffer ground
UNUSED	4	1	—	Not used in CMOS mode

FUNCTIONAL BLOCK DIAGRAMS

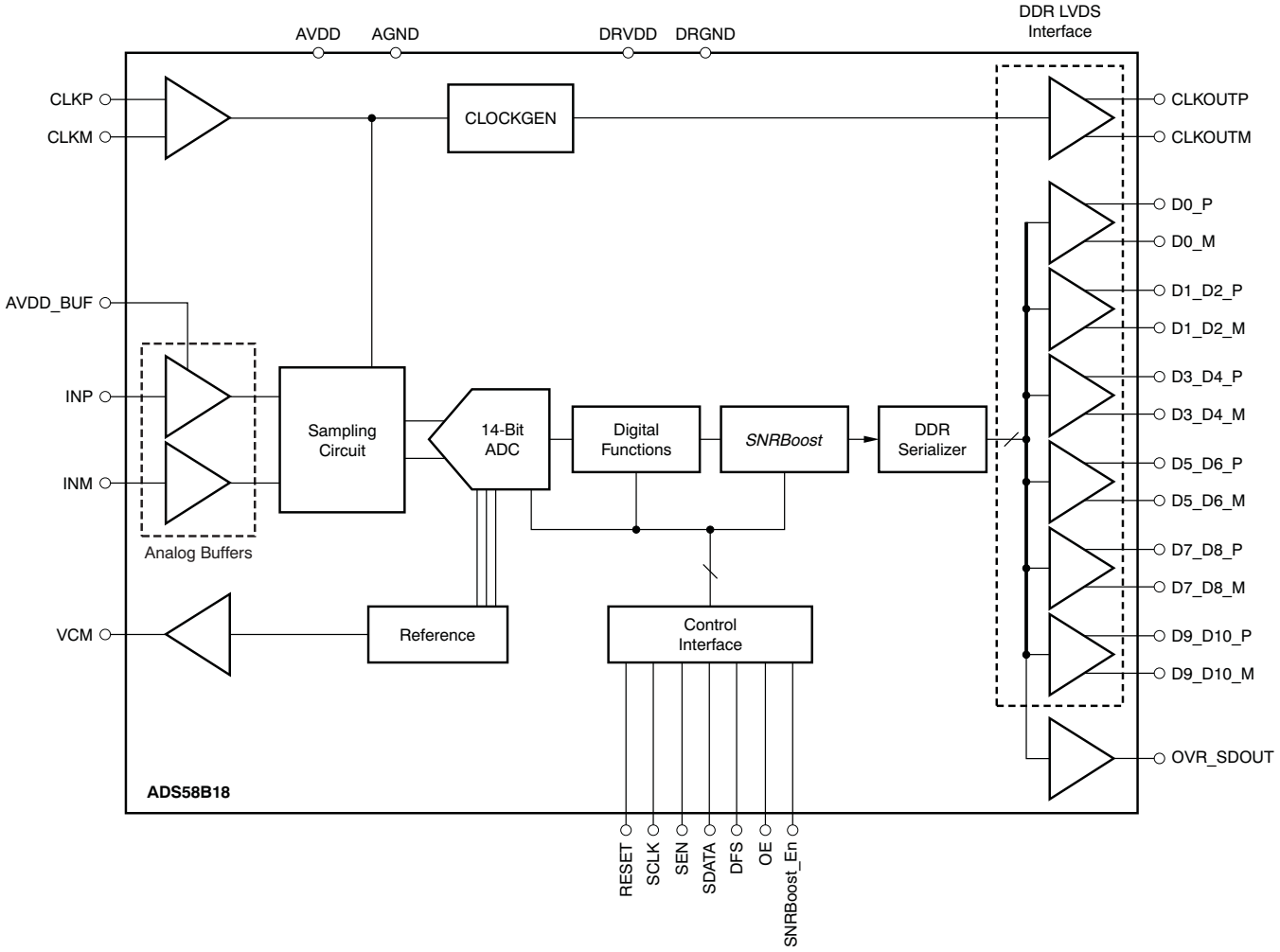


Figure 5. ADS58B18 Block Diagram

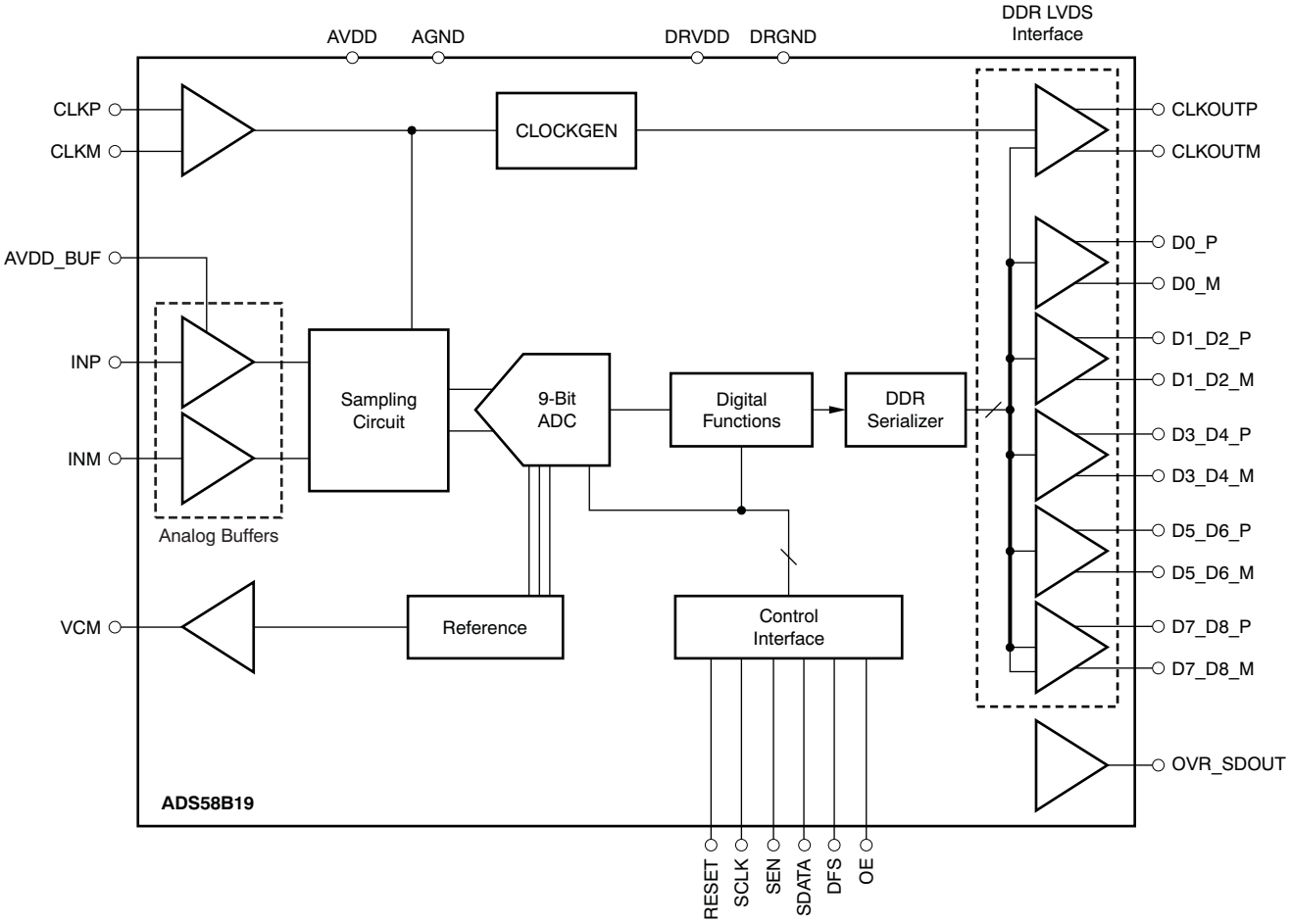
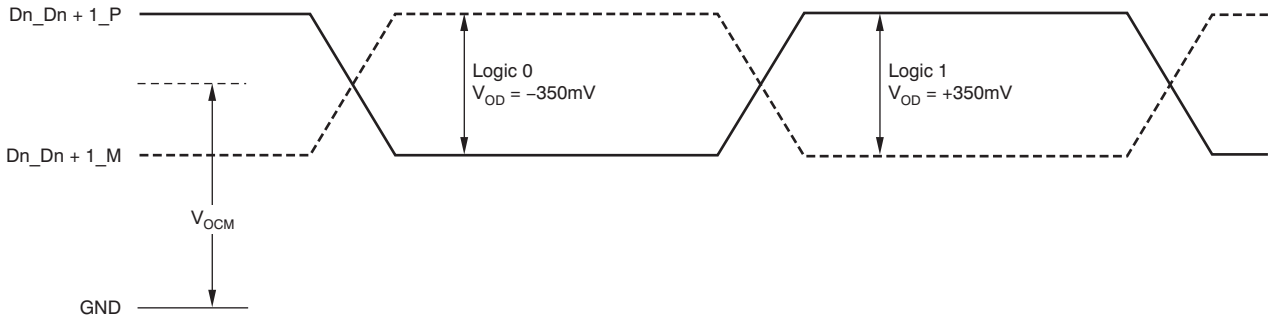


Figure 6. ADS58B19 Block Diagram

TIMING CHARACTERISTICS



(1) With external 100Ω termination.

Figure 7. LVDS Output Voltage Levels

TIMING REQUIREMENTS: LVDS and CMOS Modes(1)

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 5pF(2), and R_{LOAD} = 100Ω(3), unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, and DRVDD = 1.7V to 1.9V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_A	Aperture delay(4)		0.6	0.8	1.2	ns
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±100		ps
t_J	Aperture jitter			100		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		5	25	µs
		Time to valid data after coming out of PDN GLOBAL mode		100	500	µs
	ADC latency(5)	After reset, gain enabled and offset correction disabled		16		Clock cycles
		Gain and offset correction enabled		17		Clock cycles
DDR LVDS MODE(6)						
t_{SU}	Data setup time(7)	Data valid to zero-crossing of CLKOUTP	0.75	1.1		ns
t_H	Data hold time(7)	Zero-crossing of CLKOUTP to data becoming invalid	0.35	0.6		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *1MSPS ≤ sampling frequency ≤ 250MSPS*	3	4.2	5.4	ns
	Variation of t_{PDI}	Between two devices at the same temperature and DRVDD supply		±0.6		ns

(1) Timing parameters are ensured by design and characterization but are not production tested.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) This parameter is specified by design.
(5) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(6) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(7) Data valid refers to a logic high of +100mV and a logic low of –100mV.

TIMING REQUIREMENTS: LVDS and CMOS Modes(1) (continued)

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 5pF(2), and R_{LOAD} = 100Ω(3), unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, and DRVDD = 1.7V to 1.9V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
DDR LVDS MODE (continued)						
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP – CLKOUTM) *1MSPS ≤ sampling frequency ≤ 250MSPS*	42	48	54	%
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100mV to +100mV Fall time measured from +100mV to –100mV *1MSPS ≤ sampling frequency ≤ 250MSPS*		0.14		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100mV to +100mV Fall time measured from +100mV to –100mV *1MSPS ≤ sampling frequency ≤ 250MSPS*		0.14		ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		50	100	ns
PARALLEL CMOS MODE(8)						
t_{START}	Input clock to data delay	Input clock rising edge cross-over to start of data valid(9)			1.1	ns
t_{DV}	Data valid time	Time interval of valid data(9)	2.5	3.2		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *1MSPS ≤ sampling frequency ≤ 200MSPS*	4	5.5	7	ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT *1MSPS ≤ sampling frequency ≤ 200MSPS*		47		%
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ sampling frequency ≤ 250MSPS*		0.35		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ sampling frequency ≤ 200MSPS*		0.35		ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		20	40	ns

(8) For f_S > 200MSPS, it is recommended to use an external clock for data capture instead of the device output clock signal (CLKOUT).
(9) Data valid refers to a logic high of 1.26V and a logic low of 0.54V.

Table 1. LVDS Timing Across Sampling Frequencies

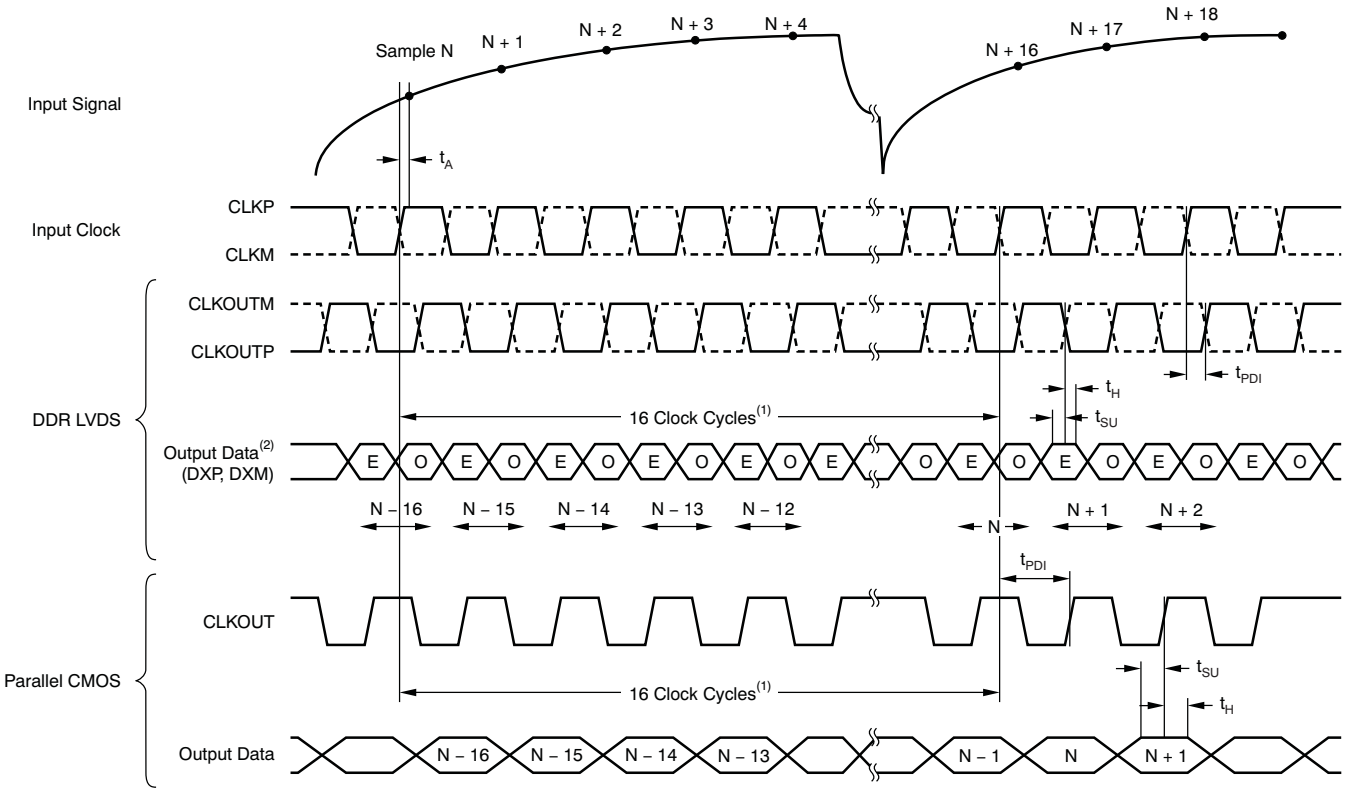
SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)			HOLD TIME (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
230	0.85	1.25		0.35	0.6	
200	1.05	1.55		0.35	0.6	
185	1.1	1.7		0.35	0.6	
160	1.6	2.1		0.35	0.6	
125	2.3	3		0.35	0.6	
80	4.5	5.2		0.35	0.6	

Table 2. CMOS Timing Across Sampling Frequencies (Default, After Reset)

SAMPLING FREQUENCY (MSPS)	TIMING SPECIFIED WITH RESPECT TO OUTPUT CLOCK								
	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
200	1	1.6		2	2.8		4	5.5	7
185	1.3	2		2.2	3		4	5.5	7
160	1.8	2.5		2.5	3.3		4	5.5	7
125	2.5	3.2		3.5	4.3		4	5.5	7
80	4.8	5.5		5.7	6.5		4	5.5	7

Table 3. CMOS Timing Across Sampling Frequencies (Default, After Reset)

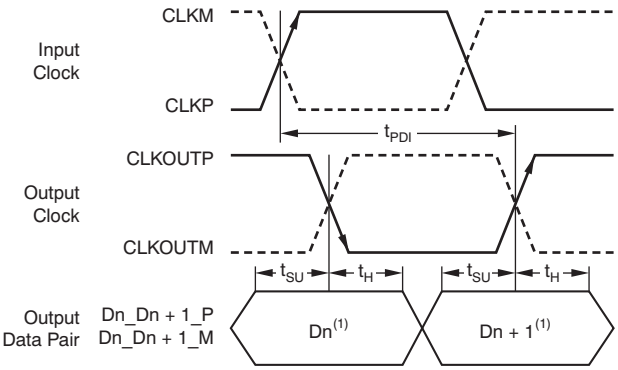
SAMPLING FREQUENCY (MSPS)	TIMING SPECIFIED WITH RESPECT TO INPUT CLOCK					
	t_{START} (ns)			t_{DV} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
250			1.6	2.5	3.2	
230			1.1	2.9	3.5	
200			0.3	3.5	4.2	
185			0	3.9	4.5	
170			–1.3	4.3	5	



(1) At higher sampling frequencies, t_{DPI} is greater than one clock cycle, which then makes the overall latency = ADC latency + 1.

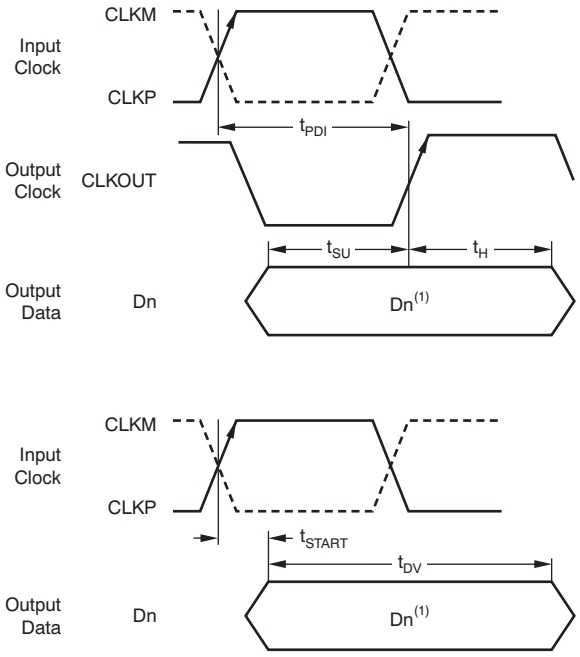
(2) E = Even bits (D0, D2, D4, etc). O = Odd bits (D1, D3, D5, etc).

Figure 8. Latency Diagram



(1) Dn = bits D0, D2, D4, etc. Dn + 1 = Bits D1, D3, D5, etc.

Figure 9. LVDS Mode Timing



Dn = bits D0, D1, D2, etc.

Figure 10. CMOS Mode Timing

DEVICE CONFIGURATION

The ADS58B18/9 have several modes that can be configured using a serial programming interface, as described in Table 4 through Table 7. In addition, the devices have three dedicated parallel pins for quickly configuring commonly-used functions. The parallel pins are DFS (analog 4-level control pin), OE (digital control pin), and SNRBoost_En (digital control pin). The analog control pin can be easily configured using a simple resistor divider (with 10% tolerance resistors).

Table 4. DFS: Analog Control Pin

VOLTAGE APPLIED ON DFS	DESCRIPTION (Data Format/Output Interface)
0, +100mV/–0mV	Twos complement/DDR LVDS
(3/8) AVDD ± 100mV	Twos complement/parallel CMOS
(5/8) AVDD ± 100mV	Straight binary/parallel CMOS
AVDD, +0mV/–100mV	Straight binary/DDR LVDS

Table 5. OE: Digital Control Pin

VOLTAGE APPLIED ON OE	DESCRIPTION
0	Output data buffers disabled
AVDD	Output data buffers enabled

Table 6. SNRBoost_En: Digital Control Pin (ADS58B18 Only)

VOLTAGE APPLIED ON SNRBoost_En	DESCRIPTION
0	SNRBoost disabled
Logic high	SNRBoost enabled

When the serial interface is not used, the SDATA pin can also be used as a standby control pin. To enable this, the RESET pin must be tied high.

Table 7. SDATA: Digital Control Pin

VOLTAGE APPLIED ON SDATA	DESCRIPTION
0	Normal operation
Logic high	Device enters standby

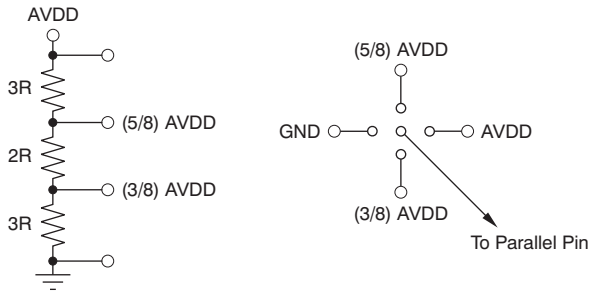


Figure 11. Simplified Diagram to Configure DFS Pin

SERIAL INTERFACE

The analog-to-digital converter (ADC) has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. When SEN is low, the serial shift of bits into the device is enabled, the serial data (on SDATA) are latched at every falling edge of SCLK, and the serial data are loaded into the register at every 16th SCLK falling edge.

In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequency from 20MHz down to very low speeds (a few hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on the RESET pin (of width greater than 10ns), as shown in Figure 12; or
2. By applying a software reset. When using the serial interface, set the RESET bit (D7 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is held low.

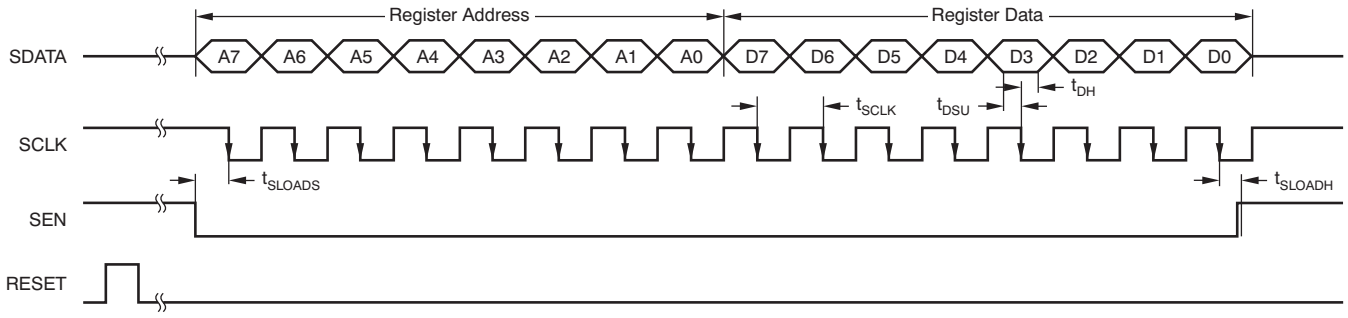


Figure 12. Serial Interface Timing

SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at +25°C, minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, and DRVDD = 1.8V, unless otherwise noted.

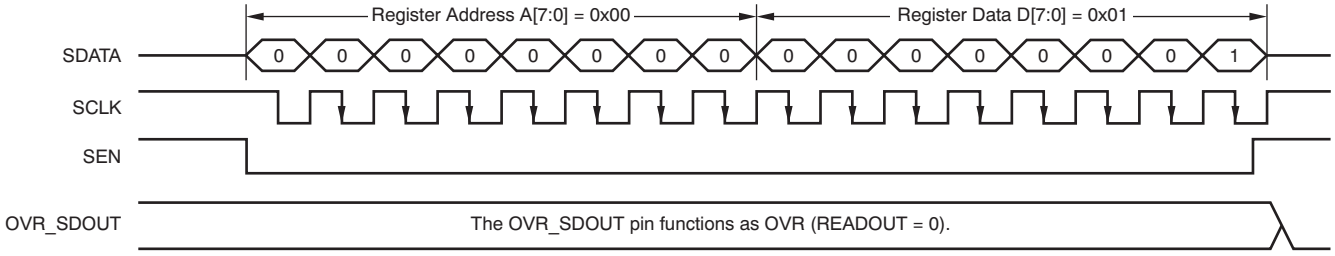
PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to $1/t_{SCLK}$)	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

Serial Register Readout

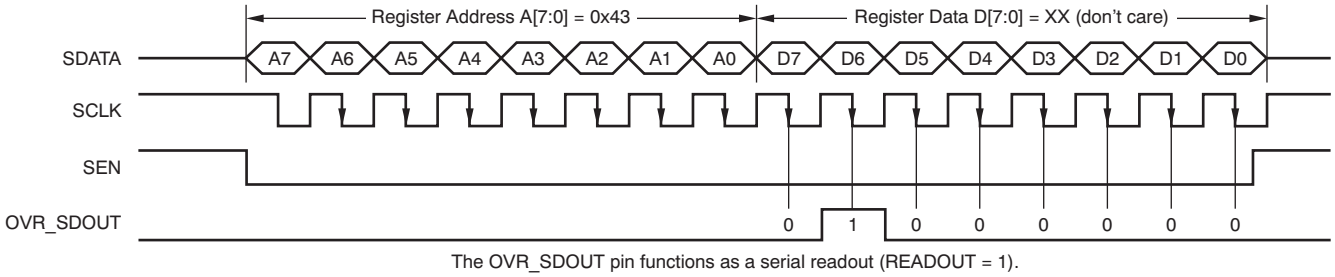
The device includes a mode where the contents of the internal registers can be read back on the OVR_SDOUT pin. This readback may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

After power-up and device reset, the OVR_SDOUT pin functions as an over-range indicator pin by default. When the readout mode is enabled, OVR_SDOUT outputs the contents of the selected register serially. OVR_SDOUT is a CMOS logic output buffer that runs off the DRVDD supply.

1. Set the READOUT register bit to '1'. This setting puts the device in serial readout mode and disables any further writes to the internal registers **except** the register at address 0. Note that the READOUT bit itself is also located in register 0. The device can exit readout mode by writing READOUT to 0. Only the contents of the register at address 0 cannot be read in the register readout mode.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content must be read.
3. The device serially outputs the contents (D7 to D0) of the selected register on the OVR_SDOUT pin.
4. The external controller can latch the contents at the falling edge of SCLK.
5. To exit the serial readout mode, the reset register bit READOUT = 0 enables writes into all registers of the device. At this point, the OVR_SDOUT pin becomes an over-range indicator pin.



a) Enable serial readout (READOUT = 1)



b) Read contents of register 0x43.
This register has been initialized with 0x40 (device is put in global power-down mode).

(1) The OVR_SDOUT pin finctions as OVR (READOUT = 0).

(2) The OVR_SDOUT pin finctions as a serial readout (READOUT = 1).

Figure 13. Serial Readout Timing Diagram

SERIAL REGISTER MAP

Table 8 summarizes the functions supported by the serial interface.

Table 8. Serial Interface Register Map(1)

REGISTER ADDRESS	DEFAULT VALUE AFTER RESET	REGISTER DATA							
A[7:0] (Hex)	D[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	00	0	0	0	0	0	0	RESET	READOUT
01	00	LVDS SWING						0	0
25	00	GAIN				0	TEST PATTERNS		
26	00	0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH
3D	00	DATA FORMAT		ENABLE OFFSET CORR	SNRBoost Enable	SNRBoost Coeff1			
3E	00	SNRBoost Coeff2				0	0	0	0
3F	00	CUSTOM PATTERN HIGH D[10:3]							
40	00	CUSTOM PATTERN D[2:0]			0	0	0	0	0
41	00	LVDS CMOS		CMOS CLKOUT STRENGTH		ENABLE CLKOUT RISE	CLKOUT RISE POSN		ENABLE CLKOUT FALL
42	00	CLKOUT FALL POSN		0	0	DIS LOW LATENCY	STBY	0	BYTE-WISE En
43	00	0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	
BF	00	OFFSET PEDESTAL			0	0	0	0	0
CF	00	FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0
EA	00	OVERRIDE SNRBoost_ EN PIN	0	0	0	0	0	0	0
DF	00	0	0	LOW SPEED		0	0	0	0

(1) Multiple functions in a register can be programmed in a single write operation.

DESCRIPTION OF SERIAL REGISTERS

Register Address 00h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

Bits[7:2] **Always write '0'**

Bit 1 **RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit 0 **READOUT: Serial readout**

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the OVR_SDOUT pin functions as an over-voltage indicator.
1 = Serial readout enabled; the OVR_SDOUT pin functions as a serial data readout. See the *Serial Register Readout* section.

Register Address 01h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS SWING						0	0

Bits[7:2] **LVDS SWING: LVDS swing programmability(1)**

000000 = Default LVDS swing; ±350mV with external 100Ω termination

011011 = LVDS swing increases to ±410mV

110010 = LVDS swing increases to ±465mV

010100 = LVDS swing increases to ±570mV

111110 = LVDS swing decreases to ±200mV

001111 = LVDS swing decreases to ±125mV

Bits[1:0] **Always write '0'**

(1) The EN LVDS SWING register bits must be set to enable LVDS swing control.

Register Address 25h (Default = 00h)

7	6	5	4	3	2	1	0
GAIN				0	TEST PATTERNS		

Bits[7:4] GAIN: Gain programmability

These bits set the gain programmability in 0.5dB steps.

0000 = 0dB gain (default after reset)
0110 = 0.5dB gain
0111 = 1dB gain
1000 = 1.5dB gain
1001 = 2dB gain
1010 = 2.5dB gain
1011 = 3dB gain
1100 = 3.5dB gain

Bit 3 Always write '0'

Bits[2:0] TEST PATTERNS: Data capture

These bits can be used to verify data capture.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern

In the ADS58B18, output data D[10:0] are an alternating sequence of *01010101010* and *10101010101*.
In the ADS58B19, output data D[8:0] are an alternating sequence of *010101010* and *101010101*.

100 = Outputs digital ramp

Output data increments by one LSB (11-bit) every eighth clock cycle from code 0 to code 2047

101 = Output custom pattern (use registers 3Fh and 40h for setting the custom pattern)
110 = Unused
111 = Unused

Register Address 26h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH

Bits[7:2] Always write '0'

Bit 1 LVDS CLKOUT STRENGTH: LVDS output clock buffer strength

This bit determines the external termination to be used with the LVDS output clock buffer.

0 = 100Ω external termination (default strength)

1 = 50Ω external termination (2x strength)

Bit 0 LVDS DATA STRENGTH: LVDS data buffer strength

This bit determines the external termination to be used with all of the LVDS data buffers.

0 = 100Ω external termination (default strength)

1 = 50Ω external termination (2x strength)

Register Address 3Dh (Default = 00h)

7	6	5	4	3	2	1	0
DATA FORMAT		ENABLE OFFSET CORR	SNRBoost Enable	SNRBoost Coeff1			

Bits[7:6] DATA FORMAT: Data format selection

These bits select the data format.
00 = The DFS pin controls data format selection
10 = Twos complement
11 = Offset binary

Bit 5 ENABLE OFFSET CORR: Offset correction setting

This bit sets the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

Bit 4 SNRBoost Enable: SNRBoost setting

This bit enables the SNRBoost.
0 = SNRBoost disabled
1 = SNRBoost enabled

Bits[3:0] SNRBoost Coeff1: SNRBoost coefficient 1

See the *SNR Enhancement Using SNRBoost* section.

Register Address 3Eh (Default = 00h)

7	6	5	4	3	2	1	0
SNRBoost Coeff2				0	0	0	0

Bits[7:4] SNRBoost Coeff2: SNRBoost coefficient 2

See the *SNR Enhancement Using SNRBoost* section.

Bits[3:0] Always write '0'

Register Address 3Fh (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8	CUSTOM PATTERN D7	CUSTOM PATTERN D6	CUSTOM PATTERN D5	CUSTOM PATTERN D4	CUSTOM PATTERN D3

Bits[7:0] CUSTOM PATTERN

These bits set the custom pattern.

Register Address 40h (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0	0	0	0	0	0

Bits[7:5] CUSTOM PATTERN

These bits set the custom pattern.

Bits[4:0] Always write '0'

Register Address 41h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STRENGTH		ENABLE CLKOUT RISE	CLKOUT RISE POSN		ENABLE CLKOUT FALL

Bits[7:6] LVDS CMOS: Interface selection

These bits select the interface.
00 = The DFS pin controls the selection of either LVDS or CMOS interface
01 = DDR LVDS interface
11 = Parallel CMOS interface

Bits[5:4] CMOS CLKOUT STRENGTH

Controls strength of CMOS output clock only.
00 = Maximum strength (recommended and used for specified timings)
01 = Medium strength
10 = Low strength
11 = Very low strength

Bit 3 ENABLE CLKOUT RISE

0 = Disables control of output clock rising edge
1 = Enables control of output clock rising edge

Bits[2:1] CLKOUT RISE POSN: CLKOUT rise control

Controls position of output clock rising edge
LVDS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 500ps, hold increases by 500ps
10 = Data transition is aligned with rising edge
11 = Setup reduces by 200ps, hold increases by 200ps
CMOS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 100ps, hold increases by 100ps
10 = Setup reduces by 200ps, hold increases by 200ps
11 = Setup reduces by 1.5ns, hold increases by 1.5ns

Bit 0 ENABLE CLKOUT FALL

0 = Disables control of output clock fall edge
1 = Enables control of output clock fall edge

Register Address 42h (Default = 00h)

7	6	5	4	3	2	1	0
CLKOUT FALL POSN		0	0	DIS LOW LATENCY	STBY	0	BYTE-WISE En

Bits[7:6] CLKOUT FALL POSN

These bits control the position of the output clock falling edge.
LVDS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 400ps, hold increases by 400ps
10 = Data transition is aligned with rising edge
11 = Setup reduces by 200ps, hold increases by 200ps
CMOS interface:
00 = Default position (timings are specified in this condition)
01 = Falling edge is advanced by 100ps
10 = Falling edge is advanced by 200ps
11 = Falling edge is advanced by 1.5ns

Bits[5:4] Always write '0'

Bit 3 DIS LOW LATENCY: Disable low latency

This bit controls the low-latency mode.
0 = Recommended not to use this mode.
1 = After reset, the low-latency mode is disabled and 0dB gain is enabled.

Bit 2 STBY: Standby mode

This bit sets the standby mode.
0 = Normal operation
1 = Only the ADC and output buffers are powered down; internal reference is active; wake-up time from standby is fast

Bit 1 Always write '0'

Bit 0 BYTE-WISE En: Output data enable

0 = The output data bit sequence is bit-wise (see Figure 22).
1 = The output data bit sequence is byte-wise (see Figure 23 and Figure 24).

Register Address 43h (Default = 00h)

7	6	5	4	3	2	1	0
0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	

Bit 7 **Always write '0'**

Bit 6 **PDN GLOBAL: Power-down**

This bit sets the state of operation.
0 = Normal operation
1 = Total power down; the ADC, internal references, and output buffers are powered down; slow wake-up time.

Bit 5 **Always write '0'**

Bit 4 **PDN OBUF: Power-down output buffer**

This bit set the output buffer.
0 = Output buffer enabled
1 = Output buffer powered down

Bits[3:2] **Always write '0'**

Bits[1:0] **EN LVDS SWING: LVDS swing control**

00 = LVDS swing control using LVDS SWING register bits is disabled
01 = Do not use
10 = Do not use
11 = LVDS swing control using LVDS SWING register bits is enabled

Register Address BFh (Default = 00h)

7	6	5	4	3	2	1	0
OFFSET PEDESTAL			0	0	0	0	0

Bits[7:5] **OFFSET PEDESTAL**

These bits set the offset pedestal.
When the offset correction is enabled, the final converged value after the offset is corrected is the ADC mid-code value. A pedestal can be added to the final converged value by programming these bits.

011 = +3 LSB

010 = +2 LSB

001 = +1 LSB

000 = 0 LSB

111 = –1 LSB

110 = –2 LSB

101 = –3 LSB

100 = –4 LSB

Bits[4:0] **Always write '0'**

Register Address CFh (Default = 00h)

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0

Bit 7 **FREEZE OFFSET CORR**

This bit sets the freeze offset correction.

0 = Estimation of offset correction is not frozen (bit ENABLE OFFSET CORR must be set).

1 = Estimation of offset correction is frozen (bit EN OFFSET CORR must be set). When frozen, the last estimated value is used for offset correction every clock cycle; see *Offset Correction* section.

Bit 6 **Always write '0'**

Bit[5:2] **OFFSET CORR TIME CONSTANT**

These bits set the offset correction time constant for the correction loop time constant in number of clock cycles.

VALUE	TIME CONSTANT (Number of Clock Cycles)
0000	1M
0001	2M
0010	3M
0011	4M
0100	16M
0101	32M
0110	64M
0111	128M
1000	256M
1001	512M
1010	1G
1011	2G

Bits[1:0] **Always write '0'**

Register Address EAh (Default = 00h)

7	6	5	4	3	2	1	0
OVERRIDE SNBoost_EN PIN	0	0	0	0	0	0	0

Bit 7 **OVERRIDE SNBoost_EN PIN: SNBoost_EN pin override**

After reset, the SNRBoost_En pin controls the turning on and off of the SNRBoost function, independent of the state of register bit SNRBoost Enable. By setting the OVER-RIDE bit to '1', the register bit can control the SNRBoost function.

0 = SNRBoost_En pin controls SNRBoost function, independent of register bit.

1 = Register bit SNRBoost Enable controls the SNRBoost function, independent of SNRBoost_En pin.

Bits[6:0] **Always write '0'**

Register Address DFh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	LOW SPEED		0	0	0	0

Bits[7:6] Always write '0'

Bits[5:4] LOW SPEED: Low-speed mode

00, 01, 10 = Low-speed mode disabled (default state after reset); this setting is recommended for sampling rates greater than 80MSPS.
11 = Low-speed mode enabled; this setting is recommended for sampling rates lower than or equal to 80MSPS.

Bits[3:0] Always write '0'

TYPICAL CHARACTERISTICS: ADS58B18

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

FFT FOR 20MHz INPUT SIGNAL

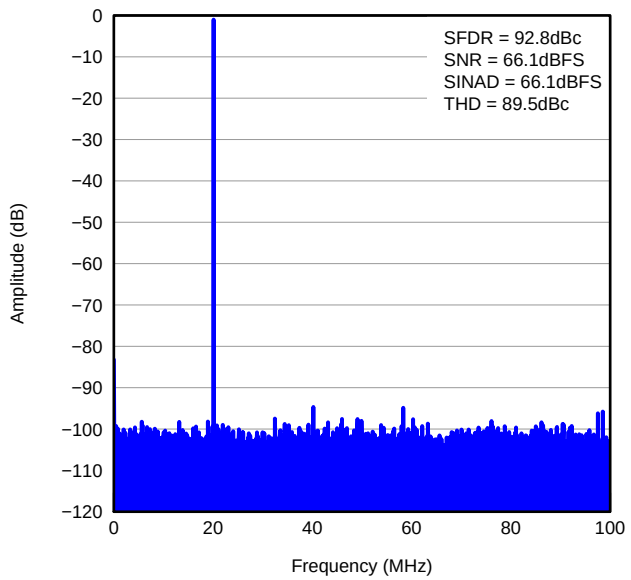


Figure 14.

FFT FOR 170MHz INPUT SIGNAL

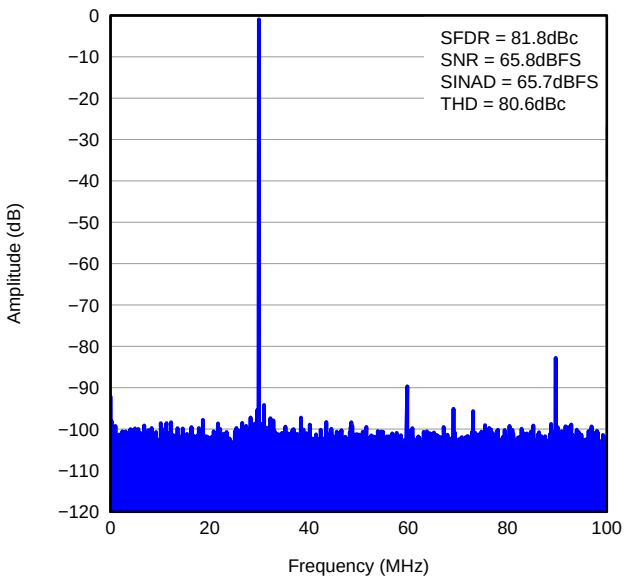


Figure 15.

FFT FOR TWO-TONE INPUT SIGNAL

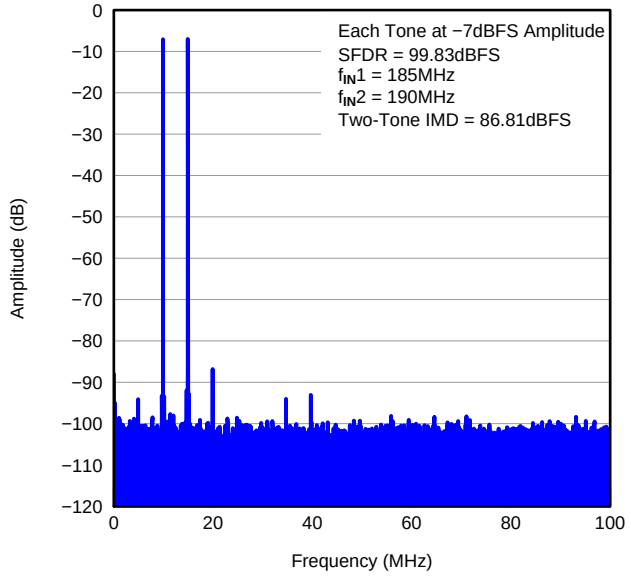


Figure 16.

FFT FOR TWO-TONE INPUT SIGNAL

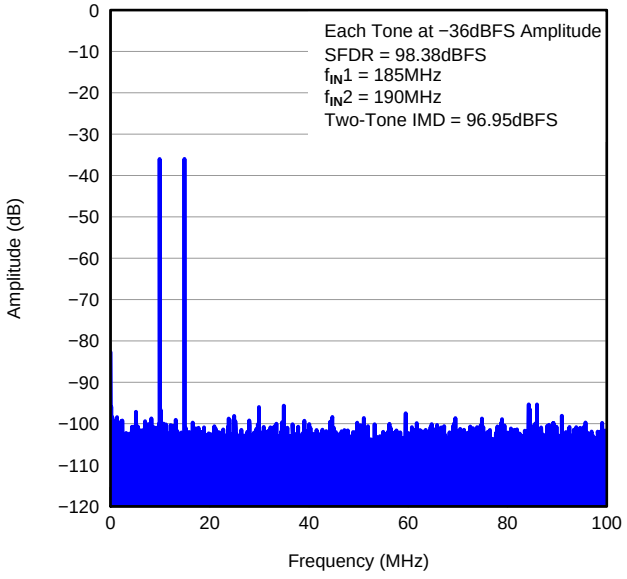


Figure 17.

TYPICAL CHARACTERISTICS: ADS58B18 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

FFT FOR 150MHz INPUT SIGNAL (SNRBoost Enabled, 5MHz Bandwidth)

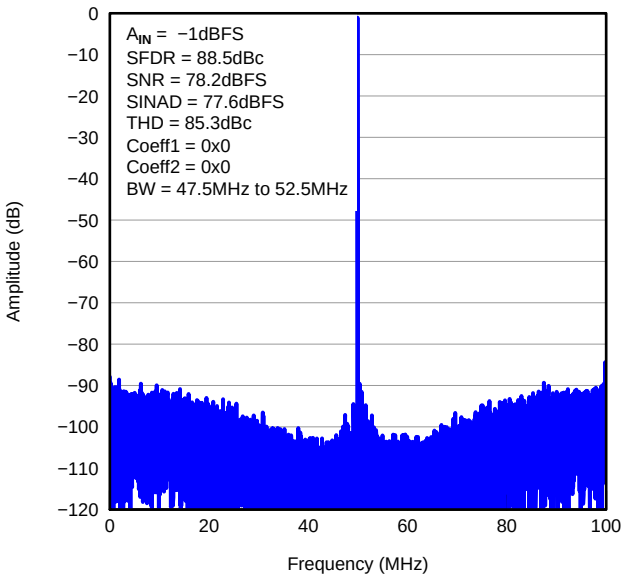


Figure 18.

FFT FOR 150MHz INPUT SIGNAL (SNRBoost Enabled, 5MHz Bandwidth)

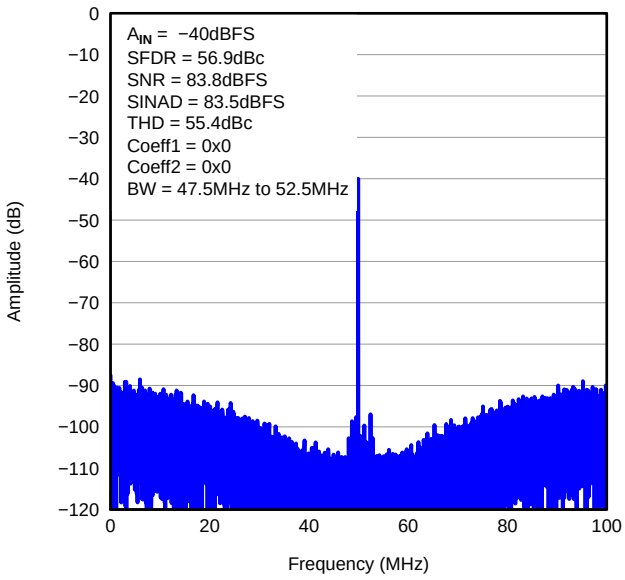


Figure 19.

FFT FOR 150MHz INPUT SIGNAL (SNRBoost Enabled, 20MHz Bandwidth)

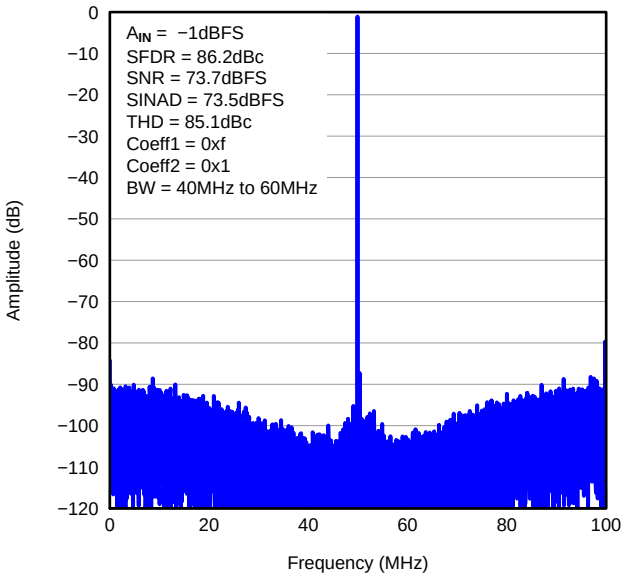


Figure 20.

FFT FOR 150MHz INPUT SIGNAL (SNRBoost Enabled, 20MHz Bandwidth)

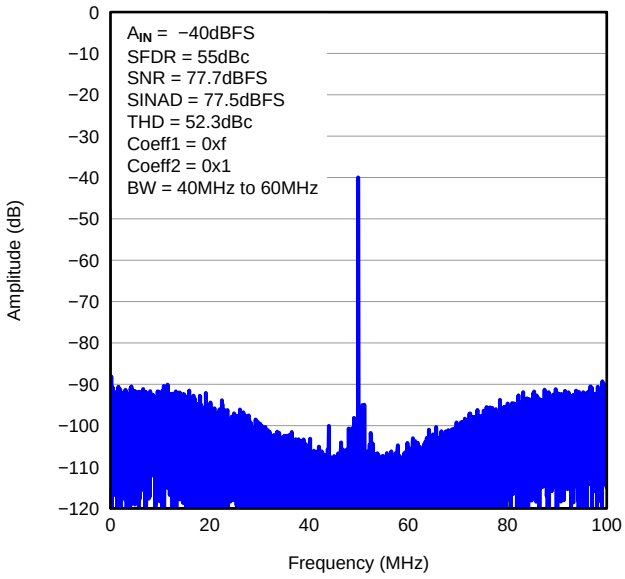


Figure 21.

TYPICAL CHARACTERISTICS: ADS58B18 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

FFT FOR 150MHz INPUT SIGNAL (SNRBoost Enabled, 30MHz Bandwidth)

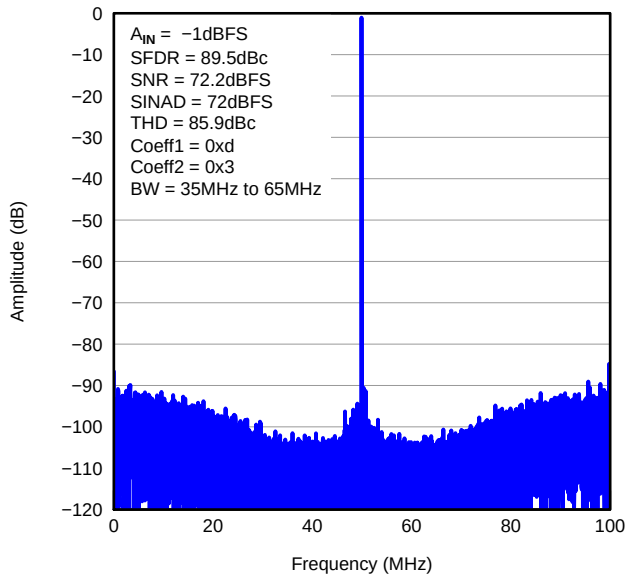


Figure 22.

FFT FOR 150MHz INPUT SIGNAL (SNRBoost Enabled, 30MHz Bandwidth)

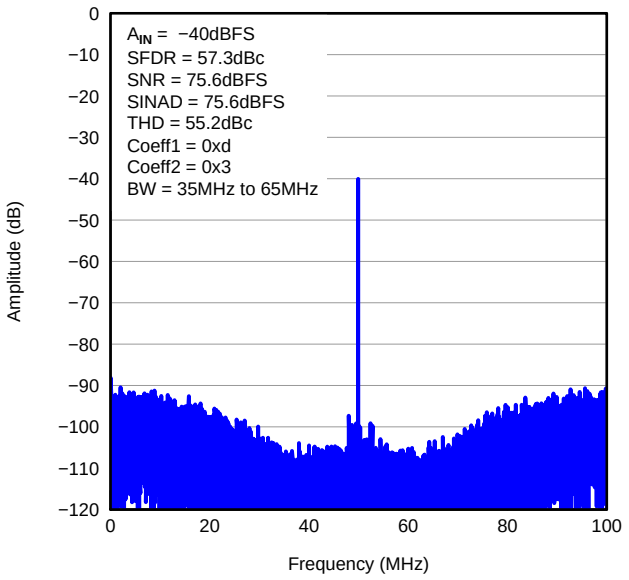


Figure 23.

SFDR ACROSS INPUT FREQUENCY

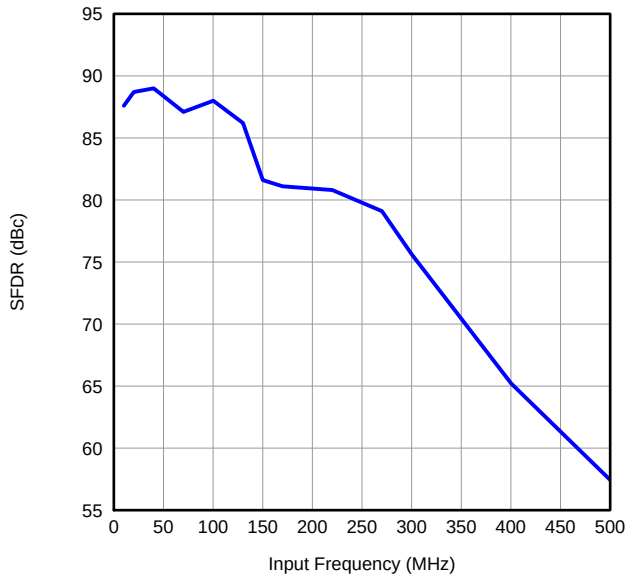


Figure 24.

SNR ACROSS INPUT FREQUENCY

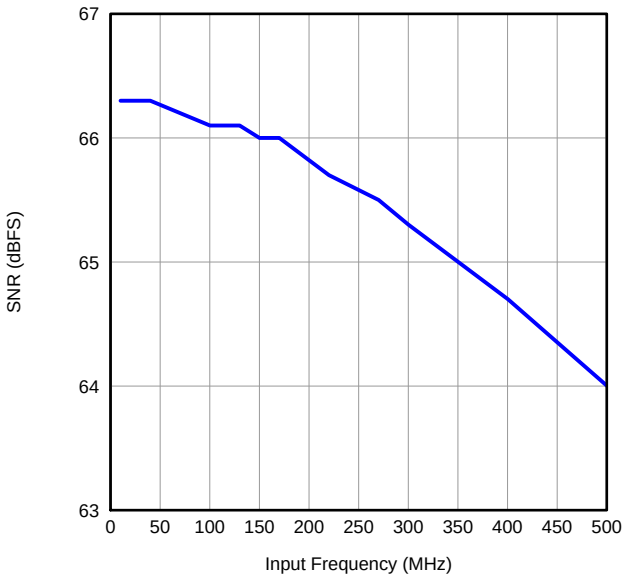


Figure 25.

TYPICAL CHARACTERISTICS: ADS58B18 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SFDR ACROSS GAIN

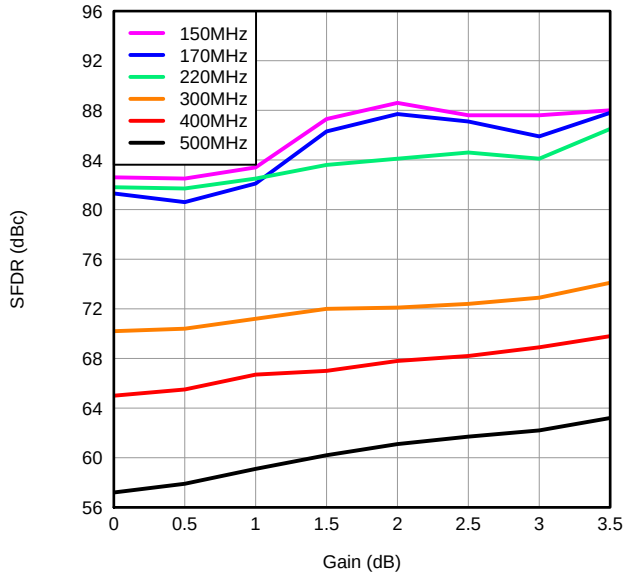


Figure 26.

SINAD ACROSS GAIN

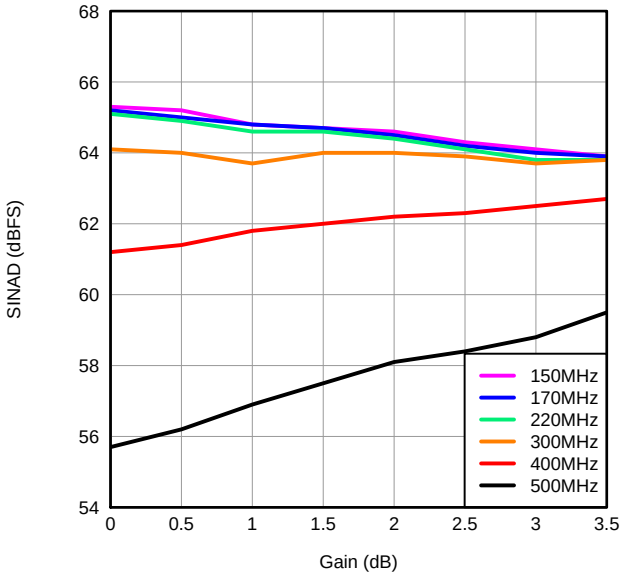


Figure 27.

SFDR ACROSS AVDD SUPPLY vs TEMPERATURE

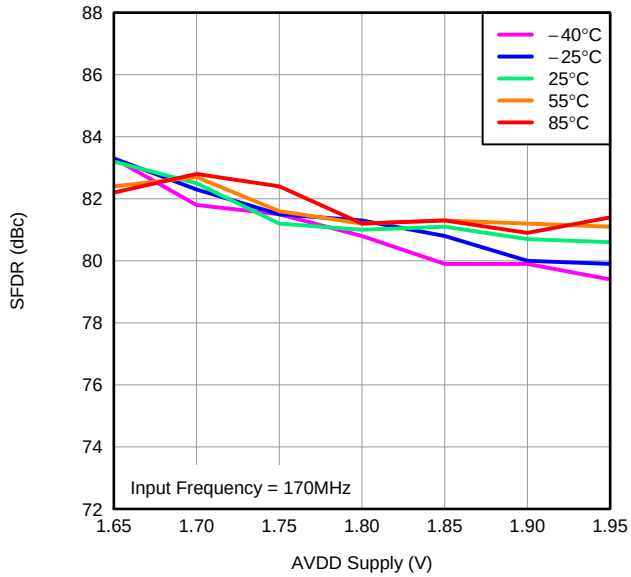


Figure 28.

SNR ACROSS AVDD SUPPLY vs TEMPERATURE

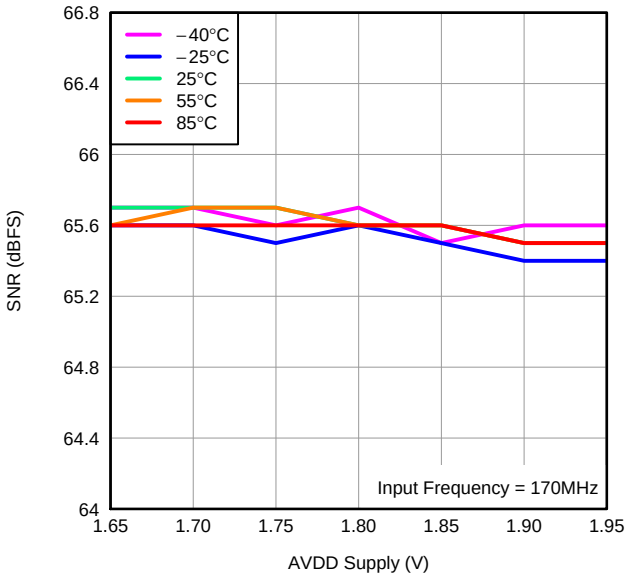


Figure 29.

TYPICAL CHARACTERISTICS: ADS58B18 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

PERFORMANCE ACROSS DRVDD SUPPLY

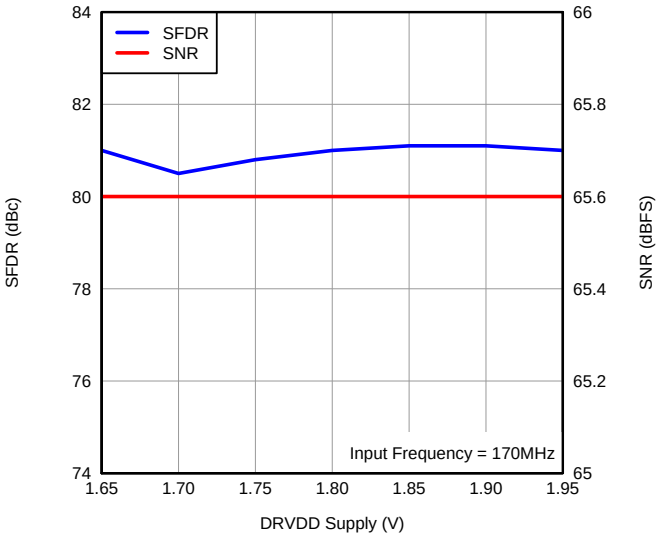


Figure 30.

PERFORMANCE ACROSS INPUT AMPLITUDE

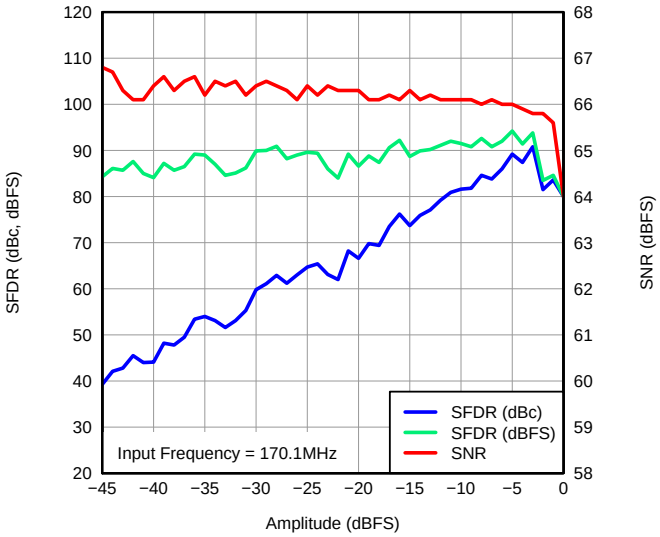


Figure 31.

PERFORMANCE ACROSS INPUT COMMON-MODE VOLTAGE

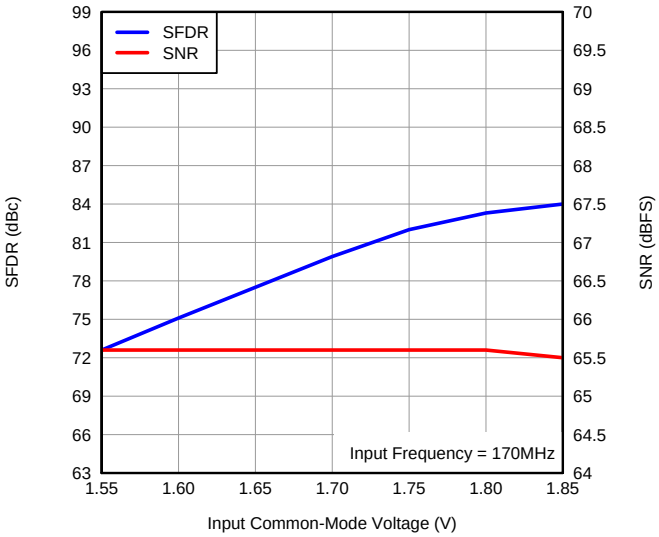


Figure 32.

PERFORMANCE ACROSS INPUT CLOCK AMPLITUDE

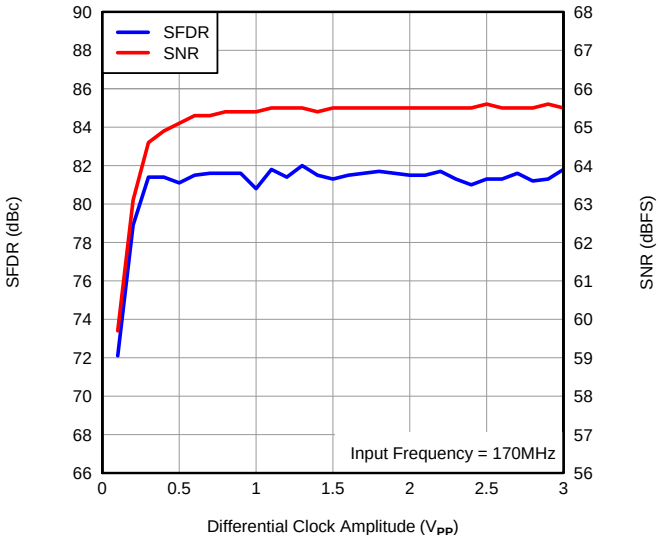


Figure 33.

TYPICAL CHARACTERISTICS: ADS58B18 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

PERFORMANCE ACROSS INPUT CLOCK DUTY CYCLE

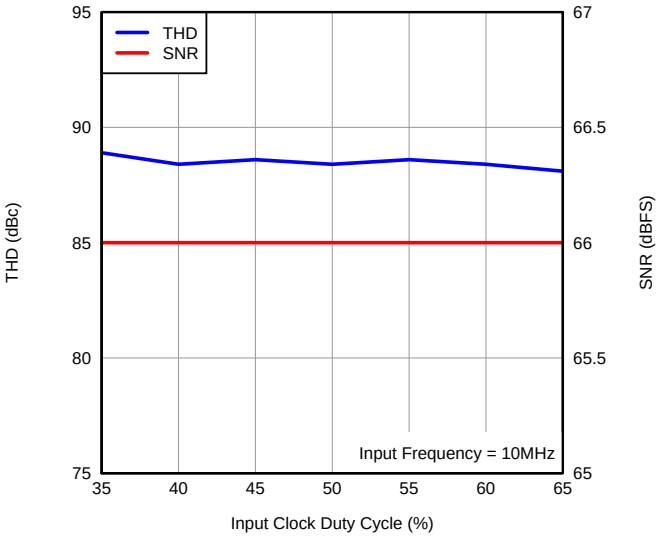


Figure 34.

ANALOG POWER vs SAMPLING FREQUENCY

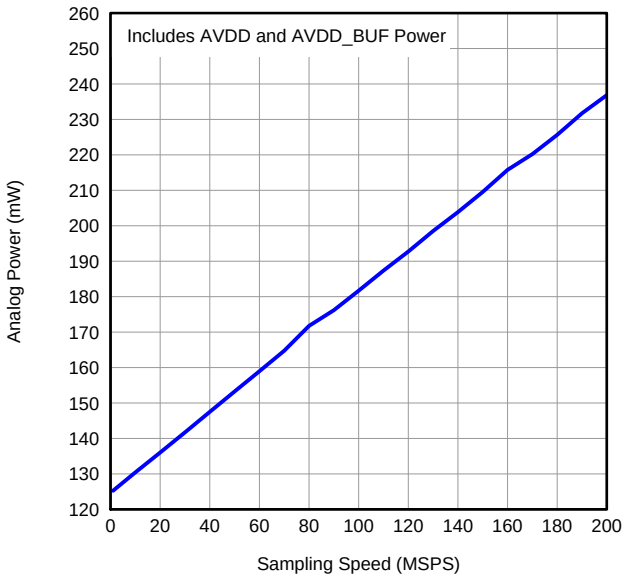


Figure 35.

DRVDD POWER vs SAMPLING FREQUENCY

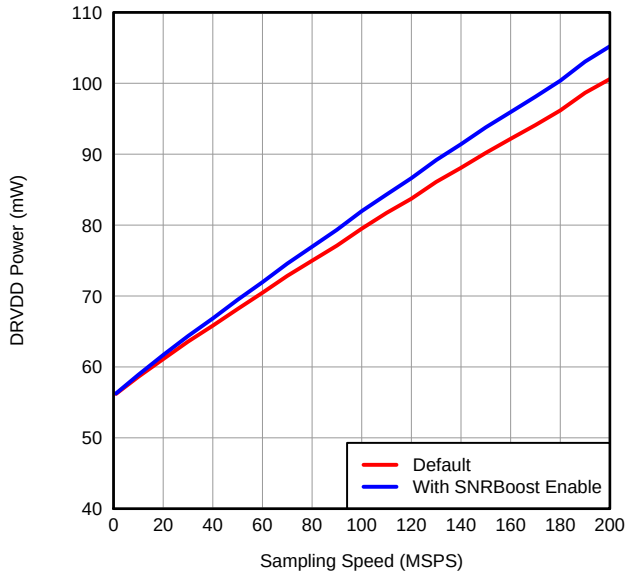


Figure 36.

TYPICAL CHARACTERISTICS: ADS58B19

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

FFT FOR 20MHz INPUT SIGNAL

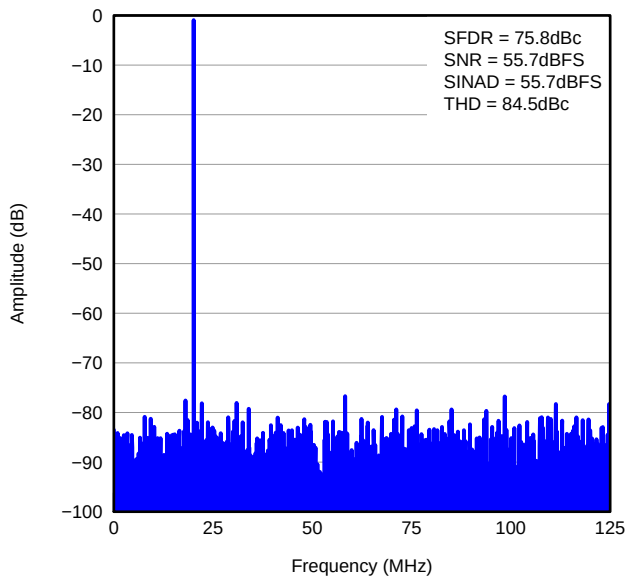


Figure 37.

FFT FOR 170MHz INPUT SIGNAL

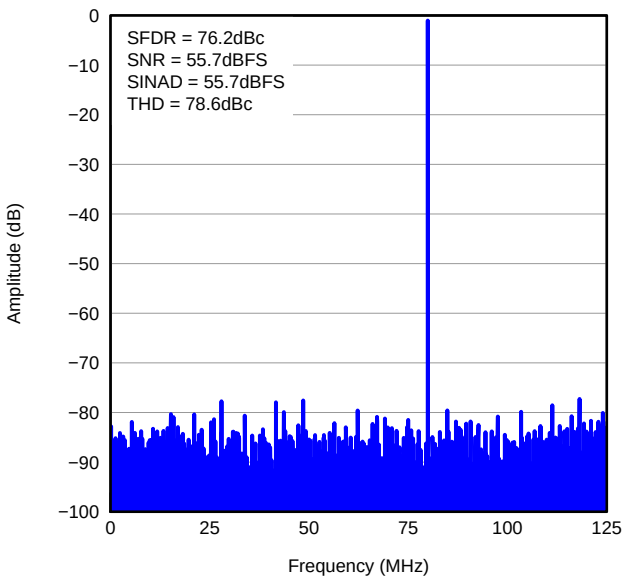


Figure 38.

FFT FOR TWO-TONE INPUT SIGNAL

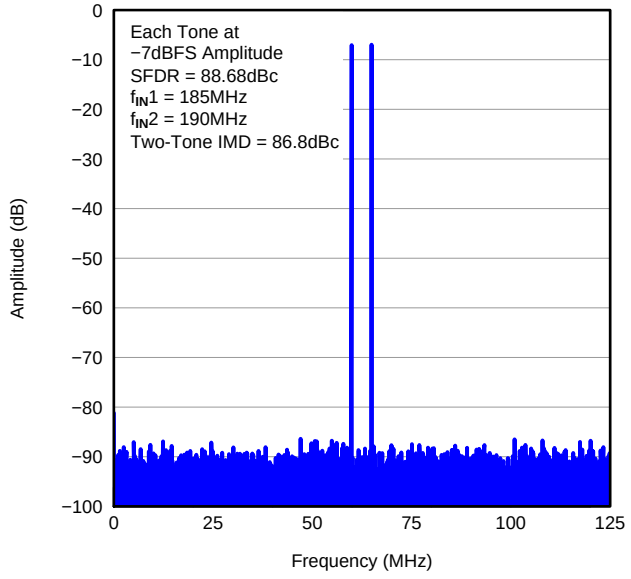


Figure 39.

FFT FOR TWO-TONE INPUT SIGNAL

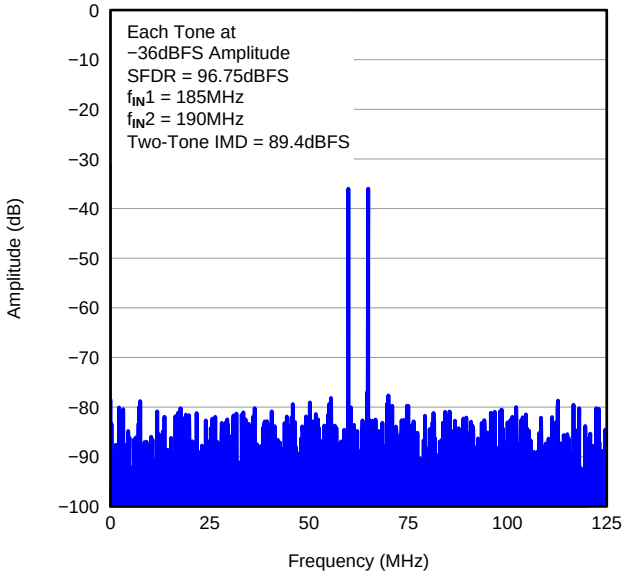


Figure 40.

TYPICAL CHARACTERISTICS: ADS58B19 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SFDR ACROSS INPUT FREQUENCY

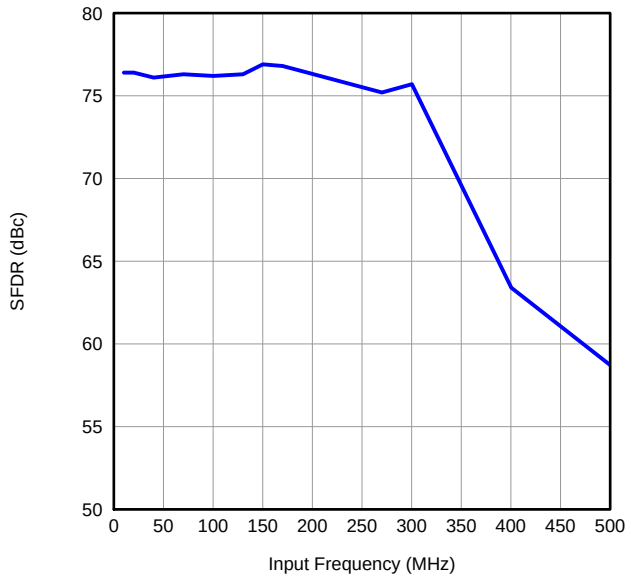


Figure 41.

SNR ACROSS INPUT FREQUENCY

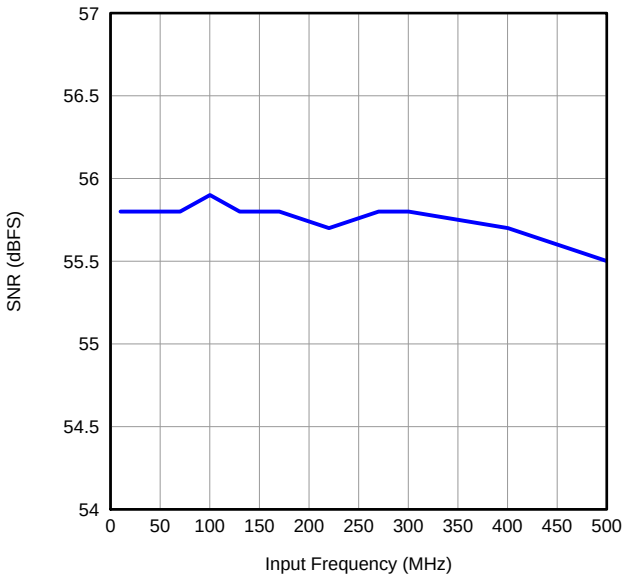


Figure 42.

SFDR ACROSS GAIN

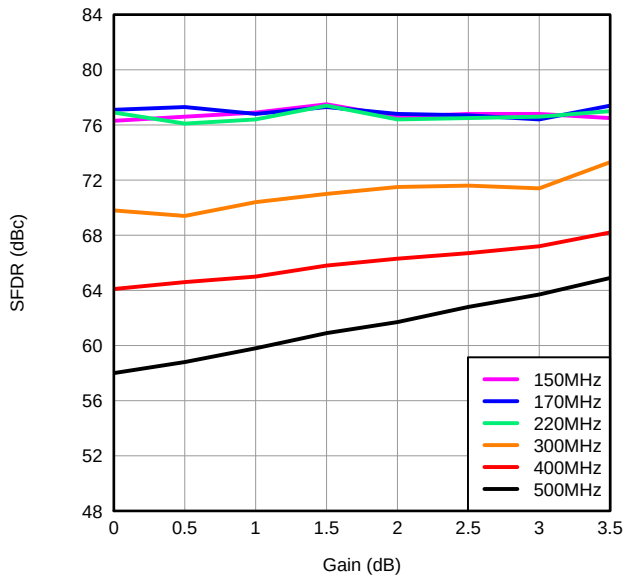


Figure 43.

SINAD ACROSS GAIN

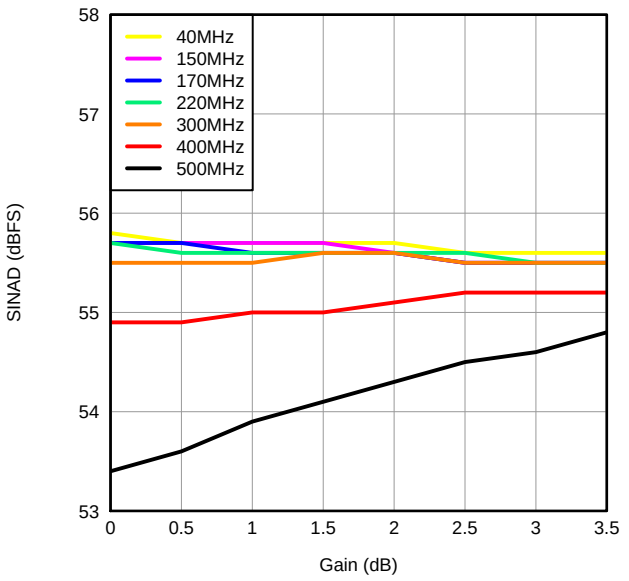


Figure 44.

TYPICAL CHARACTERISTICS: ADS58B19 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

SFDR ACROSS AVDD SUPPLY vs TEMPERATURE

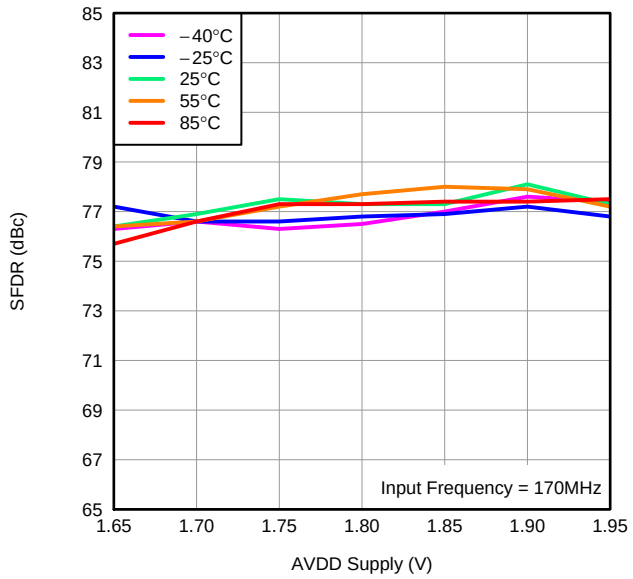


Figure 45.

SNR ACROSS AVDD SUPPLY vs TEMPERATURE

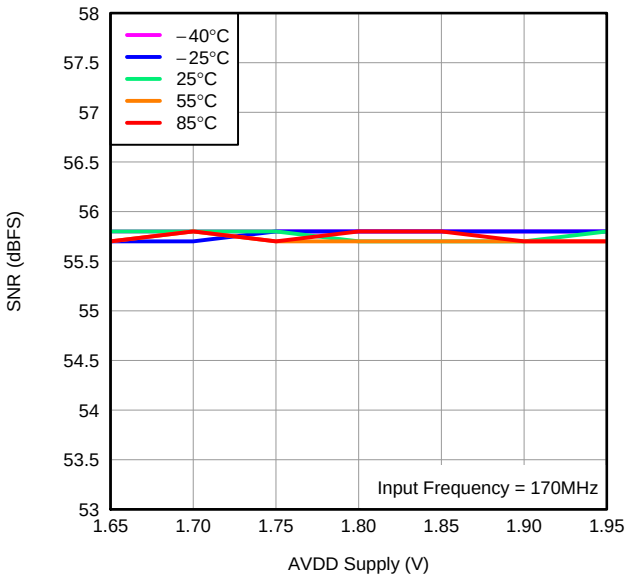


Figure 46.

PERFORMANCE ACROSS DRVDD SUPPLY

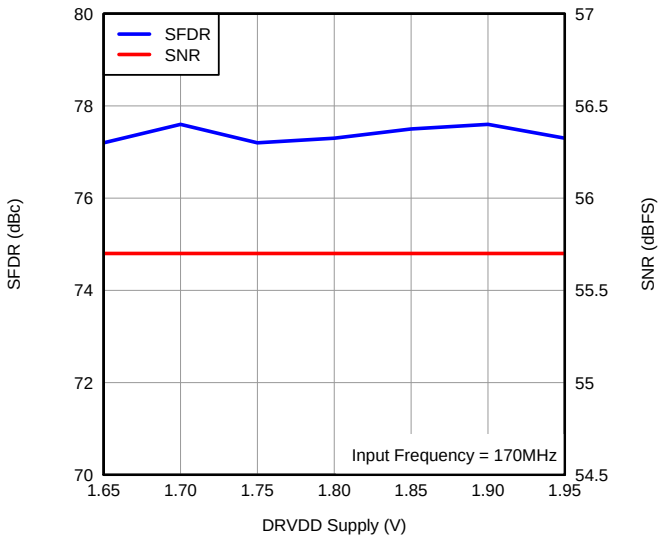


Figure 47.

PERFORMANCE ACROSS INPUT AMPLITUDE

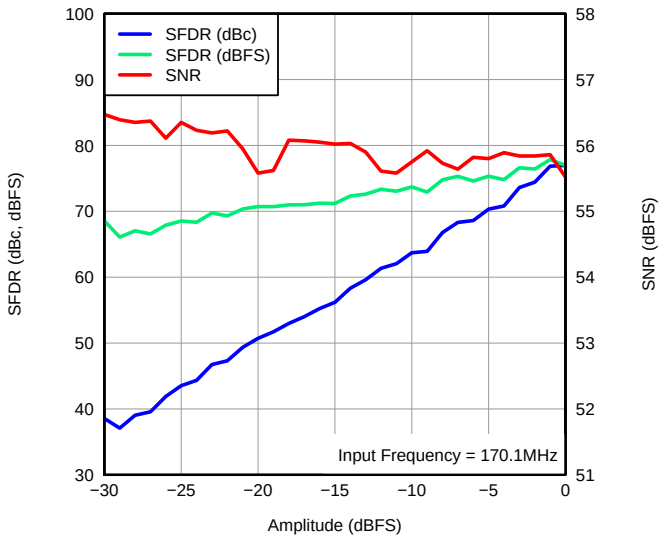


Figure 48.

TYPICAL CHARACTERISTICS: ADS58B19 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

PERFORMANCE ACROSS INPUT COMMON-MODE VOLTAGE

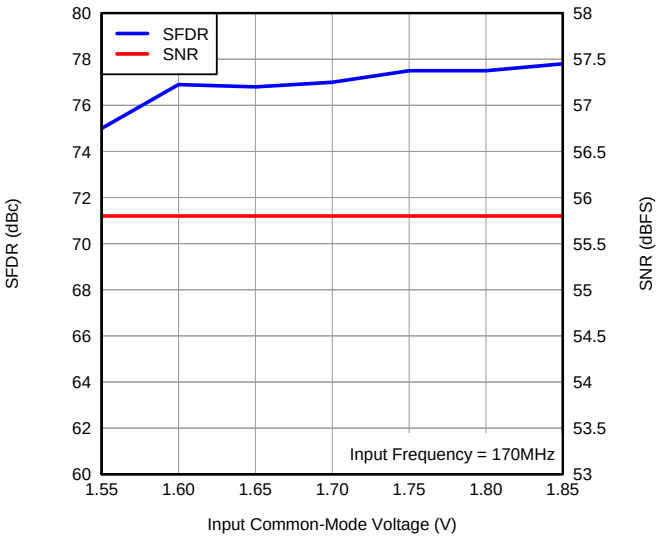


Figure 49.

PERFORMANCE ACROSS INPUT CLOCK AMPLITUDE

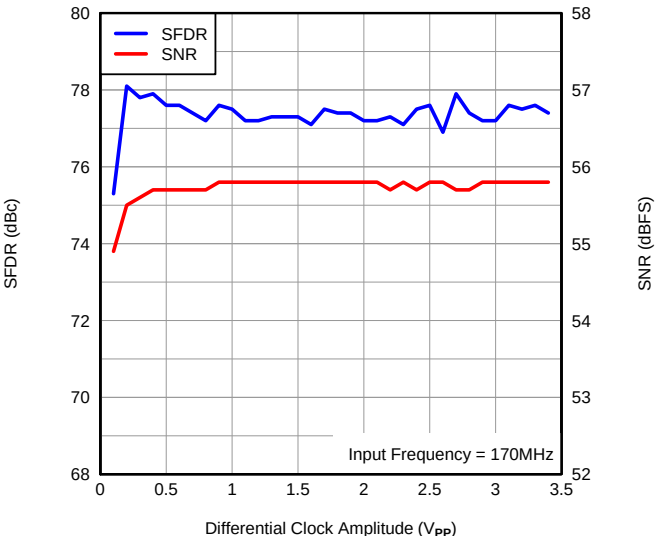


Figure 50.

PERFORMANCE ACROSS INPUT CLOCK DUTY CYCLE

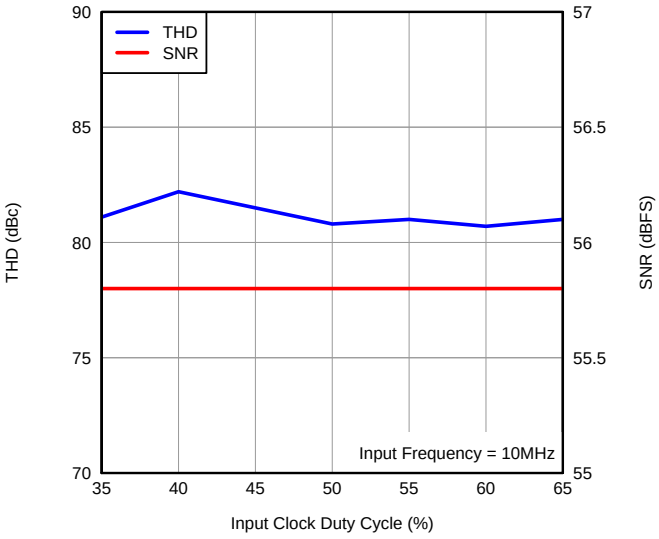


Figure 51.

ANALOG POWER vs SAMPLING FREQUENCY

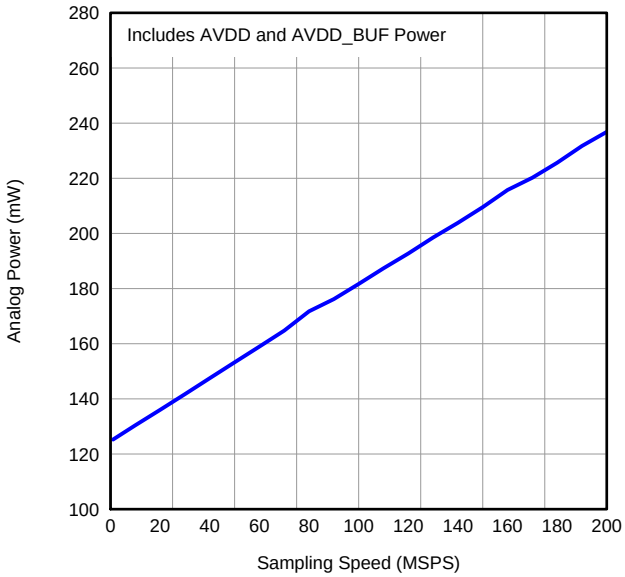


Figure 52.

TYPICAL CHARACTERISTICS: ADS58B19 (continued)

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

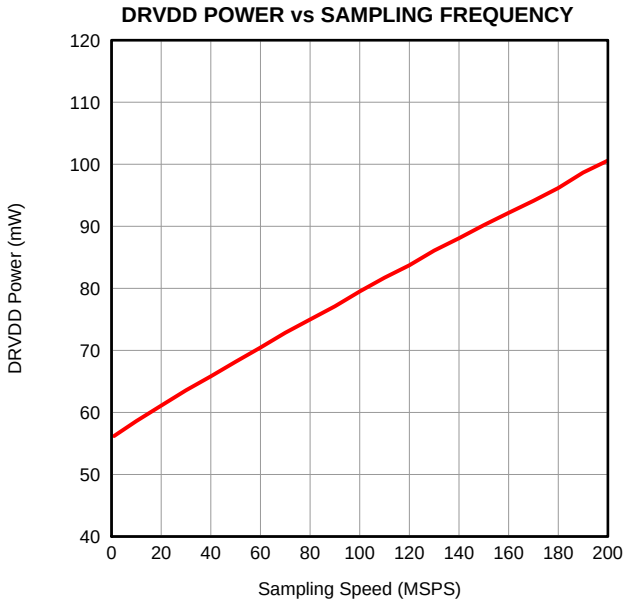


Figure 53.

TYPICAL CHARACTERISTICS: GENERAL

At +25°C, AVDD = 1.8V, AVDD_BUF = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

PSRR ACROSS FREQUENCY

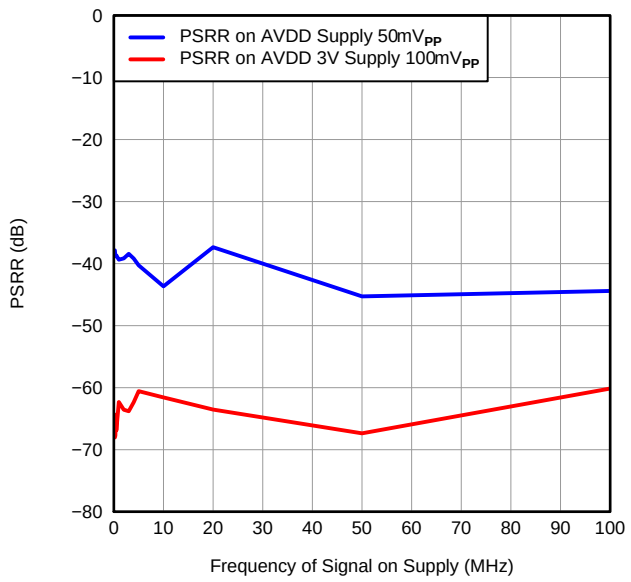


Figure 54.

ZOOMED VIEW OF SPECTRUM WITH PSRR SIGNAL

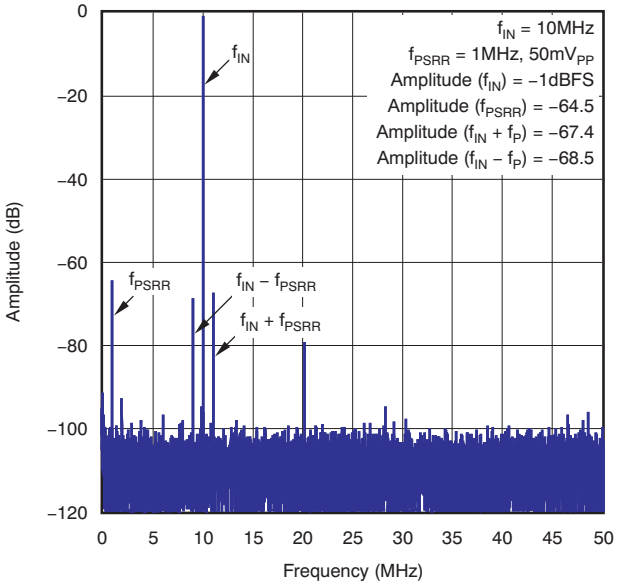


Figure 55.

CMRR ACROSS FREQUENCY

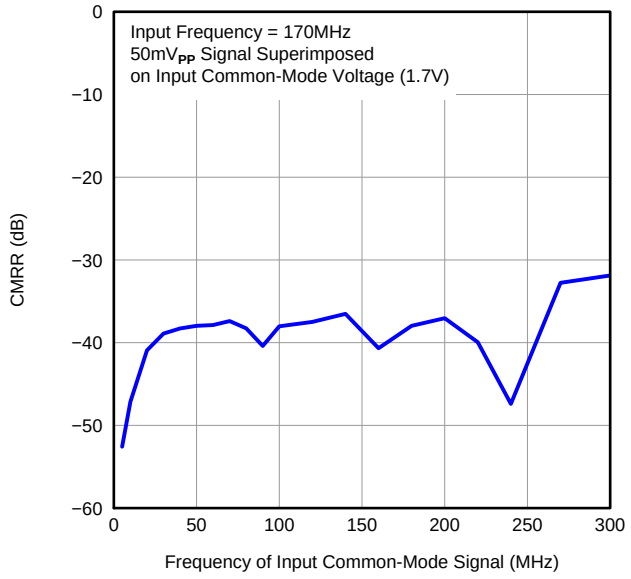


Figure 56.

SPECTRUM WITH CMRR SIGNAL

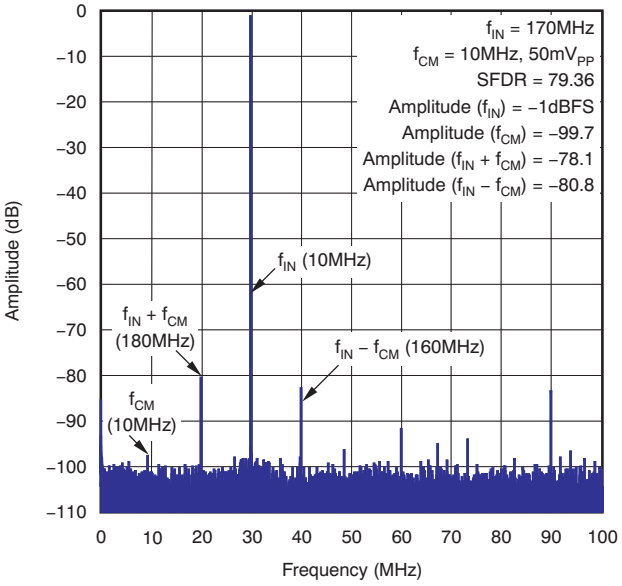


Figure 57.

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS58B18 and ADS58B19 are members of the ultralow power ADS4xxx analog-to-digital converter (ADC) family with integrated analog buffers and SNRBoost technology. The analog-to-digital conversion process is initiated by a rising edge of the external input clock when the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 10 clock cycles. The output is available as 11-bit data (ADS58B18) or 9-bit data (ADS58B19), in DDR LVDS or CMOS, and coded in either offset binary or binary twos complement format.

ANALOG INPUT

The analog inputs include an analog buffer (powered by the AVDD_BUF supply) that internally drives the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10kΩ dc resistance and 2pF input capacitance).

The buffer helps to isolate the external driving source from the switching currents of the sampling circuit. With a constant input impedance, the ADC is easier to drive and to reproduce data sheet measurements. For wideband applications (such as power amplifier linearization) the signal gain across frequency is more consistent. Spectral performance variation across the sampling frequency is also reduced.

The input common-mode is set internally using a 5kΩ resistor from each input pin to 1.7V, so the input signal can be ac-coupled to the pins. For a full-scale differential input, each input pin (INP, INM) must swing symmetrically between V_{CM} + 0.375V and V_{CM} – 0.375V, resulting in a $1.5V_{PP}$ differential input swing. The input sampling circuit has a high 3dB bandwidth that extends up to 550MHz (measured from the input pins to the sampled voltage). Figure 58 shows an equivalent circuit for the analog input.

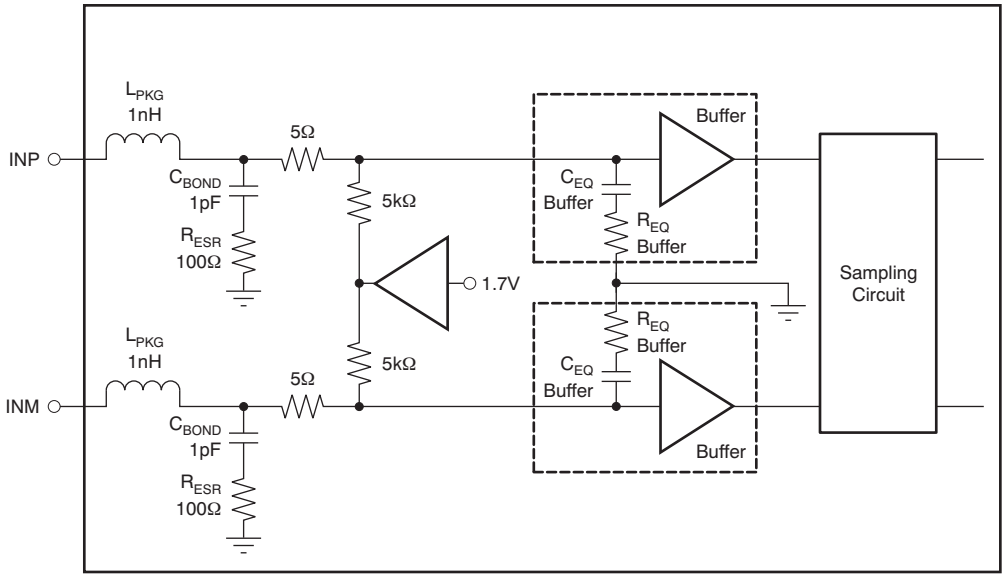


Figure 58. Analog Input Equivalent Circuit

Drive Circuit Requirements

The primary advantage of the buffered analog inputs is the isolation of the external drive source from the switching currents of the sampling circuit. The filtering of the glitches with an external R-C-R filter, as suggested for the ADS4149 family, is not required. Using a simple drive circuit, it is possible to obtain uniform performance over a wide frequency range.

For optimum performance, the analog inputs must be driven differentially. This configuration improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5Ω to 10Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 59 and Figure 60 show the differential impedance (Z_{IN} = R_{IN} || C_{IN}) seen by looking into the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1GHz.

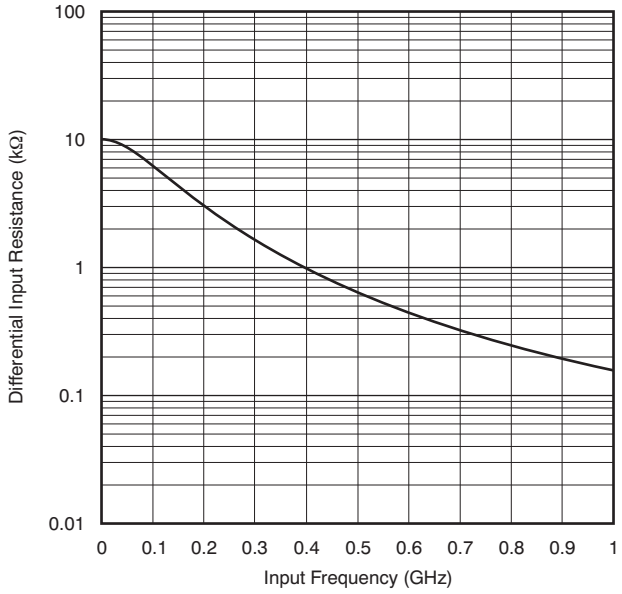


Figure 59. ADC Analog Input Resistance (R_{IN}) Across Frequency

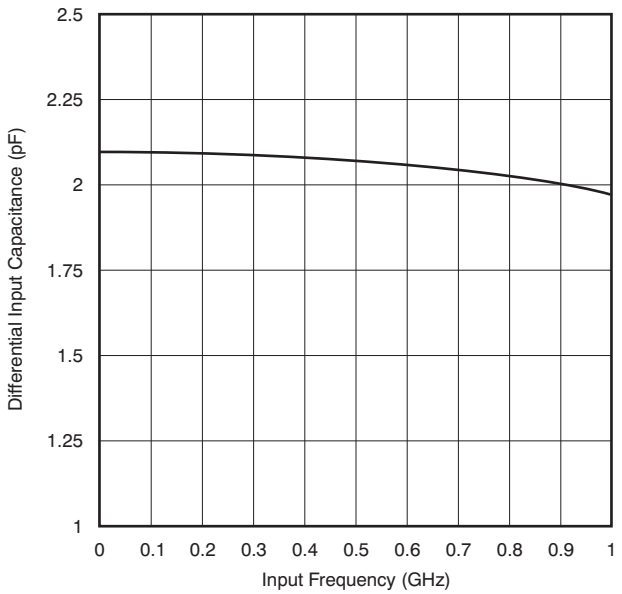


Figure 60. ADC Analog Input Capacitance (C_{IN}) Across Frequency

Driving Circuit

Two example driving circuit configurations are shown in Figure 61 and Figure 62—one optimized for low input frequencies and the other optimized for high input frequencies. Notice in both cases that the board circuitry is simplified compared to the non-buffered ADS4149.

In Figure 61, a single transformer is used and is suited for low input frequencies. To optimize even-harmonic performance at high input frequencies (greater than the first Nyquist), the use of back-to-back transformers is recommended (see Figure 62). Note that both drive circuits have been terminated by 50Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage.

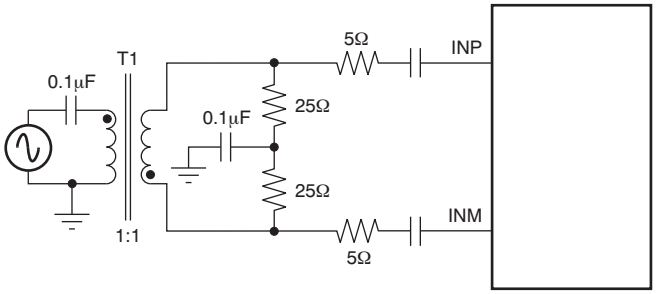


Figure 61. Drive Circuit for Low Input Frequencies

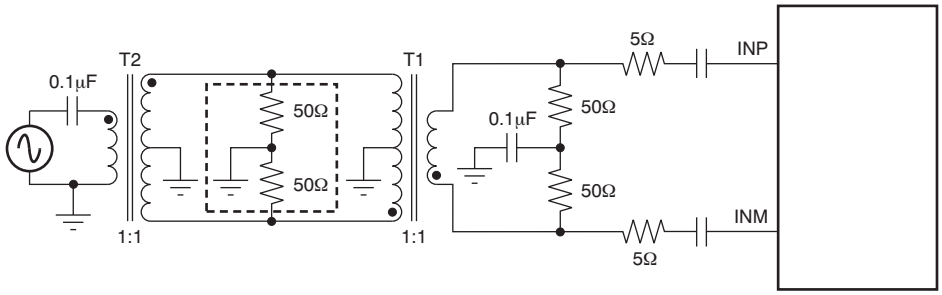
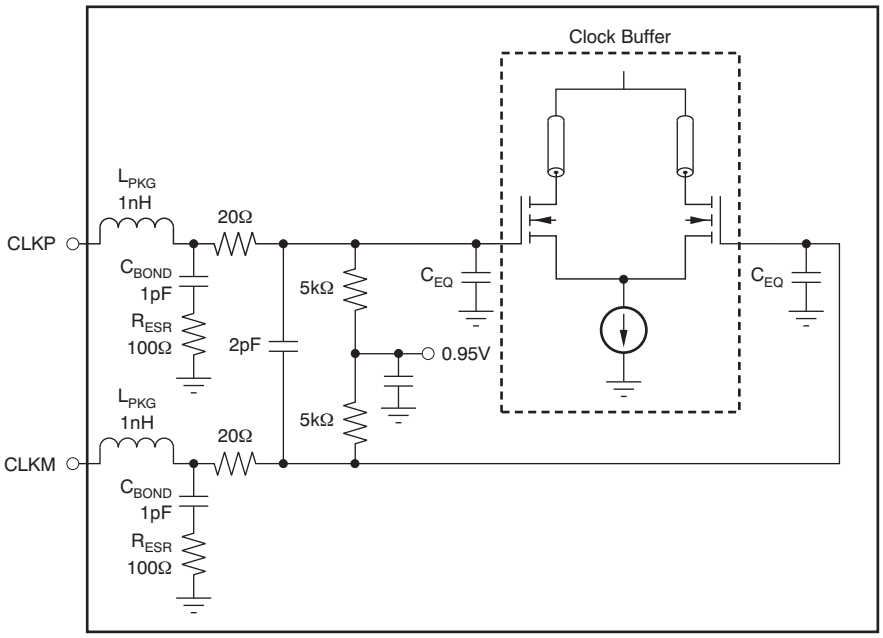


Figure 62. Drive Circuit for High Input Frequencies

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 61 and Figure 62. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50Ω (for a 50Ω source impedance).

CLOCK INPUT

The ADS58B18/19 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance. The common-mode voltage of the clock inputs is set to VCM using internal 5kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources. Figure 63 shows a circuit for the internal clock buffer.



NOTE: C_{EQ} is 1pF to 3pF and is the equivalent input capacitance of the clock buffer.

Figure 63. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1µF capacitor, as shown in Figure 64. For best performance, the clock inputs must be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input (see Figure 34). Figure 65 shows a differential circuit.

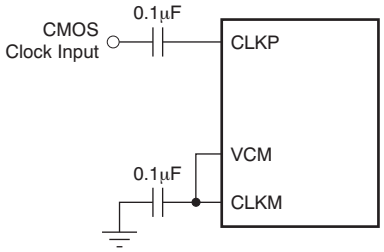


Figure 64. Single-Ended Clock Driving Circuit

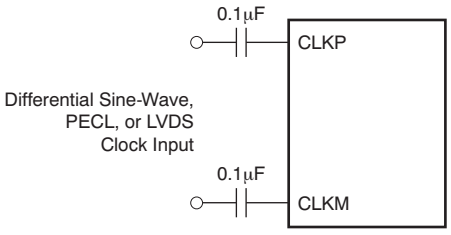


Figure 65. Differential Clock Driving Circuit

SNR ENHANCEMENT USING SNRBoost (ADS58B18 ONLY)

SNRBoost technology makes it possible to overcome SNR limitations resulting from quantization noise. Using SNRBoost, enhanced SNR can be obtained for any bandwidth (less than Nyquist or $f_S/2$; see Table 4). SNR improvement is achieved without affecting the default harmonic performance.

SNRBoost can be enabled using the SNRBoost_EN pin or via register bits. When SNRBoost is enabled, the noise floor in the spectrum acquires a typical *bathtub* shape; see Figure 66. The bathtub is centered around a specific frequency (called *center frequency*). The center frequency is located midway between two corner frequencies that are specified by the SNRBoost coefficients (register bits SNRBoost Coeff1 and SNRBoost Coeff2).

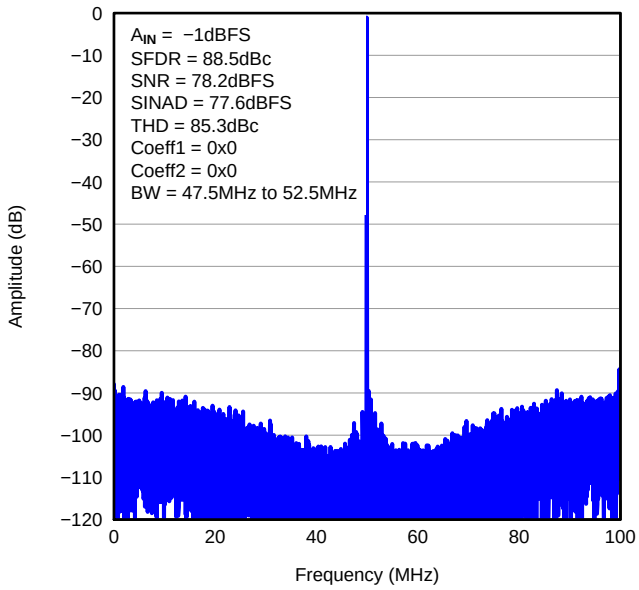


Figure 66. Spectrum with SNRBoost Enabled

Table 9 shows the relation between each coefficient and its corner frequency. By choosing appropriate coefficients, the bathtub can be positioned over the frequency range of 0 to $f_S/2$ (Table 10 shows some examples). By positioning the bathtub within the desired signal band, SNR improvement can be achieved (see Table 4). Note that as the bandwidth is increased, the amount of SNR improvement reduces.

After a reset, the device is in low-latency disabled mode. To use the SNRBoost:

- For the required bathtub position, write the appropriate coefficients in the SNRBoost Coeff1 and SNRBoost Coeff2 registers
- SNRBoost can be enabled or disabled using the SNRBoost_EN digital input pin. This pin has higher priority over the SNRBoost Enable1 and SNRBoost Enable2 register bits
- To use the enable register bits, set the override bit (OVER_RIDE SNRBoost pin).

Table 9. Setting the Corner Frequency

SNRBoost COEFFICIENT VALUE	NORMALIZED CORNER FREQUENCY (f/f_S)	SNRBoost COEFFICIENT VALUE	NORMALIZED CORNER FREQUENCY (f/f_S)
7	0.42	F	0.23
6	0.385	E	0.21
5	0.357	D	0.189
4	0.333	C	0.167
3	0.311	B	0.143
2	0.29	A	0.115
1	0.27	9	0.08
0	0.25	8	0

Table 10. Positioning the Corner Frequency

SNRBoost COEFFICIENT1 (SNRBoost Coeff1)	NORMALIZED CORNER FREQUENCY1 (f/f_S)	SNRBoost COEFFICIENT1 (SNRBoost Coeff2)	NORMALIZED CORNER FREQUENCY2 (f/f_S)	CENTER FREQUENCY
0	0.25	0	0.25	$f_S \times 0.25$
F	0.23	1	0.27	$f_S \times 0.25$
6	0.385	2	0.29	$f_S \times 0.3375$
D	0.189	B	0.143	$f_S \times 0.166$
9	0.08	7	0.42	$f_S \times 0.25$

GAIN FOR SFDR/SNR TRADE-OFF

The ADS58B18/19 include gain settings that can be used to get improved SFDR performance. The gain is programmable from 0dB to 3.5dB (in 0.5dB steps) using the GAIN register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 11.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5dB and 1dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used to trade-off between SFDR and SNR.

After a reset, the device is in low-latency disabled mode and gain is enabled with 0dB gain. For other gain settings, program the GAIN bits.

Table 11. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V_{PP})
0	Default after reset	1.5
0.5	Programmable gain	1.41
1		1.33
1.5		1.26
2		1.19
2.5		1.12
3		1.06
3.5		1

OFFSET CORRECTION

The ADS58B18/19 has an internal offset corretion algorithm that estimates and corrects dc offset up to ±10mV. The correction can be enabled using the ENABLE OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 12.

Table 12. Time Constant of Offset Correction Loop

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (sec)(1)
0000	1M	5ms
0001	2M	10.5ms
0010	4M	21ms
0011	8M	42ms
0100	16M	84ms
0101	32M	168ms
0110	64M	336ms
0111	128M	671ms
1000	256M	1.34s
1001	512M	2.68s
1010	1G	5.37s
1011	2G	10.7s
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency, f_S = 250MSPS.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 1. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

After a reset, the device is in low-latency disabled mode. To use offset correction, set ENABLE OFFSET CORR to '1' and program the required time constant.

POWER DOWN

The ADS58B18/19 has three power-down modes: power-down global, standby, and output buffer disable.

Power-Down Global

In this mode, the entire chip (including the ADC, internal reference, and the output buffers) are powered down, resulting in reduced total power dissipation of about 10mW. The output buffers are in a high-impedance state. The wake-up time from the global power-down to data becoming valid in normal mode is typically 100µs. To enter the global power-down mode, set the PDN GLOBAL register bit.

Standby

In this mode, only the ADC is powered down and the internal references are active, resulting in a fast wake-up time of 5µs. The total power dissipation in standby mode is approximately 185mW. To enter the standby mode, set the STANDBY register bit.

Output Buffer Disable

The output buffers can be disabled and put in a high-impedance state; wakeup time from this mode is fast, approximately 100ns. This can be controlled using the PDN OBUF register bit or using the OE pin.

Input Clock Stop

In addition, the converter enters a low-power mode when the input clock frequency falls below 1MSPS. The power dissipation is approximately 80mW.

POWER-SUPPLY SEQUENCE

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated in the device. Externally, they can be driven from separate supplies or from a single supply.

DIGITAL OUTPUT INFORMATION

The ADS58B18/19 provide either 11-bit or 9-bit data and an output clock synchronized with the data.

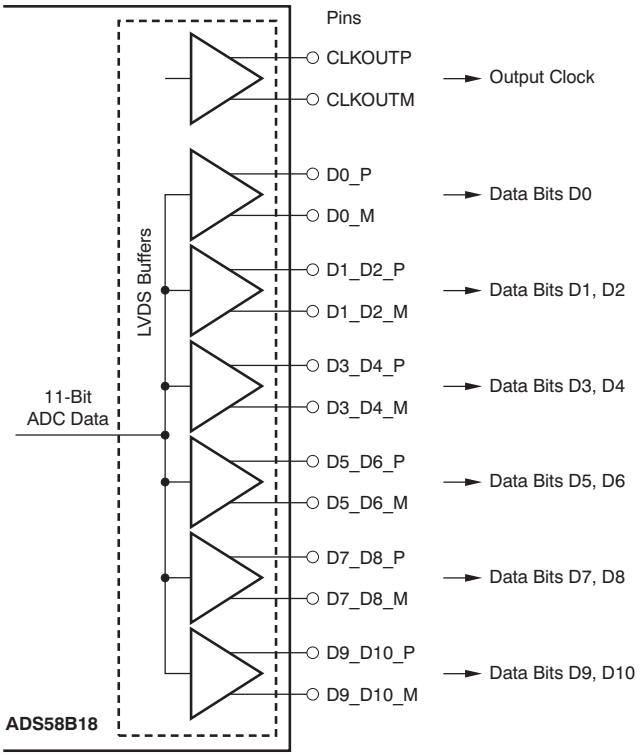
Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. The output can be selected using the LVDS CMOS serial interface register bit or using the DFS pin. The DFS pin has higher priority for deciding the type of interface, unless the LVDS CMOS override bit is set.

DDR LVDS Outputs

In this mode, the data bits and clock are output using low voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 67 and Figure 68. Two bit order options are available: bit-wise sequence (default) and byte-wise sequence. Byte-wise sequence can be programmed with the BYTE-WISE En Register bit.

Figure 67. ADS58B18 LVDS Outputs



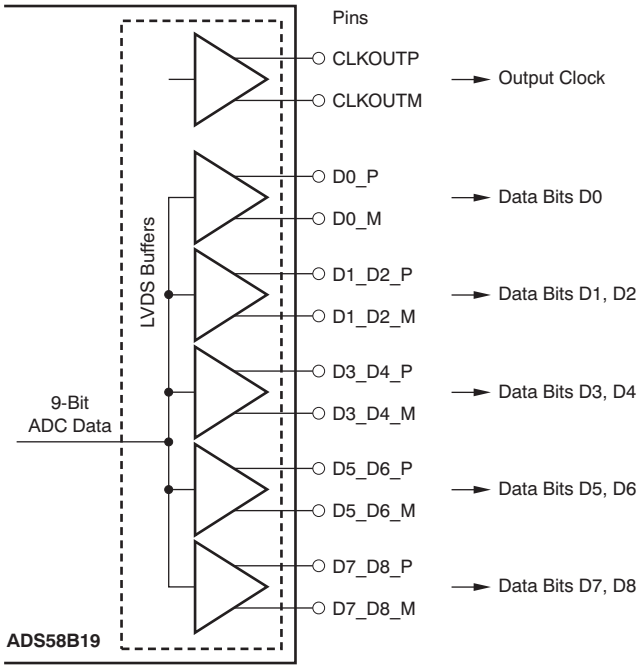


Figure 68. ADS58B19 LVDS Outputs

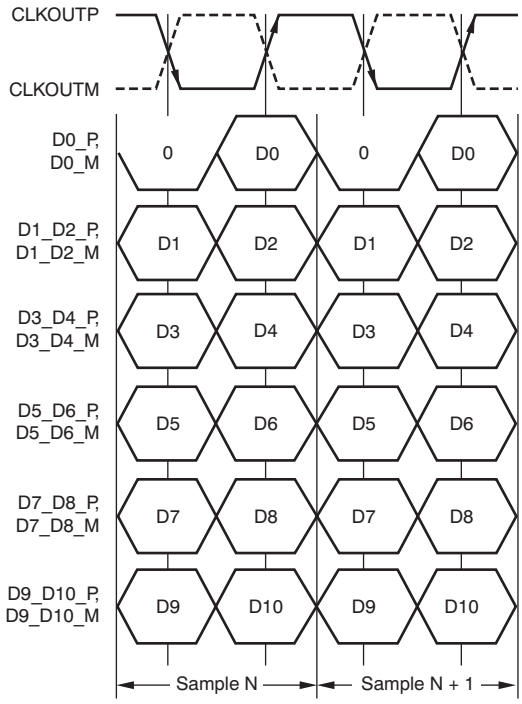
Bit-Wise Sequence

Even data bits (D0, D2, D4, etc) are output at the rising edge of CLKOUTP and the odd data bits (D1, D3, D5, etc) are output at the falling edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all the data bits; see Figure 69.

Byte-Wise Sequence

In the ADS58B18, data bits D[0:4] are output at the falling edge of CLKOUTP and data bits D[5:10] are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all the data bits; see Figure 70.

In the ADS58B19, data bits D[0:3] are output at the falling edge of CLKOUTP and data bits D[4:8] are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all the data bits; see Figure 71.



(1) Bits D9 and D10 are only available in the ADS58B18.

Figure 69. Bit-Wise Sequence (Only with DDR LVDS Interface)

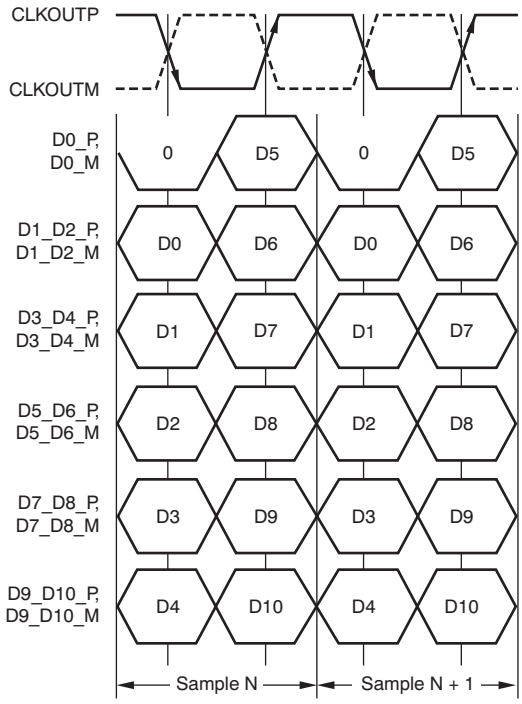


Figure 70. ADS58B18 Byte-Wise Sequence (Only with DDR LVDS Interface)

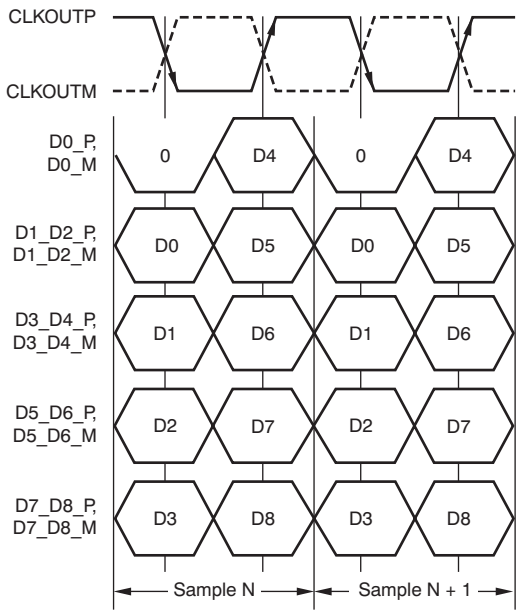


Figure 71. ADS58B19 Byte-Wise Sequence (Only with DDR LVDS Interface)

LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in Figure 72. After reset, the buffer presents an output impedance of 100Ω to match with the external 100Ω termination.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50Ω differential termination. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.

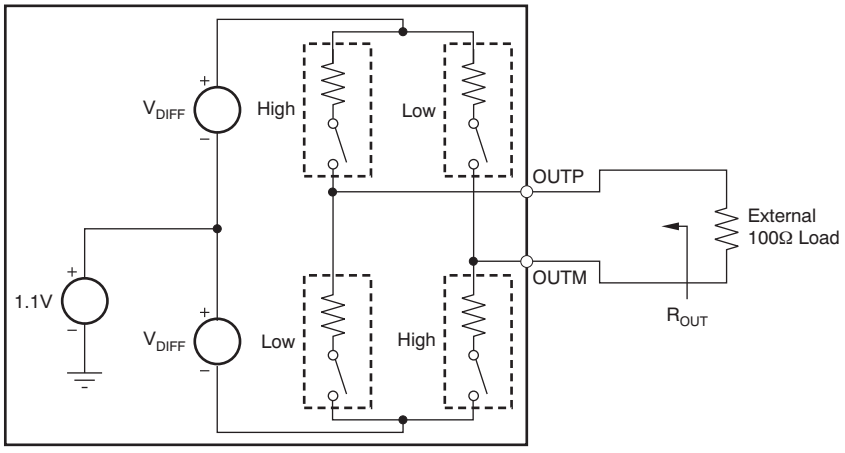


Figure 72. LVDS Buffer Equivalent Circuit

Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as the CMOS voltage level, for every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. Figure 73 depicts the CMOS output interface.

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs and degrade SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this degradation, the CMOS output buffers are designed with controlled drive strength. The default drive strength ensures a wide data stable window (even at 250MSPS) is provided so the data outputs have minimal load capacitance. It is recommended to use short traces (1 to 2 inches, or 2,54cm to 5,08cm) terminated with less than 5pF load capacitance, as shown in Figure 74.

For sampling frequencies greater than 200MSPS, it is recommended to use an external clock to capture data. The delay from input clock to output data and the data valid times are specified for higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture data.

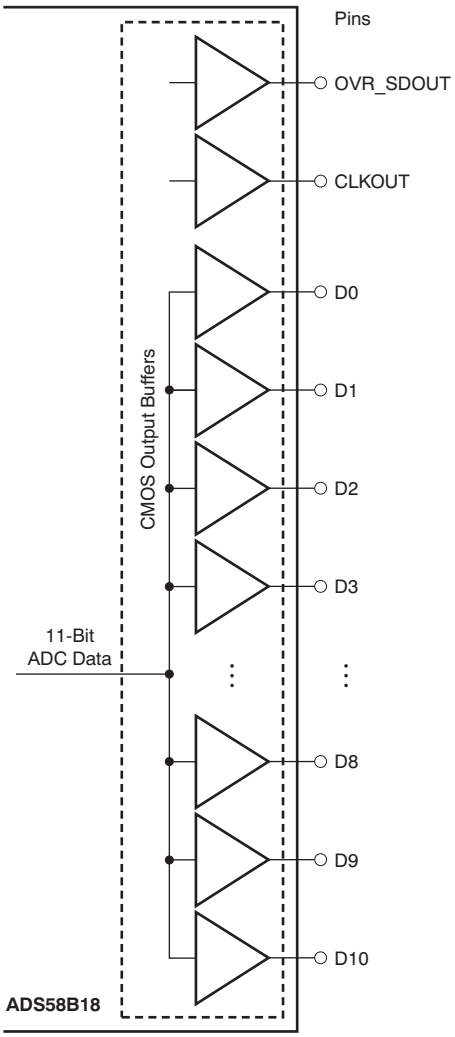


Figure 73. CMOS Output Interface

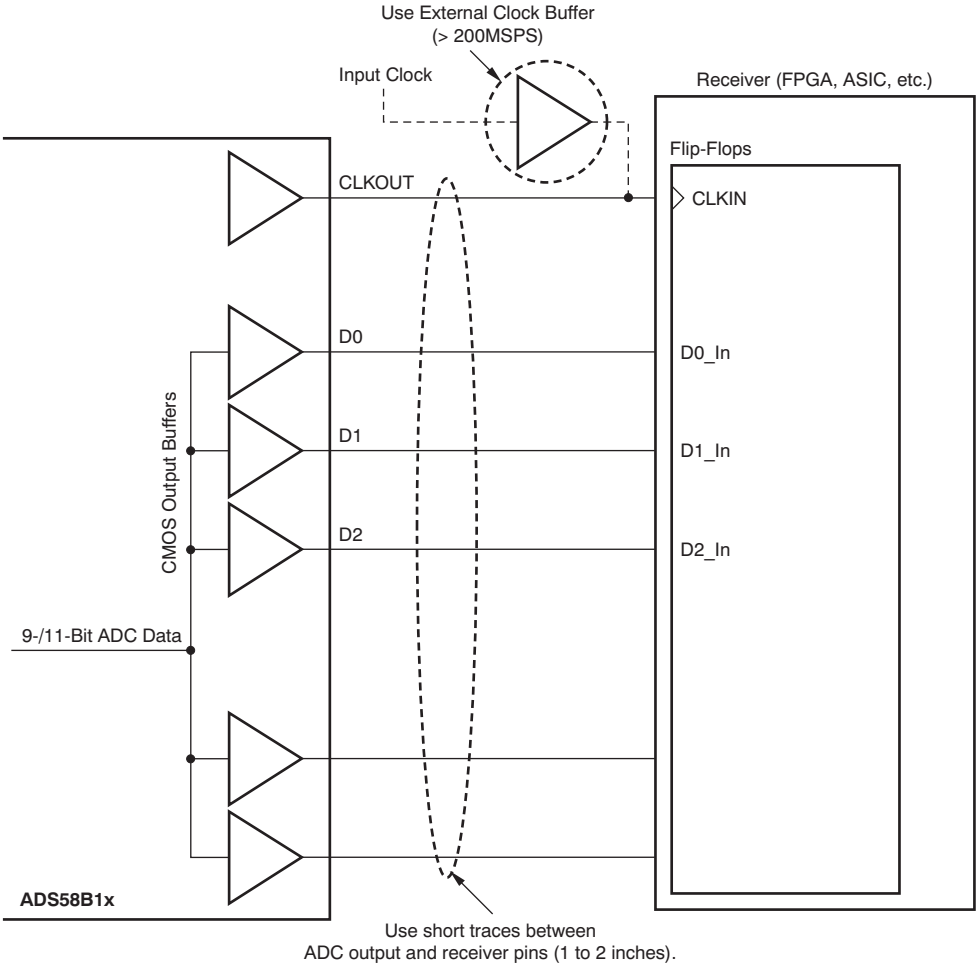


Figure 74. CMOS Capture Example

CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between '0' and '1' every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital Current as a Result of CMOS Output Switching = $C_L \times DRVDD \times (N \times f_{AVG})$

where:

C_L = load capacitance,

$N \times F_{AVG}$ = average number of output bits switching. (1)

Input Over-Voltage Indication (OVR_SDOUT Pin)

The device has an OVR_SDOUT pin that provides information about analog input overload (as long as the READOUT register bit is '0'). When the READOUT bit is '1', it functions as a serial readout pin.

At any clock cycle, if the sampled input voltage exceeds the positive or negative full-scale range, the OVR pin goes high. The OVR remains high as long as the overload condition persists. The OVR pin is a CMOS output buffer (running off DRVDD supply), independent of the type of output data interface (DDR LVDS or CMOS).

For a positive overload, the D[10:0] output data bits are 7FFh in offset binary output format and 3FFh in twos complement output format. For a negative input overload, the output code is 000h in offset binary output format and 400h in twos complement output format.

Output Data Format

Two output data formats are supported: twos complement and offset binary. They can be selected using the DATA FORMAT serial interface register bit or using the DFS pin.

BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS414x, ADS412x EVM User Guide* (SLWU067) for details on layout and grounding.

Supply Decoupling

Because the ADS58B18/19 already include internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise, so the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically internally connected to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271), both available for download at the TI web site (www.ti.com).

DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3dB with respect to the low-frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (2)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (3)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB) – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{4}$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$\text{THD} = 10\text{Log}^{10} \frac{P_S}{P_N} \tag{5}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR) – DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \tag{6}$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \tag{7}$$

Crosstalk (only for multi-channel ADCs) – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2010) to Revision D **Page**

- Changed documet status to production data 1
- Updated status of ADS58B19 to production data throughout document 1
- Updated document format to current standards 1
- Changed Clock Input, *Input clock sample rate* parameters for both ADS58B18 and ADS58B19 in Recommended Operating Conditions table 3
- Added footnote 3 to Recommended Operating Conditions table 3
- Changed conditions of *ADC latency* parameter in Timing Requirements table 15
- Deleted footnote 7 from Timing Requirements table 15
- Deleted footnote 10 in Timing Requirements tableα 16
- Deleted table 2 (CMOS Timing Across Sampling Frequencies, withe respect to output clock) and table 4 (CMOS Timing Across Sampling Frequencies, withe respect to input clock) 17
- Changed titles of Table 2 and Table 3 17
- Updated Figure 8 18
- Changed description of logic high in Table 6 20
- Updated bit D3 of registers 25 and 42 and added register DF to Table 8 23
- Changed bit 3 and description of bits 2 to 0 in Register Address 25h 25
- Changed description of bit 4 in Register Address 3Dh 26
- Changed bit 3 of register address 42h 28
- Added Register Address DFh to *Description of Serial Registers* section 31
- Updated conditions of Typical Characteristics: ADS58B18 32
- Updated Figure 36 37
- Updated conditions of Typical Characteristics: ADS58B19 38
- Updated Figure 53 42
- Updated conditions of Typical Characteristics: General 43
- Deleted *Digital Functions and Low-Latency Mode* section 48
- Changed SNRBoost enable description in *SNR Enhancement Using SNRBoost* section 49
- Changed reset description in *Gain for SFDR/SNR Trade-Off* section 50
- Changed reset description in *Offset Correction* section 51

Changes from Revision B (July 2010) to Revision C **Page**

- Changed Analog Inputs, *Input common-mode voltage* typical specification in Recommended Operating Conditions table 3
- Added Clock Input, *Input clock duty cycle* minimum and maximum specifiations to Recommended Operating Conditions table 3
- Updated format of Typical Characteristics graphs 32

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS58B18IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58B18
ADS58B18IRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58B18
ADS58B18IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58B18
ADS58B18IRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58B18
ADS58B19IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58B19
ADS58B19IRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58B19
ADS58B19IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58B19
ADS58B19IRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58B19

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

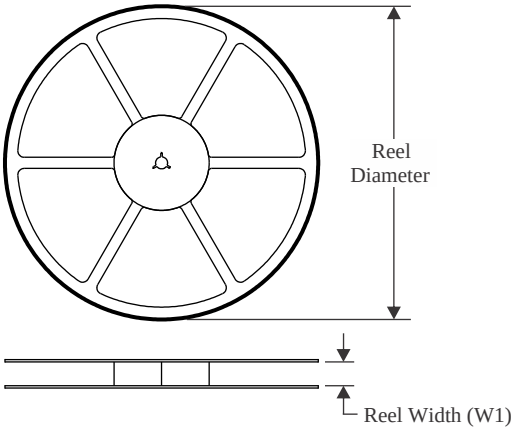
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

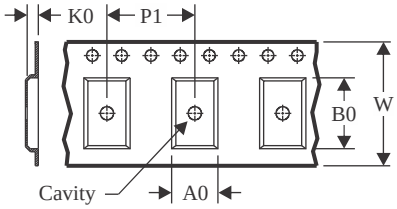
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

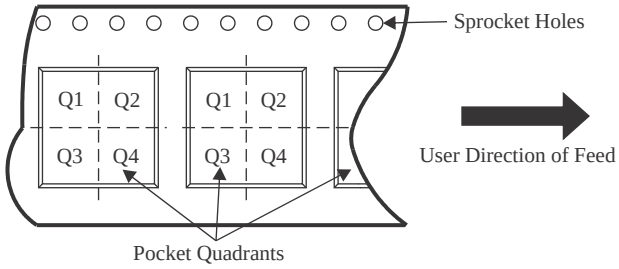


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

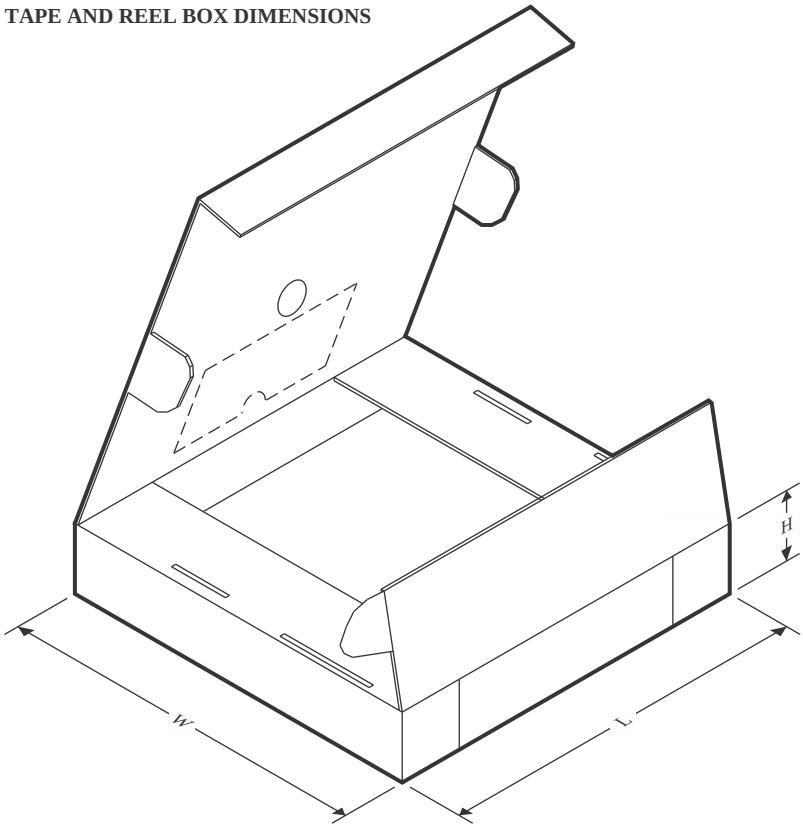
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS58B18IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS58B19IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS58B18IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS58B19IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0

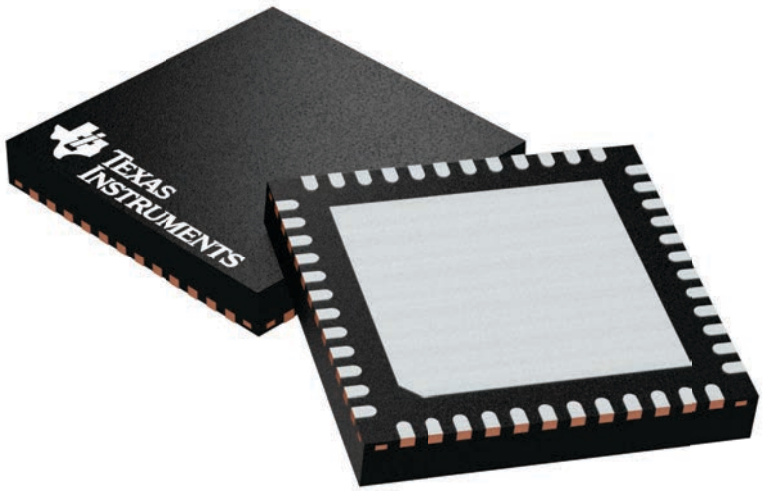
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

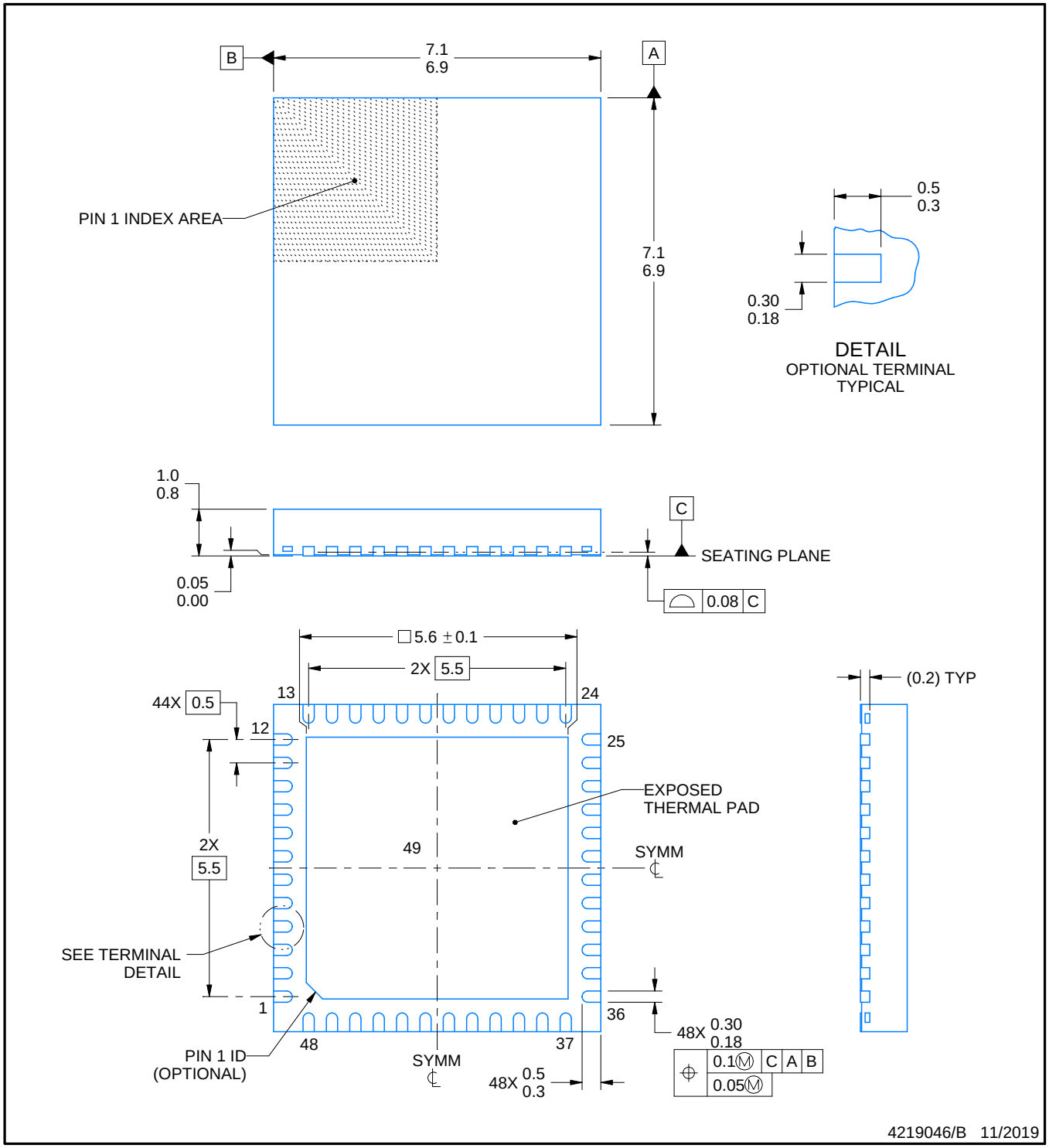
4224671/A

PACKAGE OUTLINE

RGZ0048D

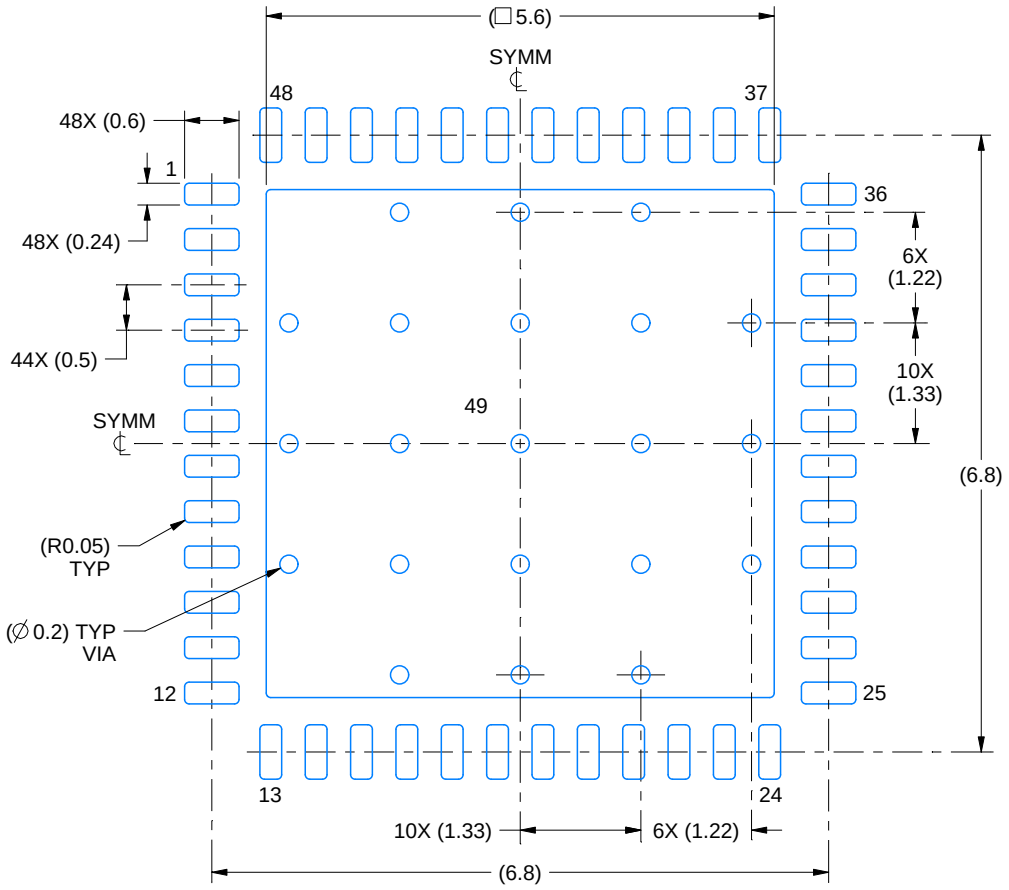
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

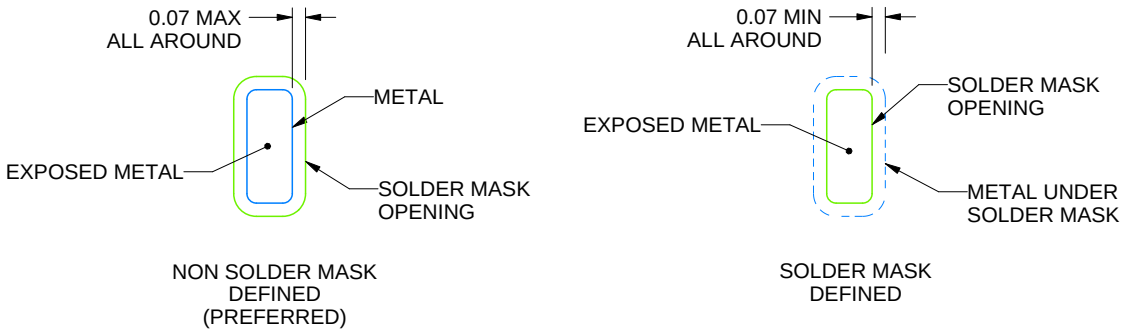


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

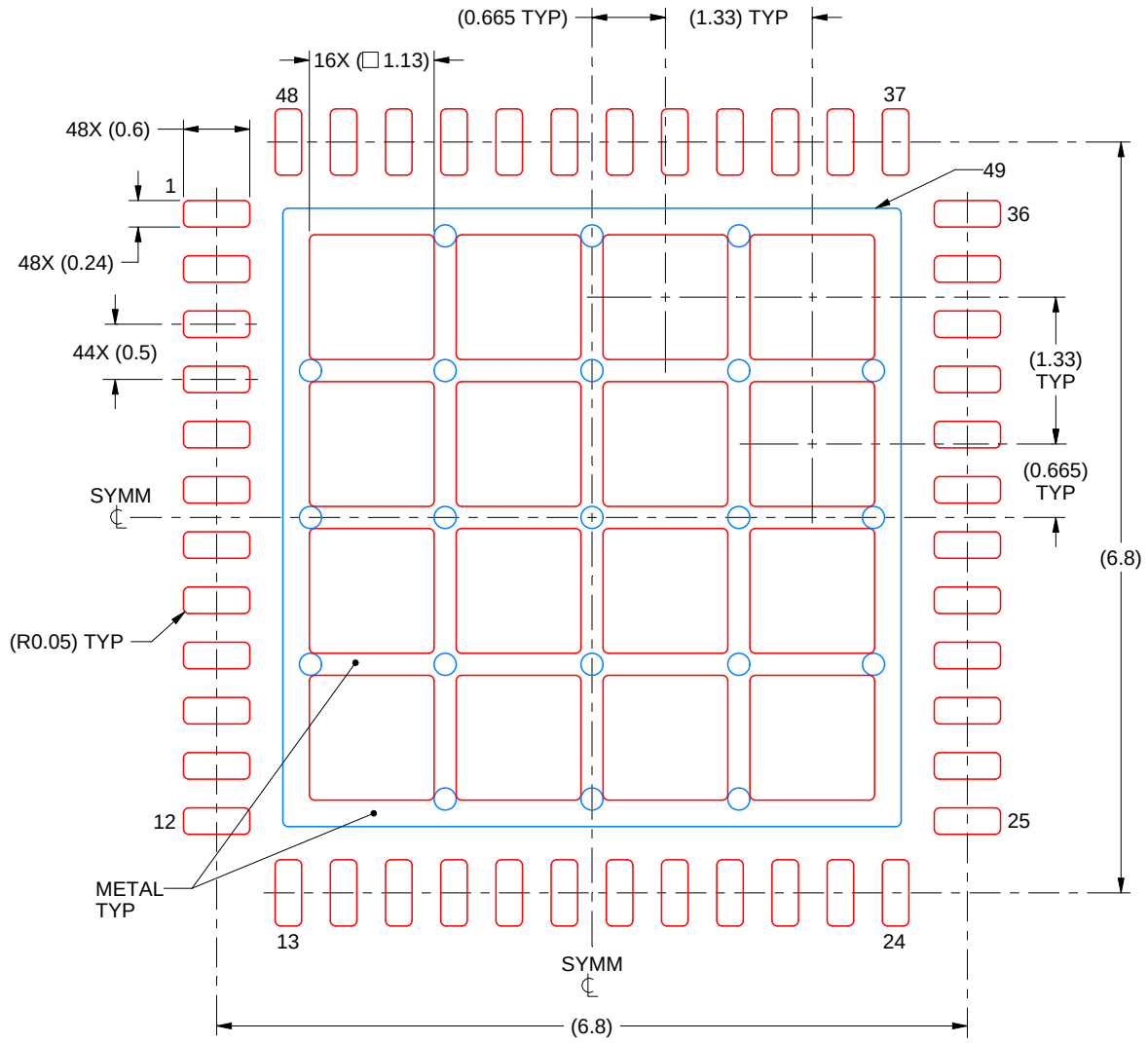


SOLDER MASK DETAILS

4219046/B 11/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4219046/B 11/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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