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## 13-BIT 210-MSPS ANALOG-TO-DIGITAL CONVERTER

#### **FEATURES**

- Controlled Baseline
  - One Assembly
  - One Test Site
  - One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree<sup>(1)</sup>
- 13-Bit Resolution
- 210-MSPS Sample Rate
- SNR = 69 dBc at 100-MHz IF and 210 MSPS
- SFDR = 76 dBc at 100-MHz IF and 210 MSPS
- SNR = 68.1 dBc at 230-MHz IF and 210 MSPS
- SFDR = 74 dBc at 230-MHz IF and 210 MSPS
- 2.2-V<sub>PP</sub> Differential Input Voltage
- Fully Buffered Analog Inputs
- 5-V Analog Supply Voltage
- LVDS Compatible Outputs
- Total Power Dissipation: 2 W
- Offset Binary Output Format

- TQFP-80 PowerPAD™ Package
- Pin Compatible With the ADS5444
- Military Temperature Range = -55°C to 125°C
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

#### **APPLICATIONS**

- Test and Measurement
- Software-Defined Radio
- Multichannel Base Station Receivers
- Base Station Tx Digital Predistortion
- Communications Instrumentation

#### **RELATED PRODUCTS**

- ADS5424 14-Bit, 105-MSPS ADC
- ADS5423 14-Bit, 80-MSPS ADC
- ADS5444 13-Bit, 250-MSPS ADC

## **DESCRIPTION**

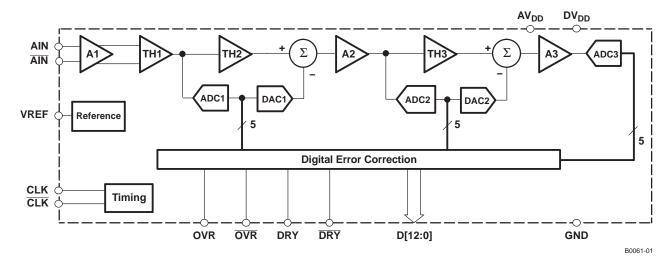
The ADS5440 is a 13-bit 210-MSPS analog-to-digital converter (ADC) that operates from a 5-V supply, while providing LVDS-compatible digital outputs from a 3.3-V supply. The ADS5440 input buffer isolates the internal switching of the onboard track and hold (T&H) from disturbing the signal source. An internal reference generator is also provided to further simplify the system design. The ADS5440 has outstanding low noise and linearity over input frequency.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.





The ADS5440 is available in an 80-pin TQFP PowerPAD™ package. The ADS5440 is built on a state-of-the-art Texas Instruments complementary bipolar process (BiCom3X) and is specified over the full military temperature range (–55°C to 125°C).





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### PACKAGING/ORDERING INFORMATION(1)

Product	Package Lead	Package Designator <sup>(1)</sup>	Specified Temperature Range	Package Marking	Ordering Number	Transport Media, Quantity
ADS5440	HTQFP-80 <sup>(2)</sup> PowerPAD	PFP	–55°C to 125°C	ADS5440M-EP	ADS5440MPFPEP	Tray, 96

<sup>1)</sup> For the most current product and ordering information, see the Package Option Addendum located at the end of this data sheet.

#### **ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE/UNIT
Cumply valtage	AV <sub>DD</sub> to GND	6 V
Supply voltage	DRV <sub>DD</sub> to GND	5 V
Analog input to GN	ND	-0.3 V to AV <sub>DD</sub> + 0.3 V
Clock input to GNI	)	-0.3 V to AV <sub>DD</sub> + 0.3 V
CLK to CLK		±2.5 V
Digital data output	to GND	-0.3 V to DRV <sub>DD</sub> + 0.3 V
Operating tempera	ature range	−55°C to 125°C
Maximum junction	temperature	150°C
Storage temperatu	ire range	-65°C to 150°C
ESD Human Body	Model (HBM)	2.5 kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.

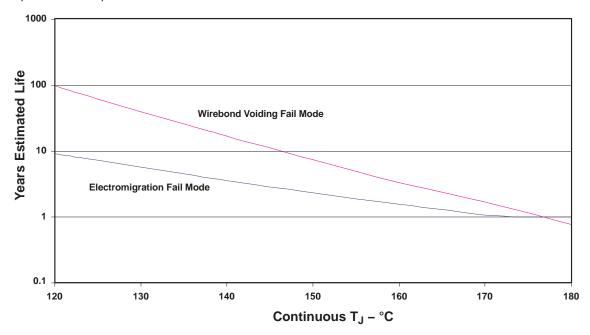


Figure 1. ADS5440MPFPEP Operating Life Derating Chart

<sup>(2)</sup> Thermal pad size: 7,5 mm x 7,5 mm (typ)



## THERMAL CHARACTERISTICS(1)

PARAMETER	TEST CONDITIONS	TYP	UNIT
	Soldered slug, no airflow	21.7	
0	Soldered slug, 250-LFPM airflow	15.4	°C/W
$\theta_{JA}$	Unsoldered slug, no airflow		°C/VV
	Unsoldered slug, 250-LFPM airflow	43.4	
$\theta_{JC}$	Bottom of package (heatslug)	2.99	°C/W

<sup>(1)</sup> Using 36 thermal vias (6 x 6 array). See the Section 2.

## **RECOMMENDED OPERATING CONDITIONS**

			MIN	NOM	MAX	UNIT	
SUPPLIE	S						
$AV_{DD}$	Analog supply voltage		4.75	5	5.25	V V V V V V V V V V V V V V V V V V V	
$DRV_DD$	Output driver supply voltage		3	3.3	3.6	V	
ANALOG	INPUT						
	Differential input range			2.2		V <sub>PP</sub>	
V <sub>CM</sub>	Input common mode			2.4		V	
CLOCK II	NPUT						
1/t <sub>C</sub>	ADCLK input sample rate (sine wave)	10			210	MSPS	
	Clock amplitude, differential sine wave			3		$V_{PP}$	
	Clock duty cycle			50%			
T <sub>A</sub>	Open free air-temperature		<b>-</b> 55		125	°C	

#### **ELECTRICAL CHARACTERISTICS**

Min, Typ, and Max values at  $T_A = 25$ °C, full temperature range is  $T_{MIN} = -55$ °C to  $T_{MAX} = 125$ °C, sampling rate = 210 MSPS, 50% clock duty cycle,  $AV_{DD} = 5$  V,  $DRV_{DD} = 3.3$  V, -1-dBFS differential input, and 3- $V_{PP}$  differential clock (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution				13		Bits
ANALO	OG INPUTS						
	Differential input range				2.2		$V_{pp}$
	Differential input resistance (DC)				1		kΩ
	Differential input capacitance				1.5		pF
	Analog input bandwidth				800		MHz
INTERI	NAL REFERENCE VOLTAGE						
VREF	Reference voltage				2.4		V
DYNAN	IIC ACCURACY						
	No missing codes				Assured		
DNL	Differential linearity error	f <sub>IN</sub> = 10 MHz		-1	±0.4	1	LSB
INL	Internal linearity, annua	£ 40 MH=	T <sub>A</sub> = 25°C	-2.2	± 0.9	2.2	LSB
IINL	Integral linearity error	f <sub>IN</sub> = 10 MHz	Full temp range	-3.2	±0.9	3.2	LOD
	Offset error			-11		11	mV
	Offset temperature coefficient				0.0005		mV/°C
	Gain error			-5		5	%FS
	Gain temperature coefficient				-0.02		Δ%/°C
	PSRR	f <sub>IN</sub> = 100 MHz			1		mV/V



Min, Typ, and Max values at  $T_A = 25^{\circ}$ C, full temperature range is  $T_{MIN} = -55^{\circ}$ C to  $T_{MAX} = 125^{\circ}$ C, sampling rate = 210 MSPS, 50% clock duty cycle,  $AV_{DD} = 5$  V,  $DRV_{DD} = 3.3$  V, -1-dBFS differential input, and 3- $V_{PP}$  differential clock (unless otherwise noted)

	PARAMETER	TEST C	MIN	TYP	MAX	UNIT				
POWER	RSUPPLY					1				
I <sub>AVDD</sub>	Analog supply current				340	410	mA			
I <sub>DRVDD</sub>	Output buffer supply current	$V_{IN}$ = full scale, $f_{IN}$ = 100	MHz, $F_S = 210 \text{ MSPS}$		80	100	mA			
	Power dissipation				2	2.35	W			
DYNAN	IIC AC CHARACTERISTICS			+						
		f <sub>IN</sub> = 10 MHz		69.8						
		f <sub>IN</sub> = 70 MHz	T		69.2					
		f <sub>IN</sub> = 100 MHz	$T_A = 25^{\circ}C$	67.5	69					
SNR	Signal-to-noise ratio		Full temp range	66	69		dBc			
SIVIX	Signal-to-noise ratio	f <sub>IN</sub> = 170 MHz			68.3		ubc			
		f <sub>IN</sub> = 230 MHz			68					
		f <sub>IN</sub> = 300 MHz		66.9						
		f <sub>IN</sub> = 400 MHz			65					
		f <sub>IN</sub> = 10 MHz			84					
		f <sub>IN</sub> = 70 MHz			77					
		f 100 MHz	T <sub>A</sub> = 25°C	70	76					
CEDD	Spurious free dynamic range	f <sub>IN</sub> = 100 MHz	Full temp range	64.5	76		dDa			
SFDR	Spurious free dynamic range	f <sub>IN</sub> = 170 MHz			74		dBc			
		f <sub>IN</sub> = 230 MHz			74					
		f <sub>IN</sub> = 300 MHz		69						
		f <sub>IN</sub> = 400 MHz			64					
		f <sub>IN</sub> = 10 MHz		96						
		f <sub>IN</sub> = 70 MHz			83 87 76					
		f <sub>IN</sub> = 100 MHz								
HD2	Second harmonic	f <sub>IN</sub> = 170 MHz								
		f <sub>IN</sub> = 230 MHz		76						
		f <sub>IN</sub> = 300 MHz								
		f <sub>IN</sub> = 400 MHz								
		f <sub>IN</sub> = 10 MHz			84					
		f <sub>IN</sub> = 70 MHz			77					
		f <sub>IN</sub> = 100 MHz			76					
HD3	Third harmonic	f <sub>IN</sub> = 170 MHz			74		dBc			
		f <sub>IN</sub> = 230 MHz			74					
		f <sub>IN</sub> = 300 MHz			73					
		f <sub>IN</sub> = 400 MHz			70					
		f <sub>IN</sub> = 10 MHz			92					
		f <sub>IN</sub> = 70 MHz								
		f <sub>IN</sub> = 100 MHz			87					
	Worst other harmonic/spur (other	f <sub>IN</sub> = 170 MHz			87		dBc			
	than HD2 and HD3)	f <sub>IN</sub> = 230 MHz		83						
		f <sub>IN</sub> = 300 MHz								
		f <sub>IN</sub> = 400 MHz			83 80					



Min, Typ, and Max values at  $T_A$  = 25°C, full temperature range is  $T_{MIN}$  = -55°C to  $T_{MAX}$  = 125°C, sampling rate = 210 MSPS, 50% clock duty cycle,  $AV_{DD}$  = 5 V,  $DRV_{DD}$  = 3.3 V, -1-dBFS differential input, and 3- $V_{PP}$  differential clock (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		f <sub>IN</sub> = 10 MHz		69.6		
		$f_{IN} = 70 \text{ MHz}$		68.8		
		$f_{IN} = 100 \text{ MHz}$		68		
	SINAD	$f_{IN} = 170 \text{ MHz}$		66.8		dBc
		$f_{IN} = 230 \text{ MHz}$		66		
		$f_{IN} = 300 \text{ MHz}$		64		
		f <sub>IN</sub> = 400 MHz		60		
ENOB	Effective number of bits	f <sub>IN</sub> = 10 MHz		11.4		Bits
	RMS idle channel noise	Inputs tied to common-mode		0.4		LSB
DIGITA	L CHARACTERISTICS – LVDS D	IGITAL OUTPUTS				
	Differential output voltage		0.247		0.452	V
	Output offset voltage		1.125	1.25	1.375	V



## **TIMING CHARACTERISTICS**

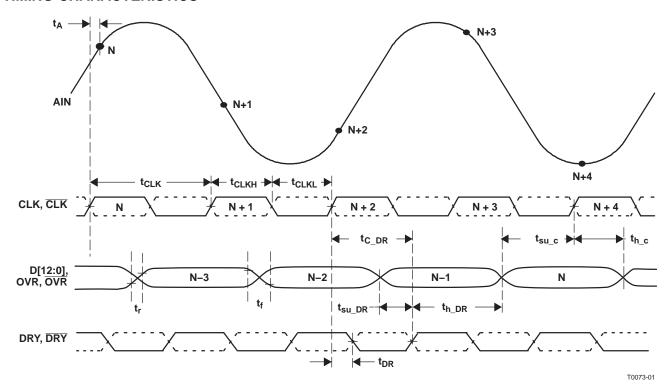


Figure 2. Timing Diagram

#### **TIMING CHARACTERISTICS**

Min, Typ, Max over full temperature range, 50% clock duty cycle, sampling rate = 210 MSPS, AV<sub>DD</sub> = 5 V, DRV<sub>DD</sub> = 3.3 V

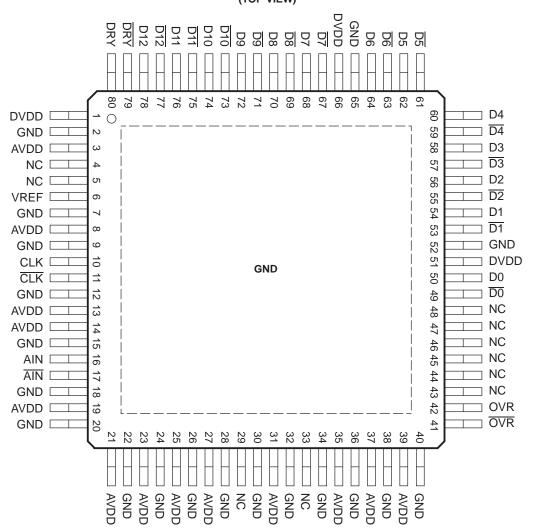
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>A</sub>	Aperture delay			500		ps	
t <sub>J</sub>	Clock slope independent aperture uncertainty (jitter)			150		fs RMS	
	Latency			4		cycles	
Clock In	put						
t <sub>CLK</sub>	Clock period			4.76		ns	
t <sub>CLKH</sub>	Clock pulse width high			2.38		ns	
t <sub>CLKL</sub>	Clock pulse width low			2.38		ns	
Clock to	DataReady (DRY)						
t <sub>DR</sub>	Clock rising to DataReady falling			1.1		ns	
t <sub>C_DR</sub>	Clock rising to DataReady rising	Clock duty cycle = 50% (1)	3.1	3.5	3.9	ns	
Clock to	DATA, OVR <sup>(2)</sup>						
t <sub>r</sub>	Data rise time (20% to 80%)			0.6		ns	
t <sub>f</sub>	Data fall time(80% to 20%)			0.6		ns	
t <sub>su_c</sub>	Data valid to clock (setup time)			3.5		ns	
t <sub>h_c</sub>	Clock to invalid Data (hold time)			0.2		ns	
DataRea	dy (DRY)/DATA, OVR <sup>(2)</sup>					•	
t <sub>su(DR)</sub>	Data valid to DRY		2.1	2.4		ns	
t <sub>h(DR)</sub>	DRY to invalid Data		0.9	1.3		ns	

 $t_{C\_DR}$  =  $t_{DR}$  +  $t_{CLKH}$  for clock duty cycles other than 50% Data is updated with clock falling edge or DRY rising edge. (2)



## **DEVICE INFORMATION**

# PFP PACKAGE (TOP VIEW)



P0027-01



# DEVICE INFORMATION (continued) TERMINAL FUNCTIONS

TEF	RMINAL	DESCRIPTION
NAME	NO.	DESCRIPTION
AVDD	3, 8, 13, 14, 19, 21, 23, 25, 27, 31, 35, 37, 39	Analog power supply
DVDD	1, 51, 66	Output driver power supply
GND	2, 7, 9, 12, 15, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 52, 65	Ground
VREF	6	Reference voltage
CLK	10	Differential input clock (positive). Conversion initiated on rising edge.
CLK	11	Differential input clock (negative)
AIN	16	Differential input signal (positive)
AIN	17	Differential input signal (negative)
OVR, OVR	42, 41	Over range indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
D0, <del>D</del> 0	50, 49	LVDS digital output pair, least-significant bit (LSB)
D1–D6, <del>D1</del> – <del>D6</del>	53–64	LVDS digital output pairs
D7–D11, <del>D7</del> – <del>D11</del>	67–76	LVDS digital output pairs
D12, D12	78, 77	LVDS digital output pair, most-significant bit (MSB)
DRY, DRY	80, 79	Data ready LVDS output pair
NC	4, 5, 29, 33, 43–48	No connect

#### **DEFINITION OF SPECIFICATIONS**

**Analog Bandwidth** The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter) The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

**Maximum Conversion Rate** The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate The minimum sampling rate at which the ADC functions.

**Differential Nonlinearity (DNL)** An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Integral Nonlinearity (INL) The INL is the deviation of the ADCs transfer function from a best fit line determined by a least squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best fit line, measured in units of LSB.

**Gain Error** The gain error is the deviation of the ADCs actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Offset Error Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

**Temperature Drift** Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at  $T_{MIN}$  or  $T_{MAX}$ . It is computed as the maximum variation the parameters over the whole temperature range divided by  $T_{MIN} - T_{MAX}$ .

Signal-to-Noise Ratio (SNR) SNR is the ratio of the power of the fundamental  $(P_S)$  to the noise floor power  $(P_N)$ , excluding the power at dc and the first five harmonics.



## **DEFINITION OF SPECIFICATIONS (continued)**

$$SNR = 10log_{10} \frac{P_S}{P_N}$$
 (1)

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

**Signal-to-Noise and Distortion (SINAD)** SINAD is the ratio of the power of the fundamental  $(P_S)$  to the power of all the other spectral components including noise  $(P_N)$  and distortion  $(P_D)$ , but excluding dc.

SINAD = 
$$10\log_{10} \frac{P_S}{P_N + P_D}$$
 (2)

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

**Effective Resolution Bandwidth** The highest input frequency where the SNR (dB) is dropped by 3 dB for a full-scale input amplitude.

**Total Harmonic Distortion (THD)** THD is the ratio of the power of the fundamental  $(P_S)$  to the power of the first five harmonics  $(P_D)$ .

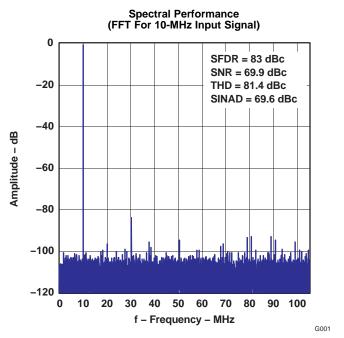
THD = 
$$10\log_{10} \frac{P_S}{P_D}$$
 (3)

THD is typically given in units of dBc (dB to carrier).

**Two-Tone Intermodulation Distortion** IMD3 is the ratio of the power of the fundamental (at frequencies  $f_1$ ,  $f_2$ ) to the power of the worst spectral component at either frequency  $2f_1 - f_2$  or  $2f_2 - f_1$ ). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.



## TYPICAL CHARACTERISTICS





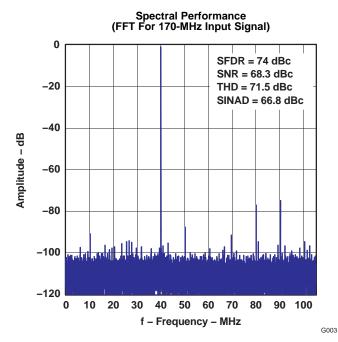


Figure 5.

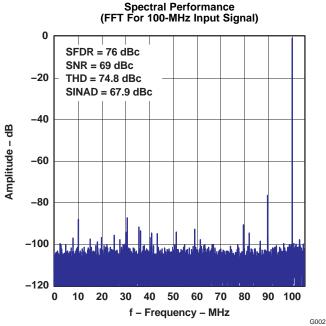


Figure 4.

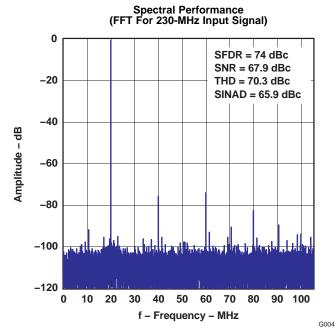


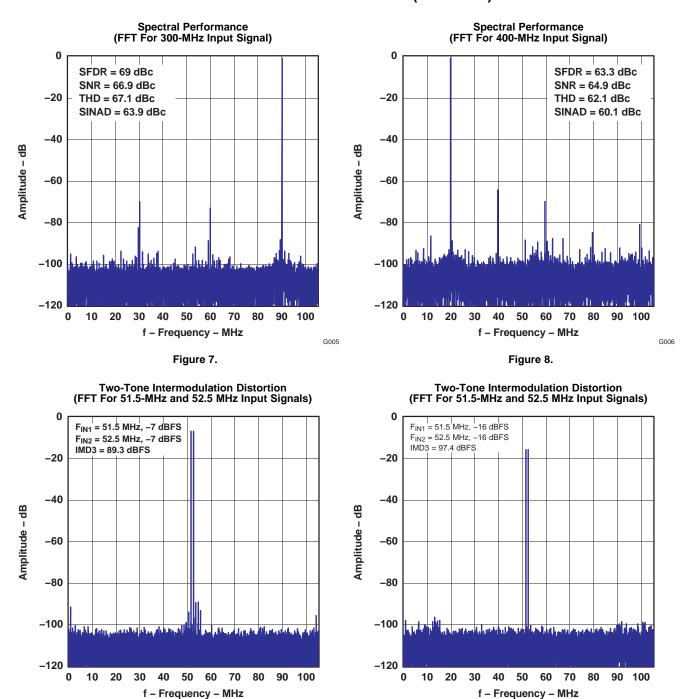
Figure 6.



G008

Figure 10.

## **TYPICAL CHARACTERISTICS (continued)**



G007

Figure 9.



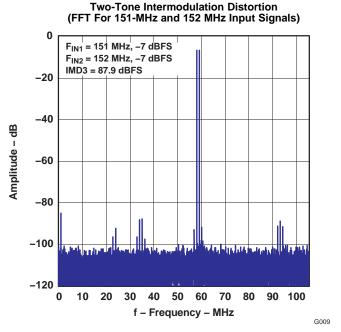


Figure 11.

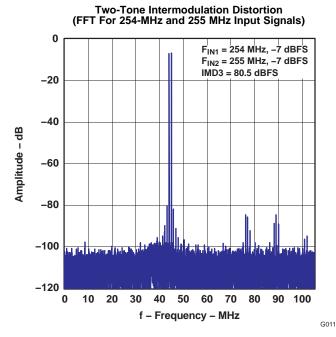
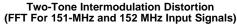


Figure 13.



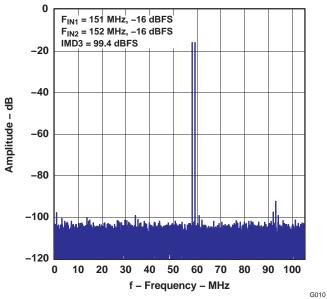


Figure 12.

## Two-Tone Intermodulation Distortion (FFT For 254-MHz and 255 MHz Input Signals)

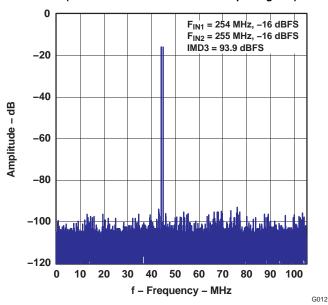


Figure 14.



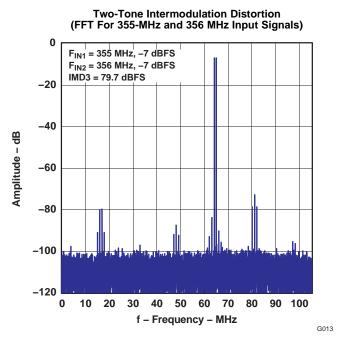


Figure 15.

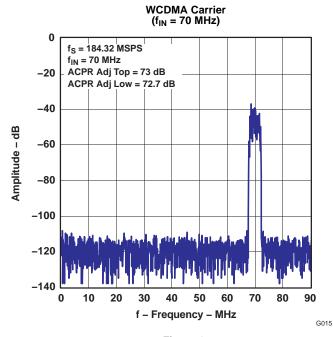
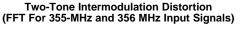


Figure 17.



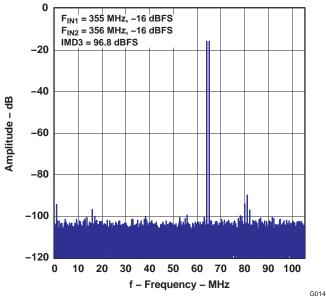


Figure 16.

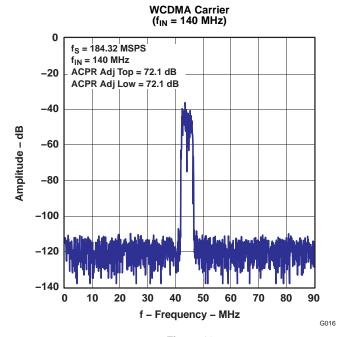


Figure 18.



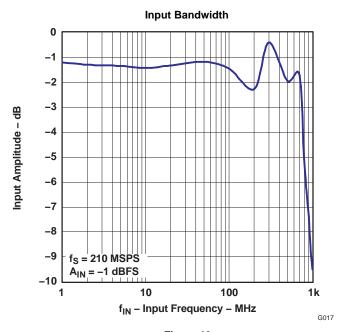


Figure 19.

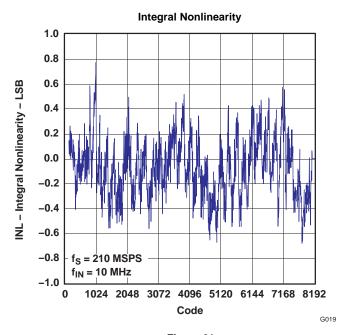


Figure 21.

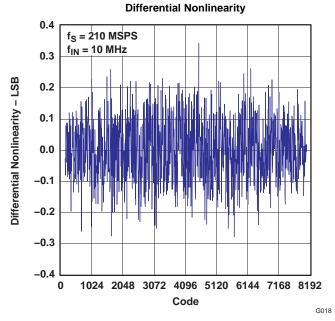


Figure 20.

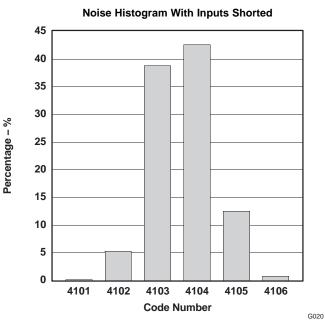


Figure 22.



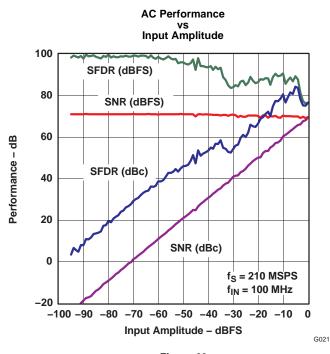


Figure 23.

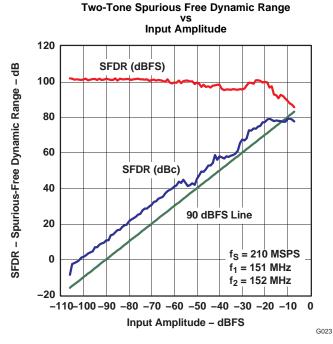


Figure 25.

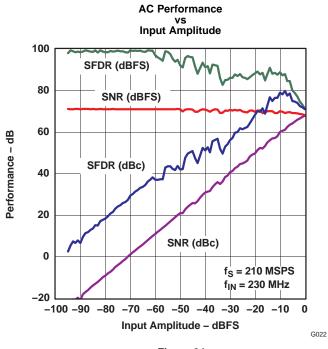


Figure 24.

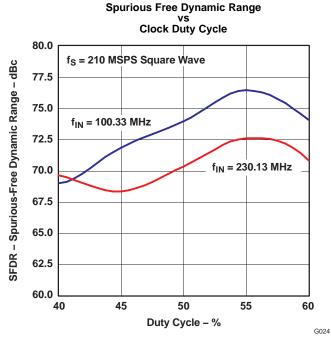


Figure 26.



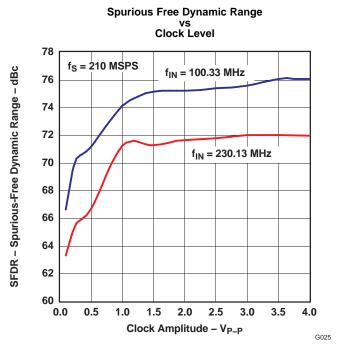


Figure 27.

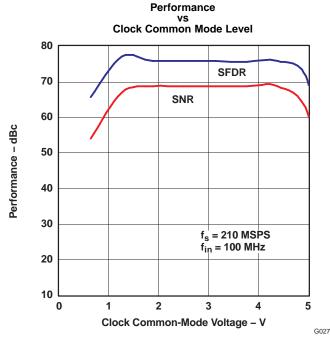


Figure 29.

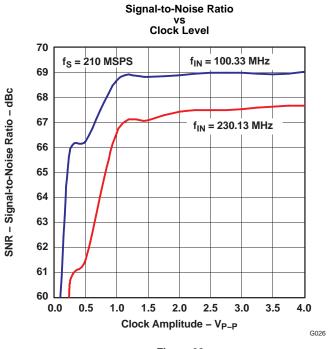


Figure 28.

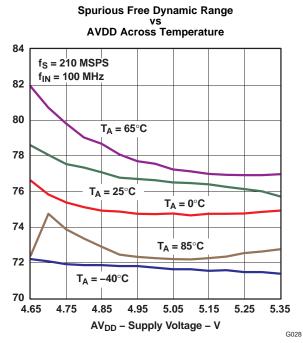
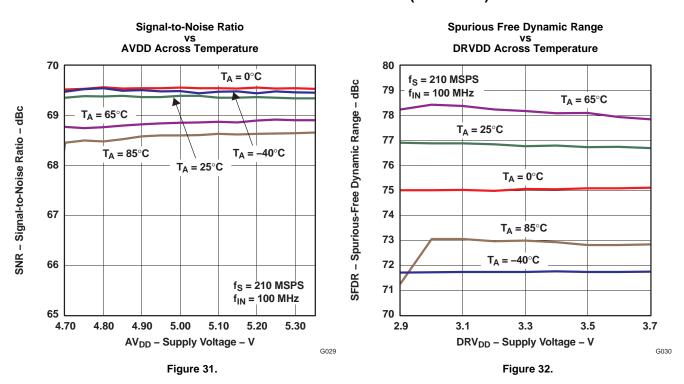
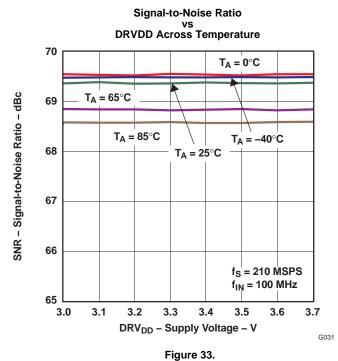


Figure 30.

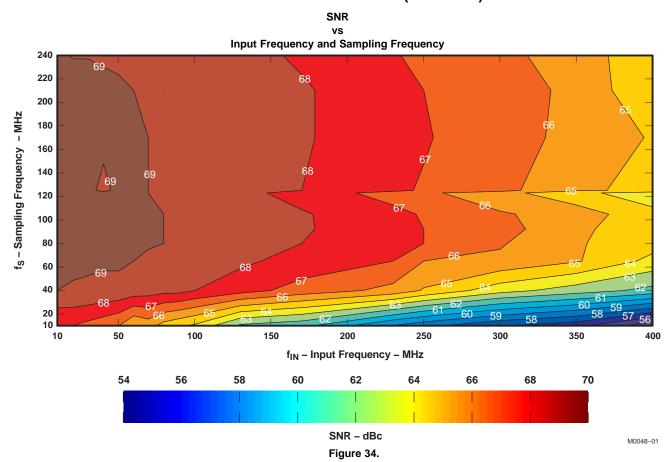
SFDR - Spurious-Free Dynamic Range - dBc







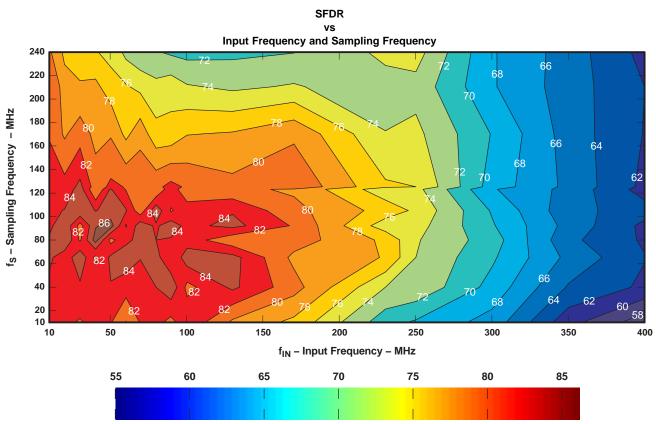






M0048-02

## **TYPICAL CHARACTERISTICS (continued)**



SFDR - dBc

Figure 35.



#### **APPLICATION INFORMATION**

## **Theory of Operation**

The ADS5440 is a 13-bit, 210-MSPS, monolithic pipeline analog-to-digital converter (ADC). Its bipolar analog core operates from a 5-V supply, while the output uses a 3.3 V supply to provide LVDS compatible outputs. The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track and hold (T&H) and the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of four clock cycles, after which the output data is available as a 13-bit parallel word, coded in offset binary format.

## **Input Configuration**

The analog input for the ADS5440 consists of an analog differential buffer followed by a bipolar T&H. The analog buffer isolates the source driving the input of the ADC from any internal switching. The input common mode is set internally through a  $500-\Omega$  resistor connected from 2.4 V to each of the inputs. This results in a differential input impedance of 1 k $\Omega$ .

For a full-scale differential input, each of the differential lines of the input signal (pins 16 and 17) swings symmetrically between 2.4 + 0.55 V and 2.4 - 0.55 V. This means that each input has a maximum signal swing of 1.1 V<sub>PP</sub> for a total differential input signal swing of 2.2 V<sub>PP</sub>. The maximum swing is determined by the internal reference voltage generator eliminating the need for any external circuitry for this purpose.

The ADS5440 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 36 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. If voltage gain is required, a step up transformer can be used. For voltage gains that would require an impractical transformer turn ratio, a single-ended amplifier driving the transformer is shown in Figure 37.

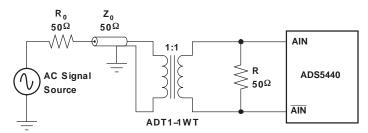


Figure 36. Converting a Single-Ended Input to a Differential Signal Using RF Transformers

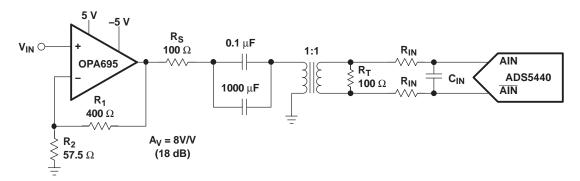


Figure 37. Using the OPA695 With the ADS5440



## Application Information (continued)

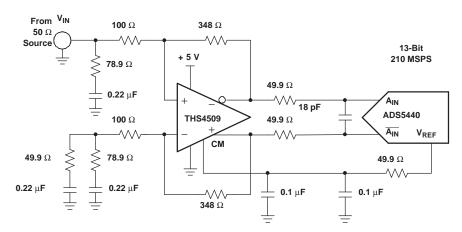


Figure 38. Using the THS4509 With the ADS5440

Besides the OPA695, TI offers a wide selection of single-ended operational amplifiers that can be selected depending on the application. An RF gain block amplifier, such as the TI THS9001, can also be used with an RF transformer for high input frequency applications. For applications requiring dc-coupling with the signal source, a differential input/differential output amplifier like the THS4509 (see Figure 38) is a good solution, as it minimizes board space and reduces the number of components.

In this configuration, the THS4509 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5440.

The 50- $\Omega$  resistors and 18-pF capacitor between the THS4509 outputs and ADS5440 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 70 MHz (–3 dB).

Input termination is accomplished via the  $78.9-\Omega$  resistor and  $0.22-\mu\text{F}$  capacitor to ground in conjunction with the input impedance of the amplifier circuit. A  $0.22-\mu\text{F}$  capacitor and  $49.9-\Omega$  resistor is inserted to ground across the  $78.9-\Omega$  resistor and  $0.22-\mu\text{F}$  capacitor on the alternate input to balance the circuit.

Gain is a function of the source impedance, termination, and 348- $\Omega$  feedback resistor. See the THS4509 data sheet (SLOS454) for further component values to set proper 50- $\Omega$  termination for other common gains.

Since the ADS5440 recommended input common-mode voltage is 2.4 V, the THS4509 is operated from a single power supply input with  $V_{S+} = 5$  V and  $V_{S-} = 0$  V (ground). This maintains maximum headroom on the internal transistors of the THS4509.

#### **Clock Inputs**

The ADS5440 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. In low input frequency applications, where jitter may not be a big concern, the use of single-ended clock (see Figure 39) could save some cost and board space without any trade-off in performance. When driven on this configuration, it is best to connect CLK to ground with a 0.01- $\mu$ F capacitor, while CLK is ac-coupled with a 0.01  $\mu$ F capacitor to the clock source, as shown in Figure 39.

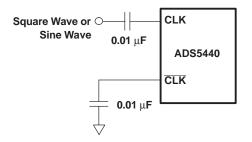


Figure 39. Single-Ended Clock



## Application Information (continued)

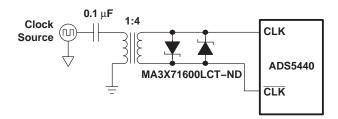


Figure 40. Differential Clock

For jitter-sensitive applications, the use of a differential clock has some advantages (as with any other ADC) at the system level. The first advantage is that it allows for common-mode noise rejection at the PCB level.

A differential clock also allows for the use of bigger clock amplitudes without exceeding the absolute maximum ratings. In the case of a sinusoidal clock, this results in higher slew rates and reduces the impact of clock noise on jitter. See *Clocking High Speed Data Converters* (SLYT075) for more detail.

Figure 40 shows this approach. The back-to-back Schottky diodes can be added to limit the clock amplitude in cases where this would exceed the absolute maximum ratings, even when using a differential clock.

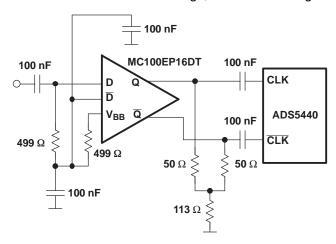


Figure 41. Differential Clock Using PECL Logic

Another possibility is the use of a logic based clock, such as PECL. In this case, the slew rate of the edges will most likely be much higher than the one obtained for the same clock amplitude based on a sinusoidal clock. This solution would minimize the effect of the slope dependent ADC jitter. Using logic gates to square a sinusoidal clock may not produce the best results as logic gates may not have been optimized to act as comparators, adding too much jitter while squaring the inputs.

The common-mode voltage of the clock inputs is set internally to 2.4 V using internal 1-k $\Omega$  resistors. It is recommended to use ac coupling, but if this scheme is not possible due to, for instance, asynchronous clocking, the ADS5440 features good tolerance to clock common-mode variation.

Additionally, the internal ADC core uses both edges of the clock for the conversion process. Ideally, a 50% duty cycle clock signal should be provided.

#### **Digital Outputs**

The ADC provides 13 data outputs (D12 to D0, with D12 being the MSB and D0 the LSB), a data-ready signal (DRY), and an over-range indicator (OVR) that equals a logic high when the output reaches the full-scale limits. The output format is offset binary. It is recommended to use the DRY signal to capture the output data of the ADS5440.

The ADS5440 digital outputs are LVDS compatible.

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## **Application Information (continued)**

## **Power Supplies**

The use of low noise power supplies with adequate decoupling is recommended. Linear supplies are the preferred choice versus switched ones, which tend to generate more noise components that can be coupled to the ADS5440.

The ADS5440 uses two power supplies. For the analog portion of the design, a 5-V AVDD is used, while for the digital outputs supply (DRVDD) we recommend the use of 3.3 V. All the ground pins are marked as GND, although AGND pins and DRGND pins are not tied together inside the package.

## **Layout Information**

The evaluation board represents a good guideline of how to layout the board to obtain the maximum performance out of the ADS5440. General design rules as the use of multilayer boards, single ground plane for ADC ground connections and local decoupling ceramic chip capacitors should be applied. The input traces should be isolated from any external source of interference or noise including the digital outputs, as well as the clock traces. The clock signal traces should also be isolated from other signals, especially in applications where low jitter is required as high IF sampling.

Besides performance oriented rules, care has to be taken when considering the heat dissipation out of the device. The thermal heatsink should be soldered to the board as described in the PowerPad Package section.

## PowerPAD™ Package

The PowerPAD package is a thermally-enhanced standard size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB using the PCB as a heatsink.

#### **Assembly Process**

- 1. Prepare the PCB top-side etch pattern including etch for the leads, as well as the thermal pad as illustrated in the Mechanical Data section.
- 2. Place a 6-by-6 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
- 3. It is recommended to place a small number of 25-mil diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
- 4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
- 5. Do not use the typical web or spoke via connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
- 6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
- 7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
- 8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the SLMA004 application brief, *PowerPAD Made Easy*, or the technical brief, *PowerPAD Thermally Enhanced Package* SLMA002.

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11-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
ADS5440MPFPEP	Active	Production	HTQFP (PFP)   80	96   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ADS5440M-EP
V62/06669-01XE	Active	Production	HTQFP (PFP)   80	96   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ADS5440M-EP

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF ADS5440-EP:

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## **PACKAGE OPTION ADDENDUM**

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• Catalog : ADS5440

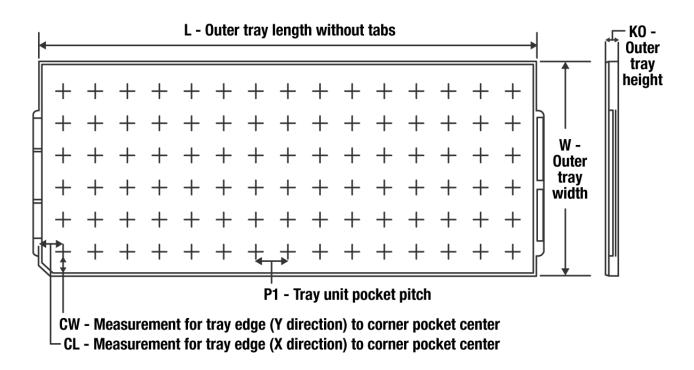
NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product



www.ti.com 5-Jan-2022

## **TRAY**



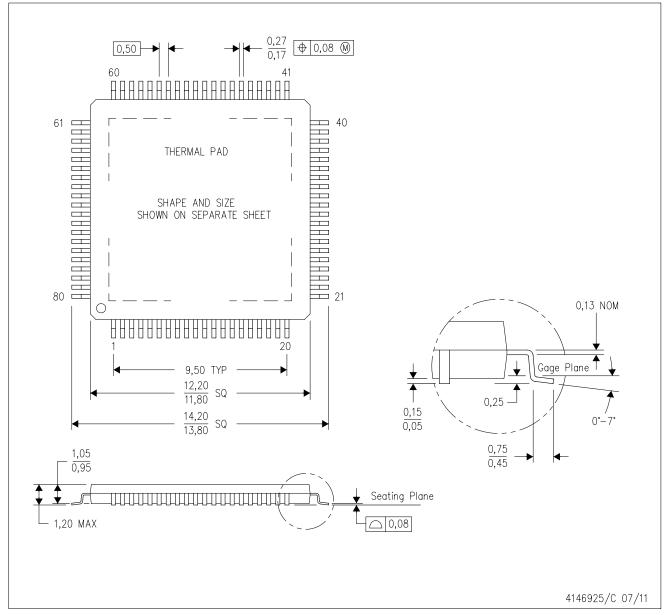
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	Κ0 (μm)	P1 (mm)	CL (mm)	CW (mm)
ADS5440MPFPEP	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
V62/06669-01XE	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3

PFP (S-PQFP-G80)

## PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <a href="https://www.ti.com">https://www.ti.com</a>>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MS-026

## PowerPAD is a trademark of Texas Instruments.



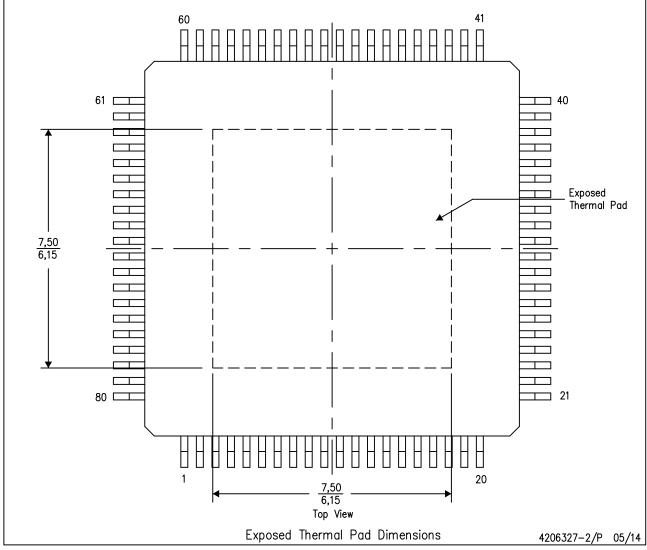
PowerPAD™ PLASTIC QUAD FLATPACK

#### THERMAL INFORMATION

This PowerPAD package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



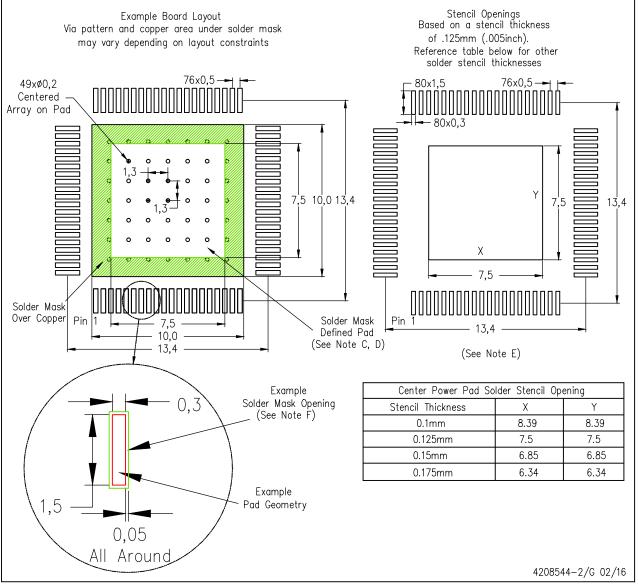
NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



## PFP (S-PQFP-G80)

## PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:

All linear dimensions are in millimeters.

- PowerPAD is a trademark of Texas Instruments.
- This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="http://www.ti.com">www.ti.com</a>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

  F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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