ADS52J65 8-Channel, 16-Bit, 125-MSPS, 70-mW/Ch ADC With JESD204B Interface

1 Features

- 16-Bit Resolution, Idle SNR: 80 dBFS
- 70 mW/Ch at 125 MSPS, 4-CH per Lane
- 45 mW/Ch at 62.5 MSPS, 8-CH per Lane
- Full-Scale Input: 2 V_{PP}
- Full-Scale SNR: 78 dBFS at f_{in} = 10 MHz
- Full-Scale SFDR: –85 dBc at f_{in} = 10 MHz
- Analog Input –3 dB Bandwidth = 250 MHz
- Maximum Input Signal Frequency for 2 V_{PP} Input = 130 MHz
- Fast and Consistent Overload Recovery
- Advanced Digital Features
  - Automatic DC Offset Correction
  - Digital Average
- Digital I/Q Demodulator
  - Fractional Decimation Filter M = 1 to 63 With Increments of 0.25
  - Data Output Rate Reduction After Decimation
  - 64 mW/Ch at 80 MSPS and Decimation = 2
  - On-Chip RAM With 32 Preset Profiles
- JESD204B Subclass 0, 1, and 2
  - 2, 4, or 8 Channels per JESD Lane
  - 10-Gbps JESD Interface
  - Supports lane rate up to 12.8 Gbps for short trace length (< 5 Inch)
- 64-Pin Non-Magnetic 9 × 9-mm Package

2 Applications

- Medical Imaging: Ultrasound, MRI
- High Frequency Ultrasound
- Non-Destructive Tests (NDT)
- Radar, Lidar, and Spectroscopy
- Digital Oscillscopes and Data Acquistion
- Flow cytometry, flow cytometer, Hematology analyzer

3 Description

The 8-channel, 16-bit ADS52J65 analog-to-digital converter (ADC) uses CMOS process and innovative circuit techniques. It is designed to operate at low power and give very high signal-to-noise ratio (SNR) performance with a 2-Vpp full-scale input. The device gives 80-dBFS idle SNR and 78-dBFS full-scale SNR at 5 MHz. The large input bandwidth of 250 MHz makes the device suitable for a wide range of applications, such as high frequency medical ultrasound, magnetic resonance imaging, multi-channel data acquisition, flow cytometry, flow cytometer, and hematology analyzer. The ADC integrates an internal reference trimmed to match across devices.

ADS52J65 has advanced digital features, including a digital I/Q demodulator with fractional decimation filter. The ADC data from each channel is encoded using an 8B to 10B format and is sent as a SerDes data stream using current-mode logic (CML) output buffers, as per the JESD204B standard. The ADC data from all eight channels can be output over a single CML buffer (1-lane SerDes) with the data rate limited to a maximum of 12.8 Gbps. Using SerDes outputs reduces the number of interface lines. This, together with the low-power design, enables eight channels to be packaged in a 9-mm × 9-mm VQFN allowing high system integration densities. ADS52J65 also supports modes where all ADC data is sent over four CML buffers (4-Lane SerDes), reducing the SerDes data rate per lane for low-cost FPGAs.

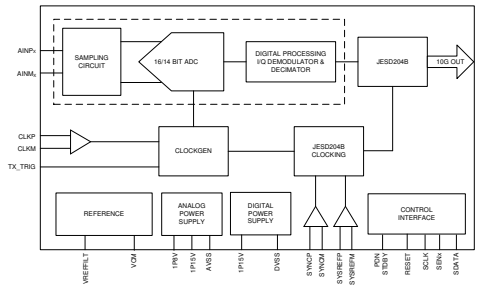
The ADS52J65 is available in a non-magnetic VQFN package that does not create any magnetic artifact. The device is specified over –40°C to +85°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS52J65	VQFN (64)	9.00 mm × 9.00 mm

(1) See the orderable addendum at the end of the data sheet.

Block Diagram



4 Revision History

Changes from Original (December 2018) to Revision A	Page

- Added *Application*: Flow cytometry, flow cytometer, Hematology analyze: 1
- Added text to the first paragraph of the *Description*: flow cytometry, flow cytometer, hematology analyze 1

5 Device and Documentation Support

5.1 Related Documentation

For related documentation see the following:

- *JESD204B Overview*
- *Clocking High-Speed Data Converters*
- *ADS52J90 10-Bit, 12-Bit, 14-Bit, Multichannel, Low-Power, High-Speed ADC with LVDS, JESD Outputs*
- *ADS5263 Quad Channel 16-Bit, 100-MSPS High-SNR ADC*
- *AFE5818 16-Channel, Ultrasound, Analog Front-End with 140-mW/Channel Power, 0.75-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, and Passive CW Mixer*
- *ISO724x High-Speed, Quad-Channel Digital Isolators*
- *LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs*
- *SN74AUP1T04 LOW POWER, 1.8/2.5/3.3-V INPUT, 3.3-V CMOS OUTPUT, SINGLE INVERTER GATE*
- *THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers*

5.2 Trademarks

All trademarks are the property of their respective owners.

5.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

5.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS52J65IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J65
ADS52J65IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J65
ADS52J65IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J65
ADS52J65IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J65

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

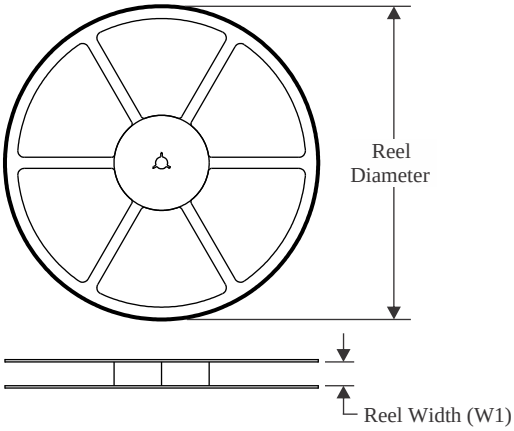
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

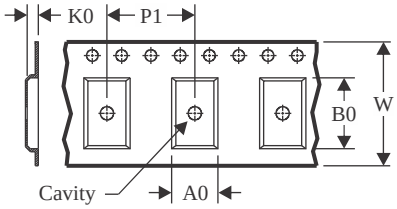
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

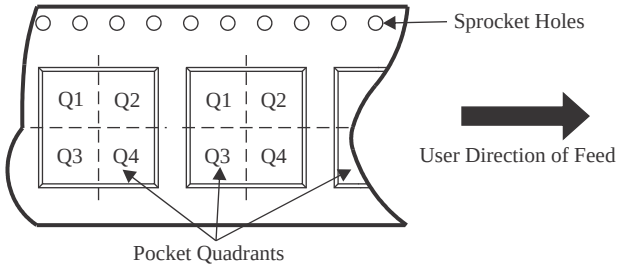


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

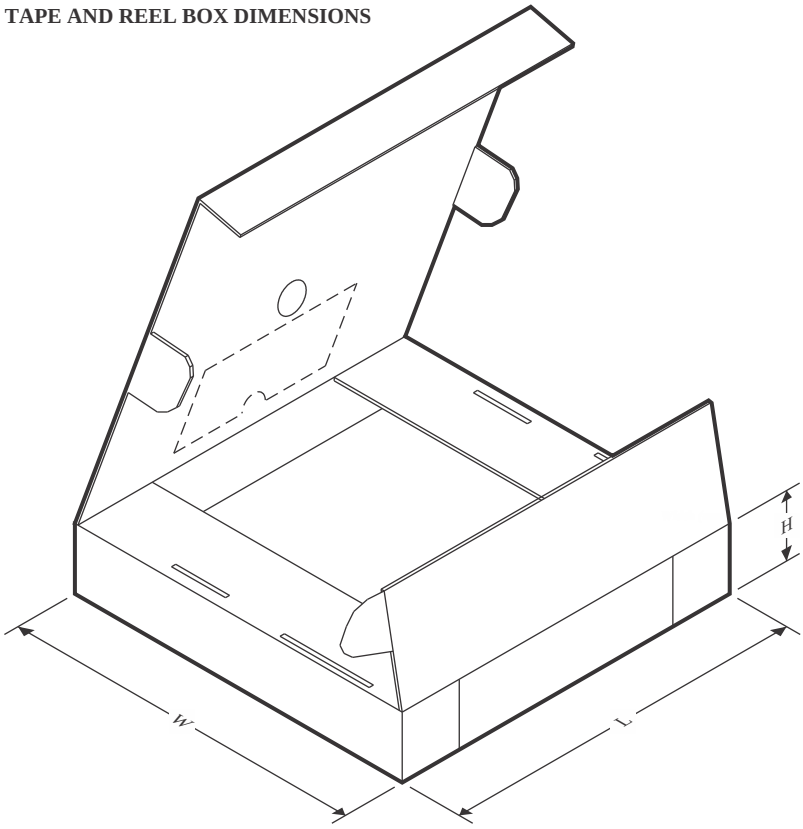
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS52J65IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS52J65IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0

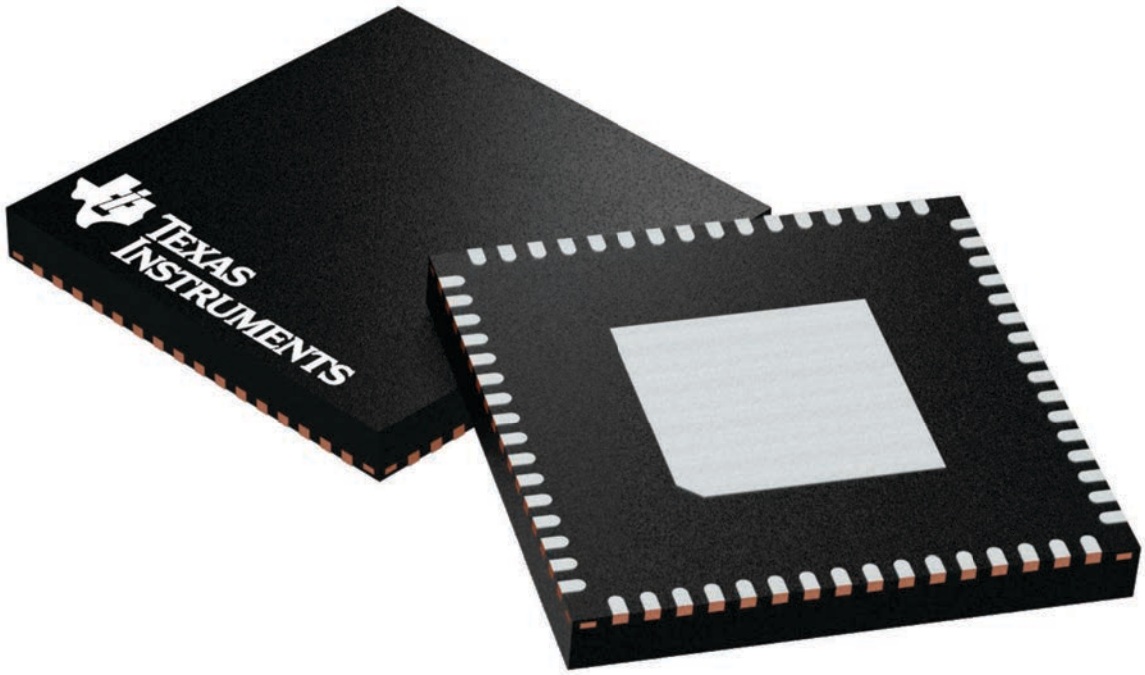
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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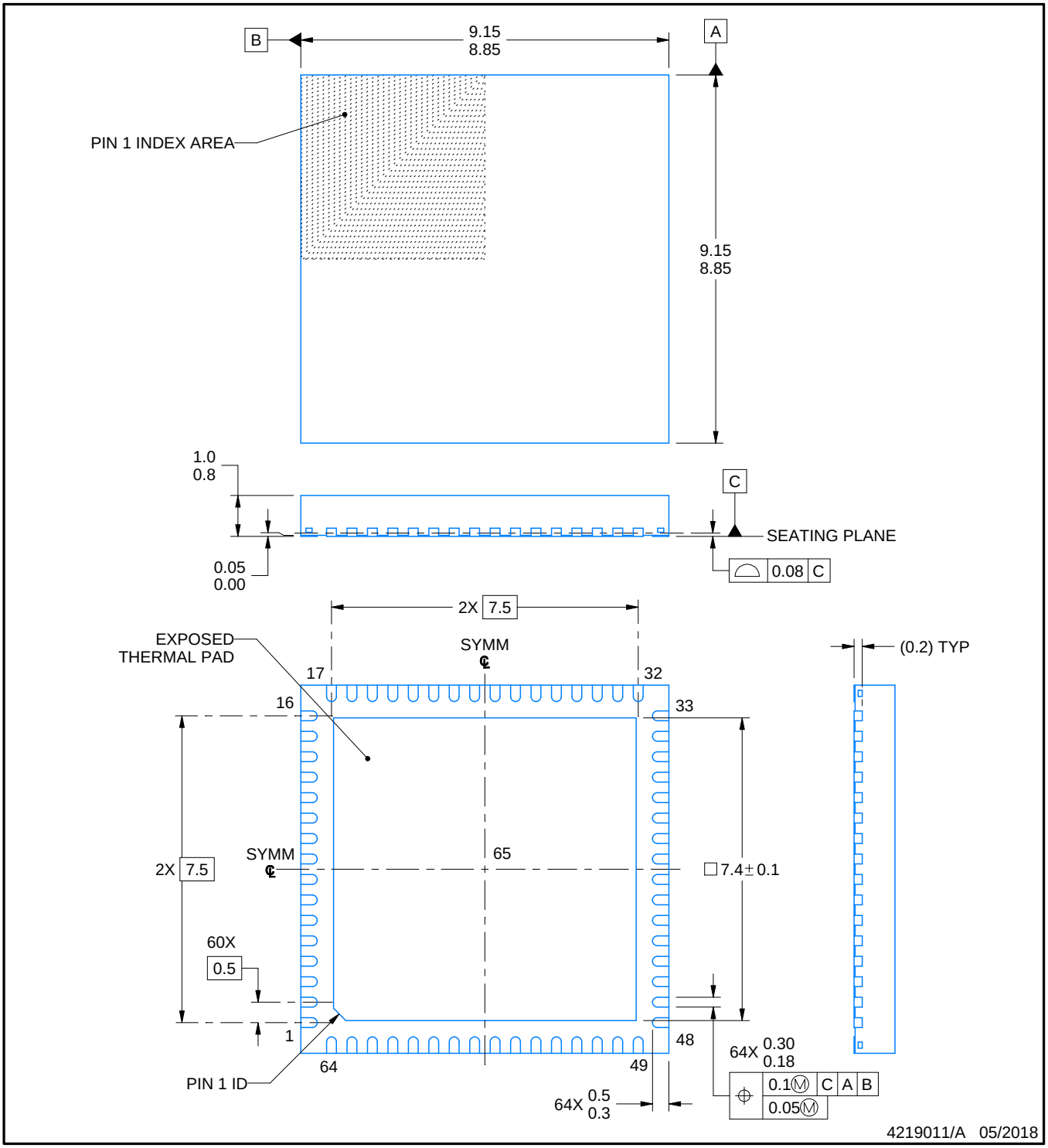
RGC0064H

PACKAGE OUTLINE

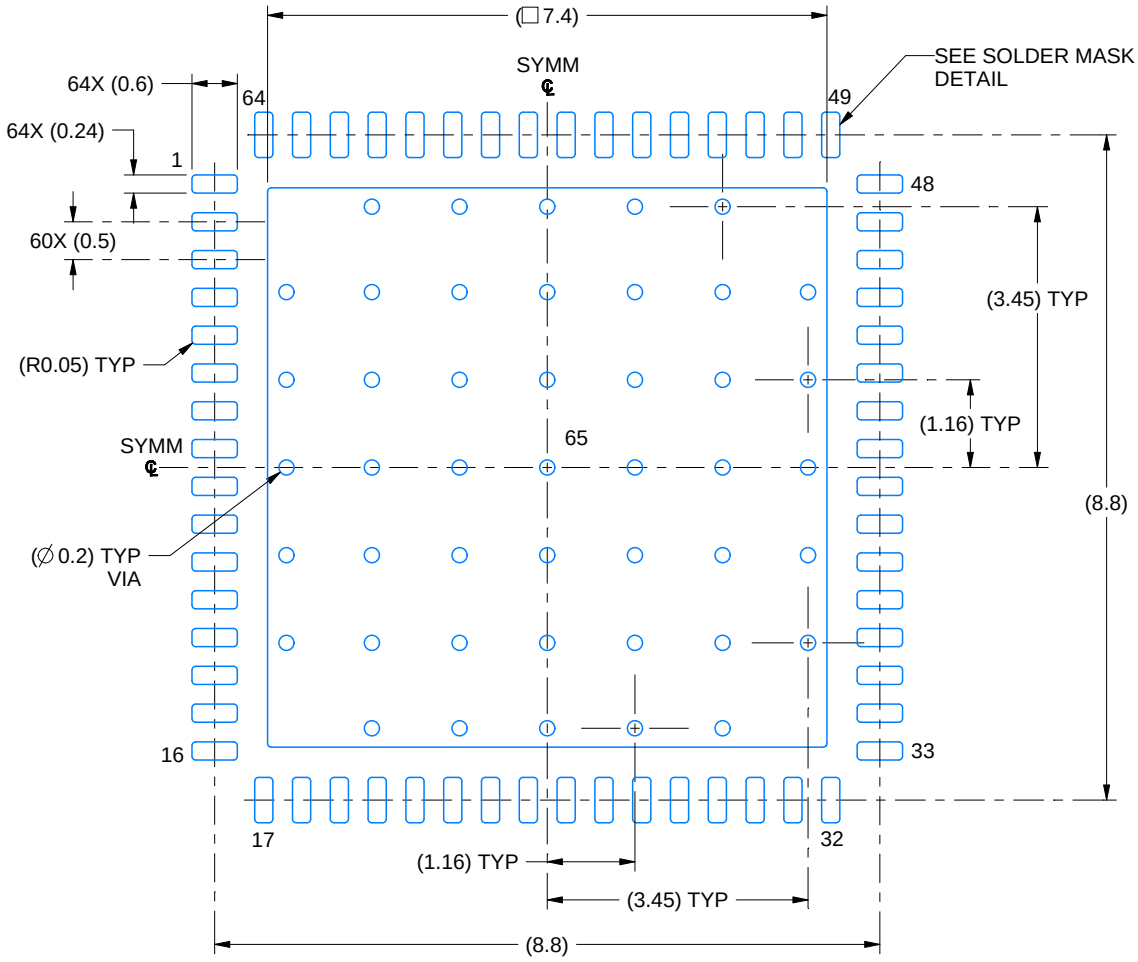
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

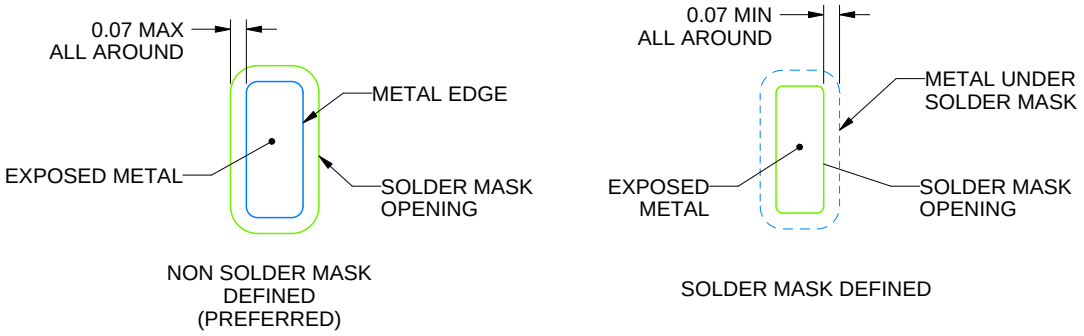


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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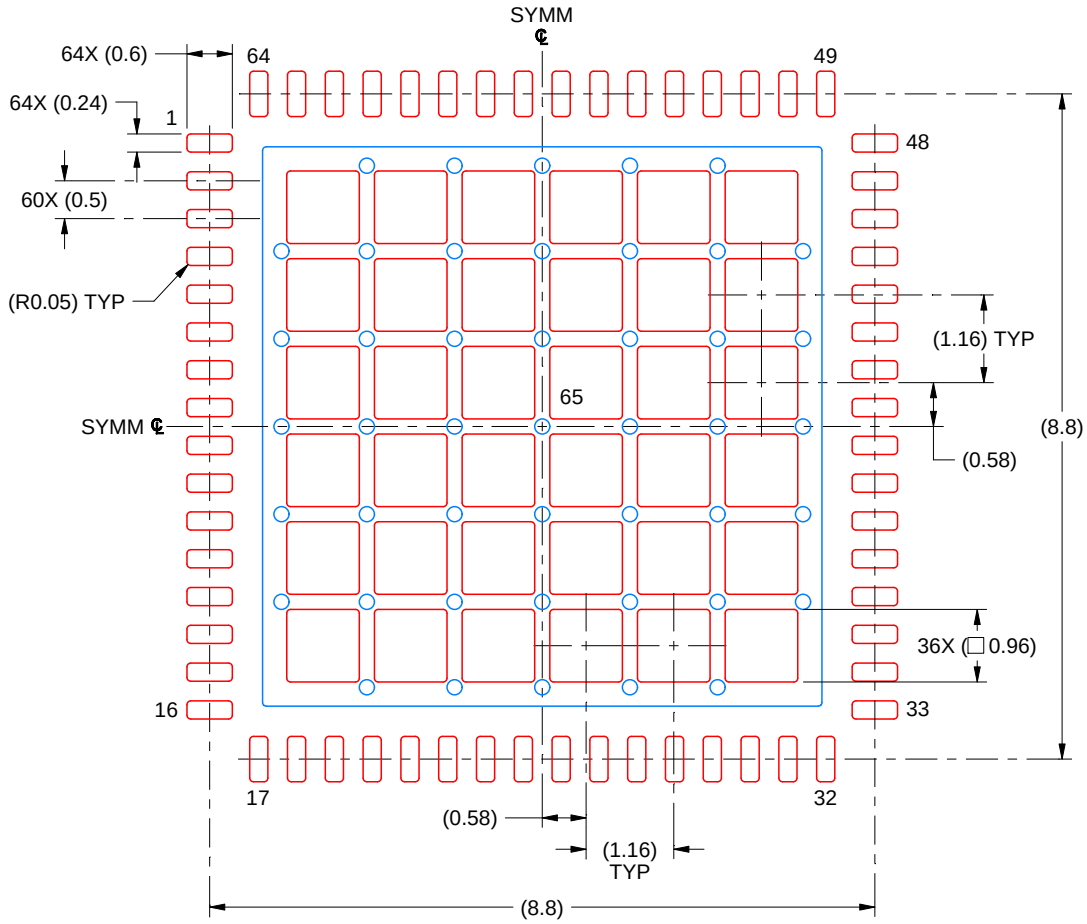
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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