ADS41Bx9 14- and 12-Bit, 250-MSPS, Ultralow-Power ADCs with Analog Buffers

1 Features

- ADS41B49: 14-Bit, 250 MSPS
  ADS41B29: 12-Bit, 250 MSPS
- Integrated High-Impedance Analog Input Buffer:
  - Input Capacitance: 2 pF
  - 200-MHz Input Resistance: 3 kΩ
- Maximum Sample Rate: 250 MSPS
- Ultralow Power:
  - 1.8-V Analog Power: 180 mW
  - 3.3-V Buffer Power: 96 mW
  - I/O Power: 135 mW (DDR LVDS)
- High Dynamic Performance:
  - SNR: 69 dBFS at 170 MHz
  - SFDR: 82.5 dBc at 170 MHz
- Output Interface:
  - Double Data Rate (DDR) LVDS with Programmable Swing and Strength:
    - Standard Swing: 350 mV
    - Low Swing: 200 mV
    - Default Strength: 100-Ω Termination
    - 2x Strength: 50-Ω Termination
  - 1.8-V Parallel CMOS Interface Also Supported
- Programmable Gain for SNR, SFDR Trade-Off
- DC Offset Correction
- Supports Low Input Clock Amplitude
- Package: VQFN-48 (7 mm × 7 mm)

2 Applications

- Power Amplifier Linearization
- Software Defined Radio
- Wireless Communications Infrastructure

3 Description

The ADS41Bx9 are members of the ultralow-power ADS4xxx analog-to-digital converter (ADC) family, featuring integrated analog input buffers. These devices use innovative design techniques to achieve high dynamic performance, and consume extremely low power. The analog input pins have buffers, with benefits of constant performance and input impedance across a wide frequency range. The devices are well-suited for multi-carrier, wide bandwidth communications applications such as PA linearization.

The ADS41Bx9 have features such as digital gain and offset correction. The gain option can be used to improve SFDR performance at lower full-scale input ranges, especially at high input frequencies. The integrated dc offset correction loop can be used to estimate and cancel the ADC offset. At lower sampling rates, the ADC automatically operates at scaled-down power with no loss in performance.

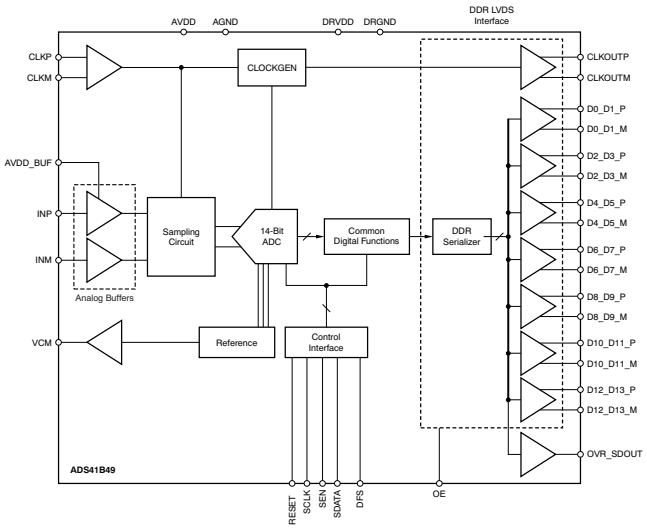
The devices support both double data rate (DDR) low-voltage differential signaling (LVDS) and parallel CMOS digital output interfaces. The low data rate of the DDR LVDS interface (maximum 500 MBPS) makes using low-cost field-programmable gate array (FPGA)-based receivers possible. The devices have a low-swing LVDS mode that can be used to further reduce the power consumption. The strength of the LVDS output buffers can also be increased to support 50-Ω differential termination.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS41Bx9	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADS41B49 Block Diagram



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4 Revision History

Changes from Revision E (July 2012) to Revision F **Page**

- Changed title and changed *ADS41B49/29* to *ADS41Bx9* and QFN to VQFN throughout document ... 1
- Added *Applications* section, *Device Information* table, front-page figure, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Programming* section, *Register Maps* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table ... 1
- Changed *Pin Functions* table: changed title and format ... 6
- Added Added last row to *Voltage applied to input pins* section in *Absolute Maximum Ratings* table ... 7
- Changed *Temperature* parameters in *Absolute Maximum Ratings* table: changed format of *Temperature* section and changed maximum specifications for T_A and T_J ... 7
- Changed TYP column header to NOM in *Recommended Operating Conditions* table ... 8
- Changed Digital Outputs, T_J parameter in *Recommended Operating Conditions* table ... 8
- Deleted *High-Performance Modes* section from *Recommended Operating Conditions* table ... 8
- Changed conditions of *Electrical Characteristics: General* table from *temperature* to *ambient temperature* ... 9
- Changed conditions of *Electrical Characteristics: ADS41B29, ADS41B49* table from *temperature* to *ambient temperature* ... 10
- Added footnote 1 to *Electrical Characteristics: ADS41B29, ADS41B49* table ... 10
- Changed conditions of *Timing Requirements: LVDS and CMOS Modes* table from *temperature* to *ambient temperature* 12
- Added footnotes 6 and 7 to *Timing Requirements: LVDS and CMOS Modes* table ... 12
- Added footnote 1 to *Timing Requirements: Reset* table ... 13
- Changed title of Figure 13 and Figure 14 ... 16
- Changed title of Figure 31 and Figure 32 ... 19

Revision History (continued)

- Changed conditions of Table 6 38
- Added *Summary of High-Performance Modes* section 40
- Changed bit registers to satisfy new standard requirements 41

Changes from Revision D (December 2010) to Revision E **Page**

- Updated *Thermal Information* table values..... 8
- Changed Analog Inputs, *Differential input capacitance* parameter typical specification in Electrical Characteristics: General table 9
- Changed value of input capacitance in *Analog Input* section..... 26
- Updated Figure 54 and footnotes..... 26
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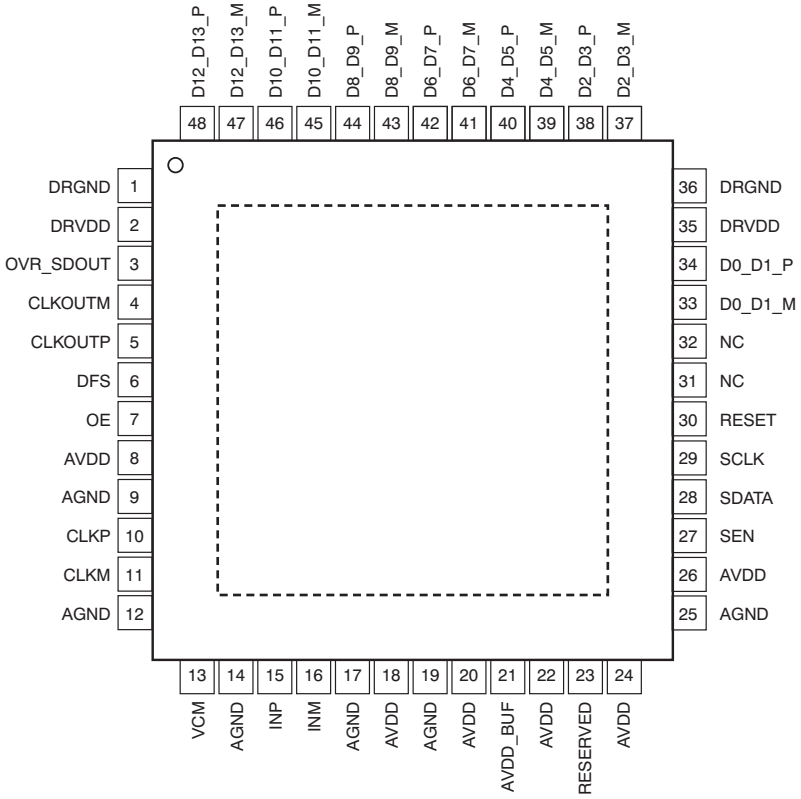
- Updated Figure 83..... 48
- Updated Figure 84..... 48

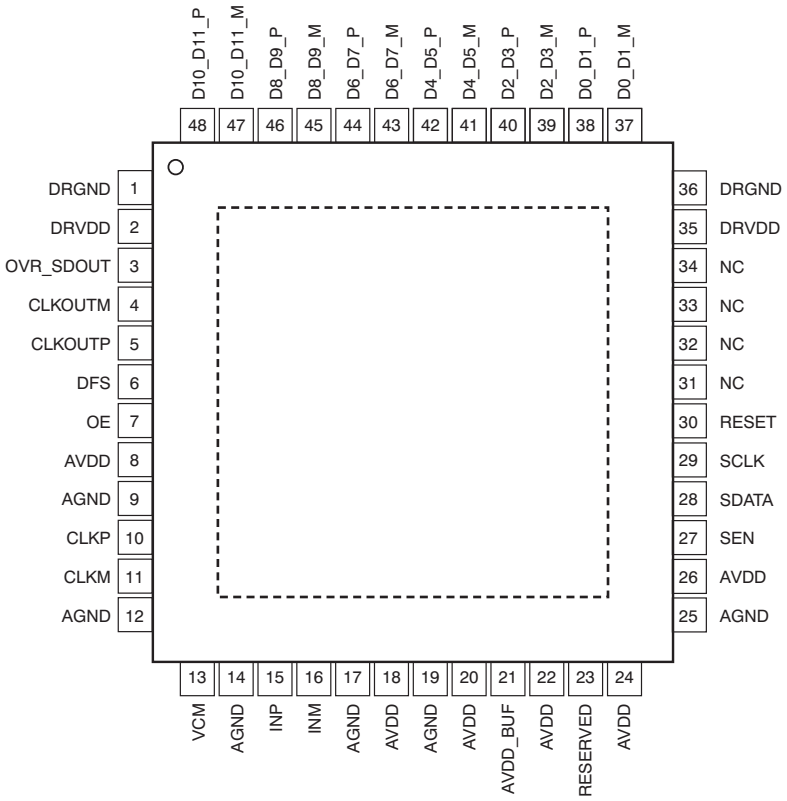
5 Pin Configuration and Functions

ADS41B49 LVDS Mode: RGZ Package(1)
48-Pin VQFN
Top View



(1) The PowerPAD™ is connected to DRGND.

ADS41B29 LVDS Mode: RGZ Package(2)
48-Pin VQFN
Top View



(1) The PowerPAD is connected to DRGND.

Pin Functions

PIN	NO.		I/O	DESCRIPTION
NAME	ADS41B49	ADS41B29		
AGND	9, 12, 14, 17, 19, 25	9, 12, 14, 17, 19, 25	I	Analog ground
AVDD	8, 18, 20, 22, 24, 26	8, 18, 20, 22, 24, 26	I	1.8-V analog power supply
AVDD_BUF	21	21	I	3.3-V input buffer supply
CLKM	11	11	I	Differential clock input, negative
CLKP	10	10	I	Differential clock input, positive
CLKOUTP	5	5	O	Differential output clock, true
CLKOUTM	4	4	O	Differential output clock, complement
D0_D1_M	33	37	O	Differential output data D0 and D1 multiplexed, complement
D0_D1_P	34	38	O	Differential output data D0 and D1 multiplexed, true
D2_D3_M	37	39	O	Differential output data D2 and D3 multiplexed, complement
D2_D3_P	38	40	O	Differential output data D2 and D3 multiplexed, true
D4_D5_M	39	41	O	Differential output data D4 and D5 multiplexed, complement
D4_D5_P	40	42	O	Differential output data D4 and D5 multiplexed, true
D6_D7_M	41	43	O	Differential output data D6 and D7 multiplexed, complement
D6_D7_P	42	44	O	Differential output data D6 and D7 multiplexed, true
D8_D9_M	43	45	O	Differential output data D8 and D9 multiplexed, complement
D8_D9_P	44	46	O	Differential output data D8 and D9 multiplexed, true
D10_D11_M	45	47	O	Differential output data D10 and D11 multiplexed, complement
D10_D11_P	46	48	O	Differential output data D10 and D11 multiplexed, true
D12_D13_M	47	—	O	Differential output data D12 and D13 multiplexed, complement
D12_D13_P	48	—	O	Differential output data D12 and D13 multiplexed, true
DFS	6	6	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS, CMOS output interface type.
DRGND	1, 36	1, 36	I	Digital and output buffer ground
DRVDD	2, 35	2, 35	I	1.8-V digital and output buffer supply
INM	16	16	I	Differential analog input, negative
INP	15	15	I	Differential analog input, positive
NC	31, 32	31-34	—	Do not connect
OE	7	7	I	Output buffer enable input, active high; this pin has an internal 100-kΩ pull-up resistor to DRVDD.
OVR_SDOUT	3	3	O	This pin functions as an out-of-range indicator after reset, when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1. This pin is a 1.8-V CMOS output pin (running off of DRVDD).
RESERVED	23	23	I	Digital control pin, reserved for future use
RESET	30	30	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; see the *Serial Interface* section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SDATA can be used as a control pin. RESET has an internal 100-kΩ pull-down resistor.
SCLK	29	29	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and must be tied to ground. This pin has an internal 180-kΩ pull-down resistor
SDATA	28	28	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 7). This pin has an internal 180-kΩ pull-down resistor.
SEN	27	27	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and must be tied to AVDD. This pin has an internal 180-kΩ pull-up resistor to AVDD.
VCM	13	13	O	Outputs the common-mode voltage that can be used externally to bias the analog input pins.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage range, AVDD		–0.3	2.1	V
Supply voltage range, AVDD_BUF		–0.3	3.9	V
Supply voltage range, DRVDD		–0.3	2.1	V
Voltage between AGND and DRGND		–0.3	0.3	V
Voltage between AVDD to DRVDD (when AVDD leads DRVDD)		–2.4	2.4	V
Voltage between DRVDD to AVDD (when DRVDD leads AVDD)		–2.4	2.4	V
Voltage between AVDD_BUF to DRVDD, AVDD		–4.2	4.2	V
Voltage applied to input pins	INP, INM	–0.3	Minimum (1.9, AVDD + 0.3)	V
	CLKP, CLKM(2)	–0.3	AVDD + 0.3	
	RESET, SCLK, SDATA, SEN, DFS	–0.3	3.6	
Temperature	Operating free-air, T_A	–40	125	°C
	Operating junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, switching off the input clock (or ensuring the voltage on CLKP, CLKM is less than |0.3 V|) is recommended. Doing so prevents the ESD protection diodes at the clock input pins from turning on.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
AVDD_BUF	Analog buffer supply voltage		3	3.3	3.6	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
	Differential input voltage range(1)			1.5		V_{PP}
	Input common-mode voltage			1.7 ± 0.05		V
	Maximum analog input frequency with 1.5-V_{PP} input amplitude(2)			400		MHz
	Maximum analog input frequency with 1-V_{PP} input amplitude(2)			600		MHz
CLOCK INPUT						
	Low-speed mode enabled(3)		20		80	MSPS
	Low-speed mode disabled(3)		> 80		250	MSPS
	Input clock amplitude differential (V_{CLKP} – V_{CLKM})					
	Sine wave, ac-coupled		0.2	1.5		V_{PP}
	LVPECL, ac-coupled			1.6		V_{PP}
	LVDS, ac-coupled			0.7		V_{PP}
	LVCMOS, single-ended, ac-coupled			1.8		V
	Input clock duty cycle	Low-speed mode enabled	40%	50%	60%	
		Low-speed mode disabled	35%	50%	65%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)			100		Ω
T_J	Operating junction temperature	Recommended			108	°C
		Maximum rated(4)			125	

(1) With 0-dB gain. See the *Gain for SFDR, SNR Trade-Off* section in *Feature Description* for the relationship between input voltage range and gain.
(2) See the *Overview* section in the *Detailed Description*.
(3) See the *Serial Interface* section for details on the low-speed mode.
(4) Prolonged use at this junction temperature can increase the device failure-in-time (FIT) rate.

6.4 Thermal Information

THERMAL METRIC(1)		ADS41B29, ADS41B49 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: General

Typical values are at T_A = 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, and 50% clock duty cycle, unless otherwise noted. Minimum and maximum values are across the full ambient temperature range: $T_{A, MIN}$ = –40°C to $T_{A, MAX}$ = 85°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Differential input voltage range			1.5		V_{PP}
	Differential input resistance	At dc (see Figure 83)		10		kΩ
	Differential input capacitance (see Figure 84)			3.5		pF
	Analog input bandwidth			800		MHz
	Analog input common-mode current (per input pin)			2		µA
VCM	Common-mode output voltage			1.7		V
	VCM output current capability			4		mA
DC ACCURACY						
	Offset error		–15	2.5	15	mV
	Temperature coefficient of offset error			0.003		mV/°C
E_{GREF}	Gain error as a result of internal reference inaccuracy alone		–2		2	%FS
E_{GCHAN}	Gain error of channel alone			2.5		%FS
POWER SUPPLY						
IAVDD	Analog supply current			99.5	115	mA
IAVDD_BUF	Analog input buffer supply current			29	42	mA
IDRVDD	Output buffer supply current(2)	LVDS interface with 100-Ω external termination, low LVDS swing (200 mV)		63		mA
		LVDS interface with 100-Ω external termination, standard LVDS swing (350 mV)		75	90	
	IDRVDD output buffer supply current(2)(3)	CMOS interface(3), 8-pF external load capacitance, f_{IN} = 2.5 MHz		35		mA
	Global power-down			10	25	mW
	Standby			200		mW

(1) Minimum values for ADS41B49 are specified across the ambient temperature range of –40°C to +105°C.
(2) The maximum DRVDD current with CMOS interface depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance on each digital output line is 10 pF.
(3) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see the *CMOS Interface Power Dissipation* section in the *Feature Description*).

6.6 Electrical Characteristics: ADS41B29, ADS41B49

Typical values are at T_A = 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, 1.5-V_{PP} clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full ambient temperature range: $T_{A, MIN}$ = –40°C to $T_{A, MAX}$ = 85°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS41B29			ADS41B49(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Resolution				12			14	Bits
SNR	Signal-to-noise ratio, LVDS	f_{IN} = 20 MHz		68.4			69.7		dBFS
		f_{IN} = 70 MHz		68.3			69.5		
		f_{IN} = 100 MHz		68.3			69.5		
		f_{IN} = 170 MHz	65.5	68		66.5	69.1		
		f_{IN} = 300 MHz		67.5			68.4		
SINAD	Signal-to-noise and distortion ratio, LVDS	f_{IN} = 20 MHz		68.3			69.5		dBFS
		f_{IN} = 70 MHz		68.1			69.3		
		f_{IN} = 100 MHz		68.2			69.3		
		f_{IN} = 170 MHz	65	67.8		66	68.8		
		f_{IN} = 300 MHz		66.5			67.4		
SFDR	Spurious-free dynamic range	f_{IN} = 20 MHz		89			89		dBc
		f_{IN} = 70 MHz		85			85		
		f_{IN} = 100 MHz		87			87		
		f_{IN} = 170 MHz	71	82		72	82		
		f_{IN} = 300 MHz		75			75		
THD	Total harmonic distortion	f_{IN} = 20 MHz		85			85		dBc
		f_{IN} = 70 MHz		82			82		
		f_{IN} = 100 MHz		83			83		
		f_{IN} = 170 MHz	68	79.5		69	79.5		
		f_{IN} = 300 MHz		72			72		
HD2	Second-order harmonic distortion	f_{IN} = 20 MHz		93			93		dBc
		f_{IN} = 70 MHz		85			85		
		f_{IN} = 100 MHz		87			87		
		f_{IN} = 170 MHz	71	87		72	87		
		f_{IN} = 300 MHz		80			80		
HD3	Third-order harmonic distortion	f_{IN} = 20 MHz		93			93		dBc
		f_{IN} = 70 MHz		88			88		
		f_{IN} = 100 MHz		88			88		
		f_{IN} = 170 MHz	71	82		72	82		
		f_{IN} = 300 MHz		75			75		
	Worst spur (other than second- and third-order harmonics)	f_{IN} = 20 MHz		89			89		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	76	88		77.5	88		
		f_{IN} = 300 MHz		88			88		
IMD	Two-tone intermodulation distortion	f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		–86			–86		dBFS
	Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine-wave input		1			1		Clock cycles
PSRR	AC power-supply rejection ratio	For 100-mV_{PP} signal on AVDD supply, up to 10 MHz		> 30			> 30		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11			11.2		LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±1.5	±3.5		±2.5	±5	LSBs

(1) Minimum values for the ADS41B49 are specified across the ambient temperature range of –40°C to +105°C.

6.7 Digital Characteristics[1]

Typical values are at T_A = 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V, unless otherwise noted. Minimum and maximum values are across the full ambient temperature range: $T_{A, MIN}$ = –40°C to $T_{A, MAX}$ = 85°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, OE)							
	High-level input voltage		RESET, SCLK, SDATA, and SEN support 1.8-V and 3.3-V CMOS logic levels	1.3			V
			OE only supports 1.8-V CMOS logic levels	1.3			V
	Low-level input voltage		RESET, SCLK, SDATA, and SEN support 1.8-V and 3.3-V CMOS logic levels			0.4	V
			OE only supports 1.8-V CMOS logic levels			0.4	V
	High-level input current	SDATA, SCLK[2]	V_{HIGH} = 1.8 V		10		µA
		SEN[3]	V_{HIGH} = 1.8 V		0		µA
	Low-level input current	SDATA, SCLK	V_{LOW} = 0 V		0		µA
		SEN	V_{LOW} = 0 V		–10		µA
DIGITAL OUTPUTS (CMOS INTERFACE: D0 TO D13, OVR_SDOUT)							
	High-level output voltage			DRVDD – 0.1	DRVDD		V
	Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS (LVDS INTERFACE: D0_D1_P/M to D12_D13_P/M, CLKOUTP/M)							
V_{ODH}	High-level output voltage[4]		Standard swing LVDS	270	350	430	mV
			Low swing LVDS		200		mV
V_{ODL}	Low-level output voltage[4]		Standard swing LVDS	–430	–350	–270	mV
			Low swing LVDS		–200		mV
V_{OCM}	Output common-mode voltage			0.85	1.05	1.25	V

(1) Minimum values for ADS41B49 are specified across the ambient temperature range of –40°C to +105°C.
(2) SDATA and SCLK have an internal 180-kΩ pull-down resistor.
(3) SEN has an internal 180-kΩ pull-up resistor to AVDD.
(4) With an external 100-Ω termination.

6.8 Timing Requirements: LVDS and CMOS Modes

Typical values are at T_A = 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine-wave input clock, C_{LOAD} = 5 pF(1), and R_{LOAD} = 100 Ω(2), unless otherwise noted. Minimum and maximum values are across the full ambient temperature range: $T_{A, MIN}$ = –40°C to $T_{A, MAX}$ = 85°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, and DRVDD = 1.7 V to 1.9 V.(3)

			MIN	TYP	MAX	UNIT
GENERAL						
t_A	Aperture delay		0.6	0.8	1.2	ns
	Variation of aperture delay between two devices at the same temperature and DRVDD supply			±100		ps
t_J	Aperture jitter			100		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		5	25	µs
		Time to valid data after coming out of PDN GLOBAL mode		100	500	
	ADC latency(4)	Gain enabled (default after reset)		21		Clock cycles
		Gain and offset correction enabled		22		
DDR LVDS MODE						
t_{SU}	Data setup time(2): data valid(5) to zero-crossing of CLKOUTP		0.75(6)	1.1		ns
t_H	Data hold time(2): zero-crossing of CLKOUTP to data becoming invalid(5)		0.35(7)	0.6		ns
t_{PDI}	Clock propagation delay: input clock rising edge cross-over to output clock rising edge cross-over, *1 MSPS ≤ sampling frequency ≤ 250 MSPS*		3	4.2	5.4	ns
	Variation of t_{PDI} between two devices at the same temperature and DRVDD supply			±0.6		ns
	LVDS bit clock duty cycle of differential clock, (CLKOUTP – CLKOUTM), *1 MSPS ≤ sampling frequency ≤ 250 MSPS*		42%	48%	54%	
t_{RISE}, t_{FALL}	Data rise and fall time: rise time measured from –100 mV to +100 mV, fall time measured from +100 mV to –100 mV, *1 MSPS ≤ sampling frequency ≤ 250 MSPS*			0.14		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise and fall time: rise time measured from –100 mV to +100 mV, fall time measured from +100 mV to –100 mV, *1 MSPS ≤ sampling frequency ≤ 250 MSPS*			0.14		ns
t_{OE}	Output enable (OE) to data delay time to valid data after OE becomes active			50	100	ns
PARALLEL CMOS MODE(8)						
t_{START}	Input clock to data delay: input clock rising edge cross-over to start of data valid(5)				1.6	ns
t_{DV}	Data valid time interval of valid data(5)		2.5	3.2		ns
t_{PDI}	Clock propagation delay: input clock rising edge cross-over to, output clock rising edge cross-over, *1 MSPS ≤ sampling frequency ≤ 200 MSPS*		4	5.5	7	ns
	Output clock duty cycle of output clock (CLKOUT), *1 MSPS ≤ sampling frequency ≤ 200 MSPS*			47%		
t_{RISE}, t_{FALL}	Data rise and fall time: rise time measured from 20% to 80% of DRVDD, fall time measured from 80% to 20% of DRVDD, *1 MSPS ≤ sampling frequency ≤ 250 MSPS*			0.35		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise and fall time: rise time measured from 20% to 80% of DRVDD, fall time measured from 80% to 20% of DRVDD, *1 MSPS ≤ sampling frequency ≤ 200 MSPS*			0.35		ns
t_{OE}	Output enable (OE) to data delay time to valid data after OE becomes active			20	40	ns

(1) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(2) R_{LOAD} is the differential load resistance between the LVDS output pair.
(3) Timing parameters are ensured by design and characterization but are not production tested.
(4) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(5) Data valid refers to a logic high of 1.26 V and a logic low of 0.54 V.
(6) For an ambient temperature range of –40°C to +105°C, the minimum value of setup time reduces to 0.7 ns.
(7) For an ambient temperature range of –40°C to +105°C, the minimum value of setup time reduces to 0.3 ns.
(8) For f_S > 200 MSPS, using an external clock is recommended for data capture instead of the device output clock signal (CLKOUT).

6.9 Timing Requirements: Reset

Typical values at T_A = 25°C and minimum and maximum values across the full ambient temperature range: $T_{A, MIN}$ = –40°C to $T_{A, MAX}$ = 85°C, unless otherwise noted.(1)

		MIN	TYP	MAX	UNIT
t_1	Power-on delay from power-up of AVDD and DRVDD to RESET pulse active	1			ms
t_2	Reset pulse duration of active RESET signal that resets the serial registers	10			ns
				1(2)	µs
t_3	Delay from RESET disable to SEN active	100			ns

(1) For the ADS41B49, the minimum and maximum values are given for the ambient temperature range of $T_{A, MIN}$ = –40°C to $T_{A, MAX}$ = 105°C.
(2) The reset pulse is needed only when using the serial interface configuration. If the pulse width is greater than 1 µs, the device could enter the parallel configuration mode briefly and then return back to serial interface mode.

6.10 Timing Requirements: LVDS Timing Across Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)			HOLD TIME (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
230	0.85	1.25		0.35	0.6	
200	1.05	1.55		0.35	0.6	
185	1.1	1.7		0.35	0.6	
160	1.6	2.1		0.35	0.6	
125	2.3	3		0.35	0.6	
80	4.5	5.2		0.35	0.6	

6.11 Timing Requirements: CMOS Timing Across Sampling Frequencies

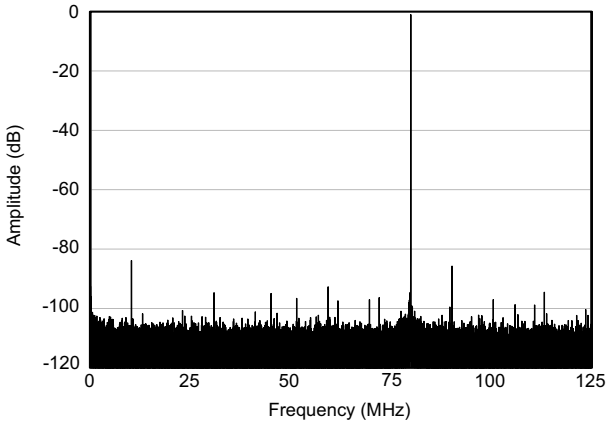
SAMPLING FREQUENCY (MSPS)	TIMING SPECIFIED WITH RESPECT TO OUTPUT CLOCK								
	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
200	1	1.6		2	2.8		4	5.5	7
185	1.3	2		2.2	3		4	5.5	7
160	1.8	2.5		2.5	3.3		4	5.5	7
125	2.5	3.2		3.5	4.3		4	5.5	7
80	4.8	5.5		5.7	6.5		4	5.5	7

6.12 Timing Requirements: CMOS Timing Across Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	TIMING SPECIFIED WITH RESPECT TO INPUT CLOCK					
	t_{START} (ns)			t_{DV} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
250			1.6	2.5	3.2	
230			1.1	2.9	3.5	
200			0.3	3.5	4.2	
185			0	3.9	4.5	
170			–1.3	4.3	5	

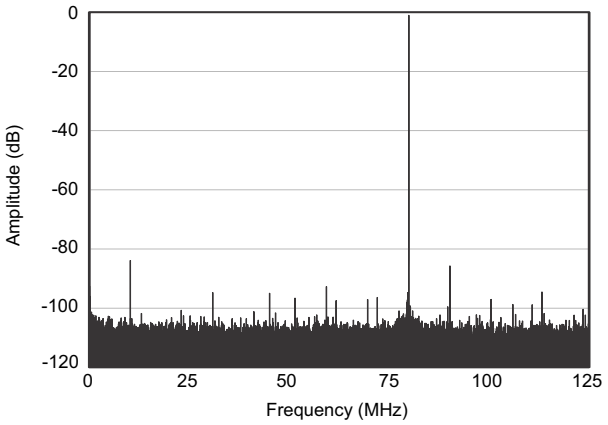
6.13 Typical Characteristics: ADS41B49

At 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.



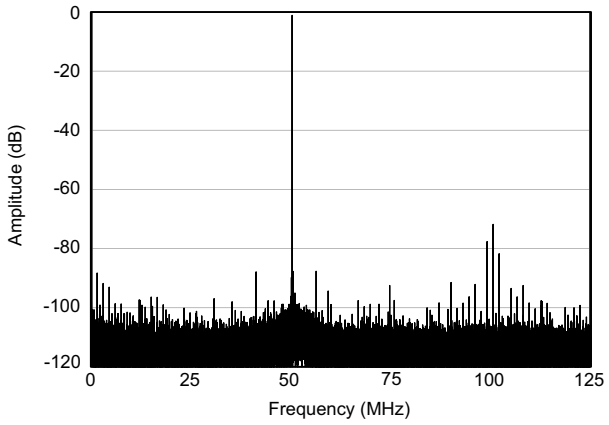
SFDR = 90.3 dBc, SNR = 69.9 dBFS, SINAD = 69.8 dBFS, THD = 85.2 dBc

Figure 1. FFT for 20-MHz Input Signal



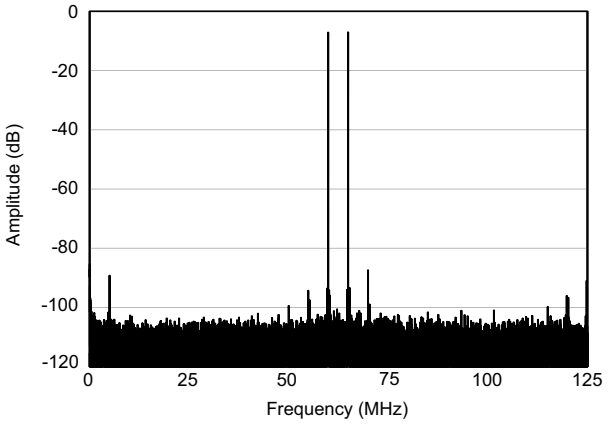
SFDR = 82.9 dBc, SNR = 69.3 dBFS, SINAD = 69 dBFS, THD = 80.3 dBc

Figure 2. FFT for 170-MHz Input Signal



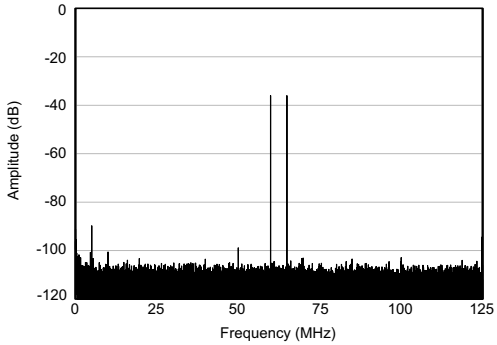
SFDR = 70.7 dBc, SNR = 68.4 dBFS, SINAD = 66.3 dBFS, THD = 69.3 dBc

Figure 3. FFT for 300-MHz Input Signal



Each tone at –7-dBFS amplitude, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, two-tone IMD = 87.3 dBFS, SFDR = 96.0 dBFS

Figure 4. FFT for Two-Tone Input Signal



Each tone at –36-dBFS amplitude, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, two-tone IMD = 89.7 dBFS, SFDR = 106.4 dBFS

Figure 5. FFT for Two-Tone Input Signal

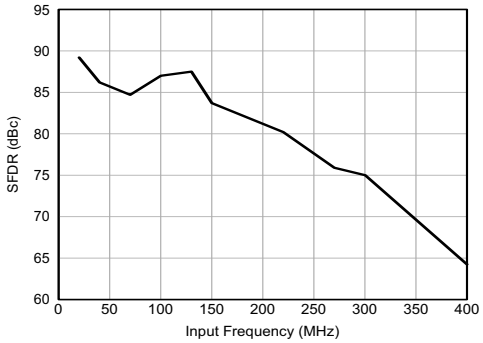


Figure 6. SFDR vs Input Frequency

Typical Characteristics: ADS41B49 (continued)

At 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

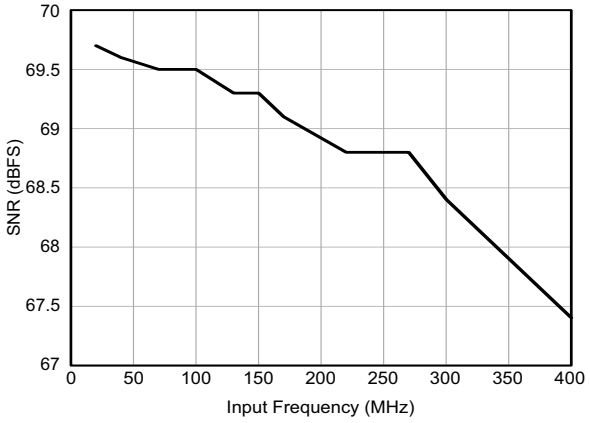


Figure 7. SNR vs Input Frequency

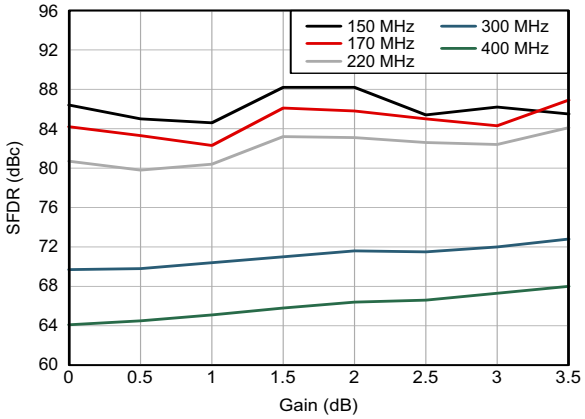


Figure 8. SFDR Across Gain and Input Frequency

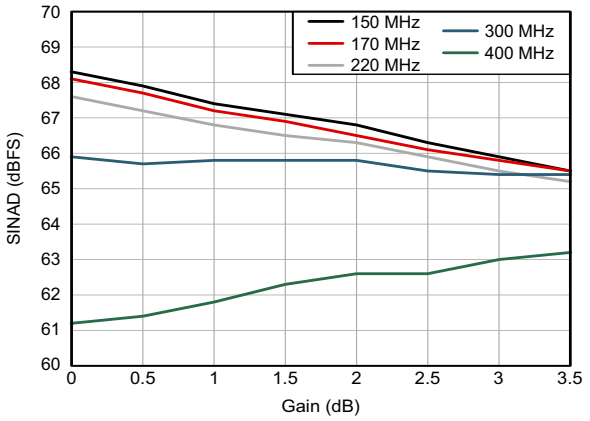
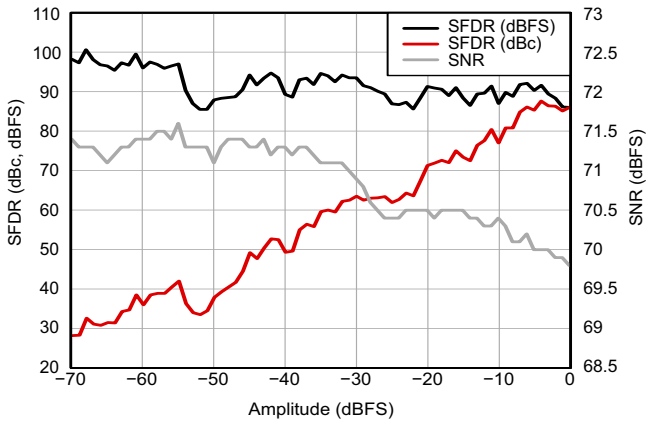
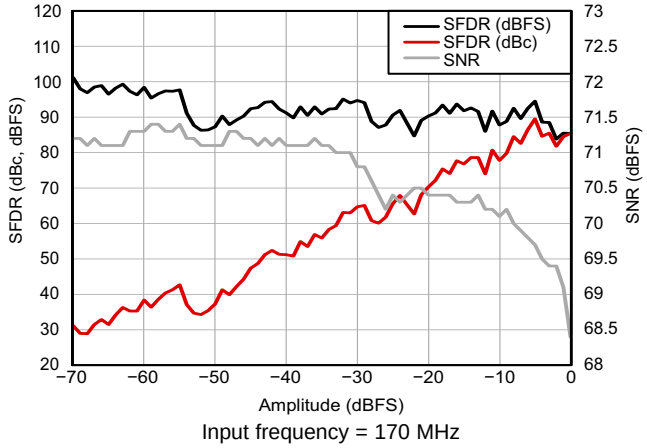


Figure 9. SINAD Across Gain and Input Frequency



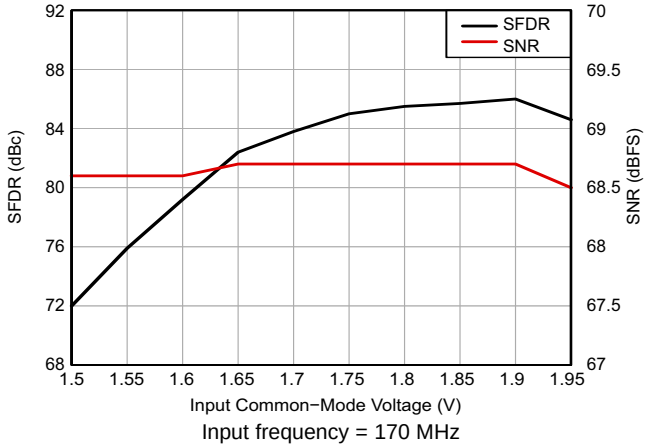
Input frequency = 40 MHz

Figure 10. Performance Across Input Amplitude (Single Tone)



Input frequency = 170 MHz

Figure 11. Performance Across Input Amplitude (Single Tone)



Input frequency = 170 MHz

Figure 12. Performance vs Input Common-Mode Voltage

Typical Characteristics: ADS41B49 (continued)

At 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

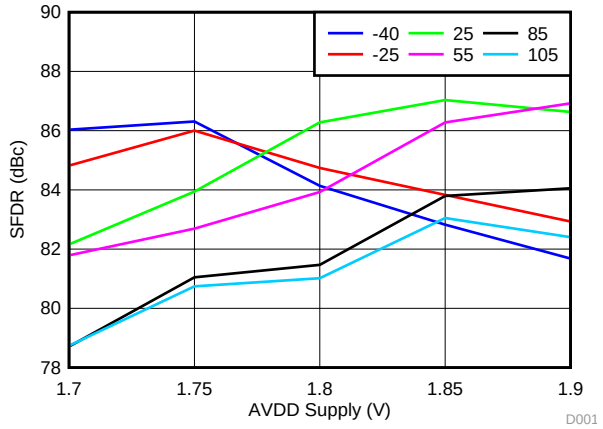


Figure 13. SFDR Across Ambient Temperature vs AVDD Supply

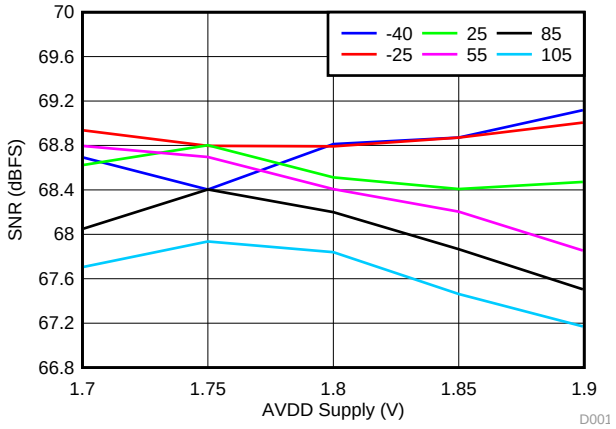


Figure 14. SNR Across Ambient Temperature vs AVDD Supply

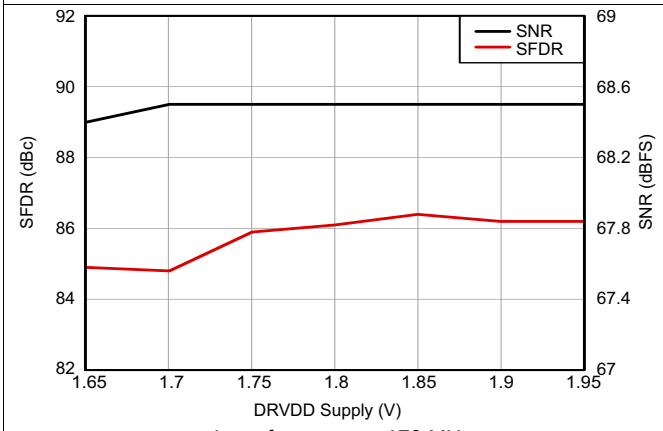


Figure 15. Performance Across DRVDD Supply Voltage

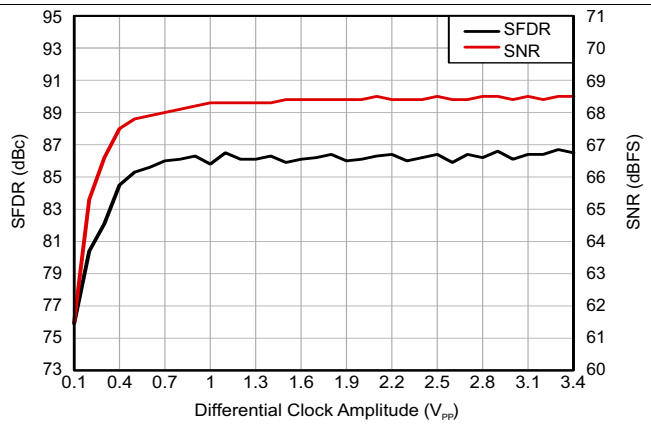


Figure 16. Performance Across Input Clock Amplitude

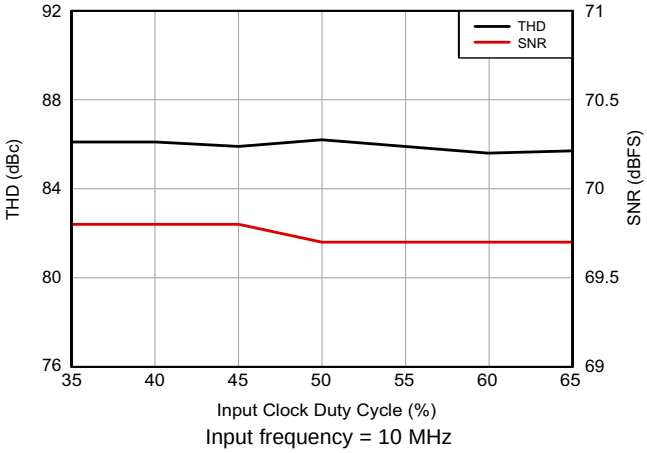


Figure 17. Performance Across Input Clock Duty Cycle

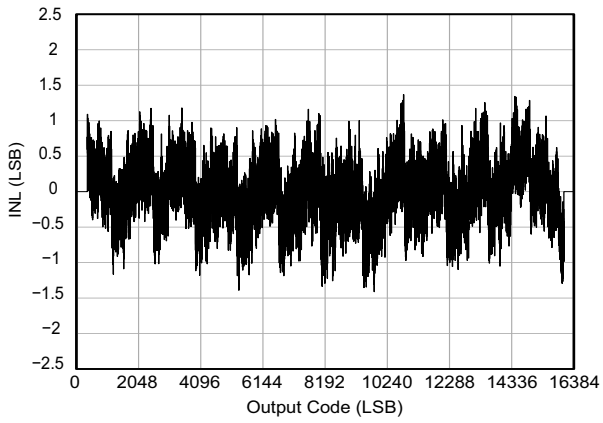
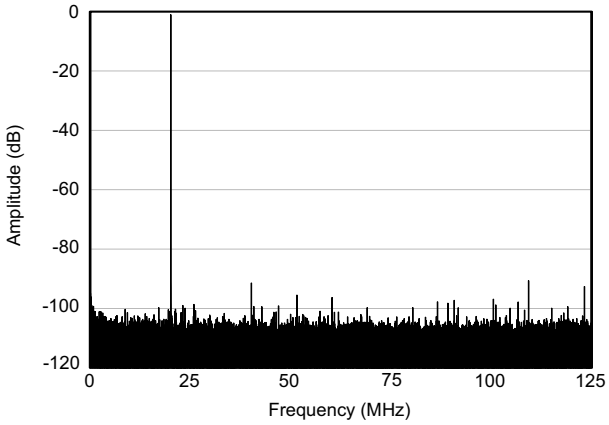


Figure 18. Integral Nonlinearity

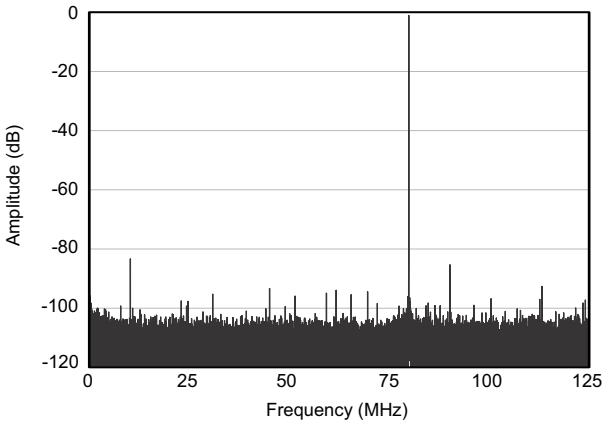
6.14 Typical Characteristics: ADS41B29

At 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.



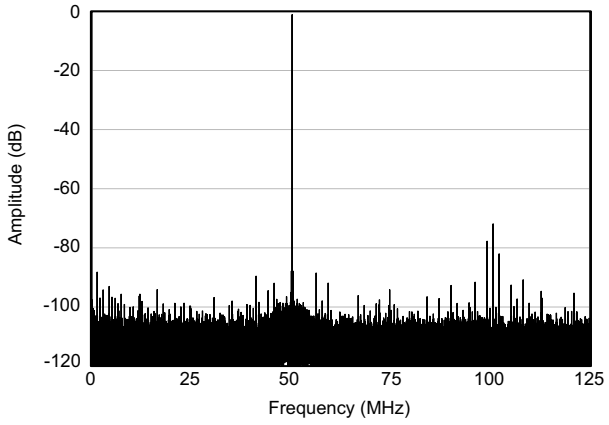
SFDR = 89.6 dBc, SNR = 68.6 dBFS, SINAD = 68.5 dBFS, THD = 85.2 dBc

Figure 19. FFT for 20-MHz Input Signal



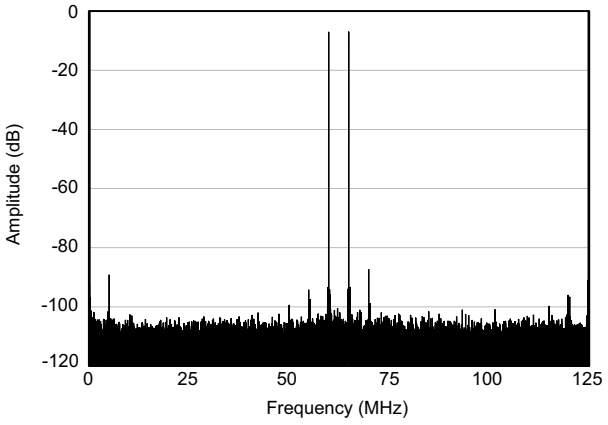
SFDR = 82.3 dBc, SNR = 68.1 dBFS, SINAD = 67.8 dBFS, THD = 79.9 dBc

Figure 20. FFT for 170-MHz Input Signal



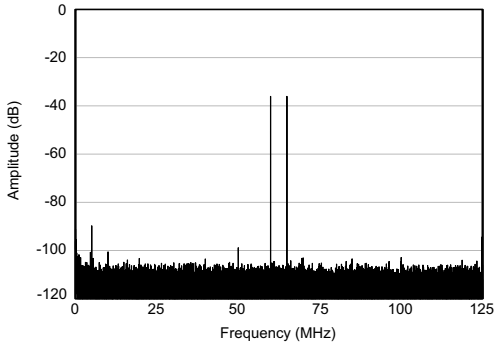
SFDR = 70.8 dBc, SNR = 67.4 dBFS, SINAD = 65.7 dBFS, THD = 69.4 dBc

Figure 21. FFT for 300-MHz Input Signal



Each tone at –7-dBFS amplitude, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, two-tone IMD = 87.3 dBFS, SFDR = 85.9 dBFS

Figure 22. FFT for Two-Tone Input Signal



Each tone at –36-dBFS amplitude, f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, two-tone IMD = 89.8 dBFS, SFDR = 98.5 dBFS

Figure 23. FFT for Two-Tone Input Signal

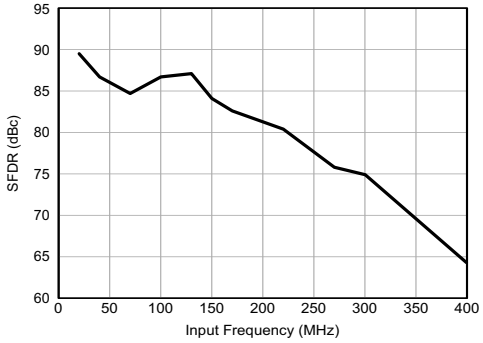


Figure 24. SFDR vs Input Frequency

Typical Characteristics: ADS41B29 (continued)

At 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

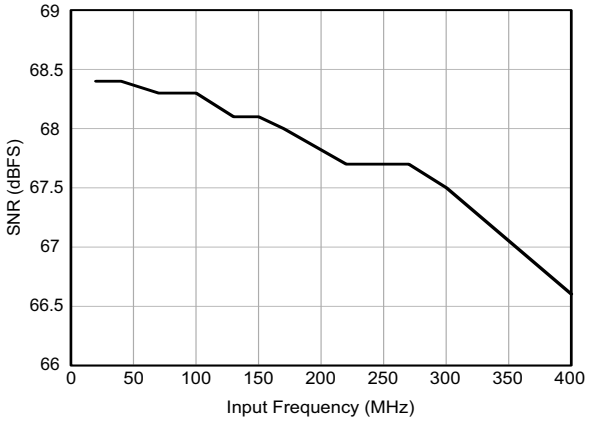


Figure 25. SNR vs Input Frequency

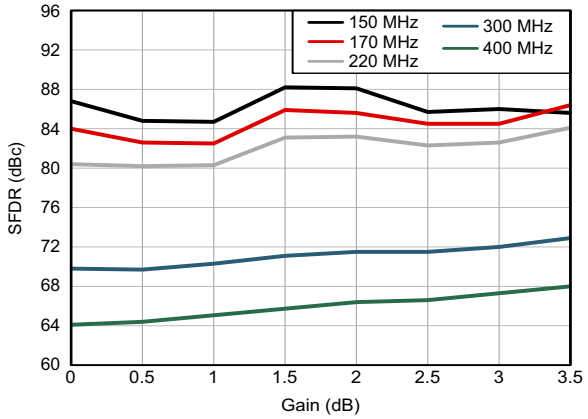


Figure 26. SFDR Across Gain and Input Frequency

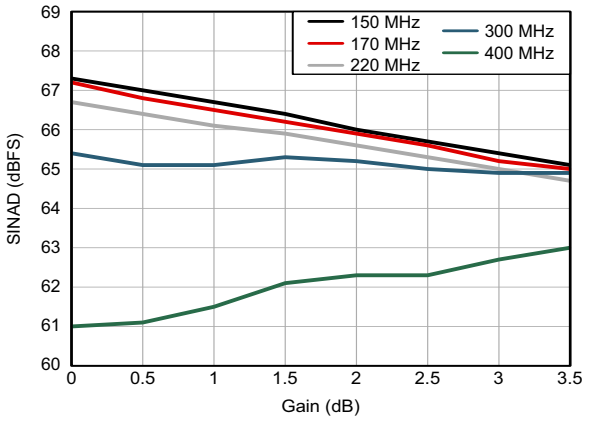
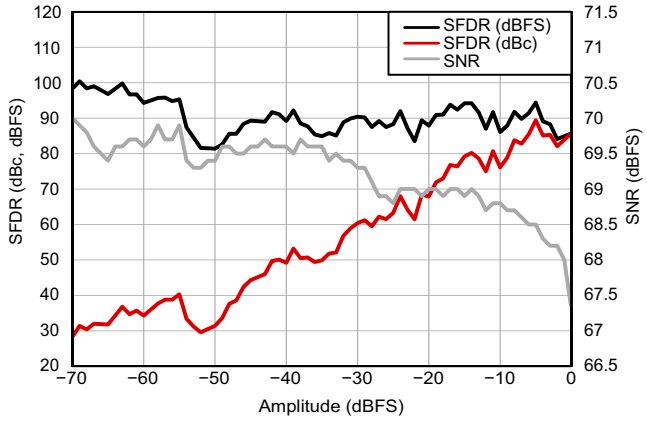
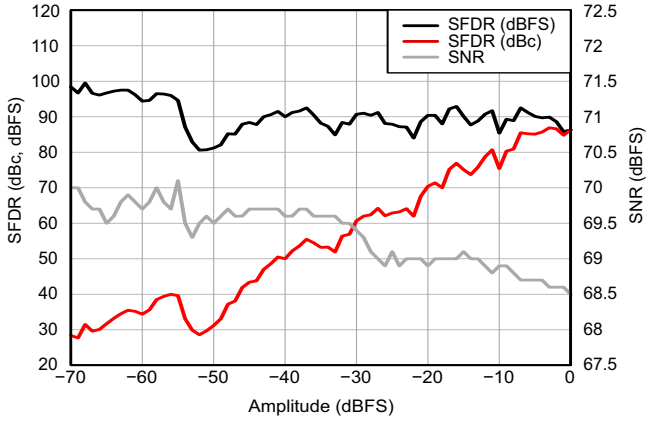


Figure 27. SINAD Across Gain and Input Frequency



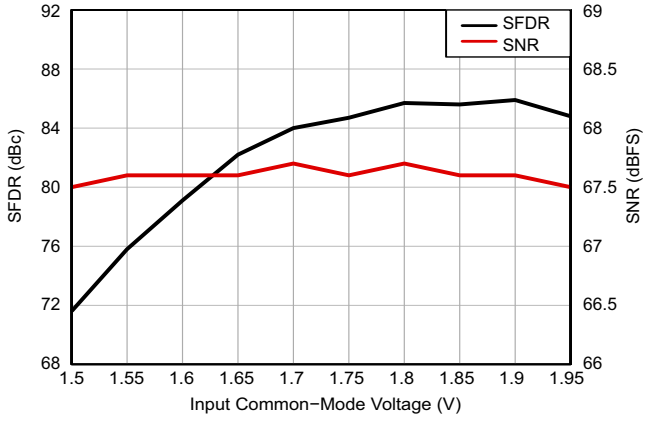
Input frequency = 170 MHz

Figure 28. Performance Across Input Amplitude (Single Tone)



Input frequency = 40 MHz

Figure 29. Performance Across Input Amplitude (Single Tone)



Input frequency = 170 MHz

Figure 30. Performance vs input Common-Mode Voltage

Typical Characteristics: ADS41B29 (continued)

At 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

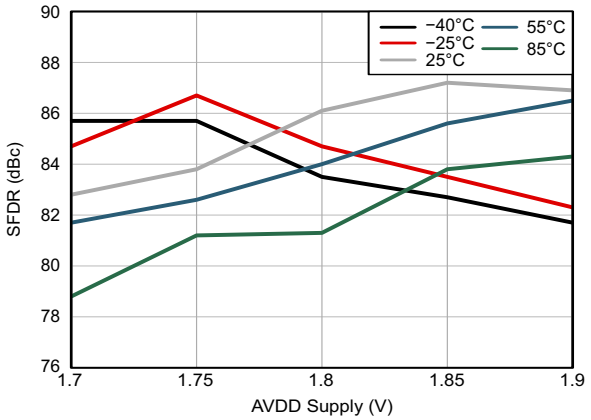


Figure 31. SFDR Across Ambient Temperature vs AVDD Supply

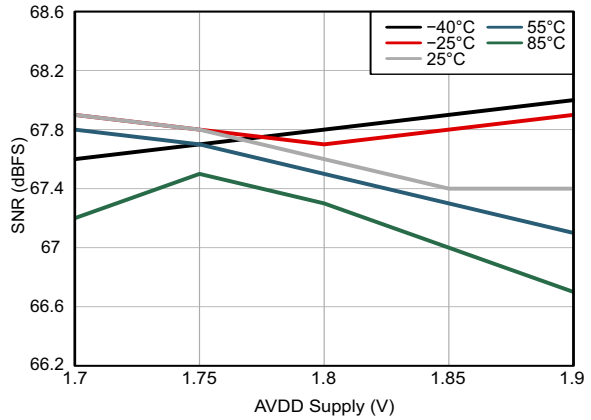


Figure 32. SNR Across Ambient Temperature vs AVDD Supply

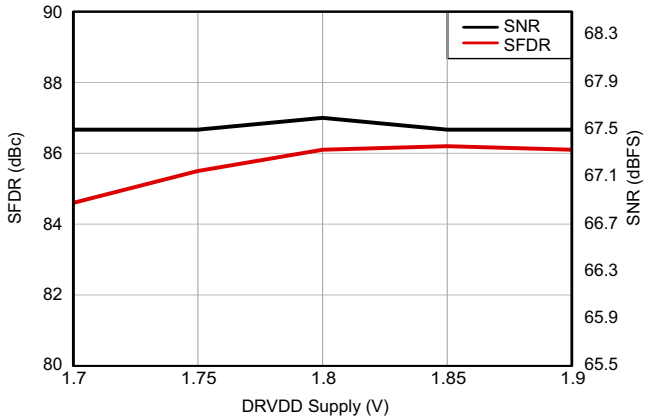


Figure 33. Performance Across DRVDD Supply Voltage

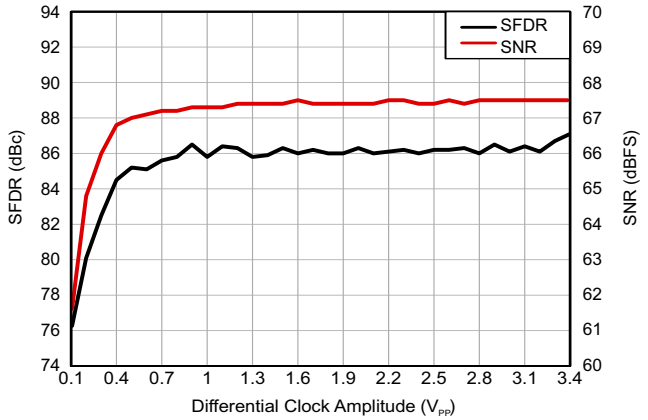


Figure 34. Performance Across Input Clock Amplitude

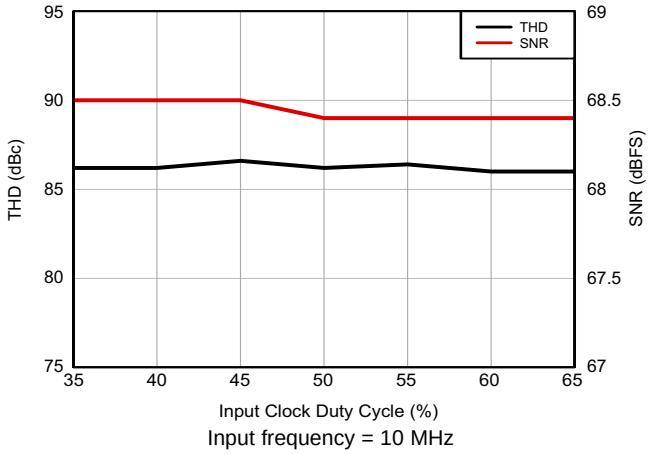
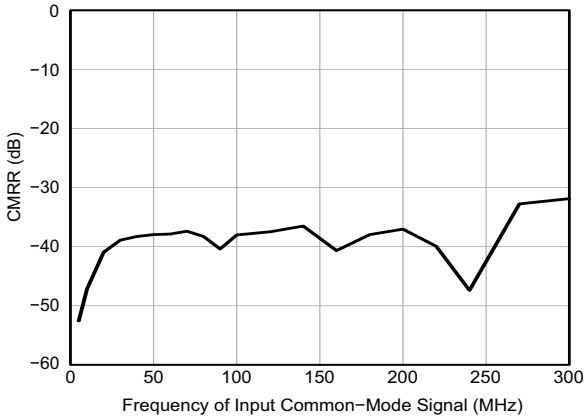


Figure 35. Performance Across Input Clock Duty Cycle

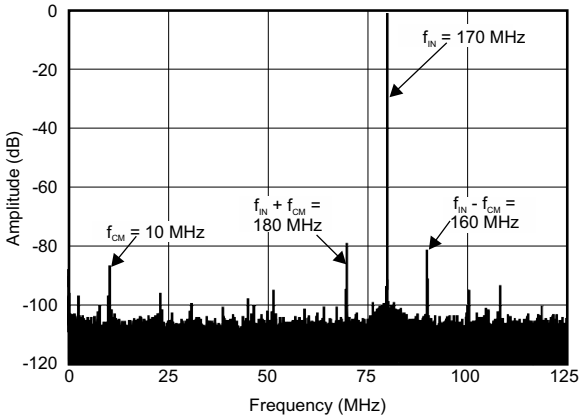
6.15 Typical Characteristics: General

At 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.



Input frequency = 170 MHz, 50-mV_{PP} signal superimposed on input common-mode voltage (1.7 V)

Figure 36. CMRR Across Frequency



f_{IN} = 170 MHz; f_{CM} = 10 MHz, 50 mV_{PP}; SFDR = 77.69 dB; amplitude: (f_{IN}) = –1 dBFS; (f_{CM}) = –93.8 dBFS; (f_{IN} + f_{CM}) = –78.8 dBFS; (f_{IN} – f_{CM}) = –81 dBFS

Figure 37. CMRR FFT

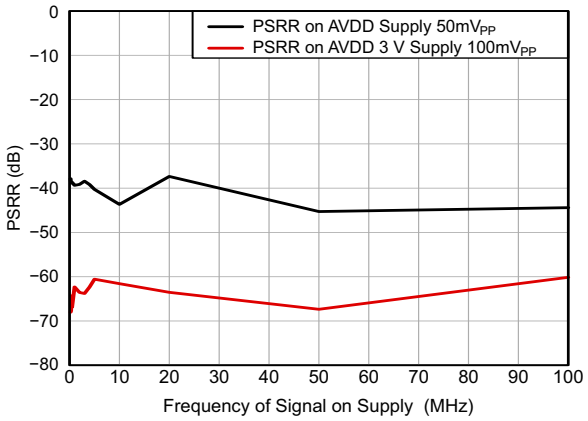
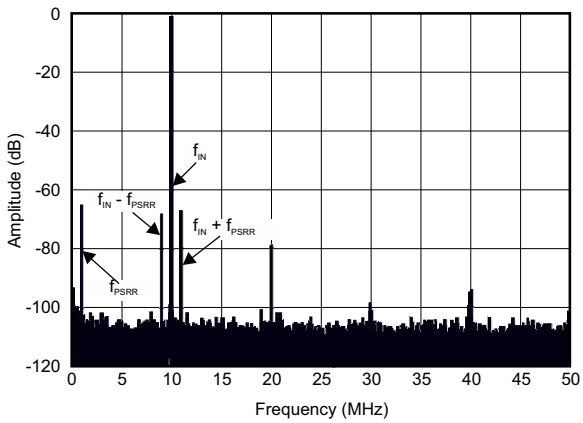


Figure 38. PSRR Across Frequency



f_{IN} = 10 MHz; f_{PSRR} = 10 MHz, 50 mV_{PP}; amplitude: (f_{IN}) = –1 dBFS; (f_{PSRR}) = –65.6 dBFS; (f_{IN} + f_{PSRR}) = –67.5 dBFS; (f_{IN} – f_{PSRR}) = –68.3 dBFS

Figure 39. PSRR FFT

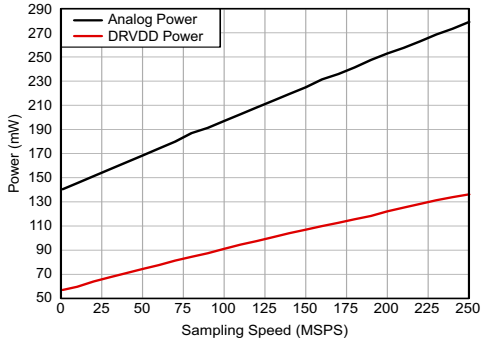


Figure 40. Power Across Sampling Frequency

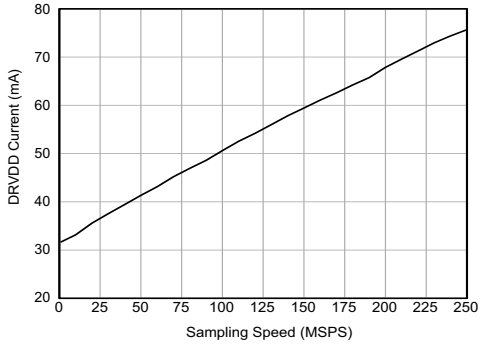


Figure 41. DRVDD Current Across Sampling Frequency

6.16 Typical Characteristics: Contour

At 25°C, AVDD = 1.8 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum-rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

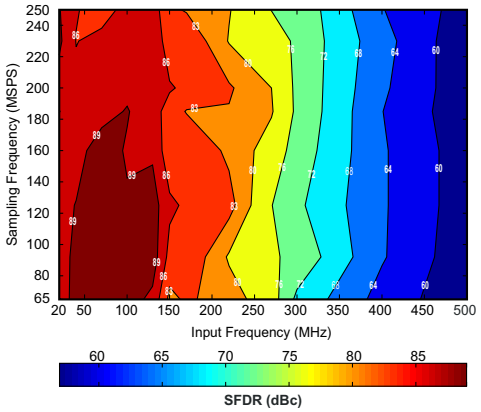


Figure 42. SFDR Contour (0-dB Gain, Applies to ADS41Bx9)

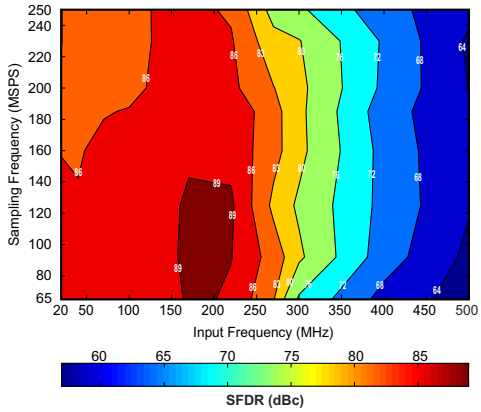


Figure 43. SFDR Contour (3.5-dB Gain, Applies to ADS41Bx9)

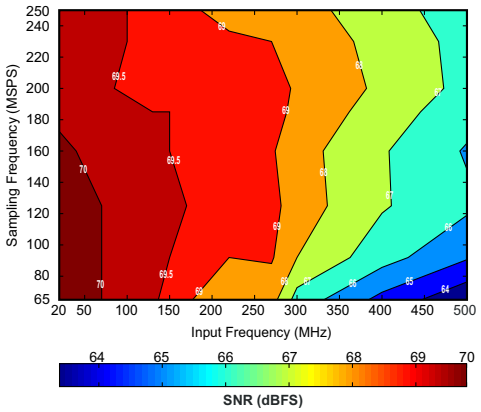


Figure 44. SNR Contour (0-dB Gain, Applies to ADS41B49)

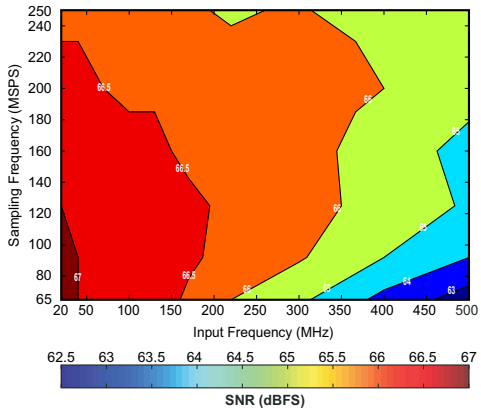


Figure 45. SNR Contour (3.5-dB Gain, Applies to ADS41B49)

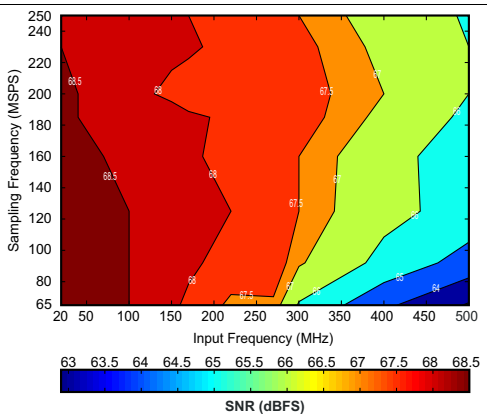


Figure 46. SNR Contour (0-dB Gain, Applies to ADS41B29)

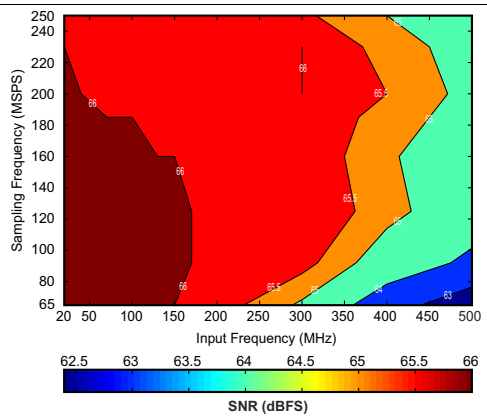
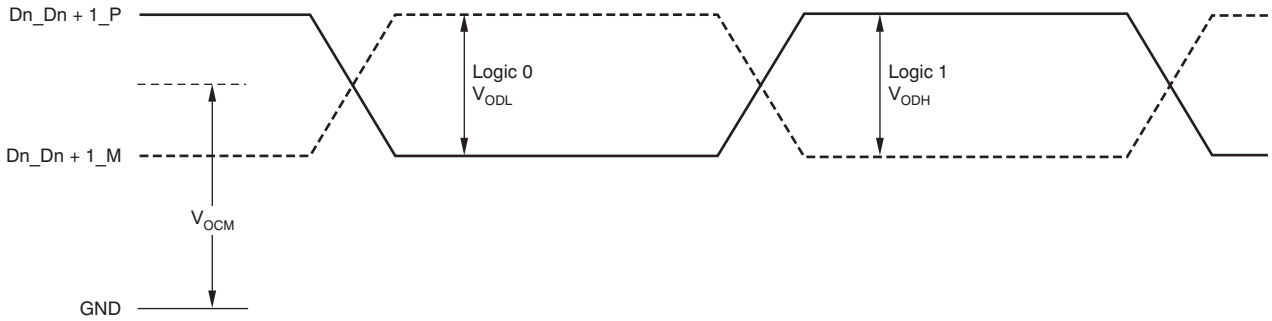


Figure 47. SNR Contour (0-dB Gain, Applies to ADS41B29)

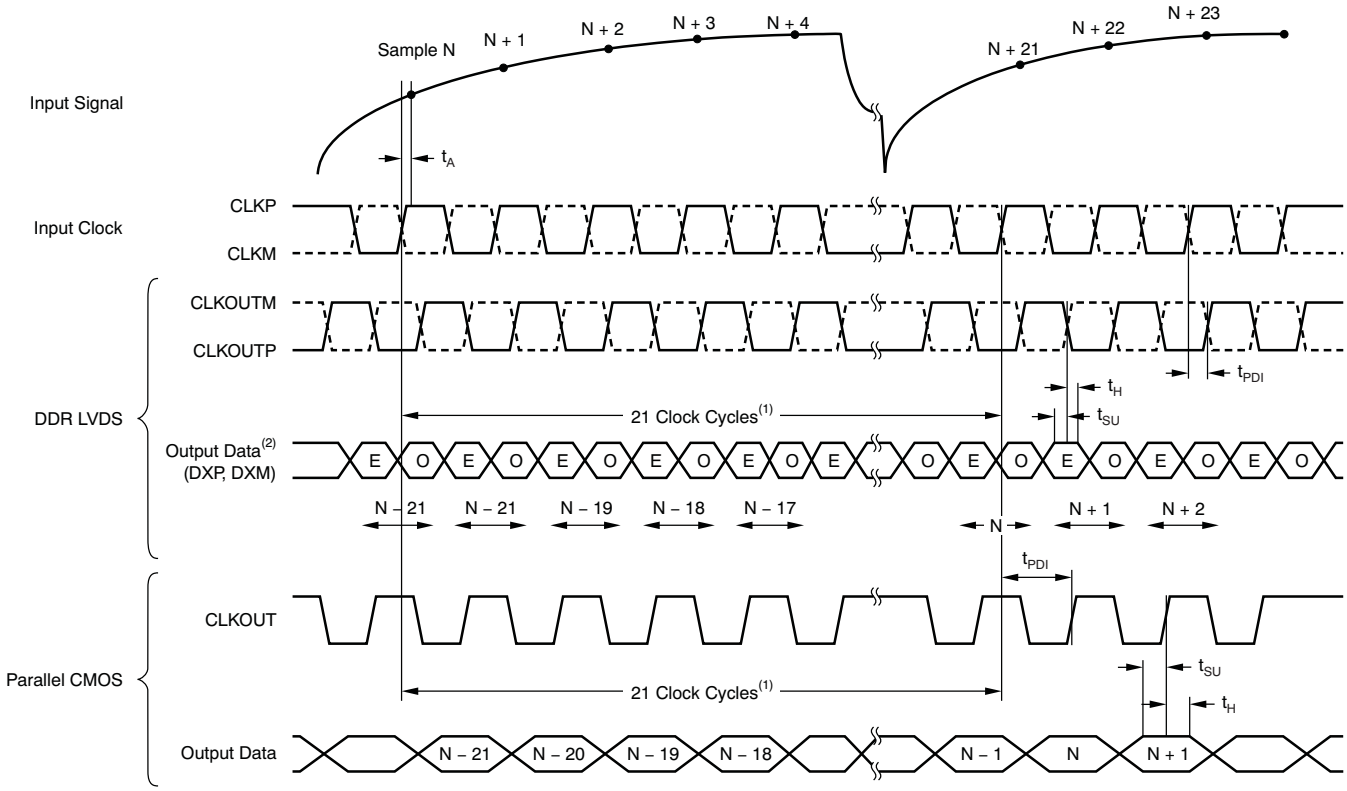
7 Parameter Measurement Information

7.1 Timing Diagrams



(1) With external 100-Ω termination.

Figure 48. LVDS Output Voltage Levels

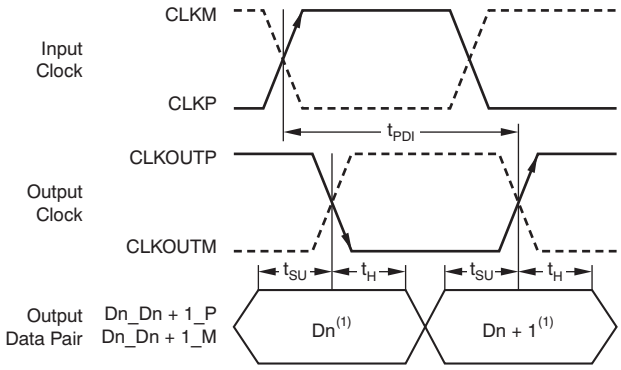


(1) At higher sampling frequencies, t_{DPI} is greater than one clock cycle which then makes the overall latency = ADC latency + 1.

(2) E = Even bits (D0, D2, D4, and so forth). O = Odd bits (D1, D3, D5, and so forth).

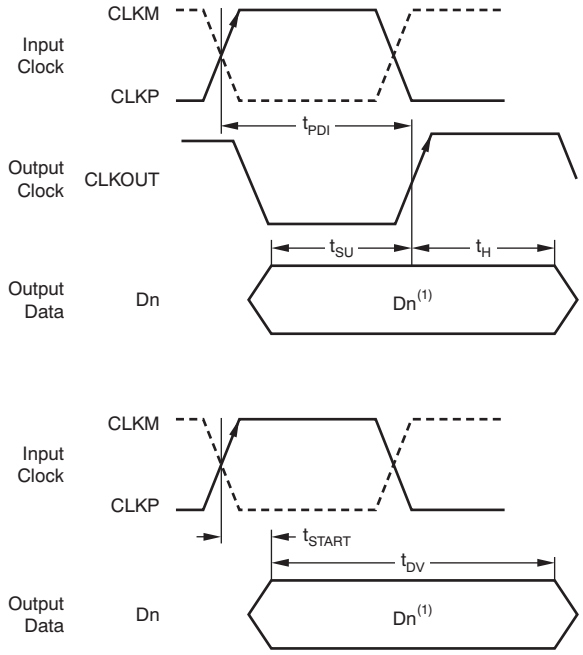
Figure 49. Latency Diagram

Timing Diagrams (continued)



(1) Dn = bits D0, D2, D4, and so forth. Dn + 1 = Bits D1, D3, D5, and so forth.

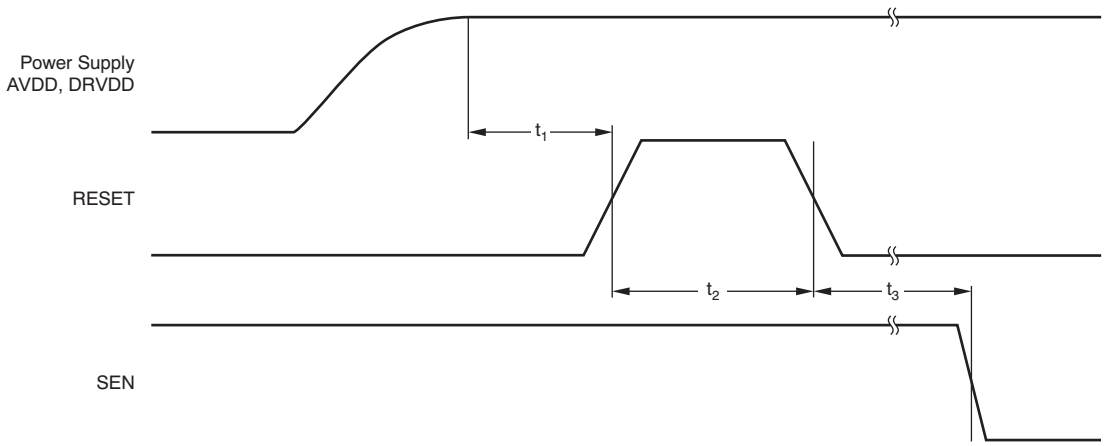
Figure 50. LVDS Mode Timing



Dn = bits D0, D1, D2, and so forth.

Figure 51. CMOS Mode Timing

Timing Diagrams (continued)



NOTE: A high pulse on the RESET pin is required in the serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 52. Reset Timing Diagram

8 Detailed Description

8.1 Overview

The ADS41Bx9 is a family of buffered analog input and ultralow power analog-to-digital converters (ADCs) with maximum sampling rates up to 250 MSPS. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 21 clock cycles. The output is available as 14-bit data or 12-bit data, in DDR LVDS mode or CMOS mode, and coded in either straight offset binary or binary twos complement format.

8.2 Functional Block Diagram

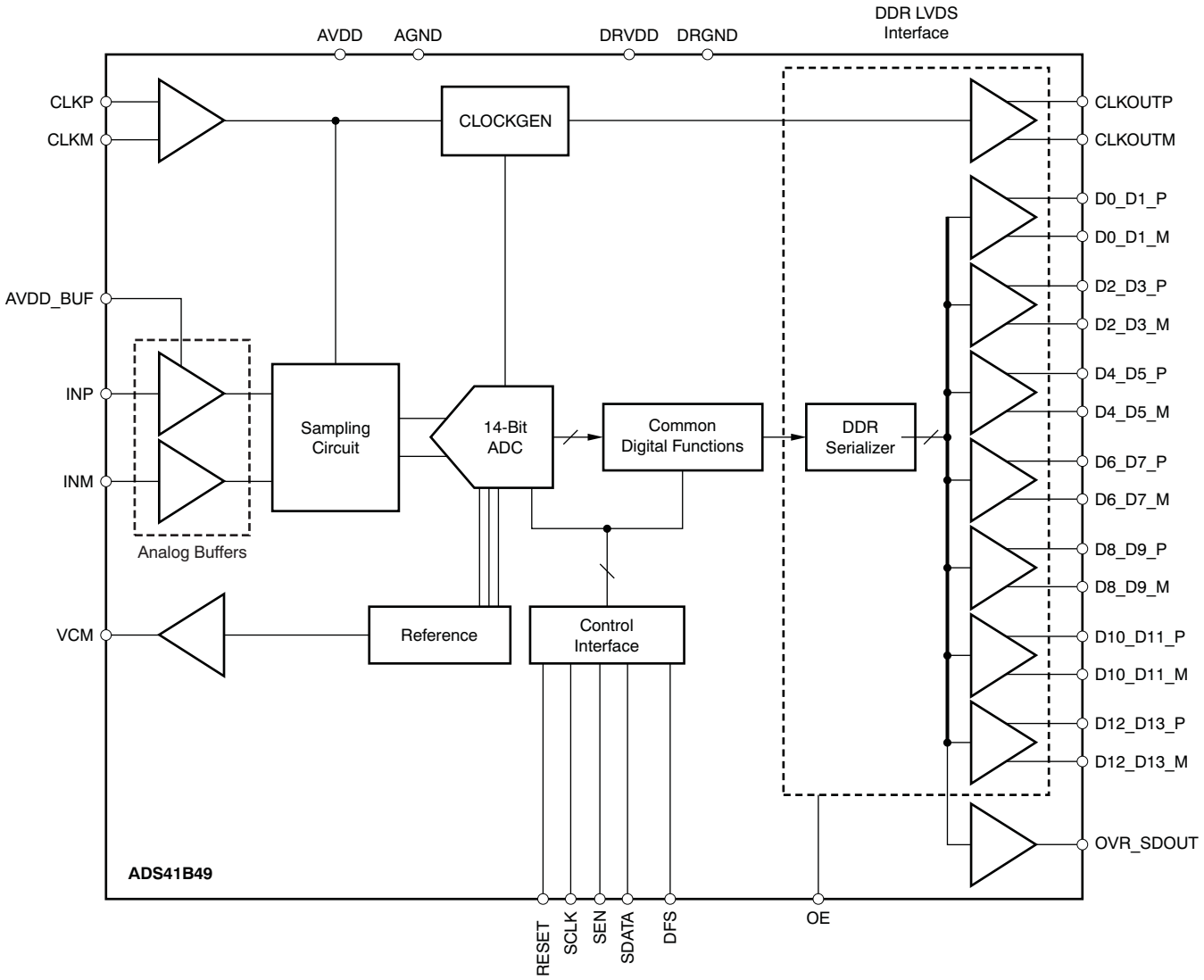


Figure 53. ADS41B49 Block Diagram

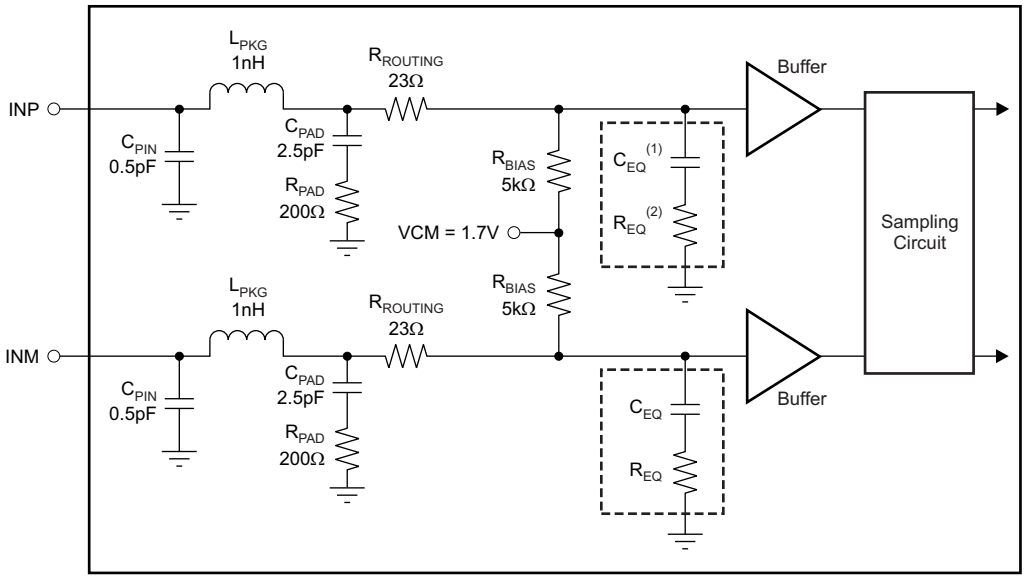
8.3 Feature Description

8.3.1 Analog Input

The analog input pins have analog buffers (running off the AVDD_BUF supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10-kΩ dc resistance and 3.5-pF input capacitance). The buffer helps to isolate the external driving source from the switching currents of the sampling circuit. This buffering makes driving the buffered inputs easy when compared to an ADC without the buffer.

The input common-mode is set internally using a 5-kΩ resistor from each input pin to 1.7 V, so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.375 V) and (VCM – 0.375 V), resulting in a 1.5-V_{PP} differential input swing.

The input sampling circuit has a high 3-dB bandwidth that extends up to 800 MHz (measured from the input pins to the sampled voltage). Figure 54 shows an equivalent circuit for the analog input.



(1) C_{EQ} refers to the equivalent input capacitance of the buffer = 4 pF.

(2) R_{EQ} refers to the R_{EQ} buffer = 10 Ω.

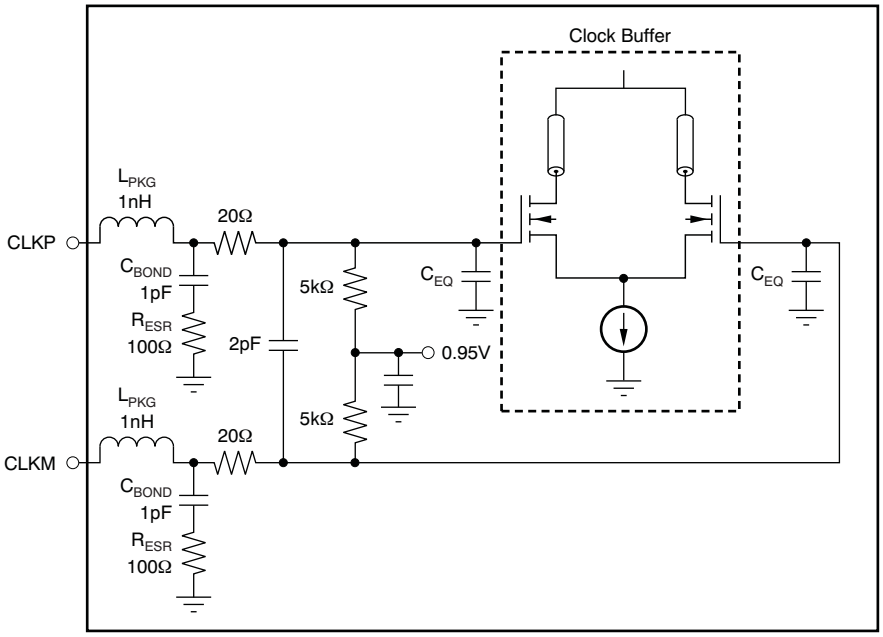
(3) This equivalent circuit is an approximation and valid for frequencies less than 700 MHz.

Figure 54. Analog Input Equivalent Circuit

Feature Description (continued)

8.3.2 Clock Input

The ADS41Bx9 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources. Figure 55 shows an equivalent circuit for the input clock.



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 55. Input Clock Equivalent Circuit

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 56. For best performance, the clock inputs must be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, using a clock source with very low jitter is recommended. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 57 shows a differential circuit.

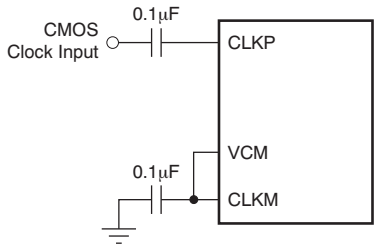


Figure 56. Single-Ended Clock Driving Circuit

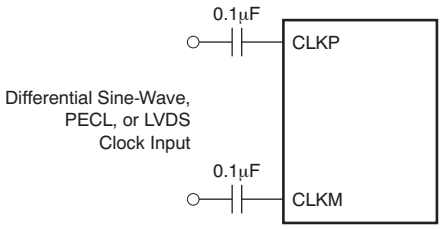


Figure 57. Differential Clock Driving Circuit

8.3.3 Gain for SFDR, SNR Trade-Off

The ADS41Bx9 includes gain settings that can be used to get improved SFDR performance. The gain is programmable from 0 dB to 3.5 dB (in 0.5-dB steps) using the GAIN register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 1.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5 dB and 1 dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used to trade-off between SFDR and SNR.

After a reset, the gain is enabled with 0dB gain setting. For other gain settings, program the GAIN register bits.

Table 1. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V_{PP})
0	Default after reset	1.5
0.5	Programmable gain	1.41
1	Programmable gain	1.33
1.5	Programmable gain	1.26
2	Programmable gain	1.19
2.5	Programmable gain	1.12
3	Programmable gain	1.06
3.5	Programmable gain	1

8.3.4 Offset Correction

The ADS41Bx9 has an internal offset correction algorithm that estimates and corrects dc offset up to ±10 mV. The correction can be enabled using the EN OFFSET CORR serial register bit. When enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 2.

Table 2. Time Constant of Offset Correction Loop

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1 / f_S$ (sec)(1)
0000	1M	4 ms
0001	2M	8 ms
0010	4M	16.7 ms
0011	8M	33.5 ms
0100	16M	67 ms
0101	32M	134 ms
0110	64M	268 ms
0111	128M	537 ms
1000	256M	1.1 s
1001	512M	2.15 s
1010	1G	4.3 s
1011	2G	8.6 s
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency, f_S = 250 MSPS.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 1. When frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by a default after reset.

After a reset, the offset correction is disabled. To use offset correction set EN OFFSET CORR to 1 and program the required time constant. Figure 58 shows the time response of the offset correction algorithm after it is enabled.

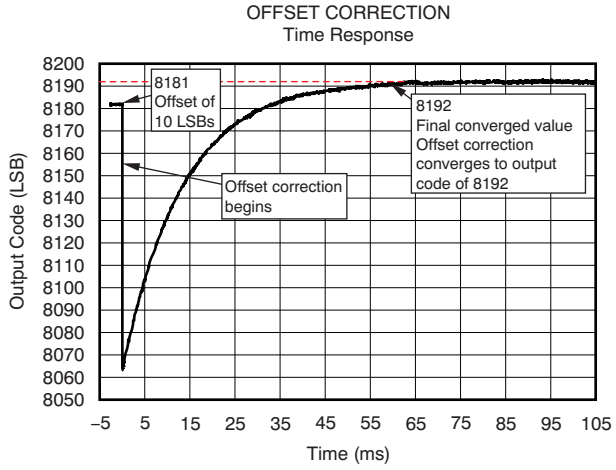


Figure 58. Time Response of Offset Correction

8.3.5 Digital Output Information

The ADS41Bx9 provides either 14-bit data or 12-bit data, respectively, and an output clock synchronized with the data.

8.3.5.1 Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the LVDS CMOS serial interface register bit or using the DFS pin.

8.3.5.2 DDR LVDS Outputs

In this mode, the data bits and clock are output using low voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as illustrated in Figure 59 and Figure 60.

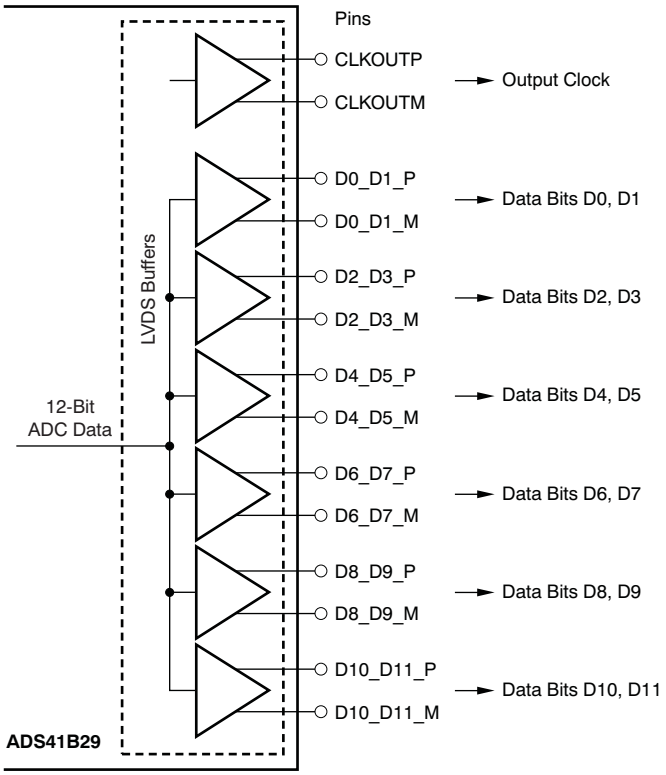


Figure 59. ADS41B29 LVDS Data Outputs

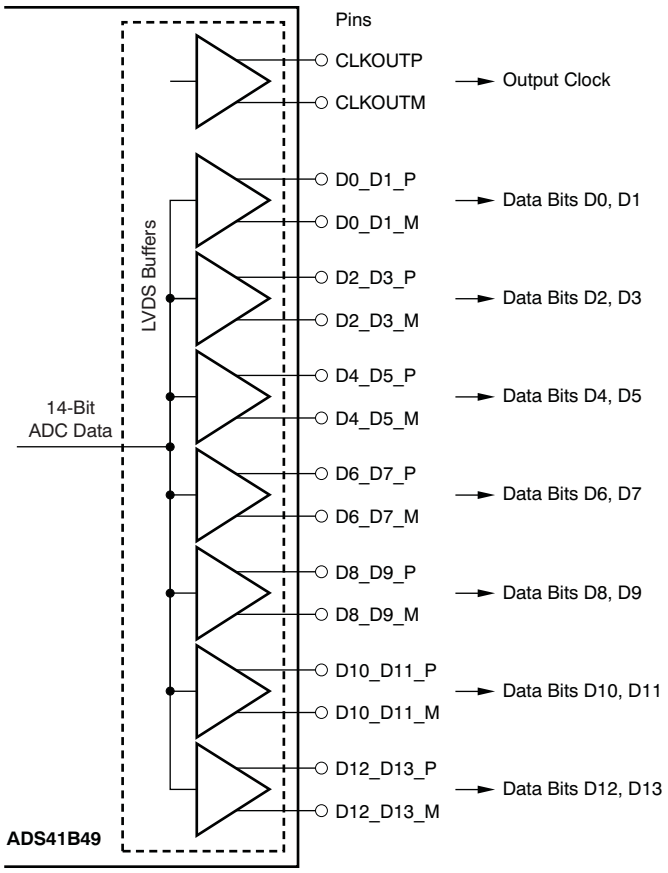


Figure 60. ADS41B49 LVDS Data Outputs

Even data bits (D0, D2, D4, and so forth) are output at the falling edge of CLKOUTP and the odd data bits (D1, D3, D5, and so forth) are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all 14 data bits, as shown in Figure 61.

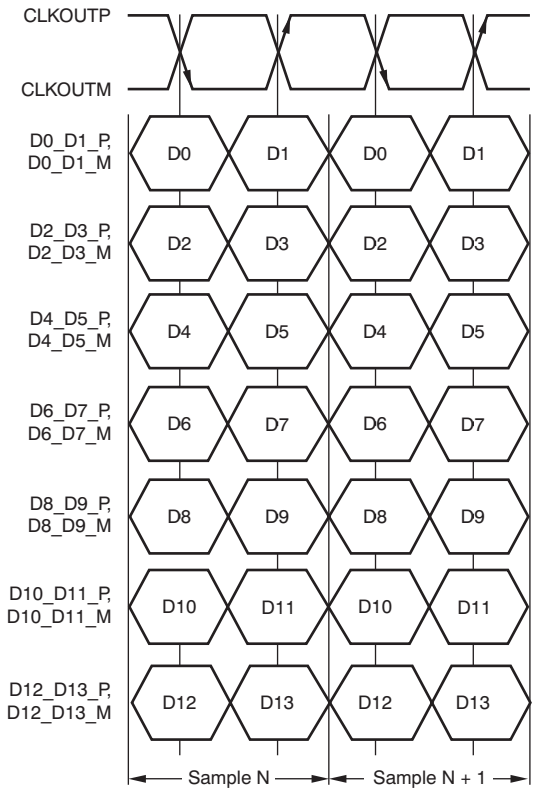


Figure 61. DDR LVDS Interface

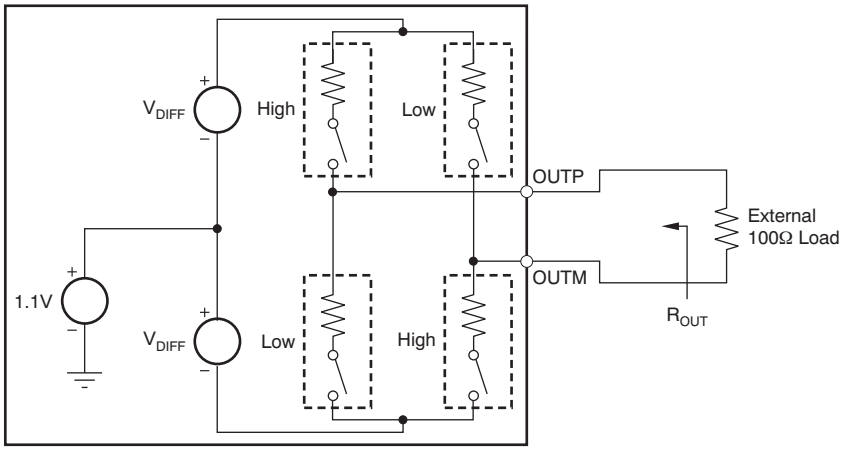
8.3.5.3 LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in Figure 62. After reset, the buffer presents an output impedance of 100Ω to match with the external 100-Ω termination.

The V_{DIFF} voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100-Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±125 mV to ±570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50-Ω differential termination. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100-Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, signal integrity is improved.



NOTE: Use the default buffer strength to match 100-Ω external termination (R_{OUT} = 100 Ω). To match with a 50-Ω external termination, set the LVDS STRENGTH bit (R_{OUT} = 50 Ω).

Figure 62. LVDS Buffer Equivalent Circuit

8.3.5.4 Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as the CMOS voltage level, for every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. Figure 63 depicts the CMOS output interface.

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs and degrade SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this degradation, the CMOS output buffers are designed with controlled drive strength. The default drive strength ensures a wide data stable window (even at 250 MSPS) is provided so the data outputs have minimal load capacitance. Using short traces (one to two inches or 2.54 cm to 5.08 cm) terminated with less than 5-pF load capacitance is recommended; see Figure 64.

For sampling frequencies greater than 200 MSPS, using an external clock to capture data is recommended. The delay from input clock to output data and the data valid times are specified for higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture data.

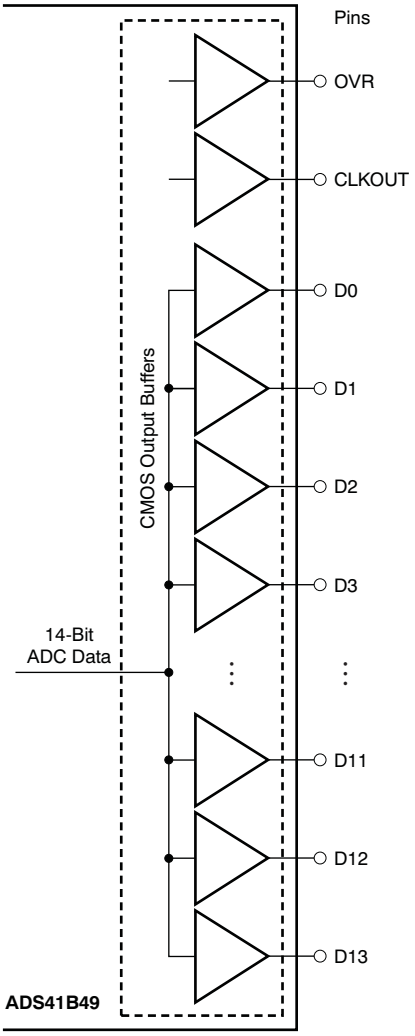


Figure 63. CMOS Output Interface

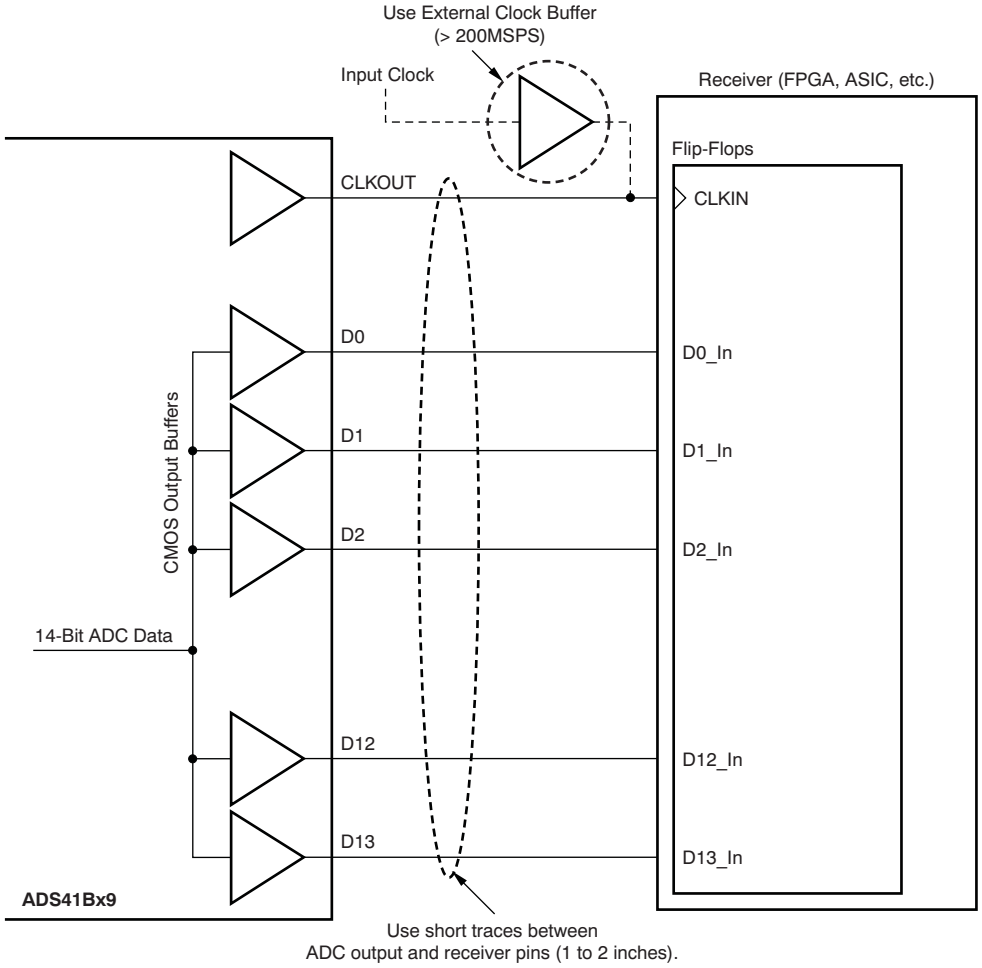


Figure 64. Using the CMOS Data Outputs

8.3.5.5 CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital Current as a Result of CMOS Output Switching = $C_L \times DRVDD \times (N \times f_{AVG})$

where:

C_L = load capacitance,

$N \times F_{AVG}$ = average number of output bits switching. (1)

Figure 41 illustrates the current across sampling frequencies at 2-MHz analog input frequency.

8.3.5.6 Input Overvoltage Indication (OVR Pin)

The device has an OVR pin that provides information about analog input overload. At any clock cycle, if the sampled input voltage exceeds the positive or negative full-scale range, the OVR pin goes high. The OVR remains high as long as the overload condition persists. The OVR pin is a CMOS output buffer (running off DRVDD supply), independent of the type of output data interface (DDR LVDS or CMOS).

For a positive overload, the D[13:0] output data bits are 0x3FFF in offset binary output format and 0x1FFF in twos complement output format. For a negative input overload, the output code is 0x0000 in offset binary output format and 0x2000 in twos complement output format.

8.3.5.7 Output Data Format

Two output data formats are supported: twos complement and offset binary. They can be selected using the DATA FORMAT serial interface register bit or controlling the DFS pin in parallel configuration mode. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level.

8.4 Device Functional Modes

8.4.1 Device Configuration

The ADS41Bx9 have several modes that can be configured using a serial programming interface, as described in Table 3, Table 4, and Table 5. In addition, the devices have two dedicated parallel pins for quickly configuring commonly used functions. The parallel pins are DFS (analog 4-level control pin) and OE (digital control pin). The analog control pins can be easily configured using a simple resistor divider (with 10% tolerance resistors).

Table 3. DFS: Analog Control Pin

VOLTAGE APPLIED ON DFS	DESCRIPTION (Data Format, Output Interface)
0, 100 mV / 0 mV	Twos complement, DDR LVDS
(3/8) AVDD ± 100 mV	Twos complement, parallel CMOS
(5/8) AVDD ± 100 mV	Offset binary, parallel CMOS
AVDD, 0 mV / –100 mV	Offset binary, DDR LVDS

Table 4. OE: Digital Control Pin

VOLTAGE APPLIED ON OE	DESCRIPTION
0	Output data buffers disabled
AVDD	Output data buffers enabled

When the serial interface is not used, the SDATA pin can also be used as a digital control pin to place the device in standby mode. To enable this, the RESET pin must be tied high. In this mode, SEN and SCLK do not have any alternative functions. Keep SEN tied high and SCLK tied low on the board.

Table 5. SDATA: Digital Control Pin

VOLTAGE APPLIED ON SDATA	DESCRIPTION
0	Normal operation
Logic high	Device enters standby

A simple diagram to configure DFS pin is shown in Figure 65.

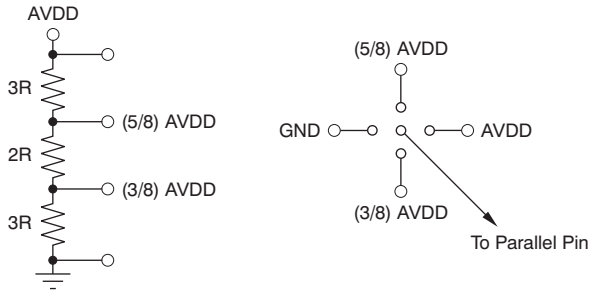


Figure 65. Simplified Diagram to Configure the DFS Pin

8.4.2 Power-Down

The ADS41Bx9 has three power-down modes: power-down global, standby, and output buffer disable.

8.4.2.1 Power-Down Global

In this mode, the entire chip (including the ADC, internal reference, and the output buffers) is powered down, resulting in reduced total power dissipation of approximately 7 mW. The output buffers are in a high-impedance state. The wake-up time from the global power-down to data becoming valid in normal mode is typically 100 µs. To enter the global power-down mode, set the PDN GLOBAL register bit.

8.4.2.2 Standby

In this mode, only the ADC is powered down and the internal references are active, resulting in a fast wake-up time of 5 µs. The total power dissipation in standby mode is approximately 200mW. To enter the standby mode, set the STBY register bit.

8.4.2.3 Output Buffer Disable

The output buffers can be disabled and put in a high-impedance state; wake-up time from this mode is fast, approximately 100 ns. This can be controlled using the PDN OBUF register bit or using the OE pin.

8.4.2.4 Input Clock Stop

In addition, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is approximately 92 mW.

8.5 Programming

8.5.1 Serial Interface

The analog-to-digital converter (ADC) has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serially shifting bits into the device is enabled when SEN is low. SDATA serial SDATA are latched at every falling edge of SCLK when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequency from 20 MHz down to very low speeds (a few hertz) and also with non-50% SCLK duty cycle.

8.5.1.1 Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on RESET pin (of width greater than 10 ns), as shown in Figure 66; or
2. By applying a software reset. When using the serial interface, set the RESET bit (D7 in register 0x00) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

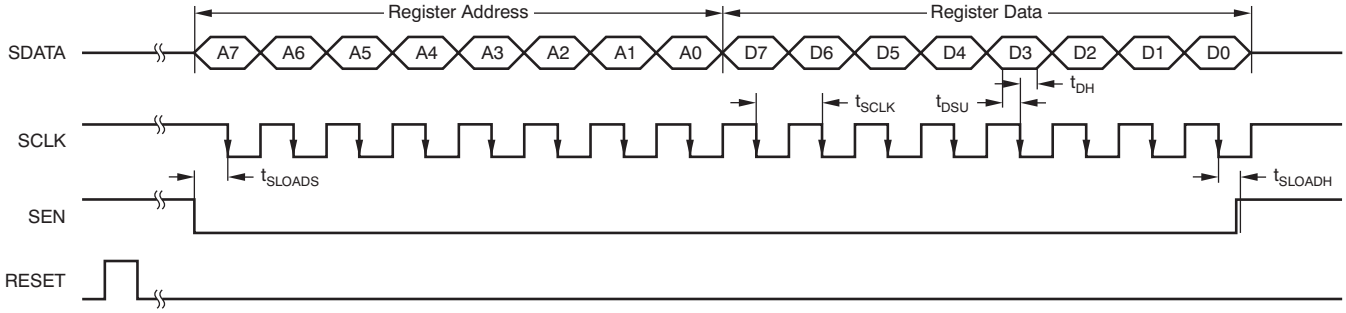


Figure 66. Serial Interface Timing

Table 6. Serial Interface Timing Characteristics(1)(2)

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

(1) Typical values are at 25°C, minimum and maximum values for the ADS41B29 are specified across the ambient temperature range of $T_{A, MIN}$ = –40°C to $T_{A, MAX}$ = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.
(2) Typical values are at 25°C, minimum and maximum values for the ADS41B49 are specified across the ambient temperature range of $T_{A, MIN}$ = –40°C to $T_{A, MAX}$ = 105°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

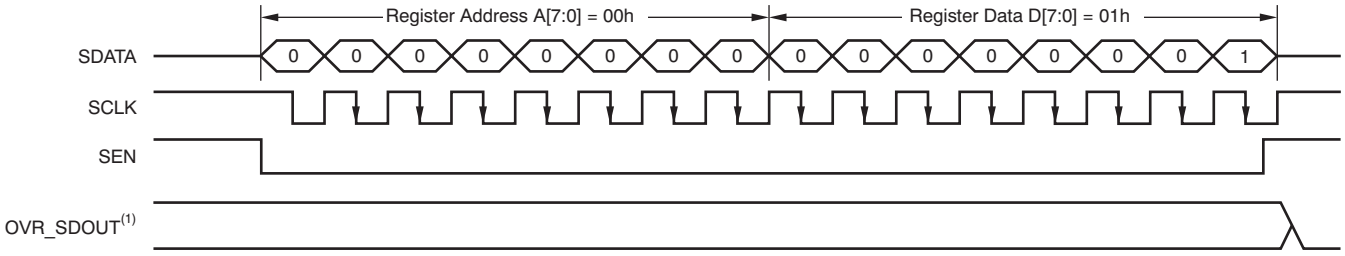
8.5.2 Serial Register Readout

The serial register readout function allows the contents of the internal registers to be read back on the OVR_SDOUT pin. This readback may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

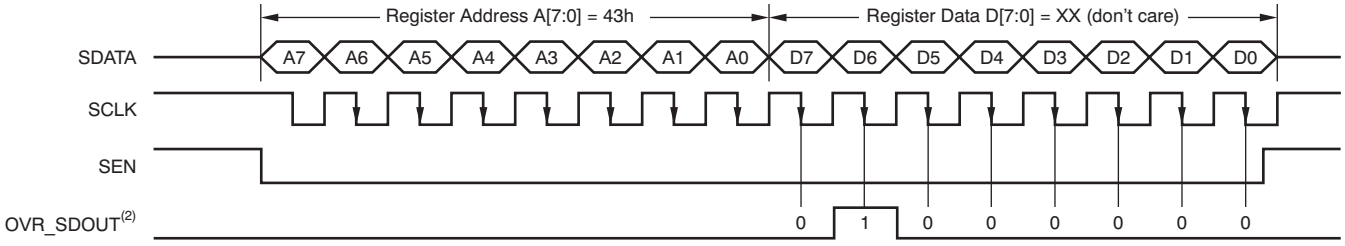
After power-up and device reset, the OVR_SDOUT pin functions as an over-range indicator pin by default. When the readout mode is enabled, OVR_SDOUT outputs the contents of the selected register serially:

1. Set the READOUT register bit to 1. This setting puts the device in serial readout mode and disables any further writes to the internal registers **except** the register at address 0. Note that the READOUT bit itself is also located in register 0. The device can exit readout mode by writing READOUT = 0. Only the contents of the register at address 0 cannot be read in the register readout mode.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device serially outputs the contents (D7 to D0) of the selected register on the OVR_SDOUT pin.
4. The external controller can latch the contents at the falling edge of SCLK.
5. To exit the serial readout mode, the reset register bit READOUT = 0 enables writes into all registers of the device. At this point, the OVR_SDOUT pin becomes an over-range indicator pin.

Figure 67 shows the process of reading out register contents on the OVR_SDOUT pin, using register 43h as example.



a) Enable Serial Readout (READOUT = 1)



b) Read Contents of Register 43h. This Register Has Been Initialized with 40h (device is put in global power-down mode).

(1) The OVR_SDOUT pin functions as OVR (READOUT = 0).

(2) The OVR_SDOUT pin functions as a serial readout (READOUT = 1).

Figure 67. Serial Readout Timing Diagram

8.6 Register Maps

8.6.1 Serial Register Map

Table 7 summarizes the functions supported by the serial interface.

Table 7. Serial Interface Register Map(1)

REGISTER ADDRESS	DEFAULT VALUE AFTER RESET	REGISTER DATA							
A[7:0] (Hex)	D[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	00	0	0	0	0	0	0	RESET	READOUT
01	00	LVDS SWING						0	0
03	00	0	0	0	0	0	0	HIGH PERF MODE 1	
25	50	GAIN				0	TEST PATTERNS		
26	00	0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH
3D	00	DATA FORMAT		EN OFFSET CORR	0	0	0	0	0
3F	00	0	0	CUSTOM PATTERN D[13:8]					
40	00	CUSTOM PATTERN D[7:0]							
41	00	LVDS CMOS		CMOS CLKOUT STRENGTH		EN CLKOUT RISE	CLKOUT RISE POSN		EN CLKOUT FALL
42	08	CLKOUT FALL POSN		0	0	1	STBY	0	0
43	00	0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	
4A	00	0	0	0	0	0	0	0	HIGH PERF MODE 2
BF	00	OFFSET PEDESTAL						0	0
CF	00	FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0
DF	00	0	0	LOW SPEED		0	0	0	0

(1) Multiple functions in a register can be programmed in a single write operation.

8.6.1.1 Summary of High-Performance Modes

Table 8 lists the location and functions of high-performance mode registers in the device.

Table 8. High-Performance Modes Summary(1)(2)(3)

MODE	LOCATION	FUNCTION
MODE 1	Register address = 03h, register data = 03h	Set the MODE 1 register bits to get the best performance across sample clock and input signal frequencies.
MODE 2	Register address = 4Ah, register data = 01h	Set the MODE 2 register bit to get the best performance at high input signal frequencies greater than 230 MHz.

(1) Using these modes is recommended to get best performance. These modes can only be set with the serial interface.
(2) See the *Serial Interface* section for details on register programming.
(3) Note that these modes cannot be set when the serial interface is not used (when the RESET pin is tied high); see the *Device Configuration* section.

8.6.1.2 Description of Serial Registers

For best performance, two special mode register bits must be enabled:

HI PERF MODE 1 and HI PERF MODE 2.

8.6.1.2.1 Register Address 00h (address = 00h) [reset = 00h]

Figure 68. Register Address 00h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

Bits 7-2 **Always write 0**

Bit 1 **RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit 0 **READOUT: Serial readout**

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the OVR_SDOUT pin functions as an over-voltage indicator.
1 = Serial readout enabled; the OVR_SDOUT pin functions as a serial data readout.

8.6.1.2.2 Register Address 01h (address = 01h) [reset = 00h]

Figure 69. Register Address 01h

7	6	5	4	3	2	1	0
LVDS SWING						0	0

Bits 7-2 **LVDS SWING: LVDS swing programmability(1)**

000000 = Default LVDS swing; ±350 mV with external 100-Ω termination
011011 = LVDS swing *increases* to ±410 mV
110010 = LVDS swing *increases* to ±465 mV
010100 = LVDS swing *increases* to ±570 mV
111110 = LVDS swing *decreases* to ±200 mV
001111 = LVDS swing *decreases* to ±125 mV

Bits 1-0 **Always write 0**

(1) The EN LVDS SWING register bits must be set to enable LVDS swing control.

8.6.1.2.3 Register Address 03h (address = 03h) [reset = 00h]

Figure 70. Register Address 03h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HI PERF MODE 1	

Bits 7-2 **Always write 0**

Bits 1-0 **HI PERF MODE 1: High performance mode 1**

00 = Default performance after reset
01 = Do not use
10 = Do not use
11 = For best performance across sampling clock and input signal frequencies, set the HIGH PERF MODE 1 bits

8.6.1.2.4 Register Address 25h (address = 25h) [reset = 50h]

Figure 71. Register Address 25h

7	6	5	4	3	2	1	0
GAIN				0	TEST PATTERNS		

Bits 7-4 GAIN: Gain programmability

These bits set the gain programmability in 0.5-dB steps.

0000, 0001, 0010, 0011, 0100 = Do not use
0101 = 0-dB gain (default after reset)
0110 = 0.5-dB gain
0111 = 1-dB gain
1000 = 1.5-dB gain
1001 = 2-dB gain
1010 = 2.5-dB gain
1011 = 3-dB gain
1100 = 3.5-dB gain

Bit 3 Always write 0

Bits 2-0 TEST PATTERNS: Data capture

These bits verify data capture.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern

In the ADS41B49, output data D[13:0] is an alternating sequence of *01010101010101* and *10101010101010*.
In the ADS41B29, output data D[11:0] is an alternating sequence of *010101010101* and *101010101010*.

100 = Outputs digital ramp

In ADS41B46, output data increments by one LSB (14-bit) every clock cycle from code 0 to code 16383
In ADS41B26, output data increments by one LSB (12-bit) every 4th clock cycle from code 0 to code 4095

101 = Output custom pattern (use registers 0x3F and 0x40 for setting the custom pattern)
110 = Unused
111 = Unused

8.6.1.2.5 Register Address 26h (address = 26h) [reset = 00h]

Figure 72. Register Address 26h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH

Bits 7-2 Always write 0

Bit 1 LVDS CLKOUT STRENGTH: LVDS output clock buffer strength

This bit determines the external termination to be used with the LVDS output clock buffer.
0 = 100-Ω external termination (default strength)
1 = 50-Ω external termination (2x strength)

Bit 0 LVDS DATA STRENGTH: LVDS data buffer strength

This bit determines the external termination to be used with all of the LVDS data buffers.
0 = 100-Ω external termination (default strength)
1 = 50-Ω external termination (2x strength)

8.6.1.2.6 Register Address 3Dh (address = 3Dh) [reset = 00h]

Figure 73. Register Address 3Dh

7	6	5	4	3	2	1	0
DATA FORMAT		EN OFFSET CORR	0	0	0	0	0

Bits 7-6 DATA FORMAT: Data format selection

These bits selects the data format.
00 = The DFS pin controls data format selection
10 = Twos complement
11 = Offset binary

Bit 5 ENABLE OFFSET CORR: Offset correction setting

This bit sets the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

Bits 4-0 Always write 0

8.6.1.2.7 Register Address 3Fh (address = 3Fh) [reset = 00h]

Figure 74. Register Address 3Fh

7	6	5	4	3	2	1	0
0	0	CUSTOM PATTERN D13	CUSTOM PATTERN D12	CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8

Bits 7-6 Always write 0

Bits 5-0 CUSTOM PATTERN(1)

These bits set the custom pattern.

(1) For the ADS41B4x, output data bits 13 to 0 are CUSTOM PATTERN D[13:0]. For the ADS41B2x, output data bits 11 to 0 are CUSTOM PATTERN D[13:2].

8.6.1.2.8 Register Address 40h (address = 40h) [reset = 00h]

Figure 75. Register Address 40h

7	6	5	4	3	2	1	0
CUSTOM PATTERN D7	CUSTOM PATTERN D6	CUSTOM PATTERN D5	CUSTOM PATTERN D4	CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0

Bits 7-0 CUSTOM PATTERN(1)

These bits set the custom pattern.

(1) For the ADS41B4x, output data bits 13 to 0 are CUSTOM PATTERN D[13:0]. For the ADS41B2x, output data bits 11 to 0 are CUSTOM PATTERN D[13:2].

8.6.1.2.9 Register Address 41h (address = 41h) [reset = 00h]

Figure 76. Register Address 41h

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STRENGTH		EN CLKOUT RISE	CLKOUT RISE POSN		EN CLKOUT FALL

Bits 7-6 LVDS CMOS: Interface selection

These bits select the interface.
00, 10 = The DFS pin controls the selection of either LVDS or CMOS interface
01 = DDR LVDS interface
11 = Parallel CMOS interface

Bits 5-4 CMOS CLKOUT STRENGTH

Controls strength of CMOS output clock only.
00 = Maximum strength (recommended and used for specified timings)
01 = Medium strength
10 = Low strength
11 = Very low strength

Bit 3 ENABLE CLKOUT RISE

0 = Disables control of output clock rising edge
1 = Enables control of output clock rising edge

Bits 2-1 CLKOUT RISE POSN: CLKOUT rise control

Controls position of output clock rising edge

LVDS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 500 ps, hold increases by 500 ps
10 = Data transition is aligned with rising edge
11 = Setup reduces by 200 ps, hold increases by 200 ps

CMOS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 100 ps, hold increases by 100 ps
10 = Setup reduces by 200 ps, hold increases by 200 ps
11 = Setup reduces by 1.5 ns, hold increases by 1.5 ns

Bit 0 ENABLE CLKOUT FALL

0 = Disables control of output clock fall edge
1 = Enables control of output clock fall edge

8.6.1.2.10 Register Address 42h (address = 42h) [reset = 08h]

Figure 77. Register Address 42h

7	6	5	4	3	2	1	0
CLKOUT FALL POSN		0	0	1	STBY	0	0

Bits 7-6 CLKOUT FALL POSN

Controls position of output clock falling edge

LVDS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 400 ps, hold increases by 400 ps
10 = Data transition is aligned with rising edge
11 = Setup reduces by 200 ps, hold increases by 200 ps

CMOS interface:
00 = Default position (timings are specified in this condition)
01 = Falling edge is advanced by 100 ps
10 = Falling edge is advanced by 200 ps
11 = Falling edge is advanced by 1.5 ns

Bits 5-4 Always write 0

Bit 3 Always write 1

Bit 2 STBY: Standby mode

This bit sets the standby mode.
0 = Normal operation
1 = Only the ADC and output buffers are powered down; internal reference is active; wake-up time from standby is fast

Bits 1-0 Always write 0

8.6.1.2.11 Register Address 43h (address = 43h) [reset = 00h]

Figure 78. Register Address 43h

7	6	5	4	3	2	1	0
0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	

Bit 7 Always write 0

Bit 6 PDN GLOBAL: Power-down

This bit sets the state of operation.
0 = Normal operation
1 = Total power down; the ADC, internal references, and output buffers are powered down; slow wake-up time.

Bit 5 Always write 0

Bit 4 PDN OBUF: Power-down output buffer

This bit set the output data and clock pins.
0 = Output data and clock pins enabled
1 = Output data and clock pins powered down and put in high- impedance state

Bits 3-2 Always write 0

Bits 1-0 EN LVDS SWING: LVDS swing control

00 = LVDS swing control using LVDS SWING register bits is disabled
01, 10 = Do not use
11 = LVDS swing control using LVDS SWING register bits is enabled

8.6.1.2.12 Register Address 4Ah (address = 4Ah) [reset = 00h]

Figure 79. Register Address 4Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HI PERF MODE 2

Bits 7-1 **Always write 0**

Bit 0 **HI PERF MODE 2: High performance mode 2**

This bit is recommended for high input signal frequencies greater than 230 MHz.
0 = Default performance after reset
1 = For best performance with high-frequency input signals, set the HIGH PERF MODE 2 bit

8.6.1.2.13 Register Address BFh (address = BFh) [reset = 00h]

Figure 80. Register Address BFh

7	6	5	4	3	2	1	0
OFFSET PEDESTAL						0	0

Bits 7-2 **OFFSET PEDESTAL**

These bits set the offset pedestal. For the ADS41B49, bits 7-2 set the pedestal; for the ADS41B29, bits 7-4 set the pedestal.
When the offset correction is enabled, the final converged value after the offset is corrected is the ADC mid-code value. A pedestal can be added to the final converged value by programming these bits.

ADS41Bx9 VALUE	PEDESTAL
011111	31 LSB
011110	30 LSB
011101	29 LSB
—	—
000000	0 LSB
—	—
111111	–1 LSB
111110	–2 LSB
—	—
100000	–32 LSB

Bits 1-0 **Always write 0**

8.6.1.2.14 Register Address CFh (address = CFh) [reset = 00h]

Figure 81. Register Address CFh

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0

Bit 7 FREEZE OFFSET CORR

This bit sets the freeze offset correction.
0 = Estimation of offset correction is not frozen (bit EN OFFSET CORR must be set)
1 = Estimation of offset correction is frozen (bit EN OFFSET CORR must be set). When frozen, the last estimated value is used for offset correction every clock cycle; see the *Offset Correction* section.

Bit 6 Always write 0

Bits 5-2 OFFSET CORR TIME CONSTANT

These bits set the offset correction time constant for the correction loop time constant in number of clock cycles.

VALUE	TIME CONSTANT (Number of Clock Cycles)
0000	1M
0001	2M
0010	4M
0011	8M
0100	16M
0101	32M
0110	64M
0111	128M
1000	256M
1001	512M
1010	1G
1011	2G

Bits 1-0 Always write 0

8.6.1.2.15 Register Address DFh (address = DFh) [reset = 00h]

Figure 82. Register Address DFh

7	6	5	4	3	2	1	0
0	0	LOW SPEED		0	0	0	0

Bits 7-6 Always write 0

Bits 5-4 LOW SPEED: Low-speed mode

00, 01, 10 = Low-speed mode disabled (default state after reset); this setting is recommended for sampling rates greater than 80 MSPS.
11 = Low-speed mode enabled; this setting is recommended for sampling rates less than or equal to 80 MSPS.

Bits 3-0 Always write 0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 83 and Figure 84 show the differential impedance (Z_{IN} = R_{IN} || C_{IN}) between the ADC analog input pins INP and INM. The presence of the analog input buffer results in an almost constant input capacitance up to 1 GHz.

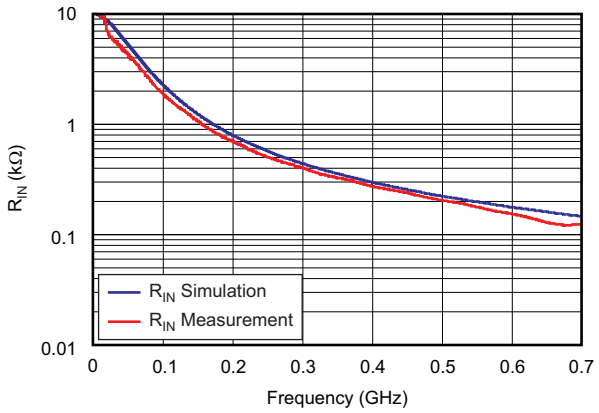


Figure 83. ADC Analog Input Resistance (R_{IN}) Across Frequency

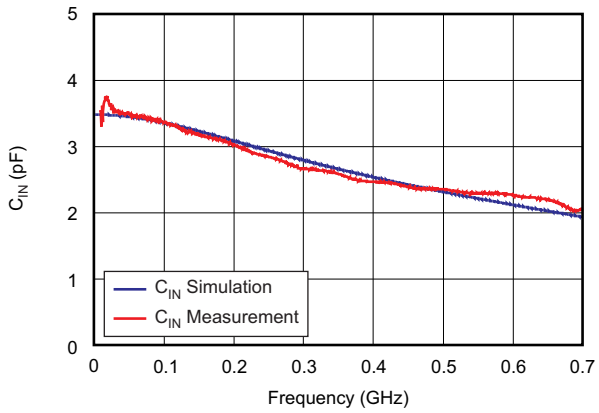


Figure 84. ADC Analog Input Capacitance (C_{IN}) Across Frequency

Application Information (continued)

9.1.2 Driving Circuit

Two example driving circuit configurations are shown in Figure 85 and Figure 86—one optimized for low input frequencies and the other optimized for high input frequencies. Notice in both cases that the board circuitry is simplified compared to the non-buffered ADS4149.

In Figure 85, a single transformer is used and is suited for low input frequencies. To optimize even-harmonic performance at high input frequencies (greater than the first Nyquist), the use of back-to-back transformers is recommended (see Figure 86). Note that both drive circuits have been terminated by 50 Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage.

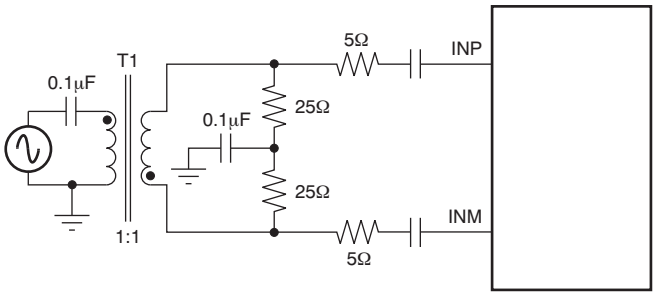


Figure 85. Drive Circuit for Low Input Frequencies

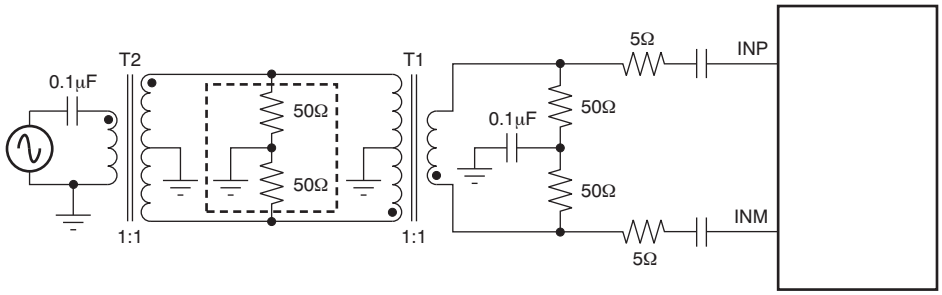


Figure 86. Drive Circuit for High Input Frequencies

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 85 and Figure 86. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50-Ω source impedance).

10 Power Supply Recommendations

10.1 Power-Supply Sequence

During power-up, the AVDD, AVDD_BUF, and DRVDD supplies can come up in any sequence. These supplies are separated in the device. Externally, AVDD and DRVDD can be driven from separate supplies or from a single supply.

11 Layout

11.1 Layout Guidelines

11.1.1 Board Design Considerations

11.1.1.1 Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS414x, ADS412x EVM User Guide*, SLWU067 for details on layout and grounding.

11.1.1.2 Supply Decoupling

Because the ADS41Bx9 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise, so the optimum number of capacitors depends on the actual application. Place the decoupling capacitors very close to the converter supply pins.

11.1.1.3 Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically internally connected to the digital ground. Therefore, the exposed pad must be soldered to the ground plane for best thermal and electrical performance. For detailed information, see application notes *VQFN Layout Guidelines*, SLOA122, and *VQFN/SON PCB Attachment*, SLUA271, both available for download at the TI web site (www.ti.com).

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

ADS4149 Data Sheet, SBAS483

ADS414x, ADS412x EVM User Guide, SLWU067

Application Note *VQFN Layout Guidelines*, SLOA122

Application Note *VQFN/SON PCB Attachment*, SLUA271

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS41B29	Click here	Click here	Click here	Click here	Click here
ADS41B49	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
PowerPAD is a trademark of Texas Instruments, Incorporated.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS41B29IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ41B29
ADS41B29IRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ41B29
ADS41B29IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ41B29
ADS41B29IRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ41B29
ADS41B49IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ41B49
ADS41B49IRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ41B49
ADS41B49IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ41B49
ADS41B49IRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ41B49

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

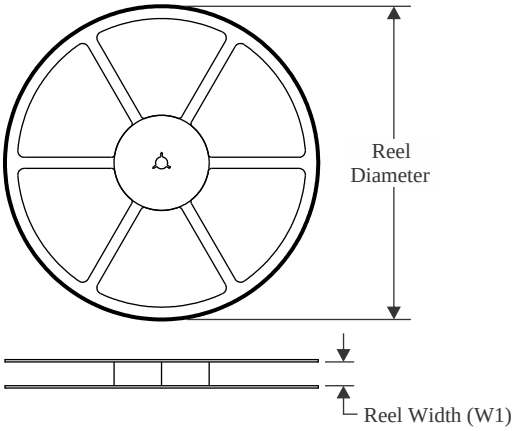
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

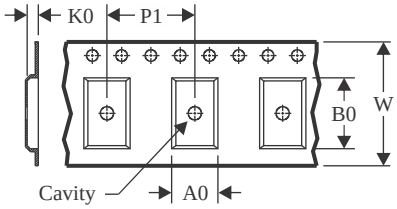
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

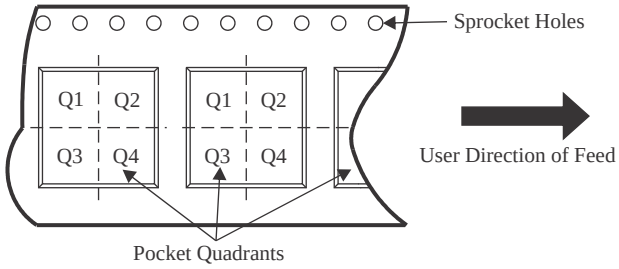


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

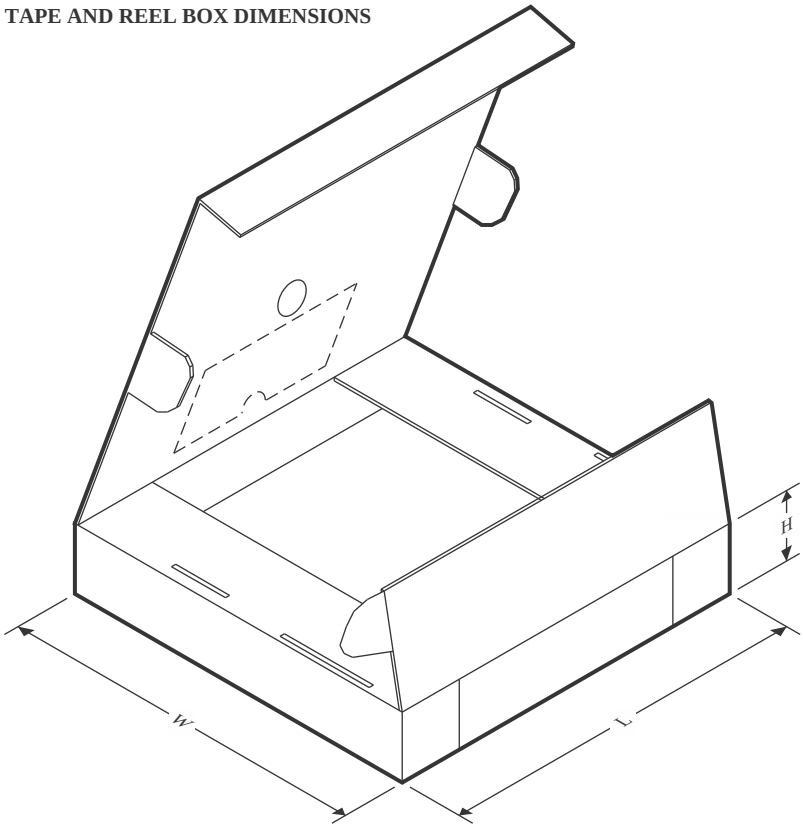
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS41B29IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS41B49IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS41B29IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADS41B49IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0

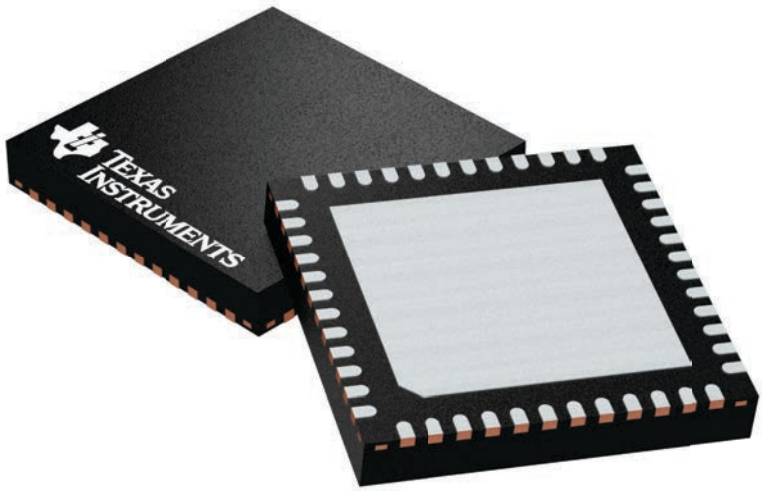
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

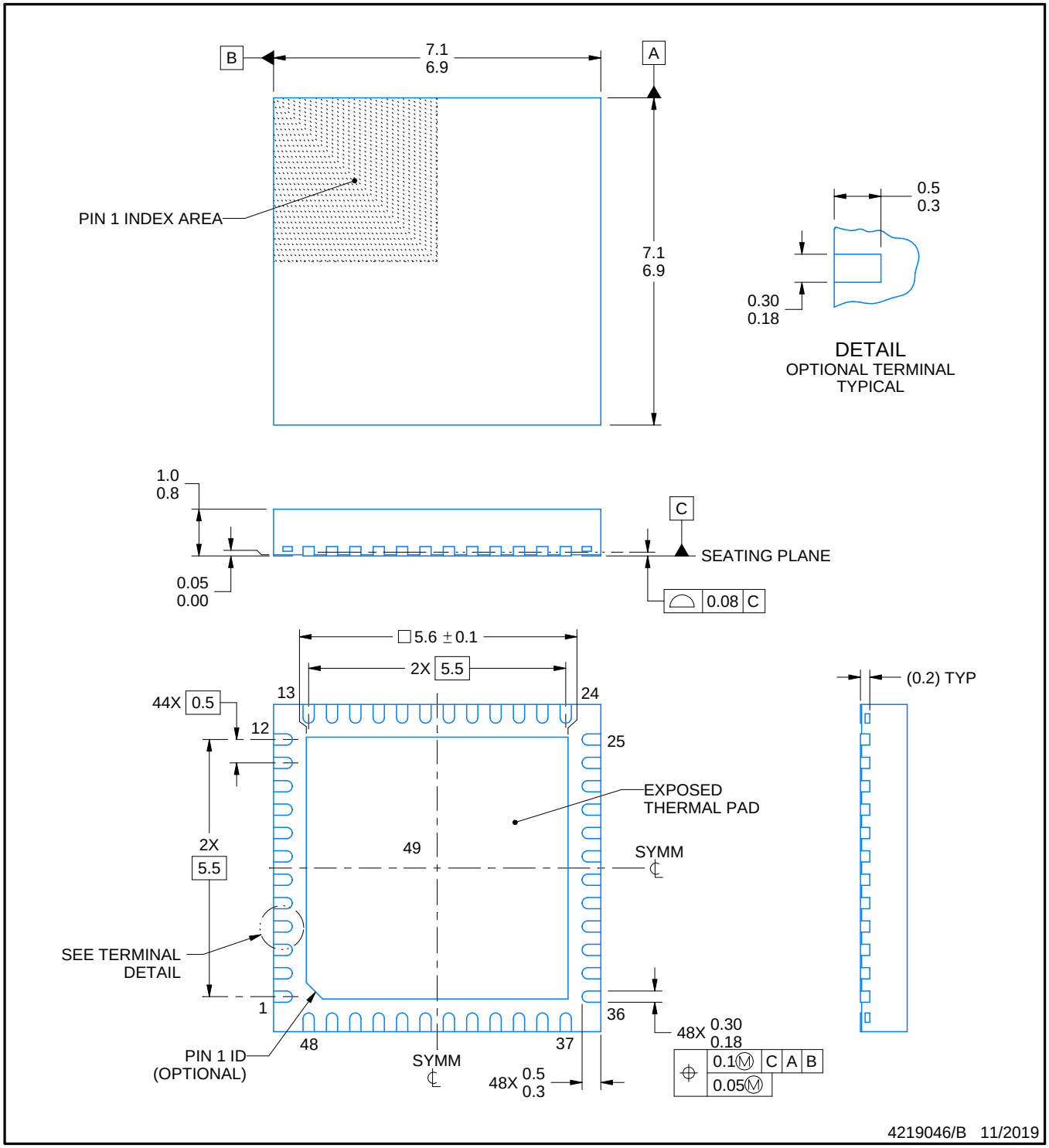
4224671/A

PACKAGE OUTLINE

RGZ0048D

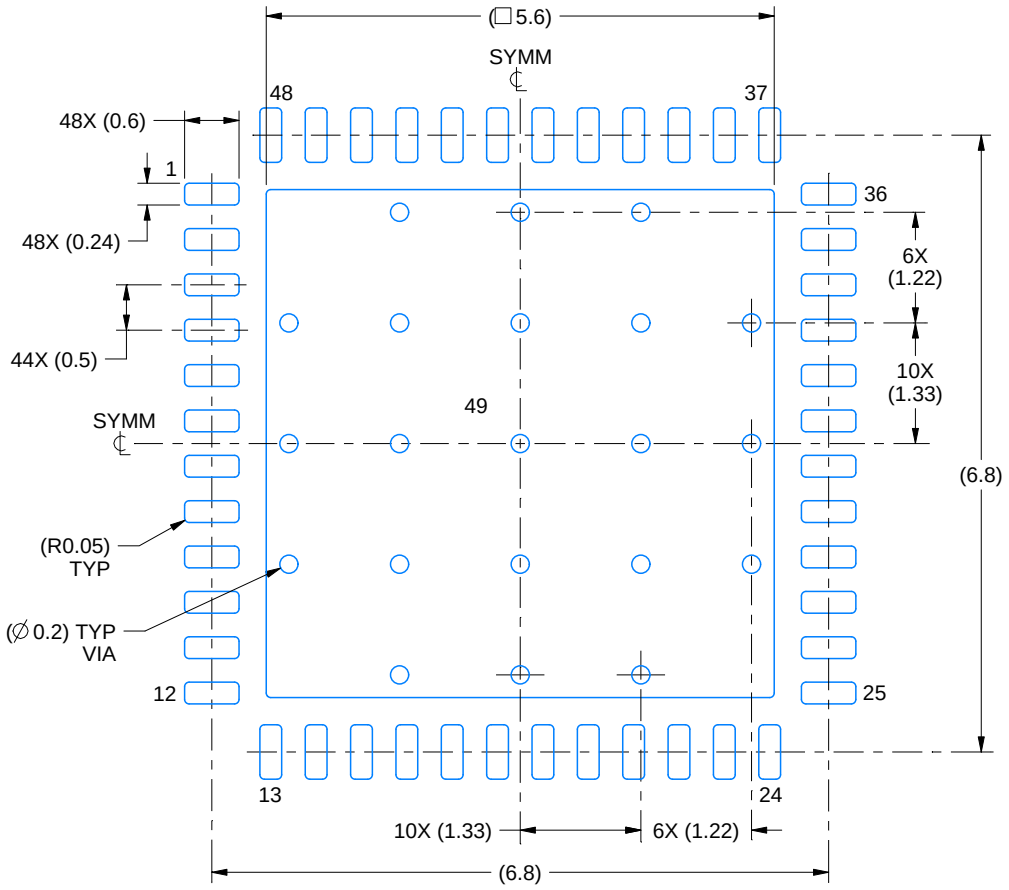
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

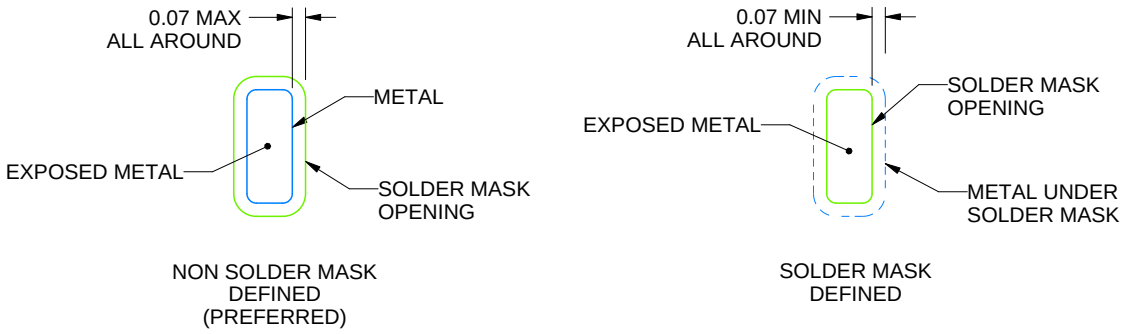


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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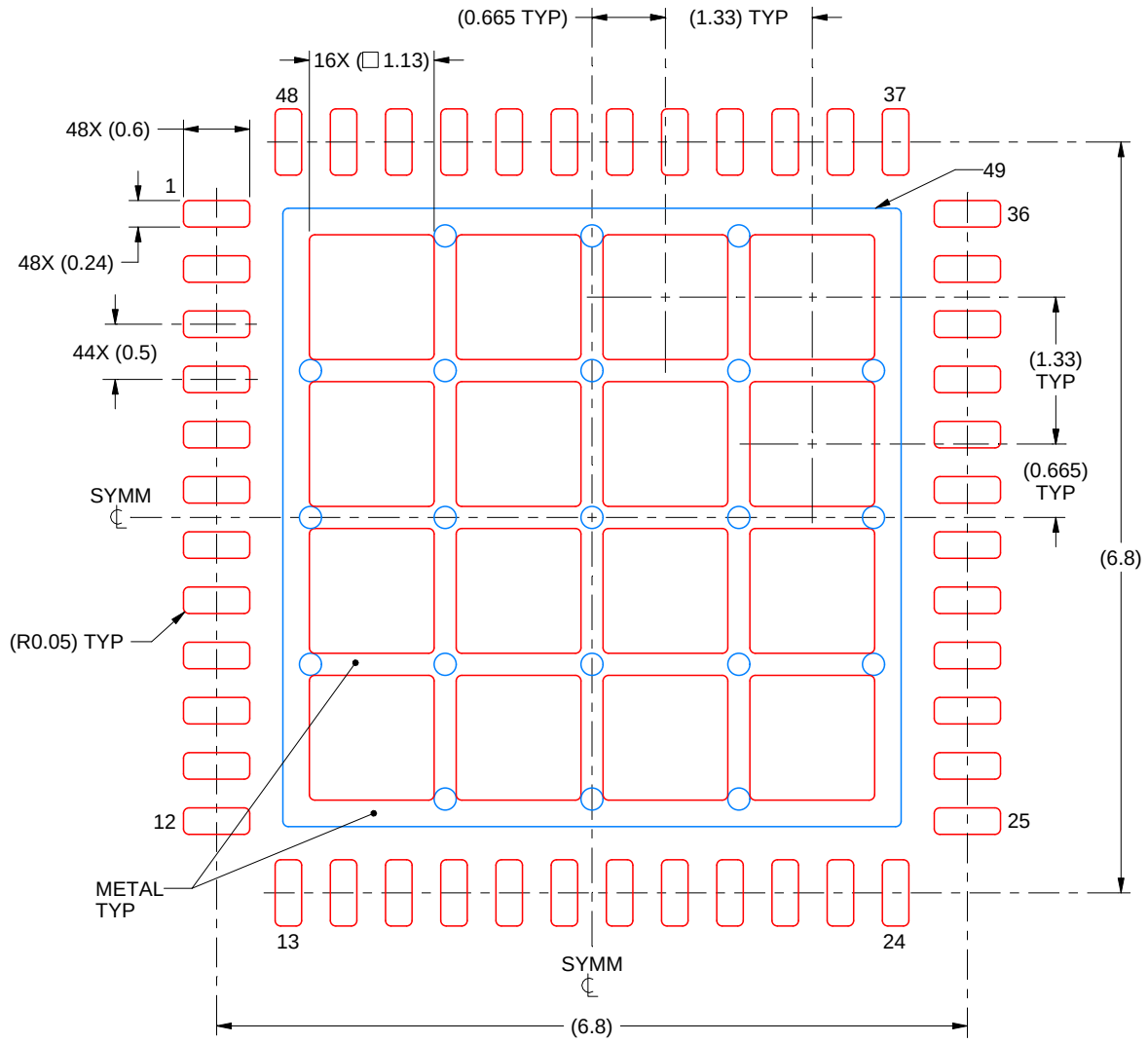
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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