ADS117L1x 512kSPS, Quad and Octal, Simultaneous-Sampling, 16-Bit ΔΣ ADCs

1 Features

- Simultaneously measure four or eight channels
- Wideband filter mode: up to 512kSPS
  - Linear phase response
  - ±0.0004dB pass-band ripple
  - 106dB stop-band attenuation
- Low-latency filter mode: up to 1365kSPS
  - 3.9µs conversion latency
- Power-scalable speed modes:
  - Max speed: 21mW/ch (512kSPS/1365kSPS)
  - High speed: 16mW/ch (400kSPS/1067kSPS)
  - Mid speed: 9mW/ch (200kSPS/533kSPS)
  - Low speed: 3mW/ch (50kSPS/133kSPS)
- High precision:
  - SNR at 200kSPS: 97.7dB (typical)
  - THD: –115dB (typical)
  - INL: 0.5LSB (typical)
  - Offset drift: 60nV/°C (typical)
  - Gain drift: 1ppm/°C of FSR (typical)
- Precharge buffered signal inputs
- Bipolar or unipolar power supply operation
- $\pm V_{REF}$ or $\pm 2V_{REF}$ input ranges
- Programmable by pin setting or SPI
- Frame-sync port for output data
- Internal or external clock operation
- Analog supply voltage: 2.85V to 5.5V

2 Applications

- Test and measurement:
  - Data acquisition (DAQ)
  - Shock and vibration instruments
  - Acoustics and dynamic strain gauges
- Factory automation and control:
  - Condition monitoring
- Aerospace and defense:
  - Sonar
- Medical:
  - Electroencephalograms (EEG)
- Grid Infrastructure:
  - Power quality analyzers

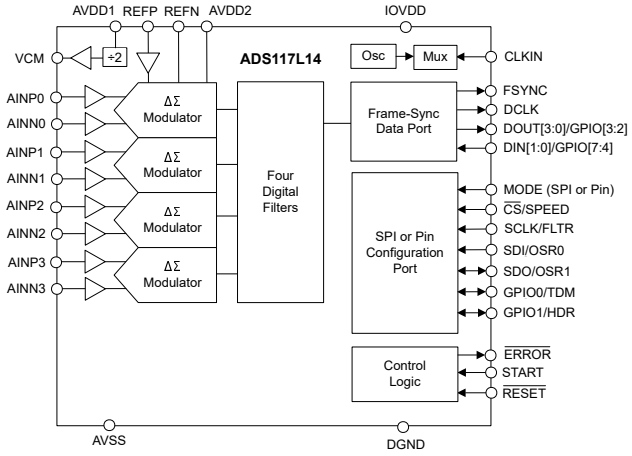
3 Description

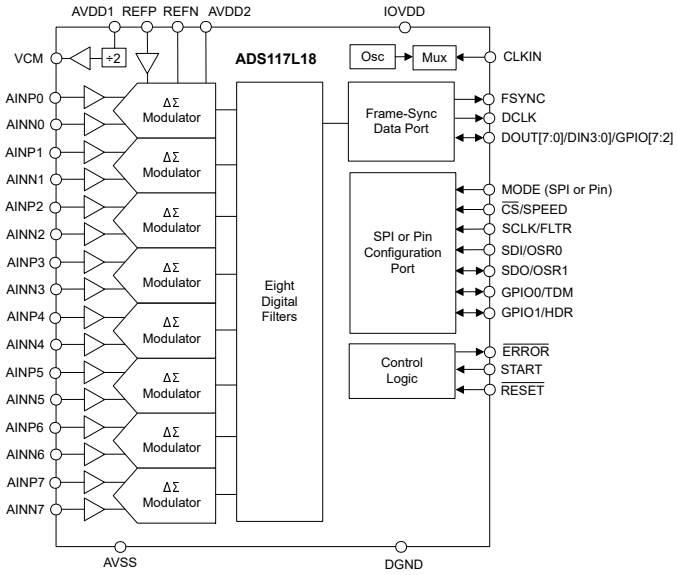
The ADS117L14 (quad) and ADS117L18 (octal) are 16-bit, delta-sigma (ΔΣ), analog-to-digital converters (ADCs). The devices provide simultaneous sampling of four or eight channels with data rates up to 512kSPS (wideband filter mode) and 1365kSPS (low-latency filter mode). The 24-bit ADS127L14 (quad) and ADS127L18 (octal) ADCs are pin-compatible devices for increased resolution.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE
ADS117L1x	RSH (VQFN, 56)	7mm × 7mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.





Functional Block Diagrams

Power-scalable speed modes allow user-optimized tradeoffs between data rate, bandwidth and power consumption. The wideband and low-latency filters optimize ac-signal performance or dc-signal data throughput, all from one device.

Programmable over-sampling ratio (OSR) determines the data rate and signal bandwidth. The linear-phase wideband filter provides a usable bandwidth of 80% of the Nyquist frequency with ±0.0004dB pass-band ripple. The low-latency filter provides data with 3.9µs conversion latency.

Precharge buffers for each input channel reduce analog input current and sampling noise to improve accuracy. Reference input buffers reduce reference loading for improved accuracy.

The low-drift modulator achieves excellent dc precision with low noise for outstanding 16-bit performance. Low crosstalk error reduces signal coupling between channels for improved data isolation.

The devices are programmed by simple pin connections or by the SPI port. The frame-sync data port with selectable number of data lanes provides the conversion data in parallel or time division multiplexed formats. Daisy chain operation expands the system channel count of multiple devices to reduce the number of data lanes.

The devices are offered in identical 7mm × 7mm VQFN packages, permitting drop-in expandability, and are fully specified for operation over the –40°C to +125°C temperature range.

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4 Pin Configuration and Functions

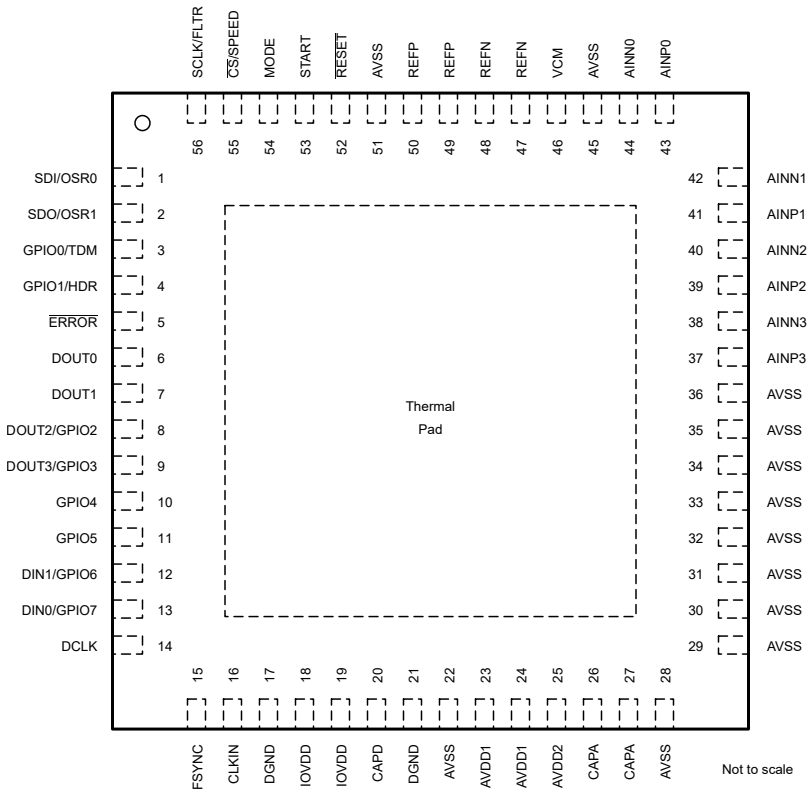


Figure 4-1. ADS117L14 RSH Package, 56-Pin VQFN (Top View)

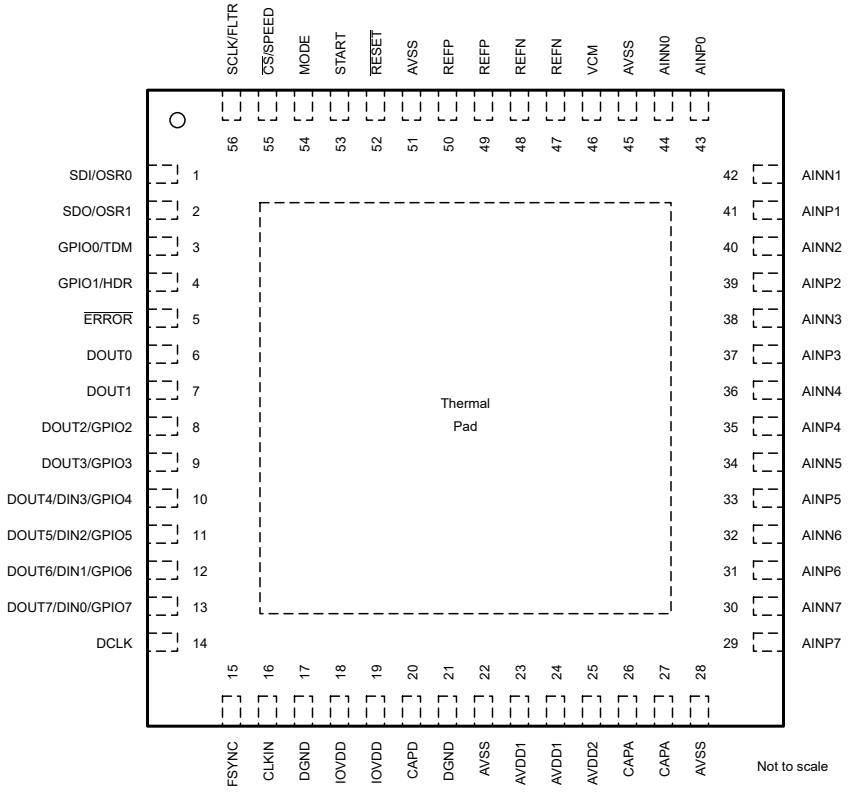


Figure 4-2. ADS117L18 RSH Package, 56-Pin VQFN (Top View)

Table 4-1. Pin Functions

NAME	ADS117L14 PIN	ADS117L18 PIN	TYPE[1]	DESCRIPTION
AINN0	44	44	I	Channel 0 negative analog input. See the *Analog Inputs* section for details.
AINN1	42	42	I	Channel 1 negative analog input. See the *Analog Inputs* section for details.
AINN2	40	40	I	Channel 2 negative analog input. See the *Analog Inputs* section for details.
AINN3	38	38	I	Channel 3 negative analog input. See the *Analog Inputs* section for details.
AINN4	—	36	I	Channel 4 negative analog input. See the *Analog Inputs* section for details.
AINN5	—	34	I	Channel 5 negative analog input. See the *Analog Inputs* section for details.
AINN6	—	32	I	Channel 6 negative analog input. See the *Analog Inputs* section for details.
AINN7	—	30	I	Channel 7 negative analog input. See the *Analog Inputs* section for details.
AINP0	43	43	I	Channel 0 positive analog input. See the *Analog Inputs* section for details.
AINP1	41	41	I	Channel 1 positive analog input. See the *Analog Inputs* section for details.
AINP2	39	39	I	Channel 2 positive analog input. See the *Analog Inputs* section for details.
AINP3	37	37	I	Channel 3 positive analog input. See the *Analog Inputs* section for details.
AINP4	—	35	I	Channel 4 positive analog input. See the *Analog Inputs* section for details.
AINP5	—	33	I	Channel 5 positive analog input. See the *Analog Inputs* section for details.
AINP6	—	31	I	Channel 6 positive analog input. See the *Analog Inputs* section for details.
AINP7	—	29	I	Channel 7 positive analog input. See the *Analog Inputs* section for details.

Table 4-1. Pin Functions (continued)

NAME	ADS117L14 PIN	ADS117L18 PIN	TYPE[1]	DESCRIPTION
AVDD1	23, 24	23, 24	P	Positive analog supply 1. See the Power Supply Recommendations section for details.
AVDD2	25	25	P	Positive analog supply 2. See the Power Supply Recommendations section for details.
AVSS	22, 28, 29, 30, 31, 32, 33, 34, 35, 36, 45, 51	22, 28, 45, 51	P	Negative analog supply. See the Power Supply Recommendations section for details.
CAPA	26, 27	26, 27	P	Analog voltage regulator output bypass. See the *CAPA and CAPD* section for details.
CAPD	20	20	P	Digital voltage regulator output bypass. See the *CAPA and CAPD* section for details.
CLKIN	16	16	I	Clock input. See the *Clock Operation* section for details.
$\overline{CS}$/SPEED	55	55	I	SPI mode: Active-low chip select. See the *SPI Programming* section for details. Hardware mode (tri-state input): Speed range select. See the *Hardware Programming* section for details.
DCLK	14	14	O	Frame-sync bit clock output. See the *Frame-Sync Data Port* section for details.
DGND	17, 21	17, 21	GND	Digital ground.
DIN0/GPIO7	13	—	I/O	Daisy-chain data input 0. See the *Frame-Sync Data Port* section for details. General-purpose input-output 7. See the *GPIO* section for details.
DIN1/GPIO6	12	—	I/O	Daisy-chain data input 1. See the *Frame-Sync Data Port* section for details. General-purpose input-output 6. See the *GPIO* section for details.
DOUT0	6	6	O	Data output 0. See the *Frame-Sync Data Port* section for details.
DOUT1	7	7	O	Data output 1. See the *Frame-Sync Data Port* section for details.
DOUT2/GPIO2	8	8	I/O	Data output 2. See the *Frame-Sync Data Port* section for details. General-purpose input-output 2. See the *GPIO* section for details.
DOUT3/GPIO3	9	9	I/O	Data output 3. See the *Frame-Sync Data Port* section for details. General-purpose input-output 3. See the *GPIO* section for details.
DOUT4/DIN3/GPIO4	—	10	I/O	Data output 4 and daisy-chain data input 3. See the *Frame-Sync Data Port* section for details. General-purpose input-output 4. See the *GPIO* section for details.
DOUT5/DIN2/GPIO5	—	11	I/O	Data output 5 and daisy-chain data input 2. See the *Frame-Sync Data Port* section for details. General-purpose input-output 5. See the *GPIO* section for details.
DOUT6/DIN1/GPIO6	—	12	I/O	Data output 6 and daisy-chain data input 1. See the *Frame-Sync Data Port* section for details. General-purpose input-output 6. See the *GPIO* section for details.
DOUT7/DIN0/GPIO7	—	13	I/O	Data output 7 and daisy-chain data input 0. See the *Frame-Sync Data Port* section for details. General-purpose input-output 7. See the *GPIO* section for details.
$\overline{ERROR}$	5	5	O	Open-drain output error signal. See the *$\overline{ERROR}$ Pin and ERR_FLAG Bit* section for details.
FSYNC	15	15	O	Frame-sync word clock output. See the *Frame-Sync Data Port* section for details.
GPIO0/TDM	3	3	I/O	General purpose input-output 0. See the *GPIO* section for details. Hardware mode (tri-state input): TDM ratio select. See the *Hardware Programming* section for details.
GPIO1/HDR	4	4	I/O	General purpose input-output 1. See the *GPIO* section for details. Hardware mode (tri-state input): Data header select. See the *Hardware Programming* section for details.
GPIO4	10	—	I/O	General-purpose input-output 4. See the *GPIO* section for details.
GPIO5	11	—	I/O	General-purpose input-output 5. See the *GPIO* section for details.
IOVDD	18, 19	18, 19	P	Digital I/O supply voltage. See the Power Supply Recommendations section for details.
MODE	54	54	I	Tri-state input. Configuration mode select: 1 = SPI program mode 0 or float = Hardware program mode
REFN	47, 48	47, 48	I	Negative reference voltage input. See the *Reference Voltage* section for details.
REFP	49, 50	49, 50	I	Positive reference voltage input. See the *Reference Voltage* section for details.
$\overline{RESET}$	52	52	I	Reset input, active low. See the *$\overline{RESET}$ Pin* section for details.

Table 4-1. Pin Functions (continued)

NAME	ADS117L14 PIN	ADS117L18 PIN	TYPE[1]	DESCRIPTION
SCLK/FLTR	56	56	I	SPI mode: Serial clock input. See the *SPI Programming* section for details. Hardware mode (tri-state input): Filter mode select. See the *Hardware Programming* section for details.
SDI/OSR0	1	1	I	SPI mode: Serial data input. See the *SPI Programming* section for details. Hardware mode (tri-state input): Filter OSR0 select. See the *Hardware Programming* section for details.
SDO/OSR1	2	2	I/O	SPI mode: Serial data output. See the *SPI Programming* section for details. Hardware mode (tri-state input): Filter OSR1 select. See the *Hardware Programming* section for details.
START	53	53	I	Conversion control. See the *Synchronization* section for details.
VCM	46	46	O	Common-mode voltage output. See the *VCM Output Voltage* section for details.
Thermal Pad			—	Thermal power pad. Connect thermal pad to AVSS.

(1) I = input, O = output, I/O = bidirectional input-output, P = power, GND = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power supply voltage	AVDD1 to AVSS	–0.3	6.5	V
	AVDD2 to AVSS	–0.3	6.5	
	AVSS to DGND	–3	0.3	
	IOVDD to DGND	–0.3	2.2	
Analog input voltage	AINPx, AINNx, REFP, REFN	AVSS – 0.3	AVDD1 + 0.3	V
Analog output voltage	CAPA to AVSS	AVSS	1.65	V
	CAPD to DGND	DGND	1.65	
	VCM to AVSS	AVSS	AVDD1	
Digital input/output voltage	To DGND	DGND – 0.3	2.2	V
Input current	Continuous, any pin except power-supply pins(2)	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional – this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Analog input pins AINPx, AINNx, REFP, and REFN are diode-clamped to AVDD1 and AVSS. Limit the input current to 10mA in the event the analog input voltage is ≥ AVDD1 + 0.3V or ≤ AVSS – 0.3V. Digital I/O pins are diode-clamped to DGND only. Limit the input current to 10mA in the event the digital pin voltage is below DGND – 0.3V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
POWER SUPPLY							
	Analog power supply	AVDD1 to AVSS	Max-speed mode	4.5		5.5	V
			High-speed mode	4.5		5.5	
			Mid-speed mode	3		5.5	
			Low-speed mode	2.85		5.5	
		AVDD1 to DGND		1.65			V
		Bipolar supply AVSS / AVDD1 ratio				1.2	|V/V|
		AVDD2 to AVSS		1.74		5.5	V
		AVSS to DGND		–2.75		0	V
	Digital power supply	IOVDD to DGND		1.65		1.95	V
ANALOG INPUTS							
V_{AINPn}, V_{AINNn}	Absolute input voltage	Input buffer off		AVSS – 0.05		AVDD1 + 0.05	V
		Input buffer on		AVSS + 0.1		AVDD1 – 0.1	
V_{INn}	Differential input voltage $V_{IN} = V_{AINPn} – V_{AINNn}$	1x input range		$–V_{REF}$		V_{REF}	V
		2x input range		$–2·V_{REF}$		$2·V_{REF}$	
VOLTAGE REFERENCE INPUTS							
V_{REF}	Differential reference voltage $V_{REF} = V_{REFP} – V_{REFN}$	Low-reference range		0.5	2.5	2.75	V
		High-reference range		1	4.096	AVDD1 – AVSS	
V_{REFN}	Negative reference voltage			AVSS – 0.05			V
V_{REFP}	Positive reference voltage	REFP buffer off				AVDD1 + 0.05	V
		REFP buffer on				AVDD1 – 0.7	
CLOCK SIGNAL							
f_{CLK}	Clock frequency	Max-speed mode		0.5	32.768	33.66	MHz
		High-speed mode		0.5	25.6	26.3	
		Mid-speed mode		0.5	12.8	13.15	
		Low-speed mode		0.5	3.2	3.29	
DIGITAL INPUTS							
	Input voltage			0		IOVDD	V
TEMPERATURE RANGE							
T_A	Ambient temperature	Operational		–50		125	°C
		Specification		–40		125	

5.4 Thermal Information

THERMAL METRIC (1)		ADS117L14, ADS117L18 VQFN (RSH) 56 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	23.5	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	11.5	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	6.3	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	0.1	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	6.2	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5V, AVDD2 = 1.8V to 5V, AVSS = 0V, IOVDD = 1.8V, V_{IN} = 0V, V_{CM} = 2.5V, V_{REFP} = 4.096V, V_{REFN} = 0V, high-reference range, 1x input range, all speed modes, all channels active, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS, MAX-SPEED MODE						
	Input current, differential input voltage	Input buffers off		125		µA/V
		Input buffers off, 2x input range		60		
		Input buffers on		±2		µA
	Input current drift, differential input voltage	Input buffers off		5		nA/V/°C
		Input buffers off, 2x input range		2		
		Input buffers on		20		nA/°C
	Input current, common-mode input voltage	Input buffers off		6.5		µA/V
		Input buffers off, 2x input range		3		
		Input buffers on		±2		µA
ANALOG INPUTS, HIGH-SPEED MODE						
	Input current, differential input voltage	Input buffers off		95		µA/V
		Input buffers off, 2x input range		47		
		Input buffers on		±1.5		µA
	Input current drift, differential input voltage	Input buffers off		3		nA/V/°C
		Input buffers off, 2x input range		1.5		
		Input buffers on		5		nA/°C
	Input current, common-mode input voltage	Input buffers off		5		µA/V
		Input buffers off, 2x input range		2.5		
		Input buffers on		±1.5		µA
ANALOG INPUTS, MID-SPEED MODE						
	Input current, differential input voltage	Input buffers off		47		µA/V
		Input buffers off, 2x input range		25		
		Input buffers on		±1.5		µA
	Input current drift, differential input voltage	Input buffers off		2		nA/V/°C
		Input buffers off, 2x input range		1		
		Input buffers on		5		nA/°C
	Input current, common-mode input voltage	Input buffers off		2.5		µA/V
		Input buffers off, 2x input range		1.3		
		Input buffers on		±1.5		µA
ANALOG INPUTS, LOW-SPEED MODE						
	Input current, differential input voltage	Input buffers off		12		µA/V
		Input buffers off, 2x input range		6		
		Input buffers on		±0.4		µA
	Input current drift, differential input voltage	Input buffers off		1		nA/V/°C
		Input buffers off, 2x input range		0.5		
		Input buffers on		0.2		nA/°C
	Input current, common-mode input voltage	Input buffers off		0.6		µA/V
		Input buffers off, 2x input range		0.3		
		Input buffers on		±0.4		µA

5.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5V, AVDD2 = 1.8V to 5V, AVSS = 0V, IOVDD = 1.8V, V_{IN} = 0V, V_{CM} = 2.5V, V_{REFP} = 4.096V, V_{REFN} = 0V, high-reference range, 1x input range, all speed modes, all channels active, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC CHARACTERISTICS							
	Resolution	No missing codes		16			Bits
e_n	DC Noise			See the Noise Performance section for details			
	Offset error	T_A = 25°C		–250	±60	250	µV
	Offset drift				50	200	nV/°C
	Gain error	T_A = 25°C		–2500	±200	2500	ppm of FSR
	Gain drift				1	3	ppm of FSR/°C
INL	Integral nonlinearity (1)				0.5	1	LSB
CMRR	Common-mode rejection ratio	DC		90	115		dB
		Up to 10kHz			110		
		DC, 2x input range			105		
PSRR	Power-supply rejection ratio	AVDD1, dc			98		dB
		AVDD2, dc			130		
		IOVDD, dc			108		
AC CHARACTERISTICS							
f_{DATA}	Data rate	Max-speed mode	Wideband filter	4		512	kSPS
			Low-latency filter	0.1024		1365.3	
		High-speed mode	Wideband filter	3.125		400	
			Low-latency filter	0.08		1067	
		Mid-speed mode	Wideband filter	1.5625		200	
			Low-latency filter	0.08		533.3	
		Low-speed mode	Wideband filter	0.390625		50	
			Low-latency filter	0.01		133.3	
SNR	Signal-to-noise ratio	f_{IN} = 1kHz, V_{IN} = –0.2dBFS, OSR = 64	Wideband filter	97.0	97.7		dB
			Wideband filter, V_{REF} = 2.5V, 2x input range		97.5		
			Low-latency filter	97.0	97.9		
			Low-latency filter V_{REF} = 2.5V, 2x input range		97.8		
THD	Total harmonic distortion	f_{IN} = 1kHz, V_{IN} = –0.2dBFS			–115	–105	dB
		Max-speed mode			–105	–100	
IMD	Intermodulation distortion	f_{IN} = 9.7kHz and 10.3kHz, V_{IN} = –6.5dBFS	Second-order terms		–120		dB
			Third-order terms		–110		
SFDR	Spurious-free dynamic range	f_{IN} = 1kHz, V_{IN} = –0.2dBFS			110		dB
	Crosstalk	f_{IN} = 1kHz, V_{IN} = –0.2dBFS (3)			–120		dB
NMRR	Normal-mode rejection ratio	f_{IN} = 50Hz (±1Hz), f_{DATA} = 50SPS, sinc3 filter		100			dB
		f_{IN} = 60Hz (±1Hz), f_{DATA} = 60SPS, sinc3 filter		100			
WIDEBAND FILTER CHARACTERISTICS							
	Pass-band frequency	Within envelope of pass-band ripple			0.4 · f_{DATA}		Hz
		–0.1dB frequency			0.4125 · f_{DATA}		
		–3dB frequency			0.4374 · f_{DATA}		
	Pass-band ripple			–0.0004		0.0004	dB
	Stop-band frequency	At stop-band attenuation			0.5 · f_{DATA}		Hz
	Stop-band attenuation (2)				106		dB

5.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5V, AVDD2 = 1.8V to 5V, AVSS = 0V, IOVDD = 1.8V, V_{IN} = 0V, V_{CM} = 2.5V, V_{REFP} = 4.096V, V_{REFN} = 0V, high-reference range, 1x input range, all speed modes, all channels active, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Group delay				34 / f_{DATA}		s
	Settling time				68 / f_{DATA}		s
VOLTAGE REFERENCE INPUTS							
	REFP and REFN input current	REFP buffer off	Max-speed mode		225		µA/V/ch
			High-speed mode		190		
			Mid-speed mode		130		
			Low-speed mode		80		
	REFP input current	REFP buffer on			±3		µA/ch
	REFP and REFN input current drift	REFP buffer off			20		nA/°C/ch
	REFP input current drift	REFP buffer on			10		nA/°C/ch
INTERNAL OSCILLATOR							
f_{OSC}	Oscillator frequency			25.4	25.6	25.8	MHz
VCM OUTPUT VOLTAGE							
	Output voltage				(AVDD1 + AVSS) / 2		V
	Accuracy			–1%	±0.1%	1%	
	Voltage noise	1kHz bandwidth			25		$µV_{RMS}$
	Start-up time	C_L = 100nF			1		ms
	Capacitive load					100	nF
	Resistive load			2			kΩ
	Short-circuit current limit				10		mA
DIGITAL INPUTS/OUTPUTS							
V_{IL}	Logic-low input level					0.3 IOVDD	V
V_{IH}	Logic-high input level			0.7 IOVDD			V
I_{LEAK}	External leakage current	Tri-state pins, floating input state		-5		5	µA
C_{LOAD}	Capacitive load	Tri-state pins, floating input state				50	pF
R_{EXT}	Pull-up or pull-down resistance	Tri-state pins, logic low or high state		0		3	kΩ
V_{OL}	Logic-low output level	OUT_DRV = 0b, I_{OL} = 2mA				0.2 · IOVDD	V
		OUT_DRV = 1b, I_{OL} = 1mA				0.2 · IOVDD	
V_{OH}	Logic-high output level	OUT_DRV = 0b, I_{OH} = –2mA		0.8 · IOVDD			V
		OUT_DRV = 1b, I_{OH} = –1mA		0.8 · IOVDD			
		$\overline{\text{ERROR}}$ pin, I_{OH} = –2µA		0.8 · IOVDD			
	Input hysteresis				150		mV
	Input current			–1		1	µA

5.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5V, AVDD2 = 1.8V to 5V, AVSS = 0V, IOVDD = 1.8V, V_{IN} = 0V, V_{CM} = 2.5V, V_{REFP} = 4.096V, V_{REFN} = 0V, high-reference range, 1x input range, all speed modes, all channels active, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SUPPLY CURRENT							
I_{AVDD1}, I_{AVSS}	AVDD1, AVSS current (buffers off)	One channel	Max-speed mode		1.9	2.1	mA
		Each additional channel			1.7	2.0	mA/ch
		One channel	High-speed mode		1.5	1.7	mA
		Each additional channel			1.3	1.6	mA/ch
		One channel	Mid-speed mode		0.9	1.0	mA
		Each additional channel			0.7	0.85	mA/ch
		One Channel	Low-speed mode		0.3	0.35	mA
		Each additional channel			0.2	0.21	mA/ch
		Standby mode			110		µA
		Power-down mode			5		µA
	AVDD1, AVSS buffer current	Input buffers	Max-speed mode		1.78	2.1	mA/buffer
			High-speed mode		1.36	1.6	
			Mid-speed mode		0.7	0.85	
			Low-speed mode		0.2	0.25	
		REFP buffers	Max-speed mode		1.6	1.7	mA/buffer
			High-speed mode		1.5	1.65	
			Mid-speed mode		0.9	1.0	
			Low-speed mode		0.4	0.5	
		VCM buffer			0.1		mA
I_{AVDD2}, I_{AVSS}	AVDD2, AVSS current	Max-speed mode			4.6	5.1	mA/ch
		High-speed mode			3.6	4.0	
		Mid-speed mode			2.3	2.55	
		Low-speed mode			0.85	0.96	
		Standby mode			60		µA
		Power-down mode			1		µA
DIGITAL SUPPLY CURRENT							
I_{IOVDD}	IOVDD current	Wideband filter OSR = 32	Max-speed mode		2.1	2.5	mA/ch
			High-speed mode		1.6	2.0	
			Mid-speed mode		0.8	1	
			Low-speed mode		0.2	0.35	
		Low-latency filter OSR = 32	Max-speed mode		0.6	0.8	
			High-speed mode		0.5	0.7	
			Mid-speed mode		0.20	0.35	
			Low-speed mode		0.05	0.15	
		Standby mode	External clock		15		µA
			Internal oscillator		50		
		Power-down mode			35		µA

5.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5V, AVDD2 = 1.8V to 5V, AVSS = 0V, IOVDD = 1.8V, V_{IN} = 0V, V_{CM} = 2.5V, V_{REFP} = 4.096V, V_{REFN} = 0V, high-reference range, 1x input range, all speed modes, all channels active, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER DISSIPATION							
P_D	Power dissipation	ADS117L14 wideband filter, AVDD2 = 1.8V, buffers off	Max-speed mode		83	95	mW
			High-speed mode		64	76	
			Mid-speed mode		37	43	
			Low-speed mode		12	14	
		ADS117L14 low-latency filter, AVDD2 = 1.8V, buffers off	Max-speed mode		72	83	
			High-speed mode		57	66	
			Mid-speed mode		33	39	
			Low-speed mode		11	13	
		ADS117L18 wideband filter, AVDD2 = 1.8V, buffers off	Max-speed mode		165	190	mW
			High-speed mode		128	151	
			Mid-speed mode		74	86	
			Low-speed mode		24	28	
		ADS117L18 low-latency filter, AVDD2 = 1.8V, buffers off	Max-speed mode		144	165	
			High-speed mode		112	132	
			Mid-speed mode		65	77	
			Low-speed mode		21	25	

(1) Best-fit method.
(2) Stop-band attenuation as provided by the digital filter. Input frequencies in the stop band intermodulate with the chop frequency beginning at f_{MOD} / 32, which results in stop-band attenuation <106dB. See the Stop-Band Attenuation figure for details.
(3) Crosstalk measured on one shorted-input channel with three (ADS117L14) and seven (ADS117L18) active channels.

5.6 Timing Requirements

1.65V ≤ IOVDD ≤ 1.95V, over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
CLOCK				
$t_{c(CLKIN)}$	CLKIN period	15	2000	ns
$t_{w(CLKINL)}$	Pulse duration, CLKIN low	6.5		ns
$t_{w(CLKINH)}$	Pulse duration, CLKIN high	6.5		ns
$t_{c(CLK)}$ (1)	ADC clock period, max-speed mode	29.7	2000	ns
	ADC clock period, high-speed mode	38	2000	
	ADC clock period, mid-speed mode	76	2000	
	ADC clock period, low-speed mode	304	2000	
$t_{w(CLKL)}$	Pulse duration, CLK low, max-speed mode	13.2		ns
	Pulse duration, CLK low, high-speed mode	17		
	Pulse duration, CLK low, mid-speed mode	34		
	Pulse duration, CLK low, low-speed mode	128		
$t_{w(CLKH)}$	Pulse duration, CLK high, max-speed mode	13.2		ns
	Pulse duration, CLK high, high-speed mode	17		
	Pulse duration, CLK high, mid-speed mode	34		
	Pulse duration, CLK high, low-speed mode	128		
FRAME-SYNC (DATA PORT)				
$t_{c(DCLK)}$	DCLK period, stand-alone operation	15		ns
	DCLK period, daisy-chain operation	29.7		ns
SPI (CONFIGURATION PORT)				
$t_{c(SCLK)}$	SCLK period	75		ns
$t_{w(SCL)}$	Pulse duration, SCLK low	25		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	25		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	20		ns
$t_{su(DI)}$	Setup time, SDI valid before SCLK falling edge	6		ns
$t_{h(DI)}$	Hold time, SDI valid after SCLK falling edge	8		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	20		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20		ns
START PIN				
$t_{w(STL)}$	Pulse duration, START low	4		t_{CLK}
$t_{w(STH)}$	Pulse duration, START high	4		t_{CLK}
$t_{su(STCL)}$	Setup time, START rising edge before CLKIN rising edge (2)	4		ns
$t_{h(STCL)}$	Hold time, START rising edge after CLKIN rising edge (2)	6		ns
$t_{su(STFS)}$	Setup time, START falling edge or STOP bit set before FSYNC rising edge to stop next conversion (start/stop conversion mode)	24		t_{CLK}
$\overline{RESET}$ PIN				
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low	4		t_{CLK}

(1) f_{CLK} is the main ADC clock.
(2) To avoid synchronization uncertainty, avoid driving START high between the setup and hold time specifications.

5.7 Switching Characteristics

1.65V ≤ IOVDD ≤ 1.9V, over operating ambient temperature range, OUT_DRV = 0b, C_{LOAD} = 20pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK						
$t_{C(CLK)}$	ADC clock period (programmable) (1)			1, 2, 3, 4 or 8 / f_{CLKIN} or / f_{OSC}		
FRAME-SYNC (DATA PORT)						
$t_{c(FSYNC)}$	FSYNC period			1 / f_{DATA}		ns
$t_{w(FSYNCH)}$	Pulse duration, FSYNC high			0.5 / f_{DATA}		ns
$t_{w(FSYNCL)}$	Pulse duration, FSYNC low			0.5 / f_{DATA}		ns
$t_{p(FSDC)}$	Propagation delay time, FSYNC rising edge to DCLK falling edge		–1		1	ns
$t_{c(DCLK)}$	DCLK period (programmable) (1)			1, 2, 4, or 8 / f_{CLKIN} or / f_{OSC}		
$t_{w(DCLKH)}$	Pulse duration, DCLK low			0.5 · $t_{C(DCLK)}$		ns
$t_{w(DCLKL)}$	Pulse duration, DCLK high			0.5 · $t_{C(DCLK)}$		ns
$t_{h(DCDO)}$	Hold time, DCLK falling edge to previous DOUT invalid		–2			ns
$t_{p(DCDO)}$	Propagation delay time, DCLK falling edge to new DOUT valid				7	ns
SPI (CONFIGURATION PORT)						
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to SDO driven state				16	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to SDO tri-state				16	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid SDO				20	ns
START PIN						
$t_{p(STFS1)}$	Propagation delay time, START falling edge to FSYNC signal stop (Start/stop mode)			11		t_{CLK}
$t_{p(STDC)}$	Propagation delay time, START falling edge to DCLK signal stop (Start/stop mode)			7		t_{CLK}
$t_{p(STFS2)}$	Propagation delay time, START rising edge to FSYNC rising edge (first conversion ready)		See the Digital Filter section			
$\overline{RESET}$ PIN						
$t_{p(RSFS)}$	Propagation delay time, $\overline{RESET}$ rising edge to FSYNC falling edge (ADC ready)			10^4		t_{CLK}

(1) Daisy-chaining requires external clock operation and CLK_DIV[2:0], DCLK_DIV[1:0] = divide by 1.

5.8 Timing Diagrams

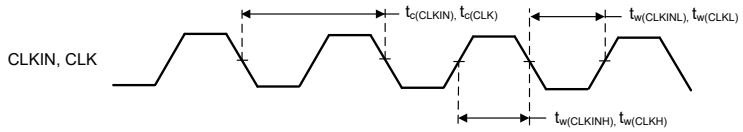


Figure 5-1. Clock Timing Requirements

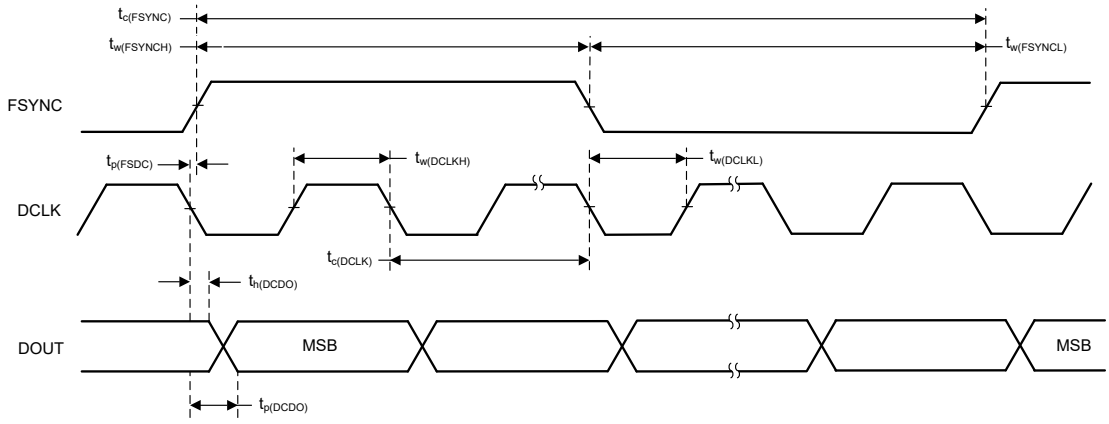


Figure 5-2. Frame-Sync Port Switching Characteristics

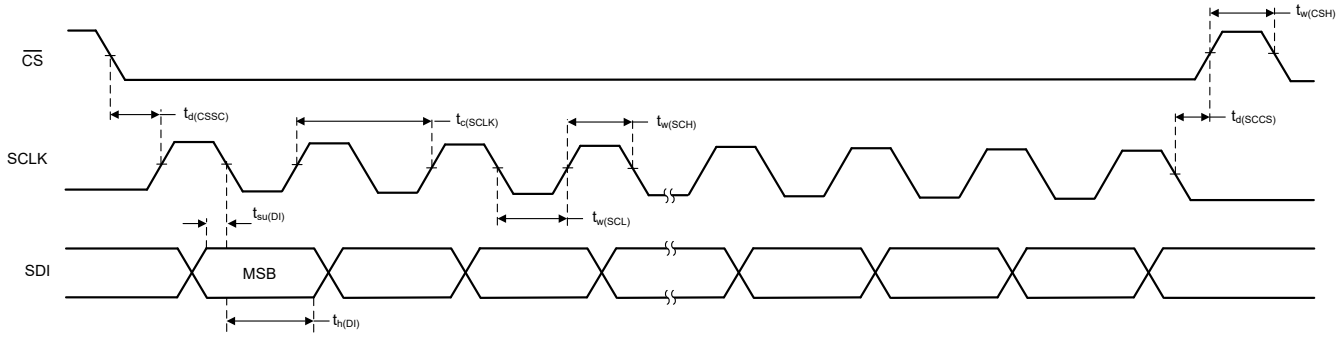


Figure 5-3. SPI Timing Requirements

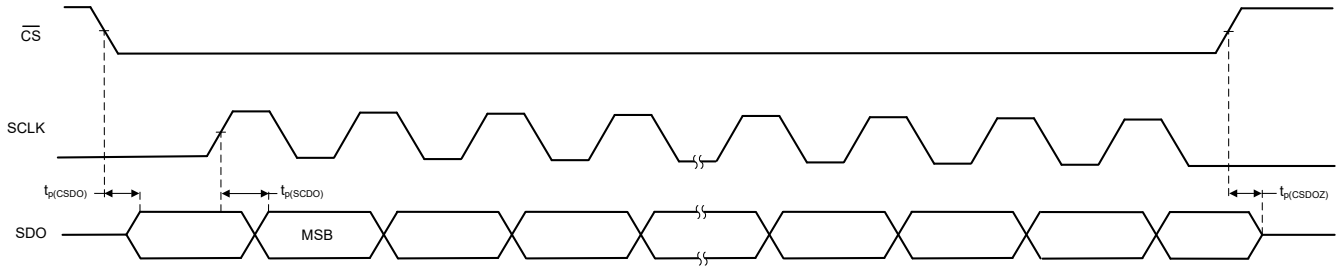


Figure 5-4. SPI Switching Characteristics

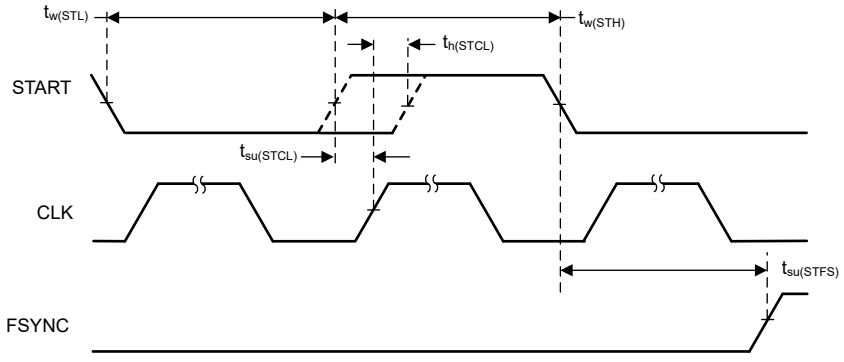


Figure 5-5. START Pin Timing Requirements

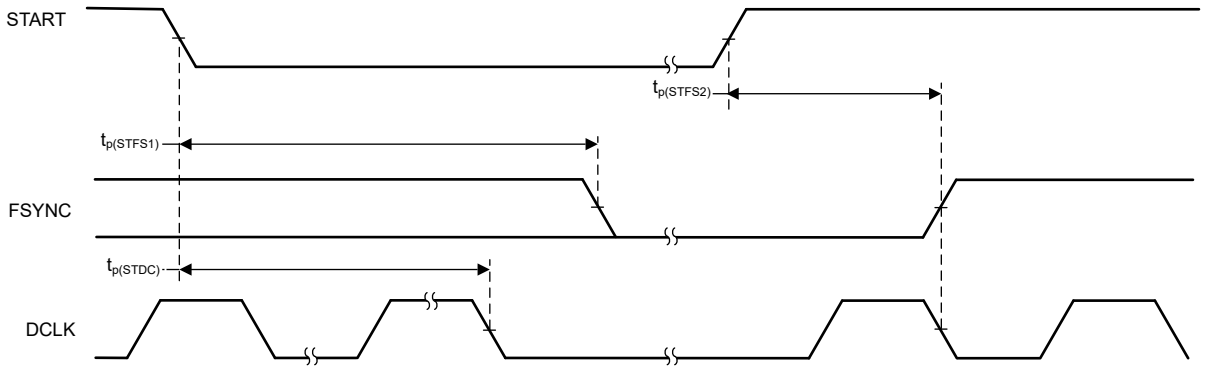


Figure 5-6. START Pin Switching Characteristics

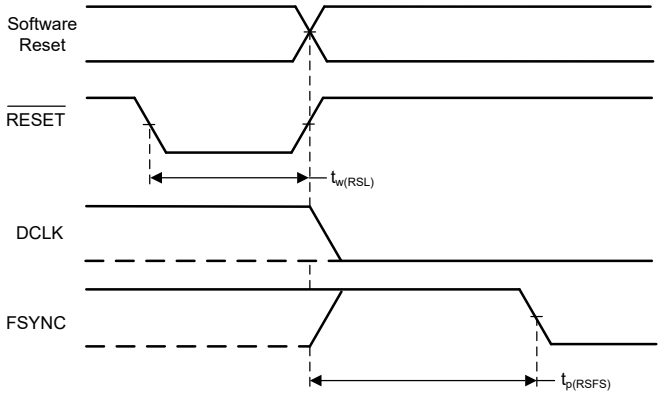


Figure 5-7. $\overline{\text{RESET}}$ Pin Timing Requirements and Switching Characteristic

5.9 Typical Characteristics

AVDD1 = AVDD2 = 5V, AVSS = 0V, IOVDD = 1.8V, V_{REF} = 4.096V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C. Data represent typical channel performance (unless otherwise noted).

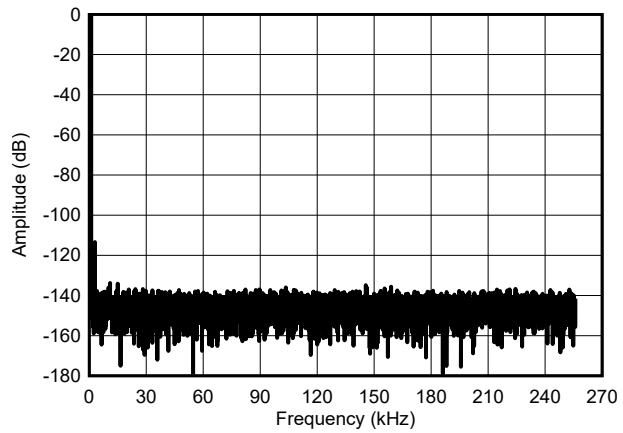


Figure 5-8. Max-Speed Mode, Full-Scale FFT

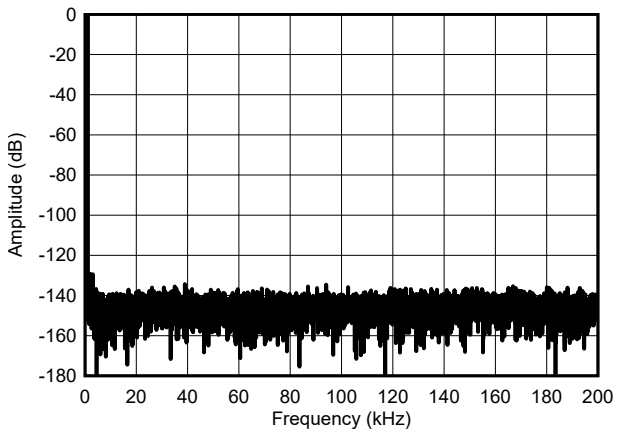


Figure 5-9. High-Speed Mode, Full-Scale FFT

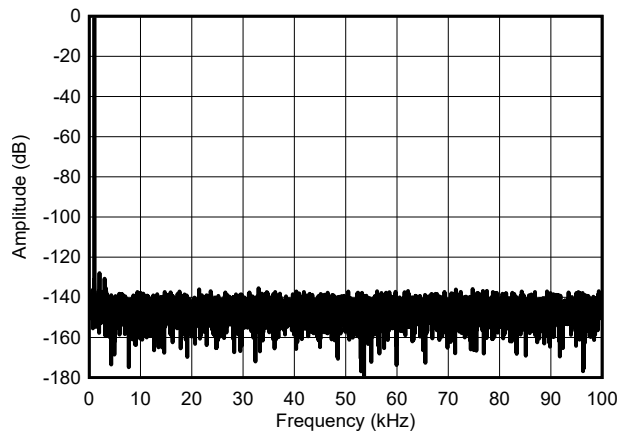


Figure 5-10. Mid-Speed Mode, Full-Scale FFT

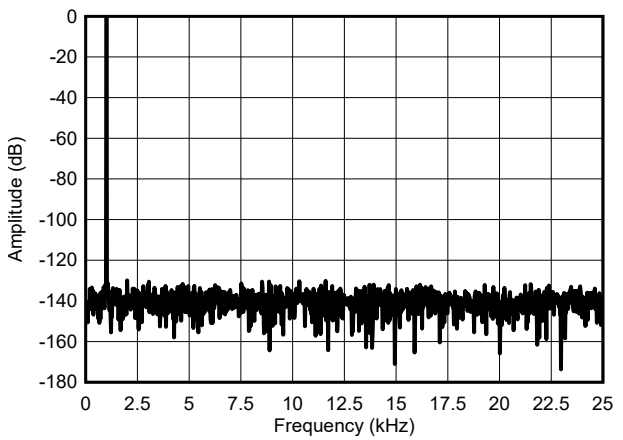


Figure 5-11. Low-Speed Mode, Full-Scale FFT

5.9 Typical Characteristics (continued)

AVDD1 = AVDD2 = 5V, AVSS = 0V, IOVDD = 1.8V, V_{REF} = 4.096V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C. Data represent typical channel performance (unless otherwise noted).

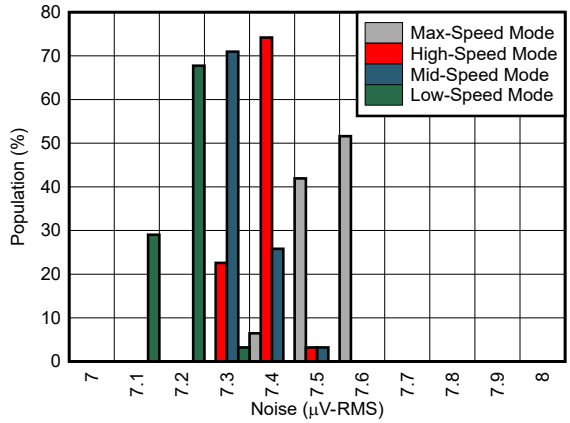


Figure 5-12. Noise Histogram

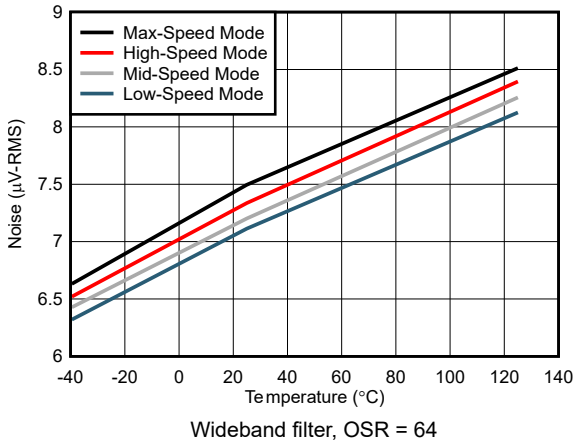


Figure 5-13. Noise vs. Temperature

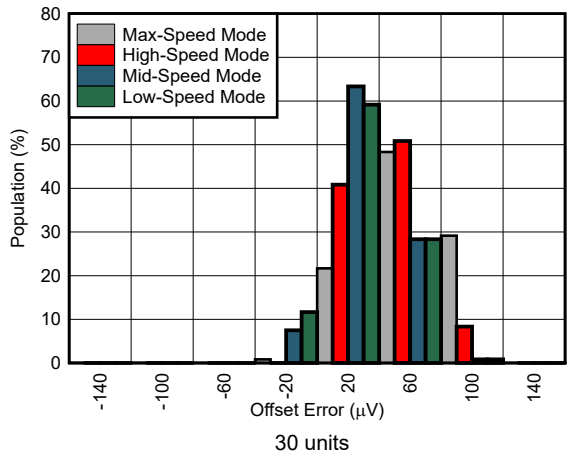


Figure 5-14. Offset Voltage Histograms

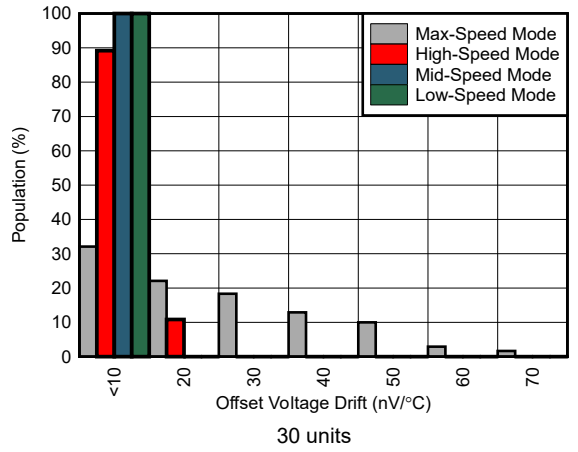


Figure 5-15. Offset Voltage Drift Histograms

5.9 Typical Characteristics (continued)

AVDD1 = AVDD2 = 5V, AVSS = 0V, IOVDD = 1.8V, V_{REF} = 4.096V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C. Data represent typical channel performance (unless otherwise noted).

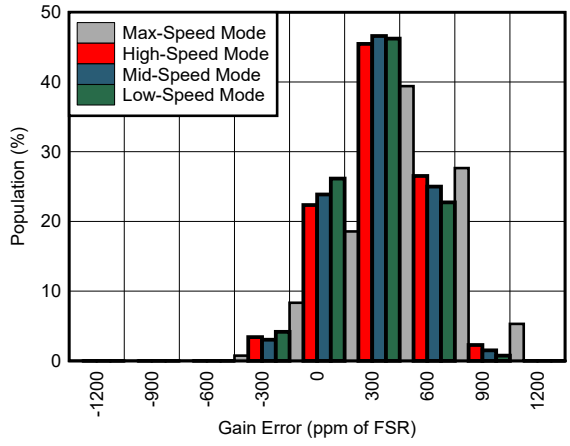


Figure 5-16. Gain Error Histograms

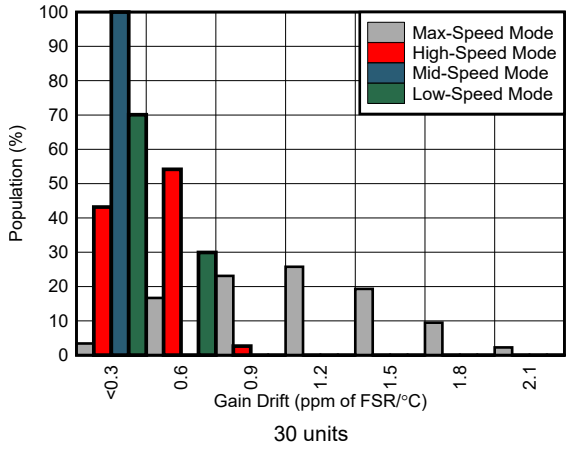


Figure 5-17. Gain Drift Histograms

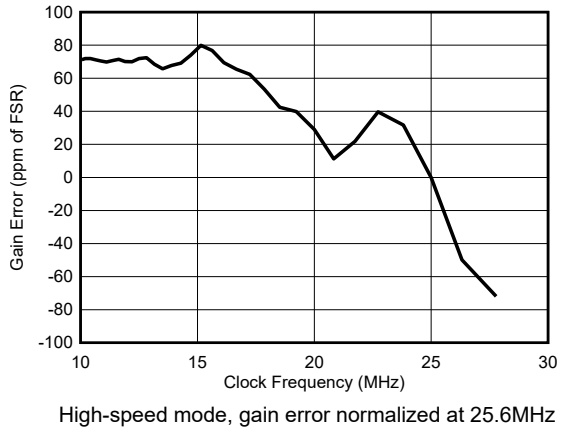


Figure 5-18. Gain Error vs. Clock Frequency

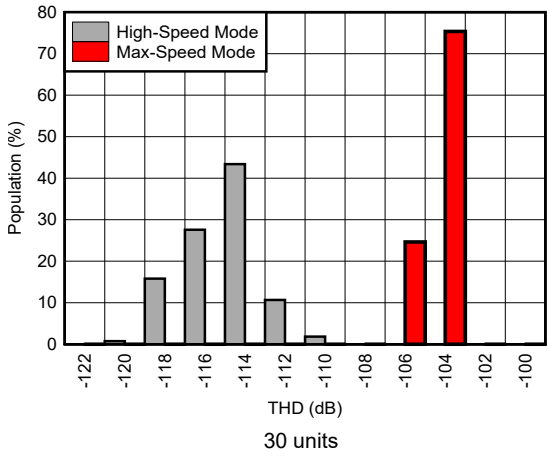


Figure 5-19. THD Histogram

5.9 Typical Characteristics (continued)

AVDD1 = AVDD2 = 5V, AVSS = 0V, IOVDD = 1.8V, V_{REF} = 4.096V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C. Data represent typical channel performance (unless otherwise noted).

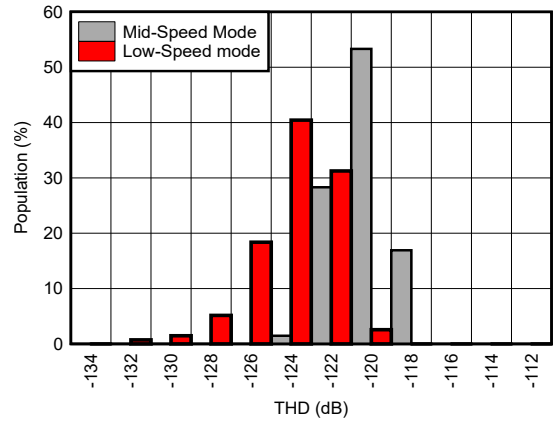


Figure 5-20. THD Histogram

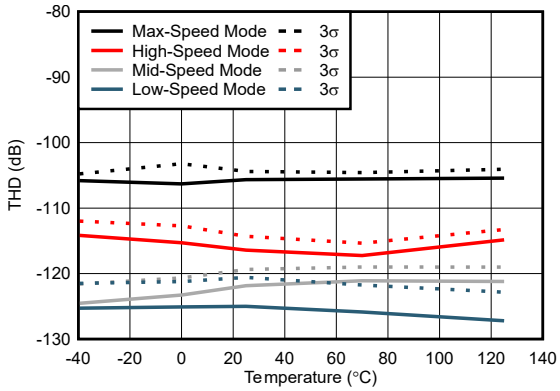


Figure 5-21. THD vs. Temperature

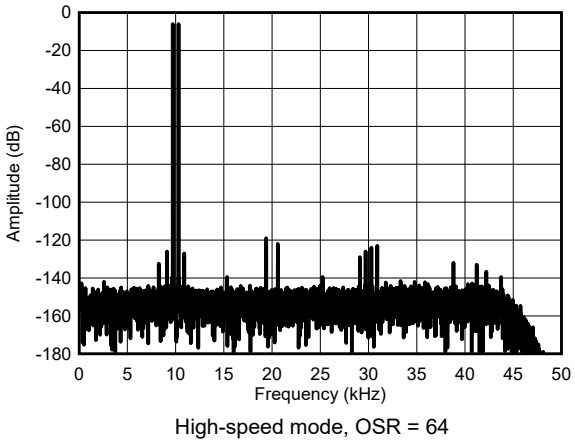


Figure 5-22. IMD FFT

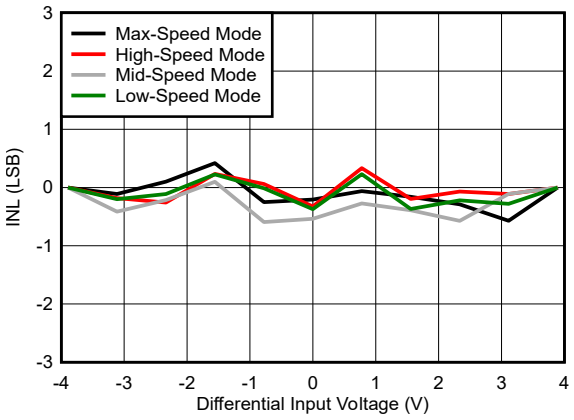


Figure 5-23. INL vs. Input Voltage

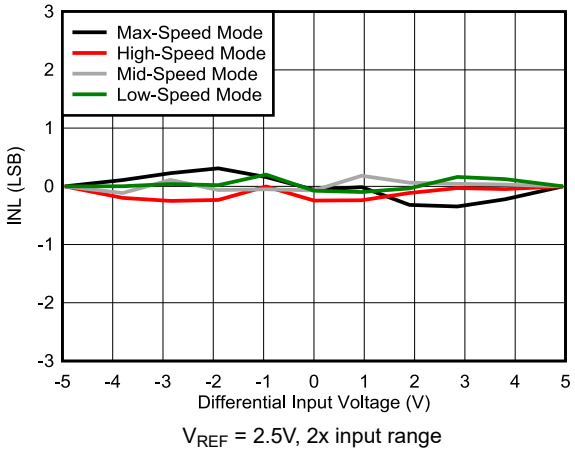


Figure 5-24. INL vs. Input Voltage

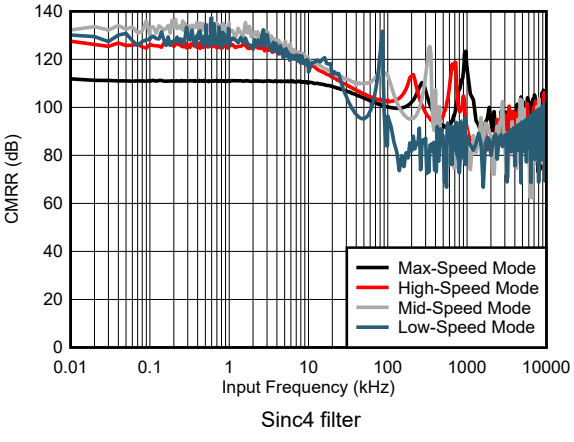
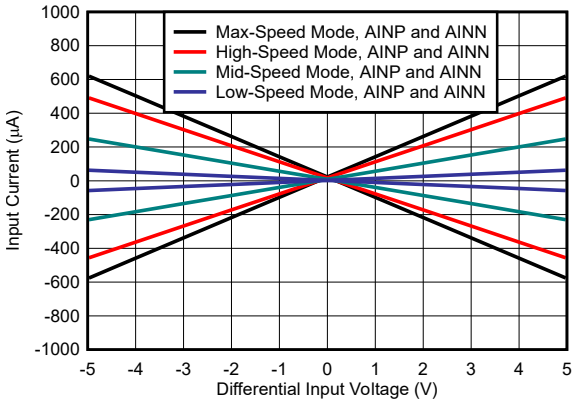


Figure 5-25. CMRR vs. Frequency

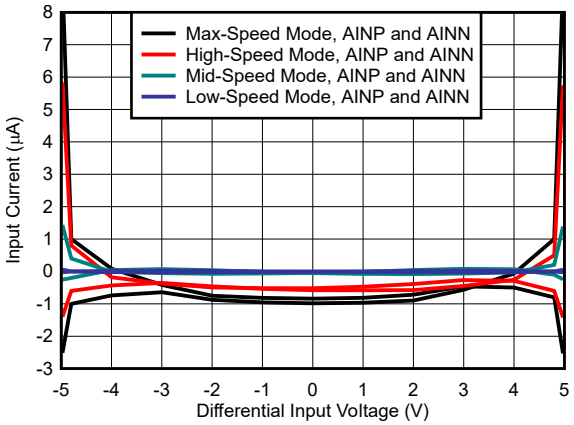
5.9 Typical Characteristics (continued)

AVDD1 = AVDD2 = 5V, AVSS = 0V, IOVDD = 1.8V, V_{REF} = 4.096V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C. Data represent typical channel performance (unless otherwise noted).



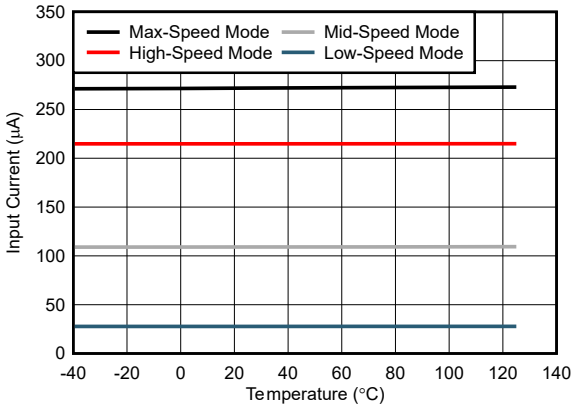
Input buffers OFF

Figure 5-26. Input Current vs. Input Voltage



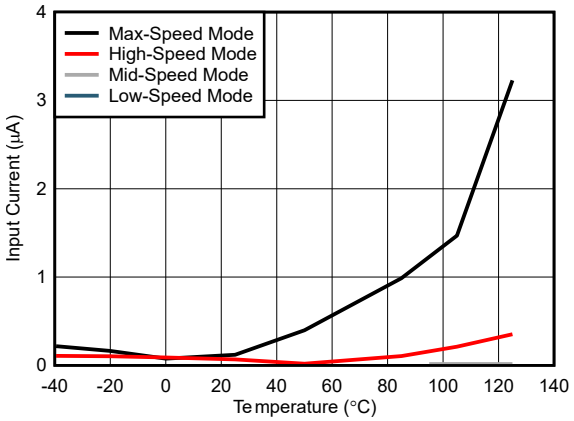
Input buffers ON

Figure 5-27. Input Current vs. Input Voltage



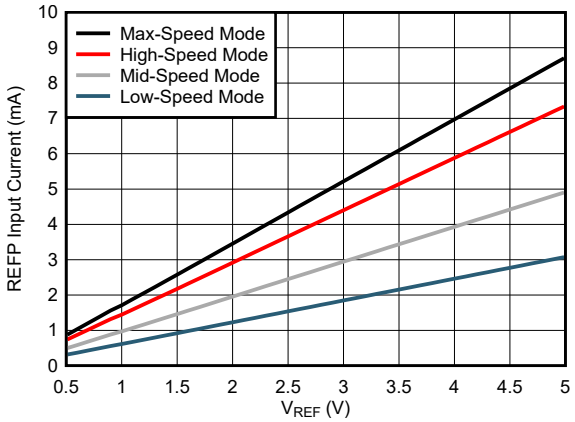
V_{IN} = 2.5V, input buffers OFF

Figure 5-28. Input Current vs. Temperature



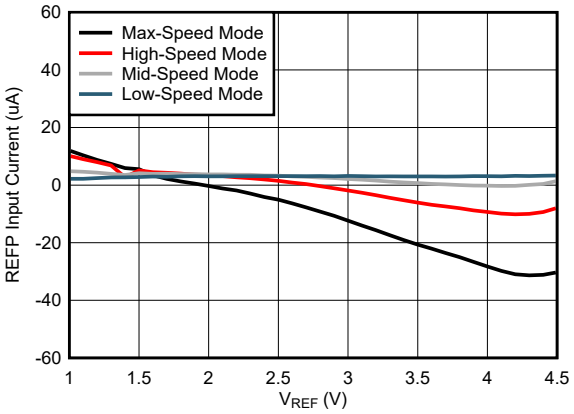
Input buffers ON

Figure 5-29. Input Current vs. Temperature



ADS117L18, REFP buffer OFF

Figure 5-30. REFP Input Current vs. Reference Voltage



ADS117L18, REFP buffer ON

Figure 5-31. REFP Input Current vs. Reference Voltage

5.9 Typical Characteristics (continued)

AVDD1 = AVDD2 = 5V, AVSS = 0V, IOVDD = 1.8V, V_{REF} = 4.096V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C. Data represent typical channel performance (unless otherwise noted).

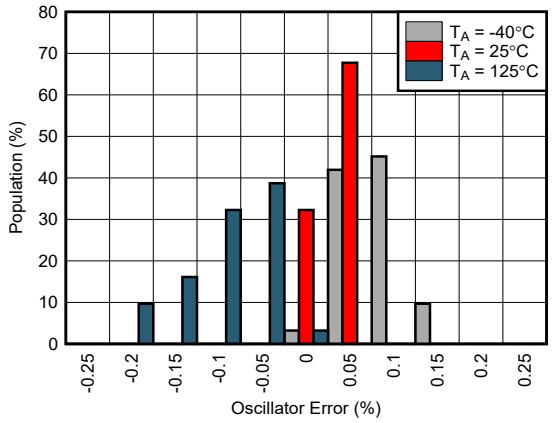


Figure 5-32. Oscillator Frequency Histogram

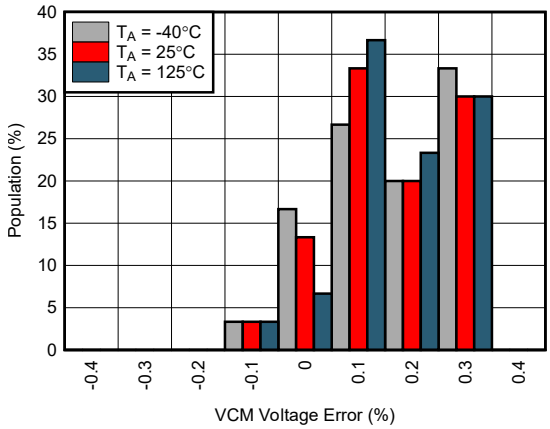


Figure 5-33. VCM Output Voltage Histogram

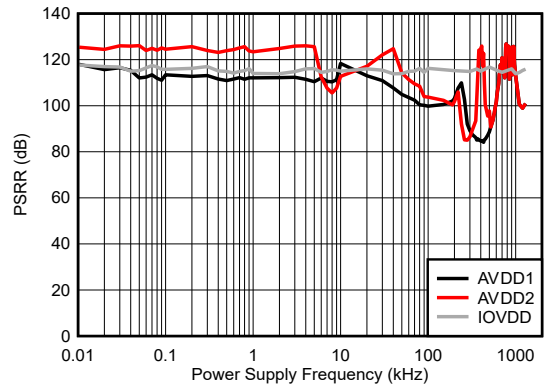


Figure 5-34. PSRR vs. Power Supply Frequency

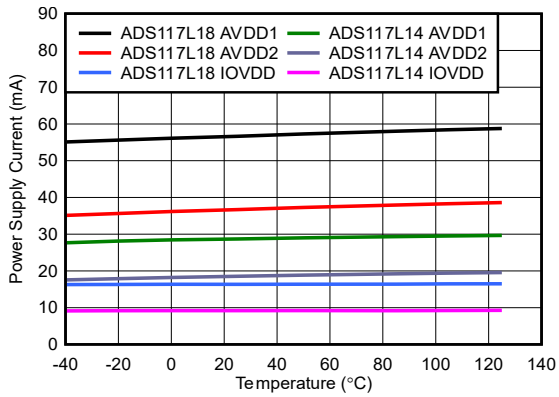


Figure 5-35. Max-Speed Mode Power Supply Currents vs. Temperature

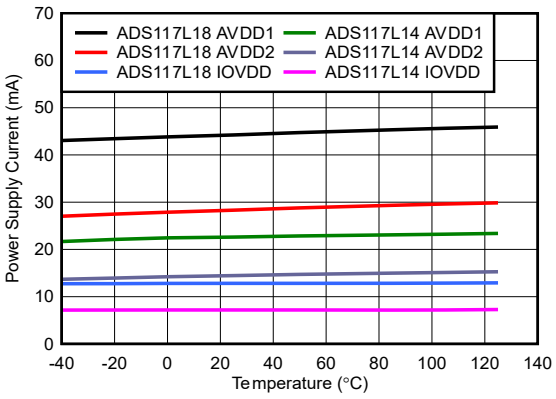


Figure 5-36. High-Speed Mode Power Supply Currents vs. Temperature

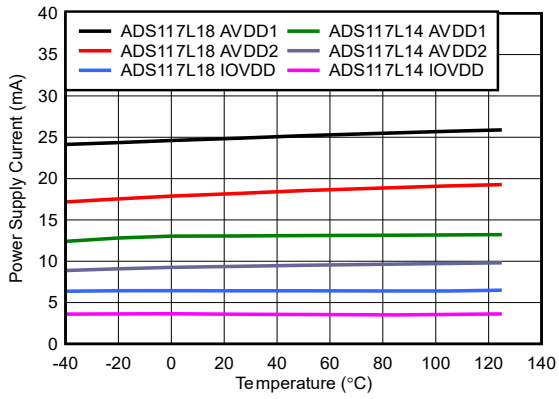


Figure 5-37. Mid-Speed Mode Power Supply Currents vs. Temperature

5.9 Typical Characteristics (continued)

AVDD1 = AVDD2 = 5V, AVSS = 0V, IOVDD = 1.8V, V_{REF} = 4.096V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C. Data represent typical channel performance (unless otherwise noted).

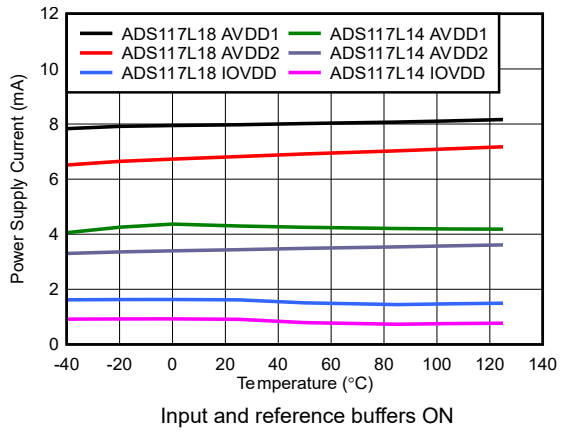


Figure 5-38. Low-Speed Mode Power Supply Currents vs. Temperature

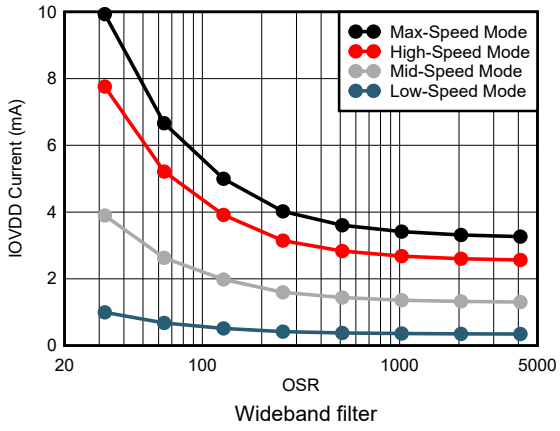


Figure 5-39. ADS117L14 IOVDD Current vs. OSR

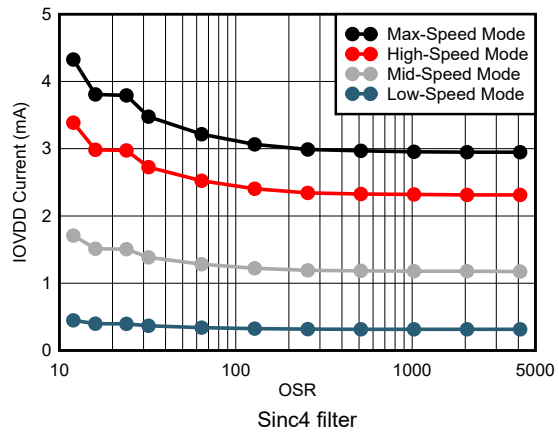


Figure 5-40. ADS117L14 IOVDD Current vs. OSR

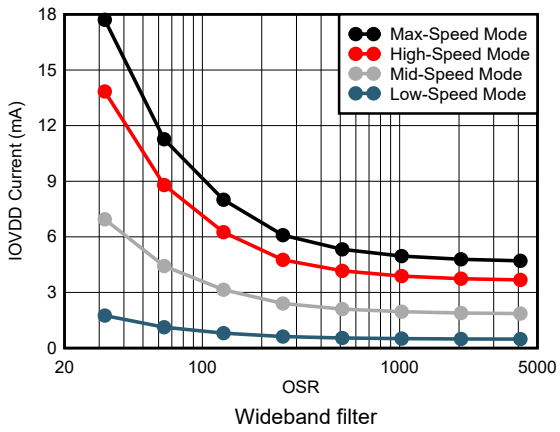


Figure 5-41. ADS117L18 IOVDD Current vs. OSR

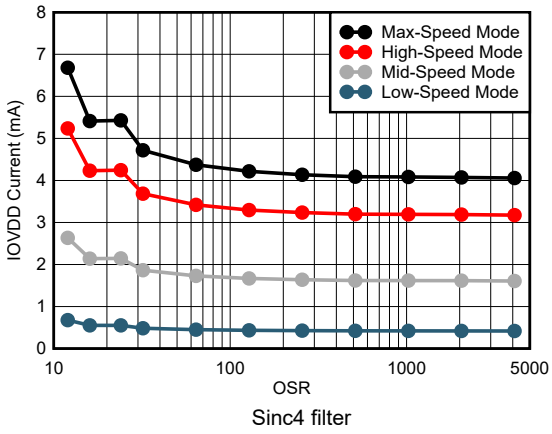


Figure 5-42. ADS117L18 IOVDD Current vs. OSR

6 Parameter Measurement Information

6.1 Offset Error Measurement

Offset error is measured with the ADC inputs externally shorted together. The input common-mode voltage is fixed to the mid-point of the AVDD1 and AVSS power-supply range. Offset error is specified at T_A = 25°C.

6.2 Offset Drift Measurement

Offset drift is defined as the change in offset voltage measured at multiple points over the specified temperature range. Offset drift is calculated using the *box method* where a box is formed over the maximum and minimum offset voltages and specified temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Equation 1 shows the offset drift calculation using the box method.

$$\text{Offset Drift (nV/°C)} = 10^9 \cdot (V_{OFSMAX} - V_{OFSMIN}) / (T_{MAX} - T_{MIN}) \quad (1)$$

where:

- V_{OFSMAX} and V_{OFSMIN} = Maximum and minimum offset voltages over the specified temperature range
- T_{MAX} and T_{MIN} = Maximum and minimum temperatures

6.3 Gain Error Measurement

Gain error is defined as the difference between the actual and the ideal slopes of the ADC transfer function. Gain error is measured by applying dc test voltages at –95% and 95% of FSR. The error is calculated by subtracting the difference of the dc test voltages (ideal slope) from the difference in the ADC output voltages (actual slope). The difference in the slopes is divided by the ideal slope and multiplied by 10^6 to convert the error to ppm of FSR. Errors resulting from the ADC reference voltage are excluded from the gain error measurement. The gain error is specified at T_A = 25°C. Equation 2 shows the calculation of gain error:

$$\text{Gain Error (ppm of FSR)} = 10^6 \cdot (\Delta V_{OUT} - \Delta V_{IN}) / \Delta V_{IN} \quad (2)$$

where:

- ΔV_{OUT} = Difference of two ADC output voltages
- ΔV_{IN} = Difference of two input test voltages

6.4 Gain Drift Measurement

Gain drift is defined as the change of gain error measured at multiple points over the specified temperature range. The box method is used in which a box is formed over the maximum and minimum gain errors over the specified temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Equation 3 describes the gain drift calculation using the box method.

$$\text{Gain Drift (ppm/°C)} = (GE_{MAX} - GE_{MIN}) / (T_{MAX} - T_{MIN}) \quad (3)$$

where:

- GE_{MAX} and GE_{MIN} = Maximum and minimum gain errors over the specified temperature range
- T_{MAX} and T_{MIN} = Maximum and minimum temperatures

6.5 NMRR Measurement

Normal-mode rejection ratio (NMRR) specifies the ability of the ADC to reject normal-mode input signals at specific frequencies. These input frequencies are usually expressed at 50Hz and 60Hz. Normal-mode rejection is uniquely determined by the frequency response of the digital filter. In this case, nulls in the frequency response of the low-latency sinc3 filter option located at 50Hz and 60Hz provide rejection at these frequencies.

6.6 CMRR Measurement

Common-mode rejection ratio (CMRR) specifies the ability of the ADC to reject common-mode input signals. CMRR is expressed as dc and ac parameters. For measurement of CMRR (dc), three common-mode test voltages are applied with the inputs externally shorted together. These test voltages are equal to AVSS + 50mV, (AVDD1 + AVSS) / 2, and AVDD1 – 50mV. The maximum change of the ADC offset voltage is recorded versus the change in common-mode test voltage. Equation 4 shows how CMRR (dc) is computed.

$$\text{CMRR (dc) (dB)} = 20 \cdot \log(\Delta V_{CM} / \Delta V_{OS}) \quad (4)$$

where:

- ΔV_{CM} = Change of dc common-mode test voltage
- ΔV_{OS} = Change of corresponding offset voltage

For the measurement of CMRR (ac), an ac common-mode signal is applied at various test frequencies at 95% full-scale range. An FFT is computed from the ADC data with the common-mode signal applied. Equation 5 shows that the nine largest amplitude spurious frequencies in the frequency spectrum are summed as powers. These frequencies are then related to the amplitude of the common-mode test signal.

$$\text{CMRR (ac) (dB)} = 20 \cdot \log(V_{CM} / V_O) \quad (5)$$

where:

- V_{CM} (RMS) = Common-mode input signal amplitude
- V_O (RMS) = Root-sum-square amplitude of spurious frequencies = $\sqrt{(V_0{}^2 + V_1{}^2 + ...V_8{}^2)}$

6.7 PSRR Measurement

Power-supply rejection ratio (PSRR) specifies the ability of the ADC to reject power-supply interference. PSRR is expressed as ac and dc parameters. For PSRR (dc) measurement, the power-supply voltage is changed over the minimum, nominal, and maximum specified voltage ranges with the inputs externally shorted together. The maximum change of ADC offset voltage is recorded versus the change in power-supply voltage. PSRR (dc) is computed as shown in Equation 6 as the ratio of change of the power-supply voltage step to the change of offset voltage.

$$\text{PSRR (dc) (dB)} = 20 \cdot \log(\Delta V_{PS} / \Delta V_{OS}) \quad (6)$$

where:

- ΔV_{PS} = Change of power-supply voltage
- ΔV_{OS} = Change of offset voltage

For the measurement of PSRR (ac), the power-supply voltage is modulated by a 100mVpp ($35mV_{RMS}$) signal at various test frequencies. An FFT of the ADC data with power-supply modulation is performed. Equation 7 shows that the nine largest amplitude spurious frequencies in the frequency spectrum are summed as powers. These frequencies are then related to the amplitude of the power-supply modulation signal.

$$\text{PSRR (ac) (dB)} = 20 \cdot \log(V_{PS} / V_O) \quad (7)$$

where:

- V_{PS} (RMS) = 35mV ac power-supply modulation signal
- V_O (RMS) = Root-sum-square amplitude of spurious frequencies = $\sqrt{(V_0{}^2 + V_1{}^2 + ...V_8{}^2)}$

6.8 SNR Measurement

Signal-to-noise ratio (SNR) is a measure of noise performance with a full-scale ac input signal. For the SNR measurement, a –0.2dBFS, 1kHz test signal is used with V_{CM} equal to the mid-supply voltage. Equation 8 shows that SNR is the rms value ratio of the input signal to the root-sum-square of all other frequency components derived from the FFT result of the ADC output samples. DC and harmonics of the original signal are excluded from the SNR calculation. If an FFT window function is used because of non-coherent sampling, the spectral leakage bins surrounding the original signal are removed to calculate SNR.

$$\text{SNR (dB)} = 20 \cdot \log(V_{IN} / e_n) \quad (8)$$

where:

- V_{IN} = Input test signal
- e_n = Root-sum-square of frequency components excluding dc and signal harmonics

6.9 INL Error Measurement

Integral nonlinearity (INL) error specifies the linearity of the ADC dc transfer function. INL is measured by applying a series of dc test voltages over the ADC input range. INL is the difference between a set of dc test voltages [$V_{IN(N)}$] to the corresponding set of output voltages [$V_{OUT(N)}$] computed from the slope and offset transfer function of the ADC. Equation 9 shows the *end-point method* of calculating INL error.

$$\text{INL (LSB)} = \text{Maximum of test voltage series } [2^{16} \cdot |V_{IN(N)} - V_{OUT(N)}| / \text{FSR}] \quad (9)$$

where:

- N = Index of dc test voltage
- [$V_{IN(N)}$] = Set of test voltages over the –95% to 95% input range
- [$V_{OUT(N)}$] = Set of corresponding ADC output voltages
- FSR (full-scale range) = 2 · V_{REF} (1x input range) or 4 · V_{REF} (2x input range)

The INL *best-fit method* uses a least-squared error (LSE) calculation to determine a new straight line. This line minimizes the root-sum-square of the INL errors above and below the original end-point line.

6.10 THD Measurement

Total harmonic distortion (THD) specifies the dynamic linearity of the ADC with an ac input signal. For the THD measurement, a –0.2dBFS, 1kHz differential input signal with V_{CM} equal to the mid-supply voltage is applied. A sufficient number of data points are collected to yield an FFT result with frequency bin widths of 5Hz or less. The 5Hz bin width reduces the noise in the harmonic bins for consistent THD measurements. As shown in Equation 10, THD is calculated as the ratio of the root-sum-square amplitude of harmonics to the input signal amplitude.

$$\text{THD (dB)} = 20 \cdot \log(V_H / V_{IN}) \quad (10)$$

where:

- V_H = Root-sum-square of harmonics: $\sqrt{(V_2{}^2 + V_3{}^2 + \ldots V_n{}^2)}$, where V_n = The ninth harmonic voltage
- V_{IN} = Input signal fundamental

6.11 IMD Measurement

Intermodulation distortion (IMD) specifies the mixing effect of two input signals. Signal mixing is caused by ADC nonlinearity resulting in new sum and difference frequencies not contained in the original signal. The IMD second-order terms are ($f_1 + f_2$) and ($f_1 – f_2$). The IMD third-order terms are ($2f_1 + f_2$), ($2f_1 – f_2$), ($f_1 + 2f_2$), and ($f_1 – 2f_2$). Test signals f_1 = 9.7kHz and f_2 = 10.3kHz are at –6.5dBFS. Equation 11 shows the IMD calculation.

$$IMD_2\,(dB) = 20 \cdot \log(V_2 / V_{IN})$$
$$IMD_3\,(dB) = 20 \cdot \log(V_3 / V_{IN}) \quad (11)$$

where:

- IMD_2 = Second-order IMD
- IMD_3 = Third-order IMD
- V_2 = Root-sum-square of second-order terms
- V_3 = Root-sum-square of third-order terms
- V_{IN} = Sum amplitude of the input test signals

6.12 SFDR Measurement

Spurious-free dynamic range (SFDR) is the ratio of the rms value of a single-tone ac input to the highest spurious signal in the ADC frequency spectrum. SFDR measurement includes harmonics of the original signal. For the SFDR measurement, a –0.2dBFS, 1kHz input signal with V_{CM} equal to the mid-supply voltage is applied. As shown in Equation 12, SFDR is the ratio of the rms values of the input signal to the single highest spurious signal, including harmonics of the original signal.

$$SFDR\,(dB) = 20 \cdot \log(V_{IN} / V_{SPUR}) \quad (12)$$

where:

- V_{IN} = Input test signal
- V_{SPUR} = Single highest spurious level

6.13 Noise Performance

The ADCs offer four speed modes with programmable OSR allowing trade-offs between power consumption and bandwidth. The modes are max speed, high speed, mid speed, and low speed, with decreasing levels of device power consumption and signal bandwidth.

With the ADC inputs shorted, the output code is a single value or flickering codes between two or more values. Code flicker depends on the ADC noise for the selected OSR value and the dc signal relative to the next code transition. The ADC peak-to-peak noise value is typically 6.6 × the RMS noise value. Code flicker results when the amplitude of noise is large enough to trigger code transitions.

The quantization error of an ADC is ±0.5 LSB. For an ac signal, the quantization *error* becomes a quantization *noise*. Figure 6-1 shows the quantization error converting to noise (*LSB error plot*) as the signal changes. For non-coherent sampling, this quantization noise is approximated as *white* noise, spread evenly across the frequency band. For an N-bit ADC, the signal-to-*quantization* noise ratio (SQNR) is as follows: SQNR (dB) = 6.02 x N + 1.76. For a 16-bit ADC, SQNR is 98.1dB.

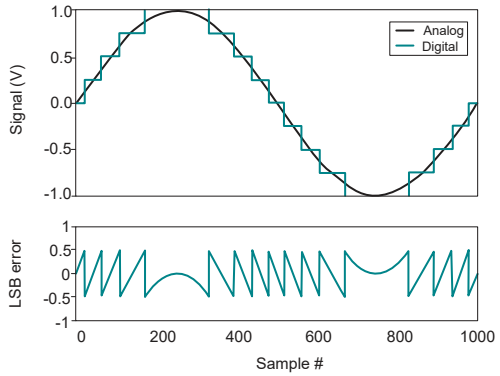


Figure 6-1. Quantization Noise of Sine Wave Input

Table 6-1 through Table 6-5 summarize noise performance. SNR values in the tables are calculated by the ratio of the RMS full scale range to the root-sum-square result of ADC thermal noise and 16-bit quantization noise. For this device, the value of quantization noise is typically greater than thermal noise, therefore SNR is limited to 98.1dB for large values of OSR.

Table 6-1. Wideband Filter Noise Performance (V_{REF} = 4.096V, 1x Input Range)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})	SNR (dB)
Max speed	32.768	32	512	10.9	97.7
High speed	25.6		400	10.8	97.7
Mid speed	12.8		200	10.5	97.8
Low speed	3.2		50	10.4	97.8
Max speed	32.768	64	256	7.48	97.9
High speed	25.6		200	7.33	97.9
Mid speed	12.8		100	7.21	97.9
Low speed	3.2		25	7.17	97.9
Max speed	32.768	128	128	5.17	98.0
High speed	25.6		100	5.14	98.0
Mid speed	12.8		50	5.02	98.0
Low speed	3.2		12.5	5.02	98.0

Table 6-1. Wideband Filter Noise Performance (V_{REF} = 4.096V, 1x Input Range) (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})	SNR (dB)
Max speed	32.768	256	64	3.64	98.1
High speed	25.6		50	3.59	98.1
Mid speed	12.8		25	3.55	98.1
Low speed	3.2		6.25	3.55	98.1
Max speed	32.768	512	32	2.56	98.1
High speed	25.6		25	2.55	98.1
Mid speed	12.8		12.5	2.49	98.1
Low speed	3.2		3.125	2.49	98.1
Max speed	32.768	1024	16	1.73	98.1
High speed	25.6		12.5	1.80	98.1
Mid speed	12.8		6.25	1.73	98.1
Low speed	3.2		1.5625	1.75	98.1
Max speed	32.768	2048	8	1.37	98.1
High speed	25.6		6.25	1.28	98.1
Mid speed	12.8		3.125	1.26	98.1
Low speed	3.2		0.78125	1.26	98.1
Max speed	32.768	4096	4	0.93	98.1
High speed	25.6		3.125	0.92	98.1
Mid speed	12.8		1.5625	0.90	98.1
Low speed	3.2		0.390625	0.89	98.1

Table 6-2. Sinc4 Filter Noise Performance (V_{REF} = 4.096V, 1x Input Range)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})	SNR (dB)
Max speed	32.768	12	1365.3	65.1	91.9
High speed	25.6		1066.6	66.1	91.8
Mid speed	12.8		533.3	65.3	91.9
Low speed	3.2		133.33	65.3	91.9
Max speed	32.768	16	1024	25.1	96.4
High speed	25.6		800	25.1	96.4
Mid speed	12.8		400	24.6	96.5
Low speed	3.2		100	24.7	96.5
Max speed	32.768	24	682.67	10.4	97.8
High speed	25.6		533.3	10.3	97.8
Mid speed	12.8		266.67	10.1	97.8
Low speed	3.2		66.67	10.1	97.8
Max speed	32.768	32	512	8.05	97.9
High speed	25.6		400	7.83	97.9
Mid speed	12.8		200	7.78	97.9
Low speed	3.2		50	7.76	97.9
Max speed	32.768	64	256	5.46	98.0
High speed	25.6		200	5.44	98.0
Mid speed	12.8		100	5.30	98.0
Low speed	3.2		25	5.30	98.0

Table 6-2. Sinc4 Filter Noise Performance (V_{REF} = 4.096V, 1x Input Range) (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})	SNR (dB)
Max speed	32.768	128	128	3.79	98.1
High speed	25.6		100	3.76	98.1
Mid speed	12.8		50	3.68	98.1
Low speed	3.2		12.5	3.62	98.1
Max speed	32.768	256	64	2.74	98.1
High speed	25.6		50	2.69	98.1
Mid speed	12.8		25	2.63	98.1
Low speed	3.2		6.25	2.62	98.1
Max speed	32.768	512	32	1.90	98.1
High speed	25.6		25	1.89	98.1
Mid speed	12.8		12.5	1.86	98.1
Low speed	3.2		3.125	1.84	98.1
Max speed	32.768	1024	16	1.34	98.1
High speed	25.6		12.5	1.34	98.1
Mid speed	12.8		6.25	1.33	98.1
Low speed	3.2		1.56	1.32	98.1
Max speed	32.768	2048	8	0.98	98.1
High speed	25.6		6.25	0.95	98.1
Mid speed	12.8		3.125	0.93	98.1
Low speed	3.2		0.78	0.92	98.1
Max speed	32.768	4096	4	0.70	98.1
High speed	25.6		3.125	0.69	98.1
Mid speed	12.8		1.563	0.66	98.1
Low speed	3.2		0.39	0.66	98.1

Table 6-3. Sinc4 + Sinc1 Filter Performance (V_{REF} = 4.096V, 1x Input Range)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n) (μV_{RMS})	SNR (dB)
Max speed	32.768	64	256	6.77	98.0
High speed	25.6		200	6.62	98.0
Mid speed	12.8		100	6.60	98.0
Low speed	3.2		25	6.50	98.0
Max speed	32.768	128	128	5.16	98.0
High speed	25.6		100	5.13	98.0
Mid speed	12.8		50	5.07	98.0
Low speed	3.2		12.5	5.02	98.0
Max speed	32.768	320	51.2	3.39	98.1
High speed	25.6		40	3.35	98.1
Mid speed	12.8		20	3.29	98.1
Low speed	3.2		5	3.28	98.1
Max speed	32.768	640	25.6	2.42	98.1
High speed	25.6		20	2.39	98.1
Mid speed	12.8		10	2.35	98.1
Low speed	3.2		2.5	2.36	98.1

Table 6-3. Sinc4 + Sinc1 Filter Performance (V_{REF} = 4.096V, 1x Input Range) (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n) (μV_{RMS})	SNR (dB)
Max speed	32.768	1280	12.8	1.74	98.1
High speed	25.6		10	1.73	98.1
Mid speed	12.8		5	1.69	98.1
Low speed	3.2		1.25	1.68	98.1
Max speed	32.768	3200	5.12	1.10	98.1
High speed	25.6		4	1.09	98.1
Mid speed	12.8		2	1.07	98.1
Low speed	3.2		0.5	1.07	98.1
Max speed	32.768	6400	2.56	0.79	98.1
High speed	25.6		2	0.78	98.1
Mid speed	12.8		1	0.77	98.1
Low speed	3.2		0.25	0.77	98.1
Max speed	32.768	12800	1.28	0.57	98.1
High speed	25.6		1	0.56	98.1
Mid speed	12.8		0.5	0.55	98.1
Low speed	3.2		0.125	0.54	98.1
Max speed	32.768	32000	0.512	0.37	98.1
High speed	25.6		0.4	0.37	98.1
Mid speed	12.8		0.2	0.37	98.1
Low speed	3.2		0.05	0.37	98.1

Table 6-4. Sinc3 Filter Performance (V_{REF} = 4.096V, 1x Input Range)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (SPS)	NOISE (e_n) (μV_{RMS})	SNR (dB)
Max speed	32.768	26667	614.4	0.32	98.1
High speed	25.6		480	0.32	98.1
Mid speed	12.8		240	0.32	98.1
Low speed	3.2		60	0.32	98.1
Max speed	32.768	32000	512	0.32	98.1
High speed	25.6		400	0.31	98.1
Mid speed	12.8		200	0.31	98.1
Low speed	3.2		50	0.31	98.1

Table 6-5. Sinc3 + Sinc1 Filter Performance (V_{REF} = 4.096V, 1x Input Range)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (SPS)	NOISE (e_n) (μV_{RMS})	SNR (dB)
Max speed	32.768	96000	170.6	0.25	98.1
High speed	25.6		133.3	0.25	98.1
Mid speed	12.8		66.6	0.25	98.1
Low speed	3.2		16.6	0.25	98.1
Max speed	32.768	160000	102.4	0.24	98.1
High speed	25.6		80	0.25	98.1
Mid speed	12.8		40	0.25	98.1
Low speed	3.2		10	0.25	98.1

7 Detailed Description

7.1 Overview

The ADS117L14 and ADS117L18 are quad and octal, 16-bit, simultaneous-sampling, delta-sigma (ΔΣ) analog-to-digital converters (ADCs). The devices offer an excellent combination of dc accuracy, ac resolution, and wide signal bandwidth for synchronized, multichannel data acquisition systems. The ADCs are optimized for wide signal bandwidths with low power consumption.

The *Functional Block Diagram* shows the device features. The devices consist of four or eight independent delta-sigma ADCs from which data is read through a frame-sync data port. Each ADC has programmable digital filters that provide sample rates up to 512kSPS in wideband filter mode and 1365.3kSPS in low-latency filter mode. Four selectable power-scalable speed modes allow optimization of signal bandwidth, SNR, and power consumption.

Signal and reference voltage input precharge buffers of each ADC channel reduce analog input current and sampling noise to allow the use of low bandwidth signal drivers. The VCM output is a buffered mid-supply voltage used to drive the common-mode voltage of external buffers and gain stages.

The multibit ΔΣ modulator measures the differential input signal, $V_{IN} = (V_{AINP} – V_{AINN})$, against the differential reference, $V_{REF} = (V_{REFP} – V_{REFN})$. The modulator produces low-resolution, high-frequency data. Noise shaping of the modulator shifts the quantization noise of the low-resolution data to an out-of-band frequency range where the digital filter removes this noise. The noise remaining within the pass band is low-level thermal noise. The digital filter decimates and filters the modulator data to provide the final output data.

The digital filter has two filter modes: low-latency filter (typically used for dc signal measurement) and wideband filter (typically used for ac signal measurement). The low-latency filter is a variable-order sinc filter with filter options for sinc4, sinc4 + sinc1, sinc3, and sinc3 + sinc1. This filter allows optimization between noise performance, conversion latency, and signal bandwidth. The wideband filter is a multi-stage, linear phase finite impulse response (FIR) filter. This filter provides outstanding frequency response characteristics with low pass-band ripple, narrow transition-band, and high stop-band attenuation. The devices allow power-of-2 related data rates between channels.

The MODE pin selects the method of device configuration: by hardware pin settings or by the SPI serial interface.

The frame-sync data port provides the conversion data using four or eight data lanes or time division multiplex (TDM) format to reduce the data lanes to two or one. Daisy-chain multiple devices by routing the DOUTx pins to the DINx pins of the chained devices.

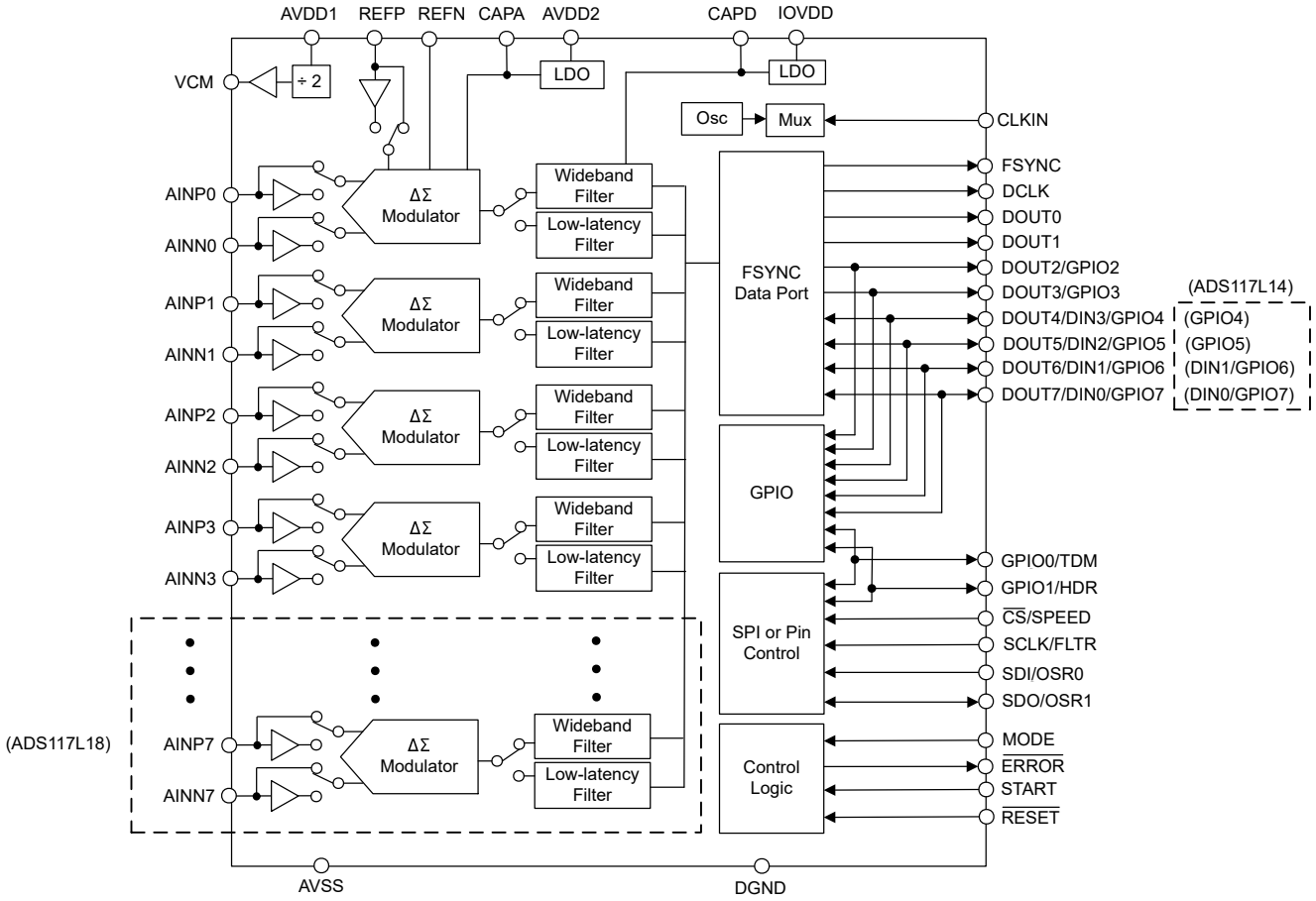
The device supports external clock operation for synchronized applications and internal oscillator operation for stand-alone applications. The START pin provides simultaneous synchronization of the ADC channels. The $\overline{\text{RESET}}$ pin resets the ADC.

Cyclic redundancy check (CRC) error detection is available for the frame-sync port and the SPI configuration port. The register map CRC operates in the background to detect unintended changes to the register values after the initial values are uploaded to the device. The open-drain $\overline{\text{ERROR}}$ output pin asserts low when an ADC error is detected.

Eight general-purpose input/output (GPIO) pins are available. Two GPIOs are standalone pins and the remaining six GPIO pins are multiplexed with the frame-sync DINx and DOUTx pins.

The AVDD1 supply voltage powers the precharge buffers and the input sampling switches. AVDD2 powers the modulators through an internal voltage regulator. The IOVDD supply voltage is the digital I/O voltage and also powers the digital cores through a second voltage regulator. The internal regulators reduce overall power consumption and maintain consistent levels of device performance under varying power supply conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs (AINP, AINN)

The analog inputs of the ADC channels are differential, with the input defined as a difference voltage: $V_{IN} = V_{AINP} – V_{AINN}$. For best performance, drive the input with a differential signal with the common-mode voltage centered to mid-supply (AVDD1 + AVSS) / 2. Tie unused inputs to ground or a dc voltage within the AVSS to AVDD1 power supply range.

The ADC accepts either unipolar or bipolar input signals by configuring the AVDD1 and AVSS power supplies accordingly. Figure 7-1 illustrates an example of a differential signal in unipolar supply configuration. Symmetric input voltage headroom is provided when the common-mode voltage is equal to mid-supply (AVDD1 / 2). For unipolar operation, use AVDD1 = 5V and AVSS = 0V (mid- and low-speed modes offer the option of reduced AVDD1 supply voltage). The VCM pin provides a buffered common-mode voltage to level-shift the signal voltage in the external driver stage.

Figure 7-2 illustrates an example of a differential signal in bipolar supply configuration. The common-mode voltage of the signal is normally 0V. For bipolar operation, use AVDD1 and AVSS = ±2.5V (mid- and low-speed modes offer the option of reduced AVDD1 – AVSS supply voltage).

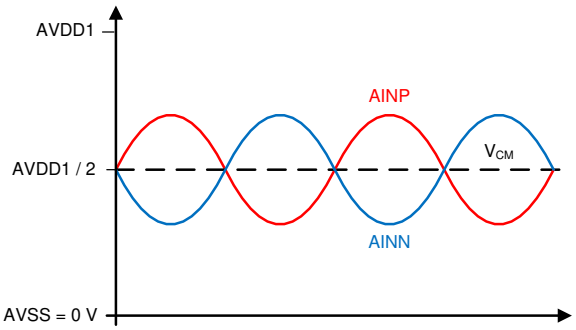


Figure 7-1. Unipolar Differential Input Signal

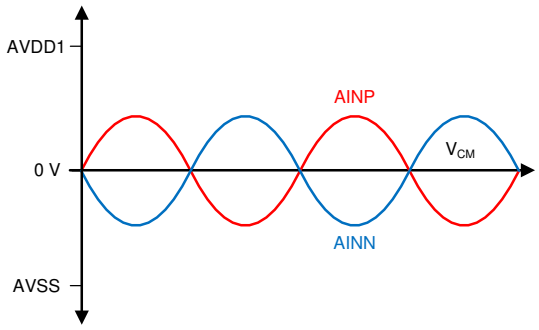


Figure 7-2. Bipolar Differential Input Signal

In both bipolar and unipolar configurations, the ADC accepts single-ended input signals by tying the AINN input to AVSS, ground, or to mid-supply. However, because AINN is a fixed voltage, the full differential input swing range is not obtained. Thus, the ADC dynamic range is limited to the voltage swing of the AINP input (±2.5V or 0V to 5V for a 5V supply).

The circuit of Figure 7-3 shows the simplified analog input circuit of the ADC channels. Diodes protect the analog inputs from electrostatic discharge (ESD) events that occur during the manufacturing process and during printed circuit board (PCB) assembly when manufactured in an ESD-controlled environment. If the inputs are driven below AVSS – 0.3 V, or above AVDD1 + 0.3 V, the protection diodes potentially conduct. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to the value shown in the Absolute Maximum Ratings section.

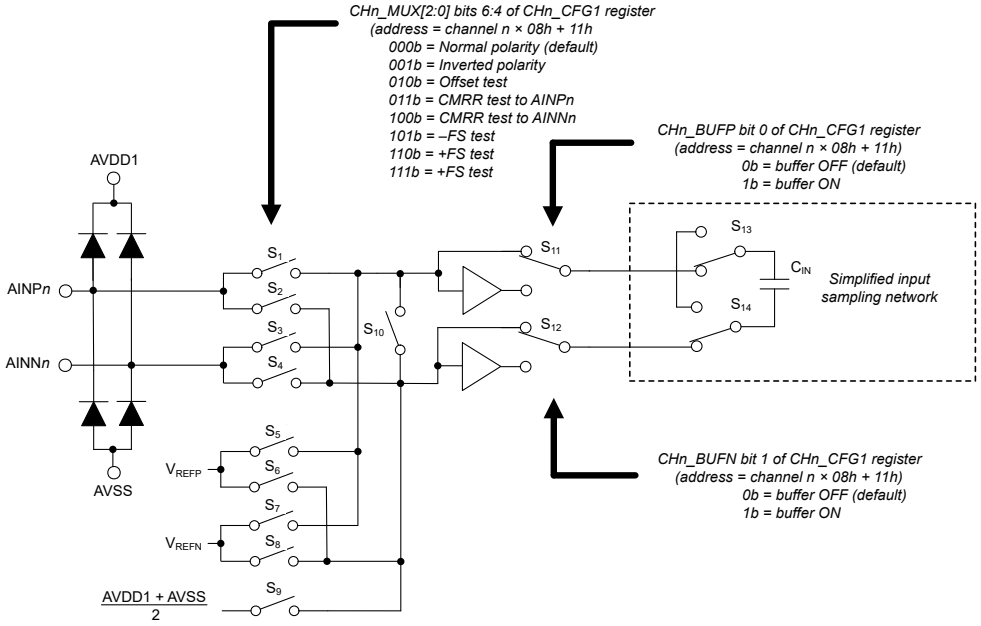


Figure 7-3. Analog Input Circuit

The input multiplexers of the ADC channels are independently configurable. The multiplexer offers the option of normal or reverse signal polarities and internal test modes. The test modes are used for ADC performance testing and diagnostics. The input-short test mode verifies noise and offset errors by shorting the inputs to mid-supply voltage. Full-scale range is tested by selecting the +FS or –FS connection. To avoid clipped output codes during evaluation, reduce the value of the gain registers or program the ADC to the extended range mode. The CMRR test mode verifies CMRR performance by shorting the inputs together and the user applying a dc

or ac test signal to the AINPn or AINNn input. The resulting data is analyzed by the user to determines CMRR performance. Enable the input precharge buffers for best accuracy when using the test modes.

Table 7-1 shows the switch configurations of the input multiplexer circuit of Figure 7-3.

Table 7-1. Input Multiplexer Configurations

CH*n*_MUX[2:0] BITS	CLOSED SWITCHES	DESCRIPTION
000b	S_1, S_4	Normal polarity input
001b	S_2, S_3	Reverse polarity input
010b	S_9, S_{10}	Input short for offset voltage and noise test
011b	S_1, S_{10}	Input short with user applied signal to AINP*n* for CMRR test
100b	S_4, S_{10}	Input short with user applied signal to AINN*n* for CMRR test
101b	S_6, S_7	–FS dc signal for gain test
110b	S_5, S_8	+FS dc signal for gain test
111b	S_5, S_8	+FS dc signal for gain test

The input sampling capacitor C_{IN} is part of the simplified input sampling network denoted in the dashed box of Figure 7-3. The instantaneous charge demand of C_{IN} requires the signal to settle within a half cycle of the modulator frequency $t = 1 / (2 \cdot f_{MOD})$. To satisfy this requirement, the driver bandwidth is typically much larger than the original signal frequency. The bandwidth of the driver is determined as sufficient when the THD and SNR data sheet performance are achieved. Because the modulator sampling rate is eight times slower in low-speed mode compared to high-speed mode, more time is available for driver settling.

The charge required by the input sampling capacitor is modeled as an average input current of the ADC inputs. As shown in Equation 13 and Equation 14, the input current is comprised of differential and absolute components.

$$\text{Input Current (Differential Input Voltage)} = f_{MOD} \cdot C_{IN} \cdot 10^6 \ (\mu A/V) \quad (13)$$

where:

- $f_{MOD} = f_{CLK} / 2$
- C_{IN} = 7.4pF (1x input range), 3.6pF (2x input range)

$$\text{Input Current (Absolute Input Voltage)} = f_{MOD} \cdot C_{CM} \cdot 10^6 \ (\mu A/V) \quad (14)$$

where:

- $f_{MOD} = f_{CLK} / 2$
- C_{CM} = 0.35pF (1x input range), 0.17pF (2x input range)

For f_{MOD} = 12.8MHz (high-speed mode), C_{IN} = 7.4pF and C_{CM} = 0.3pF, the input current resulting from the differential voltage is 95µA/V and the input current resulting from the absolute voltage is 4.5µA/V. For example, if AINP*n* = 4.5V and AINN*n* = 0.5 , then V_{IN} = 4V. The total AINP*n* input current = (4V · 95µA/V) + (4.5V · 4.5µA/V) = 400µA. The total AINN*n* current is (–4V · 95µA/V) + (0.5 · 4.5µA/V) = –378µA.

The device incorporates input precharge buffers to significantly reduce the charge required by capacitor C_{IN}. In operation, the precharge buffers provide the charging current. Near the end of the sampling phase, capacitor C_{IN} is nearly fully charged. The buffers are disconnected (S_{11} and S_{12} of Figure 7-3 in up positions) to allow the external driver to provide the fine charge to the capacitor. When the sample phase is completed, the sampling capacitor is discharged to complete the cycle, at which time the sample process repeats. The operation of the precharge buffers reduces the input current by more than 99%, and in many cases leads to improved THD and SNR performance. The precharge buffers are enabled by the CH*n*_BUFP and CH*n*_BUFN bits of the CHn_CFG1 register. If the AINN input of any channel is tied to ground or to a low-impedance source, disable the AINN buffer to reduce power consumption. A single-ended input application is an example of a low-impedance source.

7.3.1.1 Input Range

The input range of the ADC is programmable, defined as $V_{IN} = \pm V_{REF}$ or as $V_{IN} = \pm 2V_{REF}$. The $\pm 2V_{REF}$ input range doubles the usable input range when using a 2.5V reference voltage. The $\pm 2V_{REF}$ input range typically improves dynamic range by +1dB. However, the inputs are required to be driven to the AVDD1 and AVSS supply rails to achieve full dynamic range (with a 2.5V reference voltage). Compared to operation with a 2.5V reference voltage, dynamic range performance improves by using 4.096V (+4dB) or 5V (+6dB) reference voltages. The $\pm 2V_{REF}$ range selection is internally forced to the $\pm V_{REF}$ range when the high-reference range is selected (used for 4.096V or 5V reference voltages). See the CH*n*_INP_RNG bits of the CH*n*_CFG1 registers to program the input range.

In some ADC configurations, the available input range exceeds the power supply voltage. An example is when using a 3V AVDD1 power supply with a 2.5V reference voltage in the $\pm 2V_{REF}$ mode. In this case, the full $\pm 2V_{REF}$ input range is not available.

The ADC channels have the option to extend the input range by 25%. This mode provides additional headroom for the signal. Output data are scaled such that the positive and negative full-scale output codes (7FFFFFh and 800000h) occur at:

$$V_{IN} = \pm 1.25 \times k \times V_{REF} \quad (15)$$

where:

- k = 1 or 2, depending on the $\pm V_{REF}$ or $\pm 2V_{REF}$ range selection

See the CH*n*_CFG1 register to program the extended range option.

When the signal exceeds 110% of normal full-scale range in the extended range mode, the ADC provides valid conversion results, but SNR performance degrades due to modulator saturation. The MOD_FLAG bit of the frame-sync STATUS byte indicates when modulator saturation is occurring. See the Frame-Sync STATUS byte for details. Figure 7-4 shows SNR performance versus input amplitude in the extended range mode.

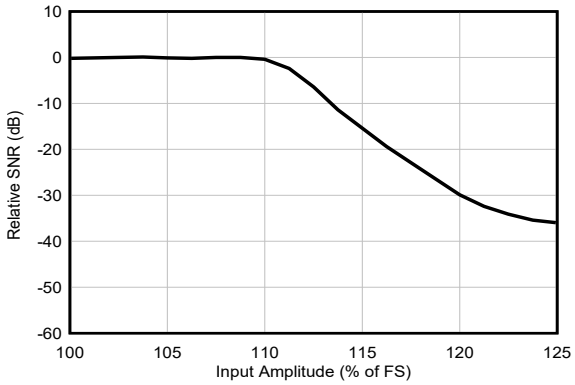


Figure 7-4. Extended Range SNR Performance

7.3.2 Reference Voltage (REFP, REFN)

A reference voltage is required for operation. The reference voltage input is differential, defined as: $V_{REF} = V_{REFP} - V_{REFN}$, and is applied to the REFP and REFN inputs for all channels. See the *Reference Voltage Range* section for details of the reference voltage operating range.

As shown in Figure 7-5, the reference input sampling structure is similar to the analog input structure. ESD diodes protect the reference inputs and turn on when the reference pin voltage thresholds are exceeded. To keep these diodes off, make sure the reference pin voltages do not go below AVSS by more than 0.3V or above AVDD1 by 0.3V. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to the specified value.

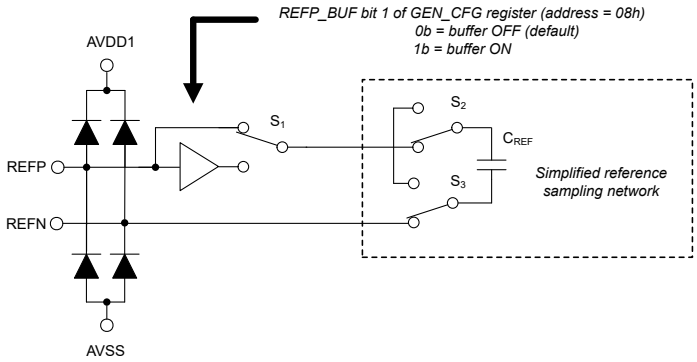


Figure 7-5. Reference Input Circuit

The reference voltage is sampled by a sampling capacitor C_{REF}. In unbuffered mode, current flows through the reference inputs to charge the sampling capacitor. The current consists of a dc component and an ac component that varies with the frequency of the modulator sampling clock. See the *Section 5.5* table for the reference input current specification.

Charging the reference sampling capacitor requires the external reference driver to settle at the end of the sample phase $t = 1 / (2 \cdot f_{MOD})$. Incomplete settling of the reference voltage increases gain error and gain error drift. Operation in the lower speed mode reduces the modulator sampling clock frequency, therefore allowing more time for the reference driver to settle.

A precharge buffer option is available for the REFP input to reduce the charge drawn by the sampling capacitor. The precharge buffer provides the coarse charge for the reference sampling capacitor C_{REF}. Halfway through the sample phase, the precharge buffer is bypassed (S_1 is in an up position as demonstrated in Figure 7-5). At this time, the external driver provides the fine charge to the sampling capacitor. Because the buffer reduces the charge demand of the sampling capacitor, the bandwidth requirement of the external driver is greatly reduced.

The sampling current flowing through the REFN input is not reduced by the REFP buffer. Because many applications ground REFN, or connect REFN to AVSS, a precharge buffer for REFN is not necessary. For applications when REFN is not low-impedance, buffer the REFN input.

7.3.2.1 Reference Voltage Range

Optimize the ADC performance by selecting a reference voltage range: low-reference range or high-reference range. Program the range to match the reference voltage, such as 2.5V or 4.096V. The low range accepts voltages from 0.5V to 2.75V, and the high range accepts voltages 1V to AVDD1 – AVSS. For cases where the ranges overlap, such as 2.5V, use the low-reference range for best performance. Program the REF_RNG bit of the GEN_CFG1 register to select the reference voltage range. When the high-reference range is selected, the input range is forced to $V_{IN} = \pm V_{REF}$.

7.3.3 Clock Operation

Figure 7-6 shows the clock diagram. The input clock multiplexer selects the external clock signal of the CLKIN pin or the internal clock oscillator signal. The signal is routed to all ADC channels. The clock dividers program the main ADC clock frequency (f_{CLK}) and the frequency of the frame-sync port DCLK signal (f_{DCLK}). f_{CLK} is divided by 2 to derive the modulator sampling clock frequency (f_{MOD}). f_{CLK} is also divided by 32 to drive a free-running counter for clock signal diagnostics (CLK_CNT register).

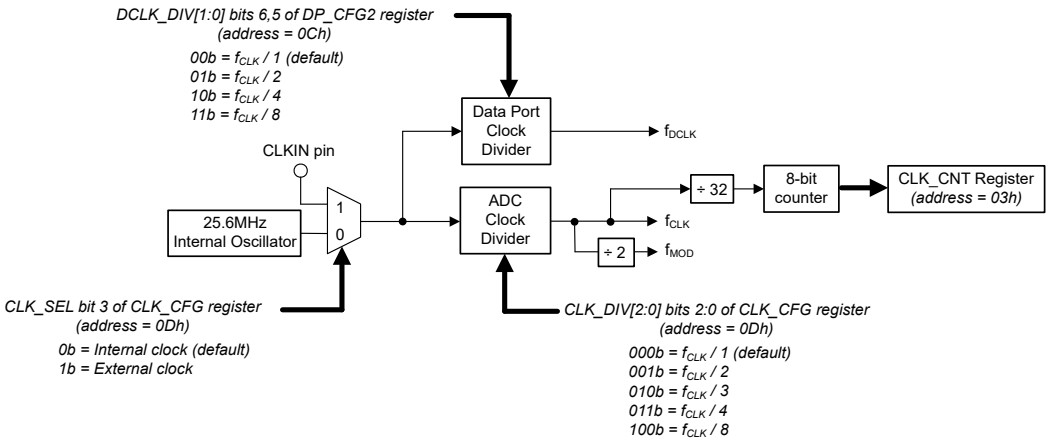


Figure 7-6. Clock Block Diagram

The speed modes determine the maximum allowable clock frequency. See the Speed Modes section for the clock frequencies of each speed mode.

7.3.3.1 Clock Dividers

The ADC provides two clock dividers, one divider for the ADC clock and one divider for the DCLK signal of the frame-sync port.

The ADC clock frequency is divided by 1, 2, 3, 4 or 8 using the CLK_DIV[2:0] bits. For clock divider values > 1, ADC synchronization has uncertainty due to the unknown phase of the divided clock signal. However, the ADC channels within the device are synchronized together. To avoid synchronization uncertainty, use the divide by 1 option. In addition, daisy chain operation of the frame-sync port requires the divide by1 option.

The DCLK frequency is divided by 1, 2, 4, or 8 using the DCLK_DIV[1:0] bits. DCLK can be operated faster compared to the ADC clock to support high rates of data transfer.

7.3.3.2 Internal Oscillator

The ADC provides an internal oscillator for ADC operation. Because of the clock jitter, the internal oscillator is recommended only for measurement of dc signals. Use an external clock for measurement of ac signals, when the devices are daisy-chained or when synchronization to a system clock is important. In SPI mode, default operation is the internal oscillator and is changed to external clock by setting the CLK_SEL bit = 1b. In the hardware programming mode, external clock operation is the default. Because the internal oscillator is 25.6MHz fixed frequency, program the ADC clock divider to set the ADC frequency according to the speed mode.

When changing the clock mode from an external clock to the internal oscillator, maintain the external clock after changing the clock mode. Maintain the clock mode for at least four cycles after the SPI register write command that changed the clock mode. After the clock mode change, the ADC ignores the control inputs (the START and RESET pins) for a period of 150µs. This time period allows the internal oscillator to stabilize.

7.3.3.3 External Clock

The ADC provides external clock operation. To select external clock operation in SPI programming mode, set the CLK_SEL bit to 1 and apply the clock signal to the CLKIN pin. In the hardware programming mode, only external clock operation is possible.

If desired, decrease the clock frequency from nominal specified frequency to yield specific data rates between the available OSR values. When doing so, the conversion noise at the reduced data rate is the same as the original frequency. Reduction of conversion noise is only possible by increasing the digital filter OSR value or changing the speed or filter modes.

Clock jitter causes timing variations of the modulator sampling that results in degraded SNR performance. Use a low-jitter clock to meet data sheet SNR performance. For example, for a 100kHz signal frequency, up to 50ps (rms) clock jitter is tolerated before SNR degrades. Many types of RC oscillators exhibit high levels of jitter to be

avoided for ac signal measurement. Instead, use a crystal oscillator or an integrated circuit clock source. Reduce ringing at the clock input by placing a series resistor at the output of the clock buffer driving the ADC.

7.3.4 Power-On Reset (POR)

The ADC uses power-supply monitors to detect power-on and brownout events. Power-on or power-cycling the IOVDD supply results in device reset. Power-on or power-cycling the analog power supplies does not result in device reset.

Figure 7-7 shows the IOVDD and regulated CAPD power-on voltage thresholds. When the voltages exceed the thresholds, the ADC is released from reset after a time delay of $t_{d(RSSC)}$. If the START pin is high, the ADC starts the conversion process and supplies data to the data port. The POR_FLAG bit of the SPI STATUS register and the PWR_FLAG of the data port header byte indicate device POR. Although not necessary for operation, write 1b to the POR_FLAG bit to clear the flag to detect the next POR event. The PWR_FLAG of the data port status byte remains disabled in hardware programming mode.

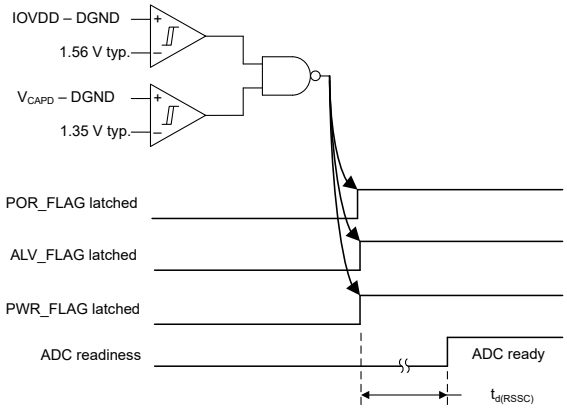


Figure 7-7. Digital Supply Threshold

Figure 7-8 shows the analog power supply power-on thresholds. Four monitors are used for four supply conditions (AVDD1 – DGND), (AVDD1 – AVSS), (AVDD2 – AVSS), and the regulated CAPA voltage (CAPA – AVSS). The ALV_FLAG bit (SPI STATUS register) and the PWR_FLAG (data port header byte) latch to 1b when the analog supply voltages are below the threshold values. Although not necessary for operation, write 1b to the ALV_FLAG bit to clear the flag to detect the next analog supply low-voltage condition. Power cycling the analog power supplies does not reset the ADC. Because a low voltage on the IOVDD supply resets the internal analog LDO (CAPA), the analog low-voltage flag (ALV_FLAG) is also set. The PWR_FLAG of the data port status byte is disabled when the device is operated in the hardware programming mode.

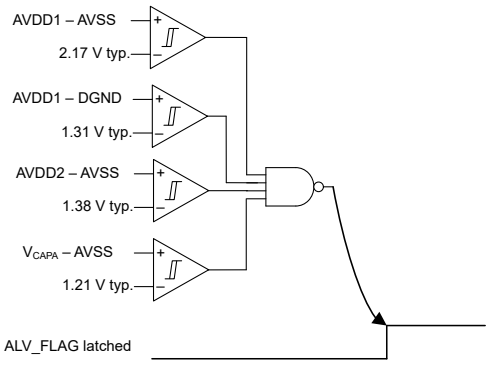


Figure 7-8. Analog Supply Threshold

7.3.5 VCM Output Voltage

The VCM pin is a buffered dc output voltage equal to the mid-point of AVDD1 and AVSS. The VCM output is a voltage to level-shift the signal, commonly used as the VCM input for a fully differential amplifier (FDA). The VCM output is enabled by the VCM bit of the GEN_CFG1 register. If VCM is not used, leave the pin unconnected and disabled.

7.3.6 GPIO

The ADC provides eight general-purpose, digital input/output (GPIO) pins. The GPIO voltage levels are IOVDD and DGND. Figure 7-9 shows the GPIO block diagram.

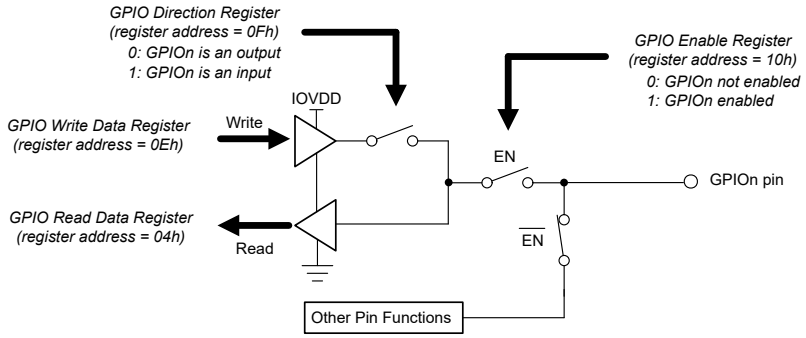


Figure 7-9. GPIO Block Diagram

The GPIO pins are enabled by the GPIO EN register and are programmable as inputs or outputs by the GPIO DIR register. The GPIO pins are read by the GPIO RD register and written by the GPIO WR register. When programmed as an output, a GPIO read register operation returns the value of the GPIO *pin* voltage. The GPIO pins are multiplexed with other functions, and when GPIO is enabled, have highest priority over other functions. As with all digital inputs, do not let the GPIO pins float when configured as inputs. Figure 7-10 shows the GPIO pin locations.

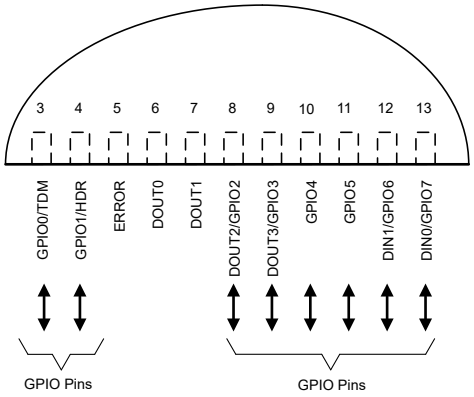


Figure 7-10. GPIO Pins (ADS117L14 pins shown)

7.3.7 Modulator

The modulator is a switched-capacitor, third-order architecture achieving excellent noise and linearity performance with low power consumption. As with most modulators, when overranged with a high amplitude signal or with an out-of-band signal, modulator saturation potentially occurs. When saturated, the in-band signal still converts, however the noise floor increases. Figure 7-11 illustrates the amplitude limit for out-of-band signals to avoid modulator saturation and increased noise. The amplitude limit for dc and in-band signals is 1dB above full-scale range.

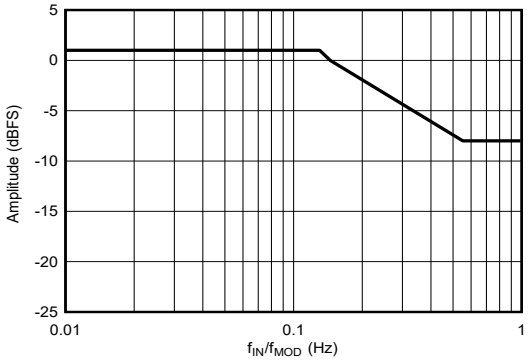


Figure 7-11. Amplitude Limit to Avoid Modulator Saturation

Modulator saturation is reported by the MOD_FLAG bit of the data port status header of each channel. The saturation status is latched during the conversion period and updated for each new conversion. Use an analog filter at the ADC inputs to filter the out-of-band signals to prevent increased noise. The *Typical Application* section shows an example of a fourth-order bandwidth limiting anti-alias filter.

7.3.8 Digital Filter

The digital filter bandwidth-limits (filters) and decimates (data rate reduction) the modulator low-resolution data to yield high-resolution, lower-speed ADC output data. The oversampling ratio (OSR) determines the amount of filtering and decimation that affects signal bandwidth, in-band noise, and ADC output data rate. The ADC output data rate is defined by: $f_{DATA} = f_{MOD} / OSR$.

The ADC provides two filter types: a wideband filter and a low-latency filter. The filters optimize the frequency characteristics (wideband filter - flat passband) or the time-domain characteristics (low-latency filter - fast response time). All ADC channels must be the same filter type, however different data rates are allowed as long as the data rates are in ratios of 2^x, where x = 0, 1, 2, 3, and so on. The filter type is programmable by the CH*n*_CFG2 registers, where *n* = channel number.

7.3.8.1 Wideband Filter

The wideband filter is a multistage FIR design featuring linear phase response, flat pass-band amplitude, narrow transition band, and high stop-band attenuation. Because of these characteristics, it is the recommended filter for measuring ac signals. The ADC provides eight programmable OSR values and four speed modes, offering a range of data rate, bandwidth and resolution options.

Figure 7-12 through Figure 7-16 illustrate the frequency response of the wideband filter. Figure 7-12 shows details of the pass-band ripple. Figure 7-13 shows the frequency response at the transition band.

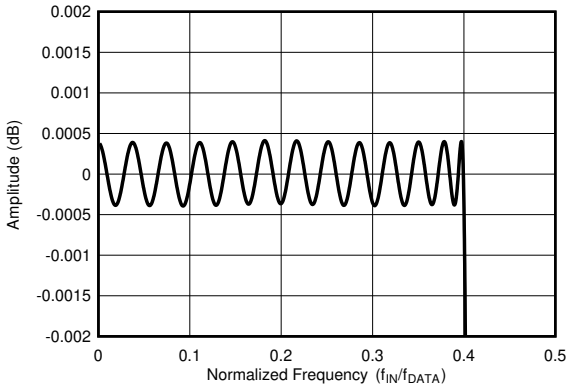


Figure 7-12. Wideband Filter Pass-Band Ripple

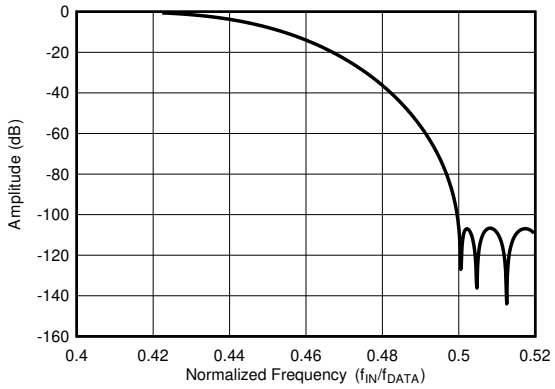


Figure 7-13. Wideband Filter Transition Band

Figure 7-14 shows the frequency response to f_{DATA} for OSR ≥ 64. The stop band begins at f_{DATA} / 2 to prevent aliasing at the Nyquist frequency. Figure 7-15 shows the stop-band attenuation to f_{MOD} for OSR = 32. In the stop-band region, out-of-band input frequencies mix with multiples of the f_{MOD} / 32 chop frequency. This process creates a pattern of stop-band response peaks that exceed the attenuation provided by the digital filter. The width of the response peaks is twice the filter bandwidth. Stop-band attenuation is improved when used in conjunction with an anti-alias filter at the ADC input.

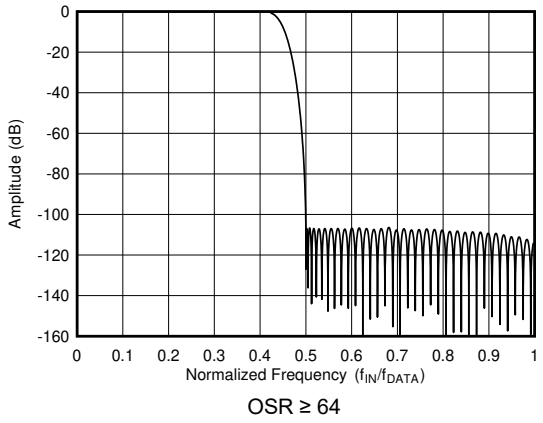


Figure 7-14. Wideband Filter Frequency Response

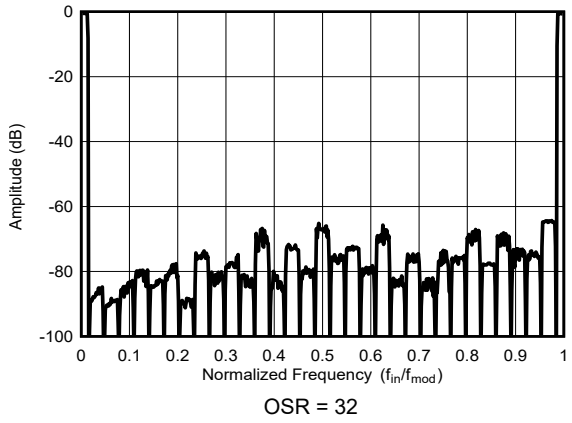


Figure 7-15. Wideband Filter Stop-Band

Figure 7-16 shows the filter response centered at f_{MOD}, where the filter response repeats. If not removed by an anti-alias filter, input frequencies at f_{MOD} appear as aliased frequencies in the pass band. Aliasing also occurs by input frequencies occurring at multiples of f_{MOD}. These frequency bands are defined by:

$$\text{Alias frequency bands: } (N \cdot f_{MOD}) \pm f_{BW} \tag{16}$$

where:

- N = 1, 2, 3, and so on
- f_{MOD} = Modulator sampling frequency
- f_{BW} = Filter bandwidth

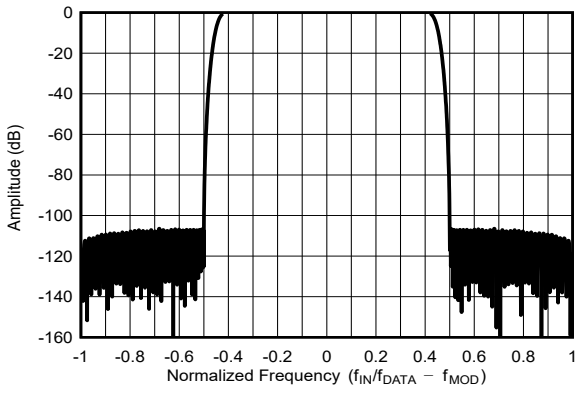


Figure 7-16. Wideband Filter Frequency Response Centered at f_{MOD}

The group delay of the filter is the time for a signal to propagate from the input to the output of the filter. Because the filter is a linear-phase design, the envelope of a multifrequency complex signal is undistorted by

filter processing. The group delay (expressed in units of time) is constant versus signal frequency and is equal to 34 / f_{DATA}. Be aware that after a step input is applied to the ADC inputs, fully settled data occurs 68 data periods later. Figure 7-17 shows the filter group delay (34 / f_{DATA}) and the settling time for a step input (68 / f_{DATA}).

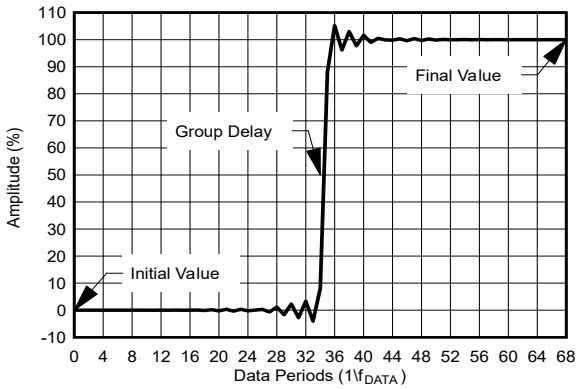


Figure 7-17. Wideband Filter Step Response

The digital filter restarts when the ADC is synchronized. After synchronization, the filter discards the next 68 conversions to account for filter settling time. The *Latency Time* column of Table 7-2 lists the time for the first conversion to appear on the frame-sync port after synchronization. The latency time includes an initial overhead time for filter reset. The first data is fully settled data. If a step input occurs while continuously converting, then the next 69 conversions are partially settled data.

Table 7-2. Wideband Filter Characteristics

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	–0.1dB FREQUENCY (kHz)	–3dB FREQUENCY (kHz)	LATENCY TIME[1] (µs)
Max speed	32.768	32	512	211.2	223.9	134.2
High speed	25.6		400	165	174.96	171.8
Mid speed	12.8		200	82.5	87.48	343.5
Low speed	3.2		50	20.63	21.87	1374
Max speed	32.768	64	256	105.6	112.0	267.0
High speed	25.6		200	82.5	87.48	341.8
Mid speed	12.8		100	41.25	43.74	683.5
Low speed	3.2		25	10.31	10.94	2734
Max speed	32.768	128	128	52.8	55.99	532.0
High speed	25.6		100	41.25	43.74	681.0
Mid speed	12.8		50	20.63	21.87	1362
Low speed	3.2		12.5	5.1562	5.468	5448
Max speed	32.768	256	64	26.4	28.00	1064
High speed	25.6		50	20.625	21.87	1362
Mid speed	12.8		25	10.31	10.93	2724
Low speed	3.2		6.25	2.578	2.734	10895
Max speed	32.768	512	32	13.2	14.00	2126
High speed	25.6		25	10.312	10.935	2721
Mid speed	12.8		12.5	5.156	5.467	5443
Low speed	3.2		3.125	1.289	1.367	21770

Table 7-2. Wideband Filter Characteristics (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	–0.1dB FREQUENCY (kHz)	–3dB FREQUENCY (kHz)	LATENCY TIME[1] (µs)
Max speed	32.768	1024	16	6.6	7.998	4251
High speed	25.6		12.5	5.156	5.467	5441
Mid speed	12.8		6.25	2.578	2.734	10883
Low speed	3.2		1.5625	0.645	0.6834	43530
Max speed	32.768	2048	8	3.3	3.499	8501
High speed	25.6		6.25	2.578	2.734	10881
Mid speed	12.8		3.125	1.289	1.367	21762
Low speed	3.2		0.78125	0.322	0.3417	87050
Max speed	32.768	4096	4	1.65	1.750	17001
High speed	25.6		3.125	1.289	1.367	21761
Mid speed	12.8		1.5625	0.645	0.6834	43522
Low speed	3.2		0.390625	0.161	0.1709	174090

(1) Latency time increases by 8 / f_{CLK} (µs) when the analog input buffers are enabled.

7.3.8.2 Low-Latency Filter (Sinc)

The low-latency filter is a cascaded-integrator-comb (CIC) topology with the main attribute of minimal delay (latency) as the input data propagates through the filter. The CIC filter is also known as a sinc filter because of the characteristic sinx/x (sinc) frequency response. The device offers the choice of four sinc filter configurations: sinc4, sinc4 + sinc1, sinc3, and sinc3 + sinc1. These configurations provide trade-offs of acquisition time, noise performance, and line-cycle rejection.

Latency time is measured from the time of device synchronization to the rising edge of FSYNC, at which time settled data are first available. The latency time is short compared to the wideband filter, making the filter useful for fast acquisition of dc signals. There is no need to discard data after synchronization because the data are settled. Detailed latency data for each sinc filter mode are given in Sinc4 Filter through Sinc3 + Sinc1 Filter sections.

If the input signal changes while continuously converting, then the next several conversions are partially settled. The number of conversions required for fully settled data is determined by rounding the latency time value to the next whole number of conversion periods.

Equation 17 shows the general expression of the sinc-filter frequency response. For single-stage sinc filter options (for example, the single-stage sinc3 or sinc4 filter), the second stage is not used.

$$\left|H_{(f)}\right| = \left| \frac{\sin\left[\frac{A\pi f}{f_{MOD}}\right]}{A\sin\left[\frac{\pi f}{f_{MOD}}\right]} \right|^{n} \cdot \left| \frac{\sin\left[\frac{AB\pi f}{f_{MOD}}\right]}{B\sin\left[\frac{A\pi f}{f_{MOD}}\right]} \right| \quad (17)$$

where:

- n = Stage 1 filter order (3 or 4)
- f = Signal frequency
- A = Stage 1 OSR
- B = Stage 2 OSR
- $f_{MOD} = f_{CLK} / 2$

7.3.8.2.1 Sinc4 Filter

The sinc4 filter performs averaging and decimation of the modulator data to produce data rates up to 1365.3kSPS in max-speed mode, 1066.6kSPS in high-speed mode, 533.3kSPS in mid-speed mode and 133.333kSPS in low-speed mode. Increasing the OSR value decreases the ADC data rate that reduces signal bandwidth and total noise resulting from increased data averaging and decimation.

Table 7-3 lists the sinc4 filter characteristics.

Table 7-3. Sinc4 Filter Characteristics

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	–3dB FREQUENCY (kHz)	LATENCY TIME (µs)[1]
Max speed	32.768	12	1365.3	310.2	3.9
High speed	25.6		1066.6	242.3	5.1
Mid speed	12.8		533.3	121.2	10.1
Low speed	3.2		133.33	30.3	40.5
Max speed	32.768	16	1024	232.7	4.9
High speed	25.6		800	181.8	6.3
Mid speed	12.8		400	90.9	12.6
Low speed	3.2		100	22.7	50.5
Max speed	32.768	24	682.67	155.1	6.9
High speed	25.6		533.3	121.2	8.9
Mid speed	12.8		266.67	60.6	17.1
Low speed	3.2		66.67	15.1	70.8
Max speed	32.768	32	512	116.3	8.9
High speed	25.6		400	90.9	11.4
Mid speed	12.8		200	45.4	22.8
Low speed	3.2		50	11.4	91.4
Max speed	32.768	64	256	58.2	16.6
High speed	25.6		200	45.4	21.3
Mid speed	12.8		100	22.7	42.6
Low speed	3.2		25	5.68	171
Max speed	32.768	128	128	29.1	32.3
High speed	25.6		100	22.7	41.3
Mid speed	12.8		50	11.4	82.6
Low speed	3.2		12.5	2.84	331
Max speed	32.768	256	64	14.5	63.6
High speed	25.6		50	11.4	81.4
Mid speed	12.8		25	5.68	163
Low speed	3.2		6.25	1.42	651
Max speed	32.768	512	32	7.27	126
High speed	25.6		25	5.68	162
Mid speed	12.8		12.5	2.84	324
Low speed	3.2		3.125	0.710	1294
Max speed	32.768	1024	16	3.64	251
High speed	25.6		12.5	2.84	321
Mid speed	12.8		6.25	1.42	643
Low speed	3.2		1.5625	0.355	2570

Table 7-3. Sinc4 Filter Characteristics (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	–3dB FREQUENCY (kHz)	LATENCY TIME (µs)(1)
Max speed	32.768	2048	8	1.82	501
High speed	25.6		6.25	1.42	641
Mid speed	12.8		3.125	0.710	1282
Low speed	3.2		0.7813	0.178	5130
Max speed	32.768	4096	4	0.909	1001
High speed	25.6		3.125	0.710	1281
Mid speed	12.8		1.563	0.355	2562
Low speed	3.2		0.391	0.089	10250

(1) Latency time increases by 8 / f_{CLK} (µs) when the analog input buffers are enabled.

Figure 7-18 and Figure 7-19 show the sinc4 frequency response for OSR = 32. The frequency response consists of a series of response nulls occurring at multiples of f_{DATA} with a series of decaying peaks in between. At the null frequencies, the filter has zero gain. A folded image of the filter response appears when f_{IN}/f_{DATA} > OSR/2, as illustrated in the frequency plot of Figure 7-19 for OSR = 32. 0dB attenuation occurs at input frequencies near n × f_{MOD} (n = 1, 2, 3, and so on). If signals are present at these frequencies, the signal is aliased to the pass band.

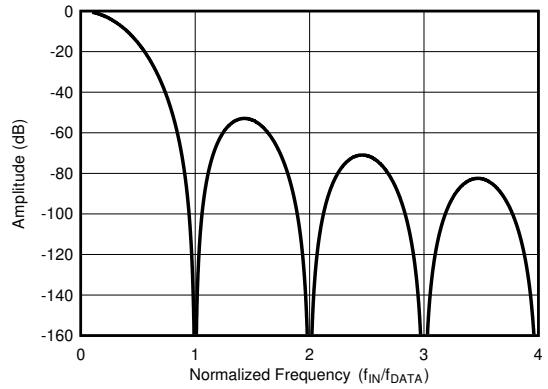


Figure 7-18. Sinc4 Frequency Response (OSR = 32)

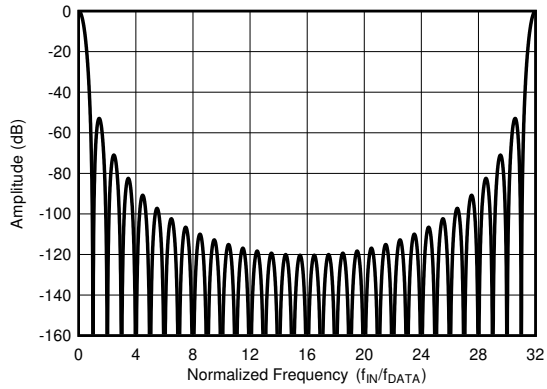


Figure 7-19. Sinc4 Frequency Response to f_{MOD} (OSR = 32)

7.3.8.2.2 Sinc4 + Sinc1 Cascade Filter

The sinc4 + sinc1 filter is the cascade of the sinc4 filter and a sinc1 filters. The fixed OSR of the sinc4 stage (OSR = 32) multiplied by the OSR of the sinc1 stage determines the ADC output data rate. The sinc4 + sinc1 filter mode has shorter latency time than the single-stage sinc4 filter. Table 7-4 summarizes the sinc4 + sinc1 filter characteristics.

Table 7-4. Sinc4 + Sinc1 Cascade Filter Characteristics

MODE	f_{CLK} (MHz)	OSR (A × B)(2)	DATA RATE (kSPS)	–3dB FREQUENCY (kHz)	LATENCY TIME (µs)(1)
Max speed	32.768	64 (32 × 2)	256	87.49	10.9
High speed	25.6		200	68.35	13.9
Mid speed	12.8		100	34.18	27.9
Low speed	3.2		25	8.544	111

Table 7-4. Sinc4 + Sinc1 Cascade Filter Characteristics (continued)

MODE	f_{CLK} (MHz)	OSR (A × B)[2]	DATA RATE (kSPS)	–3dB FREQUENCY (kHz)	LATENCY TIME (µs)[1]
Max speed	32.768	128 (32 × 4)	128	52.44	14.8
High speed	25.6		100	40.97	19.0
Mid speed	12.8		50	20.49	37.9
Low speed	3.2		12.5	5.121	152
Max speed	32.768	320 (32 × 10)	51.2	22.36	26.5
High speed	25.6		40	17.47	34.0
Mid speed	12.8		20	8.735	67.9
Low speed	3.2		5	2.184	272
Max speed	32.768	640 (32 × 20)	25.6	11.28	46.0
High speed	25.6		20	8.814	58.9
Mid speed	12.8		10	4.407	118
Low speed	3.2		2.5	1.102	471
Max speed	32.768	1280 (32 × 40)	12.8	5.658	85.1
High speed	25.6		10	4.420	109
Mid speed	12.8		5	2.210	218
Low speed	3.2		1.25	0.552	871
Max speed	32.768	3200 (32 × 100)	5.12	2.266	202
High speed	25.6		4	1.770	259
Mid speed	12.8		2	0.885	517
Low speed	3.2		0.5	0.221	2068
Max speed	32.768	6400 (32 × 200)	2.56	1.133	398
High speed	25.6		2	0.885	509
Mid speed	12.8		1	0.443	1018
Low speed	3.2		0.25	0.111	4075
Max speed	32.768	12800 (32 × 400)	1.28	0.566	788
High speed	25.6		1	0.442	1008
Mid speed	12.8		0.5	0.221	2017
Low speed	3.2		0.125	0.055	8069
Max speed	32.768	32000 (32 × 1000)	0.512	0.226	1960
High speed	25.6		0.4	0.177	2508
Mid speed	12.8		0.2	0.089	5018
Low speed	3.2		0.05	0.022	20070

(1) Latency time increases by 8 / f_{CLK} (µs) when the analog input buffers are enabled.
(2) A = First stage OSR, B = Second stage OSR.

Figure 7-20 illustrates the frequency response of the sinc4 + sinc1 filter for three OSR values. The combined frequency response is the overlaid response of the sinc4 and sinc1 filters. For low OSR values, the response profile is dominated by the roll-off of the sinc4 filter. Nulls in the frequency response occur at $n \cdot f_{DATA}$, n = 1, 2, 3, and so on. At the null frequencies, the filter has zero gain.

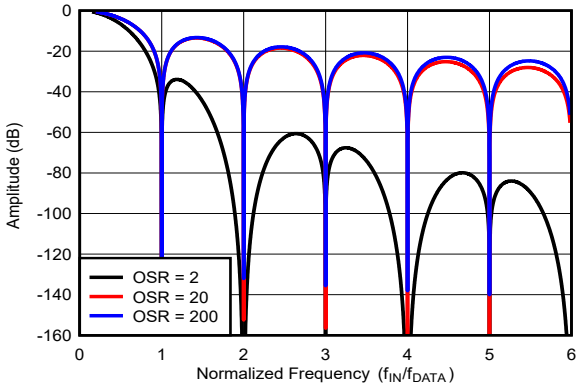


Figure 7-20. Sinc4 + Sinc1 Frequency Response

7.3.8.2.3 Sinc3 Filter

The sinc3 filter mode is a single-stage filter. The sinc3 filter provides several data rate options including 400SPS, 60SPS, and 50SPS for line-cycle noise rejection. 10SPS is achieved by slowing the ADC clock to 10/50 x 3.2MHz = 0.64MHz in low-speed mode. Because of the large width of the frequency response notch, excellent line-frequency NMRR and CMRR is achieved. Table 7-5 summarizes the characteristics of the sinc3 filter.

Table 7-5. Sinc3 Filter Characteristics

MODE	f_{CLK} (MHz)	OSR	DATA RATE (SPS)	–3dB FREQUENCY (Hz)	LATENCY (ms)	NMRR AT FIRST NULL (dB)	
						2% CLOCK TOLERANCE	6% CLOCK TOLERANCE
Max speed	32.768	26667	614.4	161.3	4.88	100	71
High speed	25.6		480	126	6.25		
Mid speed	12.8		240	63.0	12.5		
Low speed	3.2		60	15.7	50.0		
Max speed	32.768	32000	512	134	5.86	100	71
High speed	25.6		400	105	7.50		
Mid speed	12.8		200	252	15		
Low speed	3.2		50	13.1	60.0		

Figure 7-21 shows the frequency response of the sinc3 filter (OSR = 32000). Figure 7-22 shows the detailed response in the region of 0.9 to 1.1 · f_{IN} / f_{DATA}.

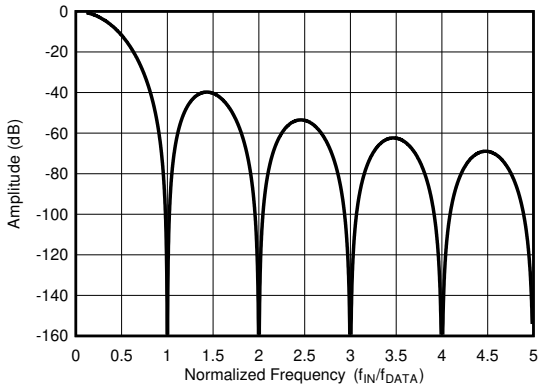


Figure 7-21. Sinc3 Frequency Response (OSR = 32000)

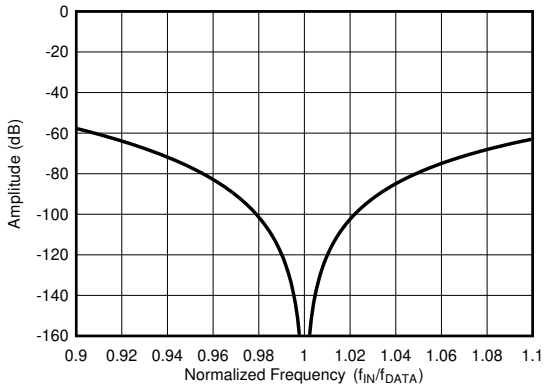


Figure 7-22. Detail Sinc3 Frequency Response (OSR = 32000)

7.3.8.2.4 Sinc3 + Sinc1 Filter

The sinc3 + sinc1 filter mode is the cascade of the sinc3 and a sinc1 filter. The OSR of the sinc3 stage is fixed (OSR = 32000) and the OSR of the sinc1 stage is programmable to 3 and 5. Table 7-6 summarizes the characteristics of the sinc3 + sinc1 filter.

Table 7-6. Sinc3 + Sinc1 Filter Characteristics

MODE	f_{CLK} (MHz)	OSR (A × B) (1)	DATA RATE (SPS)	–3dB FREQUENCY (Hz)	LATENCY (ms)	NMRR AT FIRST NULL (dB)	
						2% CLOCK TOLERANCE	6% CLOCK TOLERANCE
Max speed	32.768	96000 (32000 × 3)	170	69	9.77	34	26
High speed	25.6		133.3	54	12.5		
Mid speed	12.8		66.6	27	25		
Low speed	3.2		16.7	6.7	100		
Max speed	32.768	160000 (32000 × 5)	102	43.5	13.7	34	26
High speed	25.6		80	34	17.5		
Mid speed	12.8		40	17	35		
Low speed	3.2		10	4.2	140		

(1) A = First stage OSR, B = Second stage OSR.

Figure 7-23 shows the frequency response of the sinc3 + sinc1 filter. The frequency response exhibits the characteristic sinc filter response lobes and nulls. The nulls occur at f_{DATA} and at multiples thereof. Figure 7-24 shows the detailed response in the region of 0.9 to 1.1 · f_{IN} / f_{DATA}.

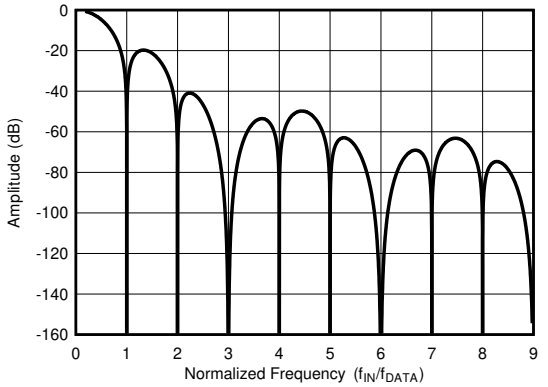


Figure 7-23. Sinc3 + Sinc1 Frequency Response

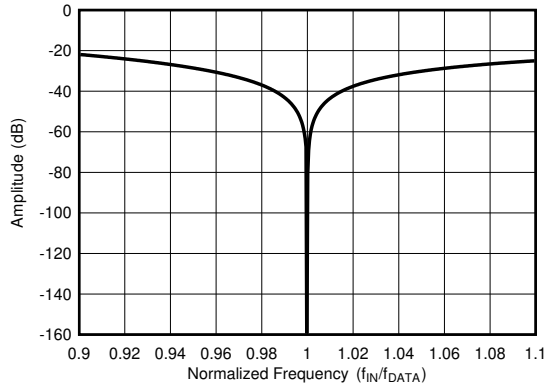


Figure 7-24. Detail Sinc3 + Sinc1 Frequency Response

7.4 Device Functional Modes

7.4.1 Reset

The ADC performs an automatic reset at power-on. Manual reset is also performed by the $\overline{\text{RESET}}$ pin or by the SPI port. The control logic, digital filter, SPI, data port operation, and user registers are reset to default values. The hardware programming pins used to program the device are also re-scanned. Device reset is confirmed by the POR_FLAG of the SPI STATUS register. See Figure 5-7 for details when the ADC is available for operation after reset.

7.4.1.1 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ pin is an active-low input that resets the ADC. The $\overline{\text{RESET}}$ pin is a Schmitt-triggered input designed to reduce noise sensitivity. See Figure 5-7 for $\overline{\text{RESET}}$ pin timing and for the start of SPI communications after reset. Because the ADC performs an automatic reset at power-on, a manual reset is not required.

7.4.1.2 Reset by SPI Register

The device is reset through SPI operation by writing 01011000b to the CONTROL register. Reset takes effect at the end of the frame at the time $\overline{\text{CS}}$ is taken high. Writing any other value to the register does not result in device reset.

7.4.1.3 Reset by SPI Input Pattern

The device is also reset through SPI by a special input pattern. The input pattern does not follow the input command format. To reset, input a *minimum* of 1024 consecutive ones, followed by taking $\overline{\text{CS}}$ high at which time reset occurs. Figure 7-25 shows the reset pattern.

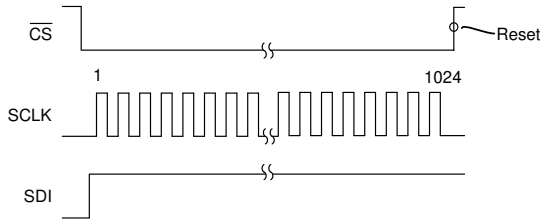


Figure 7-25. SPI Reset Pattern

7.4.2 Idle and Standby Modes

When conversions are stopped, the ADC has the option to idle the conversions or to enter standby mode. The mode is a global setting for all channels programmed by the STBY_MODE bit of the GEN_CFG2 register. In idle mode, the analog circuit is fully biased and operational, including sampling of the signal and voltage reference inputs. Only the digital filter is idle. When conversions are started, the digital filter is restarted to begin the conversion process.

When conversions are stopped in standby mode, sampling of the signal and reference voltage stop to conserve power. When conversions are restarted, sampling of the signal and reference voltages resume. Exiting standby mode adds $24f_{CLK}$ cycles to the conversion latency time of the filter.

7.4.3 Power-Down

Channels are individually powered down by the CH*n*_PWDN bits of the respective CH*n*_CFG2 configuration registers. The analog section of the channel is disabled and the output data are the last known data. In TDM mode, the slot position of a powered down channel is retained. When a channel is re-enabled, the conversions reset at the time of SPI register write. Resynchronize the ADC if required. If activating channels from all-channel power down, wait 300µs before synchronizing the channels.

7.4.4 Speed Modes

Four programmable speed modes allow tradeoffs between data rate, noise performance and power consumption. Table 7-7 shows the maximum data rates (OSR at minimum value) and nominal clock frequencies. Operation in the reduced speed modes lowers the device power consumption at reduced bandwidth for applications not requiring large signal bandwidths.

Table 7-7. Data Rates and Clock Frequencies

MODE	CLOCK FREQUENCY (f_{CLK})	f_{DATA} WIDEBAND FILTER	f_{DATA} LOW-LATENCY FILTER
Max speed	32.768MHz	512kSPS	1365.3kSPS
High speed	25.6MHz	400kSPS	1066.6kSPS
Mid speed	12.8MHz	200kSPS	533.3kSPS
Low speed	3.2MHz	50kSPS	133.3kSPS

The speed mode is programmed by the SPEED_MODE[1:0] bits of the GEN_CFG2 register. The speed mode selection is universal, applying to all channels. See the Section 5.3 for clock frequency tolerances.

7.4.5 Synchronization

The ADC channels are synchronized by the START pin or by writing the START bit of the SPI CONTROL register. Synchronization aligns the conversion times of all ADC channels together. If controlling conversions through SPI (using the start/stop control mode), keep the START pin low to avoid contention with the pin. In SPI programing mode, writing to registers in the address range of 08h through 50h results in simultaneous restart of all channels. The restart causes loss of synchronization to the original START signal. Resynchronize the ADC channels if necessary.

When using the internal clock divider with values > 1, ADC synchronization has uncertainty as to when the ADC channels are converting due to the unknown phase of the divided clock signal. However, the ADC channels remain synchronized together. To avoid synchronization uncertainty, use the divide by 1 option.

After synchronization, the ADC waits for the digital filter to settle before providing output data. The wait time is equal to the filter latency (see the *Digital Filter* section for filter latency data). When OSR values of the channels are different, the device waits for the *slowest* data channel to settle before the frame-sync output signals start. In this case, the RPT_DATA bit of the slower channel DP_STATUS byte is set when the data are repeated during faster channel updates.

The ADC has two modes for synchronization and control: *synchronized* and *start/stop* control modes, each with specific functionalities. In SPI programming mode, the mode is programmed by the START_MODE[1:0] bits of the GEN_CFG2 register. In hardware programming mode, the synchronized control mode is forced when the wideband filter mode is selected. The start/stop control mode is the forced when the low-latency filter mode is selected. The synchronized control mode is not available through SPI operation.

7.4.5.1 Synchronized Control Mode

Synchronized control mode synchronizes the ADC channels on the rising edge of the START pin. Conversions continue whether START is high or low. Apply a single synchronizing pulse input or a continuous clock input to the START pin.

As shown in Figure 7-26, synchronization occurs on the first START rising edge. If the time to the next START rising edge is an *n* multiple of the conversion period within a ±1 / f_{CLK} window, the ADC does not resynchronize (*n* = 1, 2, 3, and so on). Resynchronization does not occur because the ADC conversion period is equal to the period of the START signal. Conversely, if the START signal period is *not* an *n* multiple of the conversion period within ± one f_{CLK} cycle, the ADC channels resynchronize. There is no limit to the time period of the START signal.

Figure 7-26 shows the ADC resynchronizing when the period of START input is not equal to a single or multiples of the conversion period. As a result of the digital filter processing time, a time difference exists between the START signal that caused synchronization and the resulting FSYNC output signal. The time difference varies with the OSR value of the filter.

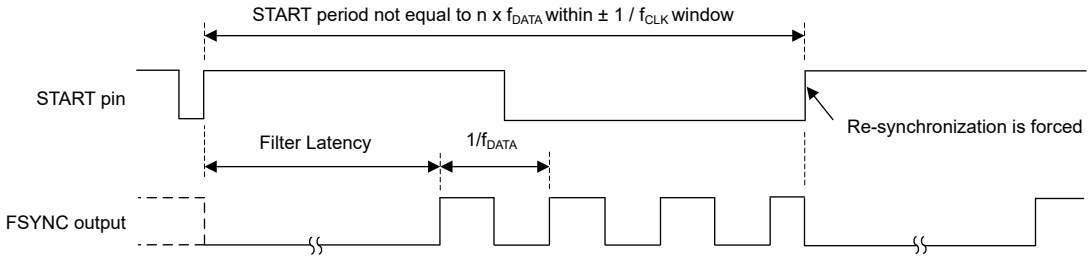


Figure 7-26. Synchronized Control Mode

7.4.5.2 Start/Stop Control Mode

Start/stop control mode enables and disables conversions. All channels are synchronized (started) by taking the START pin high or by writing 1b to the START bit of the CONTROL register. The START bit is acknowledged when $\overline{CS}$ is taken high following the register write operation. The ADC continue conversions until stopped by taking the START pin low, or by writing 1b to the STOP bit. When stopped, conversions in progress complete and additional conversions are stopped. The final rising edge of the FSYNC clock signal is the last conversion data. To restart an ongoing conversion, pulse START low to high, or write 1b to the START bit a second time. To perform a one-shot conversion, briefly pulse START high, or write to the STOP bit soon after writing to the START bit. Figure 7-27 shows the START control and the FSYNC output signal.

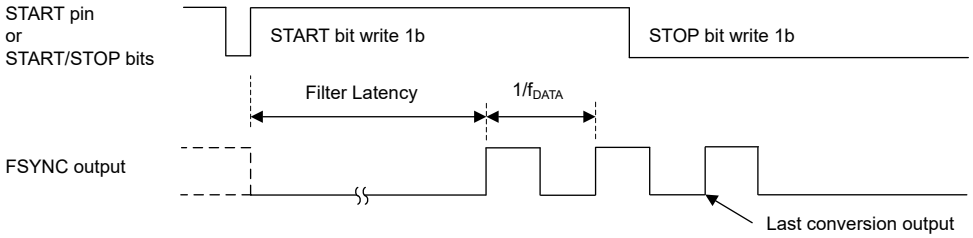


Figure 7-27. Start/Stop Control Mode

7.4.6 Conversion-Start Delay Time

A programmable delay time delays the start of the first conversion after synchronization. After the delay is used for the first conversion, following conversions are not delayed until synchronized again. The delay time allows for settling of external components. For example, providing time for signal switching through an external multiplexer. The delay is global to all ADC channels and adds to the conversion latency time. See the DELAY[2:0] bits of the GEN_CFG1 register.

7.4.7 Calibration

Offset and gain registers for each channel correct offset and gain errors. As shown in Figure 7-28, a 24-bit offset register value is subtracted from the conversion data before multiplication by a 24-bit gain register value. Data are rounded to 16-bits and clipped to +FS and –FS code values for the final output.

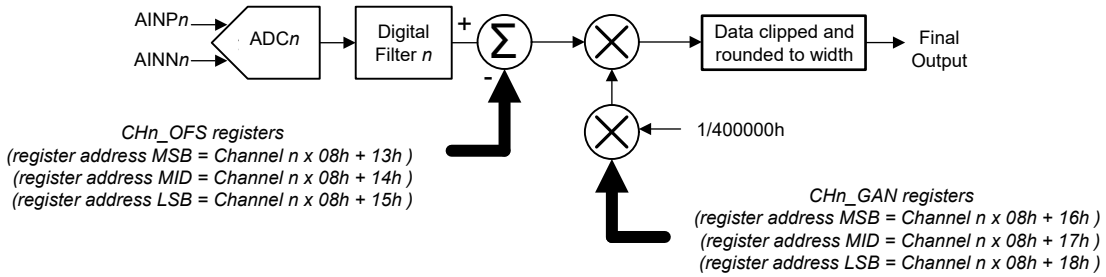


Figure 7-28. Calibration Block Diagram

Equation 18 shows how conversion data are calibrated:

$$\text{Final Output Data} = (\text{Data} - \text{CH}n\text{\_OFS}) \times \text{CH}n\text{\_GAN} / 400000\text{h} \quad (18)$$

7.4.7.1 Offset Calibration Registers

The offset calibration value is a 24-bit word consisting of three registers coded in two's-complement format. The offset value is subtracted from the conversion data. The most-significant byte of the three registers for each channel is the low address. See the CH*n* Offset register for the register addresses for each channel. The conversion data are left-justified to align with the most-significant offset byte. Table 7-8 shows example offset calibration values.

Table 7-8. OFFSET Register Values

OFFSET REGISTER VALUE	OFFSET APPLIED
001000h	–16 LSB
000100h	–1 LSB
FFFF00h	1 LSB
FFF000h	16 LSB

7.4.7.2 Gain Calibration Registers

The gain calibration value is a 24-bit word consisting of three registers coded in straight-binary format and normalized to unity gain at 400000h. For example, to correct a gain error > 1, the gain calibration value is < 400000h. Table 7-9 shows example gain calibration values. The most-significant byte of the three registers is the low address. See the CH*n*_Gain register for the gain register addresses of each channel.

Table 7-9. GAIN Register Values

GAIN REGISTER VALUE	GAIN CORRECTION APPLIED
433333h	1.05
400000h	1
3CCCCCh	0.95

7.4.7.3 Calibration Procedure

The recommended calibration procedure is as follows:

1. Preset the offset and gain calibration registers to 000000h and 400000h, respectively.
2. Perform offset calibration by shorting the inputs using the input multiplexer. To include the offset error of the external amplifier stages, short the inputs of the system. Acquire conversion data from the channel and write the average value of the data to the offset calibration registers. Averaging the data reduces conversion noise to improve calibration accuracy.
3. Perform gain calibration by applying a calibration signal to the inputs. To include the gain error of the external amplifier stage, apply the signal to the system inputs. For standard input range mode, choose the calibration voltage to be less than the full-scale input range to avoid clipping the output code. Clipped output codes result in inaccurate calibration. For example, use a 3.9V calibration signal with V_{REF} = 4.096V. If operating in extended input range mode, a calibration signal equal to V_{REF} can be used. Acquire conversion data from the channel and average the results. Use Equation 19 to calculate the gain calibration value.

   $$\text{Gain Calibration Value} = (\text{expected output code} / \text{actual output code}) \cdot 400000\text{h} \quad (19)$$

   For example, the expected output code of a 3.9V calibration voltage using a 4.096V reference voltage is: (3.9V / 4.096V) · 7FFFFFh = 79E000h.

7.4.8 Diagnostics

The device has several diagnostics to detect errors during ADC operation.

7.4.8.1 $\overline{\text{ERROR}}$ Pin and ERR_FLAG Bit

The $\overline{\text{ERROR}}$ pin is an open-drain digital output with an internal 100kΩ pull-up resistor that drives low to indicate an error. Figure 7-29 shows the $\overline{\text{ERROR}}$ pin block diagram. Use a stronger value pullup resistor if leakage current from the controller input causes an output-high voltage error. The $\overline{\text{ERROR}}$ pins from several devices can be tied together. Read the STATUS registers to determine the device that asserted the error.

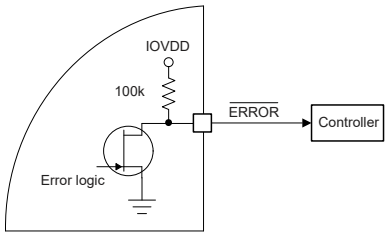


Figure 7-29. $\overline{\text{ERROR}}$ pin

An error is the logical OR of the seven SPI STATUS register bits. Table 7-10 shows the STATUS register bits that cause an error.

Table 7-10. ERROR BITS

STATUS REGISTER BITS	BIT LOCATION	FUNCTION
ALV_FLAG	STATUS[6]	Analog low-voltage flag
POR_FLAG	STATUS[5]	Power-on reset flag
SPI_ERR	STATUS[4]	SPI input CRC error
REG_ERR	STATUS[3]	Register map CRC error
ADC_ERR	STATUS[2]	Internal ADC error
ADDR_ERR	STATUS[1]	SPI register address error
SCLK_ERR	STATUS[0]	SCLK count error

$\overline{\text{ERROR}}$ is driven low at power-up due to automatic assertion of the ALV_FLAG and POR_FLAG flags. Although not required for device operation, write 1b to the SPI STATUS register to clear the power flags to allow indication of other errors. Other error bits are cleared by writing 1b after the error condition causing the error is removed. The ERR_FLAG of the data port STATUS byte is the inversion of the $\overline{\text{ERROR}}$ pin. In hardware control mode, there is no access to the STATUS register, therefore an error is caused only by the ADC_ERR bit.

7.4.8.2 SPI CRC

The SPI CRC is an SPI error check code that detects transmission errors to and from the SPI port. A CRC byte is transmitted with the ADC input data from the host. A CRC byte is transmitted with the register data from the ADC. The SPI CRC error check is enabled by the SPI_CRC_EN bit of the GEN_CFG3 register.

The SPI CRC argument is two bytes. The CRC-In code is calculated over the two input command bytes. Any input bytes padded to the start of the frame are not included in the CRC calculation. The ADC checks the input command CRC code against an internal code calculated over the two received bytes. If the CRC codes do not match, the command is not executed and the SPI_ERR bit is set in the STATUS byte. Further register write operations are blocked except to the STATUS register to allow clearing the SPI CRC error by writing 1b to the SPI_ERR bit. Register read operations are not blocked unless an SPI_CRC error is detected in the immediately preceding register read command frame.

The CRC-Out code is calculated over the output register data byte and the STATUS byte. If STATUS is disabled, the byte is treated as zero for CRC-Out calculation purposes.

The CRC value is the 8-bit remainder of a bitwise exclusive-OR (XOR) operation of the variable-length argument with the CRC polynomial. The 8-bit CRC is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X^1 + 1$. The nine coefficients of the polynomial are: 1 00000111.

The following procedure computes the CRC value:

1. Left shift the initial data value by eight bits by appending 0s in the LSB, creating a new data value.
2. Perform an initial XOR to the MSB of the new data value from step 1 with FFh.
3. Align the MSB of the CRC polynomial to the left-most, logic 1 of the data.
4. The bits of the data value not in alignment with the CRC polynomial drop down and append to the right of the new XOR result. XOR the data value with the aligned CRC polynomial. The XOR operation creates a new, shorter-length value.
5. If the XOR result is less than or equal to the 8-bit CRC length, the procedure ends, yielding an 8-bit CRC code result. Otherwise, continue with the XOR operation at step 3 using the current XOR result. The number of loop iterations depend on the value of the initial data.

7.4.8.3 Register Map CRC

The register map CRC detects changes to the register values. The CRC is a 16-bit value stored at register 05h (high byte) and register 06h (low byte). Calculate the CRC over the register address range 08h to 50h (for both ADS117L14 and ADS117L18) and write the value to the CRC registers. The ADC compares the CRC register value to an internal calculation. The REG_ERR flag of the STATUS byte is set if the CRC register value is incorrect. Correct the CRC value, then write 1b to the REG_ERR bit to clear the error. The REG_CRC_EN bit of the GEN_CFG3 register enables the register CRC.

The register map CRC uses a 16-bit polynomial based on the CRC-16-IBM polynomial: $X^{16} + X^{15} + X^2 + 1$. The 17 coefficients are *1 10000000 00000101*.

7.4.8.4 ADC Error

The ADC performs continuous checks of the internal non-volatile memory. The ADC_ERR flag of the STATUS register is set if an error is detected. Reset or power-cycle the ADC to clear the ADC_ERR.

7.4.8.5 SPI Address Range

Register access by the read and write commands is checked for valid address range. The valid address range is 00h to 50h for both ADS117L14 and ADS117L18 devices. The ADDR_ERR bit is set in the STATUS register when the register address range is exceeded. Clear the error by writing 1b. Except for the STATUS register, register write operations are blocked if the flag is set. Address range checking is enabled by setting SPI_ADDR_EN = 1b in the GEN_CFG3 register.

7.4.8.6 SCLK Counter

An SCLK counter monitors the number of SCLKs in an SPI frame to be multiples of 8. The SCLK_ERR flag of the STATUS register is set if the number of SCLKs is not a multiple of 8. Except for the STATUS register, register write operations are blocked until the flag is cleared by writing 1b to the bit. The SCLK counter is enabled by setting SCLK_CNT_EN = 1b of the GEN_CFG3 register.

7.4.8.7 Clock Counter

The ADC provides a clock counter to verify the internal clock frequency. CLK_CNT is an 8-bit register operating in continuous rollover mode at a frequency = $f_{CLK}/32$. To verify the clock frequency, read the register at known intervals and compare the difference of values to the expected value. The ADC must be in active conversion mode with a minimum SCLK frequency of $f_{CLK}/32$ to read the counter value.

The counter is enabled by the CLK_CNT_EN bit of the GEN_CFG3 register. When enabled, the counter value initializes to 00h. When disabled, the counter value is 00h.

7.4.8.8 Frame-Sync CRC

The frame-sync CRC is an optional byte appended to the conversion data. The CRC is eight bits and is calculated over the two data bytes and, if enabled, three bytes including the STATUS_DP byte. The CRC uses the same CRC-8 ATM polynomial as the SPI CRC. The DP_CRC_EN bit of the DP_CFG1 register enables the CRC byte.

7.4.8.9 Self Test

Each channel of the device provides offset error, gain error, noise, and CMRR test capability. The tests are accomplished by using the test modes of the input multiplexer and by external processing of the resulting data. See Table 7-1 for the test options.

7.4.9 Frame-Sync Data Port

The frame-sync data port outputs conversion data. The port is a synchronous, read-only interface with FSYNC and DCLK output clock signals with a programmable number of data lanes for the DOUTx pins. The frame-sync signals are continuously operated except when stopped in the start/stop control mode.

Figure 7-30 shows the frame-sync pins. Pins 8 through 13 of the frame-sync port are multiplexed with GPIO pins. When enabled, the GPIO function takes priority over the frame-sync pins. Default operation is GPIO disabled.

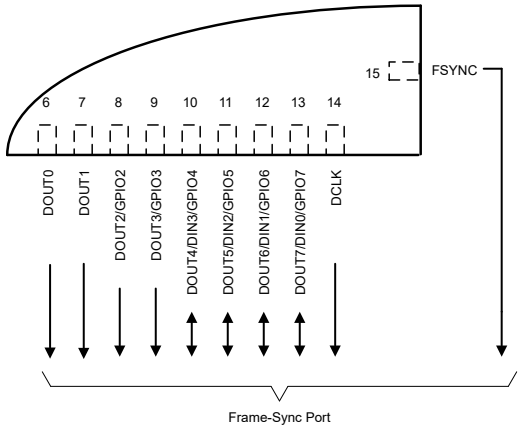


Figure 7-30. ADS117L18 Frame-Sync Port Pins

Figure 7-31 shows the FSYNC, DCLK and DOUTx signals. (DIN and GPIO functions are subsequently removed from the pin names). New conversion data are synchronized on the FSYNC rising edges, where the data bits update on the DCLK falling edges. The data are shifted out continuously with no breaks between packets. The *dependent* fields shown in the figure are dependent on the time division multiplexing and the input bits from daisy-chain operation.

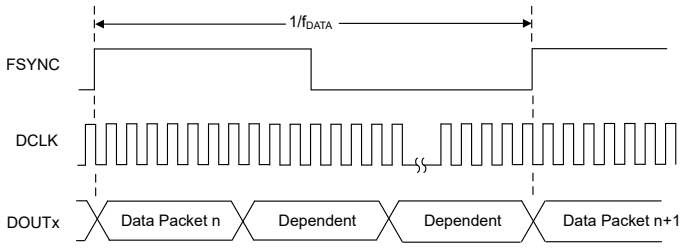
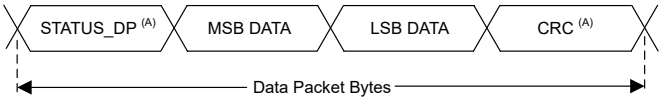


Figure 7-31. Frame-Sync Port Operation

7.4.9.1 Data Packet

The data port provides the conversion data in the form of data packets. A data packet consists of a STATUS_DP header byte, the channel data, and a CRC byte. The STATUS_DP and CRC bytes are optional and correspond to the conversion data of each channel. Figure 7-32 shows a full length, four-byte data packet, but is configurable to a two-byte packet consisting of 16-bit data alone. The STATUS_DP header and CRC bytes of the packet are enabled by bits 7 and 6 of the DP_CFG1 register.



A. STATUS_DP and CRC bytes are optional.

Figure 7-32. Data Packet

7.4.9.2 Data Format

The ADCs support two data formats: bipolar and unipolar, programmable by the CH*n*_FORMAT bits of the CH*n*_CFG1 registers for each channel. The bipolar format represents the positive and negative signal range with the data coded in two's-complement format, MSB sign bit first. The unipolar format represents the positive signal range only, coded in straight-binary format. Data values for the negative signal range are clamped to 0. Full 16-bit resolution for positive range signals is provided by the unipolar format. Table 7-11 shows the data scaling. Conversion data clips to the minimum/maximum code values when the signal exceeds the minimum/maximum input range.

Table 7-11. Bipolar Data Format (CH*n*_FORMAT = 0)

INPUT VOLTAGE, V_{IN} (V)(1)	OUTPUT DATA(2)	
	STANDARD RANGE	EXTENDED RANGE
$1.25 \cdot k \cdot V_{REF} \cdot (2^{15} - 1) / 2^{15}$	7FFFh	7FFFh
$k \cdot V_{REF} \cdot (2^{15} - 1) / 2^{15}$		6666h
$k \cdot V_{REF} / 2^{15}$	0001h	0001h
0	0000h	0000h
$-k \cdot V_{REF} / 2^{15}$	FFFFh	FFFFh
$-k \cdot V_{REF}$	8000h	999Ah
$-1.25 \cdot k \cdot V_{REF}$		8000h

Table 7-12. Unipolar Data Format (CH*n*_FORMAT = 1)

INPUT VOLTAGE, V_{IN} (V)(1)	OUTPUT DATA(2)	
	STANDARD RANGE	EXTENDED RANGE
$1.25 \cdot k \cdot V_{REF}$	FFFFh	FFFFh
$k \cdot V_{REF}$		CCCCh
$k \cdot V_{REF} / 2^{16}$	0001h	0001h
≤0	0000h	0000h

(1) k = 1 or 2 depending on the 1x or 2x input range option.
(2) Ideal output data, excluding offset, gain, linearity, and noise errors.

7.4.9.3 STATUS_DP Header Byte

STATUS_DP is an optional header byte prefixed to the conversion data. STATUS_DP indicates the channel number of the data as well as status indicators. Figure 7-33 and Table 7-13 show the field descriptions. The STATUS_DP header is enabled by setting the DP_STAT_EN bit of the DP_CFG1 register.

Figure 7-33. STATUS_DP Header

7	6	5	4	3	2	1	0
PWR_FLAG	ERR_FLAG	MOD_FLAG	RPT_DATA	$\overline{\text{PWDN}}$	CH_ID[2:0]		

Table 7-13. STATUS_DP Header Field Descriptions

Bit	Field	Description
7	PWR_FLAG	Power flag. This flag is the OR of the ALV_FLAG and POR_FLAG from the SPI STATUS register, which indicates device power-up. If desired, clear the PWR_FLAG by clearing ALV_FLAG and POR_FLAG. Clearing the PWR_FLAG is not necessary for device operation. This bit is always 0b in hardware programming mode. 0b = No power supply event from flag last cleared 1b = Power-supply event
6	ERR_FLAG	Error flag. This bit is the inversion of the ERROR pin output. This bit is always 0b in hardware programming mode. See the *Error Pin* section for more details. 0b = No error 1b = Error
5	MOD_FLAG	Modulator saturation flag. This bit indicates modulator saturation during the conversion cycle. The flag is updated at the completion of each conversion. 0b = No modulator saturation 1b = Modulator saturation
4	RPT_DATA	Repeat data flag. This bit indicates whether data are new or repeated. Repeated data are caused by different data rates between channels with slower channels repeating the original data between updates of faster channels. Repeated data are also caused by the repeat-data mode, programmed by the DP_DAISY bit of the DP_CFG1 register. This bit is always 0b in hardware programming mode. 0b = Data are new 1b = Data are repeated
3	$\overline{\text{PWDN}}$	Power down flag. This bit indicates power down or standby mode. 0b = Channel in power down or standby mode 1b = Normal operation
2:0	CH_ID[2:0]	Channel identification number. These bits show the channel number corresponding to the data. 000b = Channel 0 001b = Channel 1 010b = Channel 2 011b = Channel 3 100b = Channel 4 (ADS117L18 only) 101b = Channel 5 (ADS117L18 only) 110b = Channel 6 (ADS117L18 only) 111b = Channel 7 (ADS117L18 only)

7.4.9.4 FSYNC Pin

The FSYNC pin is the word clock signal of the frame-sync port. FSYNC transitions high to indicate the beginning of new channel data. The FSYNC clock frequency is f_{DATA}. If the channels are programmed to different data rates, the FSYNC frequency is the fastest data channel.

7.4.9.5 DCLK Pin

The DCLK pin is the frame-sync port bit-clock output signal that shifts out conversion data from the DOUTx pins. Data are updated on the falling DCLK edge and are read on the rising DCLK edge.

The DCLK frequency is derived from the clock input signal by a programmable divider. See the *Clock Operation* section for the details of the CLK and DCLK dividers. The DCLK signal frequency must be sufficient to transmit the data in one conversion period, otherwise data are lost. Equation 20 shows how to calculate the minimum DCLK frequency for the eight-channel ADS117L18.

$$f_{DCLK} \geq f_{DATA} \cdot \text{TDM ratio} \cdot \text{Data Packet Size} \quad (20)$$

where:

- f_{DATA} = Data rate (Hz).

- TDM ratio = 1: eight data lanes, 2: four data lanes, 4: two data lanes, 8: one data lane.
- Data packet = Number of bits in a channel data packet (16, 24 or 32 bits).

As an example of the eight-channel ADS117L18 operating with f_{DATA} = 200kSPS, TDM ratio = 2 (four data lanes), and 32-bit data packet, the minimum DCLK frequency = 200kHz · 2 · 32 = 12.8MHz. DCLK can be higher than the required minimum in which case the extra bits occurring after the data packet bits are ignored. For the four-channel ADS117L14, divide the TDM ratio in the f_{DCLK} equation (pertaining to the number of data lanes) by two. When operating devices in daisy-chain mode, multiply the TDM ratio in the f_{DCLK} equation by the number of devices in the chain.

Table 7-14 shows additional examples of CLK and DCLK frequencies for the ADS117L18. Use the DCLK and CLK dividers to provide the required ADC and DCLK clock frequencies based on the speed mode, data rate, TDM ratio and packet size.

Table 7-14. DCLK Frequency Examples for Eight-Channel ADS117L18

SPEED MODE	DATA RATE (kSPS)	TDM RATIO	PACKET SIZE	DCLK MIN (MHz)	CLKIN INPUT (MHZ)	CLK DIVIDER (1)	ADC CLOCK (MHz)	DCLK DIVIDER (1)	DCLK ACTUAL (MHz)
Max	1365.$\overline{3}$	2	24	65.536	65.536	2	32.768	1	65.536
Max	512	1	24	12.288	32.768	1	32.768	2	16.384
Max	512	4	24	49.152	65.536	2	32.768	1	65.536
High	400	4	24	38.4	51.2	2	25.6	1	51.2
Mid	200	4	32	25.6	25.6	2	12.8	1	25.6
Mid	200	1	32	6.4	12.8	1	12.8	1	12.8
Low	50	8	32	12.8	12.8	4	3.2	1	12.8

(1) Daisy chain operation requires that the CLK and DCLK dividers are programmed to the divide by 1 option.

7.4.9.6 DOUTx Pins

DOUTx are the data output pins of the frame-sync port. Output data are updated on the DCLK falling edges and latched by the host on the rising edges. The number of DOUTx pins providing channel data is programmed by the DP_TDM[1:0] bits of the DP_CFG1 register. Inactive DOUTx pins are available as GPIO or as daisy-chain input pins (DIN) to input data from another device.

7.4.9.7 DINx Pins

The DINx pins are the frame-sync port digital inputs that receive data from another device for daisy-chain operation. The number of DOUTx pins (or data lanes) is programmed by the DP_TDM[1:0] bits of the DP_CFG1 register. Depending on the level of DP_TDM[1:0] programming, unused DOUTx pins automatically change state to DINx input pins. The exception is the DOUT1 pin which remains as an output. If daisy-chain mode is not used, tie the DINx pins to ground or use pull-down resistors. Do not let the DINx pins float.

7.4.9.8 Time Division Multiplexing

Time division multiplexing (TDM) mode serializes channel data into the data lanes. The number of data lanes are programmable to 1, 2, 4 or 8 for ADS117L18 and 1, 2 or 4 for the ADS117L14. When the number of data lanes is less than the number of channels, the device packs data in TDM mode. The DP_TDM[1:0] bits of the DP_CFG1 register programs the number of data lanes.

The general characteristics of the data lanes are listed below.

- If the number data lanes are less than eight (ADS117L18) or less than four (ADS117L14), the unused DOUT pins become data inputs to support daisy chaining. The exception is DOUT1 which remains a driven output.
- The DINx pin numbers correlate to the DOUTx pin numbers for daisy chaining. The data inputs must either be tied low (or high as desired), or driven by a daisy chain device.
- When a channel is powered down, the data slot occupies the same position with frozen data. The channel ID bits of the STATUS byte remain active.
- When channels are powered down, the DOUTx pins of the data lanes remain as outputs.

Figure 7-34 shows the one data-lane option for the ADS117L18. DOUT2 through DOUT7 become unused inputs which must not be allowed to float. Apply daisy-chain data to the DIN0 pin. If unused, tie the pin to ground.

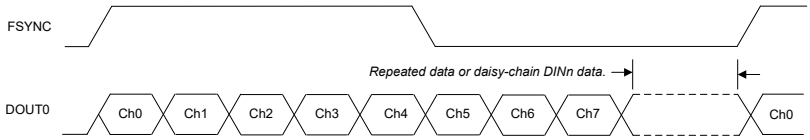


Figure 7-34. DP_TDM[1:0] = 00b, One Data Lane (ADS117L18)

Figure 7-35 shows the two data-lane option for the ADS117L18 and the one data-lane option for the ADS117L14. DOUT2 through DOUT7 (ADS117L18) and DOUT2, DOUT3 (ADS117L14) become unused inputs which must not be allowed to float. Apply daisy-chain data to the DIN0 pin (ADS117L14) and to DIN0, DIN1 (ADS117L18). If unused, tie the pins to ground.

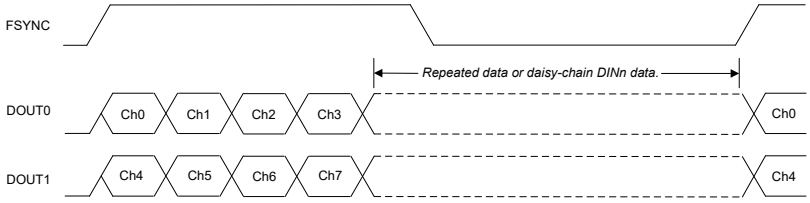


Figure 7-35. DP_TDM[1:0] = 01b, Two Data Lanes (ADS117L18) or One Data Lane (ADS117L14)

Figure 7-36 shows the four data-lane option for the ADS117L18 and the two data-lane option for the ADS117L14. DOUT4 through DOUT7 (ADS117L18) become unused inputs which must not be allowed to float. Apply daisy-chain data to DIN0, DIN1 (ADS117L14) and DIN0 through DIN3 (ADS117L18). If unused, tie to ground.

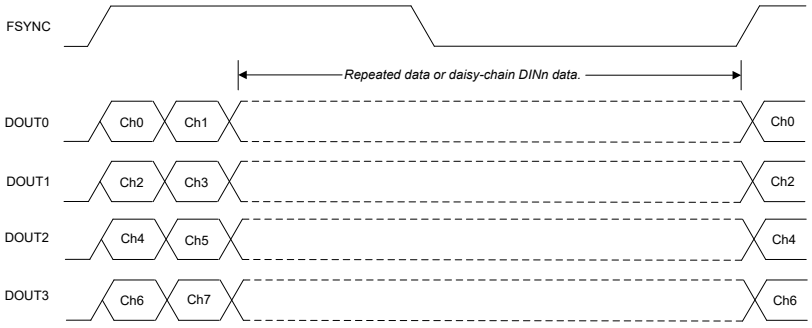


Figure 7-36. DP_TDM[1:0] = 10b, Four Data Lanes (ADS117L18) or Two Data Lanes (ADS117L14)

Figure 7-37 shows the eight data-lane option for the ADS117L18 and four data-lane option for the ADS117L14. DOUT4 through DOUT7 are not available for the ADS117L14. Daisy chaining is not possible for this mode.

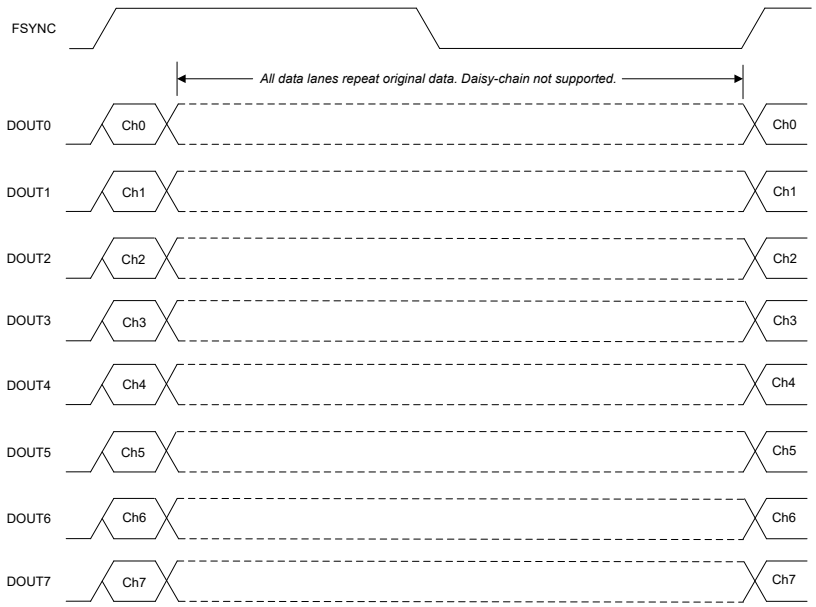


Figure 7-37. DP_TDM[1:0] = 11b, Eight Data Lanes (ADS117L18) or Four Data Lanes (ADS117L14)

7.4.9.9 Daisy Chain

The device supports daisy-chaining of the frame-sync ports to reduce the number of data lanes when multiple devices are used. For daisy-chaining, connect the DOUTx pins to the DINx pins of the following devices. Data appearing on the following devices DINx pins are shifted in and append to the data on DOUTx. The DP_DAISY bit of the DP_CFG1 register programs the DINx pins to receive data for daisy-chaining. If disabled, daisy-chain input data are ignored and original data of each device are repeated.

There is no limit to the number of daisy-chained devices, provided the OSR and packet size are considered so all data are output within a conversion period, otherwise data are lost. See the DCLK Pin section for details of DCLK.

The general requirements for devices in daisy-chain operation are as follows:

- The ADC clock and DCLK frequencies are the same.
- DCLK_DIV[1:0] and CLK_DIV[2:0] are programmed to the divide-by-1 values.
- External clock operation.
- DP_TDM[1:0] (TDM mode) is programmed the same for all devices in the chain.
- Devices are synchronized together.

Figure 7-38 shows a daisy-chain connection of two ADS117L18 devices using one data lane for 16 channels of data (DP_TDM[1:0] = 00b). In this TDM mode, the DOUT[7:4] pins default to DIN[3:0] data inputs. Because DOUT2 and DOUT3 also become unused inputs, external pull-down resistors are used to prevent the inputs from floating. DOUT1 is an unconnected output. Because of the amount of data required to be shifted out within a data period, the minimum value OSR is 256 to operate with 32-bit data packets.

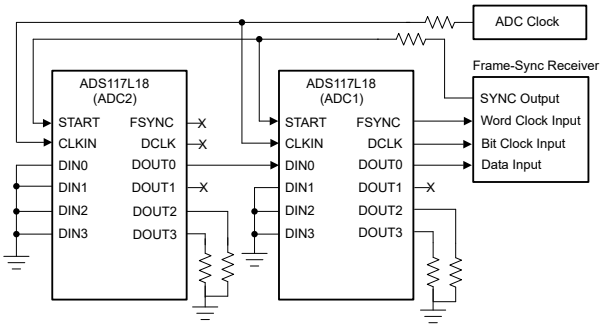


Figure 7-38. One-Lane Daisy Chain

Figure 7-39 shows the data format of the one data-lane connection.

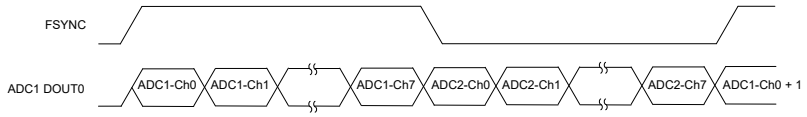


Figure 7-39. One-Lane Daisy Chain Data

Figure 7-40 shows a daisy-chain connection of two ADS117L18 devices using four data lanes for 16 channels of data (DP_TDM[1:0] = 10b). An alternative approach is to operate the devices in parallel in two data-lane mode yielding the same number of data lanes, but with a different data format.

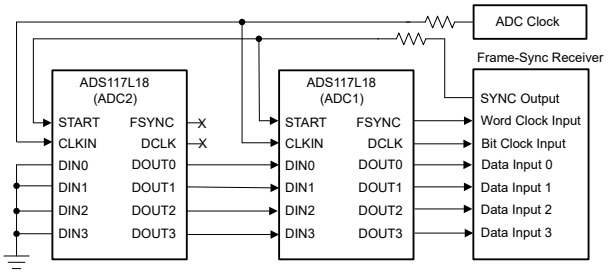


Figure 7-40. Four-Lane Daisy Chain

Figure 7-41 shows the data format of the four data-lane connection.

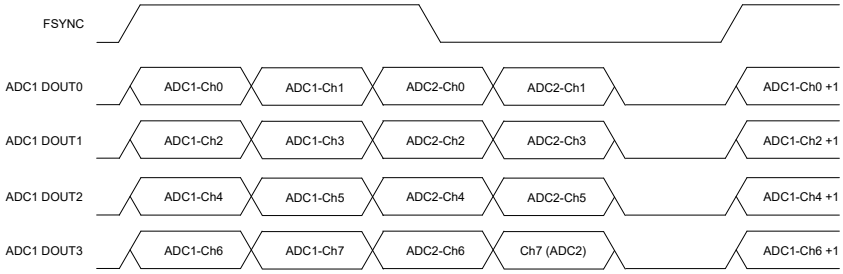


Figure 7-41. Four-Lane Daisy Chain Data

7.4.9.10 DOUTx Timing

The timing of the DOUTx pins is programmable to help meet external requirements. DOUTx is delayed or advanced relative to the FSYNC and DCLK signals over a ±6ns range with an approximate bit weight = 0.3ns, as shown in the Figure 7-42. The timing between the FSYNC and DCLK signals is fixed. The DOUT_DLY[4:0] bits of the DP_CFG2 register programs the DOUTx timing.

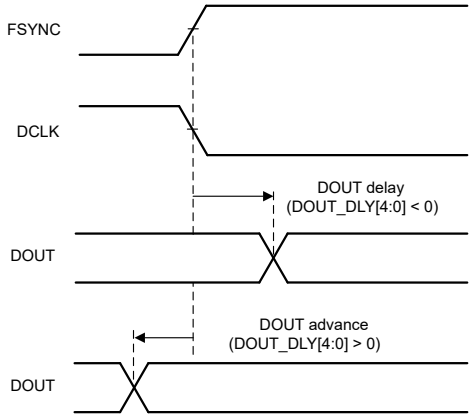


Figure 7-42. DOUT Timing Adjustment

7.5 Programming

The device has two interfaces: frame-sync and SPI. The frame-sync interface provides the conversion data and the SPI interface is used to configure the device. The device is also programmed by hardware device pins to replace SPI programming. The MODE pin selects between hardware programming or SPI programming mode. The MODE pin is read at power-up and after reset to determine the programming mode. See the *Hardware Programming* section for details. See the *SPI Programming* section for SPI programming details.

7.5.1 Hardware Programming

In the hardware programming mode, the device is programmed by strapping the pins to IOVDD, DGND or floated, but also can be tied to a controller I/O to change ADC configuration as needed. Hardware programming is selected by floating or grounding the MODE pin, in which SPI programing is disabled. Figure 7-43 and Table 7-15 show the hardware pins and the pin functionality. Not all device options are available in hardware mode. See the *SPI Programming* section for details of SPI programming.

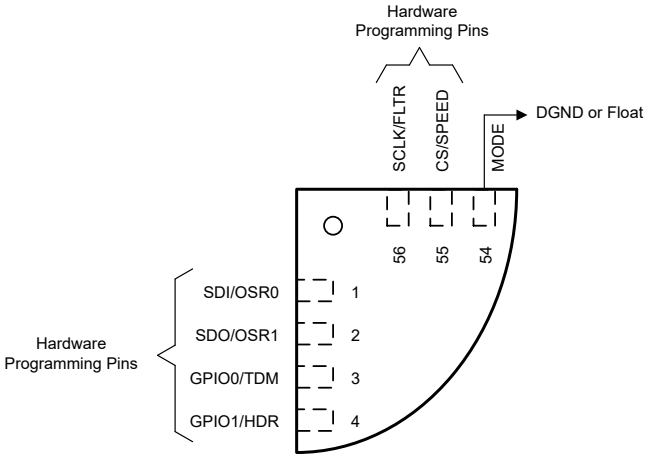


Figure 7-43. Hardware Programming Mode

Table 7-15. Hardware Programming Pins

PIN	NO.	DESCRIPTION	STATE[1]	FUNCTION		
MODE	54	SPI or hardware programming mode	0	Hardware programming, all buffers ON		
			1	SPI programming		
			F	Hardware programming, all buffers OFF		
$\overline{CS}$/SPEED	55	Speed mode	0	Low-speed mode		
			1	Max-speed mode		
			F	Mid-speed mode		
SCLK/FLTR	56	Filter type	0	Wideband filter		
			1	Low-latency sinc4 filter		
			F	Low-latency sinc4 + sinc1 filter		
SDO/OSR1 SDI/OSR0	2,1	Filter OSR	**OSR1/ OSR0**	**WIDEBAND FILTER**	**SINC4 FILTER**	**SINC4 + SINC1 FILTER**
			00	32	12	64
			01	64	16	128
			0F	128	24	320
			10	256	32	640
			11	512	64	1280
			1F	1024	128	3200
			F0	2048	256	6400
			F1	4096	1024	12800
			FF	4096	4096	32000
GPIO0/TDM	3	Data port TDM	0	No TDM, four or eight data lanes (all DOUT*x* pins are used)		
			1	ADS117L18: one data lane (DOUT0 pin)		
			F	ADS117L14: one data lane (DOUT0 pin) ADS117L18: two data lanes (DOUT0 and DOUT1 pins)		
GPIO1/HDR	4	Data-port header	0	16 data bits (only)		
			1	STATUS header byte + 16 data bits		
			F	STATUS header byte + 16 data bits + CRC byte		

1. F = float state.

The device reads the pins at power-up and at device reset by applying pulses through a weak driver (Z_{OUT} = 25kΩ). Make sure the pin levels are established prior to power-up or reset. If a floating condition is detected, the device drives the pin low to prevent the pin from floating during normal operation. After the pins are read, changes to the pins are not acknowledged until the next power up or reset cycle.

Because the device applies pulses to read the pins, the float-state condition limits the external pin capacitance and external leakage current. The logic 1 and 0 input conditions also limits the maximum pull-up and pull-down resistors. Figure 7-44 shows the electrical limits for each state. For proper pin mode detection, do not tie together floating inputs of other devices.

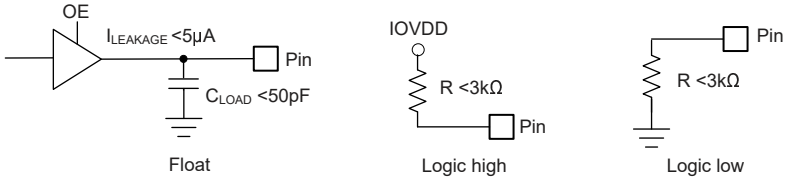


Figure 7-44. Hardware Programming Pin Conditions

Programming options not available in the hardware mode assume the SPI register default values. See the *Register Map* section for the default values. Table 7-16 shows the exceptions to the SPI defaults.

Table 7-16. Hardware Programming Default

FUNCTION	HARDWARE MODE DEFAULT
Clock mode	External clock
Reference range	High reference range
VCM output	Enabled

7.5.2 SPI Programming

SPI Programming is selected by tying the MODE pin to IOVDD. In SPI mode, the hardware mode is disabled and the device is programmed by writing to the SPI registers. Figure 7-45 shows the SPI pins.

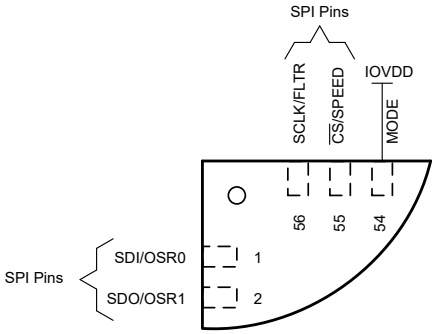


Figure 7-45. SPI Pins

The SPI consists of four signals: $\overline{CS}$, SCLK, SDI, and SDO (hardware pin functions are subsequently removed from the pin names). The interface operates in a passive mode where SCLK is an input to the device, driven by the host. The interface is compatible to SPI mode 1 (CPOL = 0 and CPHA = 1). In SPI mode 1, SCLK idles low, and data are updated on SCLK rising edges and read on SCLK falling edges. The interface supports full-duplex operation, meaning input data and output data are transmitted simultaneously.

An optional 8-bit CRC value validates data transmission between the host and the device. A 16-bit CRC register value detects register map changes after the initial register data are loaded.

7.5.2.1 Chip Select ($\overline{CS}$)

$\overline{CS}$ is an active-low input that enables the SPI for communication. Communication is started by taking $\overline{CS}$ low and is ended by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device ends communication by interpreting the last 16 bits of input data (24 bits in CRC mode). The device interprets the last bits regardless of the number of bits shifted in. When $\overline{CS}$ is high, the SPI interface resets, commands are blocked, and the SDO pin enters a high-impedance state.

7.5.2.2 Serial Clock (SCLK)

SCLK is the serial clock input that shifts register data into and out of the ADC. Output data update on the SCLK rising edge and input data are latched on the SCLK falling edge. SCLK is a Schmitt-triggered input designed to increase noise immunity. Even though SCLK is noise resistant, keep SCLK as noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. A series termination resistor placed at the SCLK driver often reduces ringing.

7.5.2.3 Serial Data Input (SDI)

SDI is the SPI data input. SDI is used to input data to the device. Data are latched on the SCLK falling edge. Idle SDI high or low when not active.

7.5.2.4 Serial Data Output (SDO)

SDO is the SPI data output. Output data from the ADC are updated on the SCLK rising edge. The SDO pin is tri-state when $\overline{CS}$ is high.

7.5.3 SPI Frame

Communication through the SPI is based on the concept of frames. A frame is started by taking $\overline{CS}$ low and is ended by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device interprets the last 16 or 24 bits of data (depending on configuration), regardless of the amount of data shifted in.

7.5.4 Commands

Commands are used to read and write register data to configure and control the device. Commands are two bytes long (plus an optional CRC byte). The *Register Map* is a series of 8-bit registers, accessible by read and write operations, one register access at a time. When SPI CRC is enabled, the device computes the CRC input value of the two bytes preceding the CRC byte to verify the command. Table 7-17 shows the command format.

Table 7-17. Commands

COMMAND	BYTE1	BYTE2	BYTE 3 (Optional CRC Mode)
Read register	00h + register address [6:0]	Don't care	CRC of byte 1 and byte 2
Write register	80h + register address [6:0]	Register data	CRC of byte 1 and byte 2

There is a special input bit pattern that directly resets the ADC. See the *Reset by SPI Input Pattern* section for details.

Table 7-18 summarizes the input and output byte sequence for read and write commands corresponding to the STATUS and CRC options. STATUS and CRC are enabled by setting the respective bits in the GEN_CFG3 register. The communication frame size is 2 or 3 bytes depending if CRC is enabled.

Table 7-18. SPI Frame Size

FRAME SIZE	STATUS	CRC	INPUT BYTE SEQUENCE	OUTPUT BYTE SEQUENCE(1)
2 bytes	no	no	Write Command: Command + Data Read Command: Command + 0	Write Command: ECHO + 0 Read Command: Data + 0
	yes	no		Write Command: ECHO + STATUS Read Command: Data + STATUS
3 bytes	no	yes	Write Command: Command + Data + CRC Read Command: Command + 0 + CRC	Write Command: ECHO + 0 + CRC Read Command: Data + 0 + CRC
	yes	yes		Write Command: ECHO + STATUS + CRC Read Command: Data + STATUS + CRC

(1) ECHO is the previous frame register-data byte of the write command echoed to the next frame

7.5.4.1 Write Register Command

The write register command writes register data. The write register operation is performed in one frame. The first byte of the command is the base value (80h) added to the 7-bit register address. The second byte of the command is the register data. When the address verification is enabled when out of range address occurs, the write operation is rejected and the ADDR_ERR flag is set in the STATUS byte. The register data format is MSB first.

Figure 7-46 shows an example of writing register data with STATUS and CRC disabled, resulting in a two-byte command operation. If the previous operation was a write register command, the first output byte is the echo of the previously written register data. Otherwise, the first output byte is the register data from the register read operation.

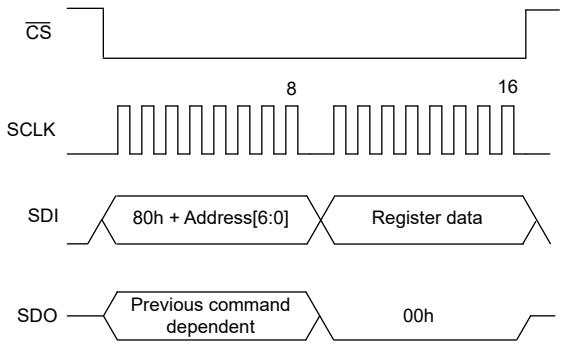


Figure 7-46. Write Register Data (STATUS and CRC Disabled)

Figure 7-47 shows an example of a write register operation with STATUS and CRC enabled. The frame is three bytes long because CRC is enabled. If the previous operation was a write register command, the first output byte is the echo of the previously written register data. If a CRC or out-of-range address error occurred in the previous frame, the write operation is rejected. The echo byte is then inverted, and the SPI_FLAG bit is set in the STATUS byte. Further register write operations are blocked until the SPI_FLAG is reset by writing 1b to clear. If the previous operation is a register read, the first output byte is the register data.

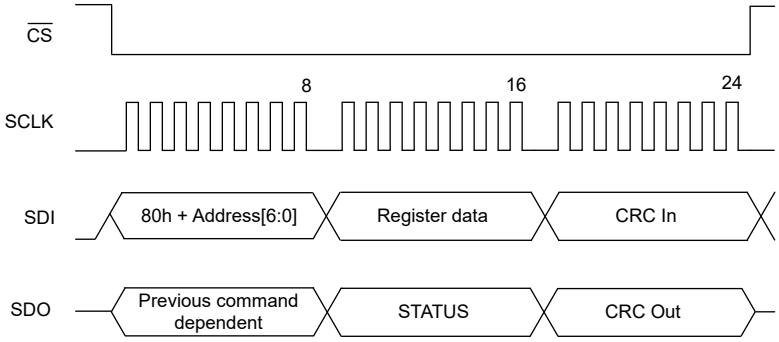


Figure 7-47. Write Register Data (STATUS and CRC Enabled)

7.5.4.2 Read Register Command

The read register command reads register data. The command follows an off-frame protocol where the read command is sent in one frame and the ADC responds with register data in the next frame. The first byte of the command is 00h plus the 7-bit register address. The second byte is unused. The response to a register address outside the valid range is 00h and if the SPI address range verification is enabled, the ADDR_ERR flag is set in the STATUS byte. The register data format is MSB first. Full duplex operation is possible by shifting in the next command while reading the current register data.

Figure 7-48 shows an example of reading register data with the STATUS and CRC bytes disabled. Frame 1 is the command frame and frame 2 is the data response frame. The frames are delimited by taking $\overline{CS}$ high. In this example, the length of the response frame is two bytes long because CRC is disabled. Optionally, short-cycle the response frame after the register data is read by taking $\overline{CS}$ high. A read from an invalid register returns zero for register data.

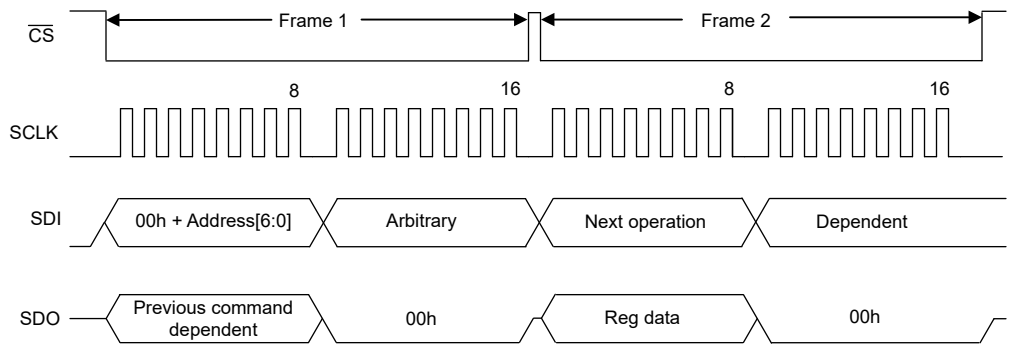


Figure 7-48. Read Register Data (STATUS and CRC Disabled)

Figure 7-49 shows an example of reading register data with STATUS and CRC enabled. The length of the frames are three bytes because CRC is enabled. The value of the second command byte is arbitrary, but is used with the first command byte to determine the *CRC In* value. The register data byte and the STATUS byte determine the *CRC Out* value.

If a CRC error occurred during the register read command, the SPI_ERR flag is set in STATUS. If an out-of-range address error occurred during the register read command, the register response data (Reg data) is zero and the ADDR_ERR flag is set in STATUS. In both cases, future reads are processed regardless whether error flags set or cleared.

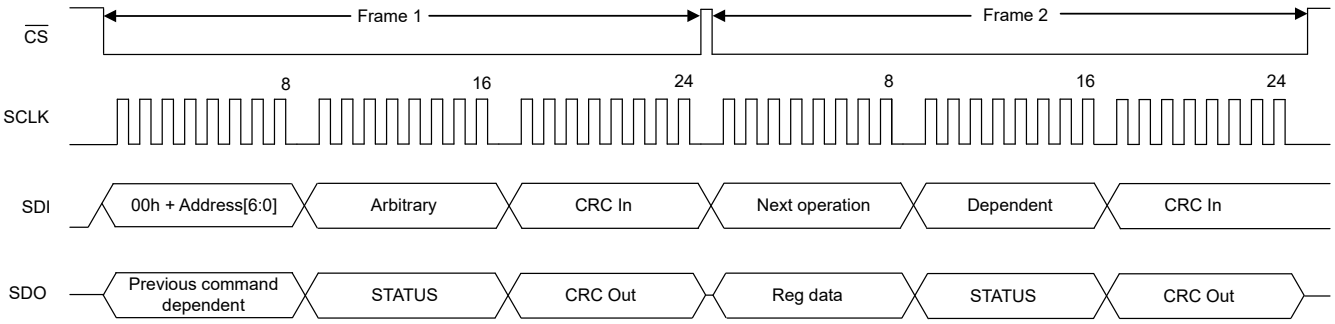


Figure 7-49. Read Register Data (STATUS and CRC Enabled)

7.5.5 SPI Daisy-Chain

The SPI supports daisy-chaining to connect multiple devices. For daisy-chain operation, connect the SDO pins to the SDI pins of the following devices. There is no special programming required, simply apply additional shift clocks to extend the frame length to access all devices in the chain. To input data, first shift in the data intended for the last device in the chain. The devices interpret the last two or three bytes of data prior to taking $\overline{CS}$ high (three bytes if CRC is enabled). Data is shifted out from the last device in the chain followed by data from the first device in the chain.

Figure 7-50 shows a two-device, daisy-chain connection and Figure 7-51 shows the data format for a register write commands for each device. The *Data Out* line of the controller connects to ADC (1) SDI and ADC (2) SDO connects to the *Data In* line of the controller. ADC (1) input data is shifted out on SDO to drive the ADC (2) SDI. The shift operation continues until the last device in the chain is reached. The SPI frame ends when $\overline{CS}$ is taken high, at which time the data shifted in to each device are interpreted. The second frame shifts out the register data from both devices through the ADC (2) SDO pin.

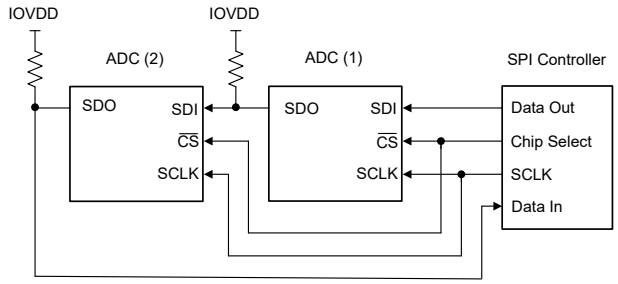


Figure 7-50. SPI Daisy-Chain

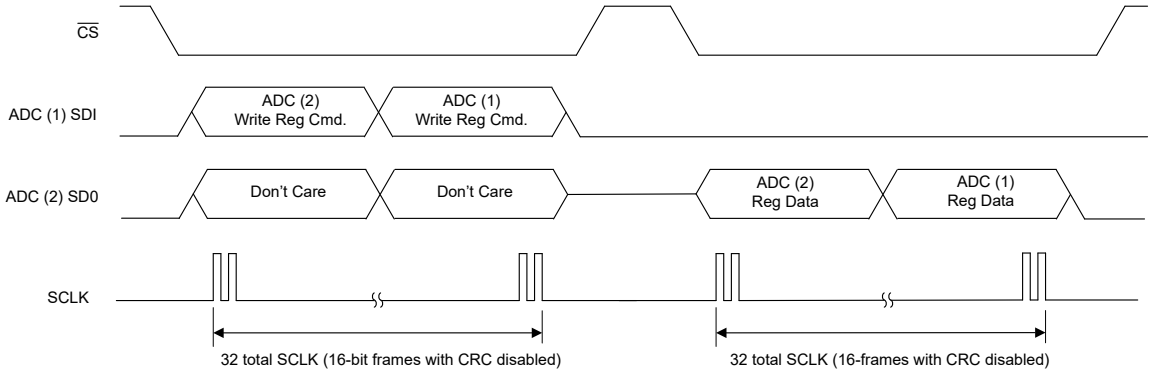


Figure 7-51. SPI Daisy-Chain Register Write Data Format

8 Register Map

Table 8-1 lists the register memory map of the ADS117L14 and ADS117L18. Memory addresses 02h to 10h are common programming to all device channels. Addresses 11h through 30h apply to device channels 0 through 3. Addresses 31h through 50h apply to device channels 4 through 7. Unlisted register addresses are not to be written to.

Table 8-1. Register Map Summary

Address	Register	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	DEV_ID	xxh	DEV_ID[7:0]							
01h	REV_ID	xxh	REV_ID[7:0]							
02h	STATUS	60h	RESERVED	ALV_FLAG	POR_FLAG	SPI_ERR	REG_ERR	ADC_ERR	ADDR_ERR	SCLK_ERR
03h	CLK_CNT	00h	CLK_CNT[7:0]							
04h	GPIO_RD	00h	GPIO_RD[7:0]							
05h	CRC_MSB	00h	CRC_MSB[7:0]							
06h	CRC_LSB	00h	CRC_LSB[7:0]							
07h	CONTROL	00h	RESET[5:0]						START	STOP
08h	GEN_CFG1	00h	RESERVED		DELAY[2:0]			VCM	REFP_BUF	REF_RNG
09h	GEN_CFG2	04h	RESERVED			START_MODE[1:0]		SPEED_MODE[1:0]		STBY_MODE
0Ah	GEN_CFG3	C0h	OUT_DRV	RESERVED	CLK_CNT_EN	SPI_STAT_EN	SPI_ADDR_EN	SCLK_CNT_EN	SPI_CRC_EN	REG_CRC_EN
0Bh	DP_CFG1	20h	DP_CRC_EN	DP_STAT_EN	DP_TDM[1:0]		RESERVED		DP_DAISY	RESERVED
0Ch	DP_CFG2	00h	RESERVED	DCLK_DIV[1:0]		DOUT_DLY[4:0]				
0Dh	CLK_CFG	00h	RESERVED				CLK_SEL	CLK_DIV[2:0]		
0Eh	GPIO_WR	00h	GPIO_WR[7:0]							
0Fh	GPIO_DIR	00h	GPIO_DIR[7:0]							
10h	GPIO_EN	00h	GPIO_EN[7:0]							
11h	CH0_CFG1	00h	CH0_FORMAT		CH0_MUX[2:0]		CH0_INP_RNG	CH0_EX_RNG	CH0_BUFN	CH0_BUFP
12h	CH0_CFG2	00h	RESERVED		CH0_PWDN	CH0_FLTR[4:0]				
13h	CH0_OFS_MSB	00h	CH0_OFFSET_MSB[7:0]							
14h	CH0_OFS_MID	00h	CH0_OFFSET_MID[7:0]							
15h	CH0_OFS_LSB	00h	CH0_OFFSET_LSB[7:0]							
16h	CH0_GAN_MSB	40h	CH0_GAIN_MSB[7:0]							
17h	CH0_GAN_MID	00h	CH0_GAIN_MID[7:0]							
18h	CH0_GAN_LSB	00h	CH0_GAIN_LSB[7:0]							
19h	CH1_CFG1	00h	CH1_FORMAT		CH1_MUX[2:0]		CH1_INP_RNG	CH1_EX_RNG	CH1_BUFN	CH1_BUFP
1Ah	CH1_CFG2	00h	RESERVED		CH1_PWDN	CH1_FLTR[4:0]				
1Bh	CH1_OFS_MSB	00h	CH1_OFFSET_MSB[7:0]							
1Ch	CH1_OFS_MID	00h	CH1_OFFSET_MID[7:0]							
1Dh	CH1_OFS_LSB	00h	CH1_OFFSET_LSB[7:0]							
1Eh	CH1_GAN_MSB	40h	CH1_GAIN_MSB[7:0]							
1Fh	CH1_GAN_MID	00h	CH1_GAIN_MID[7:0]							
20h	CH1_GAN_LSB	00h	CH1_GAIN_LSB[7:0]							
21h	CH2_CFG1	00h	CH2_FORMAT		CH2_MUX[2:0]		CH2_INP_RNG	CH2_EX_RNG	CH2_BUFN	CH2_BUFP
22h	CH2_CFG2	00h	RESERVED		CH2_PWDN	CH2_FLTR[4:0]				
23h	CH2_OFS_MSB	00h	CH2_OFFSET_MSB[7:0]							
24h	CH0_OFS_MID	00h	CH2_OFFSET_MID[7:0]							
25h	CH2_OFS_LSB	00h	CH2_OFFSET_LSB[7:0]							
26h	CH2_GAN_MSB	40h	CH2_GAIN_MSB[7:0]							
27h	CH2_GAN_MID	00h	CH2_GAIN_MID[7:0]							
28h	CH2_GAN_LSB	00h	CH2_GAIN_LSB[7:0]							
29h	CH3_CFG1	00h	CH3_FORMAT		CH3_MUX[2:0]		CH3_INP_RNG	CH3_EX_RNG	CH3_BUFN	CH3_BUFP
2Ah	CH3_CFG2	00h	RESERVED		CH3_PWDN	CH3_FLTR[4:0]				
2Bh	CH3_OFS_MSB	00h	CH3_OFFSET_MSB[7:0]							
2Ch	CH3_OFS_MID	00h	CH3_OFFSET_MID[7:0]							
2Dh	CH3_OFS_LSB	00h	CH3_OFFSET_LSB[7:0]							
2Eh	CH3_GAN_MSB	40h	CH3_GAIN_MSB[7:0]							
2Fh	CH3_GAN_MID	00h	CH3_GAIN_MID[7:0]							

Table 8-1. Register Map Summary (continued)

Address	Register	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30h	CH3_GAN_LSB	00h	CH3_GAIN_LSB[7:0]							
31h	CH4_CFG1	00h	CH4_FORMAT	CH4_MUX[2:0]			CH4_INP_RNG	CH4_EX_RNG	CH4_BUFN	CH4_BUFP
32h	CH4_CFG2	00h	RESERVED		CH4_PWDN	CH4_FLTR[4:0]				
33h	CH4_OFS_MSB	00h	CH4_OFFSET_MSB[7:0]							
34h	CH4_OFS_MID	00h	CH4_OFFSET_MID[7:0]							
35h	CH4_OFS_LSB	00h	CH4_OFFSET_LSB[7:0]							
36h	CH4_GAN_MSB	40h	CH4_GAIN_MSB[7:0]							
37h	CH4_GAN_MID	00h	CH4_GAIN_MID[7:0]							
38h	CH4_GAN_LSB	00h	CH4_GAIN_LSB[7:0]							
39h	CH5_CFG1	00h	CH5_FORMAT	CH5_MUX[2:0]			CH5_INP_RNG	CH5_EX_RNG	CH5_BUFN	CH5_BUFP
3Ah	CH5_CFG2	00h	RESERVED		CH5_PWDN	CH5_FLTR[4:0]				
3Bh	CH5_OFS_MSB	00h	CH5_OFFSET_MSB[7:0]							
3Ch	CH5_OFS_MID	00h	CH5_OFFSET_MID[7:0]							
3Dh	CH5_OFS_LSB	00h	CH5_OFFSET_LSB[7:0]							
3Eh	CH5_GAN_MSB	40h	CH5_GAIN_MSB[7:0]							
3Fh	CH5_GAN_MID	00h	CH5_GAIN_MID[7:0]							
40h	CH5_GAN_LSB	00h	CH5_GAIN_LSB[7:0]							
41h	CH6_CFG1	00h	CH6_FORMAT	CH6_MUX[2:0]			CH6_INP_RNG	CH6_EX_RNG	CH6_BUFN	CH6_BUFP
42h	CH6_CFG2	00h	RESERVED		CH6_PWDN	CH6_FLTR[4:0]				
43h	CH6_OFS_MSB	00h	CH6_OFFSET_MSB[7:0]							
44h	CH6_OFS_MID	00h	CH6_OFFSET_MID[7:0]							
45h	CH6_OFS_LSB	00h	CH6_OFFSET_LSB[7:0]							
46h	CH6_GAN_MSB	40h	CH6_GAIN_MSB[7:0]							
47h	CH6_GAN_MID	00h	CH6_GAIN_MID[7:0]							
48h	CH6_GAN_LSB	00h	CH6_GAIN_LSB[7:0]							
49h	CH7_CFG1	00h	CH7_FORMAT	CH7_MUX[2:0]			CH7_INP_RNG	CH7_EX_RNG	CH7_BUFN	CH7_BUFP
4Ah	CH7_CFG2	00h	RESERVED		CH7_PWDN	CH7_FLTR[4:0]				
4Bh	CH7_OFS_MSB	00h	CH7_OFFSET_MSB[7:0]							
4Ch	CH7_OFS_MID	00h	CH7_OFFSET_MID[7:0]							
4Dh	CH7_OFS_LSB	00h	CH7_OFFSET_LSB[7:0]							
4Eh	CH7_GAN_MSB	40h	CH7_GAIN_MSB[7:0]							
4Fh	CH7_GAN_MID	00h	CH7_GAIN_MID[7:0]							
50h	CH7_GAN_LSB	00h	CH7_GAIN_LSB[7:0]							

Table 8-2 shows the access-type codes in this section.

Table 8-2. Register Access-Type Codes

Access Type	Code	Description
R	R	Read only
W	W	Write only
W1C	W1C	Write 1 to clear
R/W	R/W	Read or write

8.1 DEV_ID Register (Address = 00h) [Reset = 04h or 06h]

DEV_ID is described in Table 8-3.

Table 8-3. DEV_ID Register Description

Bit	Field	Type	Reset	Description
7-0	DEV_ID[7:0]	R	00000xx0b	Device identification number. 00000101b = ADS117L14 00000111b = ADS117L18

8.2 REV_ID Register (Address = 01h) [Reset = xxh]

REV_ID is described in Table 8-4.

Table 8-4. REV_ID Register Description

Bit	Field	Type	Reset	Description
7-0	REV_ID[7:0]	R	xxxxxxxxb	Die revision number. The die revision number is subject to change during device production without prior notice.

8.3 STATUS Register (Address = 02h) [Reset = 60h]

STATUS is shown in Figure 8-1 and described in Table 8-5.

Figure 8-1. STATUS Register

7	6	5	4	3	2	1	0
RESERVED	ALV_FLAG	POR_FLAG	SPI_ERR	REG_ERR	ADC_ERR	ADDR_ERR	SCLK_ERR
R-0b	R/W1C-1b	R/W1C-1b	R/W1C-0b	R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b

Table 8-5. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	ALV_FLAG	R/W1C	1b	Analog supply low-voltage flag. This bit indicates a low-voltage condition of the analog power supplies. Write 1b to reset the flag to detect the next occurrence of a low-voltage condition. 0b = No event from when flag last cleared 1b = Analog power supply low-voltage detected
5	POR_FLAG	R/W1C	1b	Power-on reset flag. This bit indicates the device was reset at power-on or brownout of the IOVDD power supply or by a user reset operation. Write 1b to reset the flag to detect the next occurrence of a device reset. 0b = No reset from when flag last cleared 1b = Reset occurred
4	SPI_ERR	R/W1C	0b	SPI CRC error. This bit indicates an SPI CRC error was detected. Except for this register, register write operations are blocked when the bit is set. Clear the bit by writing 1b. CRC validation is enabled by the SPI_CRC_EN bit. 0b = No error 1b = SPI CRC error
3	REG_ERR	R/W1C	0b	Register map CRC error. This bit indicates a register map CRC error. The user writes a 16-bit CRC value to the CRC_MSB and CRC_LSB registers, calculated over addresses 08h to 50h for both devices. Clear the error by correcting the CRC value, then write 1b to clear the bit. The register map CRC validation is enabled by the REG_CRC_EN register bit. 0b = No error 1b = Register map CRC error

Table 8-5. STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ADC_ERR	R	0b	ADC error. This bit indicates an internal ADC error. Reset the device or perform a power cycle to clear the error. 0b = No error 1b = ADC error
1	ADDR_ERR	R/W1C	0b	SPI register address error. This bit indicates an invalid register read or write address. The valid address range is 00h to 50h for both devices. Except for the STATUS register, register write operations are blocked when the error is set. Clear the error by writing 1b. Address error check is enabled by setting SPI_ADDR_EN = 1b. 0b = No error 1b = Invalid register read/write address
0	SCLK_ERR	R/W1C	0b	SPI SCLK count error. This bit indicates the number of SCLK cycles was not a multiple of eight. Except for the STATUS register, register write operations are blocked when the flag is set. Clear the error by writing 1b. SCLK count error check is enabled by setting SCLK_CNT_EN = 1b. 0b = No error 1b = Number of SCLK clock cycles is not a multiple of eight

8.4 CLK_CNT Register (Address = 03h) [Reset = 00h]

CLK_CNT is described in Table 8-6.

Table 8-6. CLK_CNT Register Description

Bit	Field	Type	Reset	Description
7-0	CLK_CNT[7:0]	R	00000000b	Clock count value register. This register is a counter of the ADC clock. The counter increments at a rate of f_{CLK} / 32, divided by the CLK_DIV[2:0] setting. Read the register at known intervals to verify the ADC clock frequency. The clock count is enabled by the CLK_CNT_EN register bit. When enabled, the counter value resets to 00h. When disabled, the count value is 00h.

8.5 GPIO_RD Register (Address = 04h) [Reset = 00h]

GPIO_RD is shown in Figure 8-2 and described in Table 8-7.

Figure 8-2. GPIO_RD Register

7	6	5	4	3	2	1	0
GPIO_RD7	GPIO_RD6	GPIO_RD5	GPIO_RD4	GPIO_RD3	GPIO_RD2	GPIO_RD1	GPIO_RD0
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-7. GPIO_RD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPIO_RD[7:0]	R	00000000b	GPIO read data register. These bits are the read values of GPIO. If the GPIO is programmed as an output, the value returned is from the GPIO pin.

8.6 CRC_MSB, CRC_LSB Registers (Addresses = 05h, 06h) [Reset = 00h]

CRC registers described in Table 8-8.

Table 8-8. CRC Registers Description

Name	Address	Type	Reset	Description
CRC_MSB CRC_LSB	5h 6h	R/W R/W	00h 00h	Two-byte register map CRC value. Write a 16-bit CRC value, computed over the register range 08h to 50h. The register map CRC check is enabled by the REG_CRC_EN bit. The CRC error is reported to the REG_ERR bit of the STATUS register.

8.7 CONTROL Register (Address = 07h) [Reset = 00h]

CONTROL is shown in Figure 8-3 and described in Table 8-9.

Figure 8-3. CONTROL Register

7	6	5	4	3	2	1	0
RESET[5:0]						START	STOP
R/W-000000b						R/W-0b	R/W-0b

Table 8-9. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESET[5:0]	R/W	000000b	Software reset. Write the value of 010110b to reset the ADC. Make sure the START or STOP bits are also 0b in the same write operation. These bits self-clear and always read 000000b.
1	START	R/W	0b	START conversions. Start channel conversions by writing 1b. This bit also restarts an ongoing conversion. Conversions continue until 1b is written to the STOP bit. This bit self-clears after written, therefore always reads 0b. This bit is not functional in synchronized control mode. 0b = No operation 1b = Start or restart conversions
0	STOP	R/W	0b	Stop conversions. Stop channel conversions by writing 1b. This bit self-clears after written, therefore always reads 0b. This bit is not functional in synchronized control mode. 0b = No operation 1b = Stop conversions on all channels

8.8 GEN_CFG1 Register (Address = 08h) [Reset = 00h]

GEN_CFG1 is shown in Figure 8-4 and described in Table 8-10.

Figure 8-4. GEN_CFG1 Register

7	6	5	4	3	2	1	
RESERVED		DELAY[2:0]			VCM	REFP_BUF	REF_RNG
R-00b		R/W-000b			R/W-0b	R/W-0b	R/W-0b

Table 8-10. GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved.
5-3	DELAY[2:0]	R/W	000b	Conversion start delay time selection. Select the conversion start delay time in number of f_{MOD} cycles after taking START high (or setting the START bit). 000b = 0 001b = 4 010b = 8 011b = 16 100b = 32 101b = 128 110b = 512 111b = 1024
2	VCM	R/W	0b	Common-mode voltage output enable. This bit enables the common-mode voltage output of the VCM pin. The VCM output voltage is equal to (AVDD1 + AVSS) / 2. 0b = Disabled 1b = Enabled
1	REFP_BUF	R/W	0b	Reference positive buffer enable. This bit enables the REFP precharge buffers for all channels. 0b = Disabled 1b = Enabled
0	REF_RNG	R/W	0b	Voltage reference range selection. This bit selects the low or high voltage operating range of the reference input. Program the range to match the actual reference voltage. 0b = Low-voltage reference range 1b = High-voltage reference range

8.9 GEN_CFG2 Register (Address = 09h) [Reset = 04h]

GEN_CFG2 is shown in Figure 8-5 and described in Table 8-11.

Figure 8-5. GEN_CFG2 Register

7	6	5	4	3	2	1	0
RESERVED			START_MODE[1:0]		SPEED_MODE[1:0]		STBY_MODE
R-000b			R/W-00b		R/W-10b		R/W-0b

Table 8-11. GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	000b	Reserved
4-3	START_MODE[1:0]	R/W	00b	START mode selection. These bits program the functional mode of the START pin. See the *Synchronization* section for more details. 00b = Start/stop control mode 01b = Reserved 10b = Synchronized control mode 11b = Reserved
2-1	SPEED_MODE[1:0]	R/W	10b	Speed mode selection. These bits program the device speed mode. 00b = Low-speed mode (f_{CLK} = 3.2MHz) 01b = Mid-speed mode (f_{CLK} = 12.8MHz) 10b = High-speed mode (f_{CLK} = 25.6MHz) 11b = Max-speed mode (f_{CLK} = 32.768MHz)
0	STBY_MODE	R/W	0b	Standby mode selection. This bit enables the standby mode when conversions are stopped. Standby mode reduces power consumption compared to the idle mode. 0b = Idle mode, device fully powered 1b = Standby mode, analog section of channels powered down

8.10 GEN_CFG3 Register (Address = 0Ah) [Reset = 80h]

GEN_CFG3 is shown in Figure 8-6 and described in Table 8-12.

Figure 8-6. GEN_CFG3 Register

7	6	5	4	3	2	1	0
OUT_DRV	RESERVED	CLK_CNT_EN	SPI_STAT_EN	SPI_ADDR_EN	SCLK_CNT_EN	SPI_CRC_EN	REG_CRC_EN
R/W-1b	R-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-12. GEN_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_DRV	R/W	1b	Digital output drive selection. Select the digital output driver strength. Full drive strength increases the slew rate of the output signal. 0b = Full-power driver strength 1b = Half-power driver strength
6	RESERVED	R	1b	Reserved
5	CLK_CNT_EN	R/W	0b	Clock counter enable. This bit enables the ADC clock counter register. 0b = Disabled 1b = Enabled
4	SPI_STAT_EN	R/W	0b	SPI status byte output enable. This bit enables the STATUS register value in the SPI output. 0b = Disabled 1b = Enabled
3	SPI_ADDR_EN	R/W	0b	SPI register address enable. This bit enables the SPI address verification. The ADDR_ERR bit of the STATUS register sets if the register read or write address is invalid. 0b = Disabled 1b = Enabled
2	SCLK_CNT_EN	R/W	0b	SCLK count enable. This bit enables the SPI SCLK count verification. The SCLK_ERR bit of the STATUS register sets if the number of SCLK cycles in a frame are not multiples of 8. 0b = Disabled 1b = Enabled
1	SPI_CRC_EN	R/W	0b	SPI CRC enable. This bit enables the SPI CRC output byte and the input data CRC check. The SPI_ERR bit of the STATUS byte sets if the input CRC is in error. Write 1b to the SPI_ERR bit to clear the error. 0b = Disabled 1b = Enabled
0	REG_CRC_EN	R/W	0b	Register map CRC enable. This bit enables the register map CRC error verification. The REG_ERR bit of the STATUS byte sets if the CRC value is not correct. 0b = Disabled 1b = Enabled

8.11 DP_CFG1 Register (Address = 0Bh) [Reset = 20h]

DP_CFG1 is shown in Figure 8-7 and described in Table 8-13.

Figure 8-7. DP_CFG1 Register

7	6	5	4	3	2	1	0
DP_CRC_EN	DP_STAT_EN	DP_TDM[1:0]		RESERVED		DP_DAISY	RESERVED
R/W-0b	R/W-0b	R/W-10b		R-00b		R/W-0b	R-0b

Table 8-13. DP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DP_CRC_EN	R/W	0b	Data port CRC byte enable. This bit enables the data port CRC byte. A CRC byte is appended to the end of the channel data. 0b = Disabled 1b = Enabled
6	DP_STAT_EN	R/W	0b	Data port status byte enable. This bit enables the data port status byte. The status byte is prefixed to the beginning of the channel data. 0b = Disabled 1b = Enabled
5-4	DP_TDM[1:0]	R/W	10b	Data port time division multiplexing (TDM) configuration. These bits select the number of data lanes. See the *Time Division Multiplexing* section for details. 00b = One data lane 01b = One (ADS117L14) / two data lanes (ADS117L18) 10b = Two (ADS117L14) / four data lanes (ADS117L18) 11b = Four (ADS117L14) / eight data lanes (ADS117L18)
3-2	RESERVED	R	00b	Reserved.
1	DP_DAISY	R/W	0b	Data port daisy-chain mode. This bit selects daisy-chain or repeat data modes. 0b = TDM data mode. DINx data are shifted-in and appended to the original channel data. 1b = Repeat data mode. Original channel data are repeated and DINx data are ignored.
0	RESERVED	R	0b	Reserved.

8.12 DP_CFG2 Register (Address = 0Ch) [Reset = 00h]

DP_CFG2 is shown in Figure 8-8 and described in Table 8-14.

Figure 8-8. DP_CFG2 Register

7	6	5	4	3	2	1	0
RESERVED	DCLK_DIV[1:0]		DOUT_DLY[4:0]				
R-0b	R/W-00b		R/W-00000b				

Table 8-14. DP_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6-5	DCLK_DIV[1:0]	R/W	00b	Data port DCLK frequency divider. These bits select the frame-sync DCLK frequency. 00b = Divide by 1 01b = Divide by 2 10b = Divide by 4 11b = Divide by 8
4-0	DOUT_DLY[4:0]	R/W	00000b	Data port DOUTx delay. These bits select the delay or advance of the DOUTx signals relative to the DCLK and FSYNC signals. Positive values advance the DOUTx signals; negative values delay the DOUTx signals. The bit weight is approximately 0.3ns. See the Data Port Offset Timing section for details.

8.13 CLK_CFG Register (Address = 0Dh) [Reset = 00h]

CLK_CFG is shown in Figure 8-9 and described in Table 8-15.

Figure 8-9. CLK_CFG Register

7	6	5	4	3	2	1	0
RESERVED				CLK_SEL	CLK_DIV[2:0]		
R-0000b				R/W-0b	R/W-000b		

Table 8-15. CLK_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved.
3	CLK_SEL	R/W	0b	ADC clock selection. This bit selects the internal oscillator or external clock operation. 0b = Internal oscillator 1b = External clock
2-0	CLK_DIV[2:0]	R/W	000b	ADC clock divider. These bits select the clock signal divider for both external clock and internal oscillator. 000b = Divide by 1 001b = Divide by 2 010b = Divide by 3 011b = Divide by 4 100b - 111b = Divide by 8

8.14 GPIO_WR Register (Address = 0Eh) [Reset = 00h]

GPIO_WR is shown in Figure 8-10 and described in Table 8-16.

Figure 8-10. GPIO_WR Register

7	6	5	4	3	2	1	0
GPIO_WR7	GPIO_WR6	GPIO_WR5	GPIO_WR4	GPIO_WR3	GPIO_WR2	GPIO_WR1	GPIO_WR0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-16. GPIO_WR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPIO_WR[7:0]	R/W	00000000b	GPIO write data. This register is the GPIO write data register. Set the direction of the GPIO pins to output mode to write the value. See the GPIO_RD register to read GPIO data. 0b = GPIO pin is driven low 1b = GPIO pin is driven high

8.15 GPIO_DIR Register (Address = 0Fh) [Reset = 00h]

GPIO_DIR is shown in Figure 8-11 and described in Table 8-17.

Figure 8-11. GPIO_DIR Register

7	6	5	4	3	2	1	0
GPIO_DIR7	GPIO_DIR6	GPIO_DRI5	GPIO_DIR4	GPIO_DIR3	GPIO_DIR2	GPIO_DIR1	GPIO_DIR0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-17. GPIO_DIR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPIO_DIR[7:0]	R/W	00000000b	GPIO direction. This register programs the GPIO direction as inputs or outputs. 0b = The GPIO pin is an output 1b = The GPIO pin is an input

8.16 GPIO_EN Register (Address = 10h) [Reset = 00h]

GPIO_EN is shown in Figure 8-12 and described in Table 8-18.

Figure 8-12. GPIO_EN Register

7	6	5	4	3	2	1	0
GPIO_EN7	GPIO_EN6	GPIO_EN5	GPIO_EN4	GPIO_EN3	GPIO_EN2	GPIO_EN1	GPIO_EN0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-18. GPIO_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPIO_EN[7:0]	R/W	00000000b	GPIO enable. This register enables the GPIO function for each pin. When enabled, the GPIO pin function has priority over other pin functions. 0b = GPIO pin is disabled 1b = GPIO pin is enabled

8.17 CH*n*_CFG1 Registers (Address = Channel Number × 08h + 11h) [Reset = 00h]

Channel *n* configuration 1 register addresses are shown in Table 8-19. The register bit map is shown in Figure 8-13 and described in Table 8-20.

Table 8-19. CH*n*_CFG1 Register Addresses

NAME	DESCRIPTION	ADDRESS
CH0_CFG1	Channel 0 configuration 1	11h
CH1_CFG1	Channel 1 configuration 1	19h
CH2_CFG1	Channel 2 configuration 1	21h
CH3_CFG1	Channel 3 configuration 1	29h
CH4_CFG1	Channel 4 configuration 1	31h
CH5_CFG1	Channel 5 configuration 1	39h
CH6_CFG1	Channel 6 configuration 1	41h
CH7_CFG1	Channel 7 configuration 1	49h

Figure 8-13. CH*n*_CFG1 Register

7	6	5	4	3	2	1	0
CH*n*_FORMAT	CH*n*_MUX[2:0]			CH*n*_INP_RNG	CH*n*_EX_RNG	CH*n*_BUFN	CH*n*_BUFP
R/W-0b	R/W-000b			R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-20. CH*n*_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH*n*_FORMAT	R/W	0b	Data Format. This bit selects the data format. 0b = Two's complement format for positive and negative signals 1b = Straight binary format for positive signals only
6-4	CH*n*_MUX[2:0]	R/W	000b	Channel input multiplexer selection. These bits select between the signal input or input test modes. See the *Analog Inputs (AINP, AINN)* section for details. 000b = Normal input polarity 001b = Reverse input polarity 010b = Offset and noise test: Internal short to mid supply 011b = CMRR test to AINP 100b = CMRR test to AINN 101b = –FS test 110b = +FS test 111b = +FS test
3	CH*n*_INP_RNG	R/W	0b	Channel input range selection. This bit selects the 1x or 2x input range. See the *Input Range* section for more details. 0b = 1x input range 1b = 2x input range
2	CH*n*_EX_RNG	R/W	0b	Channel extended input range selection. This bit extends the input range by 25%. See the *Input Range* section for more details. 0b = Disabled 1b = Enabled: The FS range is extended by 25%
1	CH*n*_BUFN	R/W	0b	Channel analog input negative buffer enable. This bit enables the channel AINN precharge buffer. 0b = Disabled 1b = Enabled
0	CH*n*_BUFP	R/W	0b	Channel analog input positive buffer enable. This bit enables the channel AINP precharge buffer. 0b = Disabled 1b = Enabled

8.18 CH*n*_CFG2 Registers (Address = Channel Number × 08h + 12h) [Reset = 00h]

Channel *n* configuration 2 register addresses are shown in Table 8-21. The register bit map is shown in Figure 8-14 and described in Table 8-22.

Table 8-21. CH*n*_CFG2 Register Addresses

NAME	REGISTER DESCRIPTION	ADDRESS
CH0_CFG2	Channel 0 configuration 2	12h
CH1_CFG2	Channel 1 configuration 2	1Ah
CH2_CFG2	Channel 2 configuration 2	22h
CH3_CFG2	Channel 3 configuration 2	2Ah
CH4_CFG2	Channel 4 configuration 2	32h
CH5_CFG2	Channel 5 configuration 2	3Ah
CH6_CFG2	Channel 6 configuration 2	42h
CH7_CFG2	Channel 7 configuration 2	4Ah

Figure 8-14. CH*n*_CFG2 Register

7	6	5	4	3	2	1	0
RESERVED		CH*n*_PWDN	CH*n*_FLTR[4:0]				
R-00b		R/W-0b	R/W-00000b				

Table 8-22. CH*n*_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved.
5	CH*n*_PWDN	R/W	0b	Channel power-down mode selection. When set, the ADC channel is powered down. When powered down, channel data are the last remaining data. 0b = Active 1b = Powered down

Table 8-22. CH*n*_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CH*n*_FLTR[4:0]	R/W	00000b	Channel digital filter and data rate selection. These bits configure the digital filter and data rate for each channel. The data rate between channels must be related by power of 2. The device has five filter configurations: wideband, sinc4, sinc4 + sinc1, sinc3, and sinc3 + sinc1. See the Digital Filter section for the data rate corresponding to the OSR. 00000b = Wideband: OSR = 32 00001b = Wideband: OSR = 64 00010b = Wideband: OSR = 128 00011b = Wideband: OSR = 256 00100b = Wideband: OSR = 512 00101b = Wideband: OSR = 1024 00110b = Wideband: OSR = 2048 00111b = Wideband: OSR = 4096 01000b = Sinc4: OSR = 12 01001b = Sinc4: OSR = 16 01010b = Sinc4: OSR = 24 01011b = Sinc4: OSR = 32 01100b = Sinc4: OSR = 64 01101b = Sinc4: OSR = 128 01110b = Sinc4: OSR = 256 01111b = Sinc4: OSR = 512 10000b = Sinc4: OSR = 1024 10001b = Sinc4: OSR = 2048 10010b = Sinc4: OSR = 4096 10011b = Sinc4: OSR = 32 + sinc1: OSR = 2 10100b = Sinc4: OSR = 32 + sinc1: OSR = 4 10101b = Sinc4: OSR = 32 + sinc1: OSR = 10 10110b = Sinc4: OSR = 32 + sinc1: OSR = 20 10111b = Sinc4: OSR = 32 + sinc1: OSR = 40 11000b = Sinc4: OSR = 32 + sinc1: OSR = 100 11001b = Sinc4: OSR = 32 + sinc1: OSR = 200 11010b = Sinc4: OSR = 32 + sinc1: OSR = 400 11011b = Sinc4: OSR = 32 + sinc1: OSR = 1000 11100b = Sinc3: OSR = 26667 11101b = Sinc3: OSR = 32000 11110b = Sinc3: OSR = 32000 + sinc1: OSR = 3 11111b = Sinc3: OSR = 32000 + sinc1: OSR = 5

8.19 CH*n* Offset Registers [Reset = 000000h]

Channel *n* offset registers are described in Table 8-23.

Table 8-23. CH*n* Offset Registers Description

NAME	ADDRESS			TYPE	RESET	DESCRIPTION
	MSB	MID	LSB			
Channel 0 offset	13h	14h	15h	R/W	000000h	Three-byte offset word. Three registers form the 24-bit offset calibration word for each channel. The offset value is in two's-complement representation and is subtracted from the conversion result. The offset operation precedes the gain operation. Conversion data are left-justified to align with the offset value.
Channel 1 offset	1Bh	1Ch	1Dh			
Channel 2 offset	23h	24h	25h			
Channel 3 offset	2Bh	2Ch	2Dh			
Channel 4 offset	33h	34h	35h			
Channel 5 offset	3Bh	3Ch	3Dh			
Channel 6 offset	43h	44h	45h			
Channel 7 offset	4Bh	4Ch	4Dh			

8.20 CH*n* Gain Registers [Reset = 400000h]

Channel *n* gain registers are described in Table 8-24.

Table 8-24. CH*n* Gain Registers Description

NAME	ADDRESS			TYPE	RESET	DESCRIPTION
	MSB	MID	LSB			
Channel 0 gain	16h	17h	18h	R/W	400000h	These registers are three-byte gain registers. Three registers form the 24-bit gain calibration word of each channel. The gain value is in straight-binary representation and is normalized to 400000h for gain = 1. The conversion data are multiplied by GAIN[23:0] / 400000h after the offset operation.
Channel 1 gain	1Eh	1Fh	20h			
Channel 2 gain	26h	27h	28h			
Channel 3 gain	2Eh	2Fh	30h			
Channel 4 gain	36h	37h	38h			
Channel 5 gain	3Eh	3Fh	40h			
Channel 6 gain	46h	47h	48h			
Channel 7 gain	4Eh	4Fh	50h			

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The performance capability of the ADS117L1x devices is achievable when familiar with the requirements of the input driver, anti-alias filter, reference voltage, bypass capacitors, and PCB layout. The following sections provide design guidelines.

9.1.1 Input Driver

The input precharge buffers reduce the kick-back voltage caused by the ADC sampling capacitor. Reducing the kick-back improves linearity performance and relaxes the bandwidth requirements of the signal driver. Generally, the buffers provides the greatest benefit for input driver bandwidths of 10MHz or less. For higher bandwidth drivers, disabling the precharge buffers is optional to reduce power consumption. However, full-rated THD data sheet performance is realized when the buffers are used for input drivers below 150MHz. Slower ADC speed modes operate the modulator at slower clock rates, thus the driver has more time to settle between modulator input samples. See the related single-channel ADC *THP210 and ADS127L11 Performance* application note for details of the THP210 driver performance.

9.1.2 Anti-alias Filter

Input signals occurring near the modulator sampling rate (f_{MOD}) alias to the pass band resulting in data errors. When aliased, the errors cannot be removed by post processing. If these signals are present, an analog low-pass filter at the ADC input removes the out-of-band frequencies to reduce aliasing. The order of the anti-alias filter depends on the OSR value and the desired level of attenuation. Large values of OSR provide large frequency ranges between the Nyquist frequency and f_{MOD} for the filter to attenuate the signal. For example, for OSR = 128, more than two decades of frequency separate f_{DATA} and f_{MOD}. With a corner frequency = f_{DATA}, a third-order, 60dB per decade filter provides a 120dB alias rejection at f_{MOD}.

9.1.3 Reference Voltage

To meet data sheet performance, a reference voltage with low noise and sufficient drive strength that settles the sampled reference input is required. Incomplete settling of the reference voltage appears as a gain error to the system. In extreme cases of poor reference settling, device linearity is affected. The reference precharge buffer for the positive input significantly reduces the reference input charge leading to low gain error. See the Power Supply Recommendations section for the reference input bypass capacitor.

9.2 Typical Application

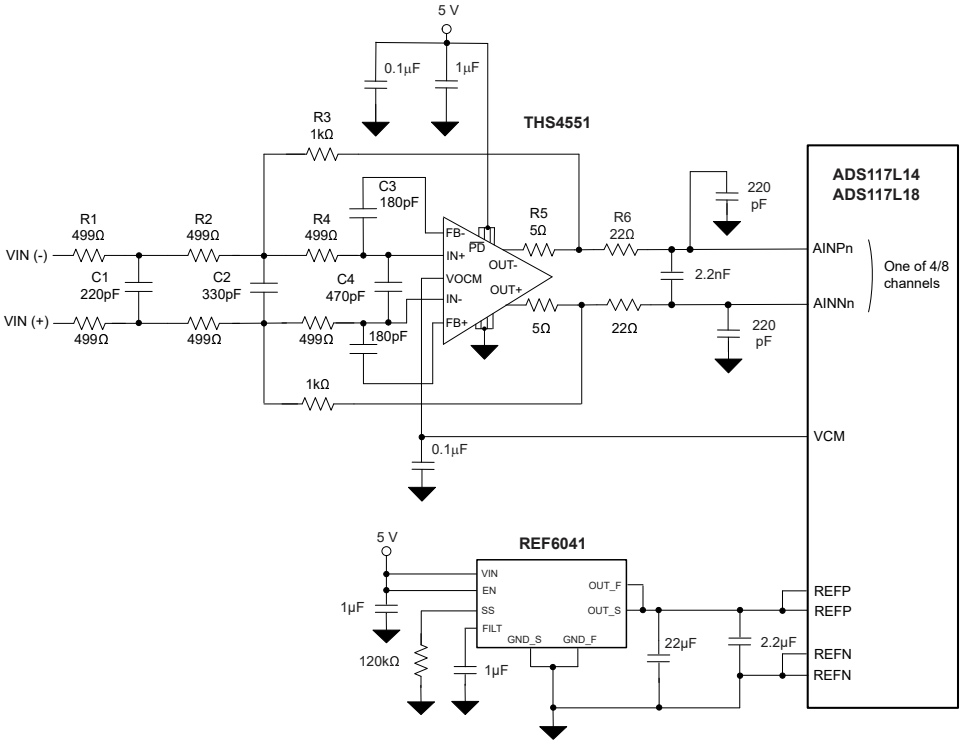


Figure 9-1. Input Signal Anti-alias Filter and Reference Voltage

9.2.1 Design Requirements

Figure 9-1 shows an input anti-alias filter using the THS4551 fully-differential input signal driver. The goal of this design is an anti-alias filter at the ADC input to attenuate out-of-band signals at the modulator sample rate (f_{MOD}). The filter requirement is 90dB attenuation at the f_{MOD} frequency (12.8MHz in high-speed mode) using OSR = 32 (f_{DATA} = 400kHz) in wideband filter mode. The other filter design goals are flat amplitude response and low group delay error within the pass band of the signal.

Table 9-1 lists the target design values and the actual values achieved in this design.

Table 9-1. Anti-alias Filter Design Requirements

FILTER PARAMETER	TARGET VALUE	ACTUAL VALUE
Voltage gain	0dB	0dB
Alias rejection at 12.8MHz	90dB	90dB
–0.1dB frequency	250kHz	260kHz
–3dB frequency	500kHz	550kHz
Pass-band amplitude peaking	20mdB	12mdB
Group delay linearity	0.1µs	0.017µs
Total noise of the filter and ADC (165kHz bandwidth)	12µV	11.8µV

9.2.2 Detailed Design Procedure

The anti-alias filter consists of a passive first-order input filter, an active second-order filter, and a passive first-order output filter. The filter is fourth-order overall. The filter design accommodates the worst-case wideband filter OSR value (32). This worst-case value results in less than two decades of frequency range between the Nyquist frequency at f_{DATA} and the f_{MOD} frequency. The fourth-order filter provides 90dB roll-off over this frequency range. The roll-off at f_{MOD} is the key requirement of the filter.

The THS4551 amplifier is selected for the active filter stage because of the 135MHz gain-bandwidth product and 50ns settling time. The amplifier GBP is sufficient to maintain flat passband response and stable filter roll-off at 12.8MHz. A 10MHz amplifier used with gain has marginal GBP to fully support the required roll-off at the f_{MOD} frequency.

The design of the active filter section begins with an equal-R assumption to reduce the number of component values to select. The dc gain of the filter is R_3 / (R_1 + R_2). The 1kΩ resistors are low enough in value to keep resistor noise and amplifier input current noise from affecting the noise of the ADC.

The 1kΩ input resistor is divided into two 499Ω resistors (R_1 and R_2) to implement the first-order filter using C_1. The first-order filter is decoupled from the second-order active filter, but shares R_1 and R_2 to determine each filter stage corner frequency. The corner frequency is given by C_1 and the Thevenin resistance at the terminals of C_1 (R_{TH} = 2 × 250Ω).

Assuming an arbitrary selection for R_4 (2 × 499Ω) is used for this design. Calculate the values of the 2 × 180pF (C3) feedback capacitors and the single 330pF differential capacitor (C2). These values are calculated by the filter design equations given in the *Design Methodology for MFB Filters in ADC Interface Applications* application note. The design inputs are filter f_O and filter Q for the multiple-feedback active-filter topology. The differential capacitor (C_4) is not part of the filter design but improves filter phase margin. The 5Ω resistors (R_5) isolate the amplifier outputs from stray capacitance to further improve filter phase margin.

The final RC filter at the ADC inputs serves two purposes. First, the filter provides a fourth pole to the overall filter response, thereby increasing roll-off. The other purpose of the RC filter at the inputs is a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand of the amplifier, maintaining low distortion and low gain error that otherwise degrades from incomplete amplifier settling. The input filter values are 2 × 22Ω and 2.2nF. The 22Ω resistors are outside the THS4551 filter loop to isolate the amplifier outputs from the 2.2nF capacitor to maintain phase margin.

Low voltage-coefficient C0G capacitors are used everywhere in the signal path for the low distortion properties. The amplifier gain resistors are 0.1% tolerance to provide best possible THD performance. The ADC VCM output connection to the amplifier VOCM input pin is optional because the same function is provided by the amplifier.

See the THS4551 data sheet for additional examples of active filter design and applications.

9.2.3 Application Curves

The following figures are produced by the TINA-TI™, SPICE-based analog simulation program. Download the THS4551 SPICE model at the THS4551 product folder.

Figure 9-2 shows the frequency response of the anti-alias filter and the *total* response of the anti-alias filter and ADC. As shown in this image, the filter provides 90dB stop-band attenuation from the Nyquist frequency to the 12.8MHz f_{MOD} frequency.

Figure 9-3 shows the analog filter group delay. The 0.575µs group delay is small in comparison to the 85µs group delay of the ADC digital filter (34 / f_{DATA}). The analog filter group delay linearity is 0.017µs, peaking at the edge of the 165kHz pass band.

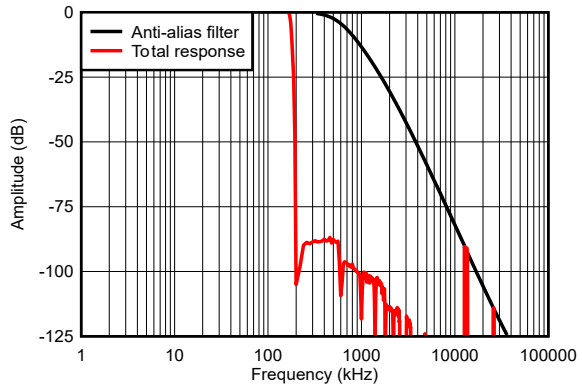


Figure 9-2. Anti-alias Filter Frequency Response

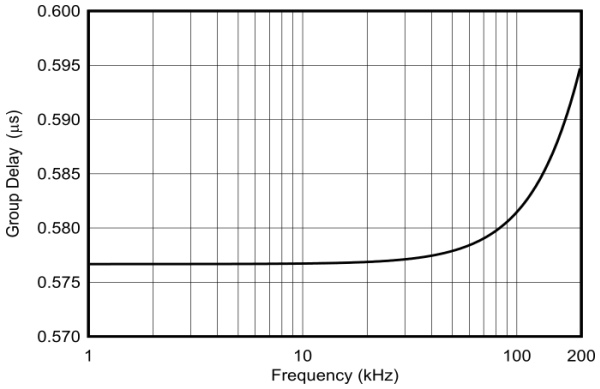


Figure 9-3. Anti-alias Filter Group Delay

Figure 9-4 shows the noise density of the anti-alias filter circuit, the noise density of the ADC, and the combined noise density of the filter and ADC. Noise density is the noise voltage per $\sqrt{Hz}$ of bandwidth plotted versus frequency.

Figure 9-5 shows the total noise from the 1Hz start frequency up to the ADC final bandwidth. Below 200Hz, noise is dominated by 1 / f voltage and current noise of the THS4551 amplifier. Above 200Hz, noise is dominated by ADC noise. The integrated noise of the filter and ADC over the 165kHz bandwidth is 11.8µV, meeting the 12µV target value.

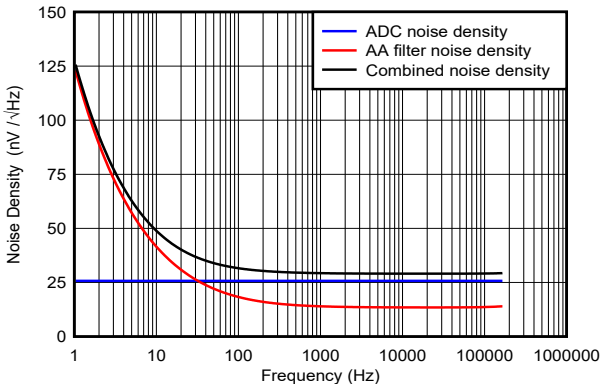


Figure 9-4. Noise Density

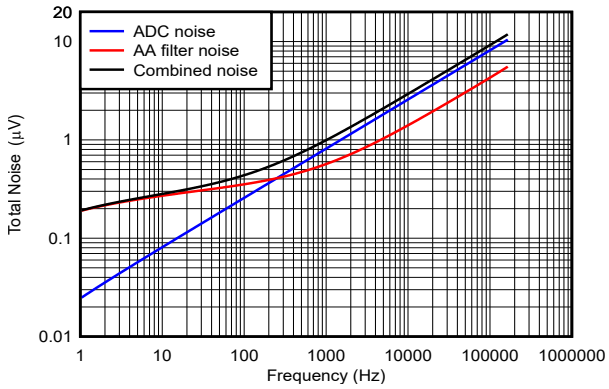


Figure 9-5. Total Noise

9.3 Power Supply Recommendations

The ADCs have three analog power supplies and one digital power supply. Power-supply voltages AVDD1 and AVSS configure the channels for unipolar or bipolar signal types. Example configurations are AVDD1 = 5V and AVSS = DGND for unipolar signals, and AVDD1 = 2.5V and AVSS = –2.5V for bipolar signals. The AVDD2 power-supply voltage is with respect to AVSS and the IOVDD power-supply voltage is with respect to DGND. The specified range of the power supplies are listed in the *Recommended Operating Conditions* section.

Table 9-2 shows power-supply configuration options. The power-supply voltage values shown are nominal.

Table 9-2. Power-Supply Configurations (Nominal)

SPEED MODE	CONFIGURATION	AVDD1 – DGND	AVSS – DGND	AVDD2 – DGND	IOVDD – DGND
Max speed	Unipolar	5V	0V	1.8V to 5V	1.8V
	Bipolar	2.5V	–2.5V	0V to 2.5V	1.8V
High speed	Unipolar	5V	0V	1.8V to 5V	1.8V
	Bipolar	2.5V	–2.5V	0V to 2.5V	1.8V
Mid speed	Unipolar	3.3V to 5V	0V	1.8V to 5V	1.8V
	Bipolar	1.65V to 2.5V	–1.65V to –2.5V	0.15V to 2.5V	1.8V
Low speed	Unipolar	3V to 5V	0V	1.8V to 5V	1.8V
	Bipolar	1.5V to 2.5V	–1.5V to –2.5V	0.3V to 2.5V	1.8V

The power supplies do not require special sequencing and are able to be powered up in any order and are tolerant to slow or fast ramp rates. However, make sure no analog or digital input exceeds the respective AVDD1 and AVSS (analog) or IOVDD (digital) power-supply voltages. An internal reset is performed after the IOVDD power-supply voltage is applied.

Table 9-3 shows the recommended bypass capacitors for the devices. All capacitors are minimum 6.3V, X7R ceramic dielectric. In addition to using a single ground plane for DGND, best performance is achieved with power planes for IOVDD, AVDD1, AVDD2, and AVSS. If AVSS = 0V for unipolar supply operation, use one ground plane for AVSS and DGND. If AVSS = -2.5V for bipolar supply operation, bypass AVSS and AVDD1 to the DGND plane.

For both the ADS117L14 and the ADS117L18, AVSS pin numbers 45 and 51 do not require bypass capacitors. In addition, the ADS117L14 AVSS pin numbers 29 through 36 do not require bypass capacitors. Tie these pins to the AVSS plane.

Table 9-3. Bypass Capacitors

POSITIVE PINS	NEGATIVE PINS	CAPACITOR (X7R)
IOVDD (pins 18, 19 tied together)	DGND (pin17)	2.2uF
CAPD (pin 20)	DGND (pin 21)	2.2uF
AVDD1 (pins 23, 24 tied together)	AVSS (pin 22)	2.2uF
AVDD2 (pin 25)	AVSS (pin 22)	2.2uF
CAPA (pins 26, 27 tied together)	AVSS (pin 28)	10uF
REFP (pins 49, 50 tied together)	REFN (pins 47, 48 tied together)	2.2µF (REFP buffer on), 10uF (REFP buffer off)
REFN (pins 47, 48 tied together)	AVSS (pins 45, 51 tied together)	2.2µF (only required if REFN is not tied to ground)

9.3.1 AVDD1 and AVSS

AVDD1 and AVSS are analog supply voltages that power the precharge buffers and the modulator sampling switches. Configure the ADC for bipolar operation (such as ±2.5V power supplies), or for unipolar operation (such as AVDD1 = 5V and AVSS = DGND). The mid- and low-speed operating modes offer the option of reducing AVDD1. See the Section 5.3 section for details.

9.3.2 AVDD2

AVDD2 is an analog supply voltage that powers the modulator core. To simplify the number of power supplies, connect AVDD2 to AVDD1, or operate AVDD2 at a reduced voltage to lower power consumption.

9.3.3 IOVDD

IOVDD is the digital power-supply voltage for the device I/O pins. IOVDD is also internally regulated to power the digital core. The voltage level of IOVDD is independent of the analog supply configuration.

9.3.4 CAPA and CAPD

CAPA and CAPD are the output voltages of the internal voltage regulators. These voltages are for internal operation and are not designed to drive external loads. These pins require external bypass capacitors as shown in Table 9-3.

9.4 Layout

9.4.1 Layout Guidelines

To achieve data sheet performance, use a minimum four-layer PCB board with the inner layers dedicated to ground and power planes. Use one or more power planes to route the power supplies to the ADC. Best performance is achieved by combining the analog and digital grounds in a single, unbroken ground plane. In some layout geometries, however, separate analog and digital grounds are necessary to direct digital currents away from the analog ground. Noisy digital currents include pulsing LED indicators, relays, and so on. In this case, consider separate ground return paths for these digital currents. When separate analog and digital grounds are used, join the grounds at the ADC.

The top and bottom layers route the analog and digital signals. Route the input signal as a matched differential pair throughout the signal chain to reduce differential noise coupling. Avoid crossing or adjacent placement of digital signals with the analog signals. Separate the ADC clock input signal from SPI, frame-sync signals and other clock signals to avoid coupling which can cause jitter.

Place the voltage reference close to the ADC. Orient the reference such that the reference ground pin is close to the ADC REFN pins with a direct connection from the ADC REFN to the reference ground pin. Place the reference input capacitor close to the ADC reference input pins. Place the signal input bypass capacitors close to the ADC inputs. Optimize the location of the differential input capacitor over the location of the capacitors from each input to ground.

Figure 9-6 shows an ADS117L18 layout example with SPI connections. The analog input differential capacitors are 2.2nF C0G dielectric. The analog input common-mode capacitors are 220pF C0G dielectric. The differential input capacitors are placed close to the analog input pins. The input drivers are shown on the top and bottom sides of the PCB to conserve space.

10Ω resistors are used in series with the digital outputs to augment the 40Ω driver output impedance to reduce the potential for ringing in the PCB trace. Pull-down resistors are used for the DOUTx/DINx/GPIOx pins (pins 10 through 13) to prevent the pins from floating in the event they are programmed for inputs.

9.4.2 Layout Example

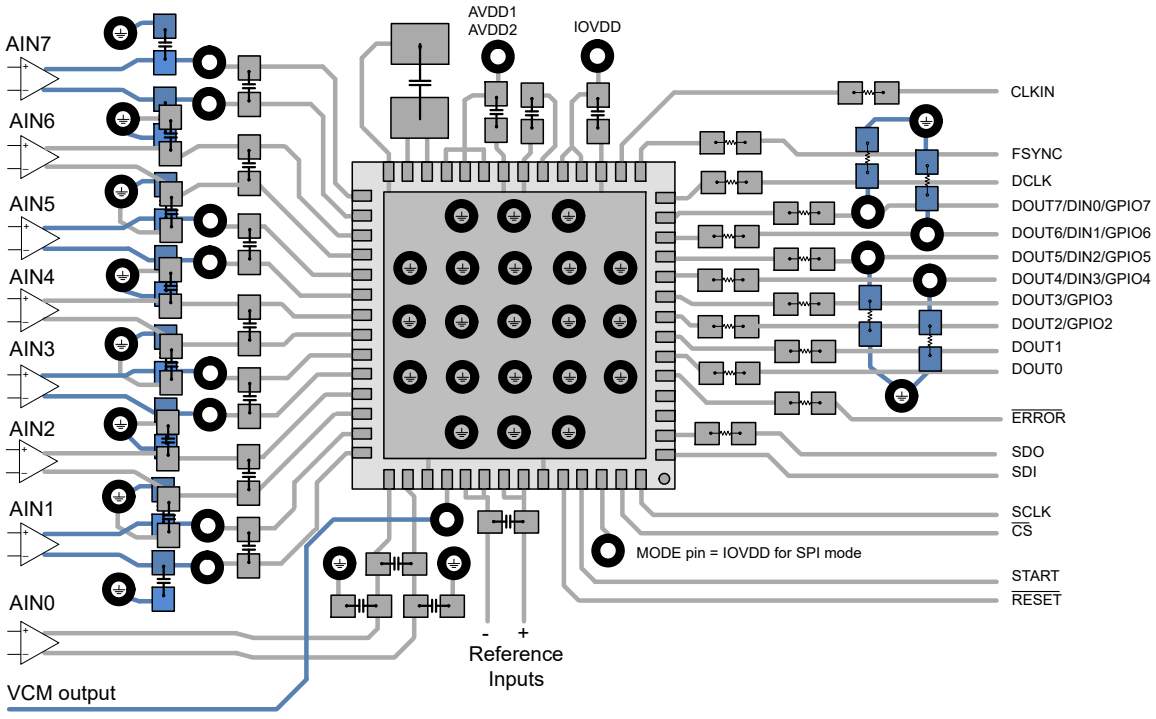


Figure 9-6. ADS117L18 PCB Layout Example

See the *QFN and SON PCB Attachment* application note for details of attaching the VQFN package to the printed circuit board.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *THP210 and ADS127L11 Performance* application note
- Texas Instruments, *ADS127L11 Design Calculator*
- Texas Instruments, *IEPE Vibration Sensor Interface Reference Design for PLC Analog Input* design guide
- Texas Instruments, *THS4551 Low-Noise, Precision, 150-MHz, Fully Differential Amplifier* data sheet
- Texas Instruments, *REF60xx High-Precision Voltage Reference with Integrated ADC Drive Buffer* data sheet
- Texas Instruments, *Design Methodology for MFB Filters in ADC Interface Applications* application note
- Texas Instruments, *QFN and SON PCB Attachment* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS117L14IRSHR	Active	Production	VQFN (RSH) | 56	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS117L14
ADS117L18IRSHR	Active	Production	VQFN (RSH) | 56	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS117L18

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

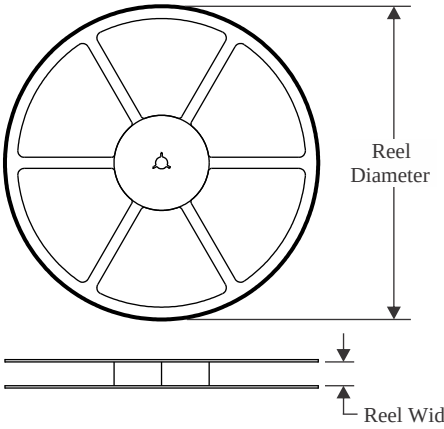
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

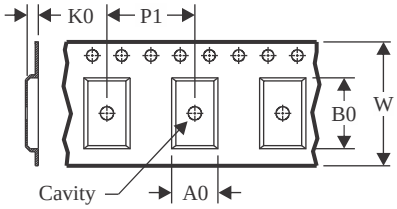
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

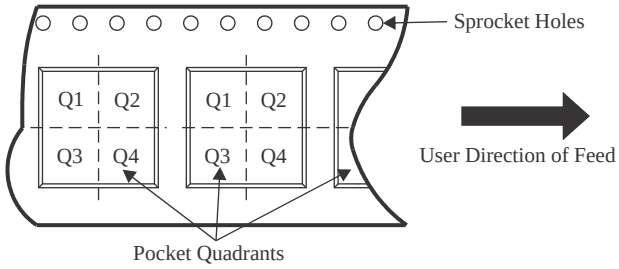


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

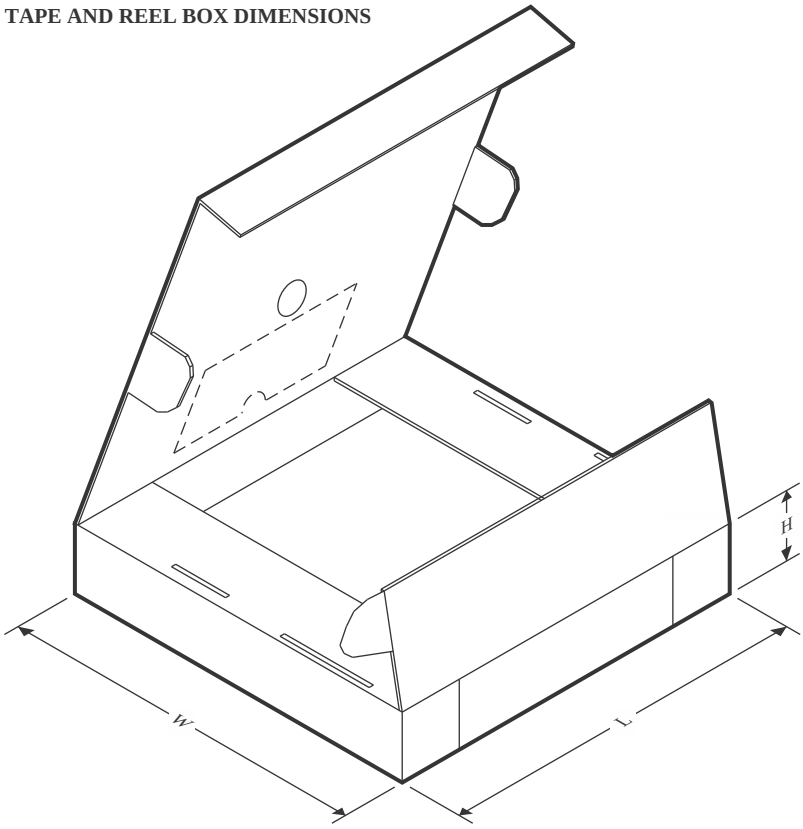
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS117L14IRSHR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
ADS117L18IRSHR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

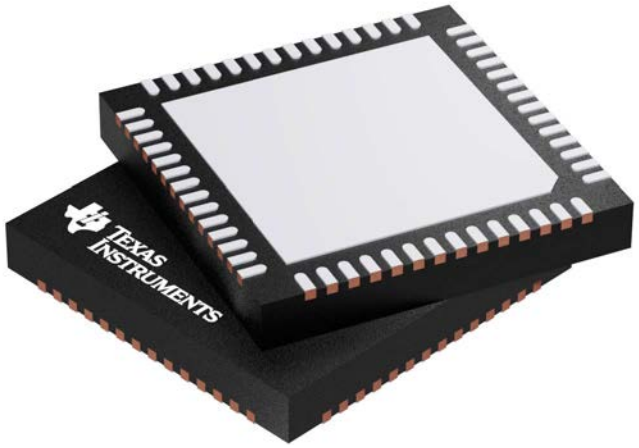
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS117L14IRSHR	VQFN	RSH	56	2500	367.0	367.0	35.0
ADS117L18IRSHR	VQFN	RSH	56	2500	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RSH 56

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

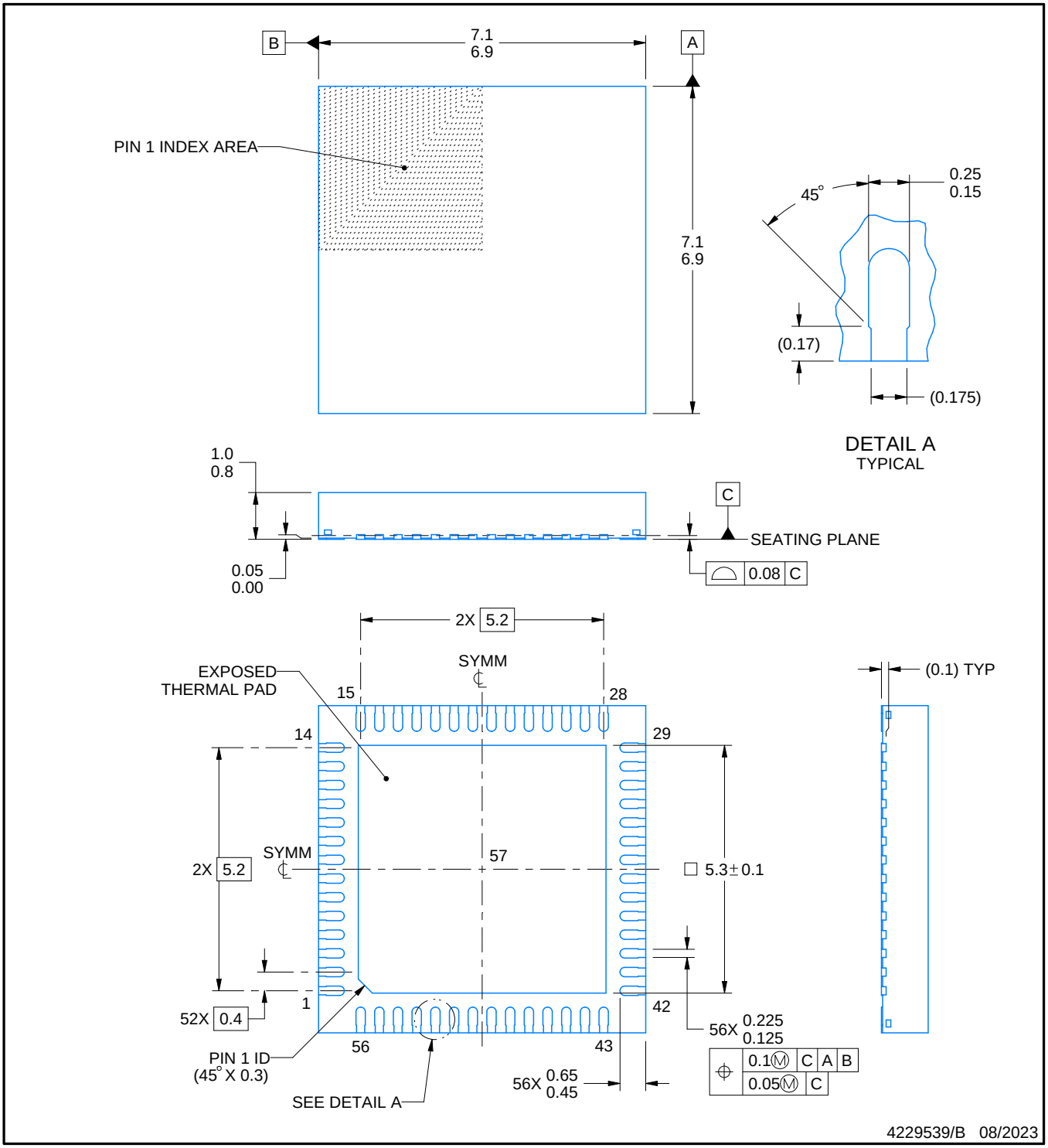
4207513/D

RSH0056G

PACKAGE OUTLINE

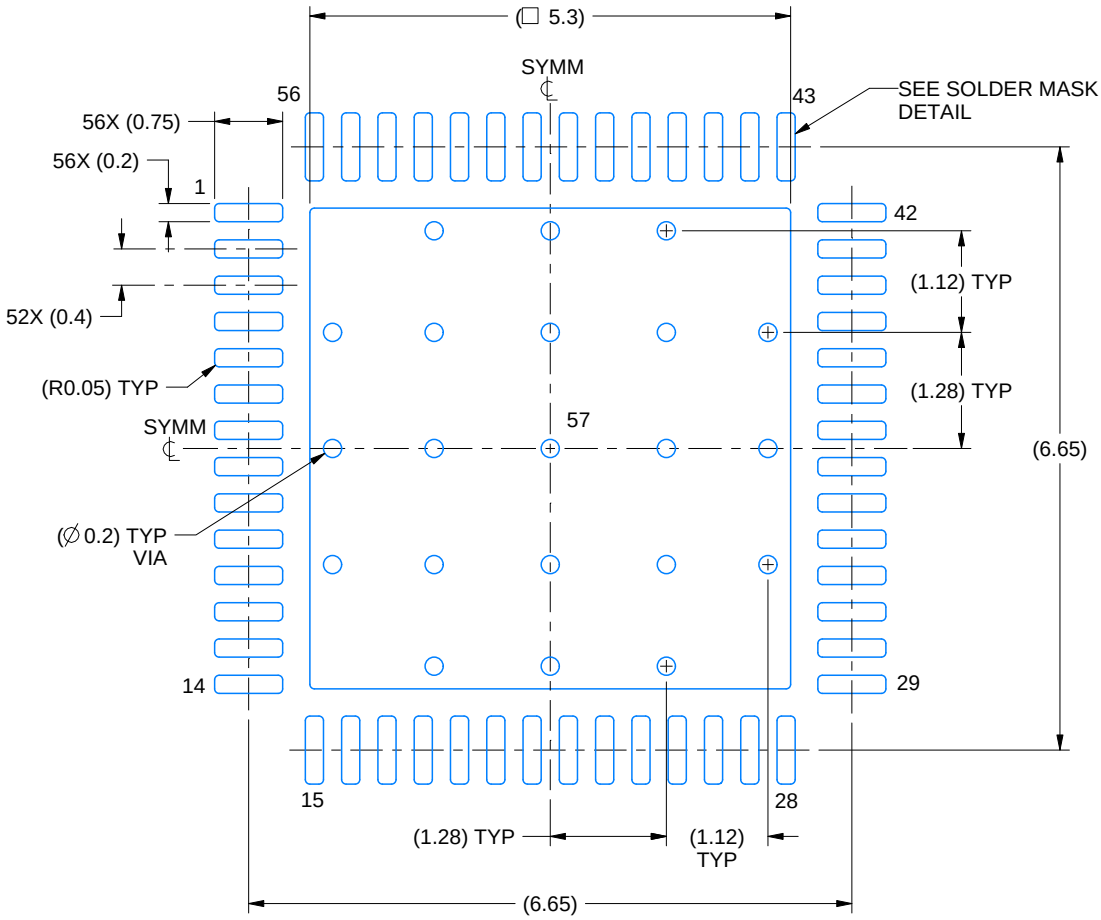
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

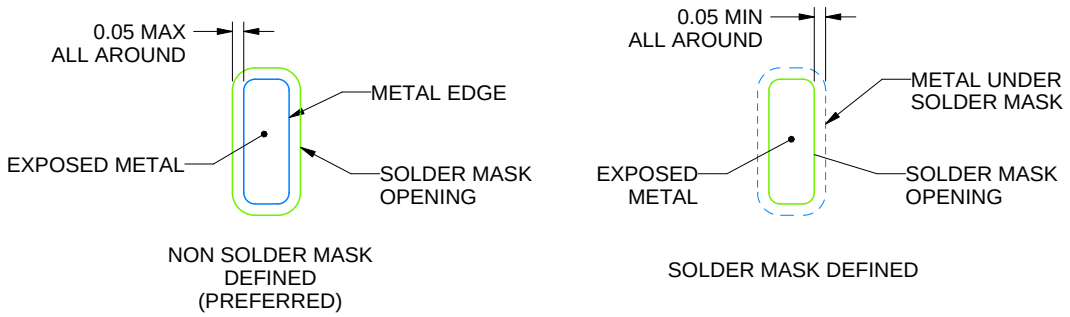


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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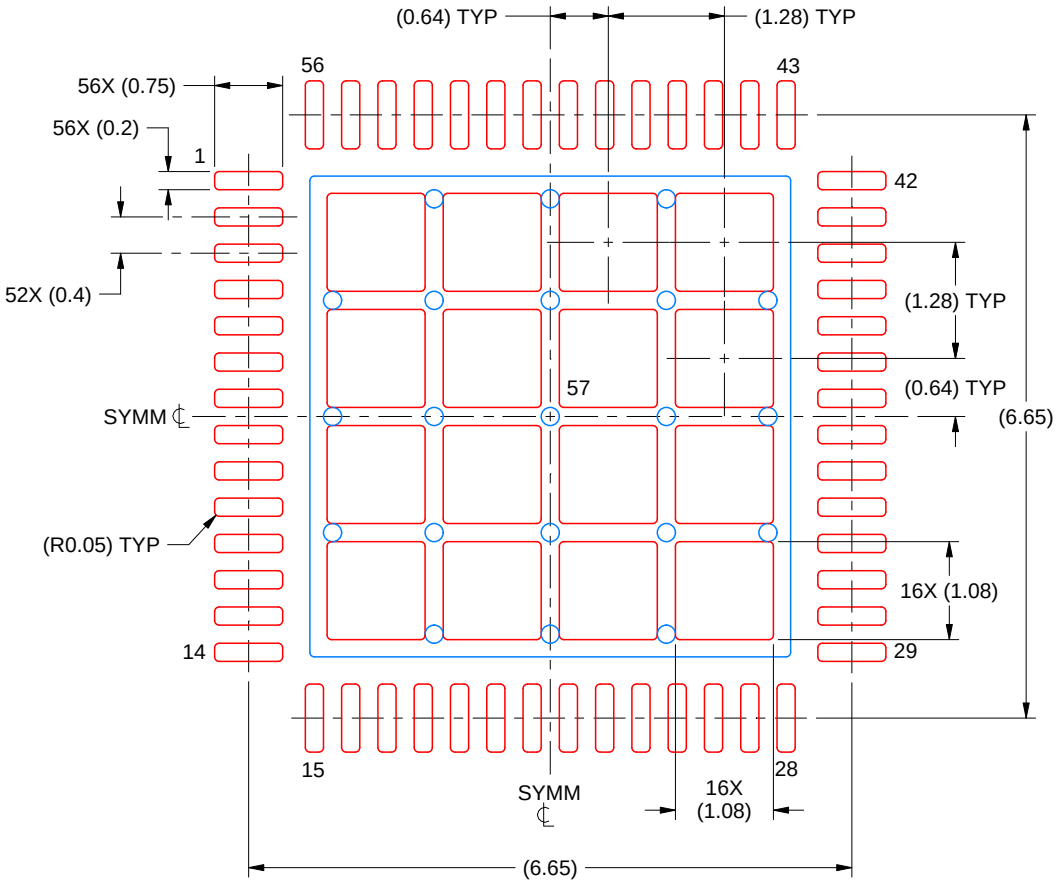
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.100 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 57
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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