ADC3668, ADC3669 Dual-Channel, 16-Bit 250MSPS and 500MSPS Analog-to-Digital Converter (ADC)

1 Features

- 16-bit, dual channel 250 and 500MSPS ADC
- Noise spectral density: -160.4dBFS/Hz
- Thermal Noise: 76.4dBFS
- Single core (non-interleaved) ADC architecture
- Aperture jitter: 75fs
- Buffered analog inputs
  - Programmable 100Ω and 200Ω termination
- Input fullscale: $2V_{PP}$
- Full power input bandwidth (-3dB): 1.4GHz
- Spectral performance (f_{IN} = 70MHz, -1dBFS):
  - SNR: 75.6dBFS
  - SFDR HD2,3: 80dBc
  - SFDR worst spur: 94dBFS
- INL: ±2 LSB (typical)
- DNL: ±0.5 LSB (typical)
- Digital down-converters (DDCs)
  - Up to four independent DDCs
  - Complex and real decimation
  - Decimation: /2, /4 to /32768 decimation
  - 48-bit NCO phase coherent frequency hopping
- DDR/Serial LVDS interface
  - 16-bit Parallel DDR LVDS for DDC bypass
  - Serial LVDS for decimation
  - 32-bit output option for high decimation
- Power consumption: 300mW/channel (500MSPS)

2 Applications

- Software defined radio
- Spectrum analyzer
- Radar
- Spectroscopy
- Power amplifier linearization
- Communications infrastructure

3 Description

The ADC3668 and ADC3669 (ADC366x) are a 16-bit, 250MSPS and 500MSPS, dual channel analog to digital converters (ADC). The devices are designed for high signal-to-noise ratio (SNR) and deliver a noise spectral density of −160dBFS/Hz (500MSPS).

The ADC366x includes an optional quad band digital down-converter (DDC) supporting wide band decimation by 2 to narrow band decimation by 32768. The DDC uses a 48-bit NCO which supports phase coherent and phase continuous frequency hopping.

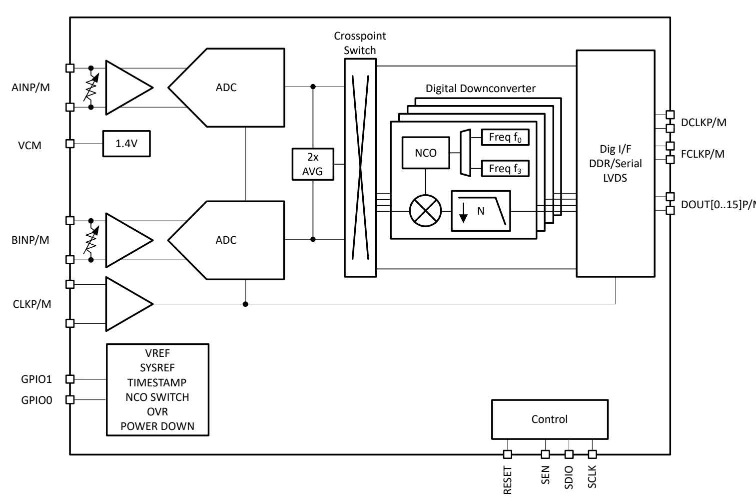
The ADC366x is outfitted with a flexible LVDS interface. In decimation bypass mode, the device uses a 16-bit wide parallel DDR LVDS interface. When using decimation, the output data is transmitted using a serial LVDS interface reducing the number of lanes needed as decimation increases. For high decimation ratios, the output resolution can be increased to 32-bit.

The power efficient ADC architecture consumes 300mW/ch at 500MSPS and provides power scaling with lower sampling rates (250mW/ch at 250MSPS).

Device Information

PART NUMBER	PACKAGE(1)	MAXIMUM SAMPLING RATE
ADC3669	64 QFN	500MSPS
ADC3668	64 QFN	250MSPS

(1) For more information, see Section 12.



Block Diagram

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4 Device Comparison

Table 4-1. Device Comparison Table

Part Number	Maximum Sampling Rate	Resolution	No. of Channels
ADC3669	500MSPS	16 bit	2
ADC3668	250MSPS	16 bit	2
ADC3569	500MSPS	16 bit	1
ADC3568	250MSPS	16 bit	1
ADC3649	500MSPS	14 bit	2
ADC3648	250MSPS	14 bit	2
ADC3549	500MSPS	14 bit	1
ADC3548	250MSPS	14 bit	1

5 Pin Configuration and Functions

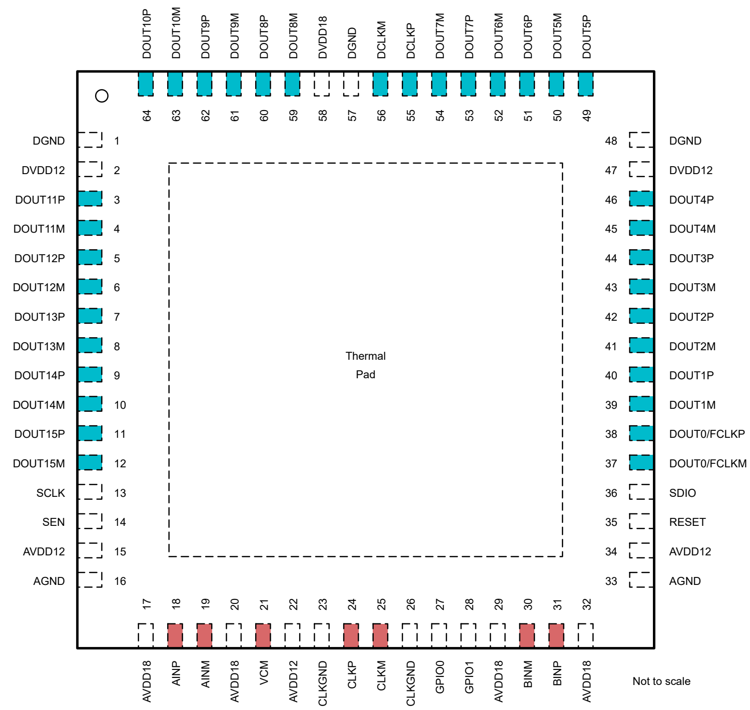


Figure 5-1. RTD Package, 64 Pin VQFNP (Top View)

Table 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
AGND	16, 33	I	Analog ground, 0V
AINM	19	I	Channel A differential signal input, negative connection. The differential input has programmable internal termination (100Ω or 200Ω) and is self biased.
AINP	18	I	Channel A differential signal input, positive connection.
AVDD12	15, 22, 34	I	Analog 1.2V supply
AVDD18	17, 20, 29, 32	I	Analog 1.8V supply
BINM	30	I	Channel B differential signal input, negative connection. The differential input has programmable internal termination (100Ω or 200Ω) and is self biased.
BINP	31	I	Channel B differential signal input, positive connection.
CLKGND	23, 26	I	Clock ground, 0V
CLKP	24	I	Device sampling clock differential input. AC coupling and terminating the clock signal externally for best AC performance is recommended. The differential input is self biased to the input common-mode voltage (0.75V).
CLKM	25	I	
DCLKP	55	O	Differential LVDS data bit clock output.
DCLKM	56	O	
DGND	1, 48, 57	I	Digital ground, 0V
DOUT0/FCLKM	37	O	Differential LVDS data bit output lane 0. In decimation mode, this pin turns to the differential SLVDS frame clock output, replacing the LSB.
DOUT0/FCLKP	38	O	
DOUT1M	39	O	Differential LVDS data bit output lane 1. Can be left floating and powered down via SPI if not used.
DOUT1P	40	O	
DOUT2M	41	O	Differential LVDS data bit output lane 2. Can be left floating and powered down via SPI if not used.
DOUT2P	42	O	

Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DOUT3M	43	O	Differential LVDS data bit output lane 3. Can be left floating and powered down via SPI if not used.
DOUT3P	44	O	
DOUT4M	45	O	Differential LVDS data bit output lane 4. Can be left floating and powered down via SPI if not used.
DOUT4P	46	O	
DOUT5P	49	O	Differential LVDS data bit output lane 5. Can be left floating and powered down via SPI if not used.
DOUT5M	50	O	
DOUT6P	51	O	Differential LVDS data bit output lane 6. Can be left floating and powered down via SPI if not used.
DOUT6M	52	O	
DOUT7P	53	O	Differential LVDS data bit output lane 7. Can be left floating and powered down via SPI if not used.
DOUT7M	54	O	
DOUT8M	59	O	Differential LVDS data bit output lane 8. Can be left floating and powered down via SPI if not used.
DOUT8P	60	O	
DOUT9M	61	O	Differential LVDS data bit output lane 9. Can be left floating and powered down via SPI if not used.
DOUT9P	62	O	
DOUT10M	63	O	Differential LVDS data bit output lane 10. Can be left floating and powered down via SPI if not used.
DOUT10P	64	O	
DOUT11P	3	O	Differential LVDS data bit output lane 11. Can be left floating and powered down via SPI if not used.
DOUT11M	4	O	
DOUT12P	5	O	Differential LVDS data bit output lane 12. Can be left floating and powered down via SPI if not used.
DOUT12M	6	O	
DOUT13P	7	O	Differential LVDS data bit output lane 13. Can be left floating and powered down via SPI if not used.
DOUT13M	8	O	
DOUT14P	9	O	Differential LVDS data bit output lane 14. Can be left floating and powered down via SPI if not used.
DOUT14M	10	O	
DOUT15P	11	O	Differential LVDS data bit output lane 15. Can be left floating and powered down via SPI if not used.
DOUT15M	12	O	
DVDD12	2, 47	I	Digital 1.2V supply
DVDD18	58	I	Digital 1.8V supply
GPIO0	27	I/O	Synchronization or control input or status output or external voltage reference (1.2V). Can be left floating if not used.
GPIO1	28	I/O	Synchronization or control input or status output or external voltage reference (1.2V). Can be left floating if not used.
RESET	35	I	Hardware reset. Active high. This pin has an internal 21kΩ pull-down resistor to DGND.
SCLK	13	I	Serial interface clock for the serial interface programming. This pin has an internal 21kΩ pull-up resistor to DVDD18.
SDIO	36	I/O	Serial interface data input/output. This pin has an internal 21kΩ pull-up resistor to DVDD18.
SEN	14	I	Serial interface chip select. This pin has an internal 21kΩ pull-up resistor to DVDD18.
VCM	21	O	Common mode voltage output (1.4V)

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage range, AVDD18		–0.3	2.1	V
Supply voltage range, AVDD12		–0.3	1.4	V
Supply voltage range, DVDD18		–0.3	2.1	V
Supply voltage range, DVDD12		–0.3	1.4	V
Voltage applied to input pins	AINP/M, BINP/M	–0.3	2.1	V
	CLKP/M	–0.3	1.4	V
	GPIO0/1, RESET, SCLK, SEN, SDIO	–0.3	DVDD18 + 0.2	V
Peak RF input power (AINP/M, BINP/M)	Differential 100 Ω termination		10	dBm
Junction temperature, T_J			125	℃
Storage temperature, T_{stg}		–65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	1500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
AVDD18	1.8 V analog supply		1.75	1.8	1.85	V
AVDD12	1.2 V analog supply		1.15	1.2	1.225	V
DVDD18	1.8 V digital supply		1.75	1.8	1.85	V
DVDD12	1.2 V digital supply		1.15	1.2	1.225	V
T_A	Operating free-air temperature		–40		105	℃
T_J	Operating junction temperature				115[1]	℃

(1) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

6.4 Thermal Information

THERMAL METRIC[1]		ADC3668/69 RTD (QFN) 64 Pins	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	22.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	11.4	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	7.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.3	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics - Power Consumption

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 500 MSPS, DDC Bypass mode, 50% clock duty cycle, nominal supply voltages and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC3668 - 250 MSPS						
I_{AVDD18}	Supply current, 1.8 V analog supply	DDR LVDS		115	130	mA
I_{AVDD12}	Supply current, 1.2 V analog supply			65	130	
I_{DVDD18}	Supply current, 1.8 V digital supply			75	105	
I_{DVDD12}	Supply current, 1.2 V digital supply			78	150	
P_{DIS}	Power dissipation			476		mW
ADC3669 - 500 MSPS						
I_{AVDD18}	Supply current, 1.8 V analog supply	DDR LVDS		126	140	mA
I_{AVDD12}	Supply current, 1.2 V analog supply			98	170	
I_{DVDD18}	Supply current, 1.8 V digital supply			69	105	
I_{DVDD12}	Supply current, 1.2 V digital supply			113	210	
P_{DIS}	Power dissipation			604		mW
POWER DOWN MODES						
P_{DIS}	Power down mode power consumption	Global power down		30		mW

6.6 Electrical Characteristics - DC Specifications

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 500 MSPS, DDC Bypass mode, 50% clock duty cycle, nominal supply voltages and –1-dBFS differential input, internal reference, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
No missing codes			16			bits
ADC3668: 250 MSPS (INTERNAL REFERENCE)						
DNL	Differential nonlinearity	F_{IN} = 70 MHz	-0.9	± 0.5		LSB
INL	Integral nonlinearity	F_{IN} = 70 MHz		± 2		LSB
V_{OS_ERR}	Offset error			10		LSB
V_{OS_DRIFT}	Offset drift over temperature			10		LSB
$GAIN_{ERR}$	Gain error	External Reference		± 1		%FSR
		Internal Reference		± 3		

6.6 Electrical Characteristics - DC Specifications (continued)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 500 MSPS, DDC Bypass mode, 50% clock duty cycle, nominal supply voltages and –1-dBFS differential input, internal reference, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$GAIN_{DRIFT}$	Gain drift over temperature	External Reference		± 0.5		%FSR
		Internal Reference		± 1		
ADC3669: 500 MSPS (INTERNAL REFERENCE)						
DNL	Differential nonlinearity	F_{IN} = 70 MHz	-0.9	± 0.5		LSB
INL	Integral nonlinearity	F_{IN} = 70 MHz		± 2		LSB
V_{OS_ERR}	Offset error			10		LSB
V_{OS_DRIFT}	Offset drift over temperature			10		LSB
$GAIN_{ERR}$	Gain error	External Reference		± 1		%FSR
		Internal Reference		± 3		
$GAIN_{DRIFT}$	Gain drift over temperature	External Reference		± 0.5		%FSR
		Internal Reference		± 1		
ADC ANALOG INPUTS (AINP/M, BINP/M)						
FS	Input full scale	Differential		2.0		Vpp
V_{ICM}	Input common model voltage		1.3	1.4	1.5	V
Z_{IN}	Differential input impedance	Differential at 100 MHz		100		Ω
V_{CM}	Output common mode voltage			1.4		V
BW	Analog Input Bandwidth (-3dB)			1.4		GHz
CLOCK INPUT (CLKP/M)						
Input clock frequency		ADC3669	100		500	MHz
		ADC3668	100		250	MHz
V_{ID}	Differential input voltage		0.5	2	2.4	Vpp
V_{ICM}	Input common mode voltage			0.75		V
Z_{IN}	Differential input impedance	Differential at 500 MHz		5		kΩ
Clock duty cycle			35	50	65	%
EXTERNAL REFERENCE INPUT (GPIO1)						
VREF	External voltage reference		1.175	1.2	1.225	V
I_{VREF}	Input current, external voltage reference input			10		uA
DIGITAL INPUTS (GPIO0, GPIO1, RESET, SCLK, SEN, SDIO)						
V_{IH}	High level input voltage		1.4	1.8		V
V_{IL}	Low level input voltage			0	0.4	V
I_{IH}	High level input current			90	150	uA
I_{IL}	Low level input current		-150	-90		uA
C_I	Input capacitance			1.5		pF
DIGITAL OUTPUTS (GPIO0, GPIO1, SDIO)						
V_{OH}	High level output voltage	I_{LOAD} = -400 uA	AVDD18 – 0.1	AVDD18		V
V_{OL}	Low level output voltage	I_{LOAD} = 400 uA			0.1	V
LVDS/SLVDS INTERFACE (DOUT[0..15]P/M, DCLKP/M)						
Output data format (default)				2s complement		
V_{OD}	Differential output voltage	differential peak-peak	500	700	850	mVpp
V_{OCM}	Output common mode voltage		0.96	1.02	1.08	V

6.7 Electrical Characteristics - AC Specifications (ADC3668 - 250 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 250 MSPS, DDC Bypass mode, 50% clock duty cycle, nominal supply voltages and –1-dBFS differential input, internal reference, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN[(1)]	TYP	MAX	UNIT
AC ACCURACY						
NSD	Noise Spectral Density	f_{IN} = 100 MHz, A_{IN} = -20 dBFS		–157.4		dBFS/Hz
NF	Noise Figure	f_{IN} = 100 MHz, A_{IN} = -20 dBFS		23.6		dB
SNR	Signal to noise ratio	f_{IN} = 10 MHz		75.5		dBFS
		f_{IN} = 70 MHz		75.2		
		f_{IN} = 170 MHz		74.6		
		f_{IN} = 300 MHz		72.9		
		f_{IN} = 450 MHz		71.4		
SINAD	Signal to noise and distortion ratio	f_{IN} = 10 MHz		73.6		dBFS
		f_{IN} = 70 MHz		74.1		
		f_{IN} = 170 MHz		72.2		
		f_{IN} = 300 MHz		68.5		
		f_{IN} = 450 MHz		64.7		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.9		Bits
		f_{IN} = 70 MHz		12.0		
		f_{IN} = 170 MHz		11.7		
		f_{IN} = 300 MHz		11.1		
		f_{IN} = 450 MHz		10.4		
THD	Total Harmonic Distortion (First five harmonics)	f_{IN} = 10 MHz		77		dBc
		f_{IN} = 70 MHz		80		
		f_{IN} = 170 MHz		75		
		f_{IN} = 300 MHz		71		
		f_{IN} = 450 MHz		65		
HD2	Second Harmonic Distortion	f_{IN} = 10 MHz		79		dBFS
		f_{IN} = 70 MHz	70	85		
		f_{IN} = 170 MHz		78		
		f_{IN} = 300 MHz		76		
		f_{IN} = 450 MHz		68		
HD3	Third Harmonic Distortion	f_{IN} = 10 MHz		83		dBFS
		f_{IN} = 70 MHz	72	81		
		f_{IN} = 170 MHz		81		
		f_{IN} = 300 MHz		79		
		f_{IN} = 450 MHz		74		
Non HD2,3	Spur free dynamic range (excluding HD2 and HD3)	f_{IN} = 10 MHz		96		dBFS
		f_{IN} = 70 MHz		96		
		f_{IN} = 170 MHz		95		
		f_{IN} = 300 MHz		88		
		f_{IN} = 450 MHz		81		
IMD3	Two tone inter-modulation distortion	f_1 = 100 MHz, f_2 = 120 MHz, A_{IN} = -7 dBFS/tone		83		dBc

(1) SNR, HD3, Non HD23 and IMD3 minimum values are specified by ATE; HD2 is specified by bench characterization.

6.8 Electrical Characteristics - AC Specifications (ADC3669 - 500 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 500 MSPS, DDC Bypass mode, 50% clock duty cycle, nominal supply voltages and –1-dBFS differential input, internal reference, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN[(1)]	TYP	MAX	UNIT
AC ACCURACY						
NSD	Noise Spectral Density	f_{IN} = 100 MHz, A_{IN} = -20 dBFS		–160.4		dBFS/Hz
NF	Noise Figure	f_{IN} = 100 MHz, A_{IN} = -20 dBFS		20.6		dB
SNR	Signal to noise ratio	f_{IN} = 10 MHz		75.8		dBFS
		f_{IN} = 70 MHz	70	75.6		
		f_{IN} = 170 MHz		74.9		
		f_{IN} = 300 MHz		72.6		
		f_{IN} = 450 MHz		71.5		
SINAD	Signal to noise and distortion ratio	f_{IN} = 10 MHz		72.6		dBFS
		f_{IN} = 70 MHz		73.7		
		f_{IN} = 170 MHz		72.4		
		f_{IN} = 300 MHz		68.2		
		f_{IN} = 450 MHz		64.4		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.8		Bits
		f_{IN} = 70 MHz		11.9		
		f_{IN} = 170 MHz		11.7		
		f_{IN} = 300 MHz		11.0		
		f_{IN} = 450 MHz		10.4		
THD	Total Harmonic Distortion (First five harmonics)	f_{IN} = 10 MHz		74		dBc
		f_{IN} = 70 MHz		77		
		f_{IN} = 170 MHz		74		
		f_{IN} = 300 MHz		68		
		f_{IN} = 450 MHz		63		
HD2	Second Harmonic Distortion	f_{IN} = 10 MHz		76		dBFS
		f_{IN} = 70 MHz	70	82		
		f_{IN} = 170 MHz		77		
		f_{IN} = 300 MHz		81		
		f_{IN} = 450 MHz		76		
HD3	Third Harmonic Distortion	f_{IN} = 10 MHz		88		dBFS
		f_{IN} = 70 MHz	70	80		
		f_{IN} = 170 MHz		83		
		f_{IN} = 300 MHz		71		
		f_{IN} = 450 MHz		65		
Non HD2,3	Spur free dynamic range (excluding HD2 and HD3)	f_{IN} = 10 MHz		94		dBFS
		f_{IN} = 70 MHz		94		
		f_{IN} = 170 MHz		90		
		f_{IN} = 300 MHz		86		
		f_{IN} = 450 MHz		87		
IMD3	Two tone inter-modulation distortion	f_1 = 100 MHz, f_2 = 120 MHz, A_{IN} = -7 dBFS/tone		86		dBc

(1) SNR, HD3, Non HD23 and IMD3 minimum values are specified by ATE; HD2 is specified by bench characterization.

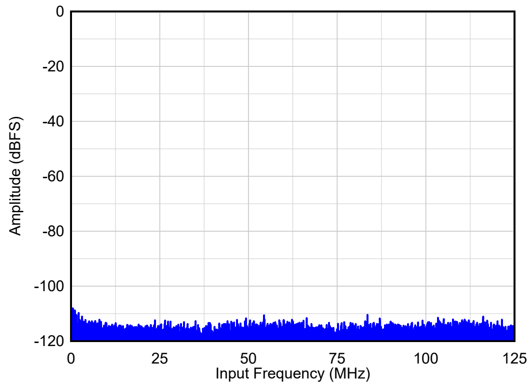
6.9 Timing Requirements

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 500 MSPS, DDC Bypass mode, 50% clock duty cycle, nominal supply voltages and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC TIMING SPECIFICATIONS						
T_{AD}	Aperture Delay			200		ps
T_A	Aperture Jitter			75		fs
CER	Code error rate	F_S = 500 MSPS, Error > 64 codes		1E-10		errors/ sample
		F_S = 500 MSPS, Error > 128 codes		3E-13		
		F_S = 250 MSPS, Error > 64 codes		1E-11		
Wake up time		time to valid data after coming out of global power down mode (internal voltage reference OFF)		3		ms
LATENCY: t_{PD} + t_{ADC} + t_{DIG}						
t_{PD}	Propagation delay: sampling clock falling edge to DCLK rising edge	Propagation delay: sampling clock falling edge to DCLK rising edge	1.4 + T_S/4	1.7 + T_S/4	2 + T_S/4	ns
t_{ADC}	ADC latency	DDR LVDS, normal mode		38		ADC clock cycles
		DDR LVDS, low latency mode		4		
	Time stamp: input to LVDS output	DDR LVDS		8		
t_{DIG}	Digital latency: interface and decimation	DDC bypass		5		Output clock cycles
		Decimation by 2 (real or complex)		24		
		Decimation by 4,8 (real or complex)		49		
		Decimation by 16...32768 (real or complex)		50		
SERIAL PROGRAMMING INTERFACE (SCLK, SEN, SDIO) - Input						
$f_{CLK(SCLK)}$	Serial clock frequency		1		20	MHz
t_{SLOADS}	Setup time from SEN falling edge to SCLK rising edge		10			ns
t_{SLOADH}	Hold time from SCLK rising edge to SEN rising edge		10			ns
t_{DSU}	Setup time from SDIO to rising edge of SCLK		10			ns
t_{DH}	Hold time from rising edge of SCLK to SDIO		10			ns
SERIAL PROGRAMMING INTERFACE (SDIO) - Output						
$t_{(OZD)}$	SDIO tri-state to driven				10	ns
$t_{(ODZ)}$	SDIO data to tri-state				14	ns
$t_{(OD)}$	SDIO valid from falling edge of SCLK				10	ns
TIMING: SYSREF						
$t_{s(SYSREF)}$	Setup time: SYSREF valid to rising edge of CLKP/M		100			ps
$t_{h(SYSREF)}$	Hold time: Rising edge of CLKP/M to SYSREF invalid		100			ps
INTERFACE TIMING: DDR AND SLVDS						
t_{DV}	Time Data Valid: data transition to DCLK transition	F_S = 500 MSPS	0.465	0.68	0.905	ns
		F_S = 250 MSPS	0.905	1.16	1.415	ns
t_{DI}	Time Data Invalid : DCLK transition to data transition	F_S = 500 MSPS	0.095	0.32	0.535	ns
		F_S = 250 MSPS	0.615	0.84	1.065	ns

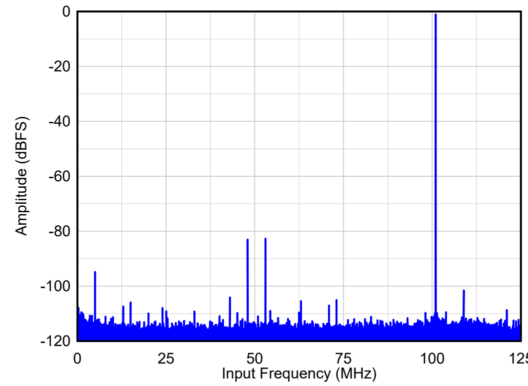
6.10 Typical Characteristics, ADC3668

Typical values are specified at T_A = 25°C, ADC sampling rate = 250MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted



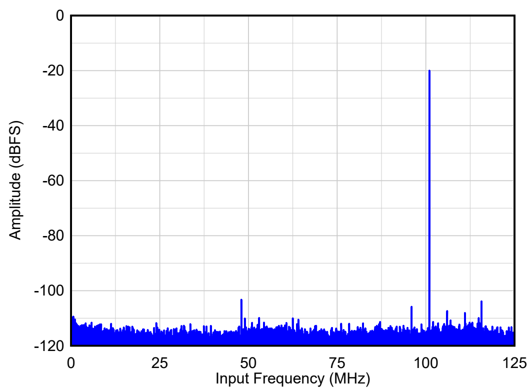
SNR = 76dBFS, NSD = −157dBFS/Hz

Figure 6-1. Idle Channel Noise



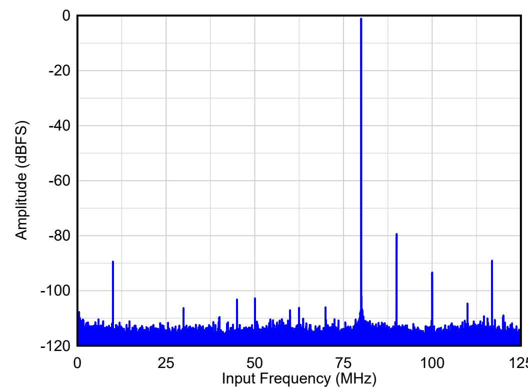
SNR = 75.2dBFS, HD23 = 82dBc, Non HD23 = 95dBFS

Figure 6-2. Single Tone FFT at F_{IN} = 101MHz



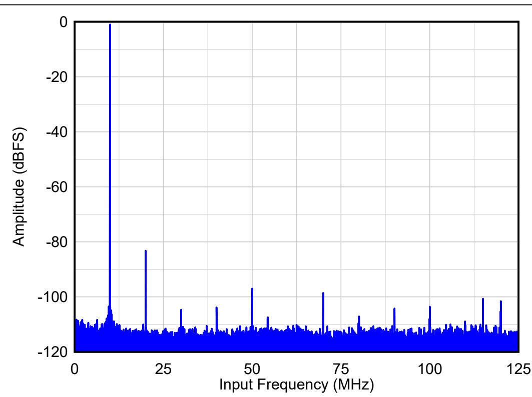
SNR = 76.2dBFS, HD23 = 89dBc, Non HD23 = 105dBFS

Figure 6-3. Single Tone FFT at F_{IN} = 101MHz, A_{IN} = −20dBFS



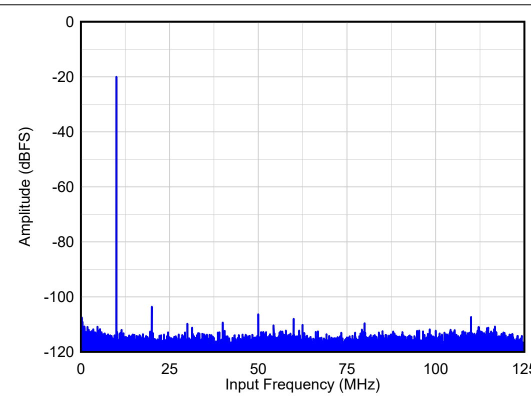
SNR = 74.8dBFS, HD23 = 79dBc, Non HD23 = 88dBFS

Figure 6-4. Single Tone FFT at F_{IN} = 170MHz



SNR = 74.3dBFS, HD23 = 82dBc, Non HD23 = 98dBFS

Figure 6-5. Single Tone FFT at F_{IN} = 240MHz

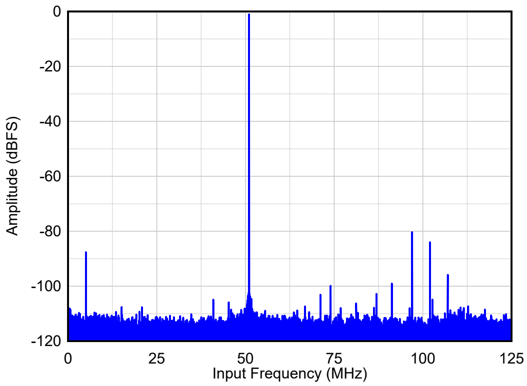


SNR = 76.1dBFS, HD23 = 86dBc, Non HD23 = 105dBFS

Figure 6-6. Single Tone FFT at F_{IN} = 240MHz, A_{IN} = −20dBFS

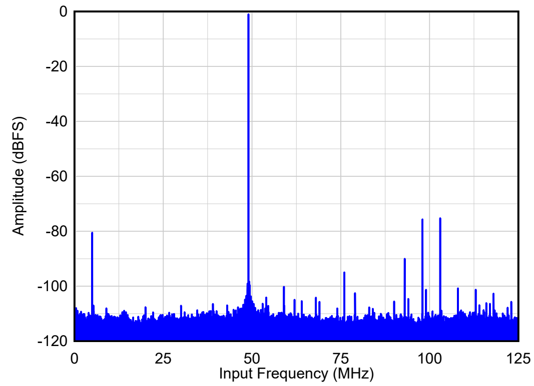
6.10 Typical Characteristics, ADC3668 (continued)

Typical values are specified at T_A = 25°C, ADC sampling rate = 250MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted



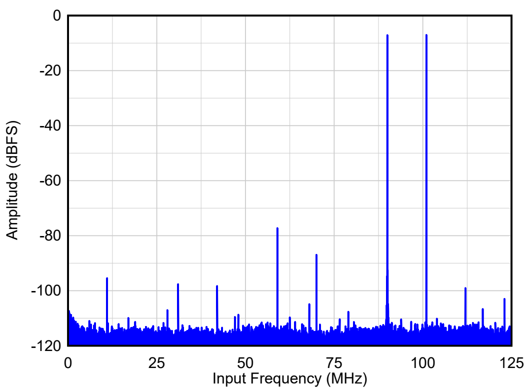
SNR = 73.4dBFS, HD23 = 80dBc, Non HD23 = 85dBFS

Figure 6-7. Single Tone FFT at F_{IN} = 300MHz



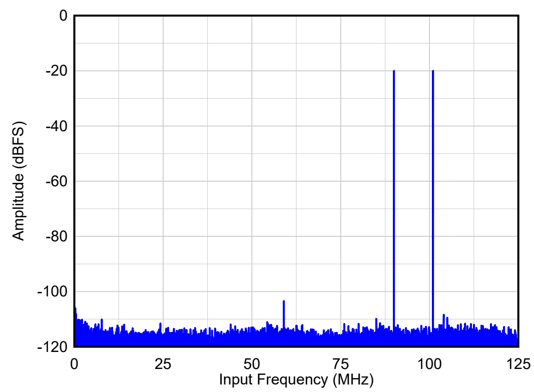
SNR = 71.5dBFS, HD23 = 76dBc, Non HD23 = 80dBFS

Figure 6-8. Single Tone FFT at F_{IN} = 450MHz



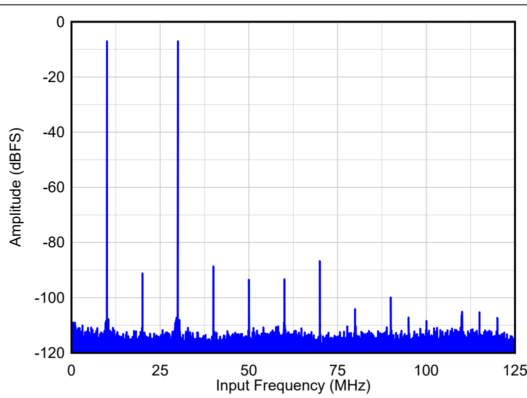
A_{IN} = -7dBFS/tone, IMD3 = 91dBc

Figure 6-9. Two Tone FFT at F_{IN} = 90/110MHz



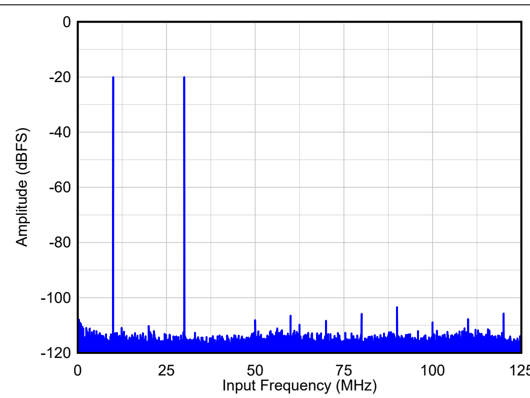
A_{IN} = -20dBFS/tone, IMD3 = 99dBc

Figure 6-10. Two Tone FFT at F_{IN} = 70/100MHz



A_{IN} = −7dBFS/tone, IMD3 = 83dBc

Figure 6-11. Two Tone FFT at F_{IN} = 220/240MHz



A_{IN} = −20dBFS/tone, IMD3 = 87dBc

Figure 6-12. Two Tone FFT at F_{IN} = 220/240MHz

6.10 Typical Characteristics, ADC3668 (continued)

Typical values are specified at T_A = 25°C, ADC sampling rate = 250MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted

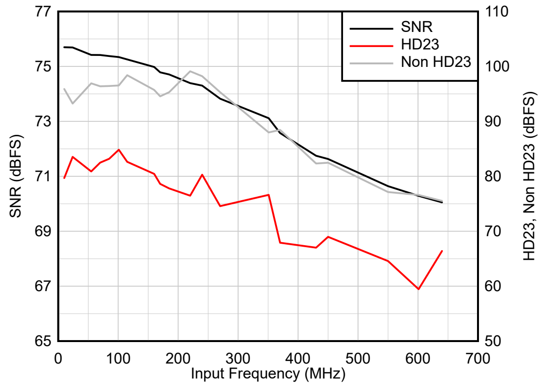
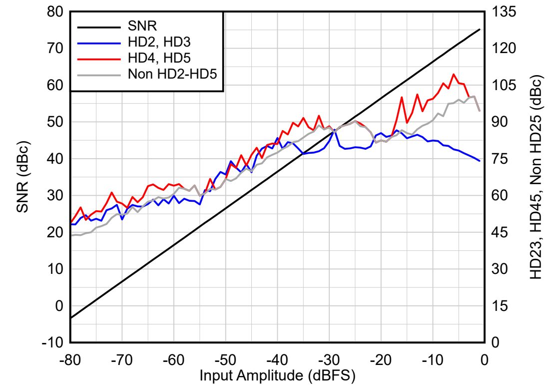
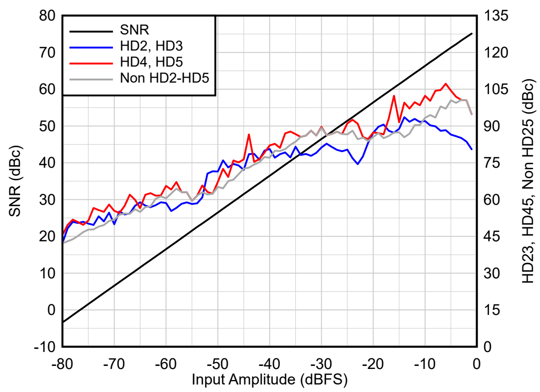


Figure 6-13. AC Performance vs F_{IN}



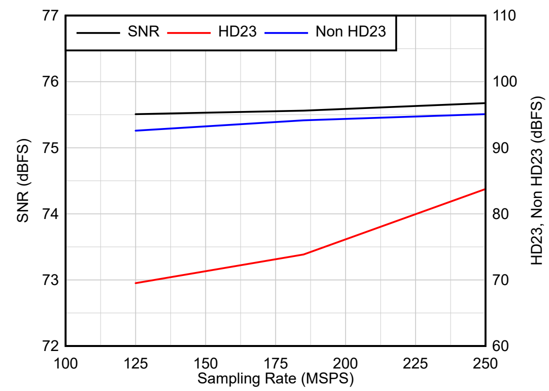
F_{IN} = 10MHz

Figure 6-14. AC Performance vs A_{IN}



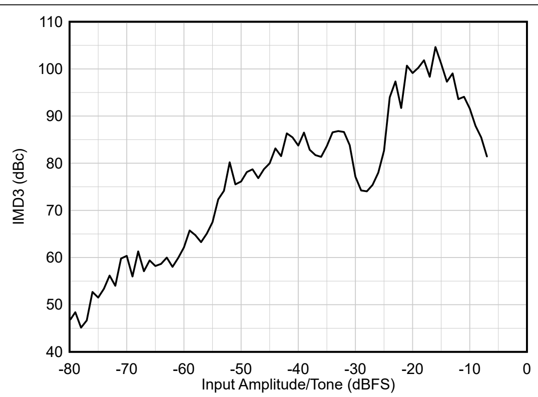
F_{IN} = 100MHz

Figure 6-15. AC Performance vs A_{IN}



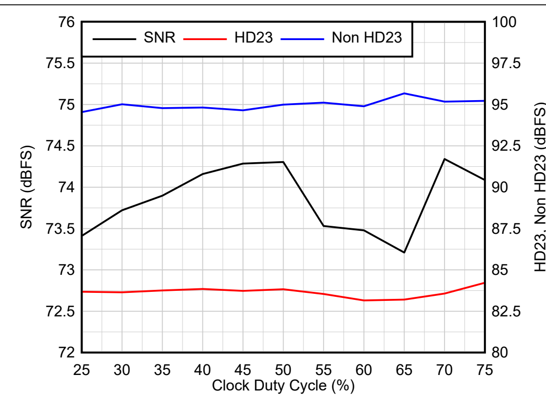
F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-16. AC Performance vs F_S



F_{IN} = 70/100MHz

Figure 6-17. IMD3 vs A_{IN}

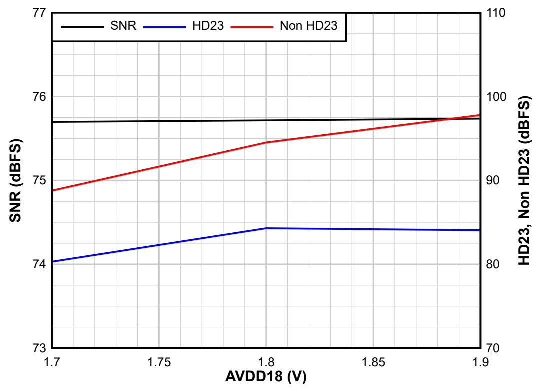


F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-18. AC Performance vs Clock Duty Cycle

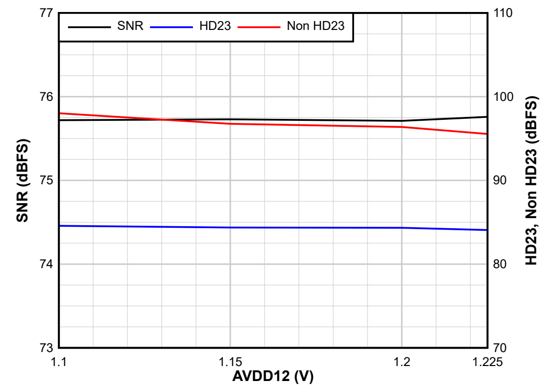
6.10 Typical Characteristics, ADC3668 (continued)

Typical values are specified at T_A = 25°C, ADC sampling rate = 250MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted



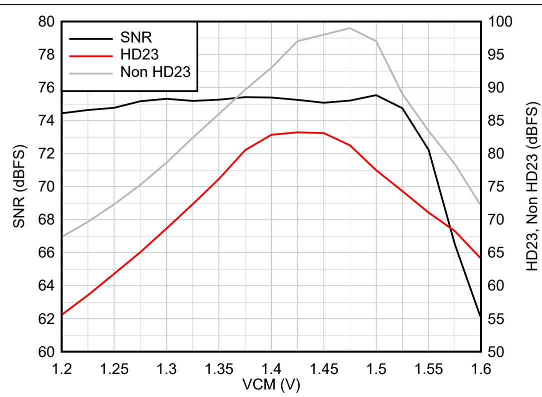
F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-19. AC Performance vs AVDD18



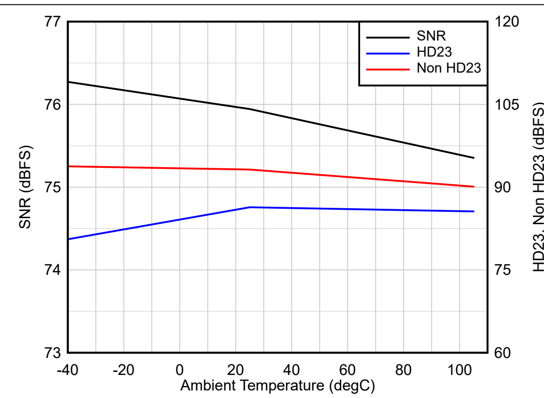
F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-20. AC Performance vs AVDD12



F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-21. AC Performance vs VCM



F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-22. AC Performance vs Temperature

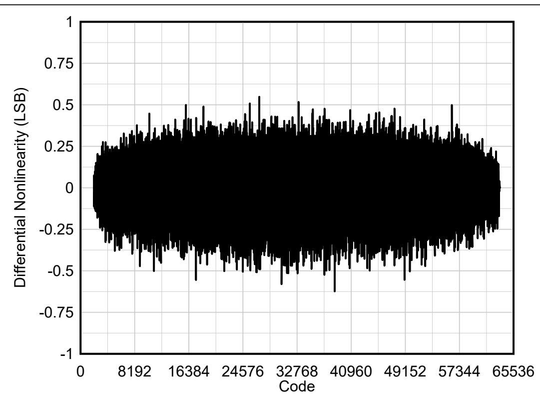


Figure 6-23. DNL

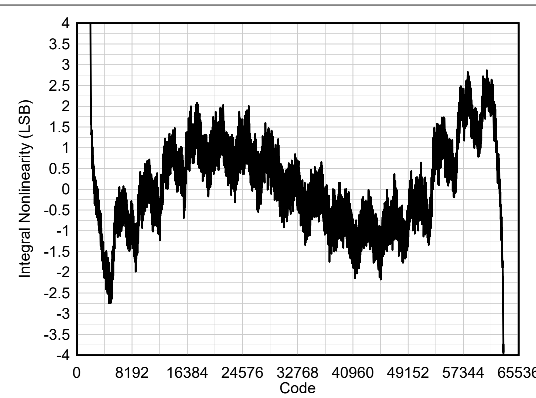


Figure 6-24. INL

6.10 Typical Characteristics, ADC3668 (continued)

Typical values are specified at T_A = 25°C, ADC sampling rate = 250MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted

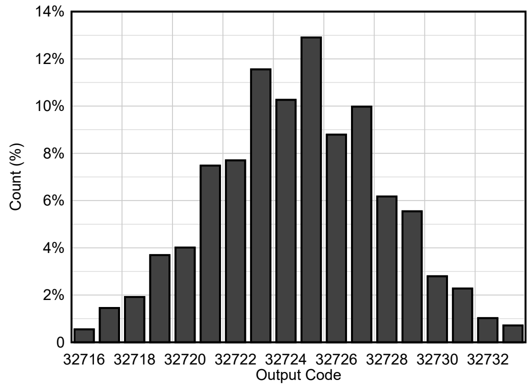


Figure 6-25. DC Offset Histogram

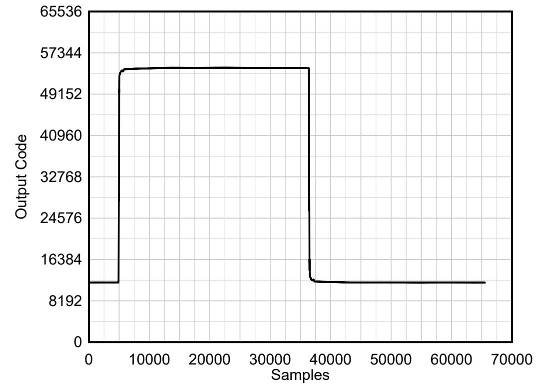
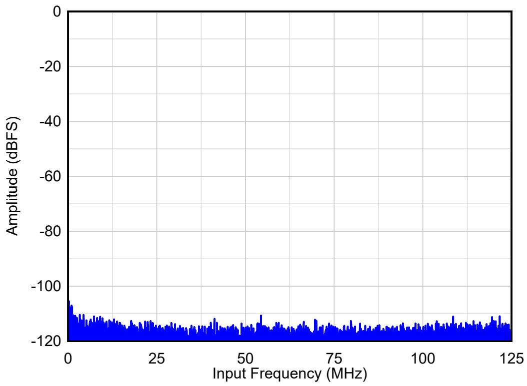


Figure 6-26. Pulse Response

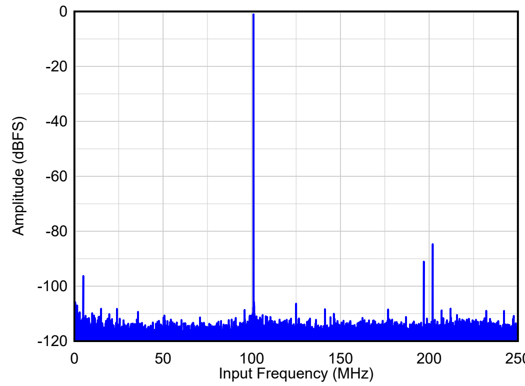
6.11 Typical Characteristics, ADC3669

Typical values are specified at T_A = 25°C, ADC sampling rate = 500MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted



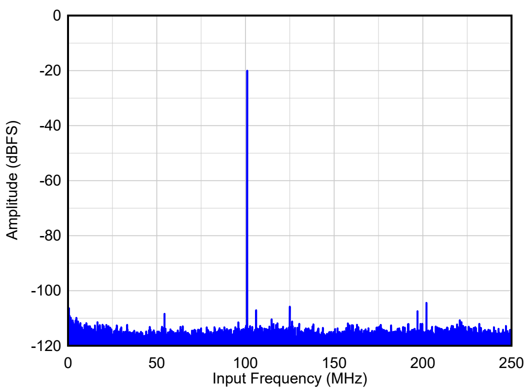
SNR = 76dBFS, NSD = −160dBFS/Hz

Figure 6-27. Idle Channel Noise



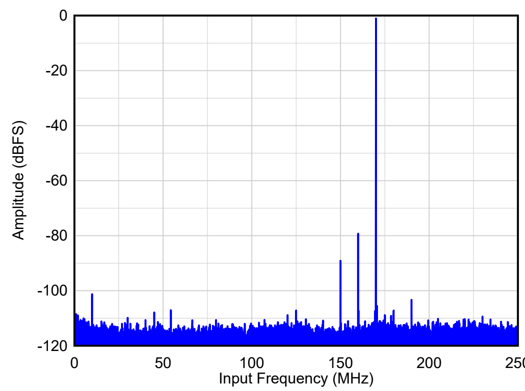
SNR = 75.3dBFS, HD23 = 84dBc, Non HD23 = 95dBFS

Figure 6-28. Single Tone FFT at F_{IN} = 101MHz



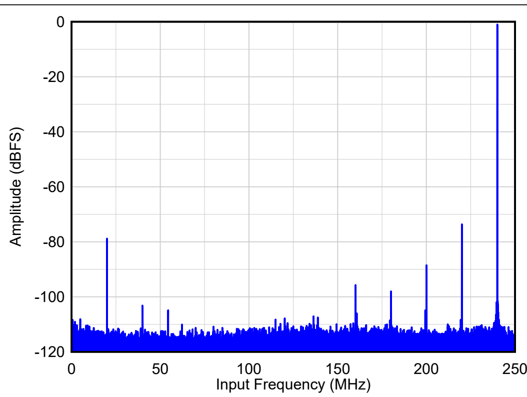
SNR = 76.2dBFS, HD23 = 89dBc, Non HD23 = 105dBFS

Figure 6-29. Single Tone FFT at F_{IN} = 101MHz, A_{IN} = −20dBFS



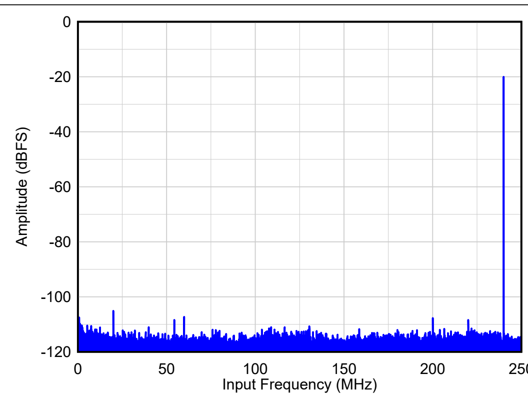
SNR = 74.4dBFS, HD23 = 78dBc, Non HD23 = 101dBFS

Figure 6-30. Single Tone FFT at F_{IN} = 170MHz



SNR = 73.4dBFS, HD23 = 74dBc, Non HD23 = 89dBFS

Figure 6-31. Single Tone FFT at F_{IN} = 240MHz

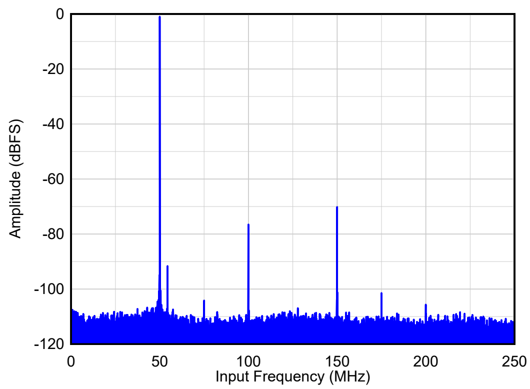


SNR = 76.1dBFS, HD23 = 86dBc, Non HD23 = 105dBFS

Figure 6-32. Single Tone FFT at F_{IN} = 240MHz, A_{IN} = −20dBFS

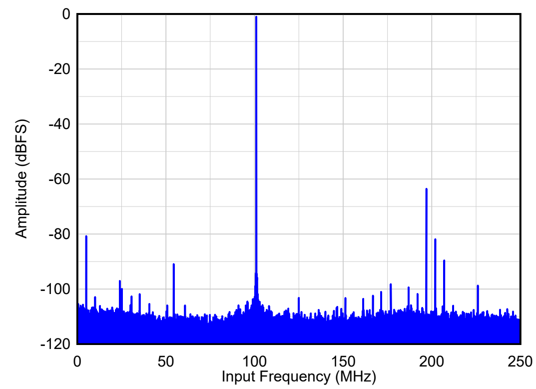
6.11 Typical Characteristics, ADC3669 (continued)

Typical values are specified at T_A = 25°C, ADC sampling rate = 500MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted



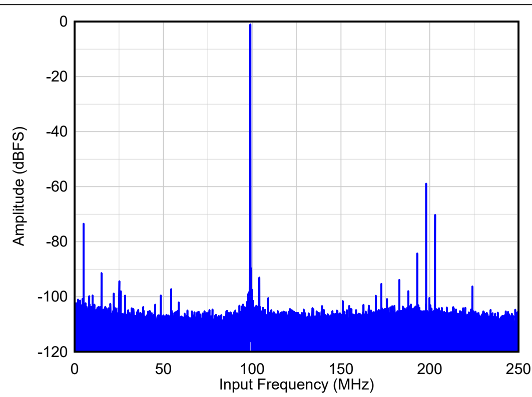
SNR = 70.7dBFS, HD23 = 74dBc, Non HD23 = 92dBFS

Figure 6-33. Single Tone FFT at F_{IN} = 450MHz



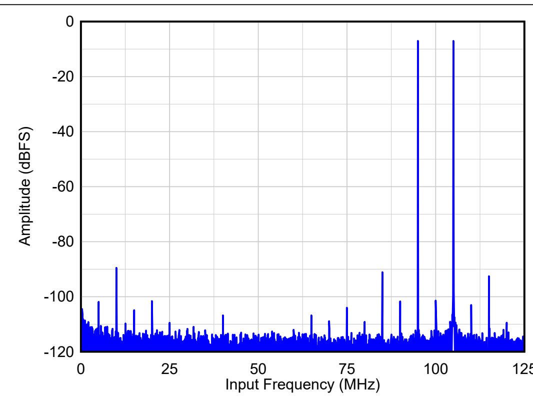
SNR = 68.9dBFS, HD23 = 69dBc, Non HD23 = 81dBFS

Figure 6-34. Single Tone FFT at F_{IN} = 605MHz



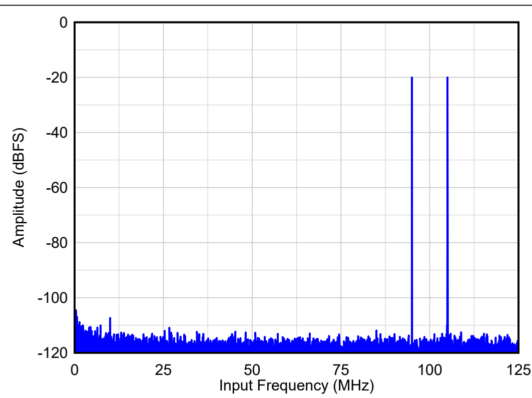
SNR = 65.7dBFS, HD23 = 63dBc, Non HD23 = 74dBFS

Figure 6-35. Single Tone FFT at F_{IN} = 905MHz



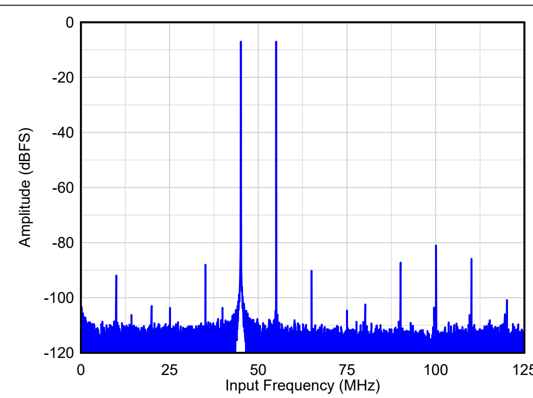
A_{IN} = −7dBFS/tone, IMD3 = 83dBc

Figure 6-36. Two Tone FFT at F_{IN} = 95/105MHz



A_{IN} = -20dBFS/tone, IMD3 = 92dBc

Figure 6-37. Two Tone FFT at F_{IN} = 95/105MHz

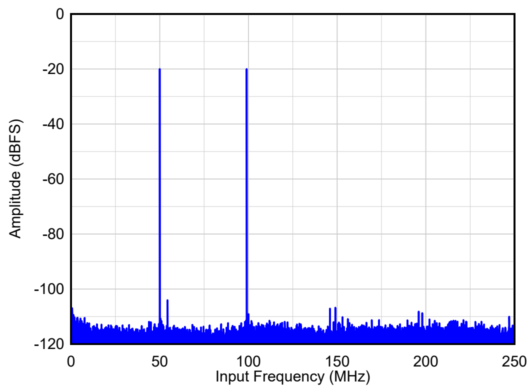


A_{IN} = −7dBFS/tone, IMD3 = 81dBc

Figure 6-38. Two Tone FFT at F_{IN} = 445/455MHz

6.11 Typical Characteristics, ADC3669 (continued)

Typical values are specified at T_A = 25°C, ADC sampling rate = 500MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted



A_{IN} = −20dBFS/tone, IMD3 = 97dBc

Figure 6-39. Two Tone FFT at F_{IN} = 445/455MHz

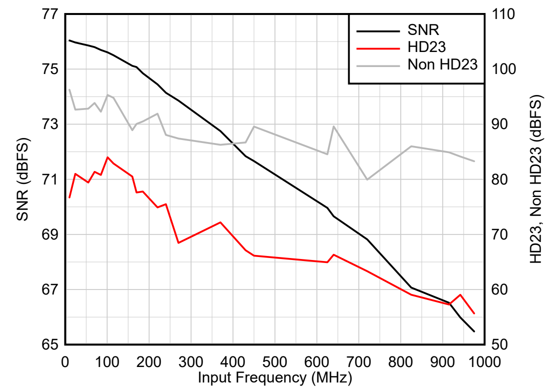
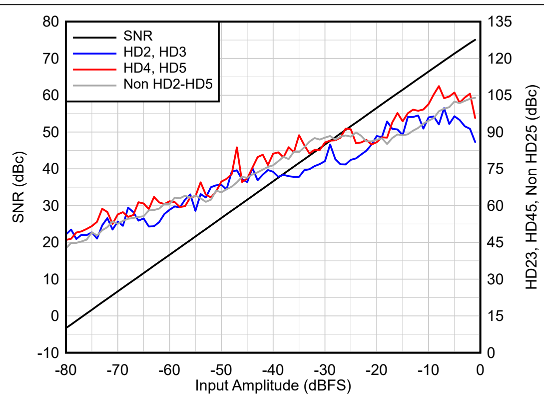
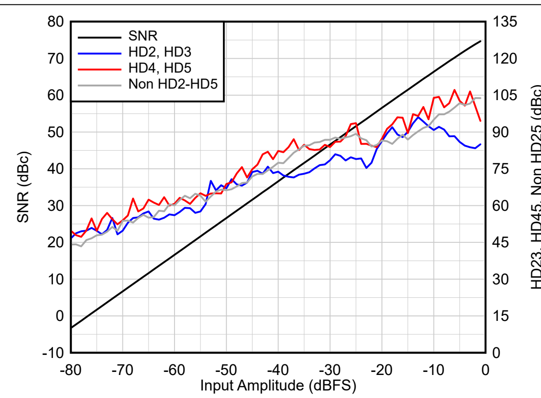


Figure 6-40. AC Performance vs F_{IN}



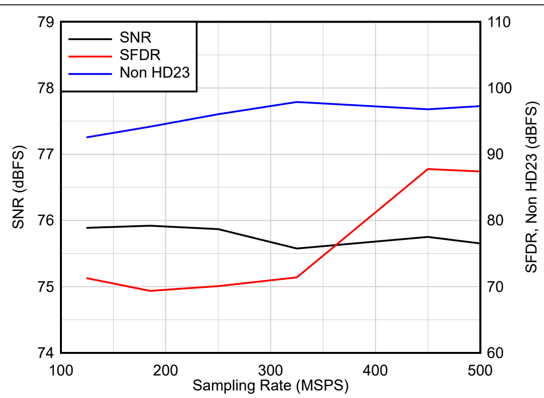
F_{IN} = 10MHz

Figure 6-41. AC Performance vs A_{IN}



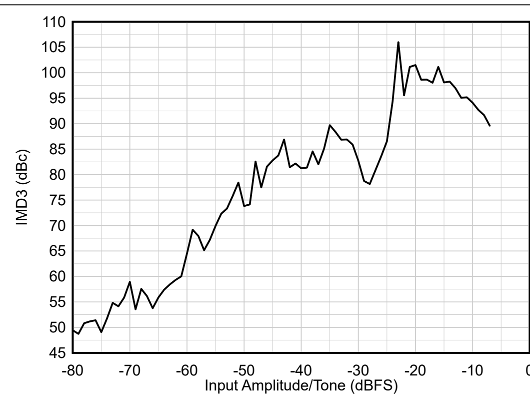
F_{IN} = 100MHz

Figure 6-42. AC Performance vs A_{IN}



F_{IN} = 100MHz

Figure 6-43. AC Performance vs F_S



F_{IN} = 70/100MHz

Figure 6-44. IMD3 vs A_{IN}

6.11 Typical Characteristics, ADC3669 (continued)

Typical values are specified at T_A = 25°C, ADC sampling rate = 500MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted

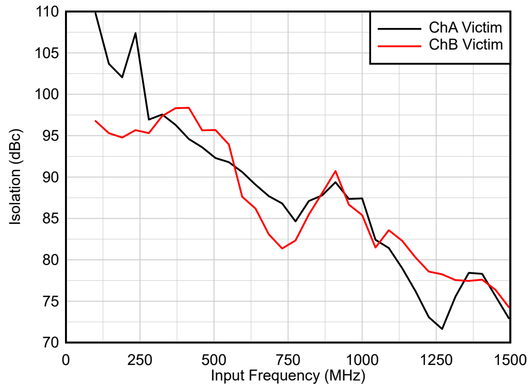
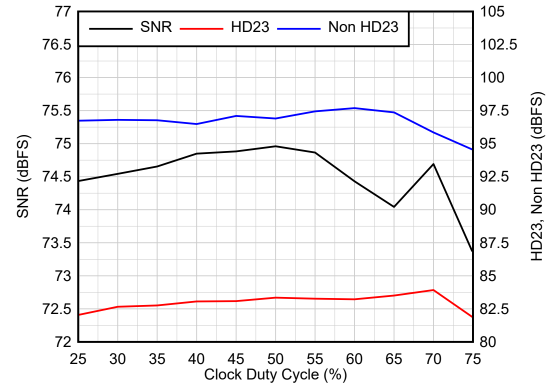
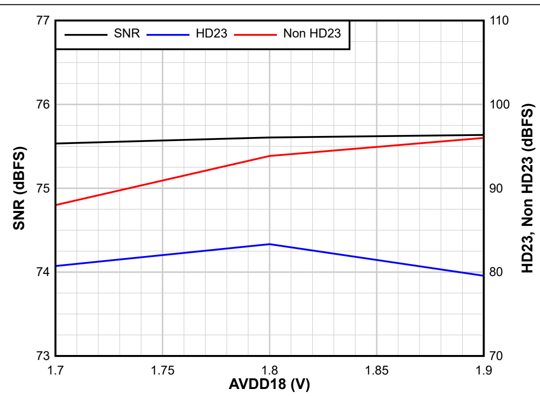


Figure 6-45. Isolation vs F_{IN}



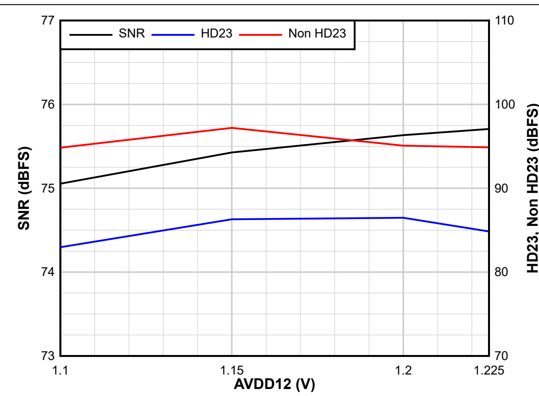
F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-46. AC Performance vs Clock Duty Cycle



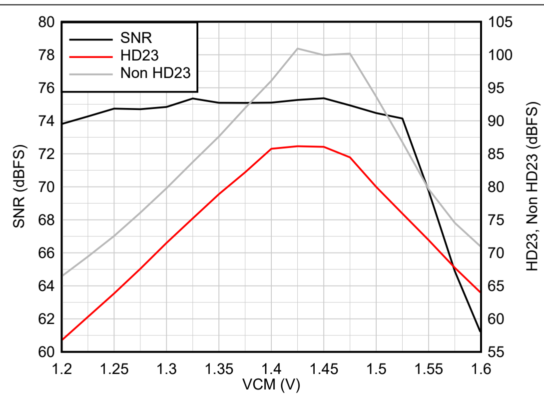
F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-47. AC Performance vs AVDD18



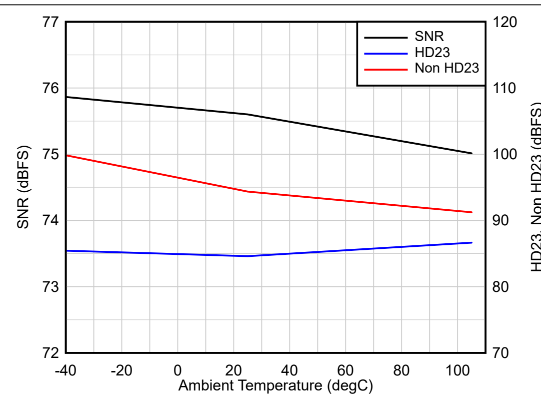
F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-48. AC Performance vs AVDD12



F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-49. AC Performance vs VCM



F_{IN} = 100MHz, A_{IN} = −1dBFS

Figure 6-50. AC Performance vs Temperature

6.11 Typical Characteristics, ADC3669 (continued)

Typical values are specified at T_A = 25°C, ADC sampling rate = 500MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted

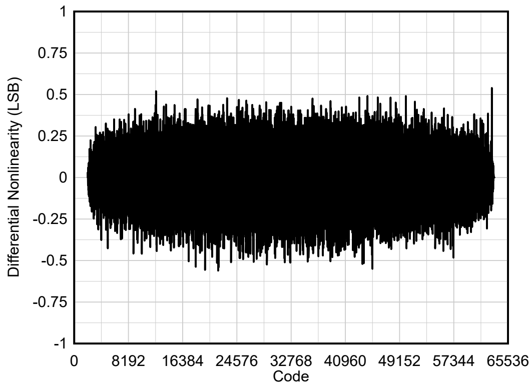


Figure 6-51. DNL

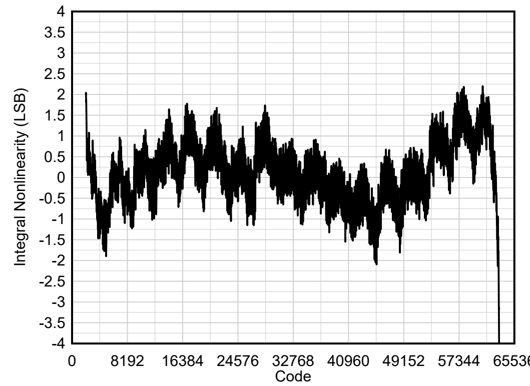


Figure 6-52. INL

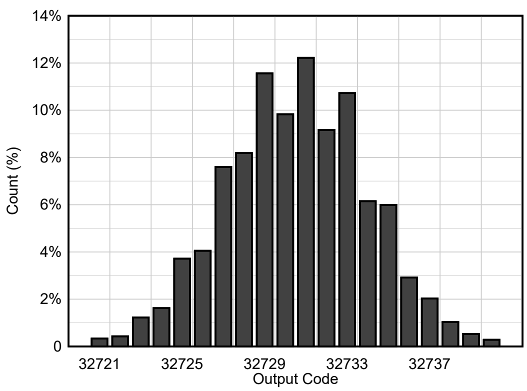


Figure 6-53. DC Offset Histogram

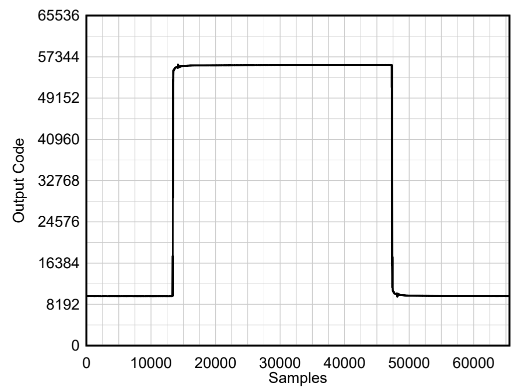
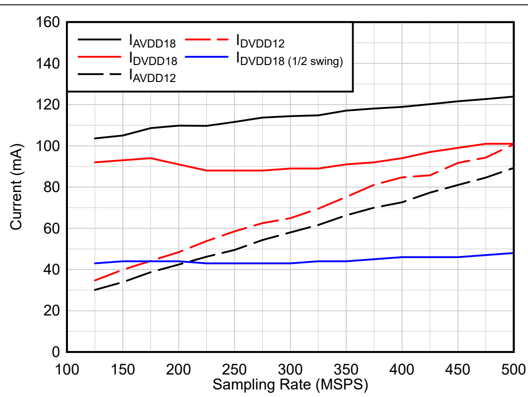
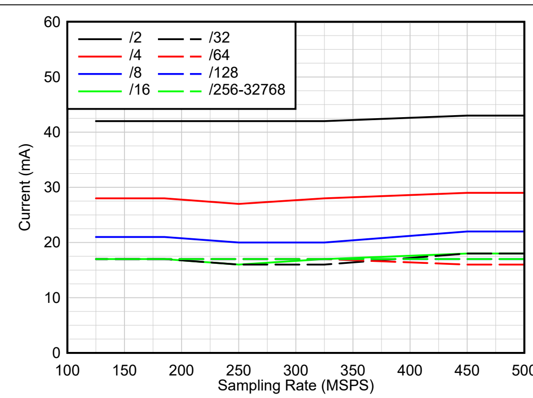


Figure 6-54. Pulse Response



Decimation bypass, DDR LVDS

Figure 6-55. Current vs Sampling Rate



Real Decimation, DVDD18

Figure 6-56. Current vs Sampling Rate

6.11 Typical Characteristics, ADC3669 (continued)

Typical values are specified at T_A = 25°C, ADC sampling rate = 500MSPS, DDC bypass mode, 50% clock duty cycle, nominal supply voltages and –1dBFS differential input, unless otherwise noted

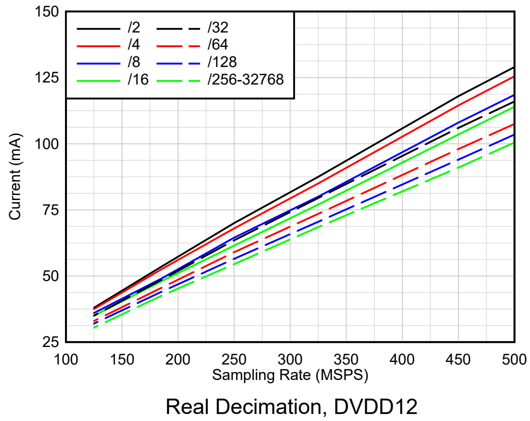


Figure 6-57. Current vs Sampling Rate

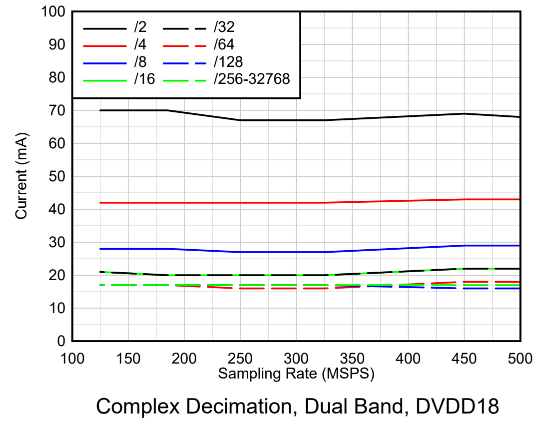


Figure 6-58. Current vs Sampling Rate

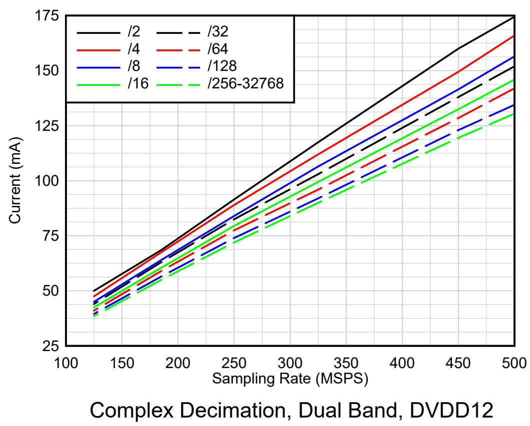


Figure 6-59. Current vs Sampling Rate

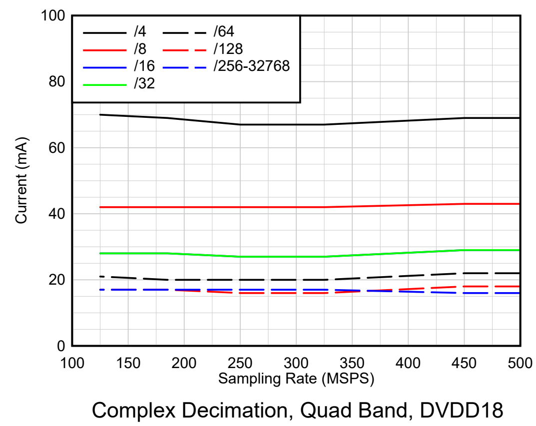


Figure 6-60. Current vs Sampling Rate

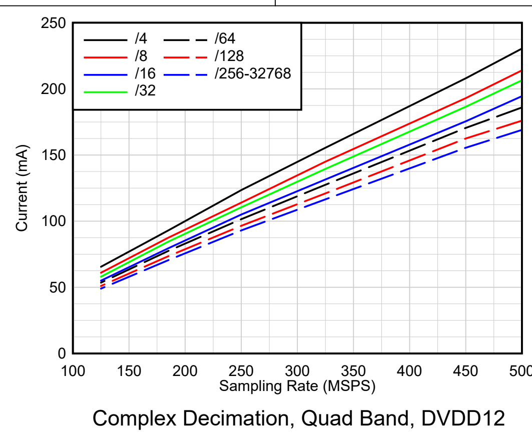


Figure 6-61. Current vs Sampling Rate

7 Parameter Measurement Information

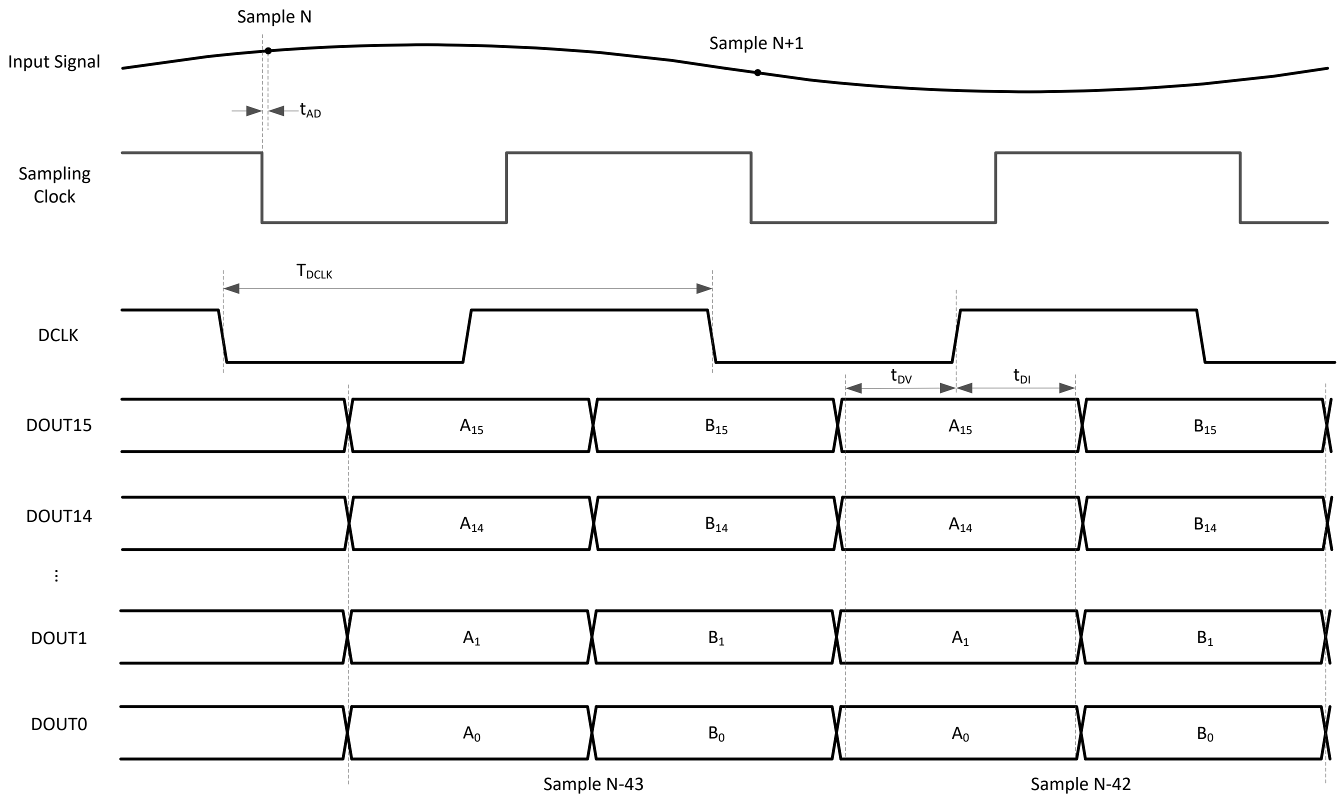


Figure 7-1. Timing Diagram: Parallel DDR LVDS

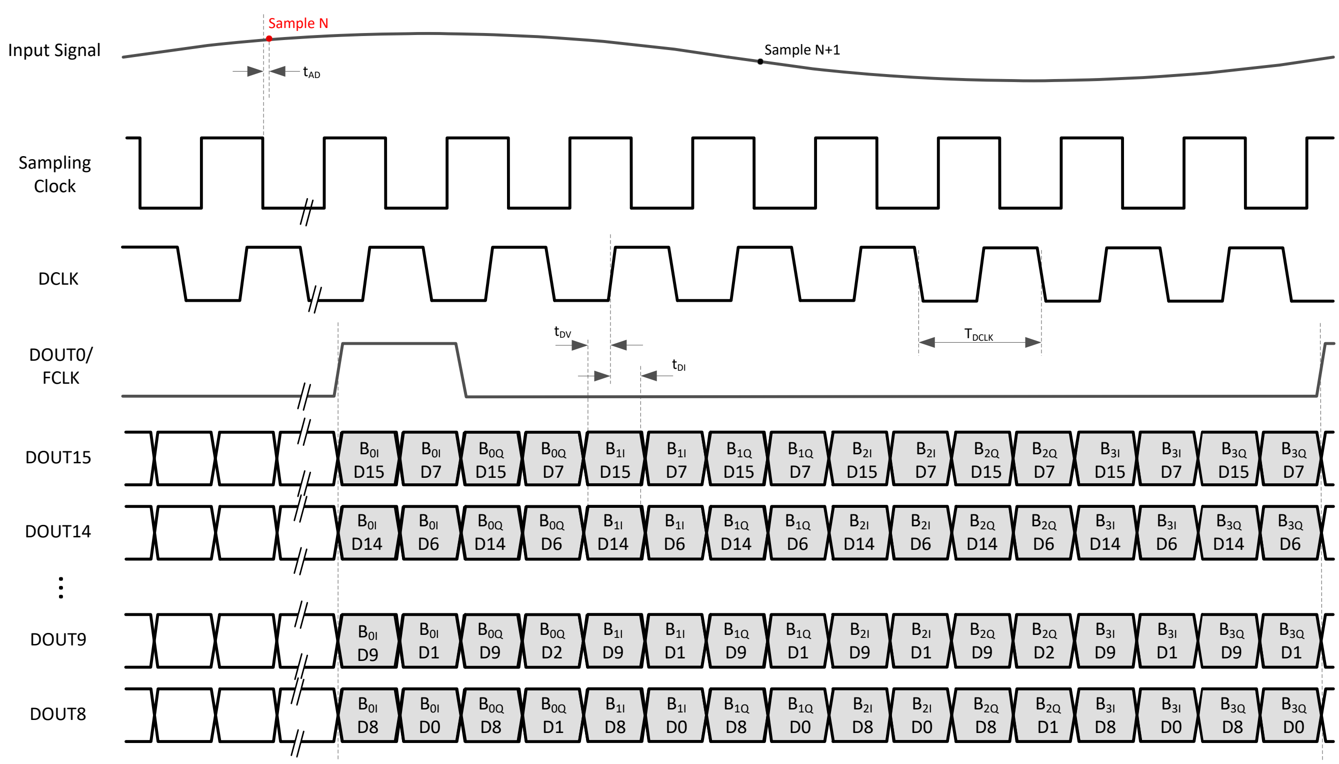


Figure 7-2. Timing Diagram: Serial LVDS (example: quad band, 16-bit, complex decimation by 8)

8 Detailed Description

8.1 Overview

The ADC366x is a 16-bit, 250 and 500MSPS, dual channel analog to digital converter (ADC). The device is designed for highest signal-to-noise ratio (SNR) and delivers a noise spectral density as low as −160dBFS/Hz. The buffered analog inputs support a programmable internal termination impedance of 100Ω and 200Ω with a full power input bandwidth of 1.4GHz (−3dB).

The ADC366x includes a quad band digital down-converter (DDC) supporting wideband decimation by 2 to narrow band decimation by 32768. The DDC uses a 48-bit NCO which supports phase coherent and phase continuous frequency hopping.

The ADC366x is outfitted with a flexible LVDS interface. In decimation bypass mode, the output data is transmitted over 16 LVDS pairs with a DDR clock. When using real or complex decimation, the output data is transmitted using a serial LVDS interface. Reducing the number of lanes used as decimation increases.

The power efficient ADC architecture consumes 300mW/ch at 500MSPS and provides power scaling with lower sampling rates (250mW/ch at 250MSPS).

8.2 Functional Block Diagram

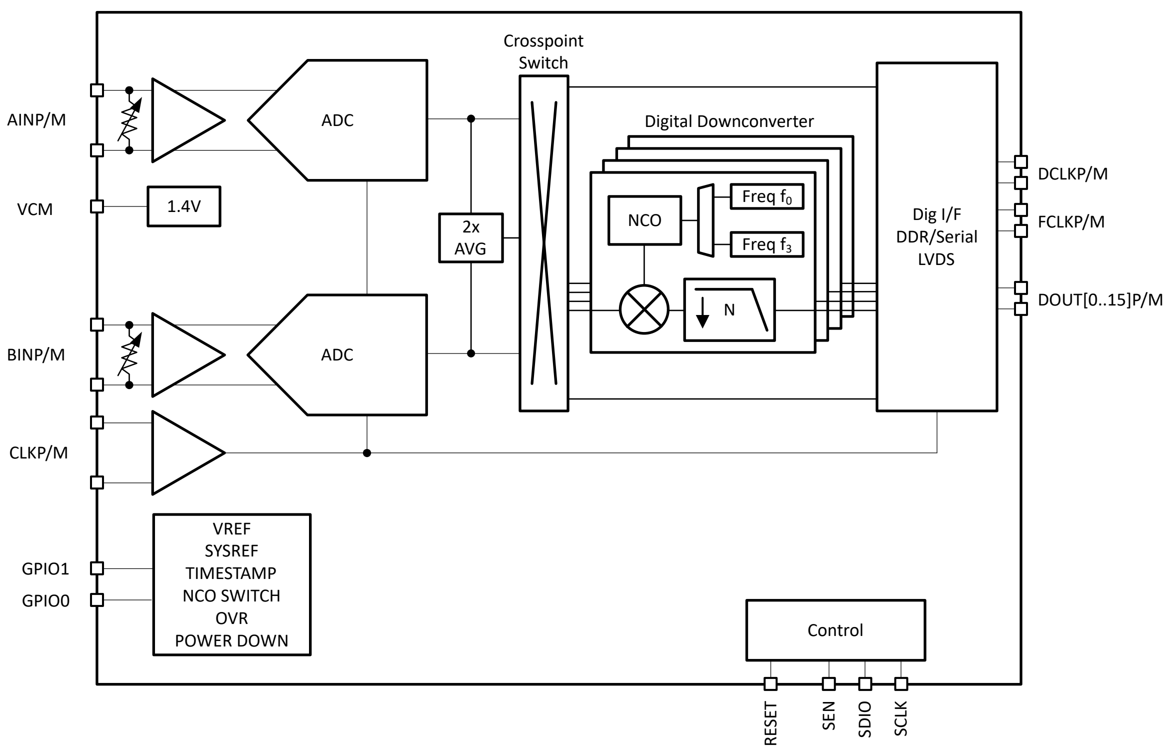


Figure 8-1. Block Diagram

8.3 Feature Description

8.3.1 Analog Inputs

The analog inputs of the ADC366x have internal buffers which isolate the sampling capacitor glitch noise from the external input circuitry. The analog inputs have a differential 100Ω split termination with internal biasing to V_{CM} as illustrated in the representative input model in Figure 8-2. This can be changed to differential 200Ω termination via SPI register write.

The input fullscale is 2Vpp and the V_{CM} is 1.4V; thus, the voltage on the analog inputs swing between 0.9V and 1.9V. The ADC inputs are reliably designed to support 1.9V for normal operation.

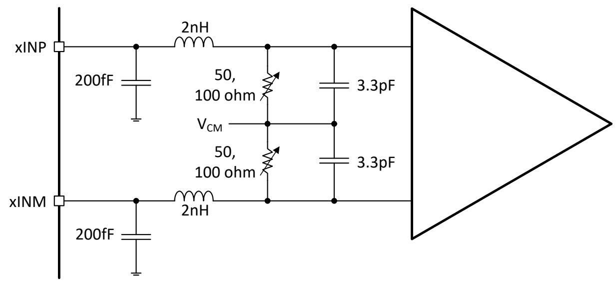


Figure 8-2. Analog input internal termination

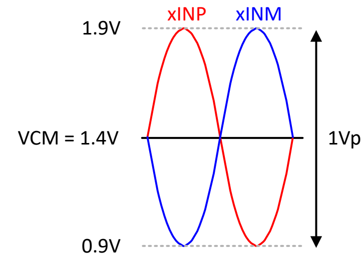


Figure 8-3. Analog input voltage range

The device supports both AC and DC coupling of the analog inputs as shown in Figure 8-4 and Figure 8-5.

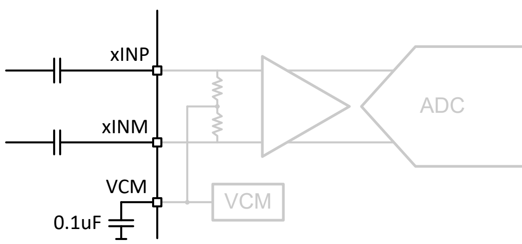


Figure 8-4. AC coupling

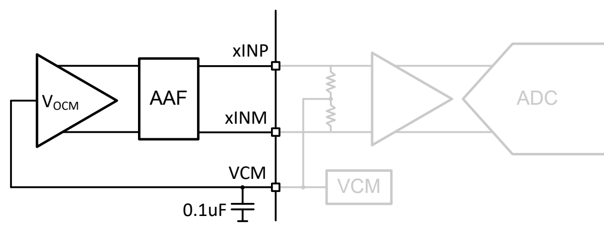


Figure 8-5. DC coupling

The input bandwidth (-3dB) for internal 100 and 200Ω termination are shown in Figure 8-6.

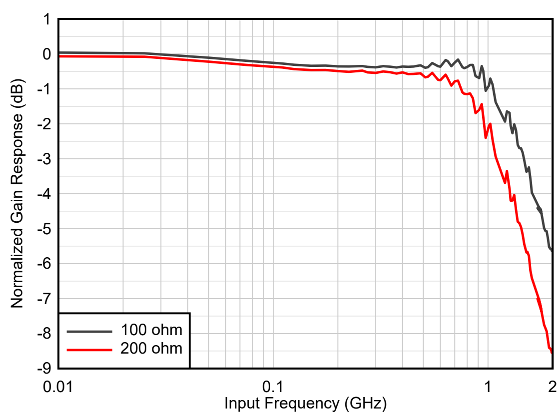


Figure 8-6. Full power input banwidth for 100 and 200Ω internal termination

8.3.1.1 Nyquist Zone Selection

The ADC includes a digital error correction which is optimized based on which Nyquist zone the signal of interest is in. For optimum performance the correct input frequency range (register 0x132) and Nyquist zone have to be selected in the SPI register map (register 0x16B). By default the first Nyquist zone is selected.

8.3.1.2 Analog Front End Design

To optimize SNR and HD3 performance of the ADC, the recommendation is to add a RCR circuitry directly in front of the analog input. Figure 8-7 shows the recommended RCR circuitry for input frequencies less and greater than 500MHz (example shows AC coupling but same applies to DC coupling), assumimg a 50Ω source impedance. If the ADC is driven by an external amplifier, the RCR circuitry may not be needed.

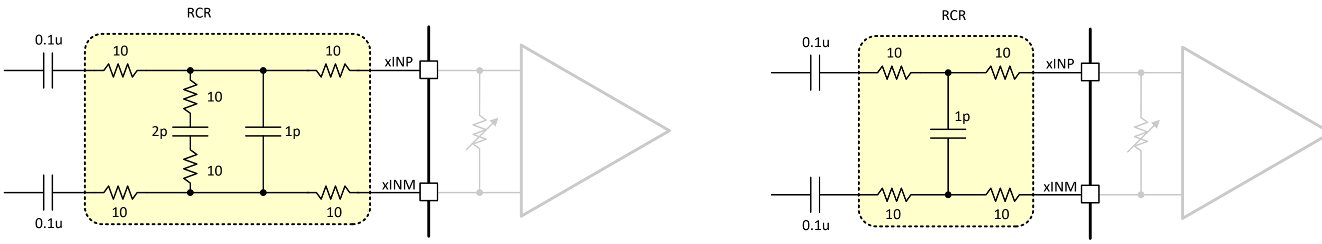


Figure 8-7. External RCR for F_{IN} < 500MHz (left) and F_{IN} > 500MHz (right)

8.3.2 Sampling Clock Input

The sampling clock input is designed to be driven differentially with external AC coupling and termination. The ADC provides internal common mode voltage biasing as shown in Figure 8-8.

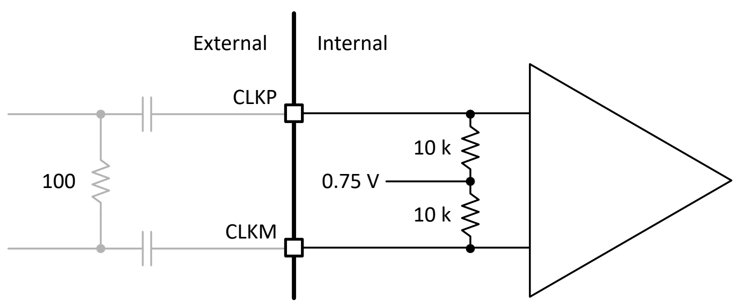


Figure 8-8. Sampling Clock Input Circuitry

The internal sampling clock path was designed for low residual phase noise contribution. The sampling clock circuitry requires a dedicated, low noise power supply for best phase noise and jitter performance. The internal residual clock phase noise is also sensitive to clock amplitude.

The internal residual clock noise consists of two components: 1) phase noise and 2) amplitude noise as shown in Table 8-1. The phase noise scales with input frequency and sampling rate ($20*\log(f_{IN}/F_S)$) while the amplitude noise does not scale.

Table 8-1. Phase and Amplitude Noise at F_S = 500MHz

Frequency Offset (MHz)	Phase Noise (dBc/Hz)	Amplitude Noise (dBc/Hz)
0.001	−130	−129
0.01	−140	−139
0.1	−150	−149
1	−160	−159
3	−165	−164
10	−165	−164

Figure 8-9 and Figure 8-10 show the phase and amplitude noise at three different input frequencies.

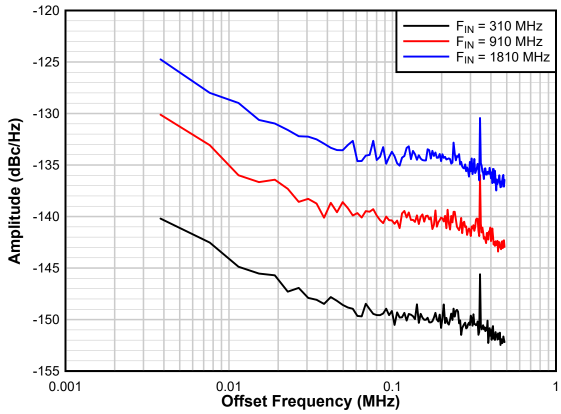


Figure 8-9. Phase Noise Examples

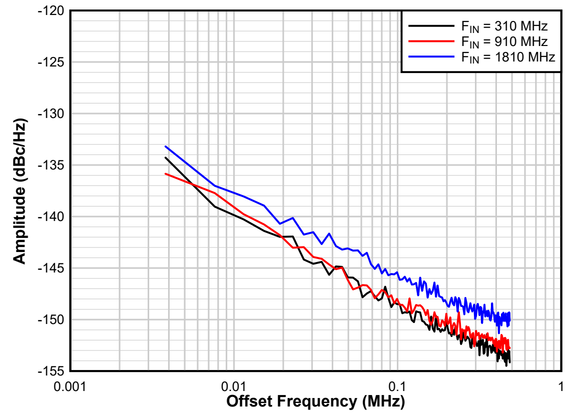


Figure 8-10. Amplitude Noise Examples

The internal clock noise is also dependent on the external clock amplitude. Figure 8-11 to Figure 8-14 show the expected AC performance for different input frequencies across clock amplitude.

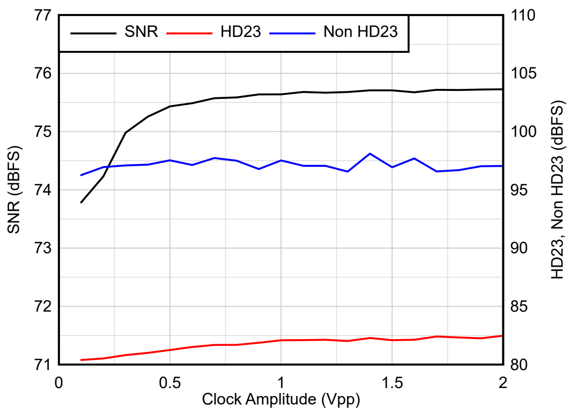


Figure 8-11. AC vs Clock Amplitude
F_S = 500MSPS, F_{IN} = 100MHz, A_{IN} = −1dBFS

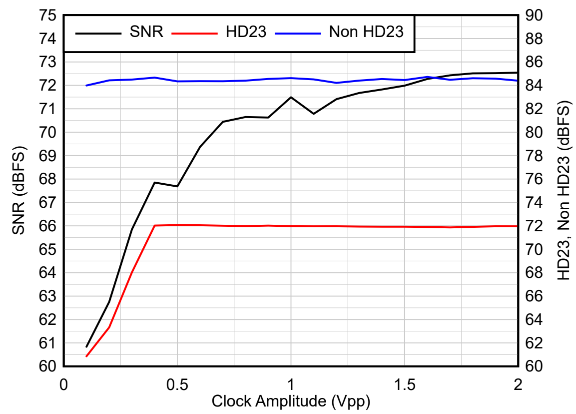


Figure 8-12. AC vs Clock Amplitude
F_S = 500MSPS, F_{IN} = 400MHz, A_{IN} = −1dBFS

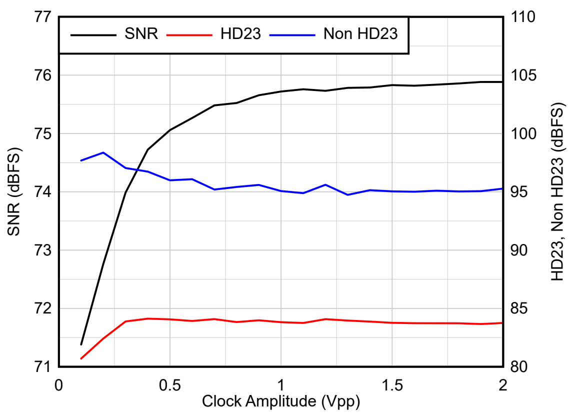


Figure 8-13. AC vs Clock Amplitude
F_S = 250MSPS, F_{IN} = 100MHz, A_{IN} = −1dBFS

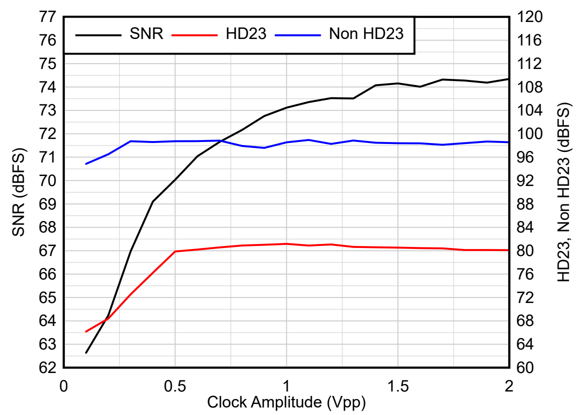


Figure 8-14. AC vs Clock Amplitude
F_S = 250MSPS, F_{IN} = 240MHz, A_{IN} = −1dBFS

8.3.3 Multi-Chip Synchronization

The device provides an option to achieve deterministic latency to ease synchronization across multiple devices, depending on operating mode:

- DDC Bypass mode: The device inherently already has deterministic latency. External multi-chip synchronization is accomplished by matching clock traces across devices. However, the internal RAMP test pattern can be reset using the SYSREF signal.
- DDC mode: Internal blocks related to the decimation filter (clock dividers, NCO phase, and so on) are reset to a deterministic state using the SYSREF signal. External multi-chip synchronization is accomplished by matching both clock and SYSREF signal traces (blue lines) across devices as shown in Figure 8-15.

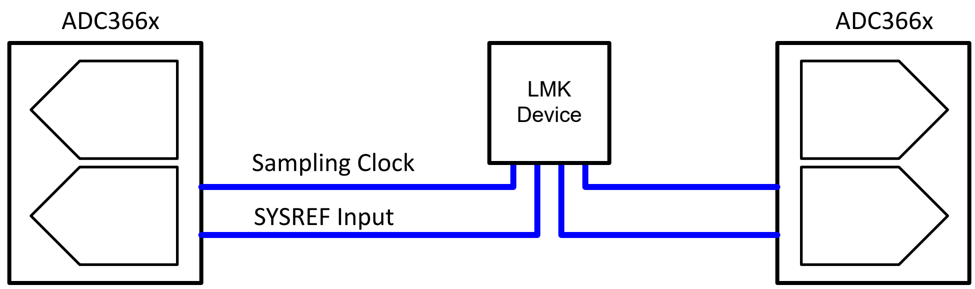


Figure 8-15. Synchronization example of 2 devices

The GPIO0 pin can be configured as a synchronization input. A single pulse can be applied for multi-chip synchronization as shown in Figure 8-16.

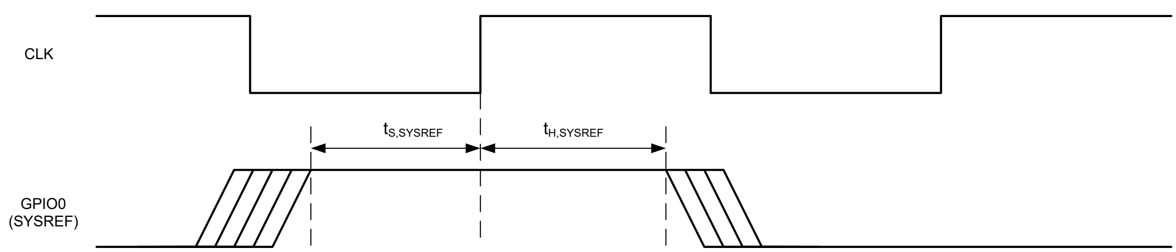


Figure 8-16. Timing: external synchronization input

In the SPI register map, there are several different synchronization masks available to reset only specific blocks such as the NCO phase.

Table 8-2. Example register writes for external SYSREF config

ADDR	DATA	DESCRIPTION
0x146	0x00	Configure pin GPIO0 as SYSREF input

8.3.3.1 SYSREF Monitor

The SYSREF input signal rising edge must be edge aligned with the falling edge of the sampling clock to maximize the setup and hold times. The SYSREF signal is internally sampled on the rising edge of the sampling clock plus 60ps.

The device includes an internal SYSREF monitoring circuitry to detect a possible SYSREF logic level metastability close to the sampling instant of SYSREF which can lead to misalignment across devices. The SYSREF monitoring circuitry provides insights into SYSREF/clock misalignment by detecting whether a SYSREF logic state transition is within -60ps to +140ps of the sampling clock rising edge. This circuitry detects and raises one of the SYSREF XOR flags corresponding to the matching SYSREF window below:

- Window XOR1: SYSREF leading sample clock by 20 to 60ps
- Window XOR2: SYSREF leading sample clock by 20ps to 0ps or SYSREF lagging sample clock by 0 to 20ps
- Window XOR3: SYSREF lagging sample clock by up to 20 to 60ps
- Window XOR4: SYSREF lagging sample clock by 60 to 100ps
- Window XOR5: SYSREF lagging sample clock by 100 to 140ps

The SYSREF monitor registers are updated at every rising edge of SYSREF. The <SYSREF DET> register (D6) is sticky (indicating a SYSREF edge was detected) and needs to be cleared manually.

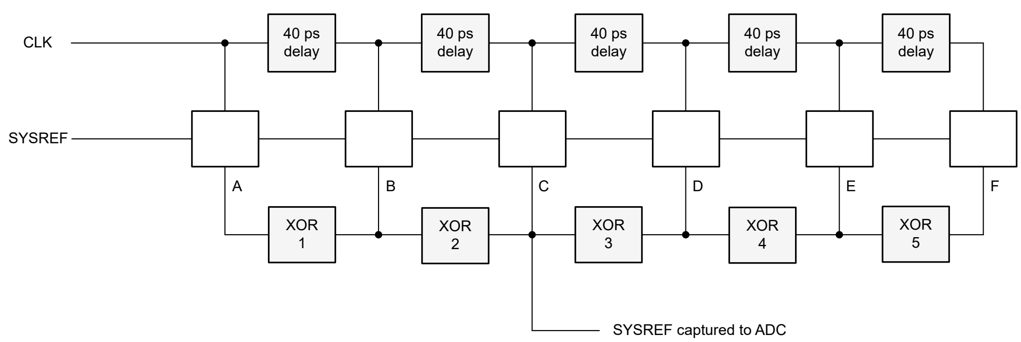


Figure 8-17. SYSREF Detection Circuitry

The example in Figure 8-18 shows a misaligned SYSREF signal where the SYSREF signal arrives much later than the sampling clock falling edge. In this example, the delayed SYSREF signal transitions between the "B" and "C" flip flop which raises the XOR2 flag. The XOR flags get reported in register 0x140. In this example, Register 0x140 reads back 0x62, as shown in Table 8-3.

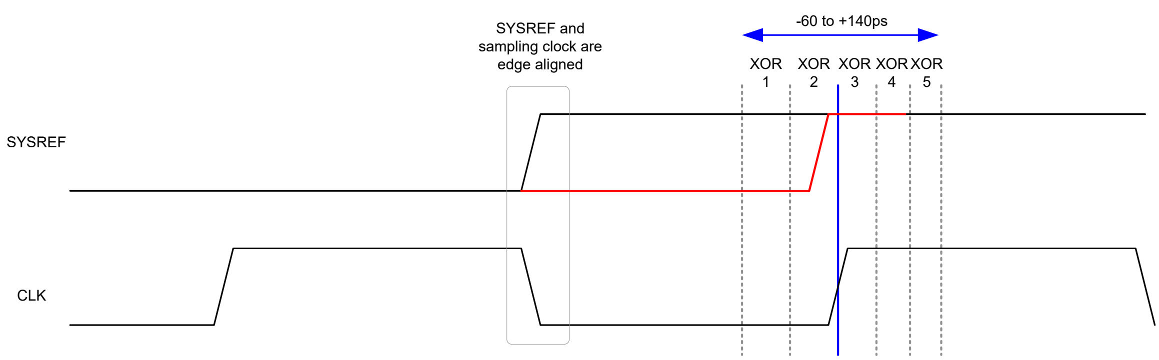


Figure 8-18. Detection of SYSREF Transition Within Capture Window

Table 8-3. SYSREF Window Register Example (0x140)

ADDR	D7	D6	D5	D4	D3	D2	D1	D0
0x140	0	SYSREF DET	SYSREF OR	SYSREF X5	SYSREF X4	SYSREF X3	SYSREF X2	SYSREF X1
	0	1	1	0	0	0	1	0

8.3.4 Time-Stamp

The ADC366x includes a time-stamp feature which enables tagging a specific sample on the analog input in DDC bypass mode. When enabling the feature (via SPI write), a logic low-to-high transition on the GPIO/SYSREF pin is registered on the rising edge of the sampling clock. The time stamp signal is output on the lane DOUT0 (LSB); however, the signal is not latency matched with the output data.

As shown in Figure 8-19 the time stamp signal is indicated 35 clock cycles ahead of the output data:

- Latency output data: 43 clock cycles
- Latency time stamp output: 8 clock cycles

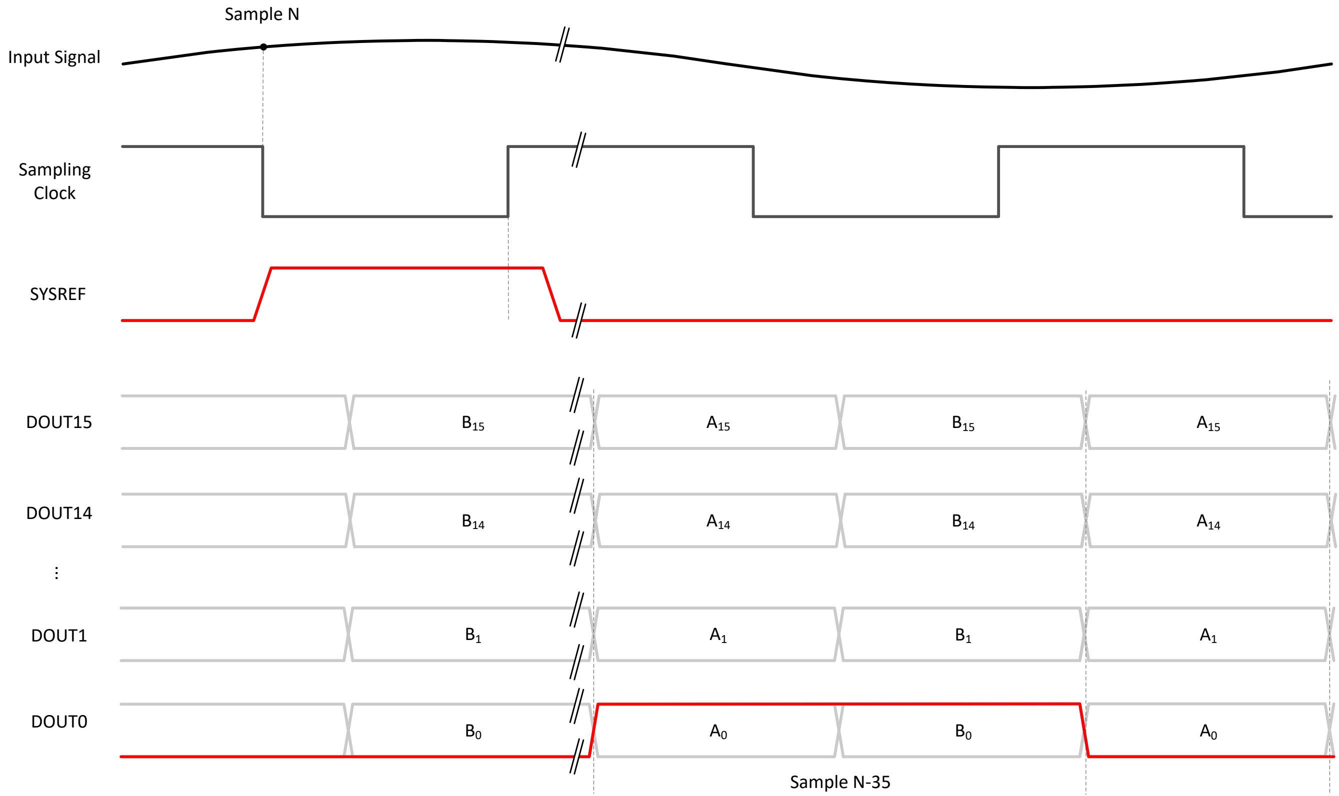


Figure 8-19. Timing Diagram - Time Stamp

Table 8-4. Example register writes to enable time stamp on pin GPIO0

ADDR	DATA	DESCRIPTION
0x146	0x00	Enable SYSREF on pin GPIO0.
0x162	0xC0	Enable time stamp function replacing the LSB.

8.3.5 Overrange

The device triggers the over-range indicator when the signal crosses the representable digital range (max code). The over-range output can be configured in registers 0x10A/0x10B. The latency of the OVR indication is equal or less than the data latency.

The OVR can be indicated in two different ways:

- GPIO pin: one GPIO OVR pin per channel or one GPIO pin with the OVR signal of both ADCs OR-ed together (register 0x146)
- LSB data: the OVR signal replaces the LSB of each channel output data (register 0x116). In decimation mode, the OVR signal replaces the LSB in the DDC output stream to which the ADC is connected (controlled via the DDC mux input).

8.3.6 External Voltage Reference

For highest accuracy and lowest temperature drift, an external 1.2V voltage reference can be supplied to the ADC. The external reference can be supplied through pin GPIO1 (configured via SPI). The recommendation is to connect a 10µF and a 0.1µF ceramic bypass capacitor (C_{VREF}) between the GPIO1 and AGND pins and placed as close to the pins as possible.

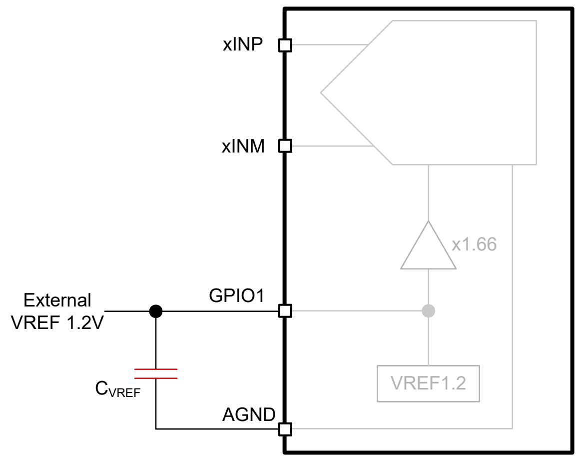


Figure 8-20. External Voltage Reference

8.3.7 Digital Gain

The device includes a programmable digital gain for both channels. The gain is programmed in registers 0x15B (CHA) and 0x15C (CHB). The 8-bit register field is 7 bit with a sign bit (2s complement).

The actual gain in dB is: 20 x log (1 + (7 bit gain / 128))

For example a register value of 0x7F corresponds to a digital gain of 6dB, 0xC0 corresponds to a digital gain of −6dB.

8.3.8 Decimation Filter

The ADC366x provides up to four digital down converters as shown in Figure 8-21. Using the cross point switch with SPI register writes, any of the four DDC can be connected to any ADC or the output of the 2x AVG block. In dual band mode (2 DDC), decimation from /2 to /32768 is supported. While in 4 DDC mode, the lowest decimation possible is /4 as shown in Table 8-5. Real (single band only) and complex decimation are supported. In real decimation, the passband is approximately 40% and in complex decimation the passband is approximately 80% as illustrated in Table 8-6.

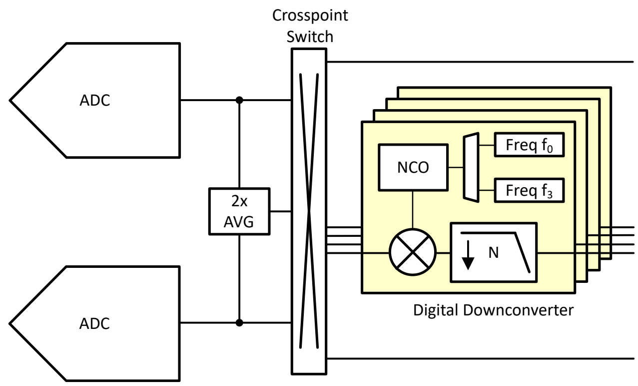


Figure 8-21. Internal digital down converter

Table 8-5. Summary of different decimation filter band options

# of DDCs	Min Decimation	Max Decimation
2	/2	/32768
4	/4	/32768

Table 8-6. Complex decimation and real decimation vs output bandwidth

Decimation Factor (complex)	Complex Output Bandwidth per DDC	Real Output Bandwidth per DDC
N	0.8 x F_S / N	0.4 x F_S / N

Decimation is enabled by setting the <COMMON DECIMATION> SPI register (0x169, D3-D0). By default, the setting is to 'real' decimation. 'Complex' decimation is enabled with register <COMPLEX EN> (0x162, D2).

8.3.8.1 Uncommon Decimation Ratios

The DDC can be programmed to have unequal, independent decimation ratios. The output data rate is based on the decimation filter with the lowest decimation ratio. The output samples of the DDC with higher decimation factors are repeated in the output data stream accordingly. For example if DDC0 is set to /4 and DDC1 to /8, then the output data rate of DDC0 is twice as fast as DDC1 (F_{out0} = F_S/4 vs F_{out1} = F_S/8). Therefore, the output samples of DDC1 are repeated once as illustrated in Figure 8-22.

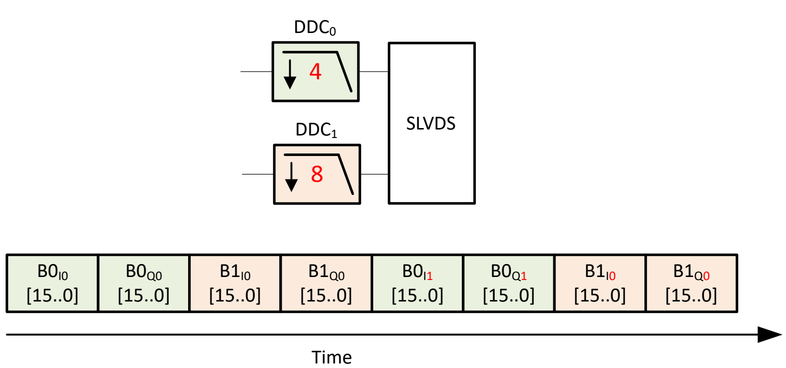


Figure 8-22. Unequal Decimation Factors

8.3.8.2 Decimation Filter Response

This section provides the different decimation filter responses with a normalized ADC sampling rate. The complex filter pass band is approximately 80% (−1dB) with a minimum of 85dB stop band rejection.

The decimation filter responses are normalized to the ADC sampling clock frequency FS and illustrated in Figure 8-24 to Figure 8-53. Each figure contains the filter pass-band, transition band and alias or stop-band as shown in Figure 8-23. The x-axis shows the offset frequency (after the NCO frequency shift) normalized to the ADC sampling rate F_S.

For example, in the divide-by-4 complex setup, the output data rate is F_S / 4 complex with a Nyquist zone of F_S / 8 or 0.125 × F_S. The transition band (colored in blue) is centered around 0.125 × F_S and the alias transition band is centered at 0.375 × F_S. The stop-bands (colored in red), which alias on top of the pass-band, are centered at 0.25 × F_S and 0.5 × F_S. The stop-band attenuation is greater than 85dB.

Note

For higher decimation ratios (/32 onward), the far out transition and stop-bands exceeds -120dB. The decimation filter plots show only the relevant closer in response with attenuation less than -120dB.

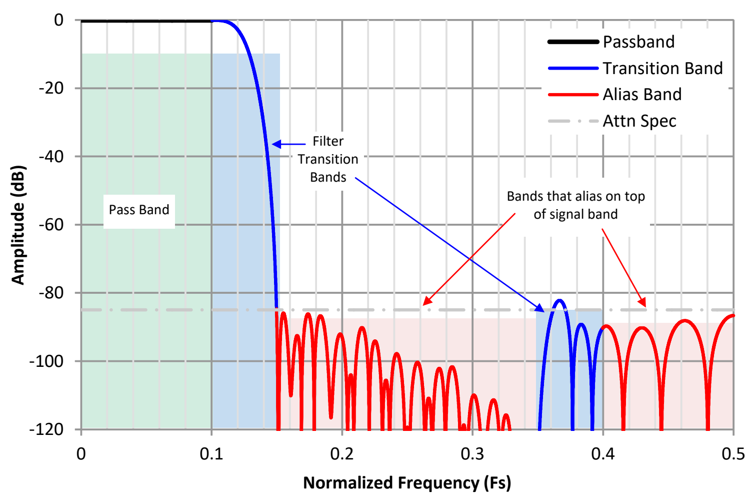


Figure 8-23. Interpretation of the Decimation Filter Plots

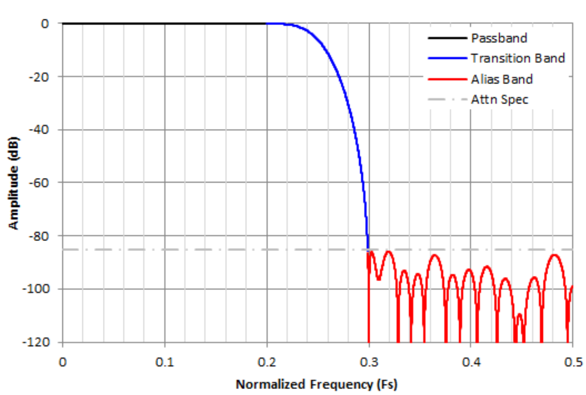


Figure 8-24. Complex Decimation by 2 Filter Response

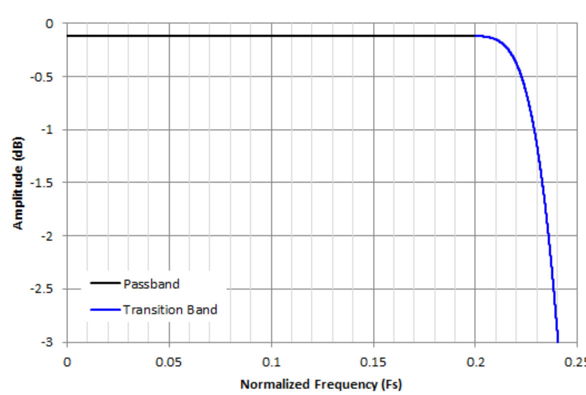


Figure 8-25. Decimation by 2 Passband Ripple Response

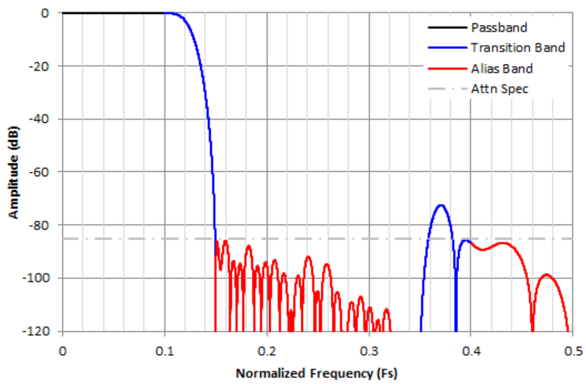


Figure 8-26. Complex Decimation by 4 Filter Response

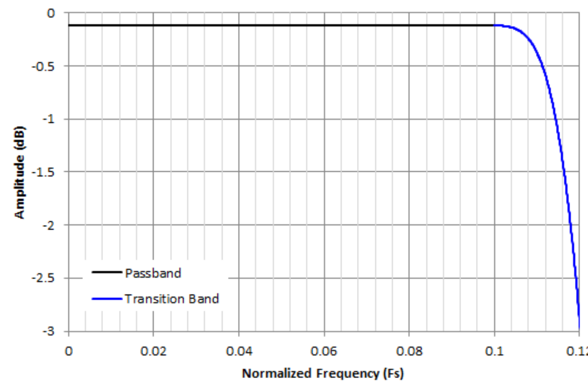


Figure 8-27. Decimation by 4 Passband Ripple Response

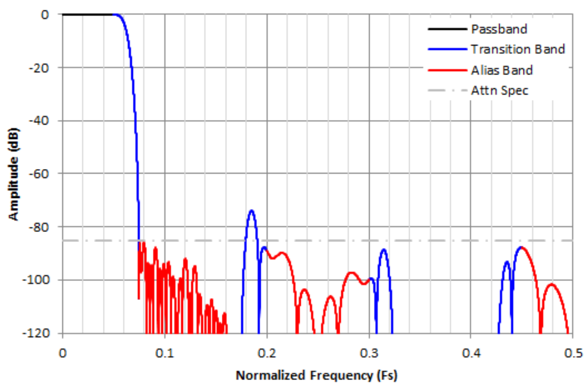


Figure 8-28. Complex Decimation by 8 Filter Response

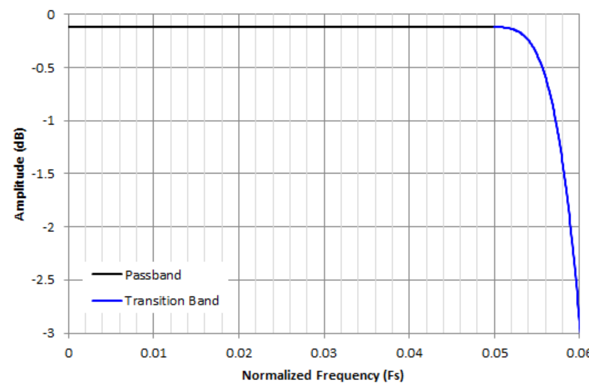


Figure 8-29. Decimation by 8 Passband Ripple Response

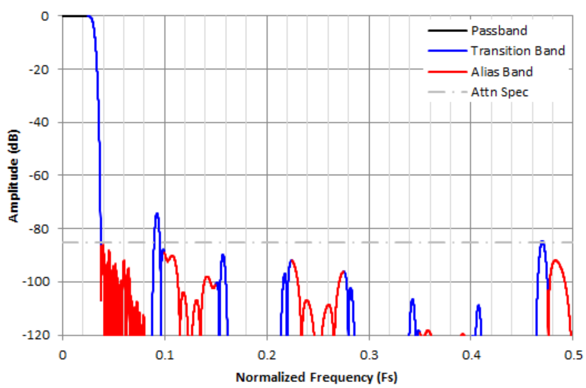


Figure 8-30. Complex Decimation by 16 Filter Response

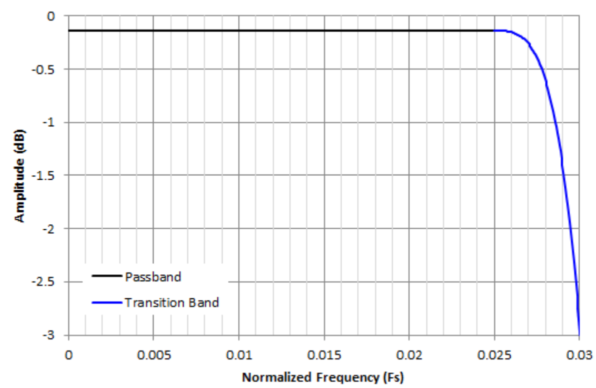


Figure 8-31. Decimation by 16 Passband Ripple Response

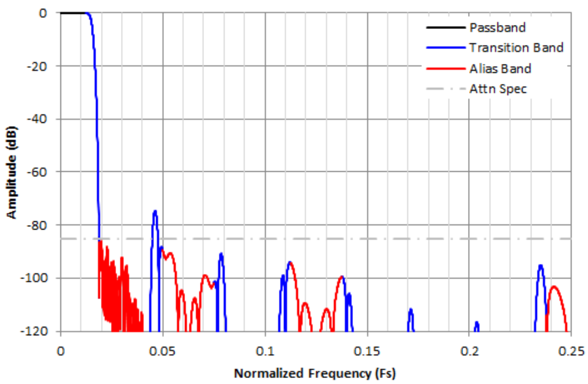


Figure 8-32. Complex Decimation by 32 Filter Response

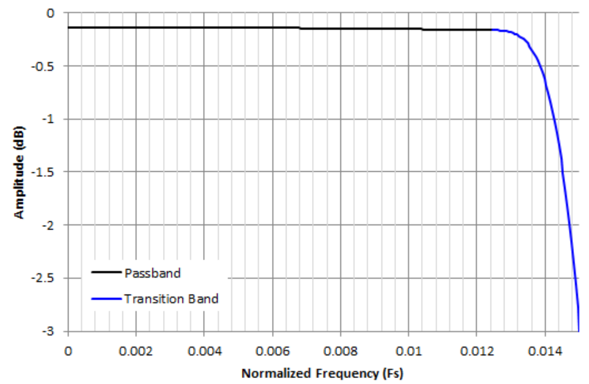


Figure 8-33. Decimation by 32 Passband Ripple Response

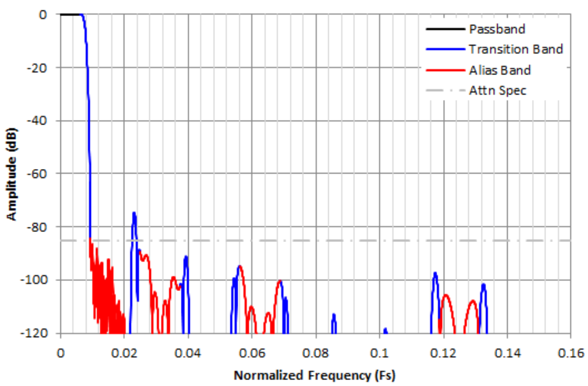


Figure 8-34. Complex Decimation by 64 Filter Response

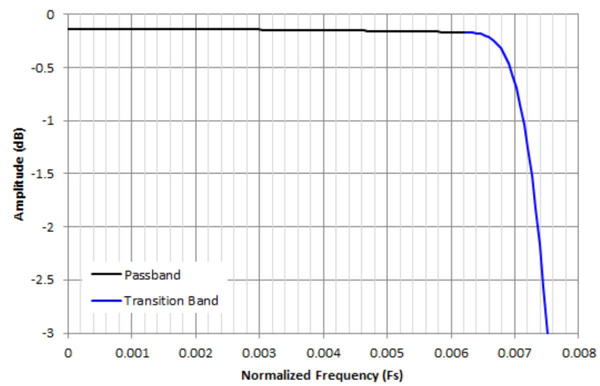


Figure 8-35. Complex Decimation by 64 Filter Ripple Response

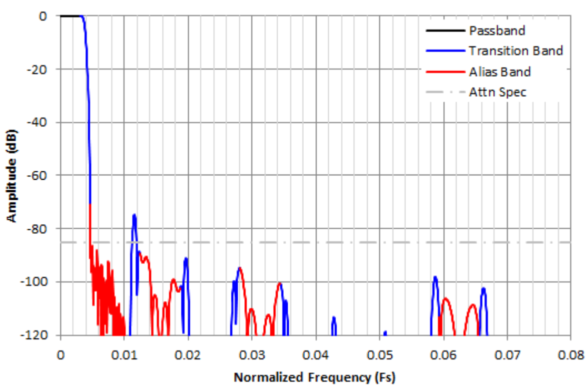


Figure 8-36. Complex Decimation by 128 Filter Response

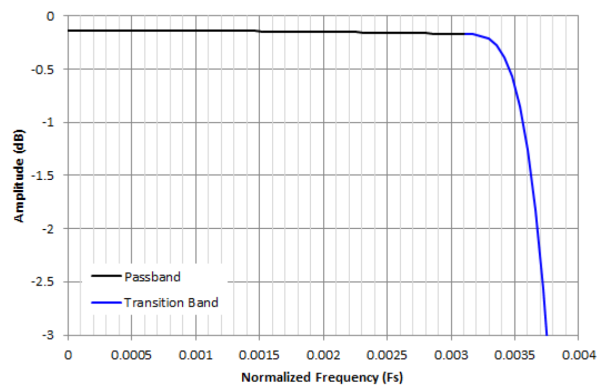


Figure 8-37. Decimation by 128 Passband Ripple Response

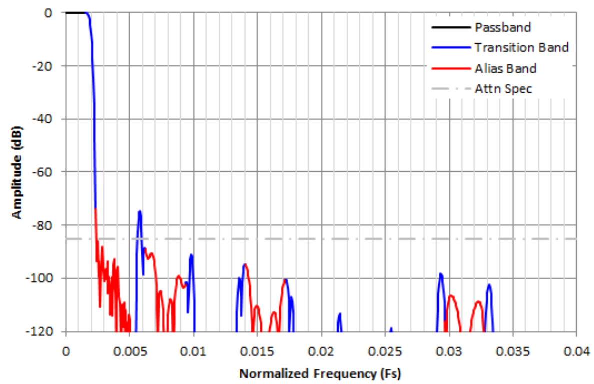


Figure 8-38. Complex Decimation by 256 Filter Response

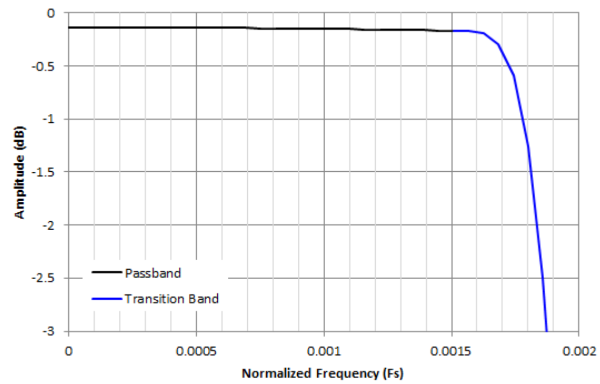


Figure 8-39. Decimation by 256 Passband Ripple Response

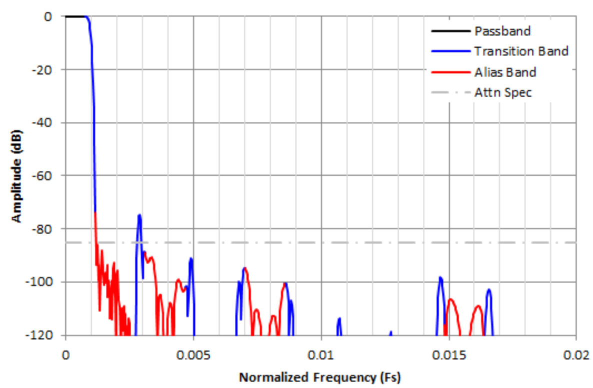


Figure 8-40. Complex Decimation by 512 Filter Response

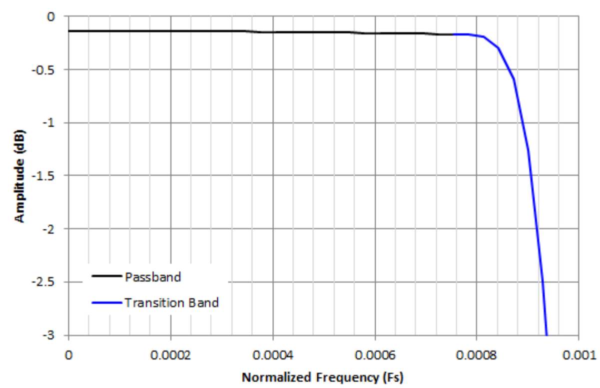


Figure 8-41. Decimation by 512 Passband Ripple Response

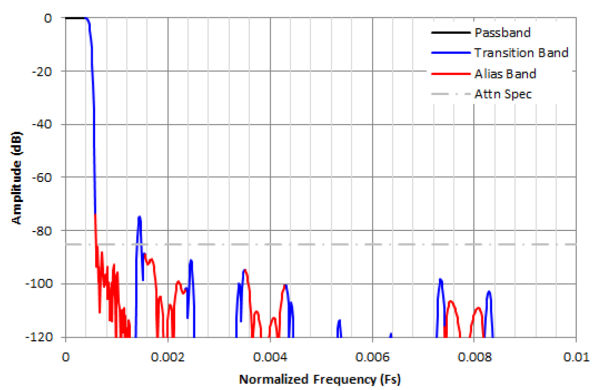


Figure 8-42. Complex Decimation by 1024 Filter Response

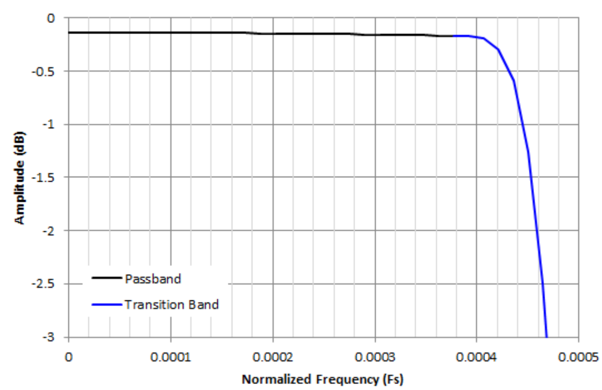


Figure 8-43. Decimation by 1024 Passband Ripple Response

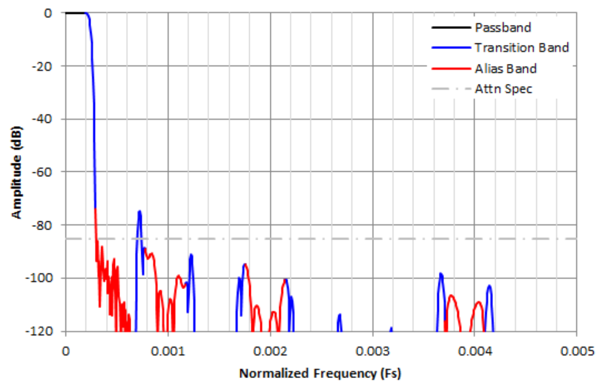


Figure 8-44. Complex Decimation by 2048 Filter Response

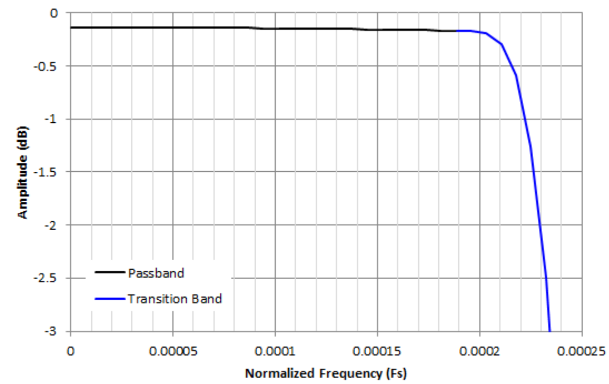


Figure 8-45. Decimation by 2048 Passband Ripple Response

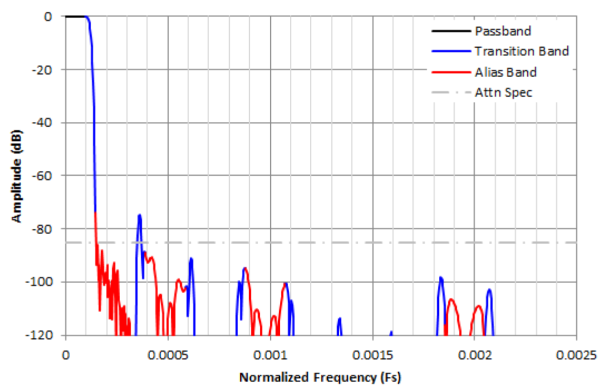


Figure 8-46. Complex Decimation by 4096 Filter Response

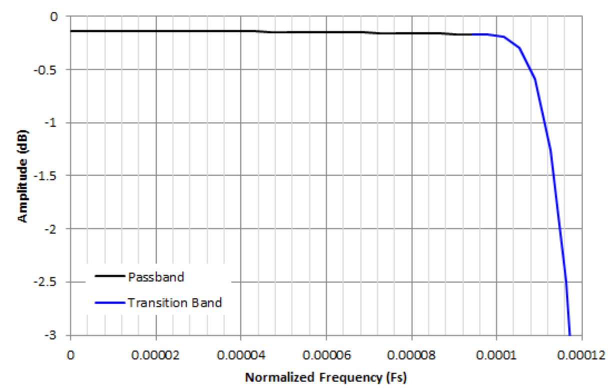


Figure 8-47. Decimation by 4096 Passband Ripple Response

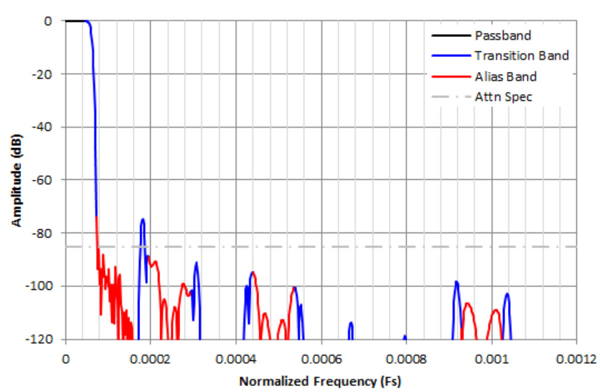


Figure 8-48. Complex Decimation by 8192 Filter Response

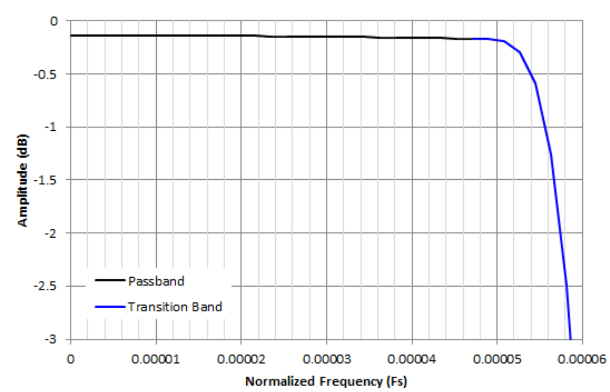


Figure 8-49. Decimation by 8192 Passband Ripple Response

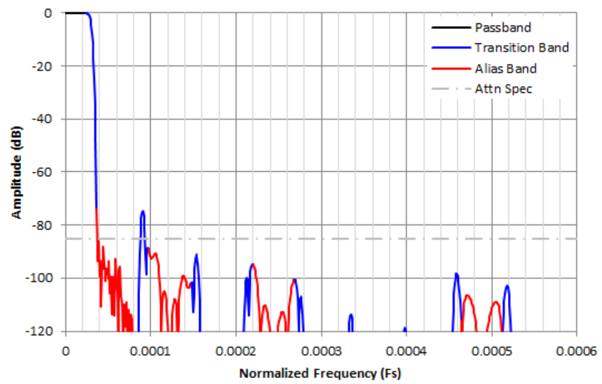


Figure 8-50. Complex Decimation by 16384 Filter Response

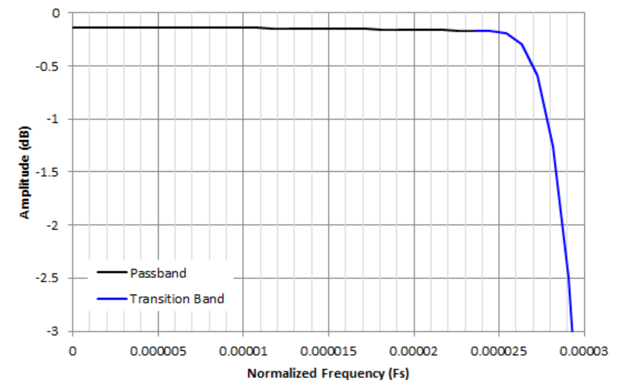


Figure 8-51. Decimation by 16384 Passband Ripple Response

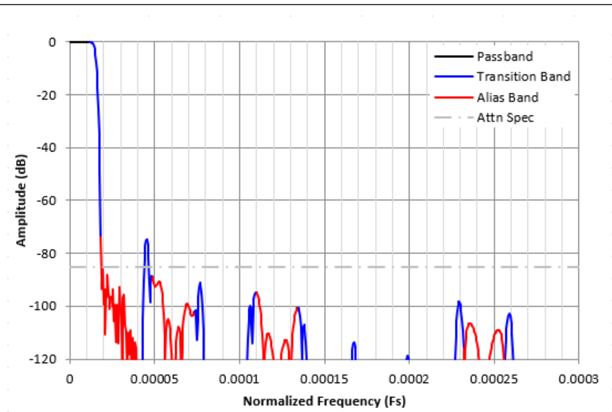


Figure 8-52. Complex Decimation by 32768 Filter Response

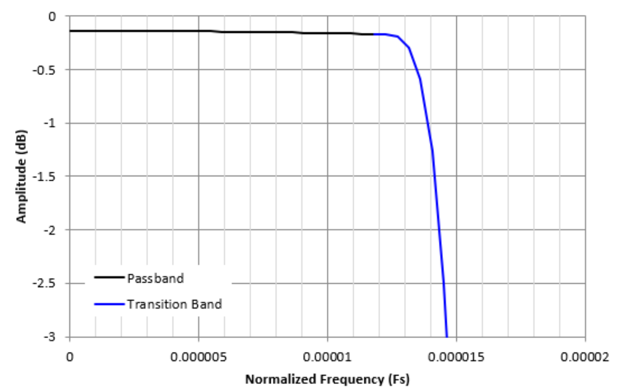


Figure 8-53. Decimation by 32768 Passband Ripple Response

8.3.8.3 Decimation Filter Configuration

The operation of the digital decimation filters can be controlled using registers 0x163 to 0x169. The NCO frequencies are mapped to registers 0x200 to 0x2DF. The DDC is versatile and can support many operating modes.

Table 8-7. Configuration of the DDCs

ADDR	DESCRIPTION
0x163	Select which ADC is connected to which DDC. By default each ADC is connected to two DDC.
0x164	Select NCO mode and update NCO frequencies
0x165	Configure NCO frequency update
0x166	Assign NCO frequency 0..3 to each NCO
0x167/168	Select Decimation for each DDC if unequal decimation factors are used
0x169	Configure # of DDC and common decimation factor

The following sequence can be used to configure the DDC for a static operating mode (either fixed NCO/slow changing NCO frequencies): Complex decimation /1024, quad band 32-bit output

Table 8-8. DDC Example Configuration

ADDR	DATA	DESCRIPTION
0x162	0x06	Select complex decimation, 32-bit output resolution.
0x169	0x1A	Configuration to 4x DDC (quad band) with common decimation of 1024.

8.3.8.4 Numerically Controlled Oscillator (NCO)

Each digital down-converter (DDC) uses a 48-bit numerically controlled oscillator (NCO) to fine tune the frequency placement prior to the digital filtering. Up to four different NCO frequencies for each DDC are programmed using SPI register writes. The digital NCOs are designed to have a SFDR of at least 100dB.

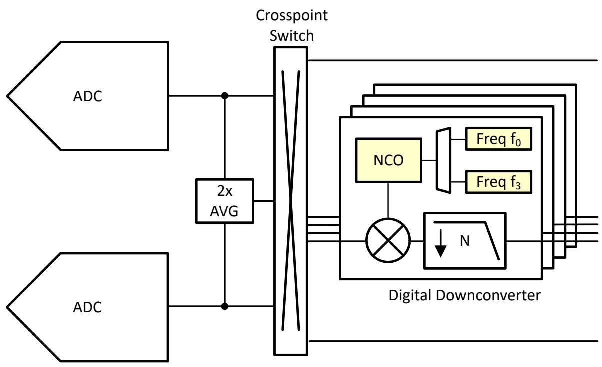


Figure 8-54. NCO Block Diagram

There are two different NCO operating modes, phase continuous and infinite phase coherent.

1. Phase Continuous NCO

   During a NCO frequency change, the NCO phase gradually adjusts to the new frequency as shown in Figure 8-55 (left). The 'dashed' line shows the phase of original f_1 frequency.
2. Infinite Phase Coherent NCO

   With a phase coherent NCO, all frequencies are synchronized to a single event using SYSREF. This enables an infinite amount of frequency hops without the need to reset the NCO as phase coherency is maintained between frequency hops. This is illustrated in Figure 8-55 (right). When returning to the original frequency f_1 the NCO phase appears as if the NCO had never changed frequencies.

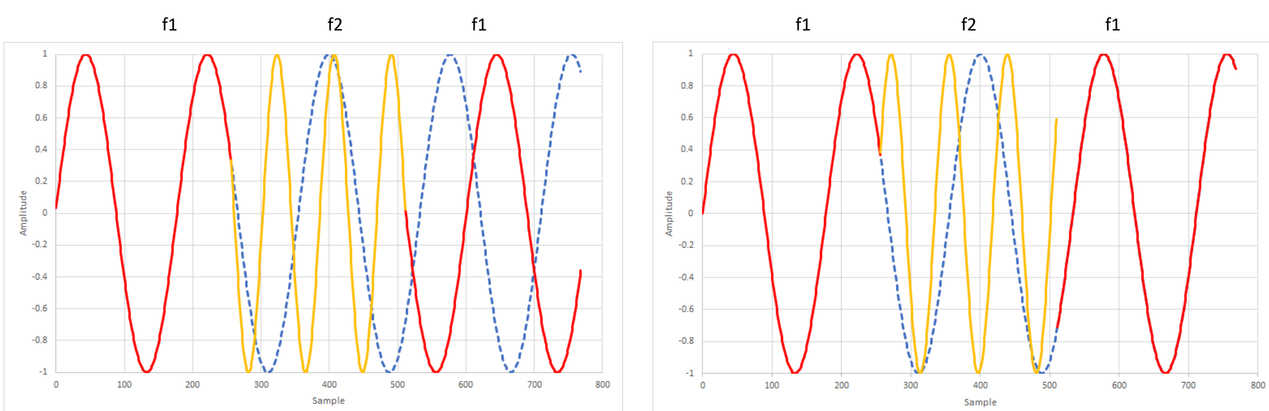


Figure 8-55. Phase Continuous (left) and Infinite Phase Coherent (right) NCO Frequency Switching

The oscillator generates a complex exponential sequence of:

$$e^{j\omega n} \text{ (default) or } e^{-j\omega n} \quad (1)$$

where: frequency (ω) is specified as a signed number by the 48-bit register setting

The complex exponential sequence is multiplied with the real input from the ADC to mix the desired carrier to a frequency equal to f_{IN} + f_{NCO}. The NCO frequency can be tuned from $-F_S/2$ to $+F_S/2$ and is processed as a signed, 2s complement number.

The NCO frequency setting is set by the 48-bit register value given and calculated as:

$$\text{NCO frequency (0 to + } F_S/2\text{): NCO} = f_{NCO} \times 2^{48} / F_S \quad (2)$$

$$\text{NCO frequency (-}F_S/2 \text{ to 0): NCO} = (f_{NCO} + F_S) \times 2^{48} / F_S \quad (3)$$

where:

- NCO = NCO register setting (decimal value)
- f_{NCO} = Desired NCO frequency (MHz)
- F_S = ADC sampling rate (MSPS)

The NCO programming is illustrated with this example:

- ADC sampling rate F_S = 500MSPS
- Desired NCO frequency = 120MHz

$$\text{NCO frequency setting} = f_{NCO} \times 2^{48} / F_S = 120\text{MHz x } 2^{48} / 500 \text{ MSPS} = 67{,}553{,}994{,}410{,}557 \quad (4)$$

Table 8-9 shows the register writes to set frequency 0 of the NCO of DDC0 to that frequency:

Table 8-9. Example register writes to change NCO frequency

ADDR	DATA	DESCRIPTION
0x200	0x3D	Set the NCO0 frequency to 120MHz (67,553,994,410,557) which is 0x3D70 A3D7 0A3D starting LSB in 0x200.
0x201	0x0A	
0x202	0xD7	
0x203	0xA3	
0x204	0x70	
0x205	0x3D	
0x165	0x00	Load and update all NCOs with the new frequencies.
0x165	0x01	
0x165	0x00	
0x160	0x00	Issue a manual SYSREF (via pin or SPI SYSREF) to update the NCO frequencies.
0x160	0x04	
0x160	0x00	

8.3.9 Digital Interface

The ADC366x supports 2 different LVDS interface depending on operating mode:

- DDR LVDS: In DDC bypass mode the data from the ADC is output using 16-bit wide DDR LVDS using both rising and falling edge of the output clock.
- Serial LVDS (SLVDS): When using decimation (real or complex) the output data is serialized and output on fewer lanes.

8.3.9.1 Parallel LVDS (DDR)

Parallel LVDS is used in decimation bypass mode. All 16 bit of channel A are transmitted on the rising edge of DCLK while the 16 bit of channel B are transmitted on the falling edge of DCLK as shown in Figure 8-56.

The output data of ChA/ChB on lanes DOUT0/1/2 can be replaced with:

- Overrange output OVR on lanes DOUT0/1/2, configured in register 0x116
- PRBS bit in output scrambling mode on lanes DOUT0/1/2, configured in register 0x116
- TIME-STAMP on lane DOUT0 only, configured in register 0x162. TIME-STAMP takes precedence over OVR and SCR when configured to DOUT0.

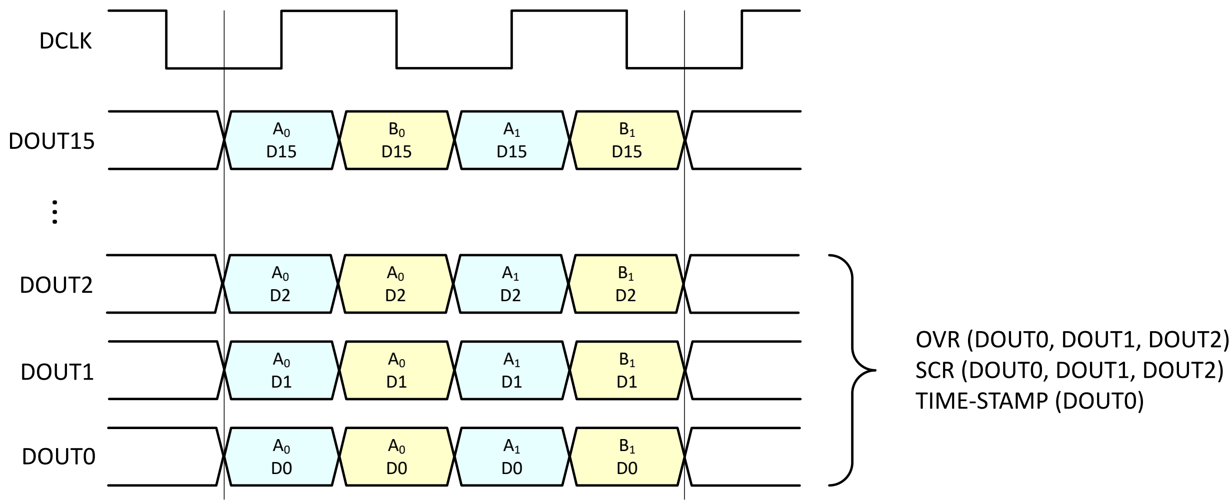


Figure 8-56. Output data format in DDR LVDS mode

8.3.9.2 Serial LVDS (SLVDS) with Decimation

When using real or complex decimation, the output data is serialized and transmitted using fewer LVDS transmitters. A frame clock (FCLK) marks the start and stop of the sample while the data bits are clocked out on the rising and falling edge of the data clock (DCLK). The frame clock is output on DOUT0 and there are a maximum number of 15 LVDS lanes available for data output. The output interface mapping always starts on lane DOUT15 unless the output mux is used.

In real decimation, only single band per ADC is supported.

The # of lanes and output data rates can be calculated with the following parameters:

- R: Output Resolution: 16-bit = 1, 32-bit = 2
- B: Total number of DDC bands
- C: Real or complex decimation: real = 1, complex = 2
- D: Decimation factor
- FS: ADC sampling clock frequency
- K = R x B x C
- L = 8 x K / D (# of LVDS output lanes)

For L < 1, the DCLK output divider needs to be enabled (0x590, D1)

Table 8-10. SLVDS clock and data rate calculations

Parameter	L ≥1	L < 1
Frame Clock (FCLK) Frequency	FS / D	
Data Bit Clock (DCLK) Frequency	FS	DOUT / 2
Data output rate DOUT per Lane (DOUT/L)	FS x 2	FS / D x 16 x K

The SLVDS frame assembly is automatically performed by the ADC and follows this scheme, starting on lane DOUT15 and with the MSB of each channel:

Table 8-11. SLVDS frame assembly

Decimation	Output Resolution	Band order
Real	16-bit	B_0, B_1
	32-bit	
Complex	16-bit	B_{0I}, B_{0Q}, B_{1I}, B_{1Q}, B_{2I}, B_{2Q}, B_{3I}, B_{3Q}
	32-bit	

Following details the frame assembly and calculations for four different examples.

Example 1: Dual band, real decimation by 8, 16-bit output resolution, FS = 500MSPS

- K = 2 (R = 1, B = 2, C = 1)
- L = 8 x K / D = 8 x 2 / 8 = 2
- FCLK = FS / D = 500MSPS / 8 = 62.5MHz
- DCLK = 500MHz
- DOUT/Lane = 1Gbps

The SLVDS frame assembly for example 1 is shown in Figure 8-57. Two lanes are used to output the data with odd bits on DCLK rising edge and even bits on DCLK falling edge.

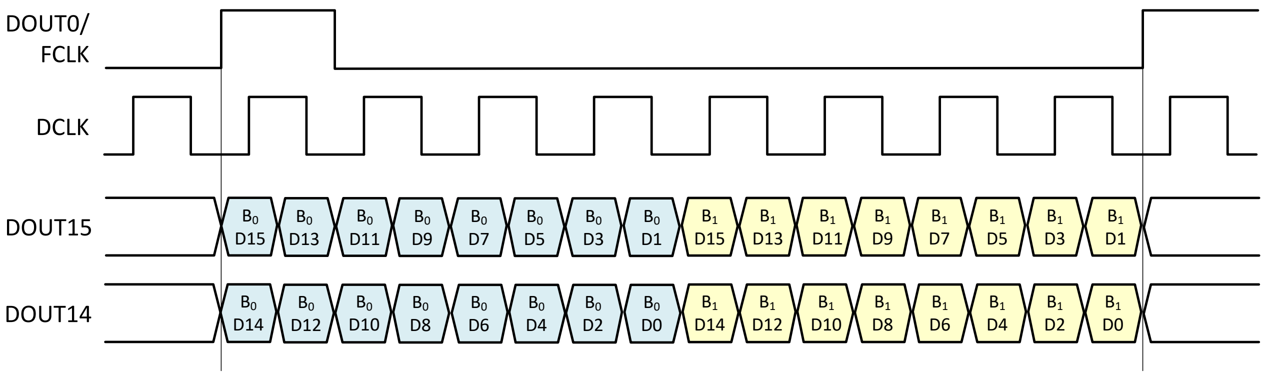


Figure 8-57. SLVDS frame assembly for example 1

Example 2: Dual band, real decimation by 128, 32-bit output resolution, FS = 500MSPS

- K = 4 (R = 2, B = 2, C = 1)
- L = 8 x K / D = 8 x 4 / 128 = 1/4 => One lane is used.
- FCLK = FS / D = 500 MSPS / 128 = 3.91MHz
- DCLK = 125MHz
- DOUT/Lane = 0.25Gbps

The SLVDS frame assembly for example 2 is shown in Figure 8-58. A single lane is used to first transmit the 32 bit of DDC band 0 (B_0) followed by 32 bit of DDC band 1.

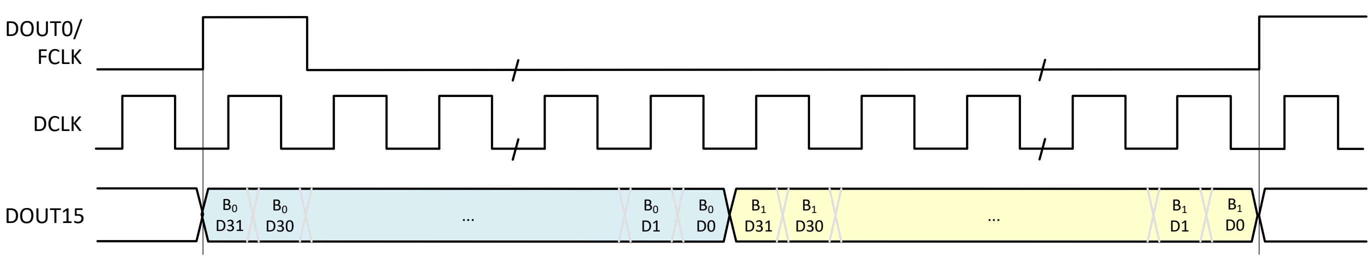


Figure 8-58. SLVDS frame assembly for example 2

Example 3: Dual band, complex decimation by 16, 16-bit output resolution, FS = 500MSPS

- K = 4 (R = 1, B = 2, C = 2)
- L = 8 x K / D = 8 x 4 / 16 = 2
- FCLK = FS / D = 500MSPS / 16 = 31.25MHz
- DCLK = 500MHz
- DOUT/Lane = 1Gbps

The SLVDS frame assembly for example 3 is shown in Figure 8-59. The frame assembly starts on DOUT15 with MSB of DDC band B_0. Each sample is spread across 2 lanes.

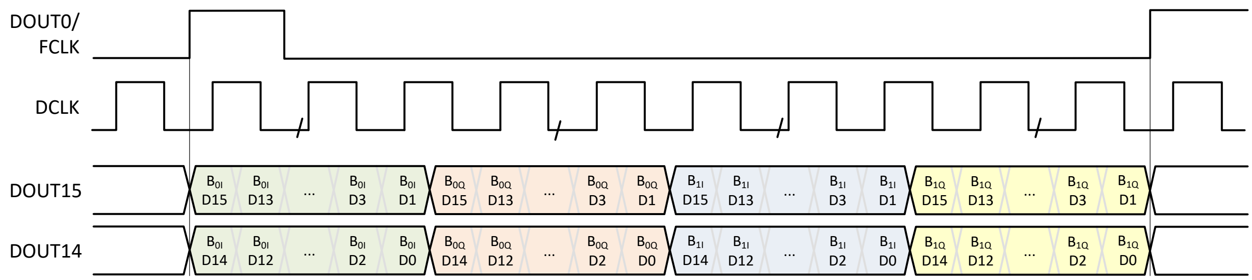


Figure 8-59. SLVDS frame assembly for example 3

Example 4: Quad band, complex decimation by 8, 16-bit output resolution, FS = 500MSPS

- K = 8 (R = 1, B = 4, C = 2)
- L = 8 x K / D = 8 x 8 / 8 = 8
- FCLK = FS / D = 500MSPS / 8 = 62.5MHz
- DCLK = 500MHz
- DOUT/Lane = 1Gbps

The SLVDS frame assembly for example 3 is shown in Figure 8-60. The frame assembly starts on DOUT15 with MSB of DDC band B_0. Each sample is spread across 8 lanes.

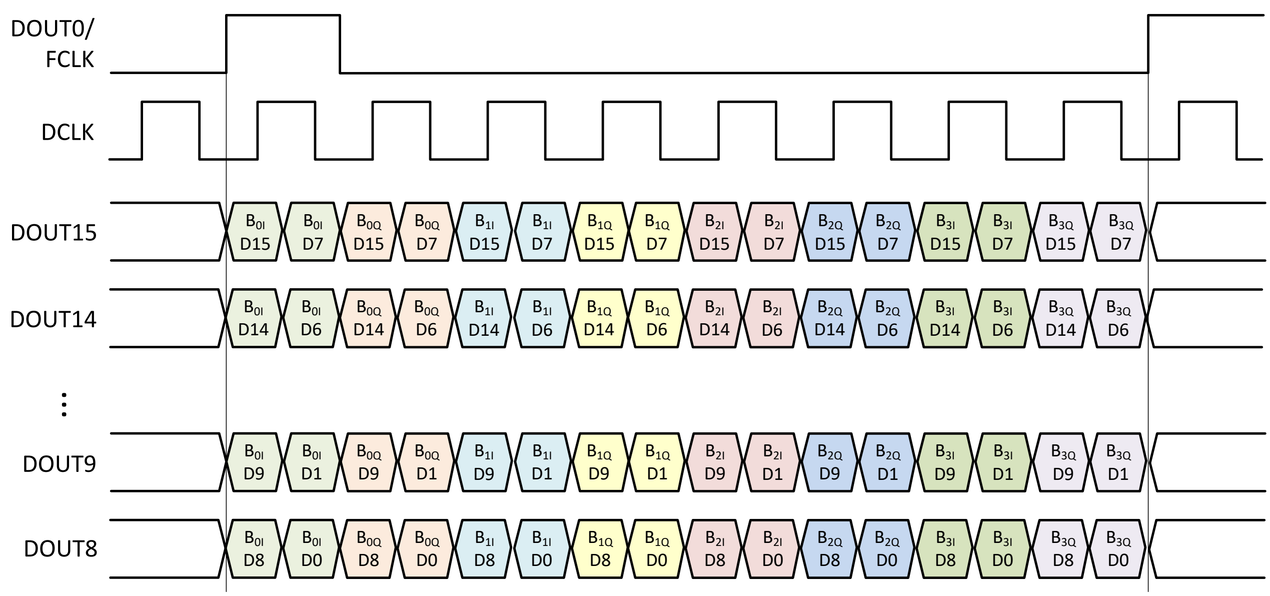


Figure 8-60. SLVDS frame assembly for example 4

Example 5: Single band, complex decimation by 256, 32-bit output resolution, FS = 500MSPS

- K = 8 (R = 2, B = 2, C = 2)
- L = 8 x K / D = 8 x 8 / 256 = 1/4 => One lane is used.
- FCLK = FS / D = 500MSPS / 256 = 1.95MHz
- DOUT/Lane = FS / D x 16 x K = 500MSPS / 256 x 16 x 8 = 250Mbps
- DCLK = 125MHz

The SLVDS frame assembly for example 4 is shown in Figure 8-61. The frame assembly uses only DOUT15 starting with the 32-bit 'I' sample of DDC band 0 and ending with the 32-bit 'Q' sample of DDC band 1.

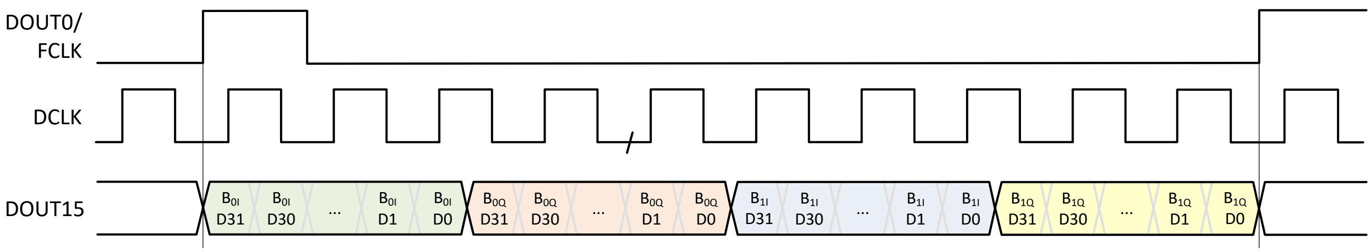


Figure 8-61. SLVDS frame assembly for example 5

8.3.9.2.1 SLVDS - Status Bit Insertion

In serial LVDS with decimation, the output data can also be substituted with the overrange or the PRBS scrambling bit (SCR). Note that the FCLK already is using output lane DOUT0.

When using 16 SLVDS lanes, the OVR or PRBS (SCR) bit can be substituted for LSB+1 (DOUT1) and/or LSB+2 (DOUT2) as shown in the quad band example in Figure 8-62.

When using less than 16 SLVDS lanes, the OVR or PRBS (SCR) bit can be substituted for LSB and/or LSB+1 as shown in the dual band example in Figure 8-63.

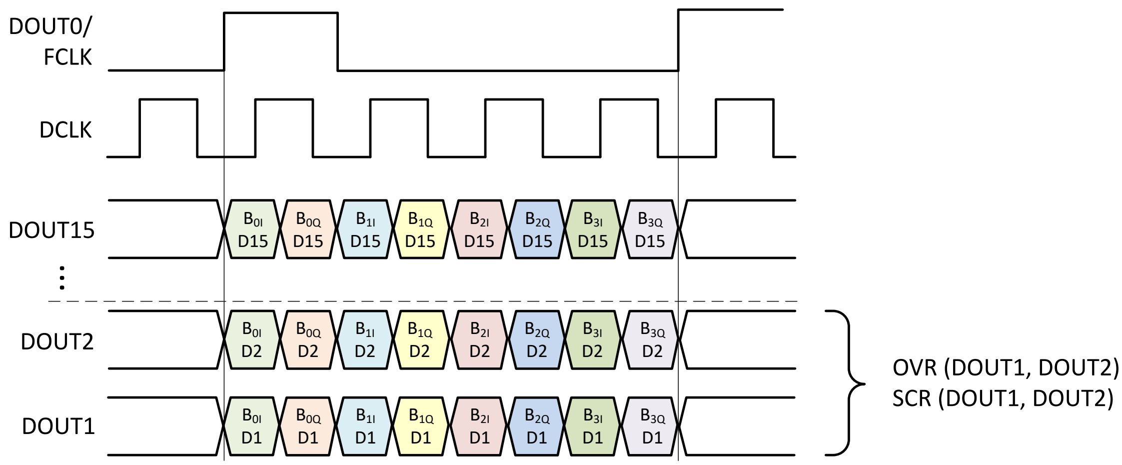


Figure 8-62. Output Data Substitution: 16 SLVDS Lanes

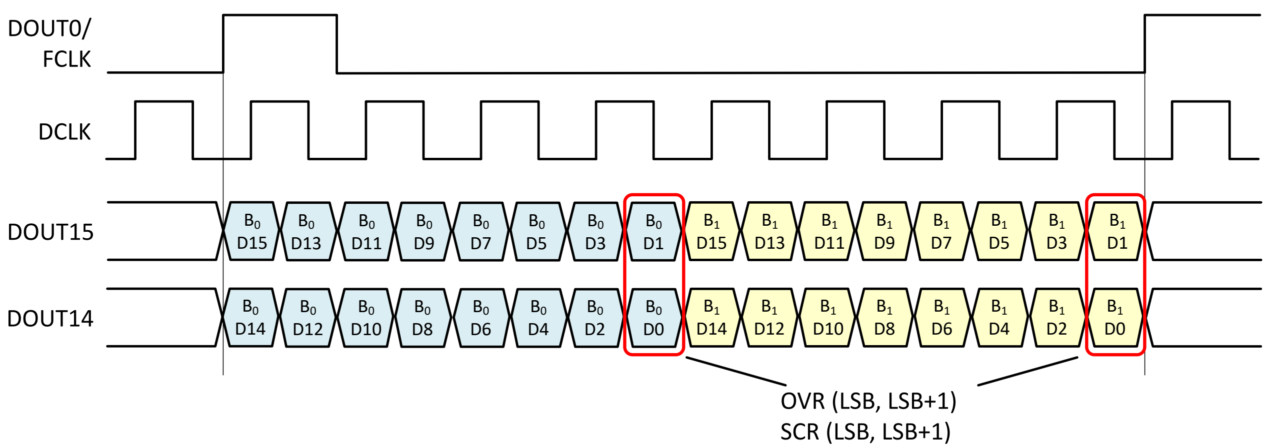


Figure 8-63. Output Data Substitution: <16 SLVDS Lanes

8.3.9.3 Output Data Format

The output data can be configured to two's complement (default) or offset binary formatting using SPI register writes (register 0x162). Table 8-12 provides an overview for minimum and maximum output codes for the two formatting options and 16 or 32-bit output resolution.

Table 8-12. Overview of minimum and maximum output codes vs resolution for different formatting

	Two's Complement (default)		Offset Binary	
RESOLUTION (BIT)	**16**	**32**	**16**	**32**
$V_{IN,MAX}$	0x7FFF	0x7FFF FFFF	0xFFFF	0xFFFF FFFF
0	0x0000	0x0000 0000	0x8000	0x8000 0000
$V_{IN,MIN}$	0x8000	0x8000 0000	0x0000	0x0000 0000

8.3.9.4 32-bit Output Resolution

The ADC366x supports both 16-bit and 32-bit output resolutions. The 32-bit output resolution is recommended for higher decimation factors (decimation by 16 real/by 32 complex and higher) to avoid SNR degradation due to quantization noise limitation as shown in Table 8-13.

The output resolution can be changed with SPI register write in register 0x162.

Table 8-13. Output SNR: Decimation vs Output Resolution

Baseline SNR (dBFS)	Real Decimation	SNR with 3dB per /2 (dBFS)	SNR with 16-bit output resolution (dBFS)	SNR with 32-bit output resolution (dBFS)
76	/16	88.0	87.6	88.0
76	/32	91.1	90.3	91.1
76	/256	100.1	96.0	100.1
76	/32768	121.1	98.0	121.1

8.3.9.5 Output Scrambler

The ADC includes an optional output scrambler. In the ADC, the internal PRBS generator generates a PRBS pattern. Each data bit gets XOR-ed with the PRBS bit stream. The scrambled output data is transmitted (via parallel or serial LVDS) along with the PRBS bit (replacing the LSB, LSB-1 or LSB-2 output data, configured in 0x146).

The receiving logic device extracts the PRBS bit stream and decodes to received data by XOR-ing each data bit with the recovered PRBS-bit.

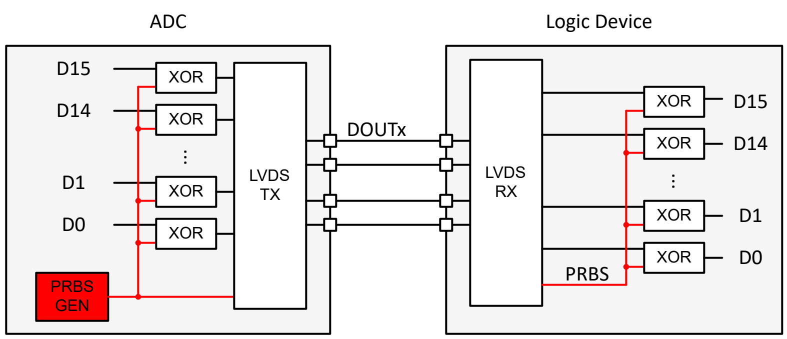


Figure 8-64. Output Scrambler

8.3.9.6 Output MUX

The LVDS output interface includes an output mux which allows rerouting of any internal digital lane to any LVDS output lane as shown in Figure 8-65. This provides lane mapping flexibility which can be used for link redundancy or link repair. The LVDS Output Mux can be enabled by setting <LVDS MUX EN> (Register 0x116, D7). The mux configuration can be controlled by writing to <DOUTxMUX> registers (0x117 to 0x11E). The mux configuration can be described mathematically as DOUTk=DIG[DOUTk_MUX], where k denotes the lane number. For example, setting a value of 2 for <DOUT2 MUX> redirects DIG2 to DOUT2. Figure 8-66 shows an example mux structure that is used for all DOUT pins.

Furthermore, when using serial LVDS (decimation only), the output mux can be used to generate duplicate, redundant outputs by connecting the same internal digital lane to multiple LVDS output lanes.

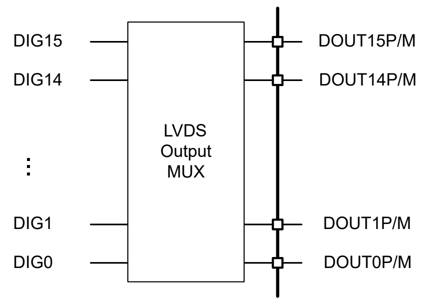


Figure 8-65. LVDS Output Mux

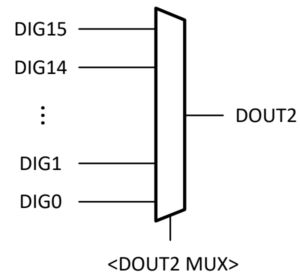


Figure 8-66. Example : Output Mux for DOUT2

8.3.9.7 Test Pattern

The device has a built-in test pattern generator for simplifying the debugging and/or calibrating of the LVDS outputs. The test pattern generator is located after the DDC as show in Figure 8-67.

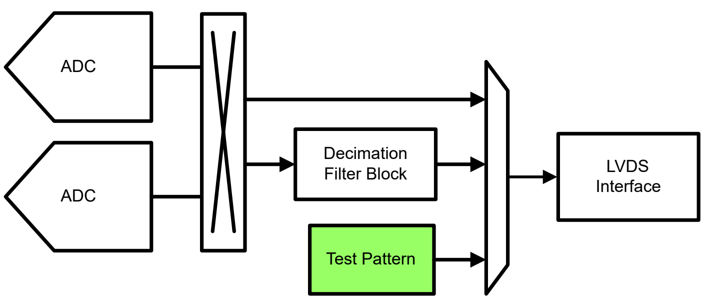


Figure 8-67. Test Pattern Generator

Enabling the test pattern generator (register <TEST PATTERN> in 0x14A) replaces all current output data samples, normal ADC or decimation data. The test pattern is the same for all channels. The test pattern block generates a 20 bit test pattern and the pattern is controlled by the value of the <TEST PATTERN> field.

In decimation, the test pattern block operates on the decimated clock by default and can be switched to run on the Fs clock by setting the <PATTERN CLK> field of register 0x14A. The test pattern feature can not be enabled in low latency operation mode.

The following register writes can be used to configure a ramp pattern with a step size of 1 with 16 bit output resolution.

Table 8-14. Example configuration for RAMP pattern with custom step size

ADDR	DATA	DESCRIPTION
0x14A	0x02	Enable ramp pattern with customer step size
0x14B	0x10	Step size is 16 LSB (at 20 bit resolution) equivalent to 1 LSB at 16 bit resolution

8.4 Device Functional Modes

Besides normal operation (DDC bypass and DDC), the device supports several additional operating modes.

8.4.1 Low Latency Mode

The device provides a low latency mode of operation by bypassing the Digital Error Correction and all other digital features such as the decimation filter, test pattern or SDR LVDS for example. This operating mode achieves a latency of 9 clock cycles and can be used in applications such as low latency control loops. However, the AC performance can degrade since the Digital Error Correction block is bypassed. The following FFT plots compare the spectrum in Low Latency Mode and Normal operating mode. The Low Latency Mode can be enabled in the <LOW LATENCY EN> register (0x165).

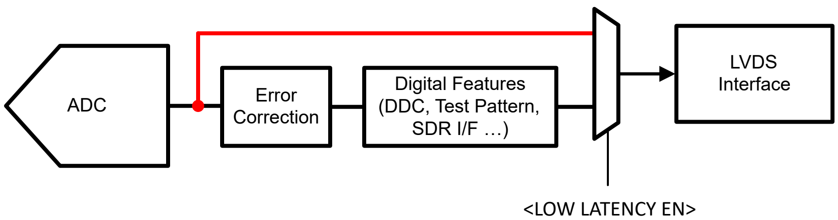
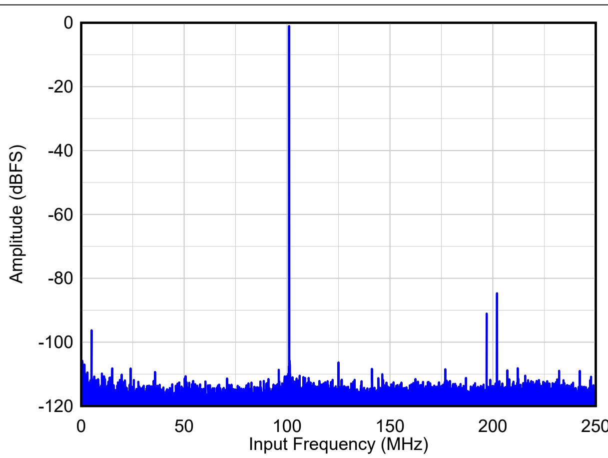
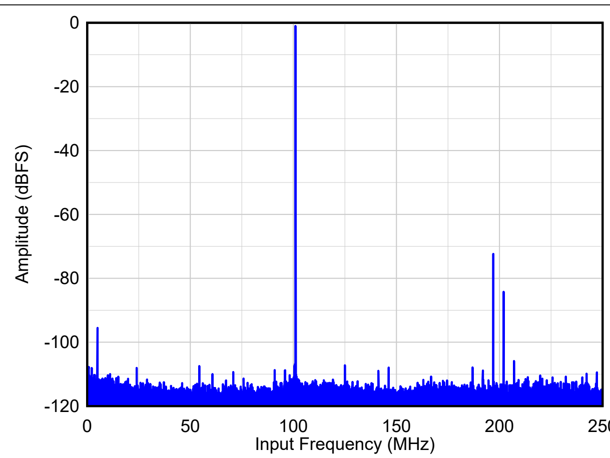


Figure 8-68. Low Latency Mode



F_{IN} = 105MHz

Figure 8-69. FFT: normal mode



F_{IN} = 105MHz,

Figure 8-70. FFT: low latency mode

8.4.2 Digital Channel Averaging

The ADC366x includes a digital channel averaging feature which enables improvement of the ADC dynamic range (see Figure 8-71). The same input signal is given to both ADC inputs externally and the output of the two ADCs is averaged internally. By averaging, uncorrelated noise (that is, ADC thermal noise) improves 3dB while correlated noise (that is, jitter in the clock path, reference noise) is unaffected. Therefore, the averaging gives close to 3dB improvement at low input frequencies but less at high input frequencies where clock jitter dominates the SNR. Using the DDC MUX select registers, the output from the digital averaging block is given out directly on the digital outputs of channel A or B or alternatively can be routed to the digital decimation filters.

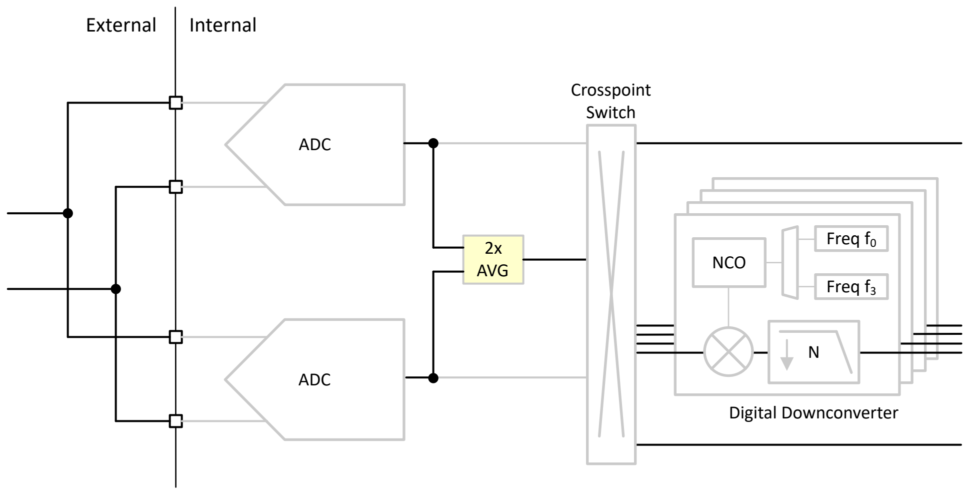


Figure 8-71. Digital Channel Averaging Diagram

The digital averaging is enabled with the following register writes:

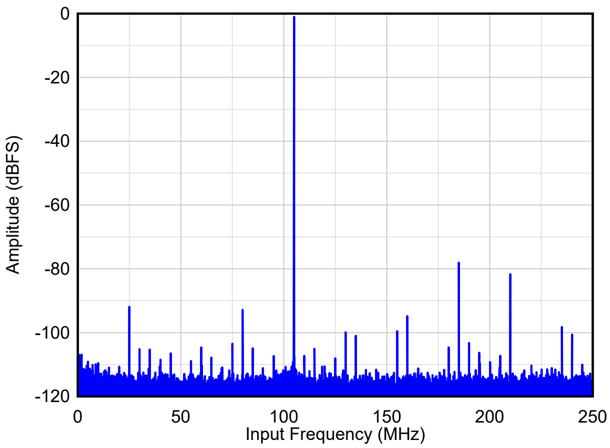
Table 8-15. Example register write for 2x AVG output on ChA

ADDR	DATA	DESCRIPTION
0x162	0x04	Enable complex decimation
0x163	0x02	Configure <DDC0 MUX> to input from '2x Average output ((ChA + ChB) / 2)'
0x169	0x20	Set <NUM of DDCS> to 1 (single DDC mode) and <COMMON DECIMATION> TO 0 (DDC bypass)

Digital averaging improves decorrelated noise contributions by 3dB per 2x AVG while correlated noise does not improve with averaging. Some of the dominant noise sources are correlated like clock jitter (external or first clock input buffer) or power supply noise. While others (such as, ADC thermal noise, clock distribution buffers) are decorrelated. Figure 8-72 to Figure 8-75 show the FFT comparison of no vs 2x internal averaging.

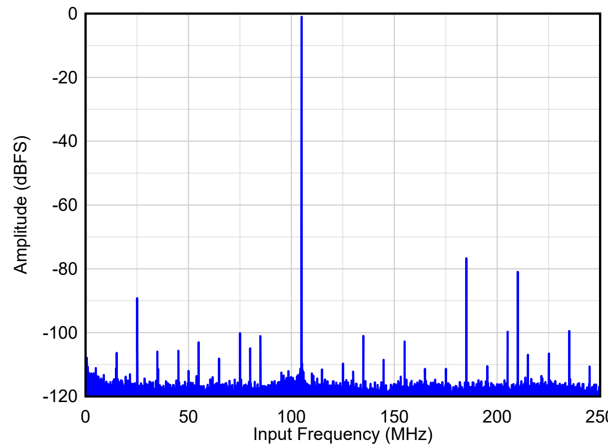
SNR: When operating close to ADC fullscale, some of the SNR limitation is due to jitter and hence the SNR improvement does not reach 3dB (2x AVG). As the input fullscale is reduced, the clock jitter contribution to SNR becomes less and the SNR improvement is approaching the 3dB per 2x AVG. The same phenomenon can be observed when using digital decimation. As the decimation factor increases, the close-in (correlated noise) becomes the more dominating noise unless the input signal amplitude is reduced.

SFDR: The amplitude of low order harmonics (HD2-HD5) and IMD3 typically is similar across ADCs; thus, the improvement with averaging is small.



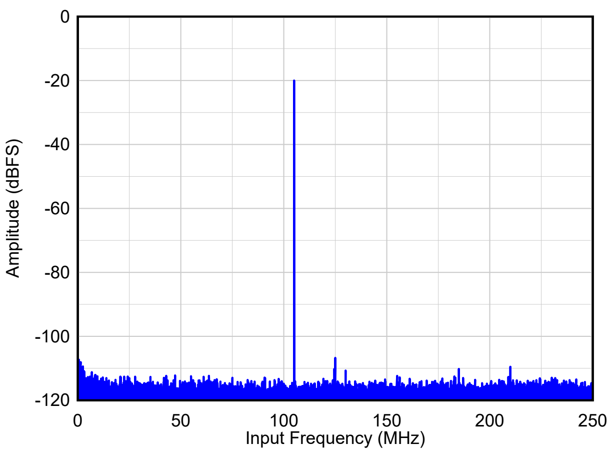
SNR = 75.3dBFS

Figure 8-72. FFT - no AVG (F_{IN} = 105MHz, A_{IN} = −1dBFS)



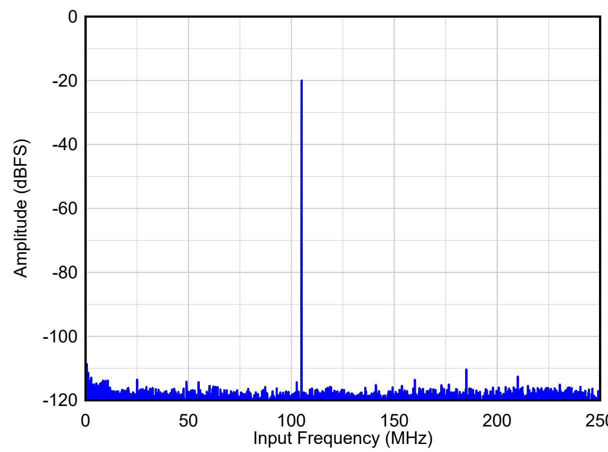
SNR = 77.4dBFS

Figure 8-73. FFT - 2x AVG (F_{IN} = 105MHz, A_{IN} = −1dBFS)



SNR = 76.4dBFS

Figure 8-74. FFT - no AVG (F_{IN} = 105MHz, A_{IN} = −20dBFS)



SNR = 78.9dBFS

Figure 8-75. FFT - 2x AVG (F_{IN} = 105MHz, A_{IN} = −20dBFS)

8.4.3 Power Down Mode

The global power down mode can be exercised using SPI writes or GPIO pins.

Table 8-16. Power Down Mode

Power Down Mode	Pd (typ, mW)	Wake up time (typ)
Global power down	30	3ms

The global power down can be assigned to either GPIO0 or GPIO1 using SPI writes in register 0x146.

Table 8-17. GPIO Pin Configuration for Power Down in Register 0x146

GPIO CONFIG	GPIO1	GPIO0
00011	GLOBAL POWER DOWN	
01010		GLOBAL POWER DOWN
01011		GLOBAL POWER DOWN

8.5 Programming

The device is primarily configured and controlled using the serial programming interface (SPI); however, the device can operate in a default configuration without requiring the SPI. Furthermore, the power down function as well as internal/external reference configuration is possible via pin control (GPIO0/1 pins).

Note

The power down command (via PIN or SPI) only goes in effect with the ADC sampling clock present.

8.5.1 GPIO Programming

The device has two GPIO pins that can be configured independently to obtain various functional modes. In the default state, the GPIO0 is configured to act as a SYSREF pin and the GPIO1 is unused. Table 8-38 gives a complete mapping of the GPIO functions. The GPIO functionality can be switched by setting the <GPIO CONFIG> in register 0x146.

The following modes are available for the GPIO pins:

- SYSREF input
- Time stamp input
- External voltage reference
- NCO switch
- Global power down
- Overrange

8.5.2 Register Write

The internal registers can be programmed following these steps:

1. Drive the SEN pin low
2. Set the R/W bit to 0 (bit A15 of the 16-bit address) and bits A[14:12] in address field to 0.
3. Initiate a serial interface cycle by specifying the address of the register (A[11:0]) whose content is written
4. Write the 8-bit data that are latched in on the SCLK rising edges

Figure 8-76 show the timing requirements for the serial register write operation.

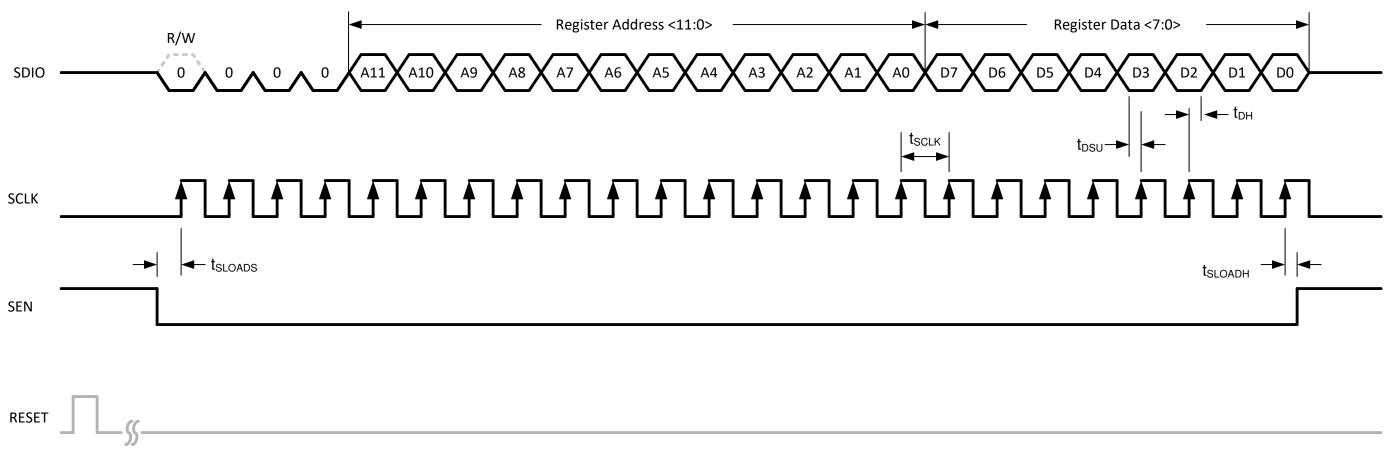


Figure 8-76. Serial Register Write Timing Diagram

8.5.3 Register Read

The device includes a mode where the contents of the internal registers can be read back using the SDIO pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers. Set A[14:12] in address field to 0.
3. Initiate a serial interface cycle specifying the address of the register (A[11:0]) whose content must be read
4. The device launches the contents (D[7:0]) of the selected register on the SDIO pin on SCLK falling edge
5. The external controller can capture the contents on the SCLK rising edge

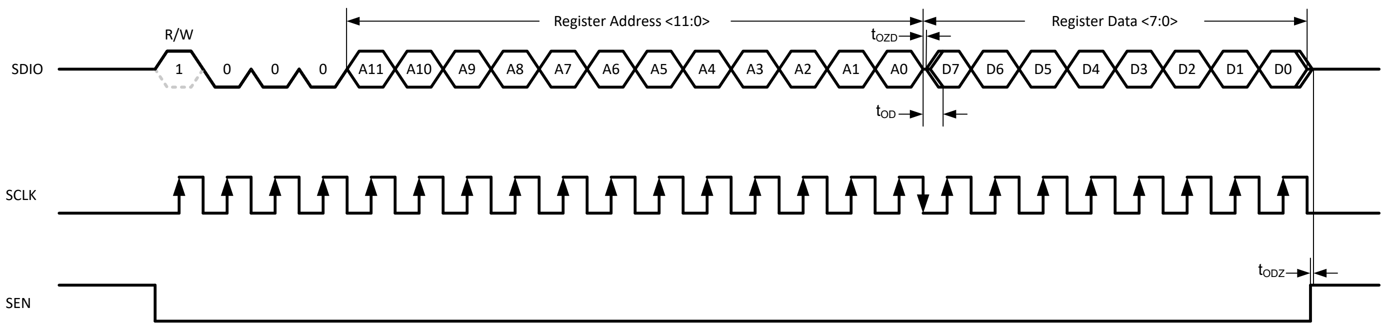


Figure 8-77. Serial Register Read Timing Diagram

8.5.4 Device Programming

All the registers of the device can be programmed using an API (library of functions, written in python). The API has functions for every field in the register map, as well as some macro functions. Macro functions use multiple low level API functions to perform a more complex operation, such as setting the decimation mode (factor, real/complex, number of bands, and so on) and setting an NCO frequency word from an input frequency.

The API user's guide is included when downloading the API from ti.com.

8.5.5 Register Map

Table 8-18. Register Map Summary

REGISTER ADDRESS	REGISTER DATA							
A[11:0]	D7	D6	D5	D4	D3	D2	D1	D0
0x25	0	0	0	CFG RDY	0	0	0	0
0x100	0	0	0	0	0	0	0	RESET
0x101	0	0	0	GBL PDN	0	0	0	0
0x102	0	SYSREF DET CLR	0	0	0	0	0	0
0x104	0	0	0	0	0	0	CHB TERM	CHA TERM
0x10A	0	0	0	0	0	OVR CLR		OVR STICKY
0x10B	OVR LENGTH							
0x110	LVDS TERM	0	LVDS HALF SWING	0	0	0	SWAP CH	0
0x111	LVDS DATA INV [7:0]							
0x112	LVDS DATA INV [15:8]							
0x113	LVDS PDN [14:8]							0
0x114	0	0	0	0	0	0	0	LVDS PDN [15]
0x115	0	0	0	0	FCLK DC	FCLK DIS	0	0
0x116	LVDS MUX EN	LVDS SWAP EDGE	0	0	0	LVDS SCR		
0x117	DOUT1 MUX				DOUT0 MUX			
0x118	DOUT3 MUX				DOUT2 MUX			
0x119	DOUT5 MUX				DOUT4 MUX			
0x11A	DOUT7 MUX				DOUT6 MUX			
0x11B	DOUT9 MUX				DOUT8 MUX			
0x11C	DOUT11 MUX				DOUT10 MUX			
0x11D	DOUT13 MUX				DOUT12 MUX			
0x11E	DOUT15 MUX				DOUT14 MUX			
0x132	HIGH FIN	0	0	0	0	0	0	0
0x140	0	SYSREF DET	SYSREF OR	SYSREF X5	SYSREF X4	SYSREF X3	SYSREF X2	SYSREF X1
0x146	0	0	0	GPIO CONFIG				
0x14A	0	0	0	PATTERN CLK	0	TEST PATTERN		
0x14B	CUSTOM PATTERN [7:0]							
0x14C	CUSTOM PATTERN [15:8]							
0x14D	0	0	0	0	CUSTOM PATTERN [19:16]			
0x15B	DIGITAL GAIN CHA							
0x15C	DIGITAL GAIN CHB							
0x160	0	0	0	0	0	0	SYSREF MODE	
0x161	LVDS SYSREF MASK		DDC SYSREF MASK		NCO SYSREF MASK		TIMER SYSREF MASK	
0x162	SYSREF TIME STAMP		0	6dB GAIN OVERRIDE		COMPLEX DDC EN	OUTPUT RES	OUTPUT FORMAT
0x163	DDC3 MUX		DDC2 MUX		DDC1 MUX		DDC0 MUX	
0x164	NCO3 UPDATE	NCO2 UPDATE	NCO1 UPDATE	NCO0 UPDATE	SEL NEG IM	0	0	NCO MODE

Table 8-18. Register Map Summary (continued)

REGISTER ADDRESS	REGISTER DATA							
A[11:0]	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x165	0	0	0	LOW LATENCY EN	0	DIS NCO AUTO UPDATE	NCO SEL EN	NCO COMMON UPDATE
0x166	DDC3 NCO SEL		DDC2 NCO SEL		DDC1 NCO SEL		DDC0 NCO SEL	
0x167	DDC1 DECIMATION				DDC0 DECIMATION			
0x168	DDC3 DECIMATION				DDC2 DECIMATION			
0x169	UNEQUAL DECIMATION	0	NUM OF DDCS		COMMON DECIMATION			
0x16B	0	0	UPDATE NYQUIST ZONE	0	0	NYQUIST_ZONE		
0x205..0x200	DDC0 NCO FREQUENCY0 [47:0]							
0x20B..0x206	DDC0 NCO FREQUENCY1 [47:0]							
0x211..0x20C	DDC0 NCO FREQUENCY2 [47:0]							
0x217..0x212	DDC0 NCO FREQUENCY3 [47:0]							
0x219/0x218	DDC0 NCO PHASE0 [15:0]							
0x21B/0x21A	DDC0 NCO PHASE1 [15:0]							
0x21D/0x21C	DDC0 NCO PHASE2 [15:0]							
0x21F/0x21E	DDC0 NCO PHASE3 [15:0]							
0x245..0x240	DDC1 NCO FREQUENCY0 [47:0]							
0x24B..0x246	DDC1 NCO FREQUENCY1 [47:0]							
0x251..0x24C	DDC1 NCO FREQUENCY2 [47:0]							
0x257..0x252	DDC1 NCO FREQUENCY3 [47:0]							
0x259/0x258	DDC1 NCO PHASE0 [15:0]							
0x25B/0x25A	DDC1 NCO PHASE1 [15:0]							
0x25D/0x25C	DDC1 NCO PHASE2 [15:0]							
0x25F/0x25E	DDC1 NCO PHASE3 [15:0]							
0x285..0x280	DDC2 NCO FREQUENCY0 [47:0]							
0x28B..0x286	DDC2 NCO FREQUENCY1 [47:0]							
0x291..0x28C	DDC2 NCO FREQUENCY2 [47:0]							
0x297..0x292	DDC2 NCO FREQUENCY3 [47:0]							
0x299/0x298	DDC2 NCO PHASE0 [15:0]							
0x29B/0x29A	DDC2 NCO PHASE1 [15:0]							
0x29D/0x29C	DDC2 NCO PHASE2 [15:0]							
0x29F/0x29E	DDC2 NCO PHASE3 [15:0]							
0x2C5...0x2C0	DDC3 NCO FREQUENCY0 [47:0]							
0x2CB..0x2C6	DDC3 NCO FREQUENCY1 [47:0]							
0x2D1..0x2CC	DDC3 NCO FREQUENCY2 [47:0]							
0x2D7..0x2D2	DDC3 NCO FREQUENCY3 [47:0]							
0x2D9/0x2D8	DDC3 NCO PHASE0 [15:0]							
0x2DB/0x2DA	DDC3 NCO PHASE1 [15:0]							
0x2DD/0x2DC	DDC3 NCO PHASE1 [15:0]							
0x2DF/0x2DE	DDC3 NCO PHASE3 [15:0]							
0x590	0	0	0	0	0	0	ENABLE DCLK DIVIDER	0

Table 8-18. Register Map Summary (continued)

REGISTER ADDRESS	REGISTER DATA							
A[11:0]	D7	D6	D5	D4	D3	D2	D1	D0
0x691	LVDS PDN [5:7]			DCLK PD	0	0	0	0
0x692	0	0	0	LVDS PDN [0:4]				

8.5.6 Detailed Register Description

Figure 8-78. Register 0x25

7	6	5	4	3	2	1	0
0	0	0	CFG RDY	0	0	0	0

Table 8-19. Register 0x25 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
0	CFG RDY	R/W	0	This bit indicates the status of the internal fuse load after HW reset. 0: Fuse load not complete 1: Fuses are loaded, applied and device ready for programming.
3-0	0	R/W	0	Must write 0

Figure 8-79. Register 0x100

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RESET

Table 8-20. Register 0x100 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0
0	RESET	R/W	0	This bit resets all internal registers to the default values and self clears to 0.

Figure 8-80. Register 0x101

7	6	5	4	3	2	1	0
0	0	0	GBL PDN	0	0	0	0

Table 8-21. Register 0x101 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	GBL PDN	R/W	0	Global power down. This bit powers down the entire device. This feature is also available using GPIO pins (0x146, D4-D0). 0: normal operation 1: Device in global power down mode
3-0	0	R/W	0	Must write 0

Figure 8-81. Register 0x102

7	6	5	4	3	2	1	0
0	SYSREF DET CLR	0	0	0	0	0	0

Table 8-22. Register 0x102 Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6	SYSREF DET CLR	R/W	0	This bit resets the SYSREF DET flag (0x140, D6) 0: normal operation 1: SYSREF DET flag gets reset.
5-0	0	R/W	0	Must write 0

Figure 8-82. Register 0x104

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CHB TERM	CHA TERM

Table 8-23. Register 0x104 Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0
1	CHB TERM	R/W	0	ChB internal termination. This bit sets the internal termination on channel B. 0: 100Ω differential termination 1: 200Ω differential termination
0	CHA TERM	R/W	0	ChA internal termination. This bit sets the internal termination on channel A. 0: 100Ω differential termination 1: 200Ω differential termination

Table 8-24. Register 0x10A

7	6	5	4	3	2	1	0
0	0	0	0	0	OVR CLR		OVR STICKY

Table 8-25. Register 0x10A Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0	Must write 0
2-1	OVR CLR	R/W	0	This is useful for clearing the sticky bit. Setting a value of 0x2 clears the sticky OVR.
0	OVR STICKY	R/W	0	This bit makes the OVR sticky. 0: OVR is non-sticky (updated based on <OVR LENGTH>) 1: OVR is sticky (use <OVR CLR> to reset)

Table 8-26. Register 0x10B

7	6	5	4	3	2	1	0
OVR LENGTH							

Table 8-27. Register 0x10B Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OVR LENGTH	R/W	0	This controls the OVR pulse expansion. This field specifies the expansion width in terms of the number of clock cycles. For example 0x0F sets the OVR length to 16 clock cycles.

Figure 8-83. Register 0x110

7	6	5	4	3	2	1	0
LVDS TERM	0	LVDS HALF SWING	0	0	0	SWAP CH	0

Table 8-28. Register 0x110 Field Descriptions

Bit	Field	Type	Reset	Description
7	LVDS TERM	R/W	0	This bit configures the LVDS termination resistance. Setting this bit enables 100Ω termination. The default termination resistance is 50Ω
6	0	R/W	0	Must write 0
5	LVDS HALF SWING	R/W	0	This bit reduces the LVDS output swing by 50% to save power consumption. 0: Normal output swing 1: Reduced output swing
4-2	0	R/W	0	Must write 0
1	SWAP CH	R/W	1	This bit internally swaps channel A and channel B. 0: Channel A and channel B are swapped 1: Normal operation
0	0	R/W	0	Must write 0

Figure 8-84. Register 0x111/0x112

7	6	5	4	3	2	1	0
LVDS DATA INV [7:0]							
LVDS DATA INV [15:8]							

Table 8-29. Register 0x111/0x112 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LVDS DATA INV [15:0]	R/W	0	These bits allow to invert polarity of individual LVDS output lanes as shown in Table 8-30. 0: Polarity as shown in pin diagram. 1: Polarity inverted

Table 8-30. LVDS data inversion register lane assignment

REG ADDR	0x112								0x111							
REG BIT	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
LVDS OUTPUT LANE	8	9	10	11	12	13	14	15	7	6	5	4	3	2	1	0

Figure 8-85. Register 0x113/0x114

7	6	5	4	3	2	1	0
LVDS PDN [14:8]							0
0	0	0	0	0	0	0	LVDS PDN [15]

Table 8-31. Register 0x113/0x114 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LVDS PDN [15:8]	R/W	0	These register bits power down the individual LVDS output lanes with LVDS pins into high impedance state (e.g. 0x113, D7 powers down output lane 14). The remaining LVDS lane (0-7) power down registers are in registers 0x691/0x692. 0: Normal operation 1: LVDS output lane powered down
7-0	0	R/W	0	Must write 0

Figure 8-86. Register 0x115

7	6	5	4	3	2	1	0
0	0	0	0	FCLK DC	FCLK DIS	0	0

Table 8-32. Register 0x115 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0	Must write 0
3	FCLK DC	R/W	0	This bit allows adjusting the FCLK duty cycle. 0: FCLK stays high for one DCLK cycle at the beginning of the output sample 1: FCLK stays high for 50% of the output sample
2	FCLK DIS	R/W	0	This bit disables the output FCLK. FCLK is transmitted on lane DOUT0. In decimation modes where all 16 lanes are used, FCLK replaces the LSB. 0: FCLK replaces the LSB data and is transmitted on DOUT0 1: FCLK is disabled and the LSB data is transmitted on DOUT0.
1	0	R/W	0	Must write 0
0	0	R/W	0	Must write 0

Figure 8-87. Register 0x116

7	6	5	4	3	2	1	0
LVDS MUX EN	LVDS SWAP EDGE	0	0	0	LVDS SCR		

Table 8-33. Register 0x116 Field Descriptions

Bit	Field	Type	Reset	Description
7	LVDS MUX EN	R/W	0	This bit enables use of the LVDS output mux in registers 0x117..0x11E. 0: LVDS output mux disabled 1: LVDS output mux enabled
6	LVDS SWAP EDGE	R/W	0	This bit swaps the output data bits transmitted on rising and falling edge of DCLK. 0: Normal operation 1: Output bits on rising and falling edge are swapped.
5-3	0	R/W	0	Must write 0
2-0	LVDS SCR	R/W	0	This field controls the scrambling and lsb insertion config on the output data 000: Default operation 001: Data is XOR'ed with a PRBS bit. This PRBS is inserted on the LSB position. The PRBS is generated using a large LFSR and can be treated as random for all practical scenarios 010: OVR is inserted on the LSB position 011: OVR is inserted on the LSB+1 position 100: Data is XOR'ed with a PRBS bit, and the PRBS is inserted on LSB+1 position 101: OVR is inserted on LSB+1 position, PRBS is inset on LSB position. Data is XOR'ed with PRBS 110: OVR is inserted on LSB+2 position, PRBS is inset on LSB+1 position. Data is XOR'ed with PRBS 111: Unused

Figure 8-88. Register 0x117...0x11E

7	6	5	4	3	2	1	0
DOUT1/3/5/7/9/11/13/15 MUX				DOUT0/2/4/6/8/10/12/14 MUX			

Table 8-34. Register 0x117...0x11E Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DOUT1/3/5/7/9/11/13/15 MUX	R/W	0000	These bits configure the data bus assignment for the individual output lanes. <LVDS MUX EN> in 0x116, D7 must be enabled. 0000: LVDS lane DOUTx carries data of internal digital bus lane DIG0 0001: LVDS lane DOUTx carries data of internal digital bus lane DIG1 ... 1111: LVDS lane DOUTx carries data of internal digital bus lane DIG15
3-0	DOUT0/2/4/6/8/10/12/14 MUX	R/W	0000	

Figure 8-89. Register 0x132

7	6	5	4	3	2	1	0
HIGH FIN	0	0	0	0	0	0	0

Table 8-35. Register 0x132 Field Descriptions

Bit	Field	Type	Reset	Description
7	HIGH FIN	R/W	0	This bit must be set for best AC performance for input frequencies greater than 500MHz 0: Input frequencies < 500MHz 1: Input frequencies > 500MHz
6-0	0	R/W	0	Must write 0

Figure 8-90. Register 0x140

7	6	5	4	3	2	1	0
0	SYSREF DET	SYSREF OR	SYSREF X5	SYSREF X4	SYSREF X3	SYSREF X2	SYSREF X1

Table 8-36. Register 0x140 Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6	SYSREF DET	R/W	0	This register indicates if a SYSREF signal is detected. Upon detection, this bit stays high until the bit is reset (0x102, D6) or a device reset is issued. 0: no SYSREF signal detected 1: SYSREF signal detected
5	SYSREF OR	R/W	0	This bit is the output of the five SYSREF XOR flags logically OR'ed together. 0: no SYSREF flag raised 1: one of the five SYSREF XOR flags is raised.
4-0	SYSREF X5..X1	R/W	0	These bits are the XOR flags from the SYSREF window monitoring circuitry. The sampling clock falling edge is used to capture the SYSREF signal. If a SYSREF signal transition happens within -60/+140 ps of the SYSREF capture, the appropriate XOR flag gets raised. These bits are updated on every SYSREF rising edge. X1: SYSREF leading sample clock by 20 to 60ps X2: SYSREF leading sample clock by 20ps to 0ps or SYSREF lagging sample clock by 0 to 20ps X3: SYSREF lagging sample clock by up to 20 to 60ps X4: SYSREF lagging sample clock by 60 to 100ps X5: SYSREF lagging sample clock by 100 to 140ps 0: No SYSREF transition detected 1: SYSREF transition detected within given window

Figure 8-91. Register 0x146

7	6	5	4	3	2	1	0
0	0	0	GPIO CONFIG				

Table 8-37. Register 0x146 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4-0	GPIO CONFIG	R/W	0	These register bits configure the functionality of the two GPIO pins as shown in Table 8-38.

Table 8-38. GPIO pin configuration

GPIO CONFIG	GPIO1	GPIO0
00000	NOT USED	SYSREF
00011	GLOBAL POWER DOWN	SYSREF
00100	EXTERNAL REFERENCE	SYSREF
00101	NCO SWITCH1	NCO SWITCH0
01000	NOT USED	SYSREF
01001	OVR CHB/CHA	SYSREF
01010	NOT USED	GLOBAL POWER DOWN
01011	OVR CHB/CHA	GLOBAL POWER DOWN
10010	OVR CHB	OVR CHA
all others	NOT USED	

Figure 8-92. Register 0x14A

7	6	5	4	3	2	1	0
0	0	0	PATTERN CLK	0	TEST PATTERN		

Table 8-39. Register 0x14A Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W		Must write 0
4	PATTERN CLK	R/W	0	This controls the clock of the pattern signal generator. Setting this bit switches the pattern generator clock to decimation clock. 0: Pattern clock uses the ADC sampling clock 1: Pattern clock uses the DDC clock.
3	0	R/W	0	Must write 0
2-0	TEST PATTERN	R/W	0	This field controls the type of pattern injected. Default value is 0 and indicates that the pattern generator is off. The generated pattern is 20 bit wide. In 16 bit resolution mode, MSB 16 bits of the pattern mode are sent out. In 32 bit resolution mode, 12 zero bits are padded to the generated pattern and sent out. 000: Test pattern is disabled 001: Ramp pattern with a step of 1 (at 20 bit level, which is equivalent to 1/16 at 16 bit level) 010: Ramp pattern with a step value set by CUSTOM PATTERN. For example, to configure a ramp pattern with unit step in 16 bit mode, the CUSTOM PATTERN must be set to 0x010 011: Unused 100: Static pattern set by CUSTOM PATTERN 101: Pattern toggles between CUSTOM PATTERN and invert of CUSTOM PATTERN 110: Pattern toggles between CUSTOM PATTERN and 0 111: Unused

Figure 8-93. Register 0x14B/0x14C/0x14D

7	6	5	4	3	2	1	0
CUSTOM PATTERN [7:0]							
CUSTOM PATTERN [15:8]							
0	0	0	0	CUSTOM PATTERN [19:16]			

Table 8-40. Register 0x14B/0x14C/0x14D Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOM PATTERN [19:0]	R/W	0	This filed controls the pattern generator. This controls different functions depending on the TEST PATTERN setting

Figure 8-94. Register 0x15B

7	6	5	4	3	2	1	0
DIGITAL GAIN CHA [7:0]							

Table 8-41. Register 0x15B Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIGITAL GAIN CHA [7:0]	R/W	0	This register controls digital gain for channel A and is interpreted as a 2's complement number. Maximum gain is 6dB (20 x log (1+(DIGITAL GAIN CHA / 128))).

Figure 8-95. Register 0x15C

7	6	5	4	3	2	1	0
DIGITAL GAIN CHB [7:0]							

Table 8-42. Register 0x15C Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIGITAL GAIN CHB [7:0]	R/W	0	This register controls digital gain for channel B and is interpreted as a 2's complement number. Maximum gain is 6dB (20 x log (1+(DIGITAL GAIN CHB / 128))).

Figure 8-96. Register 0x160

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SYSREF MODE	

Table 8-43. Register 0x160 Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0
1-0	SYSREF MODE	R/W	0	This controls the global SYSREF mask including the test pattern. 00: Pass all SYSREF pulses 01: Pass the first SYSREF pulse and gates subsequent pulses 10: Gate all SYSREF pulses 11: Issue new SYSREF pulse. The pulse is issued when the state transitions to 11

Figure 8-97. Register 0x161

7	6	5	4	3	2	1	0
LVDS SYSREF MASK		DDC SYSREF MASK		NCO SYSREF MASK		TIMER SYSREF MASK	

Table 8-44. Register 0x161 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LVDS SYSREF MASK	R/W	0	This controls the SYSREF pulse going to the SLVDS block (decimation only). Default setting is 0 and passes all SYSREF pulses. 00: Pass all SYSREF pulses 01: Pass the first SYSREF pulse and gates subsequent pulses 10: Gate all SYSREF pulses 11: Issue new SYSREF pulse. The pulse is issued when the state transitions to 11
5-4	DDC SYSREF MASK	R/W	0	This controls the SYSREF pulse of DDC block. The value - function map is same as LVDS SYSREF MASK
3-2	NCO SYSREF MASK	R/W	0	This controls the SYSREF pulse of NCO block. The value - function map is same as LVDS SYSREF MASK
1-0	TIMER SYSREF MASK	R/W	0	This controls the SYSREF pulse of TIMER block of the NCO. The value - function map is same as LVDS SYSREF MASK

Figure 8-98. Register 0x162

7	6	5	4	3	2	1	0
SYSREF TIME STAMP		0	6dB GAIN OVERRIDE		COMPLEX DDC EN	OUTPUT RES	OUTPUT FORMAT

Table 8-45. Register 0x162 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SYSREF TIME STAMP	R/W	0	Setting this field to 0x3 allows the SYSREF input to replace the LSB. OVR_ON_LSB setting takes precedence.
5	0	R/W	0	Must write 0
4-3	6dB GAIN OVERRIDE	R/W	0	This field controls 6dB gain setting of the DDC. The 6dB gain is applied in COMPLEX DDC mode by default. Setting this to 0x3 forces 6dB gain on the DDC output, irrespective of the DDC mode. Setting this to 0x2 forces unity gain irrespective of the DDC mode.
2	COMPLEX DDC EN	R/W	0	This bit enables complex decimation for all DDCs. The decimation factor is set in 0x167..0x169 0: Real decimation 1: Complex decimation
1	OUTPUT RES	R/W	0	This bit increases the output resolution from 16-bit to 32-bit 0: 16-bit output resolution 1: 32-bit output resolution
0	OUTPUT FORMAT	R/W	0	This bit selects the output format 0: Output format is 2s complement 1: Output format is offset binary

Figure 8-99. Register 0x163

7	6	5	4	3	2	1	0
DDC3 MUX		DDC2 MUX		DDC1 MUX		DDC0 MUX	

Table 8-46. Register 0x163 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DDC3 MUX	R/W	0	These register bits set the input data source to the individual decimation filters. 00: Channel B 01: Channel A 10: 2x Average output ((ChA + ChB) / 2) 11: 2x Average output ((ChA - ChB) / 2)
5-4	DDC2 MUX	R/W	0	These register bits set the input data source to the individual decimation filters. 00: Channel A 01: Channel B 10: 2x Average output ((ChA + ChB) / 2) 11: 2x Average output ((ChA - ChB) / 2)
3-2	DDC1 MUX	R/W	0	These register bits set the input data source to the individual decimation filters. 00: Channel B 01: Channel A 10: 2x Average output ((ChA + ChB) / 2) 11: 2x Average output ((ChA - ChB) / 2)
1-0	DDC0 MUX	R/W	0	These register bits set the input data source to the individual decimation filters. 00: Channel A 01: Channel B 10: 2x Average output ((ChA + ChB) / 2) 11: 2x Average output ((ChA - ChB) / 2)

Figure 8-100. Register 0x164

7	6	5	4	3	2	1	0
NCO3 UPDATE	NCO2 UPDATE	NCO1 UPDATE	NCO0 UPDATE	SEL NEG IM	0	0	NCO MODE

Table 8-47. Register 0x164 Field Descriptions

Bit	Field	Type	Reset	Description
7	NCO3 UPDATE	R/W	0	A '0' to '1' transition in these register bits updates the four NCO frequencies of the respective NCOs.
6	NCO2 UPDATE	R/W	0	
5	NCO1 UPDATE	R/W	0	
4	NCO0 UPDATE	R/W	0	
3	SEL NEG IM	R/W	0	This field controls the selection of negative frequency image, and is applicable only in COMPLEX DDC model.
2-1	0	R/W	0	Must write 0
0	NCO MODE	R/W	0	This register configures the NCOs operating mode. 0: Phase continuous 1: Infinite phase coherent

Figure 8-101. Register 0x165

7	6	5	4	3	2	1	0
0	0	0	LOW LATENCY EN	0	DIS NCO AUTO UPDATE	NCO SEL EN	NCO COMMON UPDATE

Table 8-48. Register 0x165 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	LOW LATENCY EN	R/W	0	This bit enables low latency mode by bypassing all digital features. 0: Normal operation 1: Enables low latency mode
3	0	R/W	0	Must write 0
2	DIS NCO AUTO UPDATE	R/W	0	This register bit disables the automatic update when switching the NCOs using GPIO pins 0: Normal operation 1: Automatic switch disabled
1	NCO SEL EN	R/W	0	This bit enables NCO frequency selection via SPI register 0x166 instead of GPIO pins. 0: NCO frequency selection via GPIO pins 1: NCO frequency selection via register 0x166.
0	NCO COMMON UPDATE	R/W	0	A '0' to '1' transition in this register bit updates the four NCO frequencies of all NCOs.

Figure 8-102. Register 0x166

7	6	5	4	3	2	1	0
DDC3 NCO SEL		DDC2 NCO SEL		DDC1 NCO SEL		DDC0 NCO SEL	

Table 8-49. Register 0x166 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DDC3 NCO SEL	R/W	0	These bits select which of the 4 frequencies are active in the respective DDCs/NCOs. The <NCO SEL EN> bit in register 0x165 (D1) has to be set also.
5-4	DDC2 NCO SEL	R/W	0	
3-2	DDC1 NCO SEL	R/W	0	
1-0	DDC0 NCO SEL	R/W	0	

Figure 8-103. Register 0x167/168

7	6	5	4	3	2	1	0
DDC1/3 DECIMATION				DDC0/2 DECIMATION			

Table 8-50. Register 0x167/0x168 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DDC1/3 DECIMATION	R/W	0	These bits set the decimation filter factors for the respective DDCs when using unequal decimation factors. Register <UNEQUAL DECIMATION> in register 0x169 (D7) has to be set also. 0000: DDC bypass 0001: Decimation by 2 0010: Decimation by 4 ... 1110: Decimation by 16384 1111: Decimation by 32768
3-0	DDC0/2 DECIMATION	R/W	0	

Figure 8-104. Register 0x169

7	6	5	4	3	2	1	0
UNEQUAL DECIMATION	0	NUM OF DDCS		COMMON DECIMATION			

Table 8-51. Register 0x169 Field Descriptions

Bit	Field	Type	Reset	Description
7	UNEQUAL DECIMATION	R/W	0	This bit enables configuration of DDC0..3 to have unequal decimation factors. 0: Common decimation factor for all DDCs 1: Unequal decimation factors
6	0	R/W	0	Must write 0
5-4	NUM OF DDCS	R/W	00	This register configures the # of active DDCs 00: Dual DDC Mode 01: Quad DDC Mode 10: Single DDC only (useful only when using internal 2x averaging) 11: not used
3-0	COMMON DECIMATION	R/W	0000	This register bit set the decimation filter factors for all active DDCs. 0000: DDC bypass 0001: Decimation by 2 0010: Decimation by 4 ... 1110: Decimation by 16384 1111: Decimation by 32768

Figure 8-105. Register 0x16B

7	6	5	4	3	2	1	0
0	0	0	UPDATE NYQUIST ZONE	0	NYQUIST ZONE		

Table 8-52. Register 0x16B Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	UPDATE NYQUIST ZONE	R/W	0	This field must be pulsed after the Nyquist zone if programmed. A 0 to 1 transition on this bit copies the NYQUIST ZONE field to an internal register.
3	0	R/W	0	Must write 0
2-0	NYQUIST ZONE	R/W	000	This field controls the nyquist zone of operation. The internal calibration of the device depends on the NYQUIST ZONE of the signal being sampled. This field must be programmed based on the operating Nyquist zone 000: First Nyquist zone (from 0 to Fs/2) 001: Second Nyquist (from Fs/2 to Fs) 010: Third Nyquist (from Fs to 3Fs/2) 011:Fourth Nyquist (from 3Fs/2 to 2Fs) 100: Fifth Nyquist (from 2Fs to 5Fs/2) 101: Sixth Nyquist (from 5Fs/2 to 3Fs) 110,111: not used

Figure 8-106. Register 0x200..0x2DF

7	6	5	4	3	2	1	0
DDCx NCO FREQUENCYy [48:0]							
DDCx NCO PHASEy [15:0]							

Table 8-53. Register 0x200..0x2DF Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDCx NCO FREQUENCYy [48:0]	R/W	0	These register bits configure the 48-bit frequency words for the four DDCs/NCOs. The format is little endian. The NCO frequency calculation is shown in Section 8.3.8.4.
7-0	DDCx NCO PHASEy [15:0]	R/W	0	These register bits configure the starting phase of the four frequency words for the four DDCs/NCOs. The format is little endian. The phase value is: 90° / <16-bit register>

Figure 8-107. Register 0x590

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ENABLE DCLK DIVIDER	0

Table 8-54. Register 0x590 Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0
1	ENABLE DCLK DIVIDER	R/W	0	Setting this bit enables the DCLK divider. This is required for high decimation factors when the data bit clock (DCLK) of the LVDS interface is slower than the ADC sampling clock.

Figure 8-108. Register 0x691/0x692

7	6	5	4	3	2	1	0
LVDS PDN [5:7]			DCLK PDN	0	0	0	0
0	0	0	LVDS PDN [0:4]				

Table 8-55. Register 0x691/0x692 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LVDS PDN [0:7]	R/W	0	These register bits power down the individual LVDS output lanes with LVDS pins in high impedance state as shown in Table 8-56. The remaining LVDS bus power down registers are in registers 0x113/0x114. 0: Normal operation 1: LVDS output lane powered down
4	DCLK PDN	R/W	0	This bit powers down the LVDS output clock. 0: Normal operation 1: DCLK powered down

Table 8-56. LVDS power down register lane assignment

REG ADDR	0x113							0x114	0x691			0x692				
REG BIT	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
LVDS OUTPUT LANE	14	13	12	11	10	9	8	15	5	6	7	0	1	2	3	4

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The ADC366x can be used in a wide range of applications including RADAR, frequency domain digitizer, spectrum analyzer, test and communications equipment and software-defined radios (SDR). The *Typical Applications* section describes one configuration that meets the needs of a number of these applications.

9.2 Typical Application

9.2.1 Wideband Spectrum Analyzer

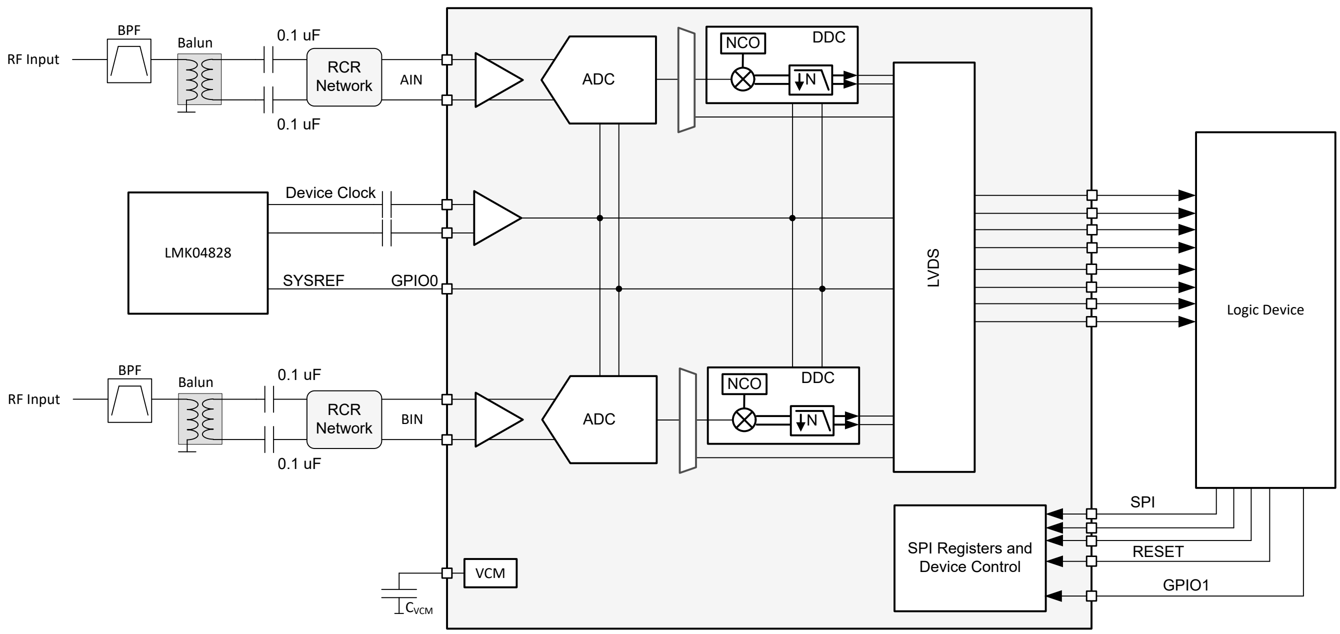


Figure 9-1. Typical Configuration for Wideband Spectrum Analyzer

9.2.2 Design Requirements

9.2.2.1 Input Signal Path

Appropriate band limiting filters must be used to reject unwanted frequencies in the receive signal path.

A 1:2 (for 100Ω effective termination impedance) or a 1:1 (for 50Ω effective termination impedance) balun transformer is needed to convert the single ended RF input to differential for input to the ADC. The balun outputs must be AC coupled with 100pF capacitors. A back-to-back balun configuration often times gives better SFDR performance. Table 9-1 lists a number of recommended baluns for different impedance ratios and frequency ranges.

The S-parameters of the ADC input can be used to design the front end matching network.

Table 9-1. Recommended Baluns

PART NUMBER	MANURACTURER[(1)]	IMPEDANCE RATIO	AMPLITUDE BALANCE (dB)	PHASE BALANCE (°)	FREQUENCY RANGE
BAL-0009SMG	Marki Microwave	1:2	0.6	5	0.5MHz to 9GHz
TCM2-43X+	Minicircuits	1:2	0.5	7	10MHz to 4GHz
TCM2-33WX+	Minicircuits	1:2	0.7	4	10MHz to 3GHz
TC1-1-13M+	Minicircuits	1:1	0.5	2-3	10MHz to 3GHz

(1) See the Section 10.1.1.

9.2.2.2 Clocking

The device clock inputs must be AC-coupled to the device to provide the rated performance. The clock source must have low jitter (integrated phase noise) for the ADC to meet the stated SNR performance, especially when operating at higher input frequencies. The clock signal can be filtered with a band pass filter to remove some of the broad band clock noise. In multi-channel systems the SYSREF signal can be generated using a LMK04828 or LMK04832 device. The LMK device can also be used as a system clock synthesizer.

9.2.3 Detailed Design Procedure

9.2.3.1 Sampling Clock

To maximize the SNR performance of the ADC a low jitter (< 75fs) sampling clock is required. Figure 9-2 shows the estimated SNR performance vs input frequency vs external clock jitter. The internal ADC aperture jitter also has some dependence to the clock amplitude (gets more sensitive with higher input frequency) as shown in Figure 9-3.

When using averaging and/or decimation, the SNR for a single ADC core must be estimated first before adding the SNR improvement from internal averaging and/or decimation.

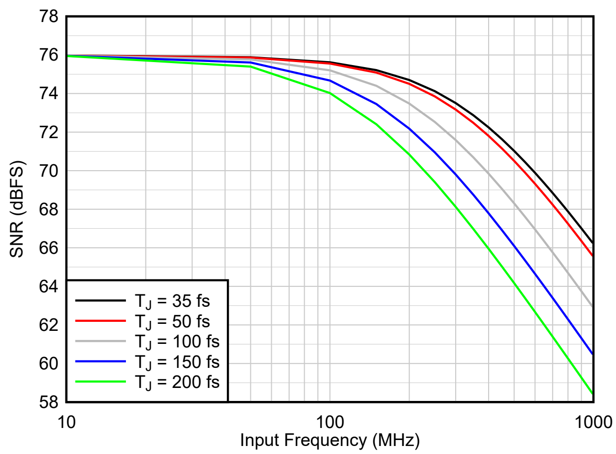


Figure 9-2. SNR vs T_{Jitter} vs F_{IN}

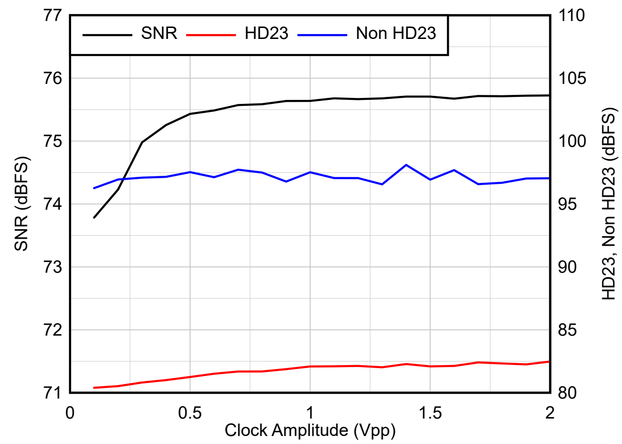


Figure 9-3. SNR vs Clock Amplitude (F_S = 500MSPS, F_{IN} = 100MHz, A_{IN} = −1dBFS)

9.2.4 Application Performance Plots

The following application curves demonstrate performance and results only of the ADC using a balun front end. The input frequency is 370MHz (F_S = 500MSPS) and input amplitudes of −1 and −20dBFS are shown. Operating modes are DDC bypass and complex decimation by 8 (NCO = 360MHz).

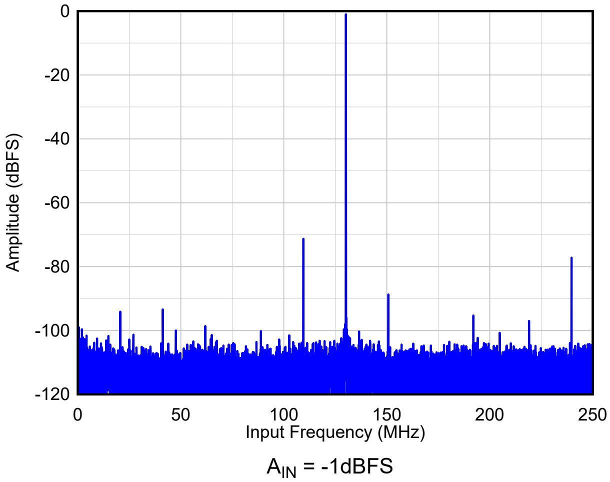


Figure 9-4. FFT1: DDC bypass

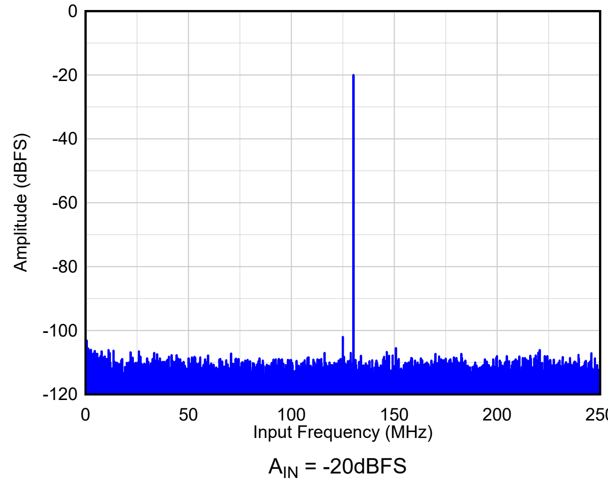


Figure 9-5. FFT2: DDC bypass

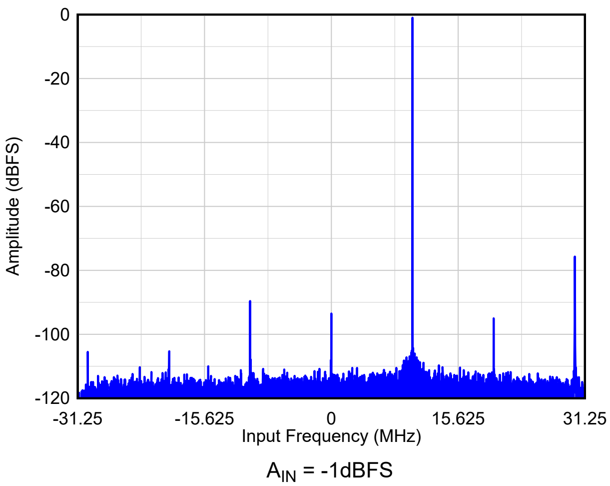


Figure 9-6. FFT3: Decimation by 8

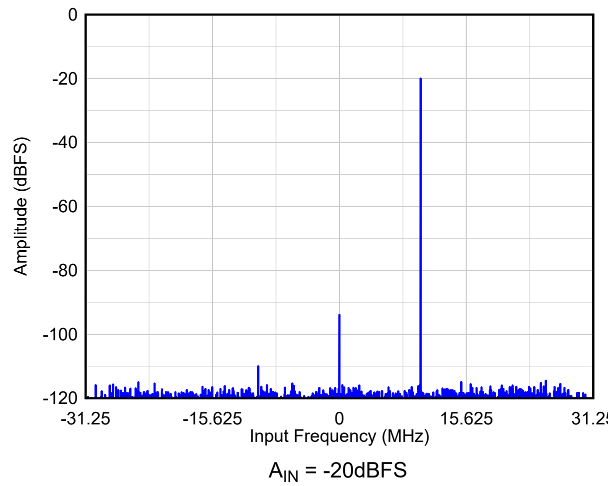


Figure 9-7. FFT4: Decimation by 8

9.2.5 Initialization Set Up

After power-up, the internal registers must be initialized to the default values through a hardware reset by applying a high pulse on the RESET pin, as shown in Figure 9-8.

1. Apply 1.2V DVDD12 digital power supply
2. Apply 1.2V AVDD12 analog power supply
3. Apply 1.8V power supplies (AVDD18, DVDD18), in no specific order
4. Apply external voltage reference and/or GPIO pin assignments (optional)
5. Apply external sampling clock
6. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses.
7. Read back 'CFG RDY register' (0x25, D4) to check if internal load is complete (< 10k clock cycles).
8. If needed, begin programming the internal registers using the SPI.
9. Full ADC performance is available after approximately 5M clock cycles.

For power down, the inverse of this sequence can be followed.

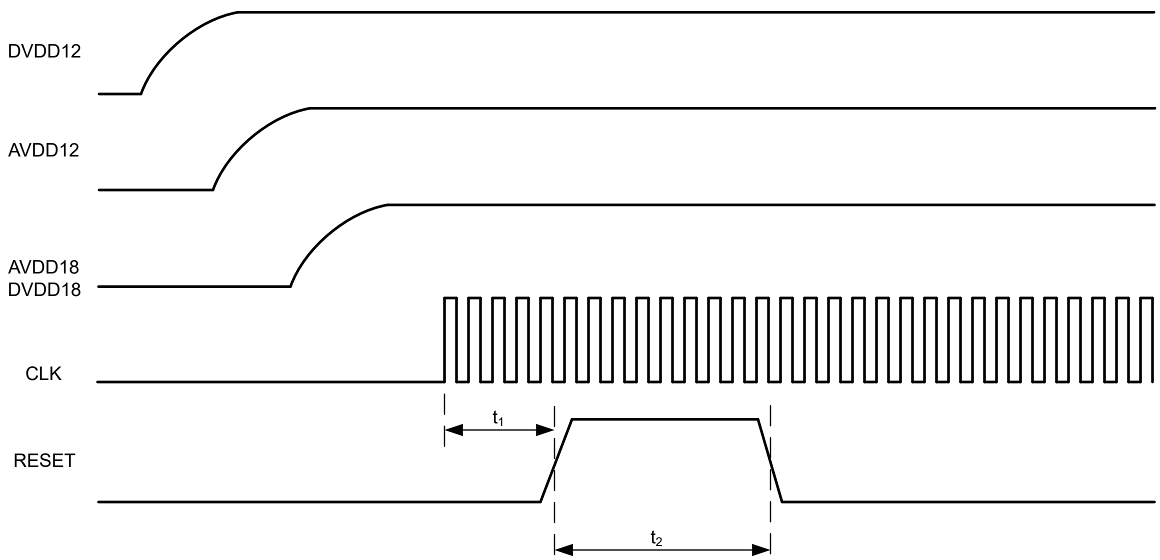


Figure 9-8. Initialization of Serial Registers After Power-Up

Table 9-2. Power-Up Timing

		MIN	TYP	MAX	UNIT
t_1	Power-on delay: delay from power up to active high RESET pulse	1			us
t_2	Reset pulse width: active high RESET pulse width	100			ns

9.3 Power Supply Recommendations

The ADC requires four different power-supplies. The AVDD18 and AVDD12 rails provide power for the internal analog and clocking circuits of the ADC. The DVDD18 and DVDD12 rail powers the digital logic (including averaging and decimation filter) and the LVDS digital interface.

Power sequencing is required as shown in Section 9.2.5. The AVDD18 and AVDD12 power supplies must be low noise to achieve data sheet performance. For applications operating near DC, the 1/f noise contribution of the power supply must also be considered.

Power supply decoupling capacitors (0.1µF) as close to the pins as possible on the top layer are recommended.

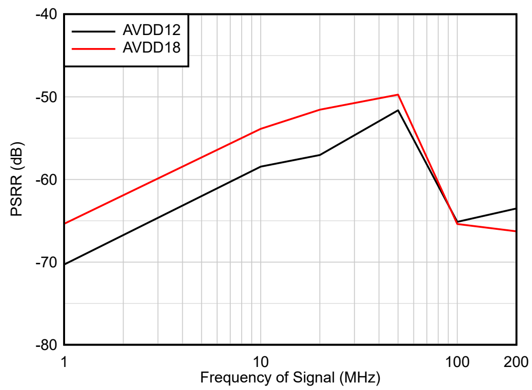


Figure 9-9. Power Supply Rejection Ratio (PSRR) vs Frequency

The recommended power supply architecture for a low noise design is to first use a high-efficiency step down switching regular, followed by a second stage of regulation using a low noise LDO for each power rail as shown in Figure 9-10. This provides additional switching noise reduction and improved voltage accuracy.

TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements. Recommended switching regulators for the first stage include the LMS3635, and similar devices. Recommended low dropout (LDO) linear regulators include the TPS7A8400, and similar devices.

AVDD18 or AVDD12 must not be shared with the DVDD18/12 to prevent digital switching noise from coupling into the analog domain.

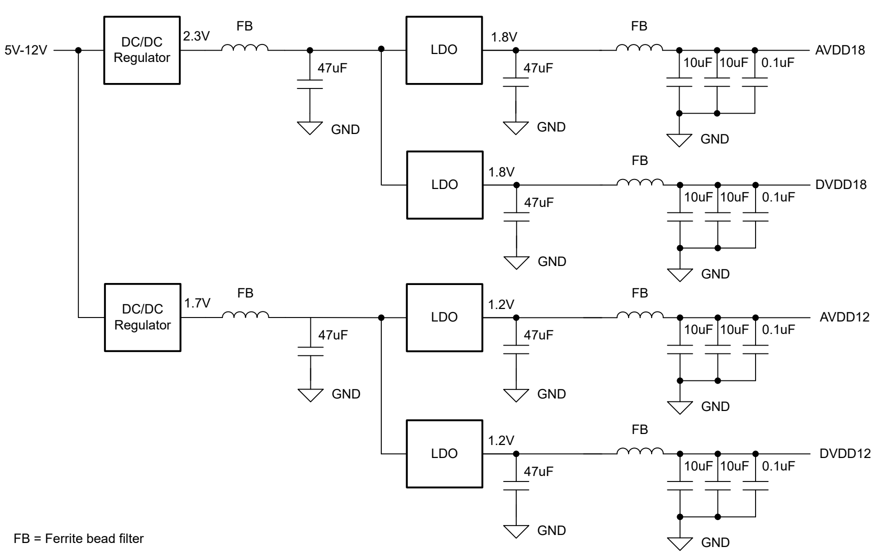


Figure 9-10. Power Supply Design Example

9.4 Layout

9.4.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
   - Make the traces as short as possible, and avoid vias where possible to minimize impedance discontinuities.
   - Traces can be routed using loosely coupled 100Ω differential traces.
   - Match differential trace lengths as close as possible to minimize phase imbalance and HD2 degradation.
2. Digital LVDS output interface
   - Route traces using tightly coupled 100Ω differential traces.
3. Power and ground connections
   - Provide low resistance connection paths to all power and ground pins.
   - Use power and ground planes instead of traces.
   - Avoid narrow, isolated paths which increase the connection resistance.
   - Use a signal, ground, power circuit board stackup to maximize coupling between the ground and power plane.

9.4.2 Layout Example

The following screen shot shows the top layer of the ADC366x EVM.

- The input signal traces are routed as loosely coupled, differential signals on the top layer avoiding vias. Figure 9-11 shows the layout example of the top layer.
- The LVDS output interface lanes are routed differential, tightly coupled and length matched.
- Bypass caps are close to the power pins on the top layer avoiding vias.

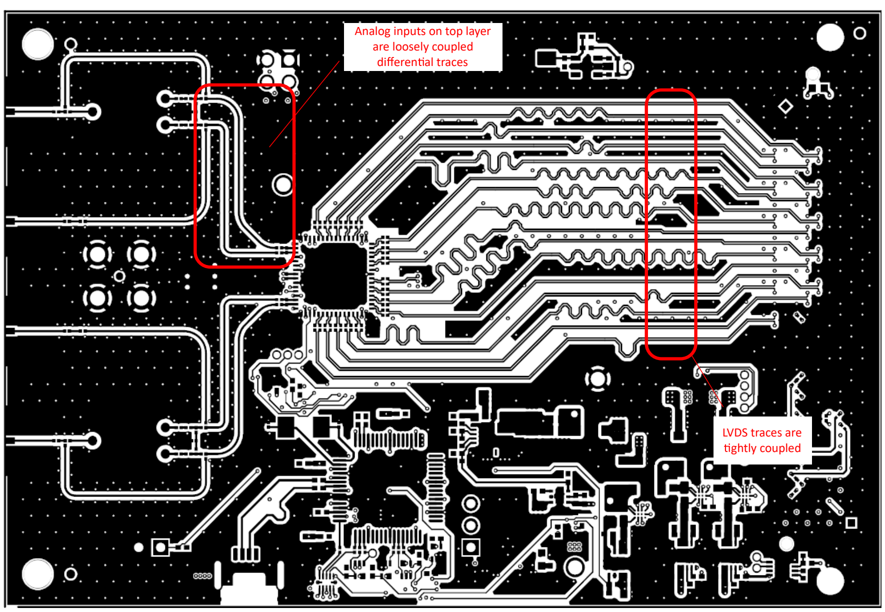


Figure 9-11. Layout example: top layer of ADC366x EVM

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Third-Party Products Disclaimer

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10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2025) to Revision B (June 2025)	Page
• Updated pins SCLK and SDIO from pull-up to DGND to pull-up to DVDD18 in the *Pin Functions*	3
• Changed min sampling rate from 125MSPS to 100MSPS in the CLOCK INPUT (CLKP/M) section	6
• Updated internal equivalent input circuitry with more detailed model in Figure 8-2	24
• Added GPIO pin assignment in step 4 of the power up sequence and added power down sequence	73

Changes from Revision * (September 2024) to Revision A (January 2025)	Page
• Changed the ADC3668 from Product Preview to *Production*	1

- Changed pins SCLK and SDIO from pull-down to pull-up in the *Pin Functions* 3
- Updated max current limits for ADC3668/69............ 6
- Added 0.5Vpp to MIN V_{ID} in the DC Specifications............ 6
- Added min HD2 value in the AC Specification (ADC36698 - 250 MSPS)............ 8
- Added min HD3 value in the AC Specification (ADC3668 - 250 MSPS)............ 8
- Changed the ENOB values in the AC Specifications (ADC3669 - 500 MSPS)............ 9
- Added min HD2 value in the AC Specification (ADC3669 - 500 MSPS)............ 9
- Added min HD3 value in the AC Specification (ADC3669 - 500 MSPS)............ 9
- Added input voltage range description to analog inputs............ 24
- Changed the *Parallel LVDS (DDR)* section............ 40
- Added the *SLVDS - Status Bit Insertion* topic............ 45
- Added the *Output Scrambler* topic............ 46
- Changed the LVDS inversion lane mapping in Table 8-30 56

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC3668IRTD	Active	Production	VQFN (RTD) | 64	260 | JEDEC TRAY (5+1)	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ3668
ADC3668IRTD.A	Active	Production	VQFN (RTD) | 64	260 | JEDEC TRAY (5+1)	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ3668
ADC3668IRTDT	Active	Production	VQFN (RTD) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ3668
ADC3668IRTDT.A	Active	Production	VQFN (RTD) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ3668
ADC3669IRTD	Active	Production	VQFN (RTD) | 64	260 | JEDEC TRAY (5+1)	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ3669
ADC3669IRTD.A	Active	Production	VQFN (RTD) | 64	260 | JEDEC TRAY (5+1)	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ3669
ADC3669IRTDT	Active	Production	VQFN (RTD) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ3669
ADC3669IRTDT.A	Active	Production	VQFN (RTD) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ3669

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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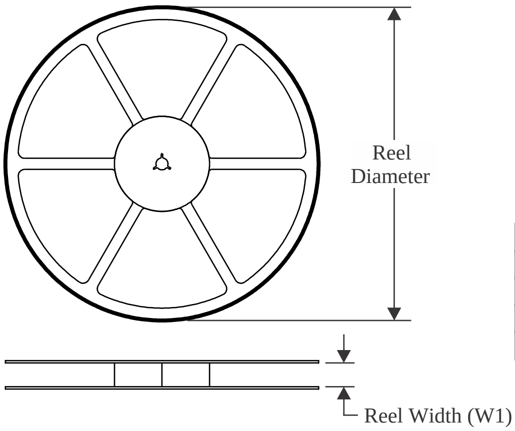
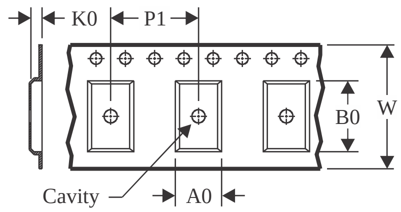
TAPE AND REEL INFORMATION

REEL DIMENSIONS

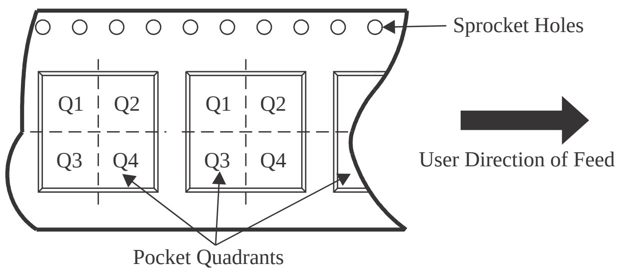


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

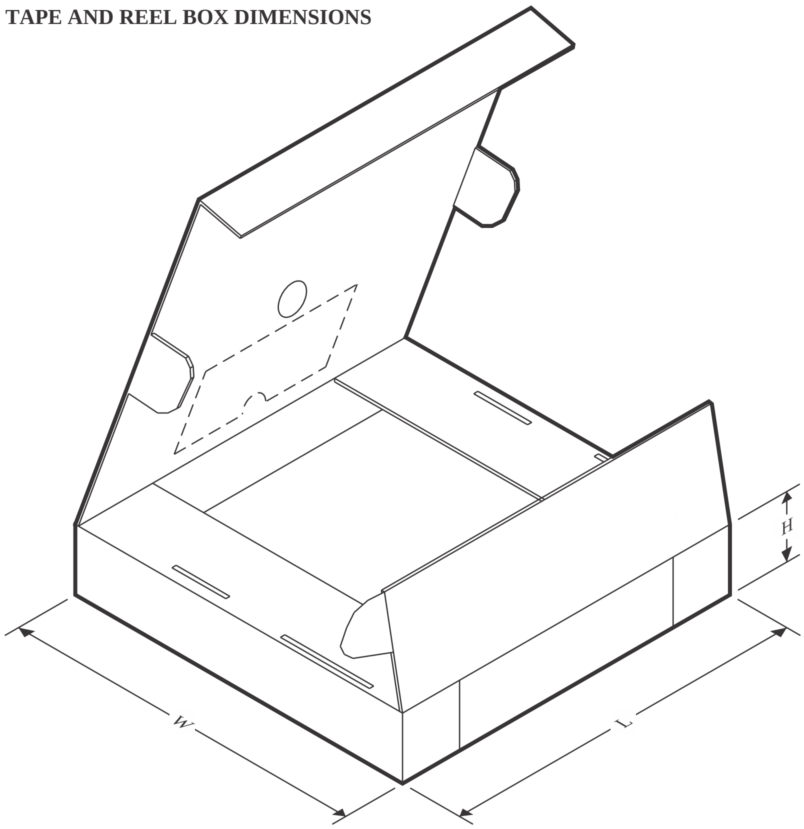
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

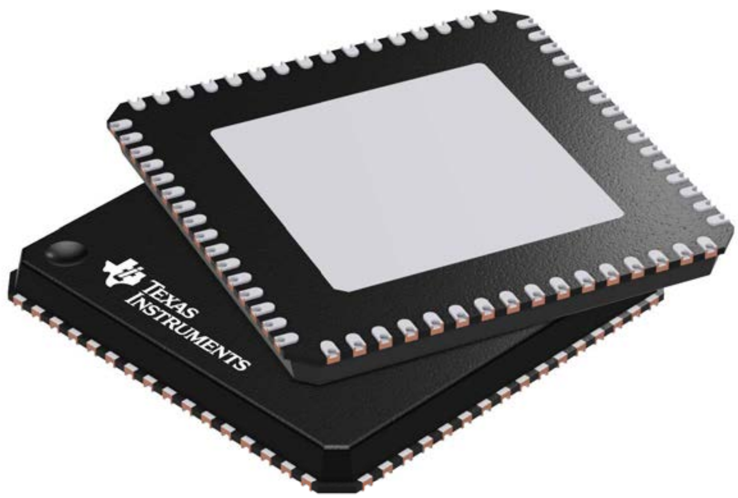
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC3668IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADC3669IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

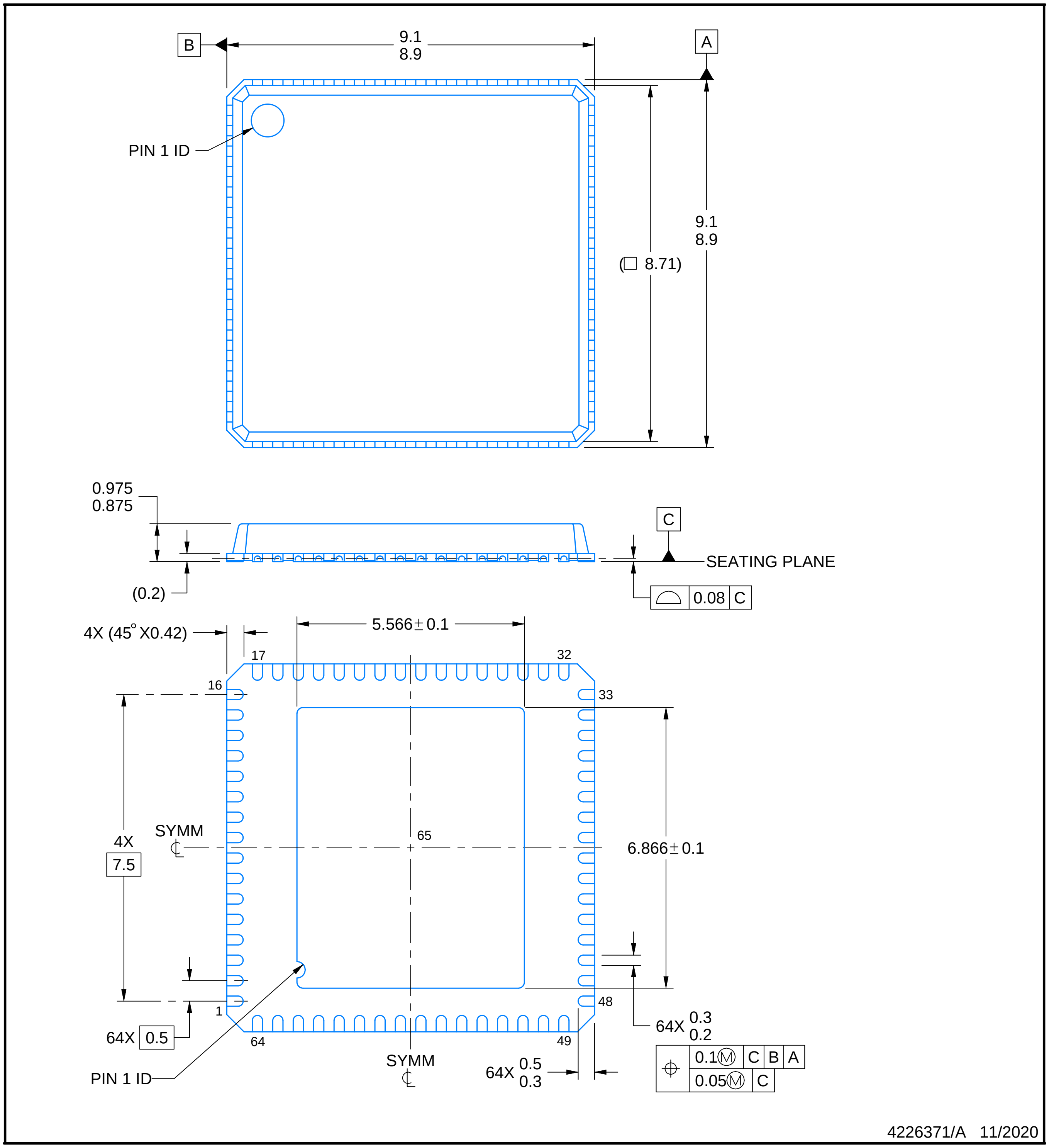


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC3668IRTDT	VQFN	RTD	64	250	213.0	191.0	55.0
ADC3669IRTDT	VQFN	RTD	64	250	213.0	191.0	55.0

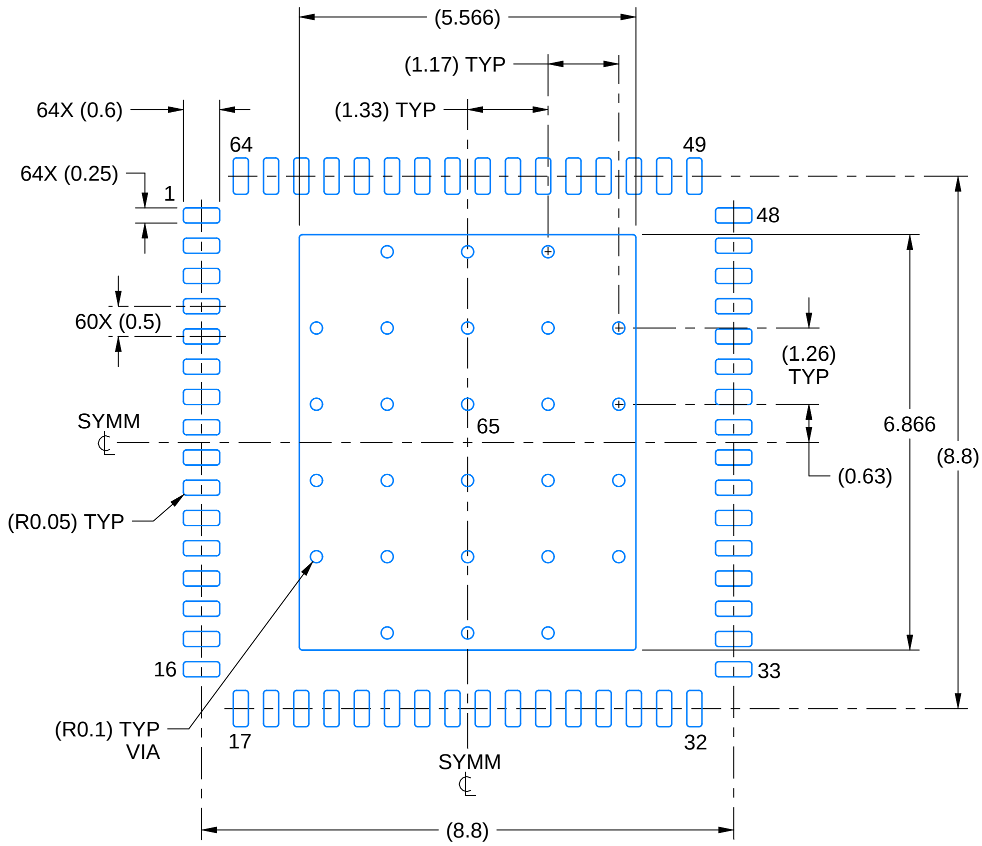


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

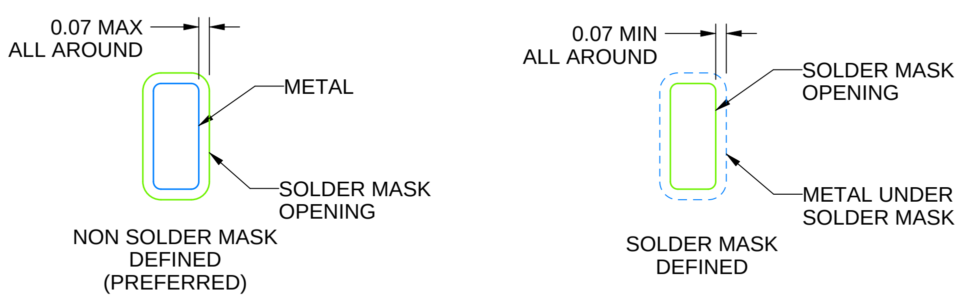


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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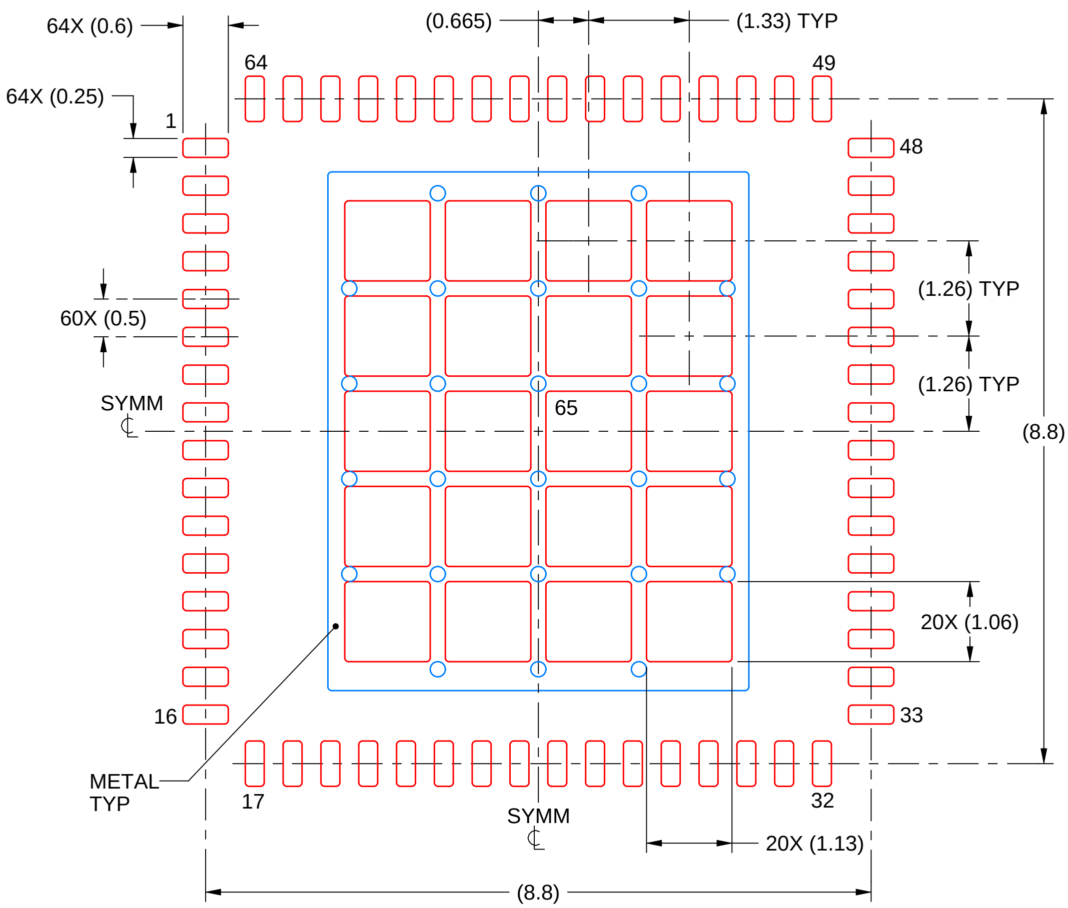
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 65:
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:10X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.