# ADC31RF80 3-GSPS Telecom Receiver and Feedback Device

## 1 Features

- 14-Bit, 3-GSPS ADC
- Noise Floor: –155 dBFS/Hz
- RF Input Supports Up To 4.0 GHz
- Aperture Jitter: 90 $f_S$
- Spectral Performance ($f_{IN}$ = 900 MHz, –2 dBFS):
  - SNR: 61.4 dBFS
  - SFDR: 71-dBc HD2, HD3
  - SFDR: 76-dBc Worst Spur
- Spectral Performance ($f_{IN}$ = 1.85 GHz, –2 dBFS):
  - SNR: 58.5 dBFS
  - SFDR: 65-dBc HD2, HD3
  - SFDR: 75-dBc Worst Spur
- On-Chip Digital Down-Converters:
  - Up to 2 DDCs (Dual-Band Mode)
  - Up to 3 Independent NCOs per DDC
- On-Chip Input Clamp for Overvoltage Protection
- Programmable On-Chip Power Detectors With Alarm Pins for AGC Support
- On-Chip Dither
- On-Chip Input Termination
- Input Full-Scale: 1.35 $V_{PP}$
- Support for Multi-Chip Synchronization
- JESD204B Interface:
  - Subclass 1-Based Deterministic Latency
  - 4 Lanes Support at 12.5 Gbps
- Total Power Dissipation: 3.2 W at 3.0 GSPS
- 72-Pin VQFN Package (10 mm × 10 mm)

## 2 Applications

- Multi-Carrier GSM Cellular Infrastructure Base Stations
- Telecommunications Receivers
- DPD Observation Receivers
- Backhaul Receivers
- RF Repeaters and Distributed Antenna Systems

## 3 Description

The ADC31RF80 device is a 14-bit, 3-GSPS, single-channel telecom receiver and feedback device that supports RF sampling with input frequencies up to 4 GHz and beyond. Designed for high signal-to-noise ratio (SNR), the ADC31RF80 delivers a noise spectral density of –155 dBFS/Hz as well as dynamic range over a large input frequency range. The buffered analog input with on-chip termination provides uniform input impedance across a wide frequency range and minimizes sample-and-hold glitch energy.

The ADC31RF80 comes with a dual-band, digital down-converter (DDC) with up to three independent, 16-bit numerically-controlled oscillators (NCOs) per DDC for phase-coherent frequency hopping. Additionally, the ADC is equipped with front-end peak and RMS power detectors and alarm functions to support external automatic gain control (AGC) algorithms.

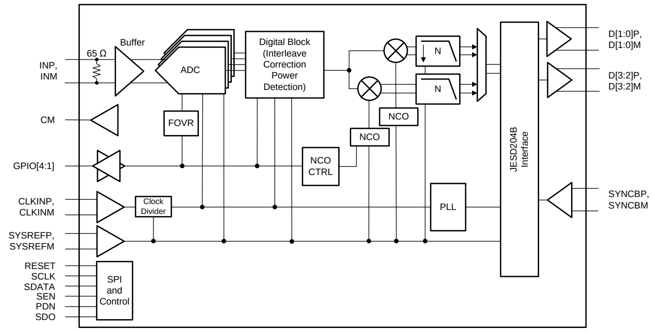
The ADC31RF80 supports the JESD204B serial interface with subclass 1-based deterministic latency using data rates up to 12.5 Gbps with up to four lanes. The device is offered in a 72-pin VQFN package (10 mm × 10 mm) and supports the industrial temperature range (–40°C to +85°C).

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| ADC31RF80 | VQFN (72) | 10.00 mm × 10.00 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

**Simplified Block Diagram**



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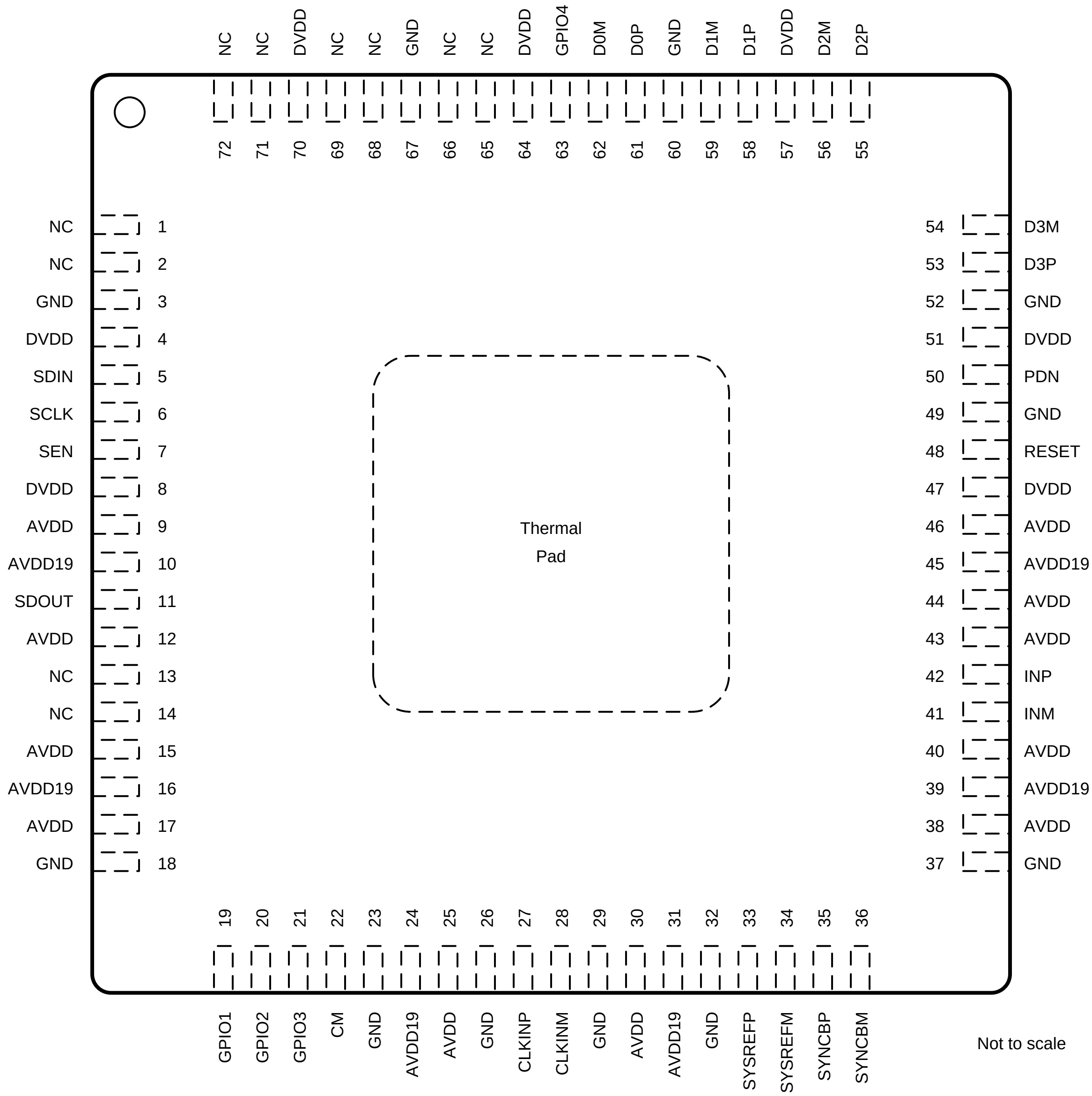
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| August 2017 | * | Initial release. |

# 5 Pin Configuration and Functions

**RMP Package**
**72-Pin VQFN**
**Top View**




## Pin Functions

| NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| **INPUT, REFERENCE** | | | |
| INM | 41 | I | Differential analog input |
| INP | 42 | | |
| CM | 22 | O | Common-mode voltage for analog inputs, 1.2 V |
| NC | 1, 2, 13, 14, 65, 66, 68, 69, 71, 72 | — | Do not connect these pins. |

## Pin Functions (continued)

| NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| **CLOCK, SYNC** | | | |
| CLKINM | 28 | I | Differential clock input for the analog-to-digital converter (ADC). This pin has an internal differential 100-Ω termination. |
| CLKINP | 27 | | |
| SYSREFM | 34 | I | External SYSREF input. This pin has an internal, differential 100-Ω termination and requires external biasing. |
| SYSREFP | 33 | | |
| GPIO1 | 19 | I/O | GPIO control pin; configured through the SPI. This pin can be configured to be either a fast overrange output, a fast detect alarm signal from the peak power detect, or a numerically-controlled oscillator (NCO) control. GPIO 4 (pin 63) can also be configured as a single-ended SYNCB input. |
| GPIO2 | 20 | | |
| GPIO3 | 21 | | |
| GPIO4 | 63 | | |
| **CONTROL, SERIAL** | | | |
| RESET | 48 | I | Hardware reset; active high. This pin has an internal 20-kΩ pulldown resistor. |
| SCLK | 6 | I | Serial interface clock input. This pin has an internal 20-kΩ pulldown resistor. |
| SDIN | 5 | I/O | Serial interface data input. This pin has an internal 20-kΩ pulldown resistor. SDIN can be data input in 4-wire mode, data input and output in 3 wire-mode. |
| SEN | 7 | I | Serial interface enable. This pin has an internal 20-kΩ pullup resistor to DVDD. |
| SDOUT | 11 | O | Serial interface data output in 4-wire mode |
| PDN | 50 | I | Power down; active high. This pin has an internal 20-kΩ pulldown resistor. |
| **DATA INTERFACE** | | | |
| D0M | 62 | O | JESD204B serial data output |
| D0P | 61 | | |
| D1M | 59 | | |
| D1P | 58 | | |
| D2M | 56 | | |
| D2P | 55 | | |
| D3M | 54 | | |
| D3P | 53 | | |
| SYNCBM | 36 | I | Synchronization input for the JESD204B port. This pin has an LVDS or 1.8-V logic input, an optional on-chip 100-Ω termination, and is selectable through the SPI. This pin requires external biasing. |
| SYNCBP | 35 | | |
| **POWER SUPPLY** | | | |
| AVDD19 | 10, 16, 24, 31, 39, 45 | I | Analog 1.9-V power supply |
| AVDD | 9, 12, 15, 17, 25, 30, 38, 40, 43, 44, 46 | I | Analog 1.15-V power supply |
| DVDD | 4, 8, 47, 51, 57, 64, 70 | I | Digital 1.15 V-power supply, including the JESD204B transmitter |
| GND | 3, 18, 23, 26, 29, 32, 37, 49, 52, 60, 67 | I | Ground; shorted to thermal pad inside device |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range | AVDD19 | –0.3 | 2.1 | V |
| | AVDD | –0.3 | 1.4 | |
| | DVDD | –0.3 | 1.4 | |
| Voltage applied to input pins | INP, INM | –0.3 | AVDD19 + 0.3 | V |
| | CLKINP, CLKINM | –0.3 | AVDD + 0.6 | |
| | SYSREFP, SYSREFM, SYNCBP, SYNCBM | –0.3 | AVDD + 0.6 | |
| | SCLK, SEN, SDIN, RESET, PDN, GPIO1, GPIO2, GPIO3, GPIO4 | –0.2 | AVDD19 + 0.2 | |
| Voltage applied to output pins | | –0.3 | 2.2 | V |
| Temperature | Operating free-air, $T_A$ | –40 | 85 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage(1) | AVDD19 | 1.8 | 1.9 | 2.0 | V |
| | AVDD | 1.1 | 1.15 | 1.25 | |
| | DVDD | 1.1 | 1.15 | 1.2 | |
| Temperature | Operating free-air, $T_A$ | –40 | | 85 | °C |
| | Operating junction, $T_J$ | | 105(2) | 125 | |

(1) Always power up the DVDD supply (1.15 V) before the AVDD19 (1.9 V) supply. The AVDD (1.15 V) supply can come up in any order.
(2) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | ADC31RF80 RMP (VQFN) 72 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 21.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 4.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 2.0 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 2.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER CONSUMPTION (Divide-by-4, Complex Output Mode[(1)])** | | | | | | |
| $I_{AVDD19}$ | 1.9-V analog supply current | $f_S$ = 2949.12 MSPS | | 956 | 1439 | mA |
| $I_{AVDD}$ | 1.15-V analog supply current | $f_S$ = 2949.12 MSPS | | 499 | 813 | mA |
| $I_{DVDD}$ | 1.15-V digital supply current | $f_S$ = 2949.12 MSPS | | 975 | 1164 | mA |
| $P_D$ | Power dissipation | $f_S$ = 2949.12 MSPS | | 3.51 | 4.71 | W |
| | Global power-down power dissipation | | | 245 | | mW |
| **ANALOG INPUTS** | | | | | | |
| | Resolution | | | 14 | | Bits |
| | Differential input full-scale | | | 1.35 | | $V_{PP}$ |
| $V_{IC}$ | Input common-mode voltage | | | 1.2[(2)] | | V |
| $R_{IN}$ | Input resistance | Differential resistance at dc | | 65 | | Ω |
| $C_{IN}$ | Input capacitance | Differential capacitance at dc | | 2 | | pF |
| | $V_{CM}$ common-mode voltage output | | | 1.2 | | V |
| | Analog input bandwidth (–3-dB point) | ADC driven with 50-Ω source | | 3200 | | MHz |
| **CLOCK INPUT[(3)]** | | | | | | |
| | Input clock frequency | | 1.5 | 3 | | GSPS |
| | Differential (peak-to-peak) input clock amplitude | | 0.5 | 1.5 | 2.5 | $V_{PP}$ |
| | Input clock duty cycle | | 45% | 50% | 55% | |
| | Internal clock biasing | | | 1.0 | | V |
| | Internal clock termination (differential) | | | 100 | | Ω |

(1) Full-scale signal is applied to the analog input; see the *Power Consumption in Different Modes* section for more details.
(2) When used in dc-coupling mode, the common-mode voltage at the analog inputs should be kept within $V_{CM}$ ±25 mV for best performance.
(3) See Figure 79.

## 6.6 AC Performance Characteristics: $f_S$ = 2949.12 MSPS

typical values specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance(1), AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN(2) | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| SNR | Signal-to-noise ratio | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 63.2 | | dBFS |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 61.4 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | 56 | 58.5 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 57.7 | | |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 56.6 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 54.6 | | |
| NSD | Noise spectral density averaged across the Nyquist zone | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 154.9 | | dBFS/Hz |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 153.1 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | 147.7 | 150.2 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 149.4 | | |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 148.3 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 146.3 | | |
| | Small-signal SNR | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –40 dBFS | | 63.1 | | dBFS |
| NF(4) | Noise figure | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –40 dBFS | | 24.7 | | dB |
| SINAD | Signal-to-noise and distortion ratio | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 62.1 | | dBFS |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 61.0 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 57.8 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 56.9 | | |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 55.7 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 54.5 | | |
| ENOB | Effective number of bits | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 10.0 | | Bits |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 9.8 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 9.3 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 9.2 | | |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 9.0 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 8.8 | | |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 68.0 | | dBc |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 71 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | 58 | 65 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 65 | | |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 63 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 68 | | |
| HD2(5) | Second-order harmonic distortion | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 68 | | dBc |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 71 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | 58 | 65 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 65 | | |
| | | $f_{IN}$ = 2700 MHz, $A_{OUT}$ = –2 dBFS | | 63 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 68 | | |

(1) Performance is shown with DDC bypassed. When DDC is enabled, performance improves by the decimation filtering process.
(2) Minimum values are specified at $A_{OUT}$ = –3 dBFS.
(3) Output amplitude, $A_{OUT}$, refers to the signal amplitude in the ADC digital output that is same as the analog input amplitude, $A_{IN}$, except when the digital gain feature is used. If digital gain is G, then $A_{OUT}$ = G + $A_{IN}$.
(4) The ADC internal resistance = 65 Ω, the driving source resistance = 50 Ω.
(5) The minimum value of HD2 is specified by bench characterization.

## AC Performance Characteristics: $f_S$ = 2949.12 MSPS (continued)

typical values specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance(1), AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN(2) | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| HD3 | Third-order harmonic distortion | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 73 | | dBc |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 80 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | 62 | 71 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 77 | | |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 79 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 76 | | |
| HD4, HD5 | Fourth- and fifth-order harmonic distortion | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 78 | | dBc |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 81.0 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | 69 | 76 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 77 | | |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 77 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 84 | | |
| IL spur | Interleaving spurs: $f_S$ / 2 – $f_{IN}$, $f_S$ / 4 ± $f_{IN}$ | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 89 | | dBc |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 88 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | 68 | 82 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 79 | | |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 81 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 75 | | |
| HD2 IL | Interleaving spur for HD2: $f_S$ / 2 – HD2 | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 85.0 | | dBc |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 79.0 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | 62 | 80.0 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 74.0 | | |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 74.0 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 80.0 | | |
| Worst spur | Spurious-free dynamic range (excluding HD2, HD3, HD4, HD5, and interleaving spurs IL and HD2 IL) | $f_{IN}$ = 100 MHz, $A_{OUT}$ = –2 dBFS | | 83.0 | | dBc |
| | | $f_{IN}$ = 900 MHz, $A_{OUT}$ = –2 dBFS | | 76.0 | | |
| | | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | 64 | 75.0 | | |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 75.0 | | |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 75.0 | | |
| | | $f_{IN}$ = 3500 MHz, $A_{OUT}$(3) = –3 dBFS with 2-dB gain | | 72.0 | | |
| IMD3 | Two-tone, third-order intermodulation distortion | $f_{IN1}$ = 900 MHz, $f_{IN2}$ = 950 MHz, $A_{OUT}$ = –8 dBFS (each tone) | | 79 | | dBFS |
| | | $f_{IN1}$ = 1770 MHz, $f_{IN2}$ = 1790 MHz, $A_{OUT}$ = –8 dBFS (each tone) | | 70 | | |
| | | $f_{IN1}$ = 1800 MHz, $f_{IN2}$ = 2600 MHz, $A_{OUT}$ = –8 dBFS (each tone) | | 73 | | |
| | | $f_{IN1}$ = 3490 MHz, $f_{IN2}$ = 3510 MHz, $A_{OUT}$ = –8 dBFS (each tone) with 2-dB gain | | 67 | | |

## 6.7 AC Performance Characteristics: $f_S$ = 2457.6 MSPS (Performance Optimized for F + A + D Band[(1)])

typical values specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| SNR | Signal-to-noise ratio | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 58.5 | | dBFS |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 55.8 | | |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 60.0 | | dBc |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 57.0 | | |
| HD2 | Second-order harmonic distortion | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 59.0 | | dBc |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 57.0 | | |
| HD3 | Third-order harmonic distortion | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 75.0 | | dBc |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 65.0 | | |
| IL spur | Interleaving spurs: $f_S$ / 2 – $f_{IN}$, $f_S$ / 4 ± $f_{IN}$ | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 84.0 | | dBc |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 76.0 | | |
| HD2 IL | Interleaving spur for HD2: $f_S$ / 2 – HD2 | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 76.0 | | dBc |
| | | $f_{IN}$ = 2600 MHz, $A_{OUT}$ = –2 dBFS | | 67.0 | | |
| IMD3 | Two-tone, third-order intermodulation distortion | $f_{IN1}$ = 1800 MHz, $f_{IN2}$ = 2600 MHz, $A_{OUT}$ = –8 dBFS (each tone) | | 67.0 | | dBFS |

(1) F-band = 1880 MHz to 1920 MHz, A-band = 2010 MHz to 2025 MHz, and D-band = 2570 MHz to 2620 MHz.

## 6.8 AC Performance Characteristics: $f_S$ = 2457.6 MSPS (Performance Optimized for F + A Band[(1)])

typical values specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| SNR | Signal-to-noise ratio | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 58.7 | | dBFS |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 57.9 | | |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 71.0 | | dBc |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 69.0 | | |
| HD2 | Second-order harmonic distortion | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 71.0 | | dBc |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 69.0 | | |
| HD3 | Third-order harmonic distortion | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 75.0 | | dBc |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 76.0 | | |
| IL spur | Interleaving spurs: $f_S$ / 2 – $f_{IN}$, $f_S$ / 4 ± $f_{IN}$ | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 82.0 | | dBc |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 84.0 | | |
| HD2 IL | Interleaving spur for HD2: $f_S$ / 2 – HD2 | $f_{IN}$ = 1850 MHz, $A_{OUT}$ = –2 dBFS | | 80.0 | | dBc |
| | | $f_{IN}$ = 2100 MHz, $A_{OUT}$ = –2 dBFS | | 80.0 | | |

(1) F-band = 1880 MHz to 1920 MHz, A-band = 2010 MHz to 2025 MHz, and D-band = 2570 MHz to 2620 MHz.

## 6.9 Digital Requirements

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

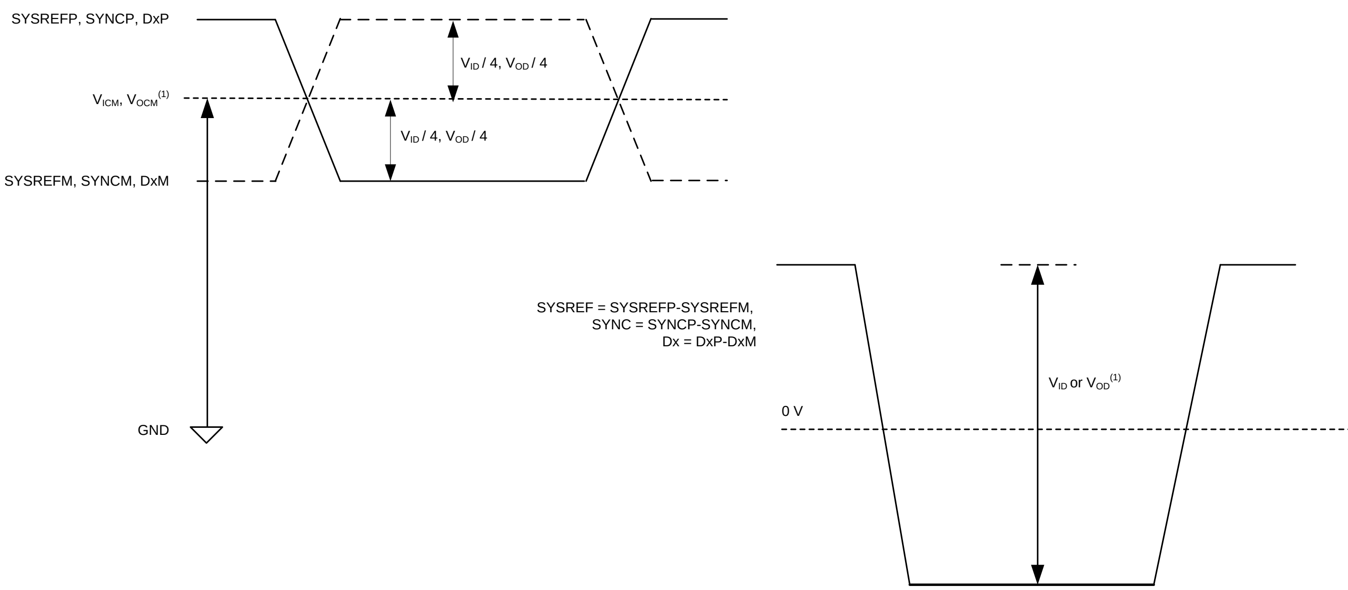
| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS (RESET, SCLK, SEN, SDIN, PDN, GPIO1, GPIO2, GPIO3, GPIO4)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.8 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.4 | V |
| $I_{IH}$ | High-level input current | | | 50 | | µA |
| $I_{IL}$ | Low-level input current | | | –50 | | µA |
| $C_i$ | Input capacitance | | | 4 | | pF |
| **DIGITAL OUTPUTS (SDOUT, GPIO1, GPIO2, GPIO3, GPIO4)** | | | | | | |
| $V_{OH}$ | High-level output voltage | | AVDD19 –0.1 | AVDD19 | | V |
| $V_{OL}$ | Low-level output voltage | | | | 0.1 | V |
| **DIGITAL INPUTS (SYSREFP and SYSREFM; SYNCBP and SYNCBM; Requires External Biasing)** | | | | | | |
| $V_{ID}$ | Differential input voltage | | 350 | 450 | 800 | $mV_{PP}$ |
| $V_{CM}$ | Input common-mode voltage | | 1.05 | 1.2 | 1.325 | V |
| **DIGITAL OUTPUTS (JESD204B Interface: D[3:0], Meets JESD204B LV-0IF-11G-SR Standard)** | | | | | | |
| $\|V_{OD}\|$ | Output differential voltage | | | 700 | | $mV_{PP}$ |
| $\|V_{OCM}\|$ | Output common-mode voltage | | | 450 | | mV |
| | Transmitter short-circuit current | Transmitter pins shorted to any voltage between –0.25 V and 1.45 V | –100 | | 100 | mA |
| $z_{os}$ | Single-ended output impedance | | | 50 | | Ω |
| $C_o$ | Output capacitance | Output capacitance inside the device, from either output to ground | | 2 | | pF |

## 6.10 Timing Requirements

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and chip sampling rate = 2949.12 MSPS, 50% clock duty cycle, DDC-bypassed performance, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SAMPLE TIMING** | | | | | | |
| | Aperture delay | | 250 | | 750 | ps |
| | Aperture delay matching between two devices at the same temperature and supply voltage | | | ±150 | | ps |
| | Aperture jitter, clock amplitude = 2 $V_{PP}$ | | | 90 | | $f_S$ |
| Latency (1)(2) | Data latency, ADC sample to digital output | DDC block bypassed | | 424 | | Input clock cycles |
| | Fast overrange latency, ADC sample to FOVR indication on GPIO pins | | | 70 | | |
| $t_{PD}$ | Propagation delay time: logic gates and output buffer delay (does not change with $f_S$) | | | 6 | | ns |
| **SYSREF TIMING (3)** | | | | | | |
| $t_{SU\_SYSREF}$ | SYSREF setup time: referenced to clock rising edge, 2949.12 MSPS | | 140 | 70 | | ps |
| $t_{H\_SYSREF}$ | SYSREF hold time: referenced to clock rising edge, 2949.12 MSPS | | 50 | 20 | | ps |
| | Valid transition window sampling period: $t_{SU\_SYSREF}$ – $t_{H\_SYSREF}$, 2949.12 MSPS | | 143 | | | ps |
| **JESD OUTPUT INTERFACE TIMING** | | | | | | |
| UI | Unit interval: 12.5 Gbps | | 80 | 100 | 400 | ps |
| | Serial output data rate | | 2.5 | 10.0 | 12.5 | Gbps |
| | Rise, fall times: 1-pF, single-ended load capacitance to ground | | | 60 | | ps |
| | Total jitter: BER of 1E-15 and lane rate = 12.5 Gbps | | | 25 | | %UI |
| | Random jitter: BER of 1E-15 and lane rate = 12.5 Gbps | | | 0.99 | | %UI, rms |
| | Deterministic jitter: BER of 1E-15 and lane rate = 12.5 Gbps | | | 9.1 | | %UI, pk-pk |

(1) Overall latency = latency + $t_{PD}$.
(2) Latency increases when the DDC modes are used; see Table 4.
(3) Common-mode voltage for the SYSREF input is kept at 1.2 V.




$V_{OCM}$ is not the same as $V_{ICM}$. Similarly, $V_{OD}$ is not the same as $V_{ID}$.

**Figure 1. Logic Levels for Digital Inputs and Outputs**

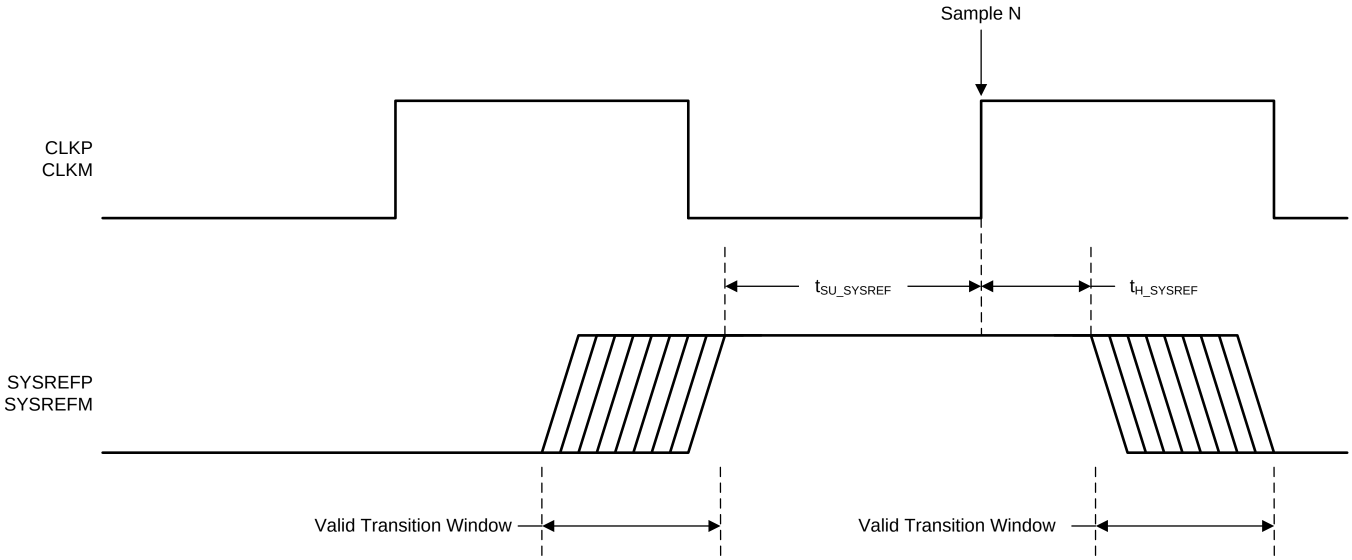
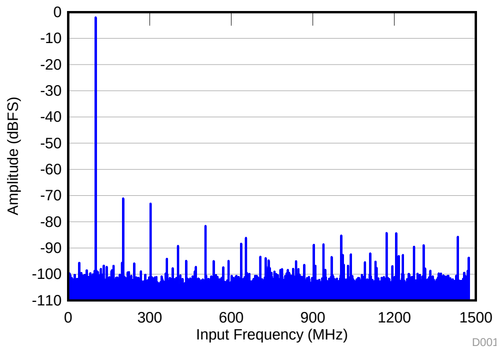



**Figure 2. SYSREF Timing Diagram**

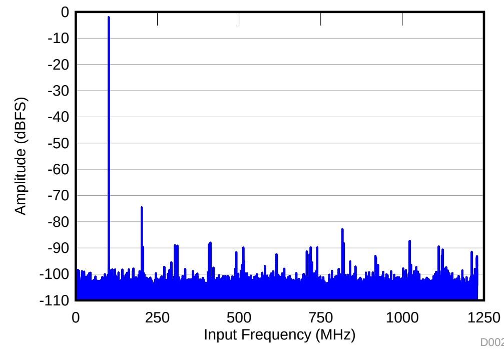
## 6.11 Typical Characteristics

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



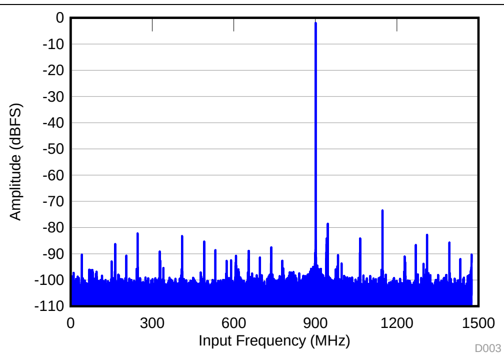

SNR = 63.4 dBFS; SFDR = 69 dBc;
HD2 = –69 dBc; HD3 = –71 dBc; non HD2, HD3 = 80 dBc;
IL spur = 82 dBc; $f_{IN}$ = 100 MHz

**Figure 3. FFT for 100-MHz Input Frequency**



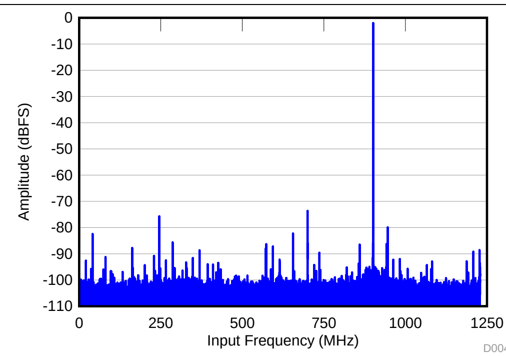

SNR = 63.3 dBFS; SFDR = 72 dBc;
HD2 = –72 dBc; HD3 = –87 dBc; non HD2, HD3 = 85 dBc;
IL spur = 80 dBc; $f_{IN}$ = 100 MHz

**Figure 4. FFT for 100-MHz Input Signal ($f_S$ = 2457.6 MSPS)**



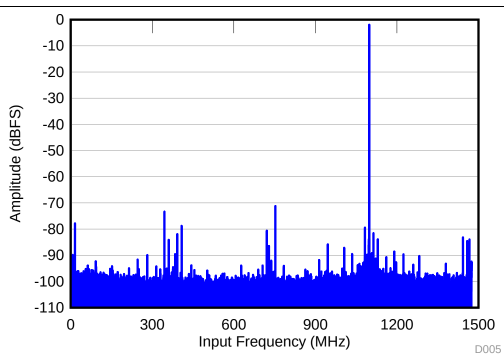

SNR = 60.8 dBFS; SFDR = 71 dBc;
HD2 = –71 dBc; HD3 = –80 dBc; non HD2, HD3 = 83 dBc;
IL spur = 83 dBc; $f_{IN}$ = 900 MHz

**Figure 5. FFT for 900-MHz Input Signal**



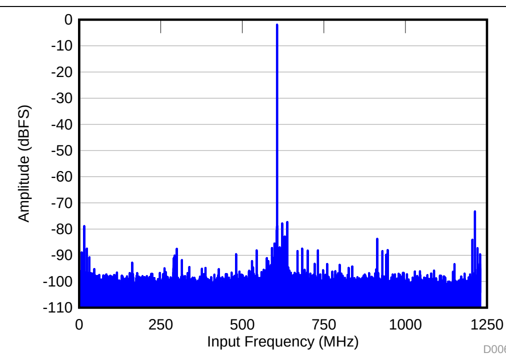

SNR = 61.4 dBFS; SFDR = 71 dBc;
HD2 = –80 dBc; HD3 = –73 dBc; non HD2, HD3 = 74 dBc;
IL spur = 80 dBc; $f_{IN}$ = 900 MHz

**Figure 6. FFT for 900-MHz Input Signal ($f_S$ = 2457.6 MSPS)**




SNR = 58.9 dBFS; SFDR = 69 dBc;
HD2 = –69 dBc; HD3 = –71 dBc; non HD2, HD3 = 77 dBc;
IL spur = 76 dBc; $f_{IN}$ = 1.85 GHz

**Figure 7. FFT for 1850-MHz Input Signal**

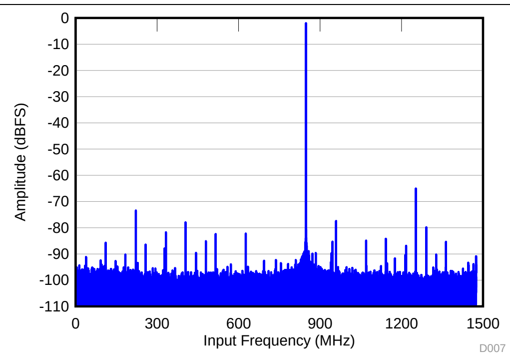



SNR = 58.9 dBFS; SFDR = 71 dBc;
HD2 = –71 dBc; HD3 = –75 dBc; non HD2, HD3 = 78 dBc;
IL spur = 76 dBc; $f_{IN}$ = 1.85 GHz

**Figure 8. FFT for 1850-MHz Input Signal ($f_S$ = 2457.6 MSPS)**

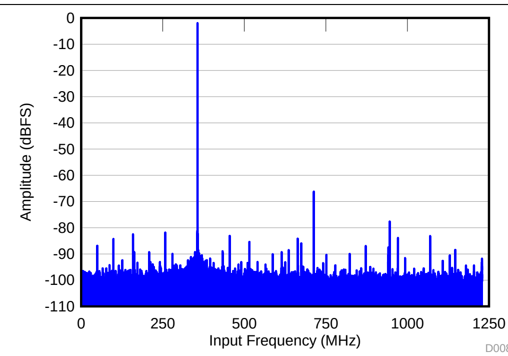
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



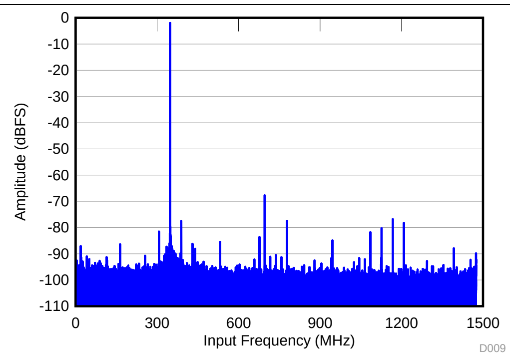

SNR = 57.9 dBFS; SFDR = 63 dBc;
HD2 = –63 dBc; HD3 = –76 dBc; non HD2, HD3 = 78 dBc;
IL spur = 73 dBc; $f_{IN}$ = 2.1 GHz

**Figure 9. FFT for 2100-MHz Input Signal**



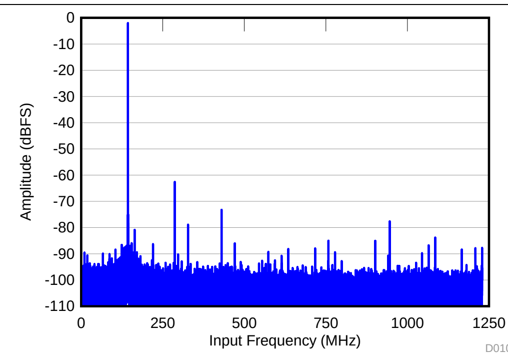

SNR = 58.2 dBFS; SFDR = 64 dBc;
HD2 = –64 dBc; HD3 = –81 dBc; non HD2, HD3 = 83 dBc;
IL spur = 80 dBc; $f_{IN}$ = 2.1 GHz

**Figure 10. FFT for 2100-MHz Input Signal ($f_S$ = 2457.6 MSPS)**



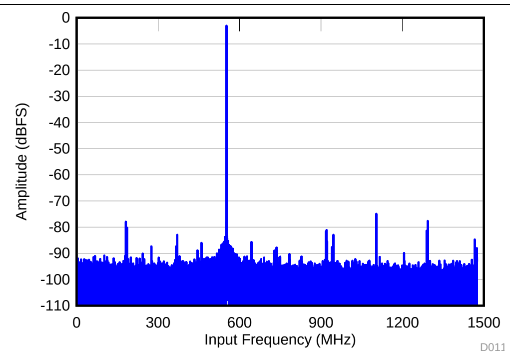

SNR = 56.8 dBFS; SFDR = 65 dBc;
HD2 = –65 dBc; HD3 = –71 dBc; non HD2, HD3 = 89 dBc;
IL spur = 74 dBc; $f_{IN}$ = 2.6 GHz

**Figure 11. FFT for 2600-MHz Input Signal**



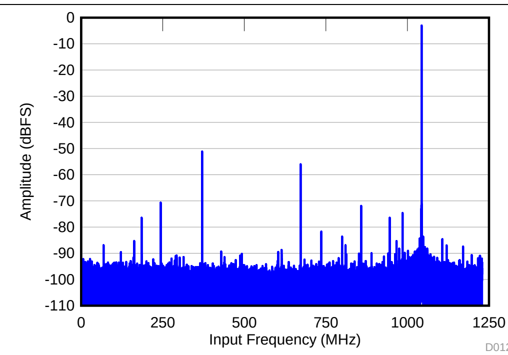

SNR = 56.8 dBFS; SFDR = 60 dBc;
HD2 = –60 dBc; HD3 = –71 dBc; non HD2, HD3 = 73 dBc;
IL spur = 75 dBc; $f_{IN}$ = 2.6 GHz

**Figure 12. FFT for 2600-MHz Input Signal ($f_S$ = 2457.6 MSPS)**




SNR = 54.6 dBFS; SFDR = 70 dBc;
HD2 = –72 dBc; HD3 = –74 dBc; non HD2, HD3 = 70 dBc;
IL spur = 76 dBc; $f_{IN}$ = 3.5 GHz, $A_{IN}$ = –3 dBFS with 2-dB gain

**Figure 13. FFT for 3500-MHz Input Signal**

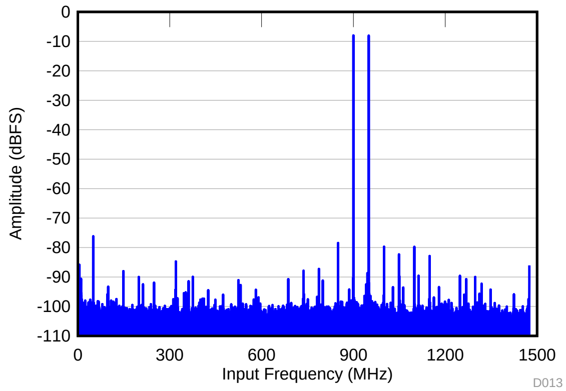



SNR = 54.9 dBFS; SFDR = 48 dBc;
HD2 = –48 dBc; HD3 = –53 dBc; non HD2, HD3 = 68 dBc;
IL spur = 69 dBc; $f_{IN}$ = 3.5 GHz, $A_{IN}$ = –3 dBFS with 2-dB gain

**Figure 14. FFT for 3500-MHz Input Signal ($f_S$ = 2457.6 MSPS)**

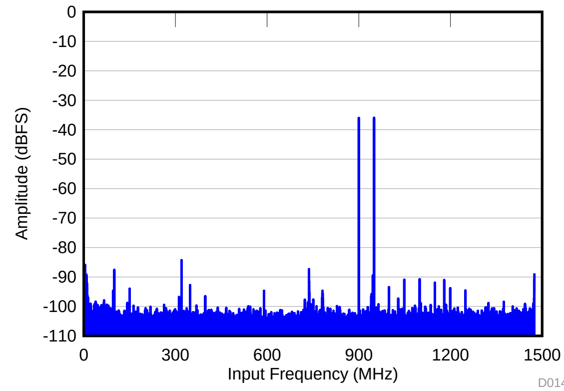
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



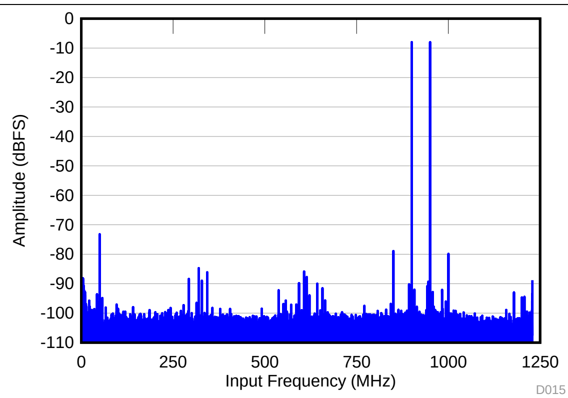

$f_{IN1}$ = 900 MHz, $f_{IN2}$ = 950 MHz, $A_{IN}$ = –8 dBFS, IMD = 79 dBFS

**Figure 15. FFT for Two-Tone Input Signal (–8 dBFS)**



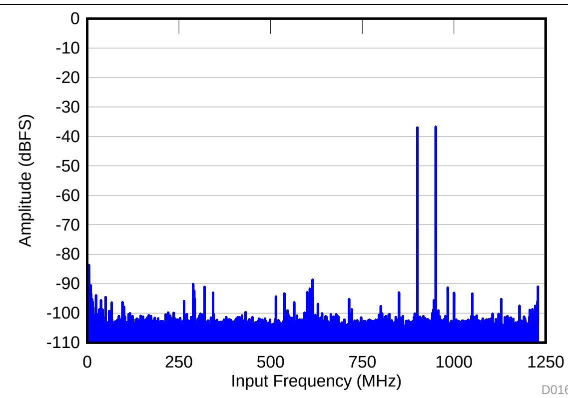

$f_{IN1}$ = 900 MHz, $f_{IN2}$ = 950 MHz, $A_{IN}$ = –36 dBFS, IMD = 94 dBFS

**Figure 16. FFT for Two-Tone Input Signal (–36 dBFS)**



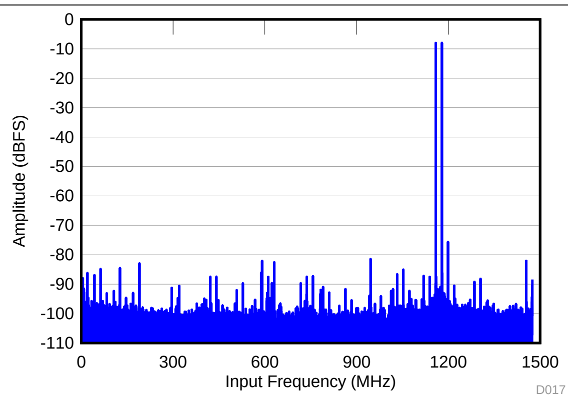

$f_{IN1}$ = 900 MHz, $f_{IN2}$ = 950 MHz, $A_{IN}$ = –8 dBFS, IMD = 78 dBFS

**Figure 17. FFT for Two-Tone Input Signal (–8 dBFS, $f_S$ = 2457.6 MSPS)**



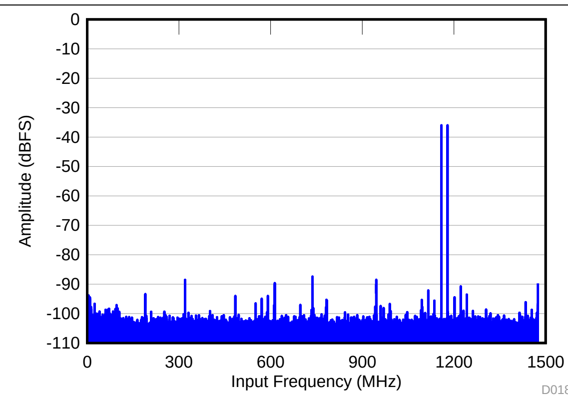

$f_{IN1}$ = 900 MHz, $f_{IN2}$ = 950 MHz, $A_{IN}$ = –36 dBFS, IMD = 92 dBFS

**Figure 18. FFT for Two-Tone Input Signal (–36 dBFS, $f_S$ = 2457.6 MSPS)**




$f_{IN1}$ = 1.77 GHz, $f_{IN2}$ = 1.79 GHz, $A_{IN}$ = –8 dBFS, IMD = 75 dBFS

**Figure 19. FFT for Two-Tone Input Signal (–8 dBFS)**

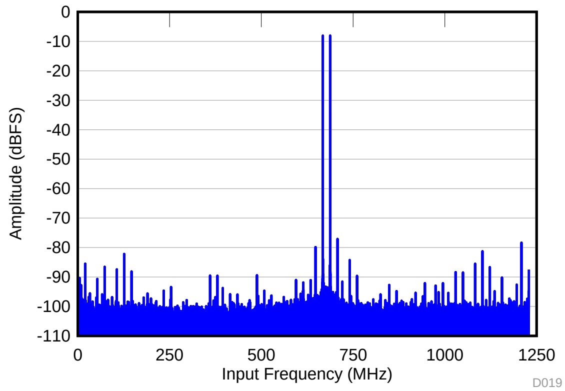



$f_{IN1}$ = 1.77 GHz, $f_{IN2}$ = 1.790 GHz, $A_{IN}$ = –36 dBFS, IMD = 94 dBFS

**Figure 20. FFT for Two-Tone Input Signal (–36 dBFS)**

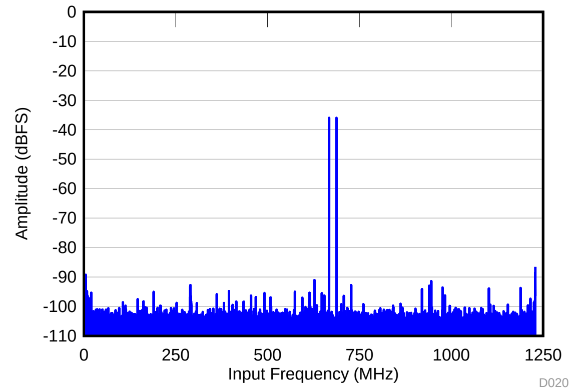
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



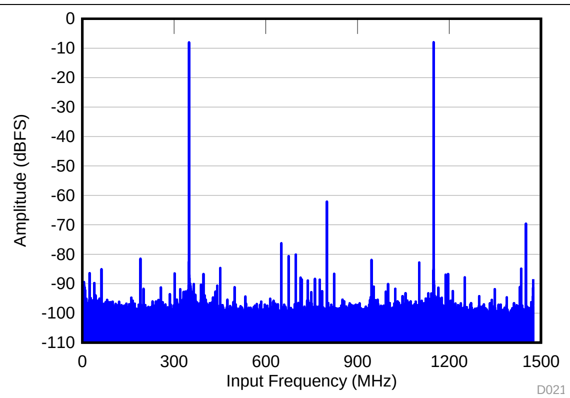

$f_{IN1}$ = 1.77 GHz, $f_{IN2}$ = 1.79 GHz, $A_{IN}$ = –8 dBFS, IMD = 76 dBFS

**Figure 21. FFT for Two-Tone Input Signal (–8 dBFS, $f_S$ = 2457.6 MSPS)**



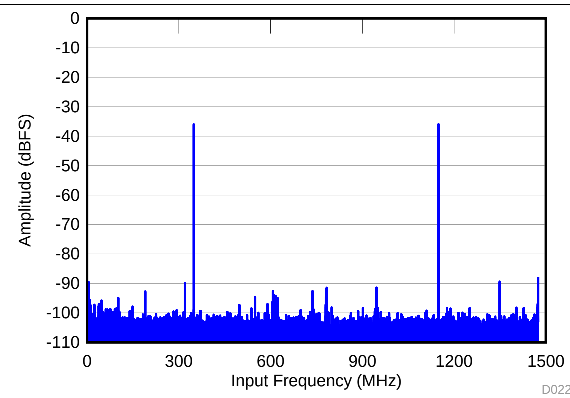

$f_{IN1}$ = 1.77 GHz, $f_{IN2}$ = 1.790 GHz, $A_{IN}$ = –36 dBFS, IMD = 92 dBFS

**Figure 22. FFT for Two-Tone Input Signal (–36 dBFS, $f_S$ = 2457.6 MSPS)**



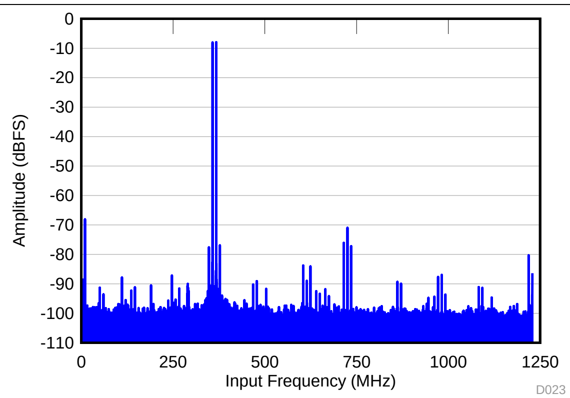

$f_{IN1}$ = 1.8 MHz, $f_{IN2}$ = 2.6 GHz, $A_{IN}$ = –8 dBFS, IMD = 70 dBFS

**Figure 23. FFT for Two-Tone Input Signal (–8 dBFS)**



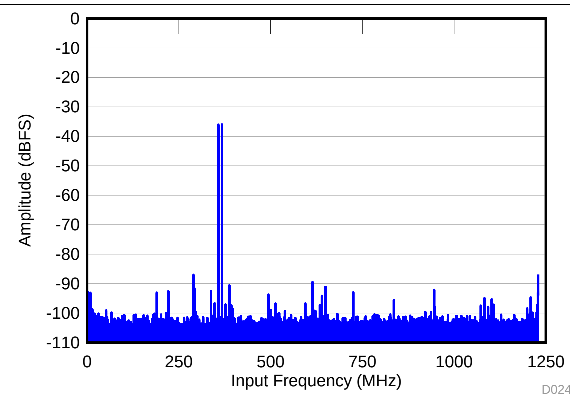

$f_{IN1}$ = 1.8 GHz, $f_{IN2}$ = 2.6 GHz, $A_{IN}$ = –36 dBFS, IMD = 95 dBFS

**Figure 24. FFT for Two-Tone Input Signal (–36 dBFS)**




$f_{IN1}$ = 2.09 GHz, $f_{IN2}$ = 2.1 GHz, $A_{IN}$ = –8 dBFS, IMD = 71 dBFS

**Figure 25. FFT for Two-Tone Input Signal (–8 dBFS, $f_S$ = 2457.6 MSPS)**

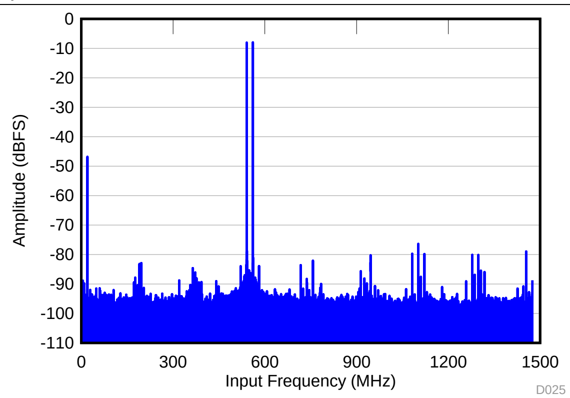



$f_{IN1}$ = 2.09 MHz, $f_{IN2}$ = 2.1 GHz, $A_{IN}$ = –36 dBFS, IMD = 92 dBFS

**Figure 26. FFT for Two-Tone Input Signal (–36 dBFS, $f_S$ = 2457.6 MSPS)**

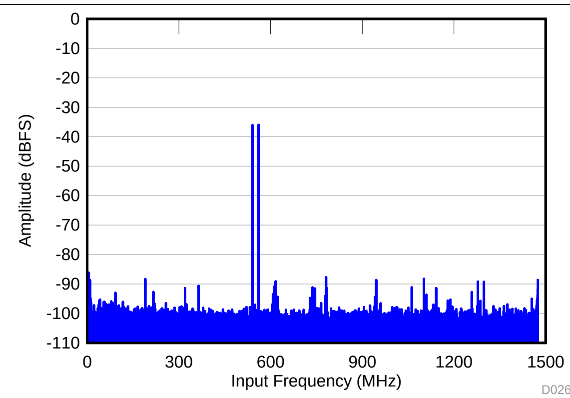
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



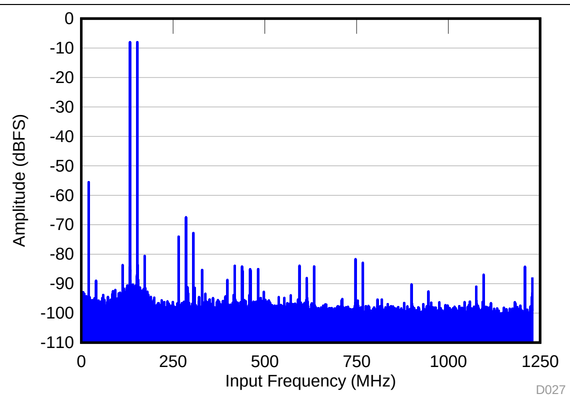

$f_{IN1}$ = 3.49 MHz, $f_{IN2}$ = 3.51 GHz, IMD = 75 dBFS, $A_{IN}$ = –8 dBFS with 2-dB gain

**Figure 27. FFT for Two-Tone Input Signal (–8 dBFS)**



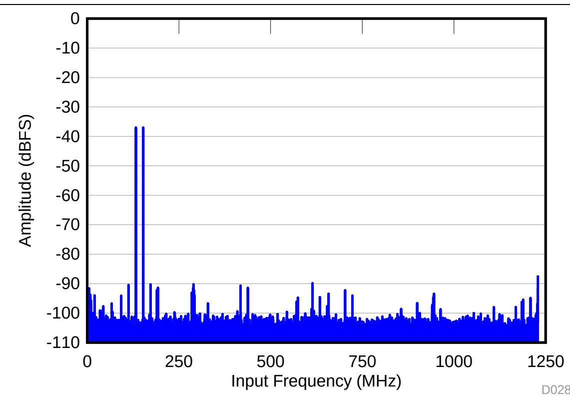

$f_{IN1}$ = 3.49 GHz, $f_{IN2}$ = 3.51 GHz, IMD = 95 dBFS, $A_{IN}$ = –36 dBFS with 2-dB gain

**Figure 28. FFT for Two-Tone Input Signal (–36 dBFS)**



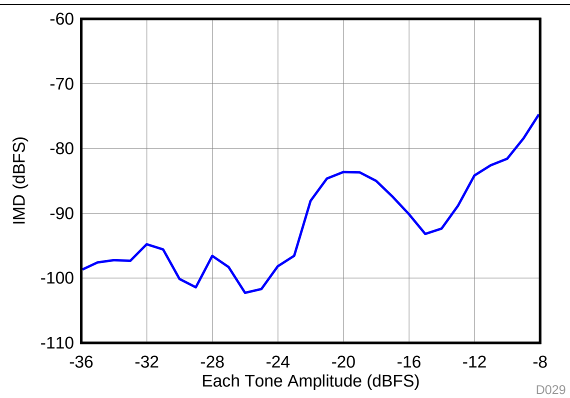

$f_{IN1}$ = 2.59 GHz, $f_{IN2}$ = 2.6 GHz, $A_{IN}$ = –8 dBFS, IMD = 68 dBFS

**Figure 29. FFT for Two-Tone Input Signal (–8 dBFS, $f_S$ = 2457.6 MSPS)**



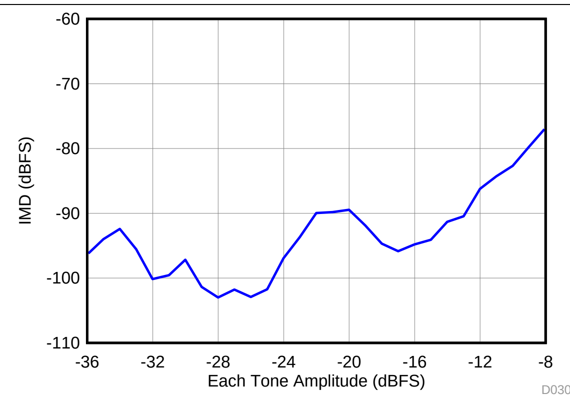

$f_{IN1}$ = 2.59 GHz, $f_{IN2}$ = 2.6 GHz, $A_{IN}$ = –36 dBFS, IMD = 92 dBFS

**Figure 30. FFT for Two-Tone Input Signal (–36 dBFS, $f_S$ = 2457.6 MSPS)**




$f_{IN1}$ = 1.77 GHz, $f_{IN2}$ = 1.79 GHz

**Figure 31. Intermodulation Distortion vs Input Amplitude (1770 MHz and 1790 MHz)**

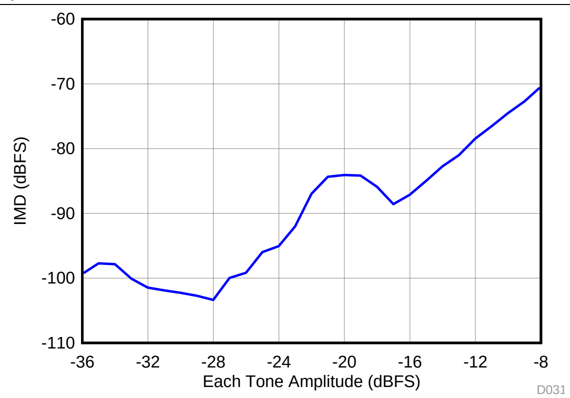



$f_{IN1}$ = 1.77 GHz, $f_{IN2}$ = 1.79 GHz

**Figure 32. Intermodulation Distortion vs Input Amplitude (1770 MHz and 1790 MHz, $f_S$ = 2457.6 MSPS)**

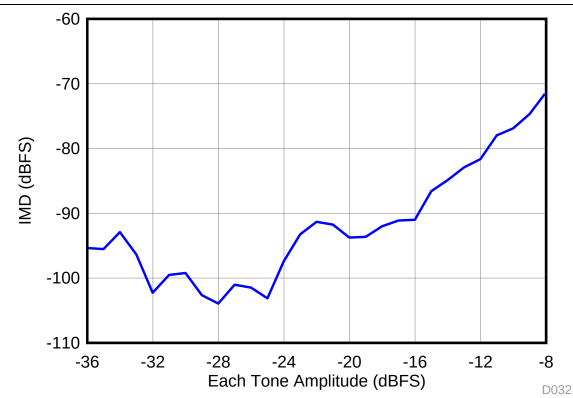
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



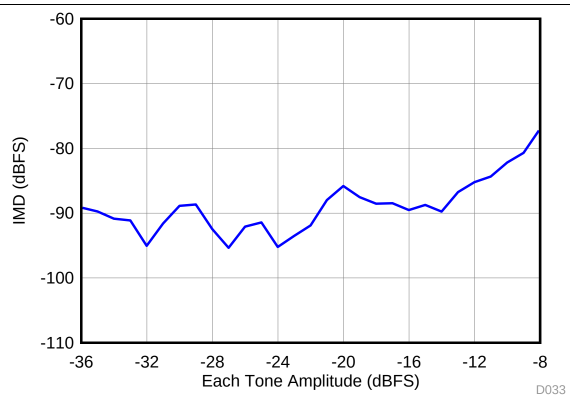

$f_{IN1}$ = 1.8 GHz, $f_{IN2}$ = 2.6 GHz, $A_{IN}$ = –36 dBFS

**Figure 33. Intermodulation Distortion vs Input Amplitude (1800 MHz and 2600 MHz)**



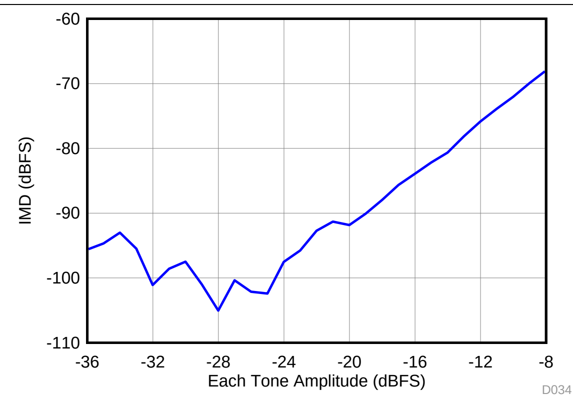

$f_{IN1}$ = 2.09 GHz, $f_{IN2}$ = 2.1 GHz

**Figure 34. Intermodulation Distortion vs Input Amplitude (2090 MHz and 2100 MHz, $f_S$ = 2457.6 MSPS)**




$f_{IN1}$ = 3.49 GHz, $f_{IN2}$ = 3.51 GHz with 2-dB digital gain

**Figure 35. Intermodulation Distortion vs Input Amplitude (3490 MHz and 3510 MHz)**




$f_{IN1}$ = 2.59GHz, $f_{IN2}$ = 2.61 GHz

**Figure 36. Intermodulation Distortion vs Input Amplitude (2590 MHz and 2600 MHz, $f_S$ = 2457.6 MSPS)**

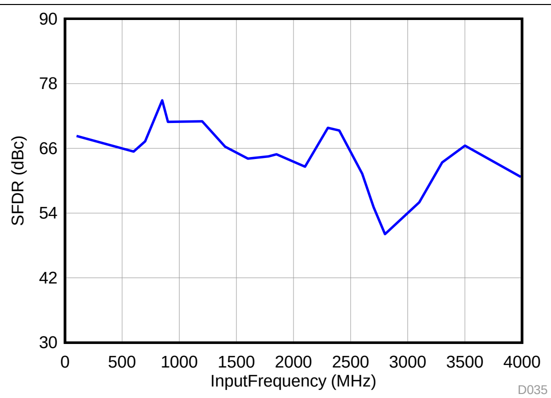



**Figure 37. Spurious-Free Dynamic Range vs Input Frequency**

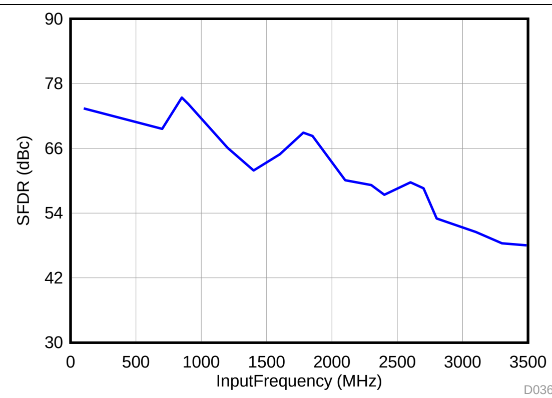



**Figure 38. Spurious-Free Dynamic Range vs Input Frequency ($f_S$ = 2457.6 MSPS)**

## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

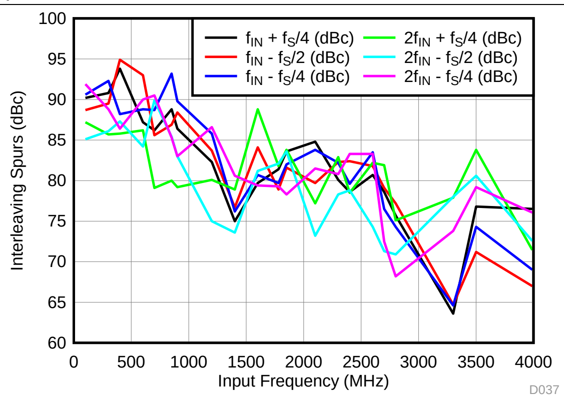



**Figure 39. IL Spur vs Input Frequency**

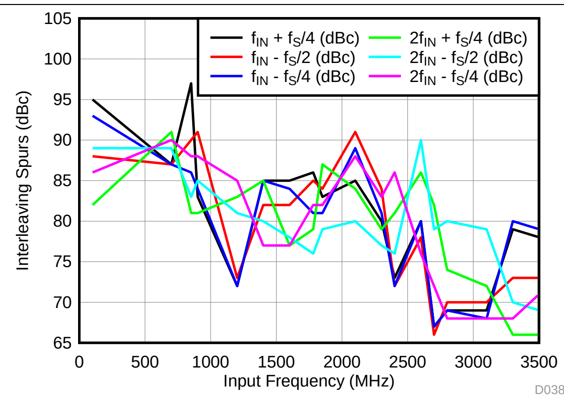



**Figure 40. IL Spur vs Input Frequency ($f_S$ = 2457.6 MSPS)**

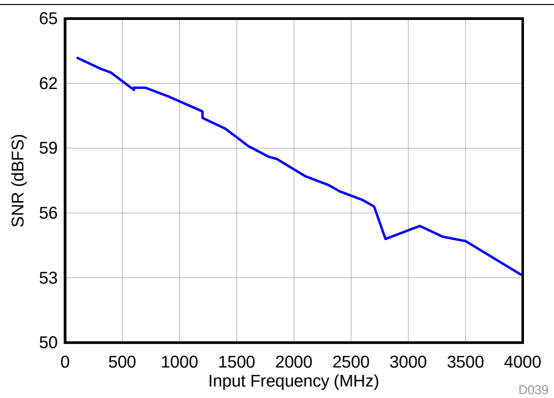



**Figure 41. Signal-to-Noise Ratio vs Input Frequency**

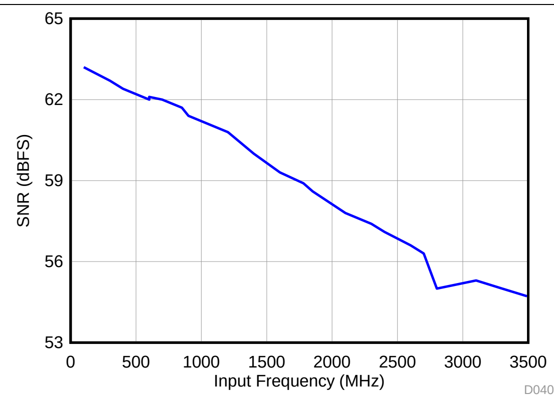
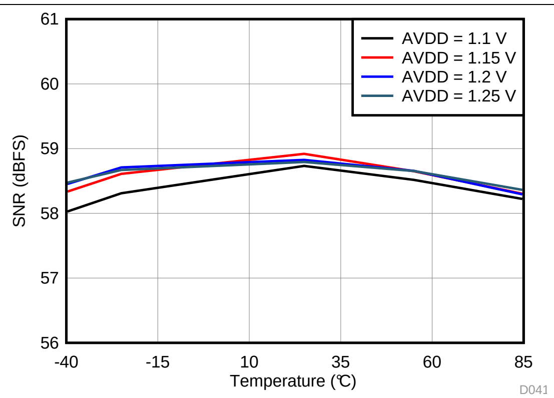
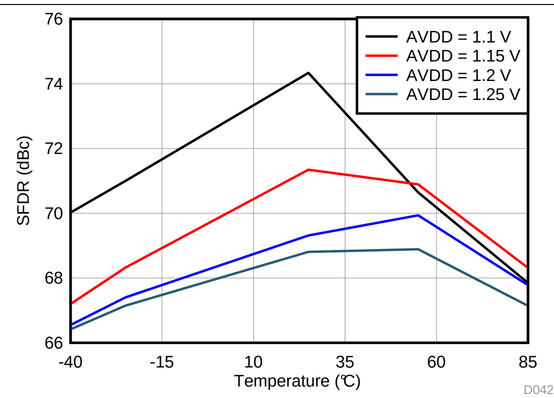



**Figure 42. Signal-to-Noise Ratio vs Input Frequency ($f_S$ = 2457.6 MSPS)**




$f_{IN}$ = 1.85 GHz, $A_{IN}$ = –2 dBFS

**Figure 43. Signal-to-Noise Ratio vs AVDD Supply and Temperature**

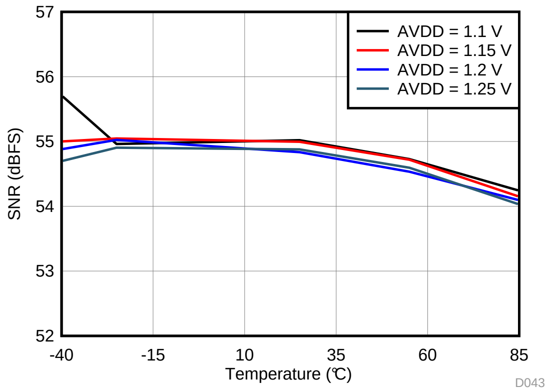



$f_{IN}$ = 1.85 GHz, $A_{IN}$ = –2 dBFS

**Figure 44. Spurious-Free Dynamic Range vs AVDD Supply and Temperature**

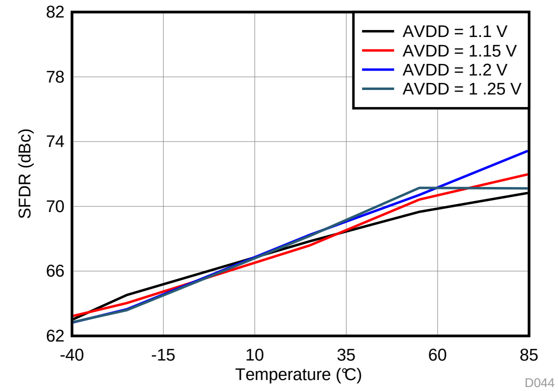
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



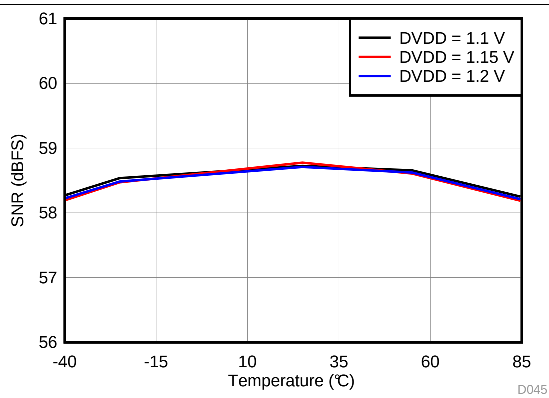

$f_{IN}$ = 3.5 GHz, $A_{IN}$ = –3 dBFS with 2-dB digital gain

**Figure 45. Signal-to-Noise Ratio vs AVDD Supply and Temperature**



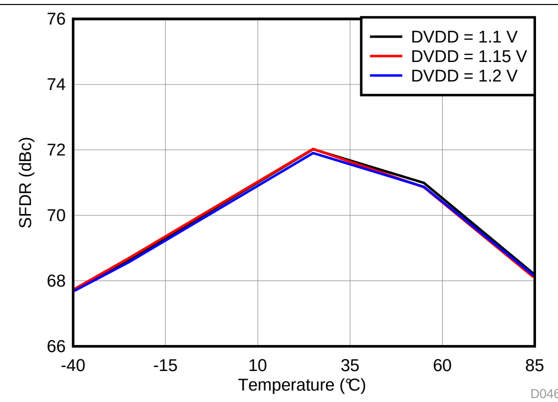

$f_{IN}$ = 3.5GHz, $A_{IN}$ = –3 dBFS with 2-dB digital gain

**Figure 46. Spurious-Free Dynamic Range vs AVDD Supply and Temperature**



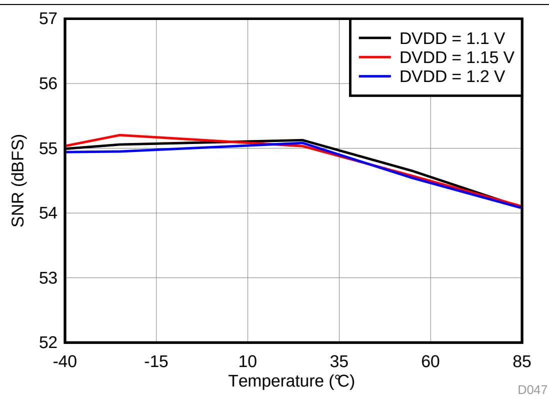

$f_{IN}$ = 1.85 GHz, $A_{IN}$ = –2 dBFS

**Figure 47. Signal-to-Noise Ratio vs DVDD Supply and Temperature**



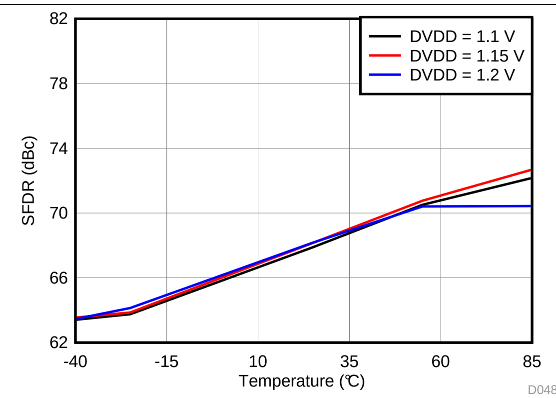

$f_{IN}$ = 1.85 GHz, $A_{IN}$ = –2 dBFS

**Figure 48. Spurious-Free Dynamic Range vs DVDD Supply and Temperature**




$f_{IN}$ = 3.5 GHz, $A_{IN}$ = –3 dBFS with 2-dB digital gain

**Figure 49. Signal-to-Noise Ratio vs DVDD Supply and Temperature**

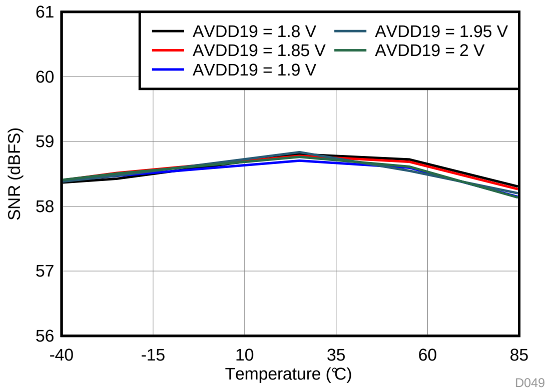



$f_{IN}$ = 3.5 GHz, $A_{IN}$ = –3 dBFS with 2-dB digital gain

**Figure 50. Spurious-Free Dynamic Range vs DVDD Supply and Temperature**

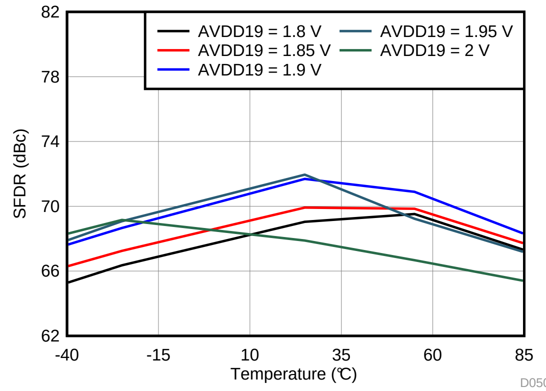
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



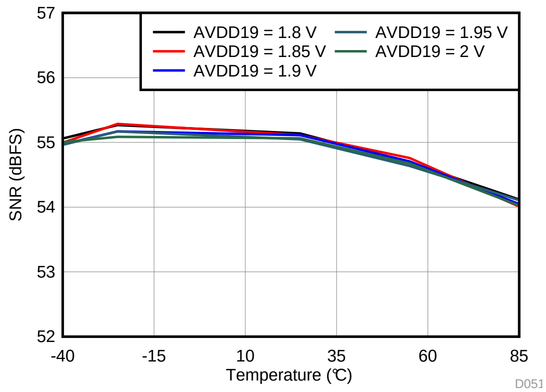

$f_{IN}$ = 1.85 GHz, $A_{IN}$ = –2 dBFS

**Figure 51. Signal-to-Noise Ratio vs AVDD19 Supply and Temperature**



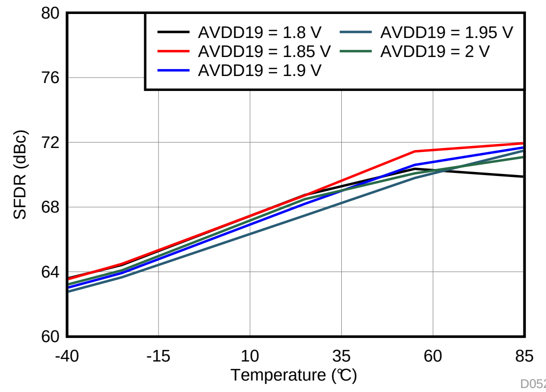

$f_{IN}$ = 1.85 GHz, $A_{IN}$ = –2 dBFS

**Figure 52. Spurious-Free Dynamic Range vs AVDD19 Supply and Temperature**



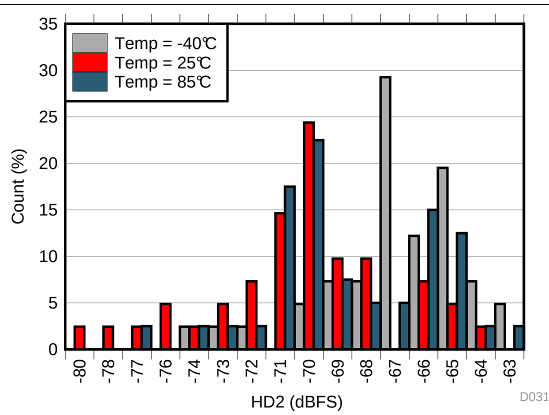

$f_{IN}$ = 3.5 GHz, $A_{IN}$ = –3 dBFS with 2-dB digital gain

**Figure 53. Signal-to-Noise Ratio vs AVDD19 Supply and Temperature**



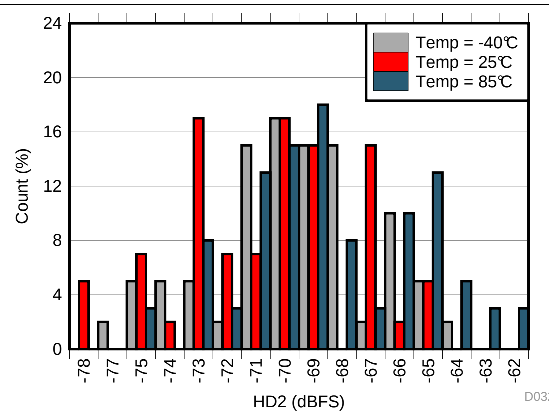

$f_{IN}$ = 3.5 GHz, $A_{IN}$ = –3 dBFS with 2-dB digital gain

**Figure 54. Spurious-Free Dynamic Range vs AVDD19 Supply and Temperature**




$f_{IN}$ = 1.78 GHz, $A_{OUT}$ = –2 dBFS

**Figure 55. HD2 Histogram at AVDD19 = 1.8 V**

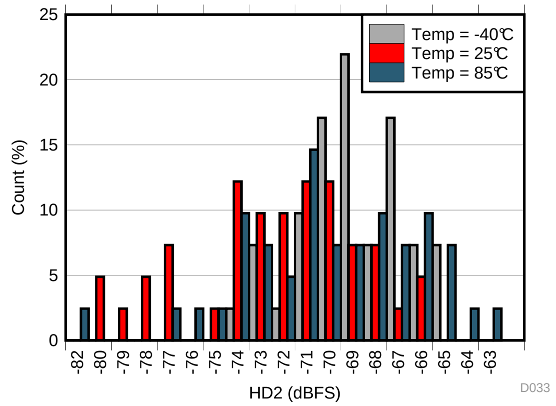



$f_{IN}$ = 1.78 GHz, $A_{OUT}$ = –2 dBFS

**Figure 56. HD2 Histogram at AVDD19 = 1.9 V**

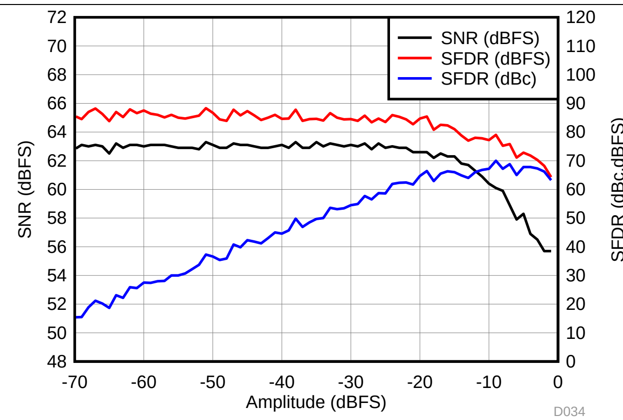
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



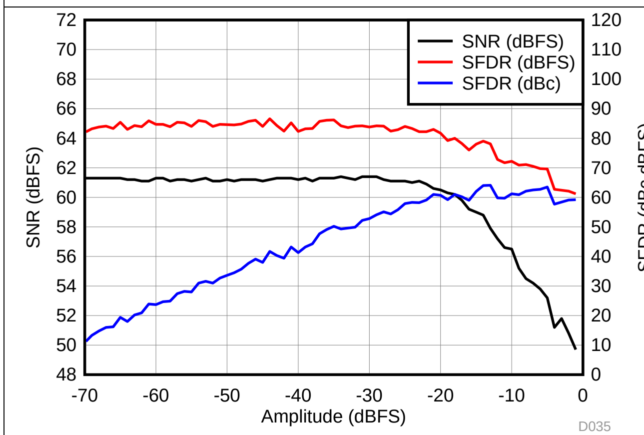

$f_{IN}$ = 1.78 GHz, $A_{OUT}$ = –2 dBFS

**Figure 57. HD2 Histogram at AVDD19 = 2.0 V**



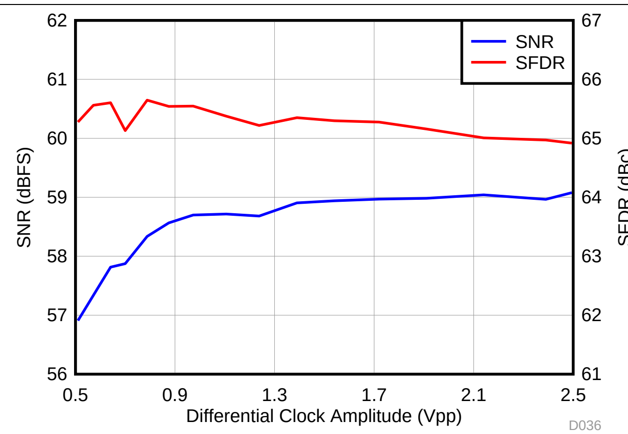

$f_{IN}$ = 1.78 GHz

**Figure 58. Performance vs Amplitude**



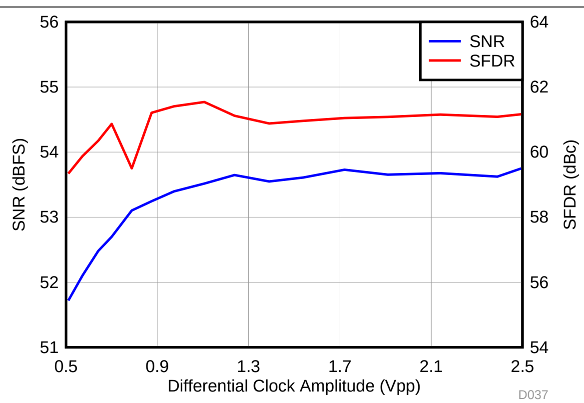

$f_{IN}$ = 3.5 GHz

**Figure 59. Performance vs Amplitude**



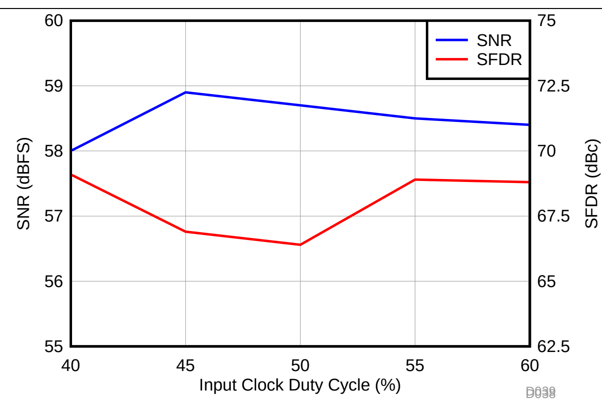

$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS

**Figure 60. Performance vs Clock Amplitude**




$f_{IN}$ = 3.5 GHz, $A_{IN}$ = –3 dBFS

**Figure 61. Performance vs Clock Amplitude**

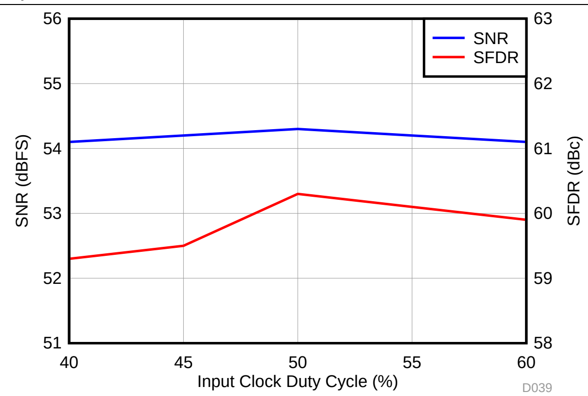



$f_{IN}$ = 1.78 GHz

**Figure 62. Performance vs Clock Duty Cycle**

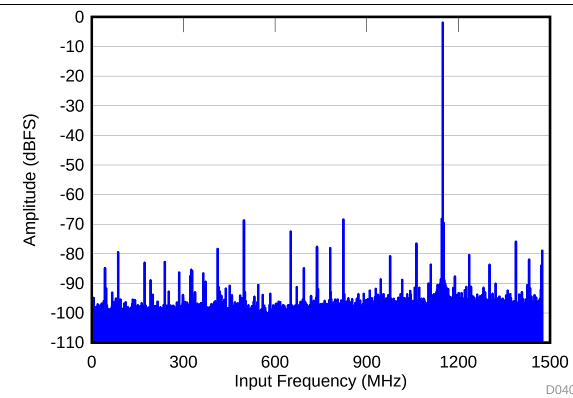
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)




$f_{IN}$ = 3.5 GHz

**Figure 63. Performance vs Clock Duty Cycle**




$f_{IN}$ = 1.8 GHz, $A_{IN}$ = –2 dBFS, PSRR = 37 dB, $f_{PSRR}$ = 3 MHz, $A_{PSRR}$ = 50 $mV_{PP}$, AVDD = 1.9 V

**Figure 64. Power-Supply Rejection Ratio FFT for Test Signal on AVDD Supply**

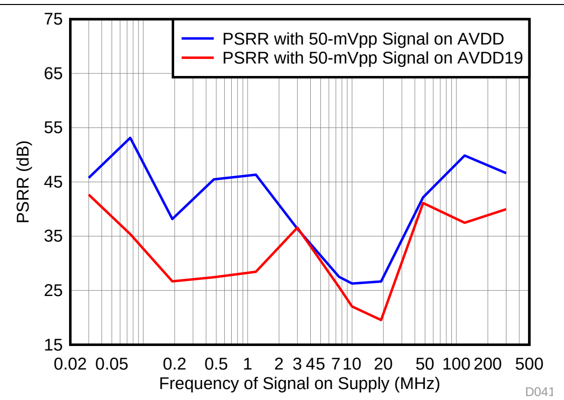
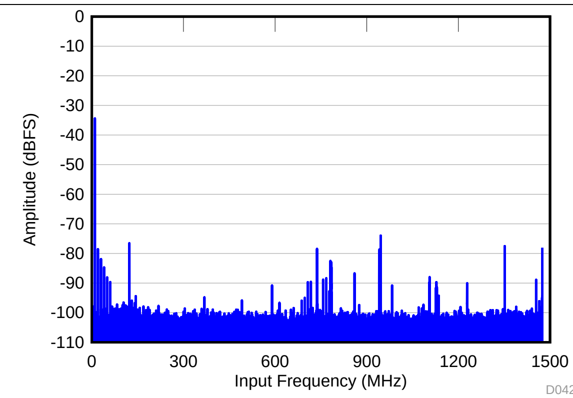



**Figure 65. Power-Supply Rejection Ratio vs Tone Frequency**




$f_{CMRR}$ = 10 MHz, $A_{PSRR}$ = 50 $mV_{PP}$, CMRR = 32 dB

**Figure 66. Common-Mode Rejection Ratio FFT**

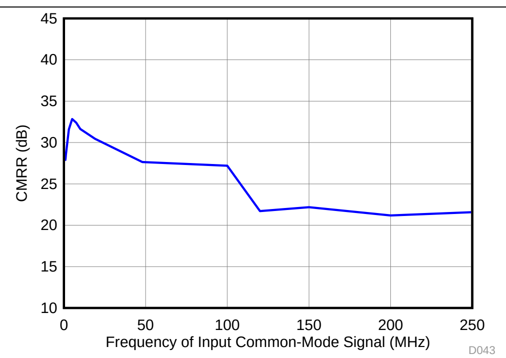
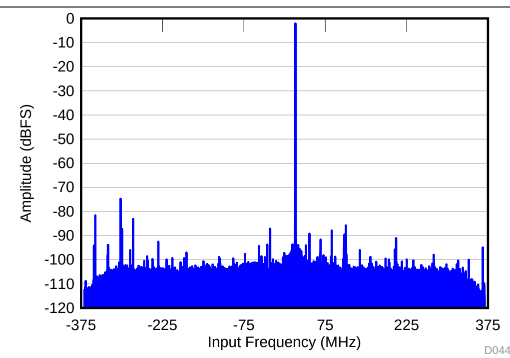



**Figure 67. Common-Mode Rejection Ratio vs Tone Frequency**

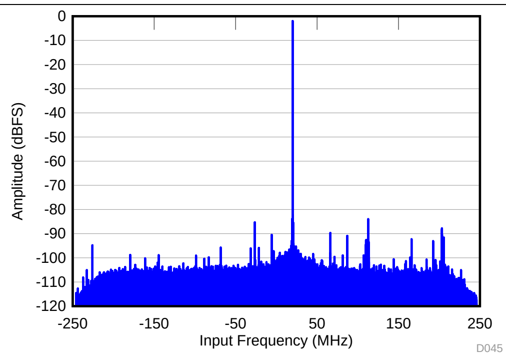



$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 60.6 dBFS, SFDR (includes IL) = 75 dBc

**Figure 68. FFT in 4x Decimation (Complex Output)**

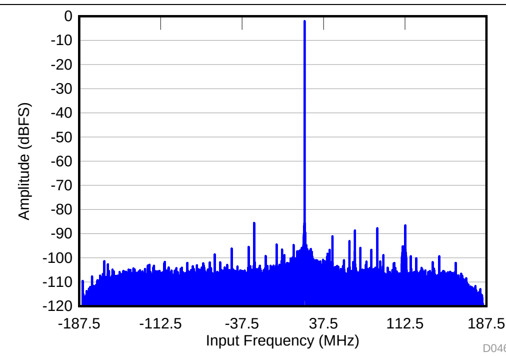
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



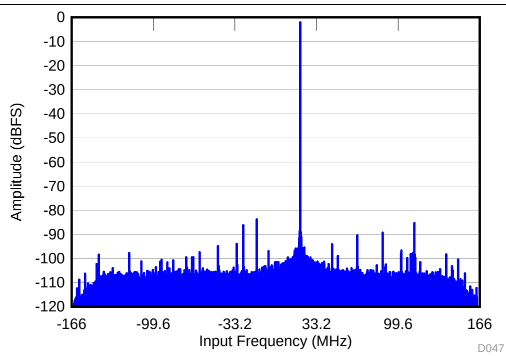

$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 61.6 dBFS, SFDR (includes IL) = 82 dBc

**Figure 69. FFT in 6x Decimation (Complex Output)**



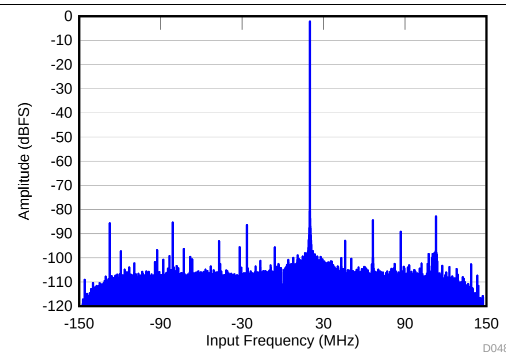

$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 62.6 dBFS, SFDR (includes IL) = 86 dBc

**Figure 70. FFT in 8x Decimation (Complex Output)**



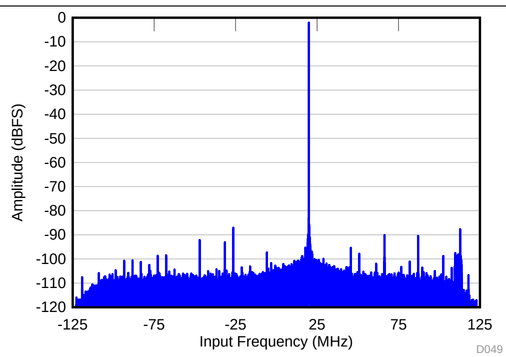

$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 63 dBFS, SFDR (includes IL) = 82 dBc

**Figure 71. FFT in 9x Decimation (Complex Output)**



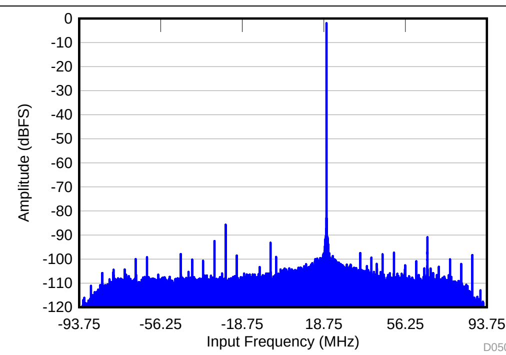

$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 63.3 dBFS, SFDR (includes IL) = 81 dBc

**Figure 72. FFT in 10x Decimation (Complex Output)**




$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 63.7 dBFS, SFDR (includes IL) = 83 dBc

**Figure 73. FFT in 12x Decimation (Complex Output)**

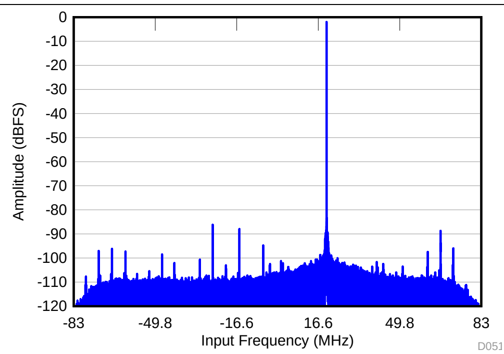



$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 63.9 dBFS, SFDR (includes IL) = 83 dBc

**Figure 74. FFT in 16x Decimation (Complex Output)**

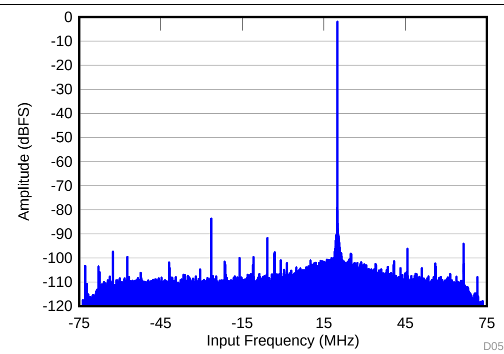
## Typical Characteristics (continued)

typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C; and ADC sampling rate = 2949.12 MSPS, DDC bypassed performance, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –2-dBFS differential input, and 0-dB digital gain (unless otherwise noted)



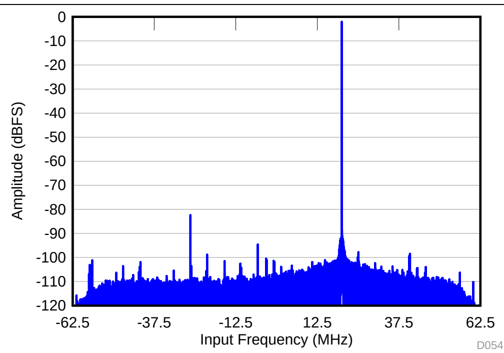

$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 64 dBFS, SFDR (includes IL) = 83 dBc

**Figure 75. FFT in 18x Decimation (Complex Output)**



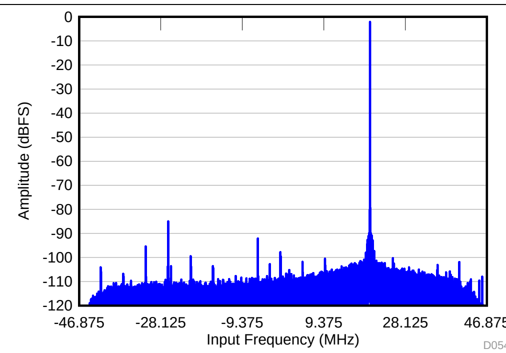

$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 64.4 dBFS, SFDR (includes IL) = 84 dBc

**Figure 76. FFT in 20x Decimation (Complex Output)**




$f_{IN}$ = 1.78 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 64.4 dBFS, SFDR (includes IL) = 82 dBc

**Figure 77. FFT in 24x Decimation (Complex Output)**




$f_{IN}$ = 1.8 GHz, $A_{IN}$ = –2 dBFS, $f_S$ = 2949.12 MSPS, SNR = 64.5 dBFS, SFDR (includes IL) = 79 dBc

**Figure 78. FFT in 32x Decimation (Complex Output)**

# 7 Parameter Measurement Information

## 7.1 Input Clock Diagram

Figure 79 shows the input clock diagram.

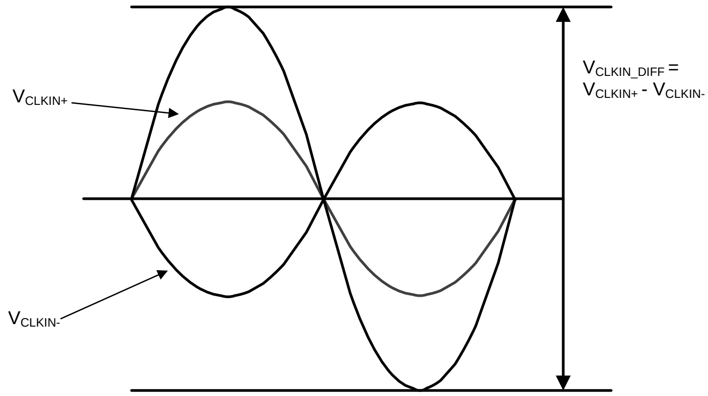



**Figure 79. Input Clock Diagram**

# 8 Detailed Description

## 8.1 Overview

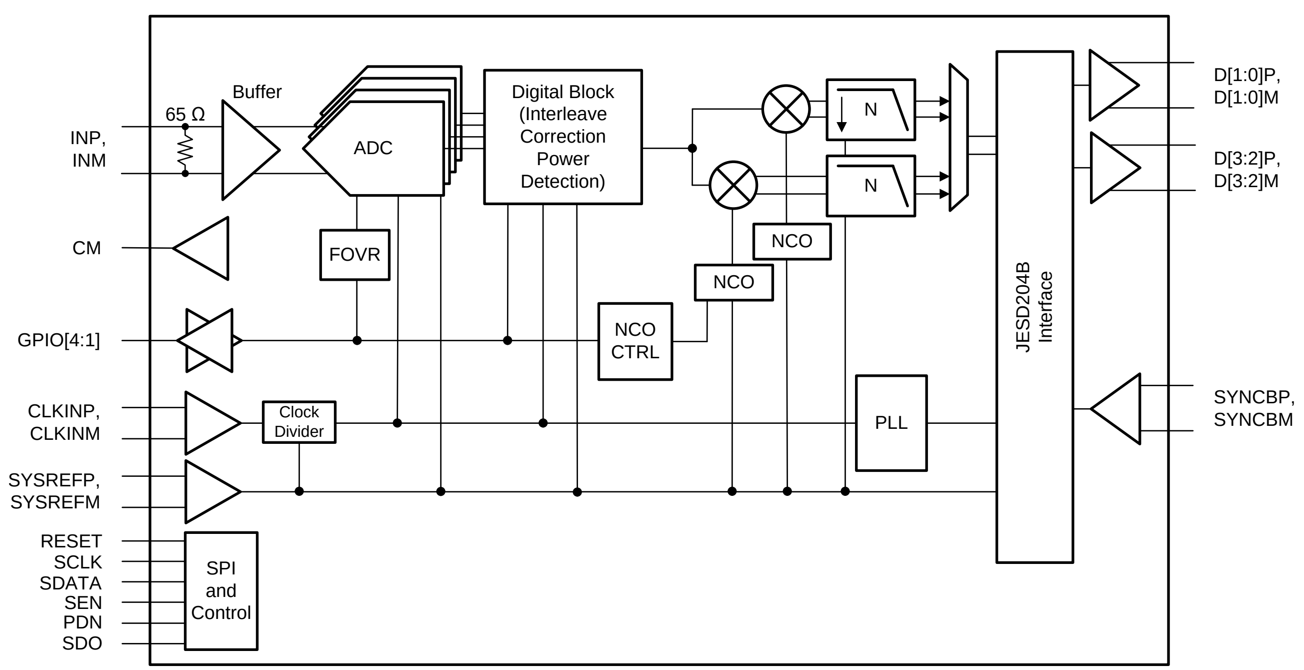
The ADC31RF80 is a single-channel, 14-bit, 2949.12-MSPS, telecom receiver and feedback device containing an analog-to-digital converter (ADC) followed by multi-band digital down-converters (DDCs), and a back-end JESD204B digital interface.

The ADC is preceded by an input buffer and on-chip termination to provide a uniform input impedance over a large input frequency range. Furthermore, an internal differential clamping circuit provides first-level protection against overvoltage conditions. The ADC is internally interleaved four times and equipped with background, analog and digital, and interleaving correction.

The on-chip DDC enables single- or dual-band internal processing to pre-select and filter smaller bands of interest and also reduces the digital output data traffic. Each DDC is equipped with up to three independent, 16-bit numerically-controlled oscillators (NCOs) for phase coherent frequency hopping; the NCOs can be controlled through the SPI or GPIO pins. The ADC31RF80 also provides three different power detectors on-chip with alarm outputs in order to support external automatic gain control (AGC) loops.

The processed data are passed into the JESD204B interface where the data are framed, encoded, serialized, and output on one to four lanes, depending on the ADC sampling rate and decimation. The CLKIN, SYSREF, and SYNCB inputs provide the device clock and the SYSREF and SYNCB signals to the JESD204B interface that are used to derive the internal local frame and local multiframe clocks and establish the serial link. All features of the ADC31RF80 are configurable through the SPI.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Analog Inputs

The ADC31RF80 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. The ADC31RF80 provides on-chip, differential termination to minimize reflections. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit, thus resulting in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to CM using the 32.5-Ω termination resistors that allow for ac-coupling of the input drive network. Figure 80 and Figure 81 show SDD11 at the analog inputs from dc to 5 GHz with a 100-Ω reference impedance.

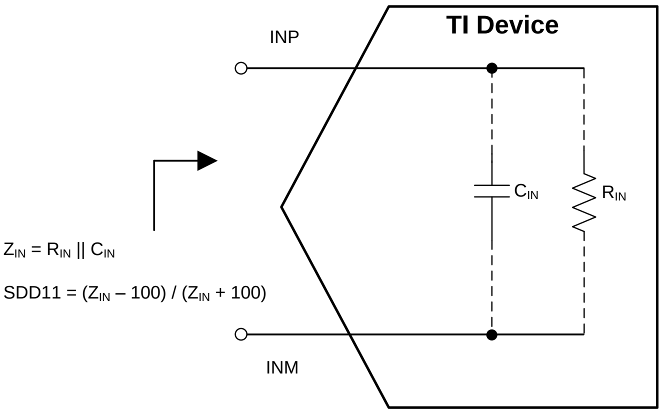





**Figure 80. Equivalent Input Impedance**

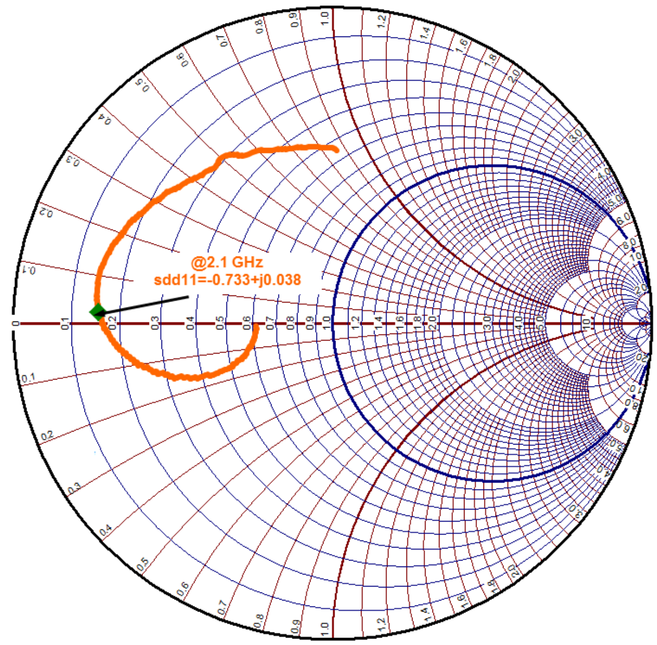



**Figure 81. SDD11 Over the Input Frequency Range**

## Feature Description (continued)

The input impedance of analog inputs can also be modelled as parallel combination of equivalent resistance and capacitance. Figure 82 and Figure 83 show how equivalent impedance ($C_{IN}$ and $R_{IN}$) vary over frequency.

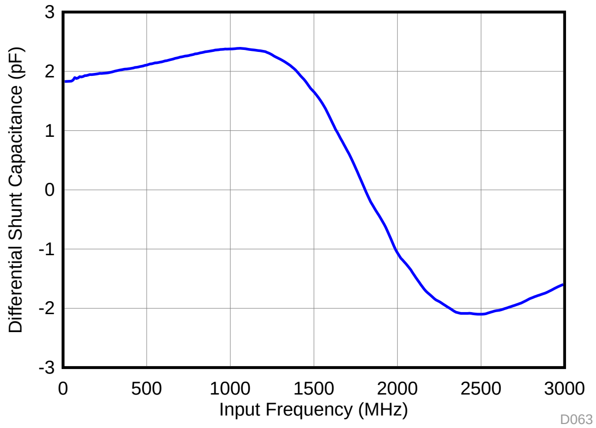



**Figure 82. Differential Input Capacitance vs Input Frequency**

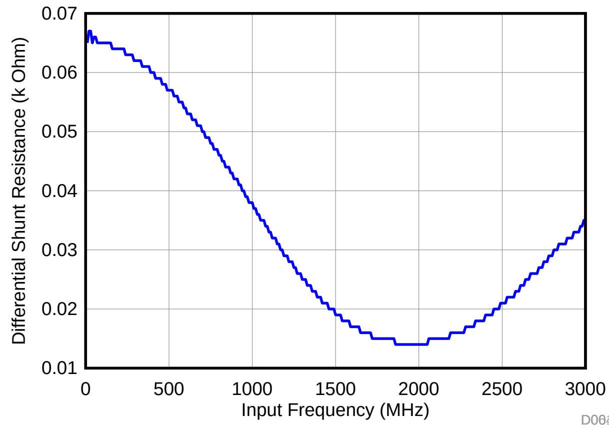



**Figure 83. Differential Input Resistance vs Input Frquency**

Each input pin (INP, INM) must swing symmetrically between (CM + 0.3375 V) and (CM – 0.3375 V), resulting in a 1.35-$V_{PP}$ (default) differential input swing. Figure 84 shows that the input sampling circuit has a 3-dB bandwidth that extends up to approximately 3.2 GHz.

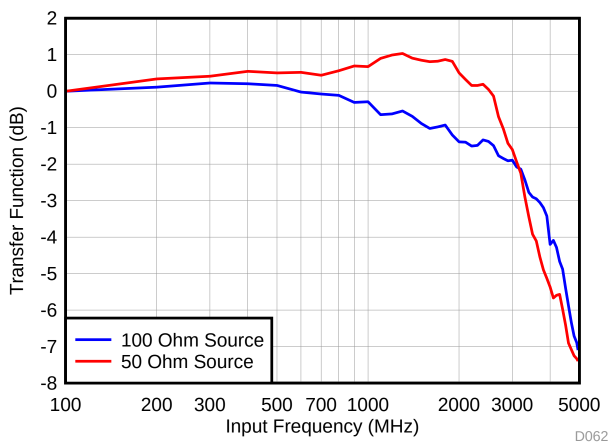



**Figure 84. Input Bandwidth with a 100-Ω Source Resistance**

## Feature Description (continued)

#### *8.3.1.1 Input Clamp Circuit*

The ADC31RF80 analog inputs include an internal, differential clamp for overvoltage protection. The clamp triggers for any input signals at approximately 600 mV above the input common-mode voltage, as shown in Figure 85 and Figure 86, effectively limiting the maximum input signal to approximately 2.4 $V_{PP}$.

When the clamp circuit conducts, the maximum differential current flowing through the circuit (via input pins) must be limited to 20 mA.

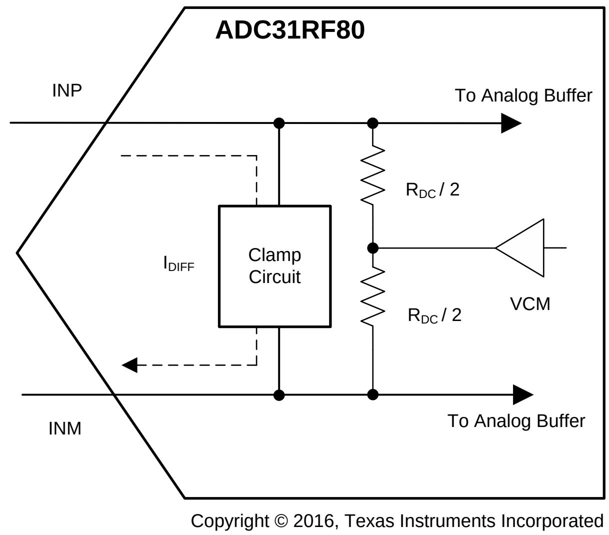



**Figure 85. Clamp Circuit in the ADC31RF80**

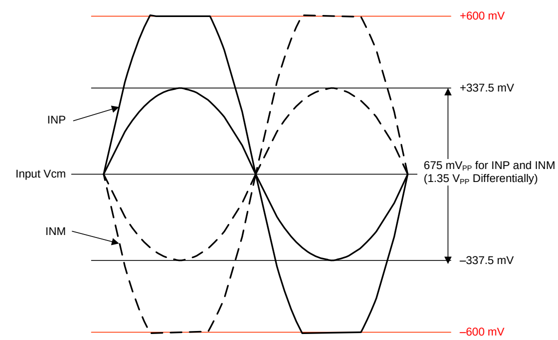



**Figure 86. Clamp Response Timing Diagram**

## Feature Description (continued)

### 8.3.2 Clock Input

The ADC31RF80 sampling clock input includes internal 100-Ω differential termination along with on-chip biasing. The clock input is recommended to be ac-coupled externally. The input bandwidth of the clock input is approximately 3 GHz; Figure 87 shows the clock input impedance with a 100-Ω reference impedance.

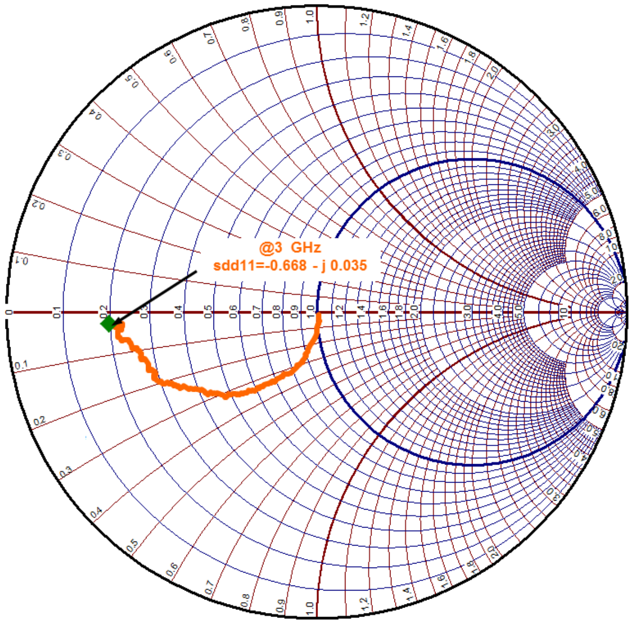



**Figure 87. SDD11 of the Clock Input**

## Feature Description (continued)

The analog-to-digital converter (ADC) aperture jitter is a function of the clock amplitude applied to the pins. Figure 88 shows the equivalent aperture jitter for input frequencies at a 1-GHz and a 2-GHz input. Depending on the clock frequency, a matching circuit can be designed in order to maximize the clock amplitude.

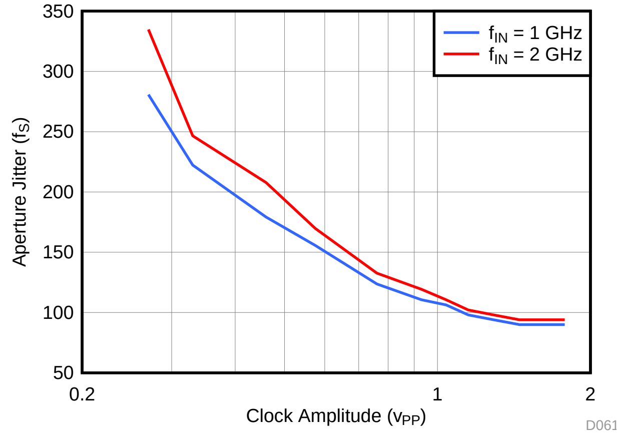



**Figure 88. Equivalent Aperture Jitter vs Input Clock Amplitude**

### 8.3.3 SYSREF Input

The SYSREF signal is a periodic signal that is sampled by the ADC31RF80 device clock and is used to align the boundary of the local multiframe clock inside the data converter. SYSREF is also used to reset critical blocks [such as the clock divider for the interleaved ADCs, numerically-controlled oscillators (NCOs), decimation filters and so forth].

The SYSREF input requires external biasing. Furthermore, SYSREF must be established before the SPI registers are programmed. A programmable delay on the SYSREF input, as shown in Figure 89, is available to help with skew adjustment when the sampling clock and SYSREF are not provided from the same source.

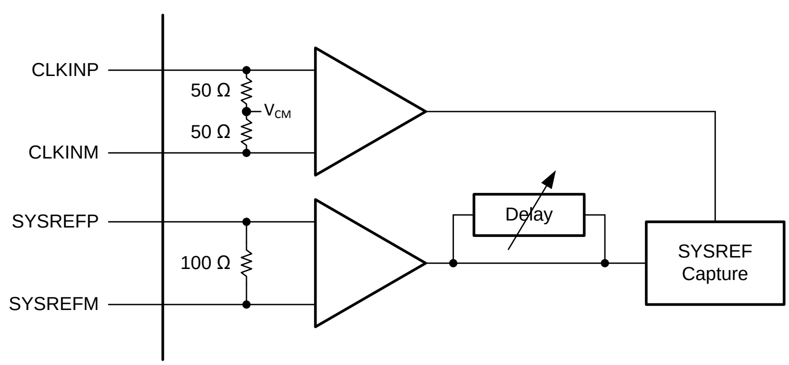



**Figure 89. SYSREF Internal Circuit Diagram**

## Feature Description (continued)

#### 8.3.3.1 Using SYSREF

The ADC31RF80 uses SYSREF information to reset the clock divider, the NCO phase, and the LMFC counter of the JESD interface. The device provides flexibility to provide SYSREF information either from dedicated pins or through SPI register bits. SYSREF is asserted by a low-to-high transition on the SYSREF pins or a 0-to-1 change in the ASSERT SYSREF REG bit, as shown in Figure 90, when using SPI registers.

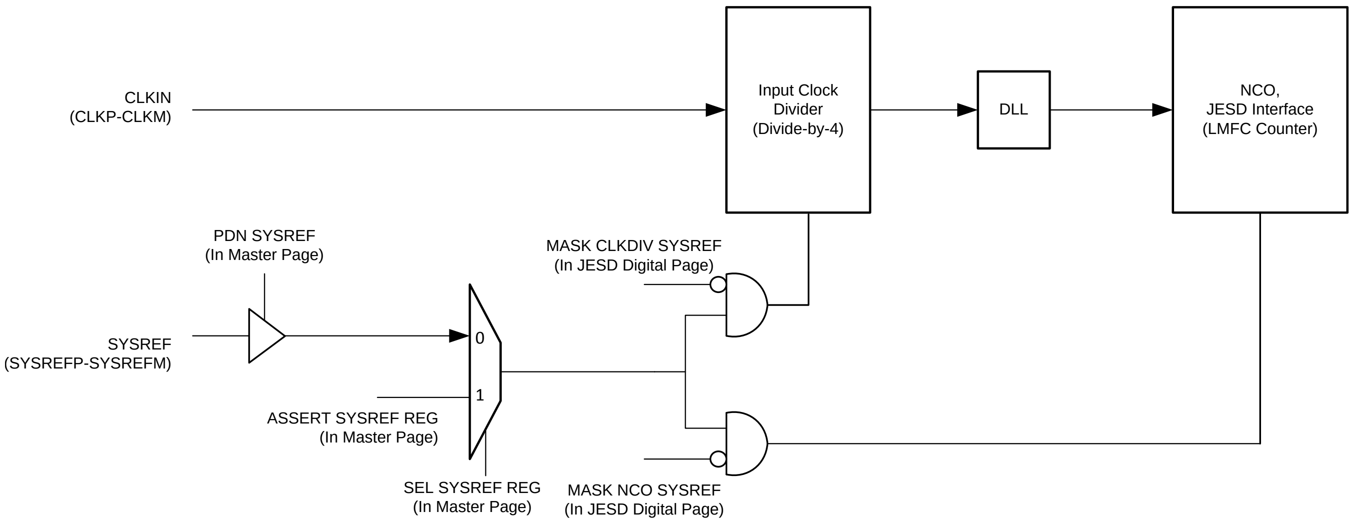



**Figure 90. Using SYSREF to Reset the Clock Divider, the NCO, and the LMFC Counter**

The ADC31RF80 samples the SYSREF signal on the input clock rising edge. Required setup and hold time are listed in the *Timing Requirements* table. The input clock divider gets reset each time that SYSREF is asserted, as shown in Table 1, whereas the NCO phase and the LMFC counter of the JESD interface are reset on each SYSREF assertion after disregarding the first two assertions.

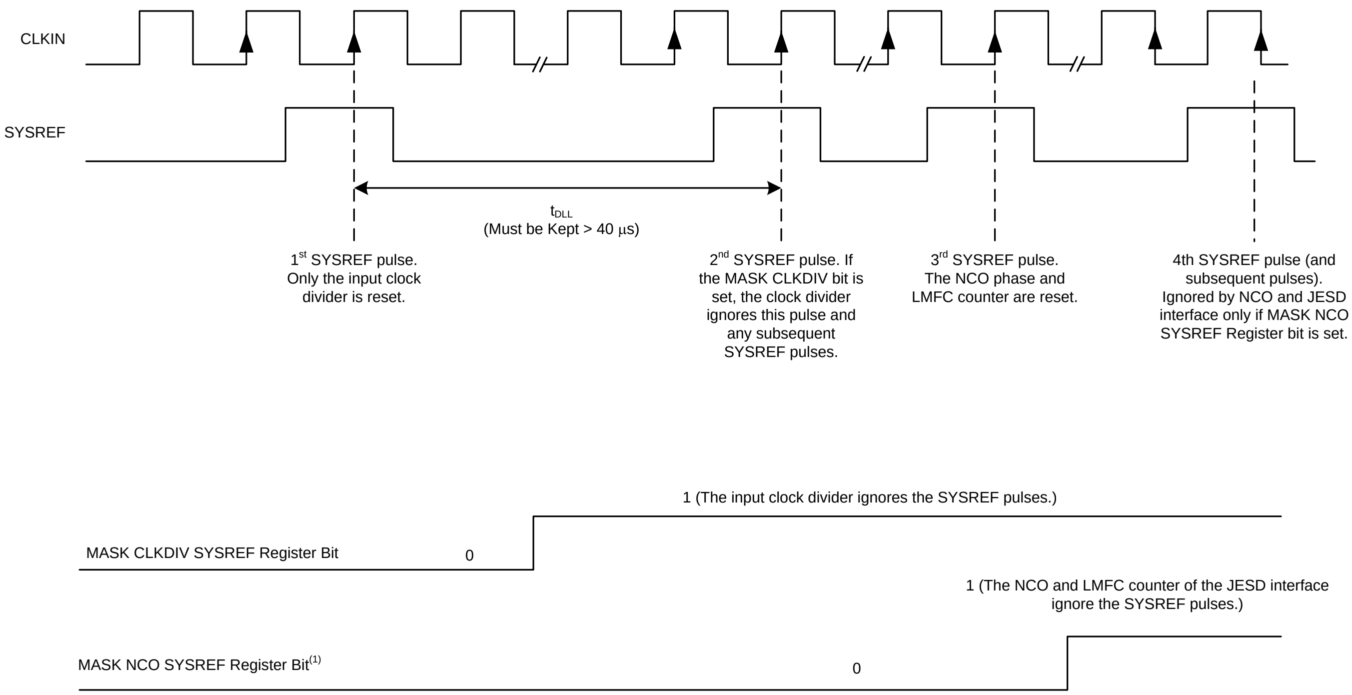
**Table 1. Asserting SYSREF**

| SYSREF ASSERTION INDEX | ACTION | | |
|---|---|---|---|
| | INPUT CLOCK DIVIDER | NCO PHASE | LMFC COUNTER |
| 1 | Gets reset | Does not get reset | Does not get reset |
| 2 | Gets reset | Does not get reset | Does not get reset |
| 3 | Gets reset | Gets reset | Gets reset |
| 4 and onwards | Gets reset | Gets reset | Gets reset |

The SESREF use-cases can be classified broadly into two categories:

1. SYSREF is applied as aperiodic multi-shot pulses.

   Figure 91 shows a case when only a counted number of pulses are applied as SYSREF to the ADC.



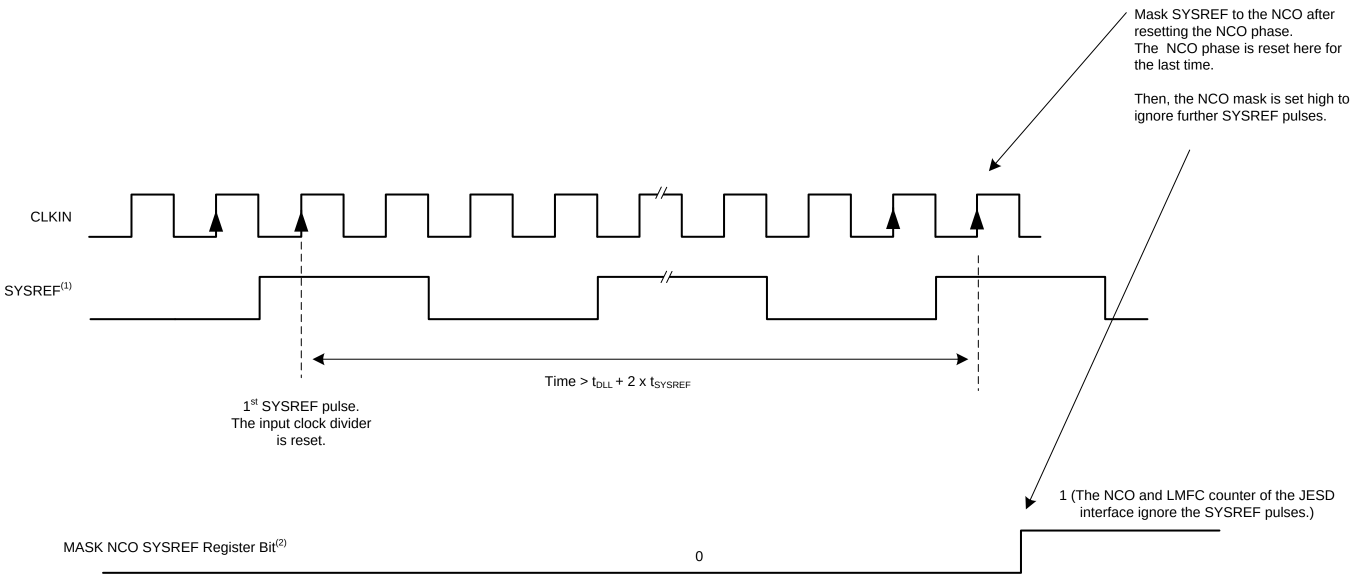

Alternatively, the SYSREF buffer can be powered down with the PDN SYSREF bit.

**Figure 91. SYSREF Used as Aperiodic, Finite Number of Pulses**

After the first SYSREF pulse is applied, allow the DLL in the clock path to settle by waiting for the $t_{DLL}$ time (> 40 µs) before applying the second pulse. During this time, mask the SYSREF going to the input clock divider by setting the MASK CLKDIV SYSREF bit so that the divider output phase remains stable. The NCO phase and LMFC counter are reset on the third SYSREF pulse. After the third SYSREF pulse, the SYSREF going to the NCO and JESD block can be disabled by setting the MASK NCO SYSREF bit to avoid any unwanted resets.

2. SYSREF is applied as a periodic pulse.

   Figure 92 shows how SYSREF can be applied as a continuous periodic waveform.




$t_{SYSREF}$ is a period of the SYSREF waveform.

Alternatively, the SYSREF buffer can be powered down using the PDN SYSREF bit.

**Figure 92. SYSREF Used as a Periodic Waveform**

After applying the SYSREF signal, DLL must be allowed to lock, and the NCO phase and LMFC counter must be allowed to reset by waiting for at least the $t_{DLL}$ (40 µs) + 2 × $t_{SYSREF}$ time. Then, the SYSREF going to the NCO and JESD can be masked by setting the MASK NCO SYSREF register bit.

#### *8.3.3.2 Frequency of the SYSREF Signal*

When SYSREF is a periodic signal, as described in Equation 1, its frequency is required to be a sub-harmonic of the internal local multi-frame clock (LMFC) frequency. The LMFC frequency is determined by the selected decimation, frames per multi-frame setting (K), samples per frame (S), and device input clock frequency.

$$SYSREF = LMFC / N$$

where

- N is an integer value (1, 2, 3, and so forth) (1)

In order for the interleaving correction engine to synchronize properly, the SYSREF frequency must also be a multiple of $f_S$ / 64. Table 2 provides a summary of the valid LMFC clock settings.

**Table 2. . SYSREF and LMFC Clock Frequency**

| OPERATING MODE | LMFS SETTING | LMFC CLOCK FREQUENCY | SYSREF FRQUENCY |
|---|---|---|---|
| Decimation | Various | $f_S$ (1) / (D × S (2) × K (3)) | $f_S$ / (N × LCM (4) (64, D (5) × S × K)) |

(1) $f_S$ = sampling (device) clock frequency.
(2) S = samples per frame.
(3) K = number of frames per multi-frame.
(4) LCM = least-common multiple.
(5) D = decimation ratio.

The SYSREF signal is recommended to be a low-frequency signal less than 5 MHz in order to reduce coupling to the signal path both on the printed circuit board (PCB) as well as internal to the device.

**Example: $f_S$ = 2949.12 MSPS, Divide-by-4 (LMFS = 8411), K = 16**

SYSREF = 2949.12 MSPS / LCM (4 ,64, 16) = 46.08 MHz / N

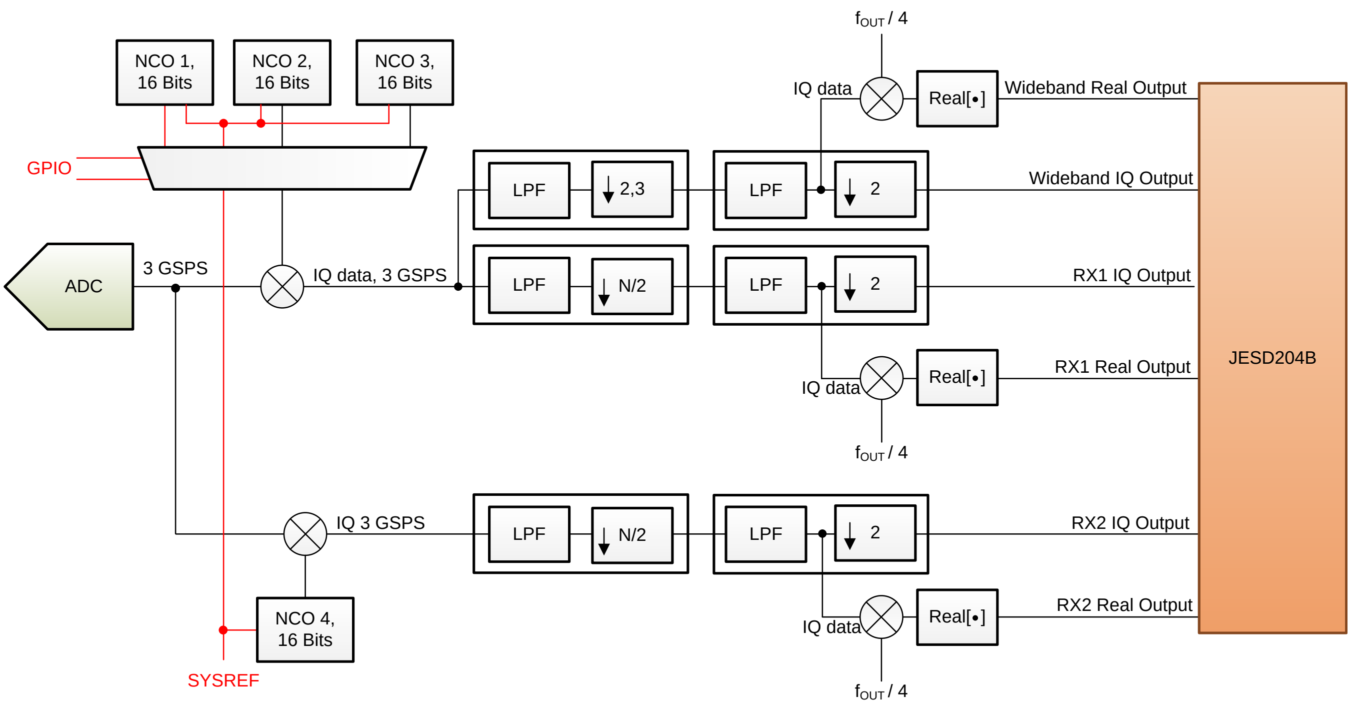
Operate SYSREF at 2.88 MHz (effectively divide-by-1024, N = 16)

For proper device operation, disable the SYSREF signal after the JESD synchronization is established.

### 8.3.4 DDC Block

The ADC31RF80 provides a sophisticated on-chip, digital down converter (DDC) block that can be controlled through SPI register settings and the general-purpose input/output (GPIO) pins. The DDC block supports two basic operating modes: receiver (RX) mode with single- or dual-band DDC and wide-bandwidth observation receiver mode.

Figure 93 shows that the ADC channel is followed by two DDC chains consisting of the digital filter along with a complex digital mixer with a 16-bit numerically-controlled oscillator (NCO). The NCOs allow accurate frequency tuning within the Nyquist zone prior to the digital filtering. One DDC chain is intended for supporting a dual-band DDC configuration in receiver mode and the second DDC chain supports the wide-bandwidth output option for the observation configuration. At any given time, either the single-band DDC, the dual-band DDC, or the wideband DDC can be enabled. Furthermore, three different NCO frequencies can be selected on that path and are quickly switched using the SPI or the GPIO pins to enable wide-bandwidth observation in a multi-band application.



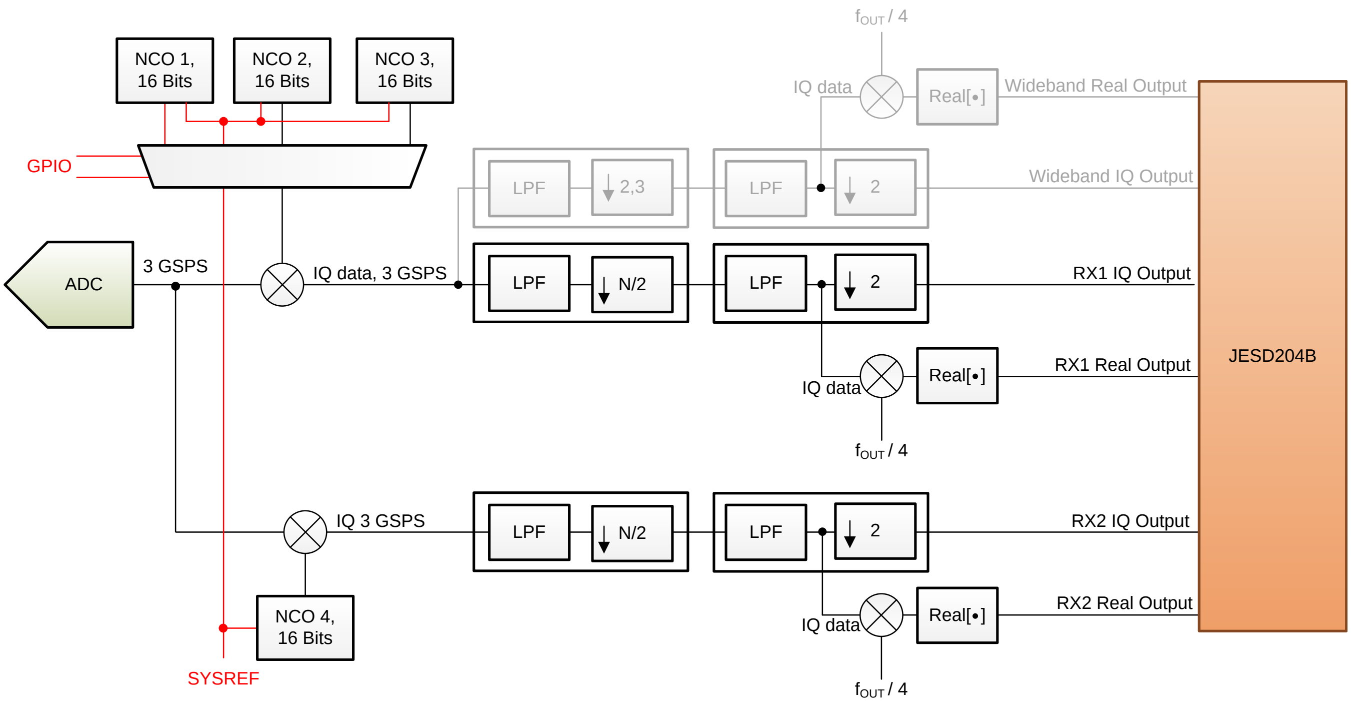

NOTE: Red traces show SYSREF going to the NCO blocks.

**Figure 93. DDC Chains Overview**

Additionally, the decimation filter block provides the option to convert the complex output back to real format at twice the decimated, complex output rate. The filter response with a real output is identical to a complex output. The band is centered in the middle of the Nyquist zone (mixed with $f_{OUT}$ / 4) based on a final output data rate of $f_{OUT}$.

#### 8.3.4.1 Operating Mode: Receiver

Figure 94 shows that the DDC block can be configured to single- or dual-band operation in receiver mode. Both DDC chains use the same decimation filter setting and the available options are discussed in the *Decimation Filters* section. The decimation filter setting also directly affects the interface rate and number of lanes of the JESD204B interface.

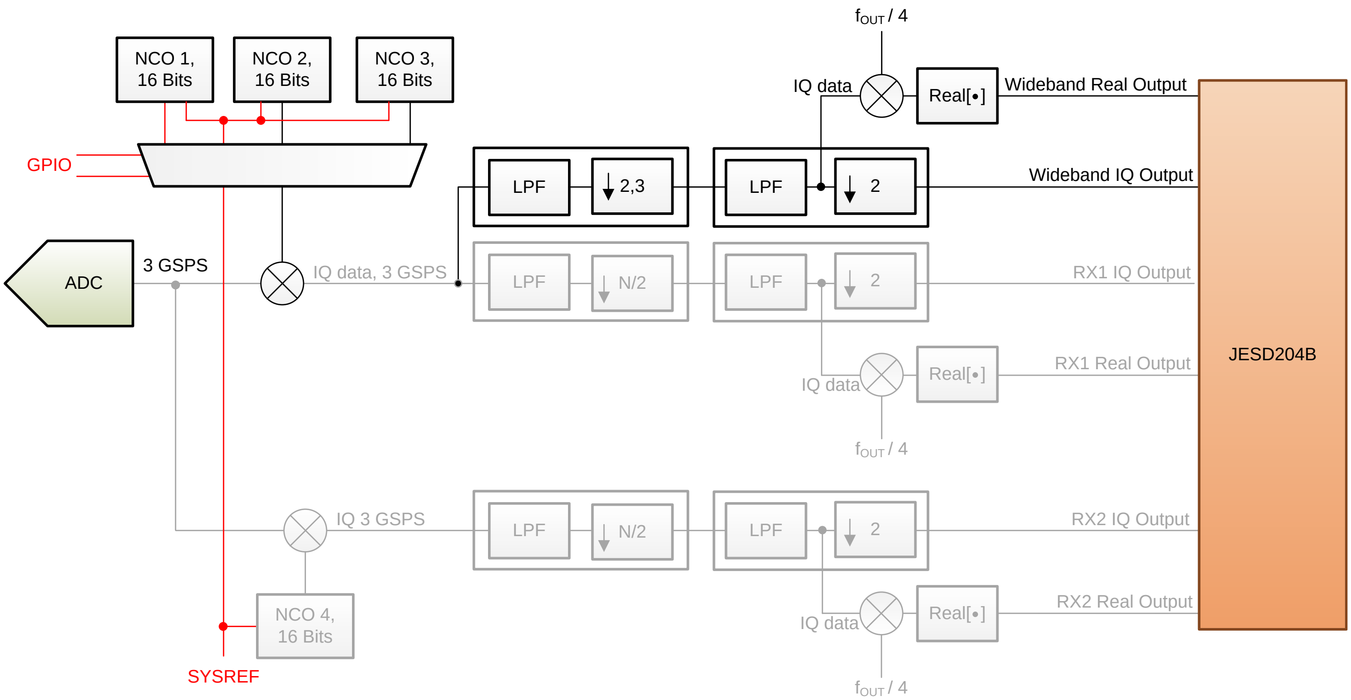



NOTE: Red traces show SYSREF going to the NCO blocks.

**Figure 94. Decimation Filter Option for Single- or Dual-Band Operation**

### 8.3.4.2 Operating Mode: Wide-Bandwidth Observation Receiver

This mode is intended for using a DDC with a wide bandwidth output, but for multiple bands. As shown in Figure 95, this mode uses a single DDC chain where up to three NCOs can be used to perform wide-bandwidth observation in a multi-band environment. The three NCOs can be switched dynamically using either the GPIO pins or an SPI command. All three NCOs operate continuously to ensure phase continuity; however, when the NCO is switched, the output data are invalid until the decimation filters are completely flushed with data from the new band.




NOTE: Red traces show SYSREF going to the NCO blocks.

**Figure 95. Decimation Filter Implementation for Single-Band and Wide-Bandwidth Mode**

#### 8.3.4.3 Decimation Filters

The stop-band rejection of the decimation filters is approximately 90 dB with a pass-band bandwidth of approximately 80%. Table 3 gives an overview of the pass-band bandwidth depending on decimation filter setting and ADC sampling rate.

**Table 3. Decimation Filter Summary and Maximum Available Output Bandwidth**

| DECIMATION SETTING | NO. OF DDCS | NOMINAL PASSBAND GAIN | BANDWIDTH | | ADC SAMPLE RATE = N MSPS | | ADC SAMPLE RATE = 3 GSPS | |
|---|---|---|---|---|---|---|---|---|
| | | | 3 dB (%) | 1 dB (%) | OUTPUT RATE (MSPS) PER BAND | OUTPUT BANDWIDTH (MHz) PER BAND | COMPLEX OUTPUT RATE (MSPS) PER BAND | OUTPUT BANDWIDTH (MHz) PER BAND |
| Divide-by-4 complex | 1 | –0.4 dB | 90.9 | 86.8 | N / 4 complex | 0.4 × N / 2 | 750 | 600 |
| Divide-by-6 complex | 1 | –0.65 dB | 90.6 | 86.1 | N / 6 complex | 0.4 × N / 3 | 500 | 400 |
| Divide-by-8 complex | 2 | –0.27 dB | 91.0 | 86.8 | N / 8 complex | 0.4 × N / 4 | 375 | 300 |
| Divide-by-9 complex | 2 | –0.45 dB | 90.7 | 86.3 | N / 9 complex | 0.4 × N / 4.5 | 333.3 | 266.6 |
| Divide-by-10 complex | 2 | –0.58 dB | 90.7 | 86.3 | N / 10 complex | 0.4 × N / 5 | 300 | 240 |
| Divide-by-12 complex | 2 | –0.55 dB | 90.7 | 86.4 | N / 12 complex | 0.4 × N / 6 | 250 | 200 |
| Divide-by-16 complex | 2 | –0.42 dB | 90.8 | 86.4 | N / 16 complex | 0.4 × N / 8 | 187.5 | 150 |
| Divide-by-18 complex | 2 | –0.83 dB | 91.2 | 87.0 | N / 18 complex | 0.4 × N / 9 | 166.6 | 133 |
| Divide-by-20 complex | 2 | –0.91 dB | 91.2 | 87.0 | N / 20 complex | 0.4 × N / 10 | 150 | 120 |
| Divide-by-24 complex | 2 | –0.95 db | 91.1 | 86.9 | N / 24 complex | 0.4 × N / 12 | 125 | 100 |
| Divide-by-32 complex | 2 | –0.78 dB | 91.1 | 86.8 | N / 32 complex | 0.4 × N / 16 | 93.75 | 75 |

Figure 96 shows a dual-band example with a divide-by-8 complex.

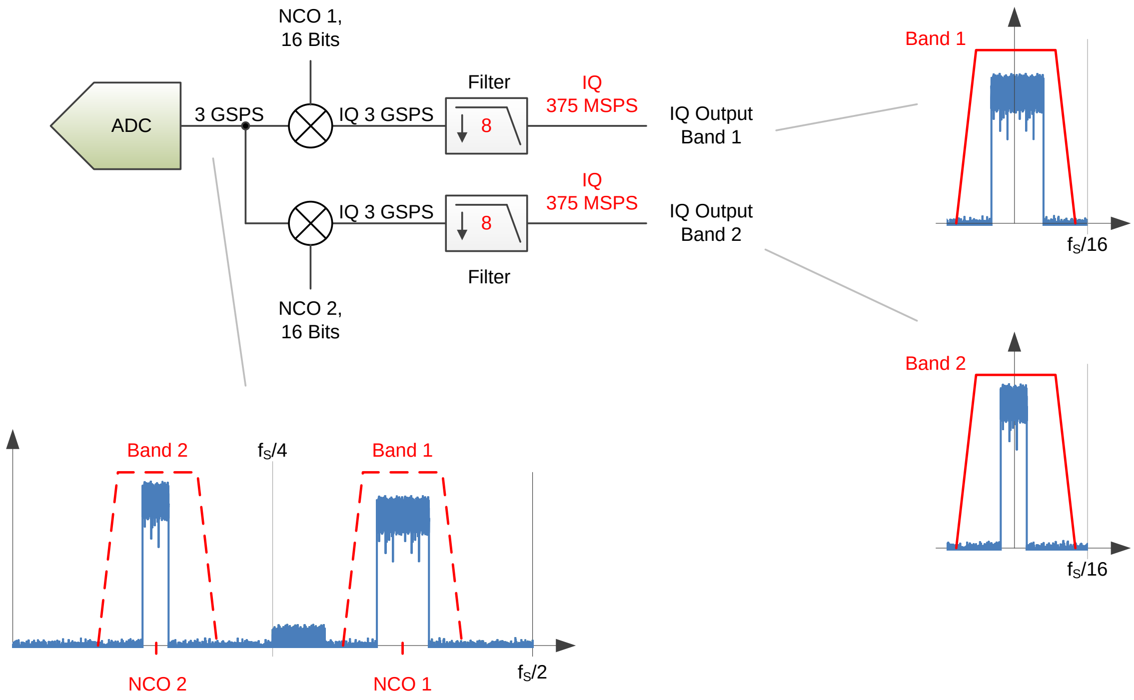



**Figure 96. Dual-Band Example**

The decimation filter responses normalized to the ADC sampling clock are illustrated in Figure 96 to Figure 119 and can be interpreted as follows:

Figure 97 shows that each figure contains the filter pass-band, transition bands, and alias bands. The x-axis in Figure 97 shows the offset frequency (after the NCO frequency shift) normalized to the ADC sampling clock frequency.

For example, in the divide-by-4 complex, the output data rate is an $f_S$ / 4 complex with a Nyquist zone of $f_S$ / 8 or 0.125 × $f_S$. The transition band is centered around 0.125 × $f_S$ and the alias transition band is centered at 0.375 × $f_S$. The alias bands that alias on top of the wanted signal band are centered at 0.25 × $f_S$ and 0.5 × $f_S$ (and are colored in red).

The decimation filters of the ADC31RF80 provide greater than 90-dB attenuation for the alias bands.

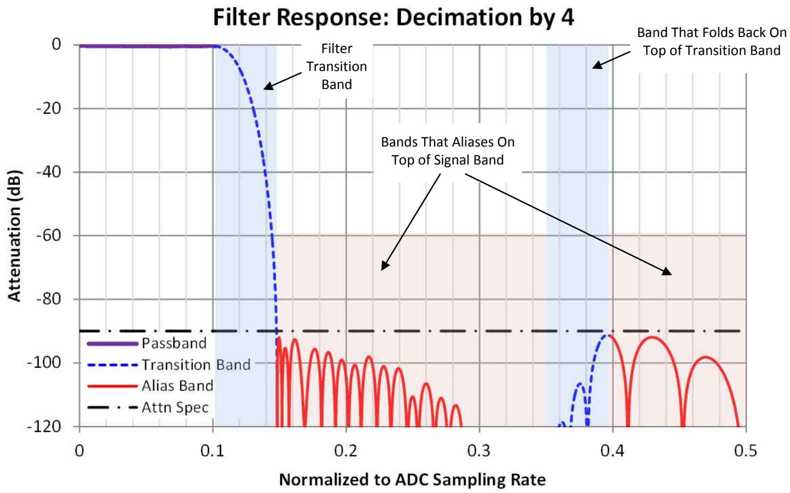



**Figure 97. Interpretation of the Decimation Filter Plots**

#### 8.3.4.3.1 Divide-by-4

Peak-to-peak pass-band ripple: approximately 0.22 dB

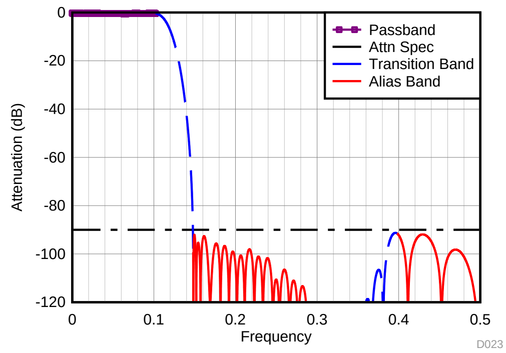



Figure 98. Divide-by-4 Filter Response

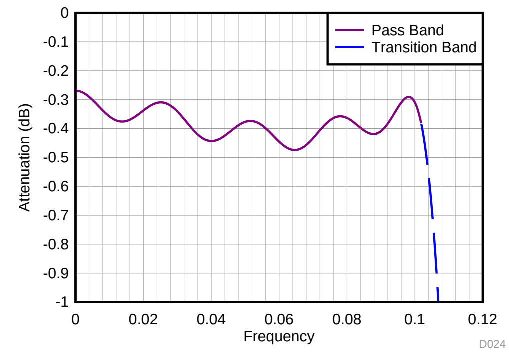



Figure 99. Divide-by-4 Filter Response (Zoomed)

#### 8.3.4.3.2 Divide-by-6

Peak-to-peak pass-band ripple: approximately 0.38 dB

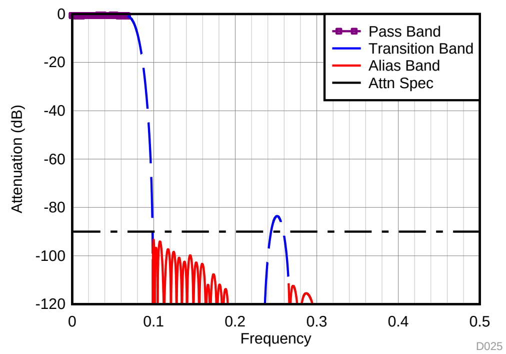



Figure 100. Divide-by-6 Filter Response

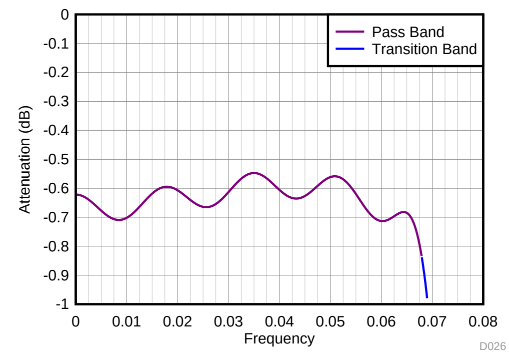



Figure 101. Divide-by-6 Filter Response (Zoomed)

#### 8.3.4.3.3 Divide-by-8

Peak-to-peak pass-band ripple: approximately 0.25 dB

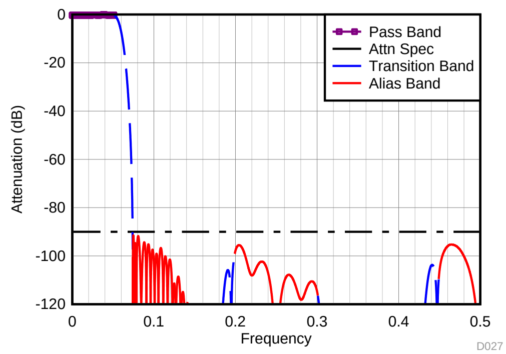



Figure 102. Divide-by-8 Filter Response

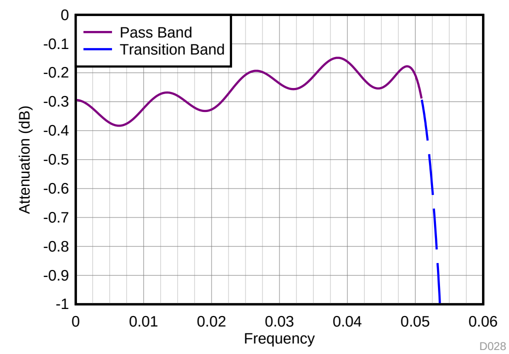



Figure 103. Divide-by-8 Filter Response (Zoomed)

#### 8.3.4.3.4 Divide-by-9

Peak-to-peak pass-band ripple: approximately 0.39 dB

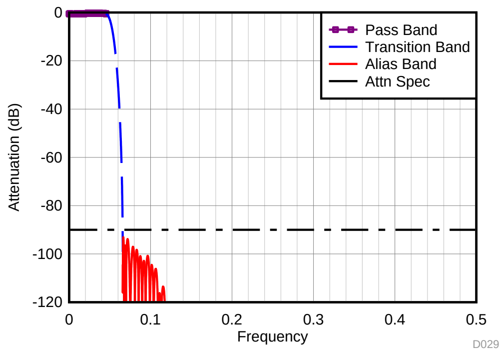



**Figure 104. Divide-by-9 Filter Response**

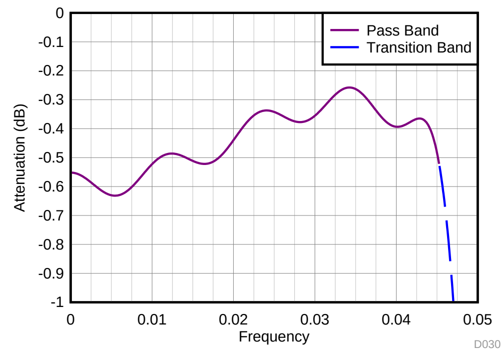



**Figure 105. Divide-by-9 Filter Response (Zoomed)**

#### 8.3.4.3.5 Divide-by-10

Peak-to-peak pass-band ripple: approximately 0.39 dB

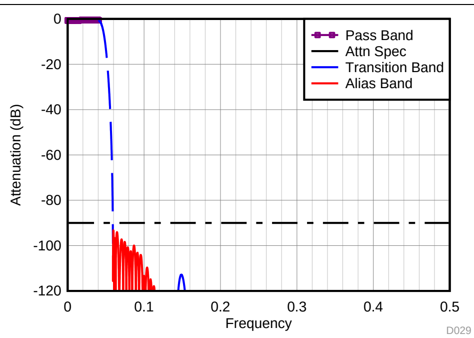



**Figure 106. Divide-by-10 Filter Response**

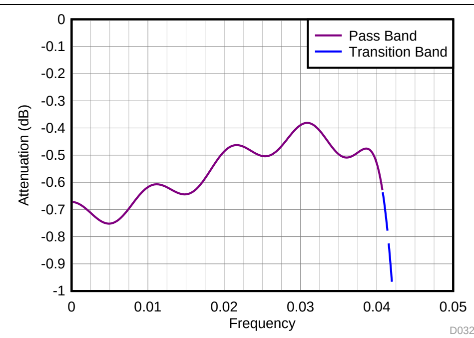



**Figure 107. Divide-by-10 Filter Response (Zoomed)**

#### 8.3.4.3.6 Divide-by-12

Peak-to-peak pass-band ripple: approximately 0.36 dB

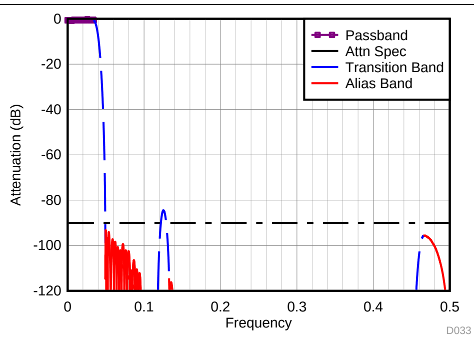



**Figure 108. Divide-by-12 Filter Response**

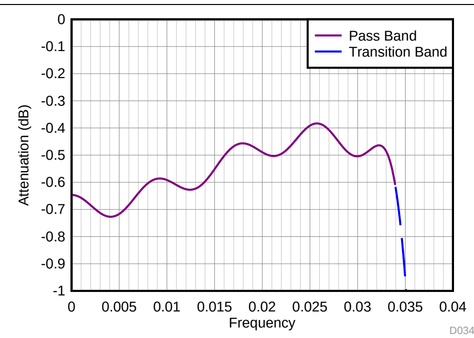



**Figure 109. Divide-by-12 Filter Response (Zoomed)**

#### 8.3.4.3.7 Divide-by-16

Peak-to-peak pass-band ripple: approximately 0.29 dB

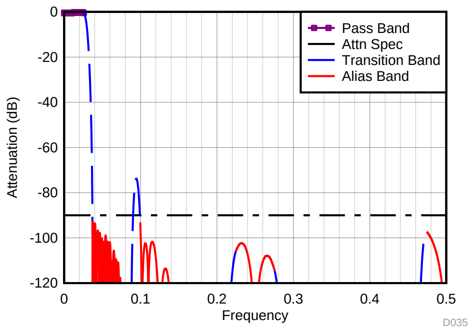



**Figure 110. Divide-by-16 Filter Response**

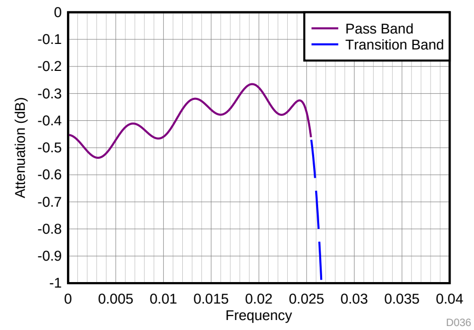



**Figure 111. Divide-by-16 Filter Response (Zoomed)**

#### 8.3.4.3.8 Divide-by-18

Peak-to-peak pass-band ripple: approximately 0.33 dB

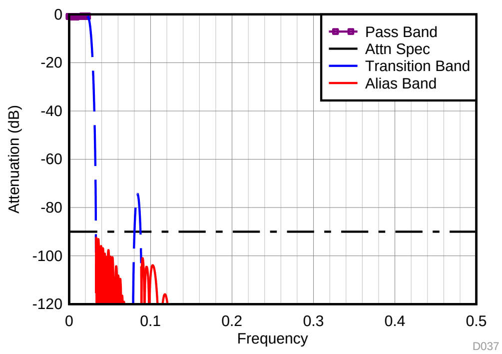



**Figure 112. Divide-by-18 Filter Response**

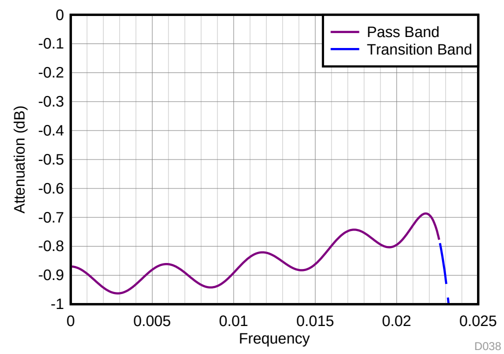



**Figure 113. Divide-by-18 Filter Response (Zoomed)**

#### 8.3.4.3.9 Divide-by-20

Peak-to-peak pass-band ripple: approximately 0.32 dB

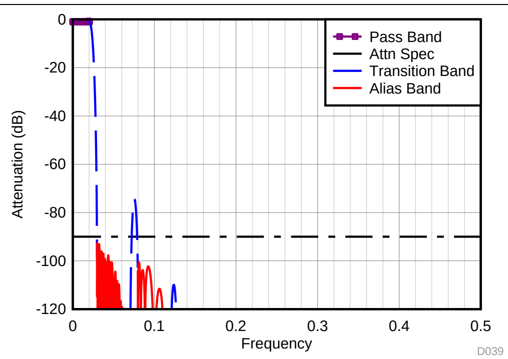



**Figure 114. Divide-by-20 Filter Response**

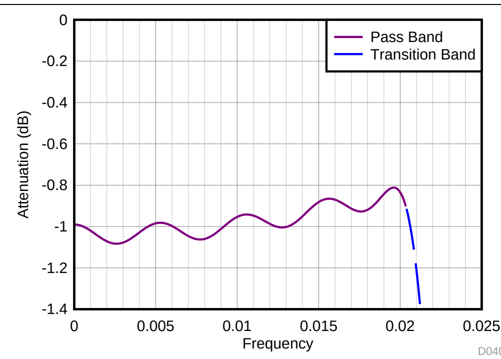



**Figure 115. Divide-by-20 Filter Response (Zoomed)**

#### 8.3.4.3.10 Divide-by-24

Peak-to-peak pass-band ripple: approximately 0.30 dB

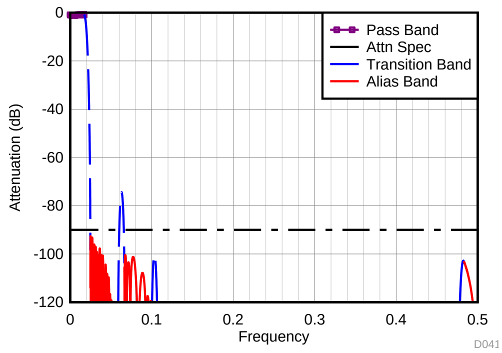



**Figure 116. Divide-by-24 Filter Response**

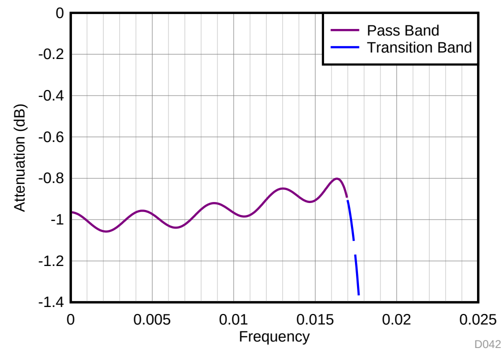



**Figure 117. Divide-by-24 Filter Response (Zoomed)**

#### 8.3.4.3.11 Divide-by-32

Peak-to-peak pass-band ripple: approximately 0.24 dB

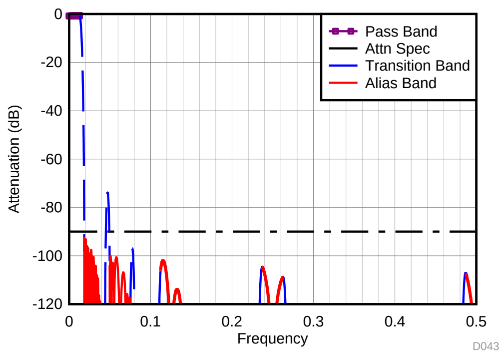



**Figure 118. Divide-by-32 Filter Response**

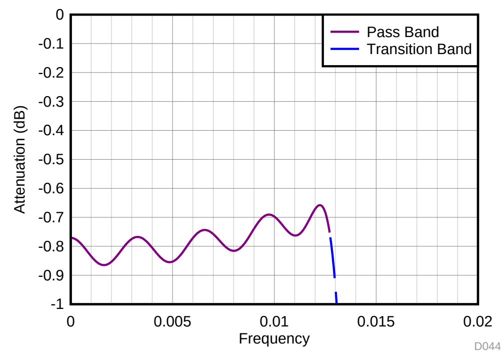



**Figure 119. Divide-by-32 Filter Response (Zoomed)**

#### 8.3.4.3.12 Latency With Decimation Options

Table 4 describes device latency for different DDC options. At higher decimation options, latency increases because of the increase in number of taps in the decimation filter.

**Table 4. Latency With Different Decimation Options**

| DECIMATION OPTION | TOTAL LATENCY, DEVICE CLOCK CYCLES |
|---|---|
| Divide-by-4 | 516 |
| Divide-by-6 | 746 |
| Divide-by-8 | 621 |
| Divide-by-9 | 763.5 |
| Divide-by-10 | 811 |
| Divide-by-12 | 897 |
| Divide-by-16 | 1045 |
| Divide-by-18 | 1164 |
| Divide-by-20 | 1256 |
| Divide-by-24 | 1443 |
| Divide-by-32 | 1773 |

### *8.3.4.4 Numerically-Controlled Oscillators (NCOs) and Mixers*

The ADC31RF80 is equipped with three independent, complex NCOs. Equation 2 shows how the oscillator generates a complex exponential sequence.

$$x[n] = e^{-j\omega n}$$

where

- frequency ($\omega$) is specified as a signed number by the 16-bit register setting (2)

The complex exponential sequence is multiplied by the real input from the ADC to mix the desired carrier down to 0 Hz.

The ADC has two DDCs. The first DDC has three NCOs and the second DDC has one NCO. The first DDC can dynamically select one of the three NCOs based on the GPIO pin or SPI selection. In wide-bandwidth mode (lower decimation factors, for example, 4 and 6), there can only be one active DDC. The NCO frequencies can be programmed independently through the DDCx, NCO[4:1], and the MSB and LSB register settings.

Equation 3 gives the NCO frequency setting that is set by the 16-bit register:

$$f_{NCO} = \frac{DDCxNCOy \times f_S}{2^{16}}$$

where

- x = 0, 1
- y = 1 to 4 (3)

For example:

If $f_S$ = 2949.12 MSPS, then the NCO register setting = 38230 (decimal).

Thus, Equation 4 defines $f_{NCO}$:

$$f_{NCO} = 38230 \times \frac{2949.12\ \text{MSPS}}{2^{16}} = 1720.35\ \text{MHz} \quad (4)$$

Any register setting changes that occur after the JESD204B interface is operational results in a non-deterministic NCO phase. If a deterministic phase is required, the JESD204B interface must be reinitialized after changing the register setting.

### 8.3.5 NCO Switching

The first DDC (DDC0) provides three different NCOs that can be used for phase-coherent frequency hopping. This feature is available in both single-band and dual-band mode, but only affects DDC0.

The NCOs can be switched by using the GPIO pins with the register configurations shown in Table 5 or through an SPI control. The assignment of which GPIO pin to use for INSEL0 and INSEL1 is done based on Table 6, using register 5438h. The NCO selection, shown in Table 7 and Figure 120, is done based on the logic selection on the GPIO pins.

**Table 5. NCO Register Configurations**

| REGISTER | ADDRESS | DESCRIPTION |
|---|---|---|
| **NCO CONTROL THROUGH GPIO PINS** | | |
| NCO SEL PIN | 500Fh | Selects the NCO control through the SPI (default) or a GPIO pin. |
| INSEL0[1:0], INSEL1[1:0] | 5438h | Selects which two GPIO pins are used to control the NCO. |
| **NCO CONTROL THROUGH SPI CONTROL** | | |
| NCO SEL PIN | 500Fh | Selects the NCO control through the SPI (default) or a GPIO pin. |
| NCO SEL[1:0] | 5010h | Selects which NCO to use for DDC0. |

**Table 6. GPIO Pin Assignment**

| INSELx[1:0] (Where x = 0 or 1) | GPIO PIN SELECTED |
|---|---|
| 00 | GPIO4 |
| 01 | GPIO1 |
| 10 | GPIO3 |
| 11 | GPIO2 |

**Table 7. NCO Selection**

| NCO SEL[1:0] | NCO SELECTED |
|---|---|
| 00 | NCO1 |
| 01 | NCO2 |
| 10 | NCO3 |
| 11 | n/a |

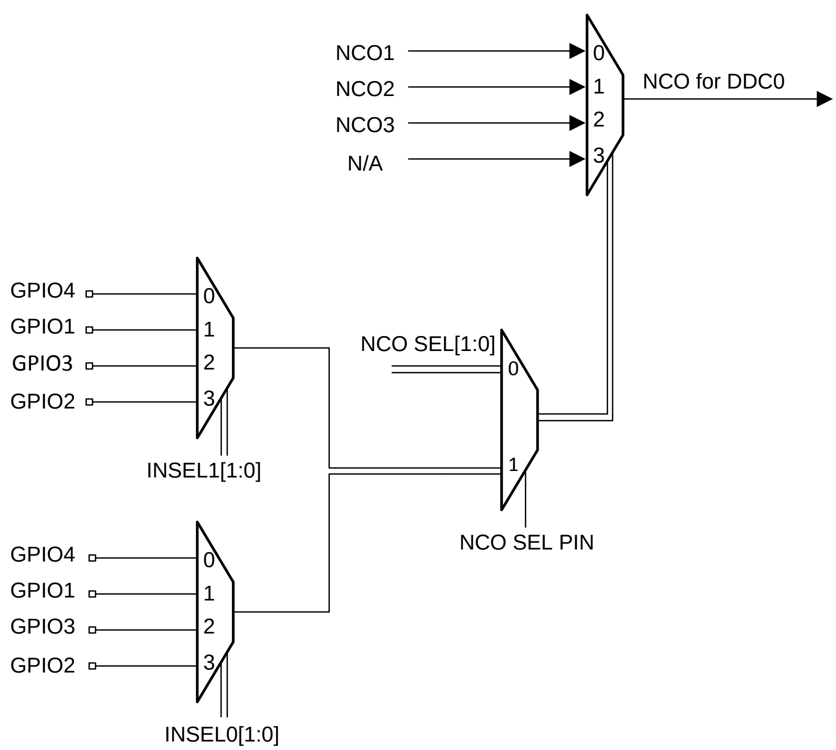



**Figure 120. NCO Switching from GPIO and SPI**

### 8.3.6 SerDes Transmitter Interface

Each 12.3-Gbps serializer, deserializer (SerDes) LVDS transmitter output requires ac-coupling between the transmitter and receiver. Terminate the differential pair, as shown in Figure 121, with 100-Ω resistance (that is, two 50-Ω resistors) as close to the receiving device as possible to avoid unwanted reflections and signal degradation.

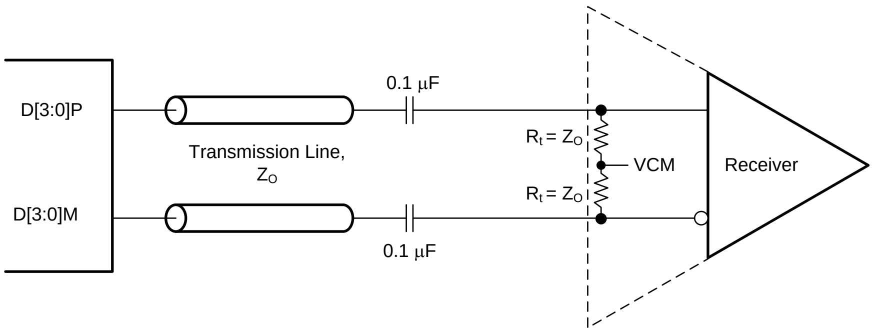



**Figure 121. External Serial JESD204B Interface Connection**

### 8.3.7 Eye Diagrams

Figure 122 and Figure 123 show the serial output eye diagrams of the ADC31RF80 at 5.0 Gbps and 12 Gbps against the JESD204B mask.

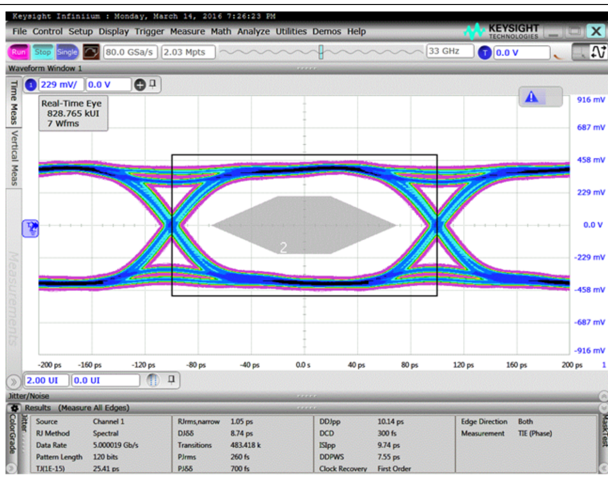


**Figure 122. Data Eye at 5 Gbps**

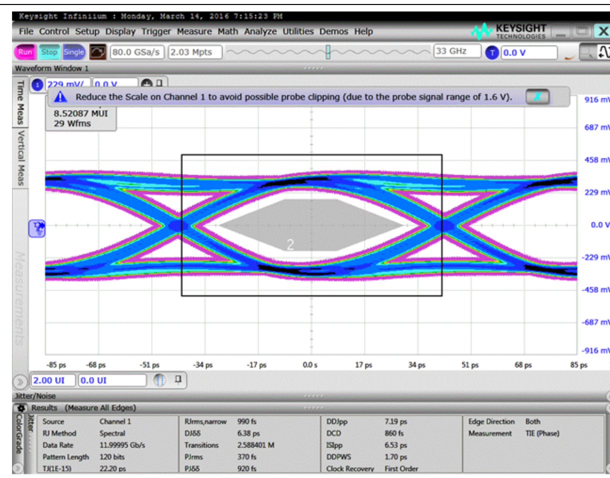


**Figure 123. Data Eye at 12 Gbps**

### 8.3.8 Alarm Outputs: Power Detectors for AGC Support

The GPIO pins can be configured as alarm outputs. The ADC31RF80 supports three different power detectors (an absolute peak power detector, crossing detector, and RMS power detector) as well as fast overrange from the ADC. The power detectors operate off the full-rate ADC output prior to the decimation filters.

#### *8.3.8.1 Absolute Peak Power Detector*

In this detector mode, the peak is computed over eight samples of the ADC output. Next, the peak for a block of N samples (N × S`) is computed over a programmable block length and then compared against a threshold to either set or reset the peak detector output (Figure 124 and Figure 125). There are two sets of thresholds and each set has two thresholds for hysteresis. The programmable DWELL-time counter is used for clearing the block detector alarm output.

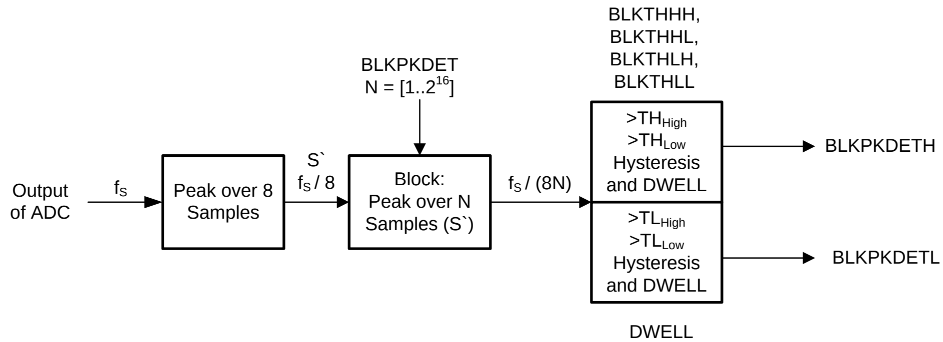



**Figure 124. Peak Power Detector Implementation**

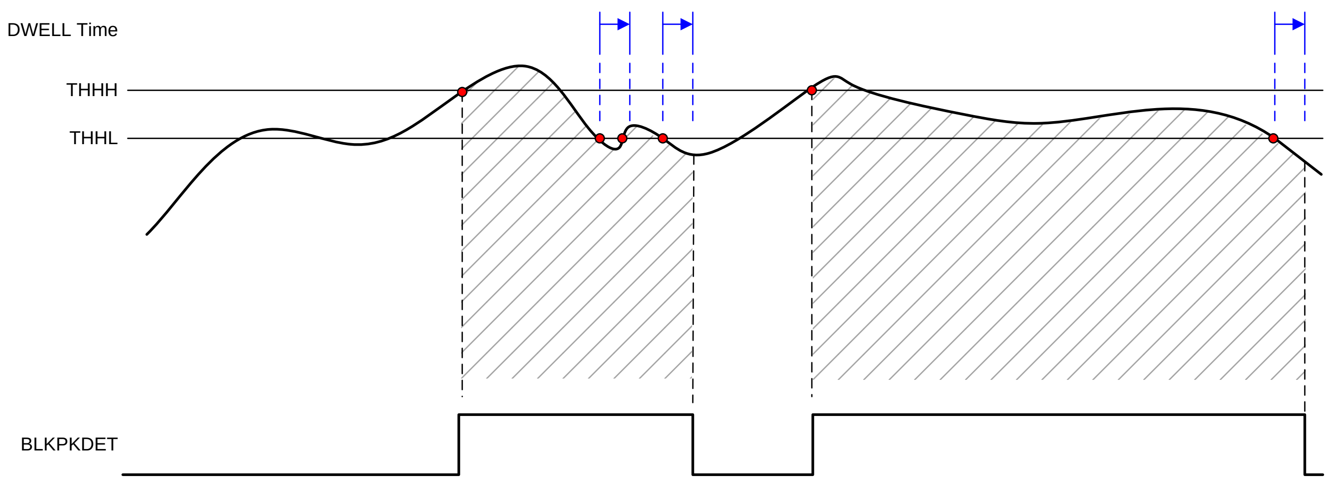



**Figure 125. Peak Power Detector Timing Diagram**

Table 8 shows the register configurations required to set up the absolute peak power detector. The detector operates in the $f_S$ / 8 clock domain; one peak sample is calculated over eight actual samples.

The automatic gain control (AGC) modes can be configured using registers in the power-detector page (54xxh).

**Table 8. Registers Required for the Peak Power Detector**

| REGISTER | ADDRESS | DESCRIPTION |
|---|---|---|
| PKDET EN | 5400h | Enables peak detector |
| BLKPKDET | 5401h, 5402h, 5403h | Sets the block length N of number of samples (S`). Number of actual ADC samples is 8x this value: N is 17 bits: 1 to $2^{16}$. |
| BLKTHHH, BLKTHHL, BLKTHLH, BLKTHLL | 5407h, 5408h, 5409h, 540Ah | Sets the different thresholds for the hysteresis function values from 0 to 256 (where 256 is equivalent to the peak amplitude).<br>For example: if BLKTHHH is to –2 dBFS from peak, $10^{(-2 / 20)} \times 256 = 203$, then set 5407h = CBh. |
| DWELL | 540Bh, 540Ch | When the computed block peak crosses the upper thresholds BLKTHHH or BLKTHLH, the peak detector output flags are set. In order to be reset, the computed block peak must remain continuously lower than the lower threshold (BLKTHHL or BLKTHLL) for the period specified by the DWELL value. This threshold is 16 bits and is specified in terms of $f_S$ / 8 clock cycles. |
| OUTSEL GPIO[4:1] | 5432h, 5433h, 5434h, 5435h | Connects the BLKPKDETH, BLKPKDETL alarms to the GPIO pins; common register. |
| IODIR | 5437h | Selects the direction for the four GPIO pins; common register. |
| RESET AGC | 542Bh | After configuration, reset the AGC module to start operation. |

### 8.3.8.2 Crossing Detector

In this detector mode the peak is computed over eight samples of the ADC output. Next, the peak for a block of N samples (N × S`) is computed over a programmable block length and then the peak is compared against two sets of programmable thresholds (with hysteresis). The crossing detector counts how many $f_S$ / 8 clock cycles that the block detector outputs are set high over a programmable time period and compares the counter value against the programmable thresholds. Figure 126 and Figure 127 show that the alarm outputs are updated at the end of the time period, routed to the GPIO pins, and held in that state through the next cycle. Alternatively, a 2-bit format can be used but (because the ADC31RF80 has four GPIO pins available) this feature uses all four pins.

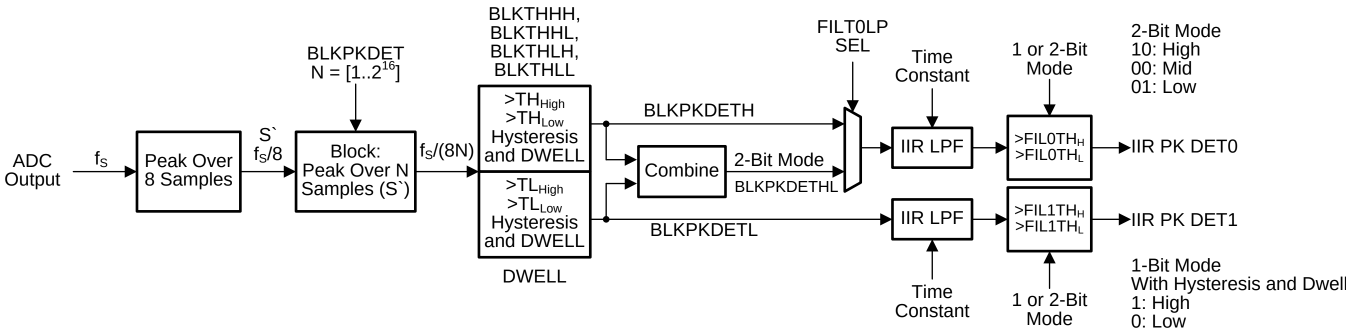



**Figure 126. Crossing Detector Implementation**

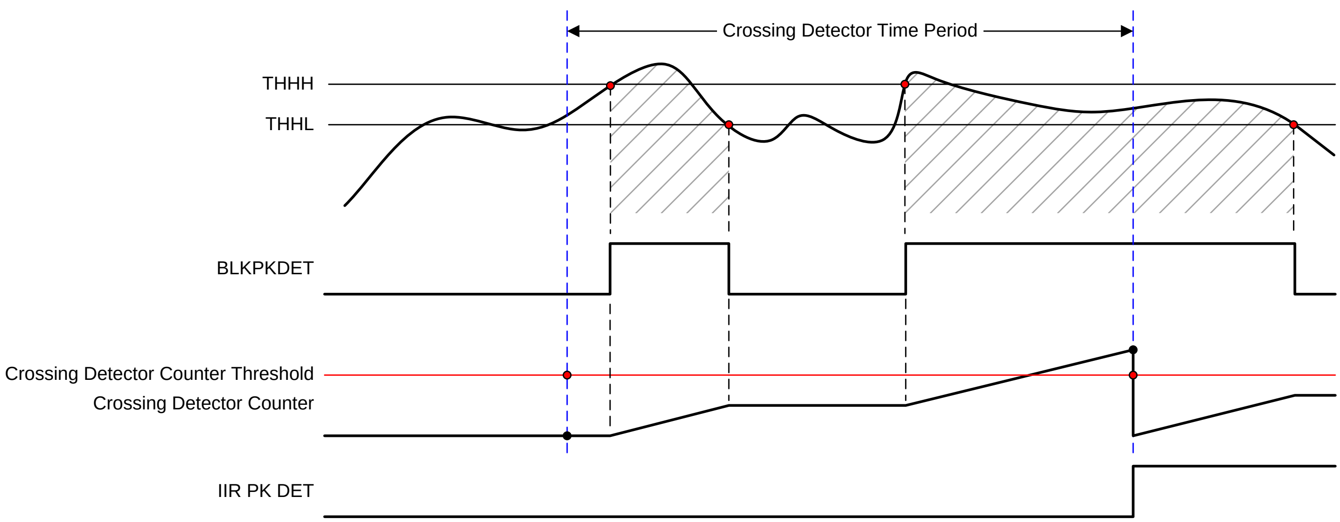



**Figure 127. Crossing Detector Timing Diagram**

Table 9 shows the register configurations required to set up the crossing detector. The detector operates in the $f_S$ / 8 clock domain. The AGC modes can be configured through registers located in the power detector page (54xxh).

**Table 9. Registers Required for the Crossing Detector Operation**

| REGISTER | ADDRESS | DESCRIPTION |
|---|---|---|
| PKDET EN | 5400h | Enables peak detector |
| BLKPKDET | 5401h, 5402h, 5403h | Sets the block length N of number of samples (S`).<br>Number of actual ADC samples is 8x this value: N is 17 bits: 1 to $2^{16}$. |
| BLKTHHH, BLKTHHL, BLKTHLH, BLKTHLL | 5407h, 5408h, 5409h, 540Ah | Sets the different thresholds for the hysteresis function values from 0 to 256 (where 256 is equivalent to the peak amplitude).<br>For example: if BLKTHHH is to –2 dBFS from peak, $10^{(-2 / 20)} \times 256 = 203$, then set 5407h = CBh. |
| FILT0LPSEL | 540Dh | Select block detector output or 2-bit output mode as the input to the interrupt identification register (IIR) filter. |
| TIMECONST | 540Eh, 540Fh, | Sets the crossing detector time period for N = 0 to 15 as 2N × $f_S$ / 8 clock cycles. The maximum time period is 32768 × $f_S$ / 8 clock cycles (approximately 87 µs at 3 GSPS). |
| FIL0THH, FIL0THL, FIL1THH, FIL1THL | 540Fh-5412h, 5416h-5419h | Comparison thresholds for the crossing detector counter. These thresholds are 16-bit thresholds in 2.14-signed notation. A value of 1 (4000h) corresponds to 100% crossings, a value of 0.125 (0800h) corresponds to 12.5% crossings. |
| DWELLIIR | 541Dh, 541Eh | DWELL counter for the IIR filter hysteresis. |
| IIR0 2BIT EN, IIR1 2BIT EN | 5413h, 54114h | Enables 2-bit output format for the crossing detector. |
| OUTSEL GPIO[4:1] | 5432h, 5433h, 5434h, 5435h | Connects the IIRPKDET0, IIRPKDET1 alarms to the GPIO pins; common register. |
| IODIR | 5437h | Selects the direction for the four GPIO pins; common register. |
| RESET AGC | 542Bh | After configuration, reset the AGC module to start operation. |

#### 8.3.8.3 RMS Power Detector

In this detector mode the peak power is computed for a block of N samples over a programmable block length and then compared against two sets of programmable thresholds (with hysteresis).

Figure 128 shows the configuration options provided by the RMS power detector circuit. The RMS power value (1 or 2 bit) can be output onto the GPIO pins. In 2-bit output mode, two different thresholds are used whereas the 1-bit output provides one threshold together with hysteresis.

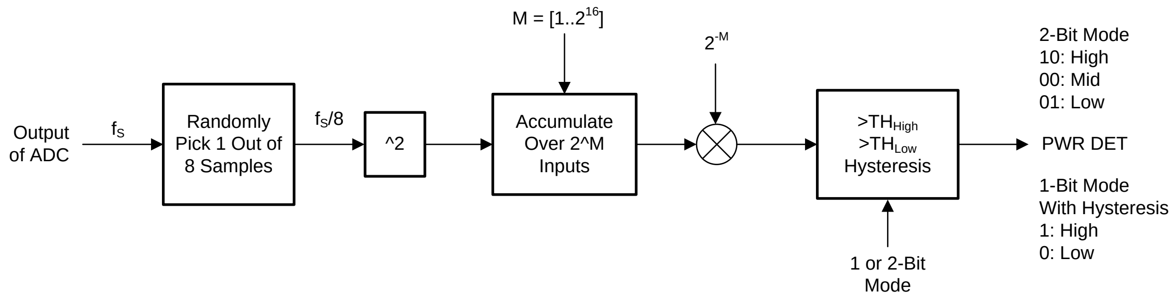



**Figure 128. RMS Power Detector Implementation**

Table 10 shows the register configurations required to set up the RMS power detector. The detector operates in the $f_S$ / 8 clock domain. The AGC modes can be configured through registers located in the power detector page (54xxh).

**Table 10. Registers Required for Using the RMS Power Detector Feature**

| REGISTER | ADDRESS | DESCRIPTION |
|---|---|---|
| RMSDET EN | 5420h | Enables RMS detector |
| PWRDETACCU | 5421h | Programs the block length to be used for RMS power computation. The block length is defined in terms of $f_S$ / 8 clocks.<br>The block length can be programmed as $2^M$ with M = 0 to 16. |
| PWRDETH, PWRDETL | 5422h, 5423h, 5424h, 5425h | The computed average power is compared against these high and low thresholds. One LSB of the thresholds represents 1 / $2^{16}$. For example: is PWRDETH is set to –14 dBFS from peak, $[10^{(-14 / 20)}]^2 \times 2^{16}$ = 2609, then set 5422h, 5423h = 0A31h. |
| RMS2BIT EN | 5427h | Enables 2-bit output format for the RMS detector output. |
| OUTSEL GPIO[4:1] | 5432h, 5433h, 5434h, 5435h | Connects the PWRDET alarms to the GPIO pins; common register. |
| IODIR | 5437h | Selects the direction for the four GPIO pins; common register. |
| RESET AGC | 542Bh | After configuration, reset the AGC module to start operation. |

#### *8.3.8.4 GPIO AGC MUX*

The GPIO pins can be used to control the NCO in wideband DDC mode or as alarm outputs. Figure 129 shows that the GPIO pins can be configured through the SPI control to output the alarm from the peak power (1 bit), crossing detector (1 or 2 bit), faster overrange, or the RMS power output.

The programmable output MUX allows connecting any signal (including the NCO control) to any of the four GPIO pins. These pins can be configured as outputs (AGC alarm) or inputs (NCO control) through SPI programming.

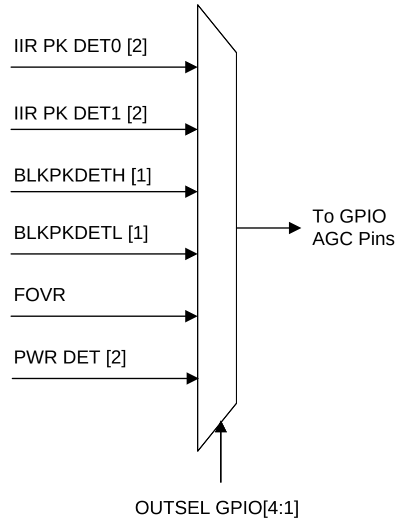



**Figure 129. GPIO Output MUX Implementation**

### 8.3.9 Power-Down Mode

The ADC31RF80 provides a lot of configurability for the power-down mode. Power-down can be enabled using the PDN pin or the SPI register writes.

### 8.3.10 ADC Test Pattern

The ADC31RF80 provides several different options to output test patterns instead of the actual output data of the ADC in order to simplify the serial interface and system debug of the JESD204B digital interface link. Figure 130 shows the output data path.

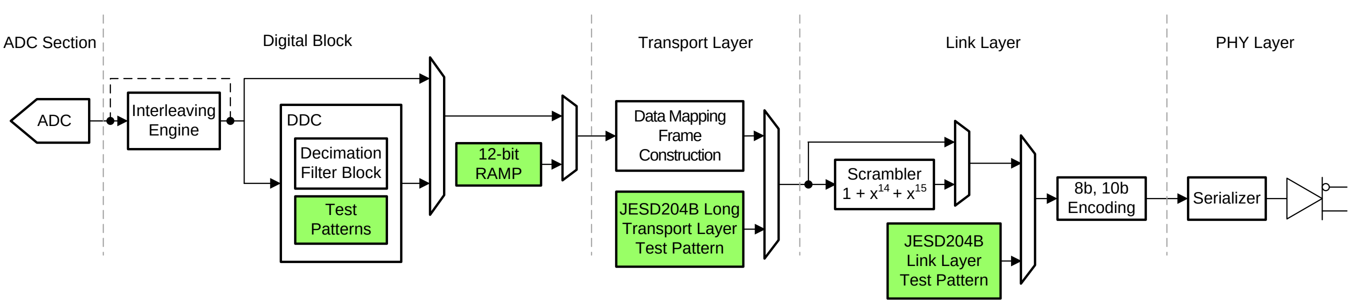



**Figure 130. Test Pattern Generator Implementation**

#### *8.3.10.1 Digital Block*

The ADC test pattern replaces the actual output data of the ADC. The test patterns listed in Table 11 are available when the DDC is enabled and located in register 37h of the decimation filter page. When programmed, the test patterns are output for each converter (M) stream. The number of converter streams increases by 2 when complex (I, Q) output or dual-band DDC is selected.

Additionally, a 12-bit test pattern is also available.

**NOTE**

The number of converters increases in dual-band DDC mode and with a complex output.

**Table 11. Test Pattern Options (Register 37h and 38h in Decimation Filter Page)**

| BIT | NAME | DEFAULT | DESCRIPTION |
|---|---|---|---|
| Address 37h, 38h (bits 7-0) | TEST PATTERN DDC1 I-DATA,<br>TEST PATTERN DDC1 Q-DATA,<br>TEST PATTERN DDC2 I-DATA,<br>TEST PATTERN DDC2 Q-DATA, | 0000 | Test pattern outputs on when the I and Q stream DDC option is chosen.<br>0000 = Normal operation using ADC output data<br>0001 = Outputs all 0s<br>0010 = Outputs all 1s<br>0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101<br>0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 65535<br>0110 = Single pattern: output data are a custom pattern 1 (75h and 76h)<br>0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2<br>1000 = Deskew pattern: output data are AAAAh<br>1001 = SYNC pattern: output data are FFFFh |

#### *8.3.10.2 Transport Layer*

The transport layer maps the ADC output data into 8-bit octets and constructs the JESD204B frames using the LMFS parameters. Tail bits or 0's are added when needed. Alternatively, the JESD204B long transport layer test pattern can be substituted, as shown in Table 12, instead of the ADC data with the JESD frame.

**Table 12. Transport Layer Test Mode EN (Register 01h)**

| BIT | NAME | DEFAULT | DESCRIPTION |
|---|---|---|---|
| 4 | TESTMODE EN | 0 | Generates long transport layer test pattern mode according to section 5.1.6.3 of the JESD204B specification.<br>0 = Test mode disabled<br>1 = Test mode disabled |

#### *8.3.10.3 Link Layer*

The link layer contains the scrambler and the 8b, 10b encoding of any data passed on from the transport layer. Additionally, the link layer also handles the initial lane alignment sequence that can be manually restarted.

The link layer test patterns are intended for testing the quality of the link (jitter testing and so forth). The test patterns do not pass through the 8b, 10b encoder and contain the options listed in Table 13.

**Table 13. Link Layer Test Mode (Register 03h)**

| BIT | NAME | DEFAULT | DESCRIPTION |
|---|---|---|---|
| 7-5 | LINK LAYER TESTMODE | 000 | Generates a pattern according to section 5.3.3.8.2 of the JESD204B document.<br>000 = Normal ADC data<br>001 = D21.5 (high-frequency jitter pattern)<br>010 = K28.5 (mixed-frequency jitter pattern)<br>011 = Repeat the initial lane alignment (generates a K28.5 character and repeats lane alignment sequences continuously)<br>100 = 12-octet random pattern (RPAT) jitter pattern |

Furthermore, a $2^{15}$ pseudo-random binary sequence (PRBS) can be enabled by setting up a custom test pattern (AAAAh) in the ADC section and running AAAAh through the 8b, 10b encoder with scrambling enabled.

## 8.4 Device Functional Modes

### 8.4.1 Device Configuration

The ADC31RF80 can be configured using a serial programming interface, as described in the *Serial Interface* section. In addition, the device has one dedicated parallel pin (PDN) for controlling the power-down modes.

### 8.4.2 JESD204B Interface

The ADC31RF80 supports device subclass 1 with a maximum output data rate of 12.5 Gbps for each serial transmitter.

An external SYSREF signal is used to align all internal clock phases and the local multiframe clock to a specific sampling clock edge. This alignment allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty. Figure 131 shows that the SYNCB input is used to control the JESD204B SerDes blocks.

Depending on the ADC sampling rate, the JESD204B output interface can be operated with one, two, or four lanes. The JESD204B setup and configuration of the frame assembly parameters is controlled through the SPI interface.

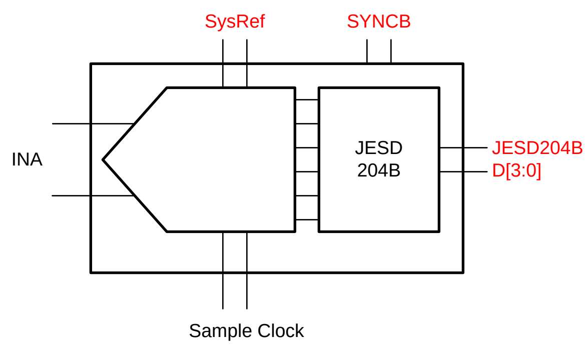



**Figure 131. JESD Signal Overview**

The JESD204B transmitter block, shown in Figure 132, consists of the transport layer, the data scrambler, and the link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format and manages if the ADC output data or test patterns are transmitted. The link layer performs the 8b, 10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer can be scrambled.

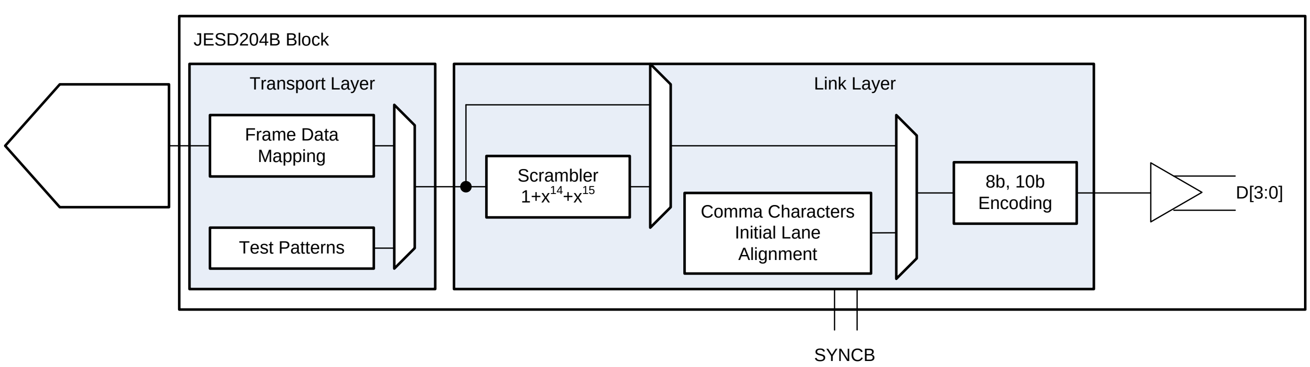



**Figure 132. JESD Digital Block Implementation**

## Device Functional Modes (continued)

#### *8.4.2.1 JESD204B Initial Lane Alignment (ILA)*

The receiving device starts the initial lane alignment process by deasserting the SYNCB signal. The SYNCB signal can be issued using the SYNCB input pins or by setting the proper SPI bits. When a logic low is detected on the SYNCB input, as shown in Figure 133, the ADC31RF80 starts transmitting comma (K28.5) characters to establish the code group synchronization.

When synchronization completes, the receiving device reasserts the SYNCB signal and the ADC31RF80 starts the initial lane alignment sequence with the next local multiframe clock boundary. The ADC31RF80 transmits four multiframes, each containing K frames (K is SPI programmable). Each of the multiframes contains the frame start and end symbols. The second multiframe also contains the JESD204 link configuration data.

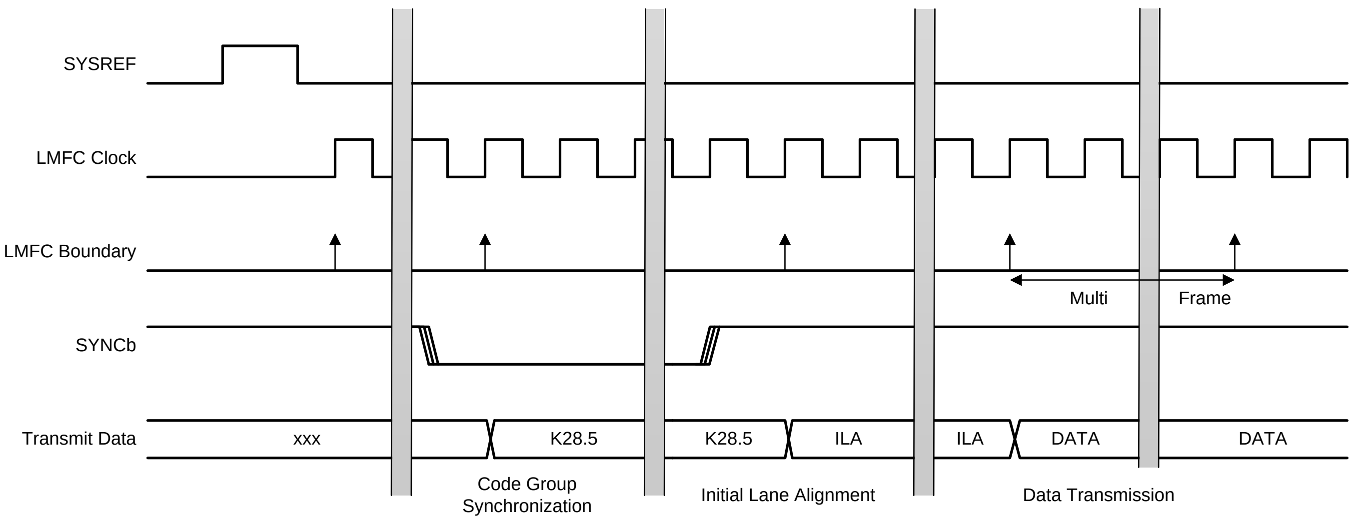



**Figure 133. JESD Internal Timing Information**

#### *8.4.2.2 JESD204B Frame Assembly*

The JESD204B standard defines the following parameters:

- F is the number of octets per frame clock period
- L is the number of lanes per link
- M is the number of converters for the device
- S is the number of samples per frame

## Device Functional Modes (continued)

### *8.4.2.3 JESD204B Frame Assembly with Decimation (Single-Band DDC): Complex Output*

Table 14 lists the available JESD204B interface formats and valid ranges for the ADC31RF80 with decimation (single-band DDC) when using a complex output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. Table 15 shows the sample alignment on the different lanes.

**Table 14. JESD Mode Options: Single-Band Complex Output**

| DECIMATION SETTING (Complex) | NUMBER OF ACTIVE DDCS | L | M | F | S | PLL MODE | JESD MODE0 | JESD MODE1 | JESD MODE2 | RATIO [$f_{SerDes}$ / $f_{CLK}$ (Gbps / GSPS)] |
|---|---|---|---|---|---|---|---|---|---|---|
| Divide-by-4 | 1 | 4 | 2 | 1 | 1 | 20x | 1 | 1 | 0 | 2.5 |
| | | 4 | 2 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 5 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-6 | 1 | 4 | 2 | 1 | 1 | 20x | 1 | 1 | 0 | 1.67 |
| | | 4 | 2 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 3.33 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-8 | 1 | 2 | 2 | 2 | 1 | 20x | 1 | 0 | 0 | 2.5 |
| | | 1 | 2 | 4 | 1 | 40x | 2 | 0 | 0 | 5 |
| Divide-by-9 | 1 | 2 | 2 | 2 | 1 | 20x | 1 | 0 | 0 | 2.22 |
| | | 1 | 2 | 4 | 1 | 40x | 2 | 0 | 0 | 4.44 |
| Divide-by-10 | 1 | 2 | 2 | 2 | 1 | 20x | 1 | 0 | 0 | 2 |
| | | 1 | 2 | 4 | 1 | 40x | 2 | 0 | 0 | 4 |
| Divide-by-12 | 1 | 2 | 2 | 2 | 1 | 20x | 1 | 0 | 0 | 1.67 |
| | | 1 | 2 | 4 | 1 | 40x | 2 | 0 | 0 | 3.33 |
| Divide-by-16 | 1 | 2 | 2 | 2 | 1 | 20x | 1 | 0 | 0 | 1.25 |
| | | 1 | 2 | 4 | 1 | 40x | 2 | 0 | 0 | 2.5 |
| Divide-by-18 | 1 | 2 | 2 | 2 | 1 | 20x | 1 | 0 | 0 | 1.11 |
| | | 1 | 2 | 4 | 1 | 40x | 2 | 0 | 0 | 2.22 |
| Divide-by-20 | 1 | 2 | 2 | 2 | 1 | 20x | 1 | 0 | 0 | 1 |
| | | 1 | 2 | 4 | 1 | 40x | 2 | 0 | 0 | 2 |
| Divide-by-24 | 1 | 1 | 2 | 4 | 1 | 20x | 1 | 0 | 0 | 1.67 |
| Divide-by-32 | 1 | 1 | 2 | 4 | 1 | 40x | 2 | 0 | 0 | 1.25 |

**Table 15. JESD Sample Lane Alignments: Single-Band Complex Output**

| OUTPUT LANE | LMFS = 8411 | LMFS = 8422 | | LMFS = 4421 20X | | LMFS = 4421 40X | | LMFS = 4442 | | | | LMFS = 2441 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D0 | $AI_0$ [15:8] | $AI_0$ [15:8] | $AI_0$ [7:0] | $AI_0$ [15:8] | $AI_0$ [7:0] | | | | | | | | | | |
| D1 | $AI_0$ [7:0] | $AI_1$ [15:8] | $AI_1$ [7:0] | $AQ_0$ [15:8] | $AQ_0$ [7:0] | $AI_0$ [15:8] | $AI_0$ [7:0] | $AI_0$ [15:8] | $AI_0$ [7:0] | $AI_1$ [15:8] | $AI_1$ [7:0] | $AI_0$ [15:8] | $AI_0$ [7:0] | $AQ_0$ [15:8] | $AQ_0$ [7:0] |
| D2 | $AQ_0$ [15:8] | $AQ_0$ [15:8] | $AQ_0$ [7:0] | | | $AQ_0$ [15:8] | $AQ_0$ [7:0] | $AQ_0$ [15:8] | $AQ_0$ [7:0] | $AQ_1$ [15:8] | $AQ_1$ [7:0] | | | | |
| D3 | $AQ_0$ [7:0] | $AQ_1$ [15:8] | $AQ_1$ [7:0] | | | | | | | | | | | | |

### 8.4.2.4 JESD204B Frame Assembly with Decimation (Single-Band DDC): Real Output

Table 16 lists the available JESD204B formats and valid ranges for the ADC31RF80 with decimation (single-band DDC) when using real output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. Table 17 shows the sample alignment on the different lanes.

**Table 16. JESD Mode Options: Single-Band Real Output (Wide Bandwidth)**

| DECIMATION SETTING (Complex) | NUMBER OF ACTIVE DDCS | L | M | F | S | PLL MODE | JESD MODE0 | JESD MODE1 | JESD MODE2 | RATIO [$f_{SerDes}$ / $f_{CLK}$ (Gbps / GSPS)] |
|---|---|---|---|---|---|---|---|---|---|---|
| Divide-by-4 (Divide-by-2 real) | 1 | 4 | 1 | 2 | 4 | 20x | 1 | 0 | 0 | 2.5 |
| | | 2 | 1 | 4 | 4 | 40x | 2 | 0 | 0 | 5 |
| | | 2 | 1 | 1 | 1 | 40x | 0 | 0 | 1 | |
| Divide-by-6 (Divide-by-3 real) | 1 | 4 | 1 | 2 | 4 | 20x | 1 | 0 | 0 | 1.67 |
| | | 2 | 1 | 4 | 4 | 40x | 2 | 0 | 0 | 3.33 |
| | | 2 | 1 | 1 | 1 | 40x | 0 | 0 | 1 | |

**Table 17. JESD Sample Lane Alignment: Single-Band Real Output (Wide Bandwidth)**

| OUTPUT LANE | LMFS = 8224 | | LMFS = 4244 | | | | LMFS = 4211 |
|---|---|---|---|---|---|---|---|
| D0 | $A_0$[15:8] | $A_0$[7:0] | | | | | |
| D1 | $A_1$[15:8] | $A_1$[7:0] | $A_0$[15:8] | $A_0$[7:0] | $A_1$[15:8] | $A_1$[7:0] | $A_0$[15:8] |
| D2 | $A_2$[15:8] | $A_2$[7:0] | $A_2$[15:8] | $A_2$[7:0] | $A_3$[15:8] | $A_3$[7:0] | $A_0$[7:0] |
| D3 | $A_3$[15:8] | $A_3$[7:0] | | | | | |

#### 8.4.2.5 *JESD204B Frame Assembly with Decimation (Single-Band DDC): Real Output*

Table 18 lists the available JESD204B formats and valid ranges for the ADC31RF80 with decimation (dual-band DDC) when using a complex output format. Table 19 shows the sample alignment on the different lanes.

**Table 18. JESD Mode Options: Single-Band Real Output**

| DECIMATION SETTING (Complex) | NUMBER OF ACTIVE DDCS | L | M | F | S | PLL MODE | JESD MODE0 | JESD MODE1 | JESD MODE2 | RATIO [$f_{SerDes}$ / $f_{CLK}$ (Gbps / GSPS)] |
|---|---|---|---|---|---|---|---|---|---|---|
| Divide-by-8 (Divide-by-4 real) | 1 | 2 | 1 | 1 | 1 | 20x | 1 | 1 | 0 | 2.5 |
| | | 2 | 1 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 1 | 1 | 2 | 1 | 40x | 0 | 0 | 1 | 5 |
| | | 1 | 1 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-9 (Divide-by-4.5 real) | 1 | 2 | 1 | 1 | 1 | 20x | 1 | 1 | 0 | 2.22 |
| | | 2 | 1 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 1 | 1 | 2 | 1 | 40x | 0 | 0 | 1 | 4.44 |
| | | 1 | 1 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-10 (Divide-by-5 real) | 1 | 2 | 1 | 1 | 1 | 20x | 1 | 1 | 0 | 2 |
| | | 2 | 1 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 1 | 1 | 2 | 1 | 40x | 0 | 0 | 1 | 4 |
| | | 1 | 1 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-12 (Divide-by-6 real) | 1 | 2 | 1 | 1 | 1 | 20x | 1 | 1 | 0 | 1.67 |
| | | 2 | 1 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 1 | 1 | 2 | 1 | 40x | 0 | 0 | 1 | 3.33 |
| | | 1 | 1 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-16 (Divide-by-8 real) | 1 | 2 | 1 | 1 | 1 | 20x | 1 | 1 | 0 | 1.25 |
| | | 2 | 1 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 1 | 1 | 2 | 1 | 40x | 0 | 0 | 1 | 2.5 |
| | | 1 | 1 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-18 (Divide-by-9 real) | 1 | 2 | 1 | 1 | 1 | 20x | 1 | 1 | 0 | 1.11 |
| | | 2 | 1 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 1 | 1 | 2 | 1 | 40x | 0 | 0 | 1 | 2.22 |
| | | 1 | 1 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-20 (Divide-by-10 real) | 1 | 2 | 1 | 1 | 1 | 20x | 1 | 1 | 0 | 1 |
| | | 2 | 1 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 1 | 1 | 2 | 1 | 40x | 0 | 0 | 1 | 2 |
| | | 1 | 1 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-24 (Divide-by-12 real) | 1 | 1 | 1 | 2 | 1 | 40x | 0 | 0 | 1 | 1.67 |
| | | 1 | 1 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-32 (Divide-by-16 real) | 1 | 1 | 1 | 2 | 1 | 40x | 0 | 0 | 1 | 1.25 |
| | | 1 | 1 | 4 | 2 | 40x | 2 | 0 | 0 | |

**Table 19. JESD Sample Lane Assignment: Single-Band Real Output**

| OUTPUT LANE | LMFS = 4211 | LMFS = 4222 | | LMFS = 2221 | | LMFS = 2242 | | | |
|---|---|---|---|---|---|---|---|---|---|
| D0 | $A_0$[15:8] | $A_0$[15:8] | $A_0$[7:0] | | | | | | |
| D1 | $A_0$[7:0] | $A_1$[15:8] | $A_1$[7:0] | $A_0$ [15:8] | $A_0$[7:0] | $A_0$[15:8] | $A_0$[7:0] | $A_1$[15:8] | $A_1$[7:0] |

#### 8.4.2.6 JESD204B Frame Assembly with Decimation (Dual-Band DDC): Complex Output

Table 20 lists the available JESD204B formats and valid ranges for the ADC31RF80 with decimation (dual-band DDC) when using a complex output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. Table 21 shows the sample alignment on the different lanes.

**Table 20. JESD Mode Options: Dual-Band Complex Output**

| DECIMATION SETTING (Complex) | NUMBER OF ACTIVE DDCS | L | M | F | S | PLL MODE | JESD MODE0 | JESD MODE1 | JESD MODE2 | RATIO [$f_{SerDes}$ / $f_{CLK}$ (Gbps / GSPS)] |
|---|---|---|---|---|---|---|---|---|---|---|
| Divide-by-8 | 2 | 4 | 4 | 2 | 1 | 20x | 1 | 0 | 0 | 2.5 |
| | | 2 | 4 | 4 | 1 | 40x | 2 | 0 | 0 | 5 |
| Divide-by-9 | 2 | 4 | 4 | 2 | 1 | 20x | 1 | 0 | 0 | 2.22 |
| | | 2 | 4 | 4 | 1 | 40x | 2 | 0 | 0 | 4.44 |
| Divide-by-10 | 2 | 4 | 4 | 2 | 1 | 20x | 1 | 0 | 0 | 2 |
| | | 2 | 4 | 4 | 1 | 40x | 2 | 0 | 0 | 4 |
| Divide-by-12 | 2 | 4 | 4 | 2 | 1 | 20x | 1 | 0 | 0 | 1.67 |
| | | 2 | 4 | 4 | 1 | 40x | 2 | 0 | 0 | 3.33 |
| Divide-by-16 | 2 | 4 | 4 | 2 | 1 | 20x | 1 | 0 | 0 | 1.25 |
| | | 2 | 4 | 4 | 1 | 40x | 2 | 0 | 0 | 2.5 |
| Divide-by-18 | 2 | 4 | 4 | 2 | 1 | 20x | 1 | 0 | 0 | 1.11 |
| | | 2 | 4 | 4 | 1 | 40x | 2 | 0 | 0 | 2.22 |
| Divide-by-20 | 2 | 4 | 4 | 2 | 1 | 20x | 1 | 0 | 0 | 1 |
| | | 2 | 4 | 4 | 1 | 40x | 2 | 0 | 0 | 2 |
| Divide-by-24 | 2 | 2 | 4 | 4 | 1 | 40x | 2 | 0 | 0 | 1.67 |
| Divide-by-32 | 2 | 2 | 4 | 4 | 1 | 40x | 2 | 0 | 0 | 1.25 |

**Table 21. JESD Sample Lane Assignment: Dual-Band Complex Output(1)**

| OUTPUT LANE | LMFS = 8821 | | LMFS = 4841 | | | |
|---|---|---|---|---|---|---|
| D0 | $A1_0$[15:8] | $A1_0$[7:0] | | | | |
| D1 | $A1Q_0$[15:8] | $A1Q_0$[7:0] | $A1I_0$[15:8] | $A1I_0$[7:0] | $A1Q_0$[15:8] | $A1Q_0$[7:0] |
| D2 | $A2I_0$[15:8] | $A2I_0$[7:0] | $A2I_0$[15:8] | $A2I_0$[7:0] | $A2Q_0$[15:8] | $A2Q_0$[7:0] |
| D3 | $A2Q_0$[15:8] | $A2Q_0$[7:0] | | | | |

(1) Blue and green shading indicates the output of the two DDC bands.

### 8.4.2.7 *JESD204B Frame Assembly with Decimation (Dual-Band DDC): Real Output*

Table 22 lists the available JESD204B formats and valid ranges for the ADC31RF80 with decimation (dual-band DDC) when using real output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. Table 23 shows the sample alignment on the different lanes.

**Table 22. JESD Mode Options: Dual-Band Real Output**

| DECIMATION SETTING (Complex) | NUMBER OF ACTIVE DDCS | L | M | F | S | PLL MODE | JESD MODE0 | JESD MODE1 | JESD MODE2 | RATIO [$f_{SerDes}$ / $f_{CLK}$ (Gbps / GSPS)] |
|---|---|---|---|---|---|---|---|---|---|---|
| Divide-by-8 (Divide-by-4 real) | 2 | 4 | 2 | 1 | 1 | 20x | 1 | 1 | 0 | 2.5 |
| | | 4 | 2 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 5 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-9 (Divide-by-4.5 real) | 2 | 4 | 2 | 1 | 1 | 20x | 1 | 1 | 0 | 2.22 |
| | | 4 | 2 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 4.44 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-10 (Divide-by-5 real) | 2 | 4 | 2 | 1 | 1 | 20x | 1 | 1 | 0 | 2 |
| | | 4 | 2 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 4 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-12 (Divide-by-6 real) | 2 | 4 | 2 | 1 | 1 | 20x | 1 | 1 | 0 | 1.67 |
| | | 4 | 2 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 3.33 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-16 (Divide-by-8 real) | 2 | 4 | 2 | 1 | 1 | 20x | 1 | 1 | 0 | 1.25 |
| | | 4 | 2 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 2.5 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-18 (Divide-by-9 real) | 2 | 4 | 2 | 1 | 1 | 20x | 1 | 1 | 0 | 1.11 |
| | | 4 | 2 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 2.22 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-20 (Divide-by-10 real) | 2 | 4 | 2 | 1 | 1 | 20x | 1 | 1 | 0 | 1 |
| | | 4 | 2 | 2 | 2 | 20x | 1 | 0 | 0 | |
| | | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 2 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-24 (Divide-by-12 real) | 2 | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 1.67 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |
| Divide-by-32 (Divide-by-16 real) | 2 | 2 | 2 | 2 | 1 | 40x | 0 | 0 | 1 | 1.25 |
| | | 2 | 2 | 4 | 2 | 40x | 2 | 0 | 0 | |

**Table 23. JESD Sample Lane Assignment: Dual-Band Complex Output(1)**

| OUTPUT LANE | LMFS = 8411 | LMFS = 8422 | | LMFS = 4421 | | LMFS = 4442 | | | |
|---|---|---|---|---|---|---|---|---|---|
| D0 | $A1_0$[15:8] | $A1_0$[15:8] | $A1_0$[7:0] | | | | | | |
| D1 | $A1_0$[7:0] | $A1_1$[15:8] | $A1_1$[7:0] | $A1_0$[15:8] | $A1_0$[7:0] | $A1_0$[15:8] | $A1_0$[7:0] | $A1_1$[15:8] | $A1_1$[7:0] |
| D2 | $A2_0$[15:8] | $A2_0$[15:8] | $A2_0$[7:0] | $A2_0$[15:8] | $A2_0$[7:0] | $A2_0$[15:8] | $A2_0$[7:0] | $A2_1$[15:8] | $A2_1$[7:0] |
| D3 | $A2_0$[7:0] | $A2_1$[15:8] | $A2_1$[7:0] | | | | | | |

(1) Blue and green shading indicates the output of the two DDC bands.

### 8.4.3 Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDIN (serial interface data) pins. Serially shifting bits into the device is enabled when SEN is low. Figure 134 shows that SDIN serial data are latched at every SCLK rising edge when SEN is active (low). Table 24 also shows that the interface can function with SCLK frequencies from 20 MHz down to low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

The SPI access uses 24 bits consisting of eight register data bits, 12 register address bits, and four special bits to distinguish between read/write, page and register, and individual channel access, as described in Table 25.

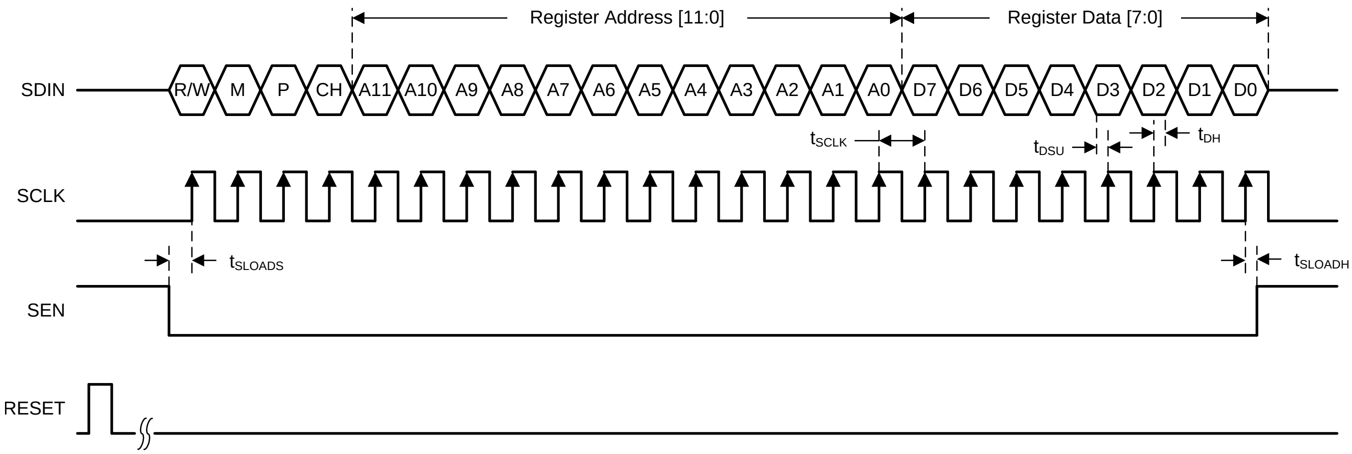



**Figure 134. SPI Timing Diagram**

**Table 24. SPI Timing Information**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCLK}$ | SCLK frequency (equal to 1 / $t_{SCLK}$) | 1 | | 20 | MHz |
| $t_{SLOADS}$ | SEN to SCLK setup time | 50 | | | ns |
| $t_{SLOADH}$ | SCLK to SEN hold time | 50 | | | ns |
| $t_{DSU}$ | SDIN setup time | 10 | | | ns |
| $t_{DH}$ | SDIN hold time | 10 | | | ns |
| $t_{SDOUT}$ | Delay between SCLK falling edge to SDOUT | | 10 | | ns |

**Table 25. SPI Input Description**

| SPI BIT | DESCRIPTION | OPTIONS |
|---|---|---|
| R/W bit | Read/write bit | 0 = SPI write<br>1 = SPI read back |
| M bit | SPI bank access | 0 = Analog SPI bank (master)<br>1 = All digital SPI banks (main digital, interleaving, decimation filter, JESD digital, and so forth) |
| P bit | JESD page selection bit | 0 = Page access<br>1 = Register access |
| CH bit | SPI access for a specific channel of the JESD SPI bank. Useful for the dual-channel device, ADC32RF80. | — |
| ADDR[11:0] | SPI address bits | — |
| DATA[7:0] | SPI data bits | — |

Figure 135 shows the SDOUT timing when data are read back from a register. Data are placed on the SDOUT bus at the SCLK falling edge after a delay of $t_{SDOUT}$ (10 ns typical) so that the data can be latched at the SCLK rising edge by the external receiver.

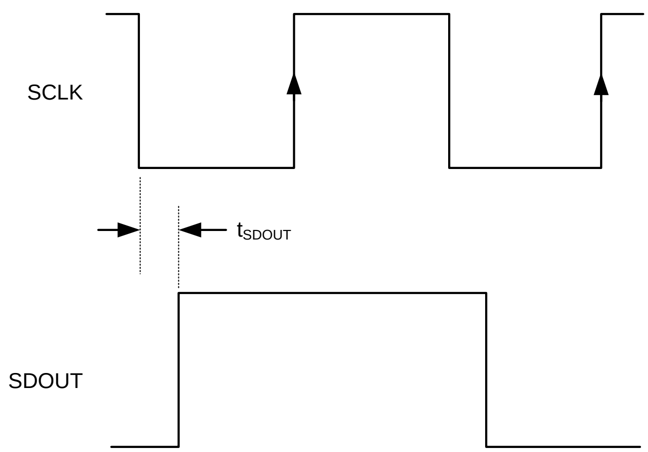



**Figure 135. SDOUT Timing**

#### 8.4.3.1 Serial Register Write: Analog Bank

The internal register of the ADC31RF80 analog bank (Figure 136) can be programmed by:

1. Driving the SEN pin low.
2. Initiating a serial interface cycle selecting the page address of the register whose content must be written. To select the master page: write address 0012h with 04h. To select the ADC page: write address 0011h with FFh.
3. Writing the register content. When a page is selected, multiple registers located in the same page can be programmed.

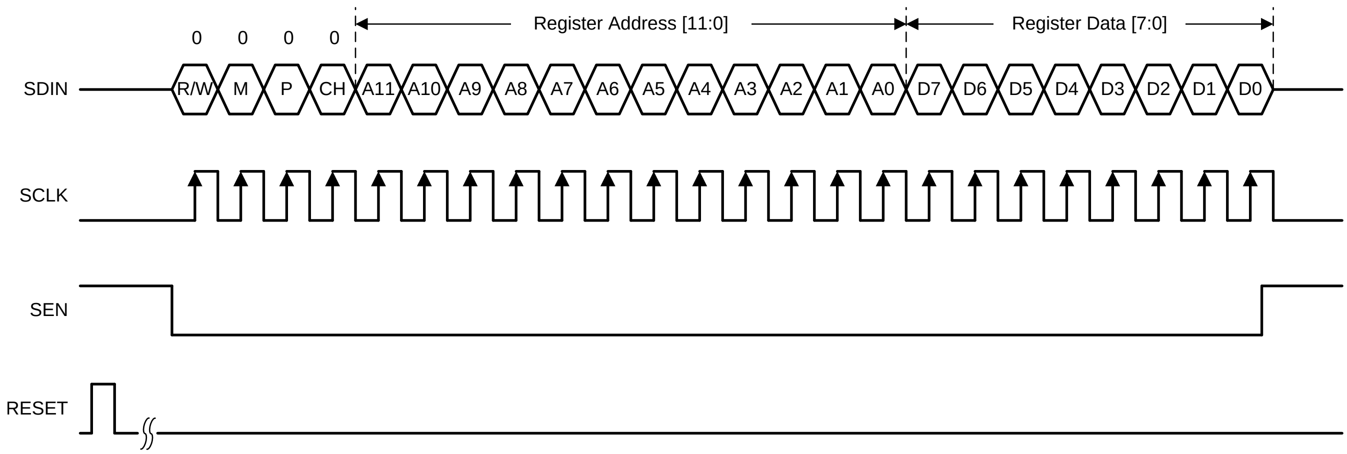



**Figure 136. SPI Write Timing Diagram for the Analog Bank**

#### 8.4.3.2 Serial Register Readout: Analog Bank

Contents of the registers located in the two pages of the analog bank (Figure 137) can be readback by:

1. Driving the SEN pin low.
2. Selecting the page address of the register whose content must be read. Master page: write address 0012h with 04h. ADC page: write address 0011h with FFh.
3. Setting the R/W bit to 1 and writing the address to be read back.
4. Reading back the register content on the SDOUT pin. When a page is selected, the contents of multiple registers located in same page can be readback.

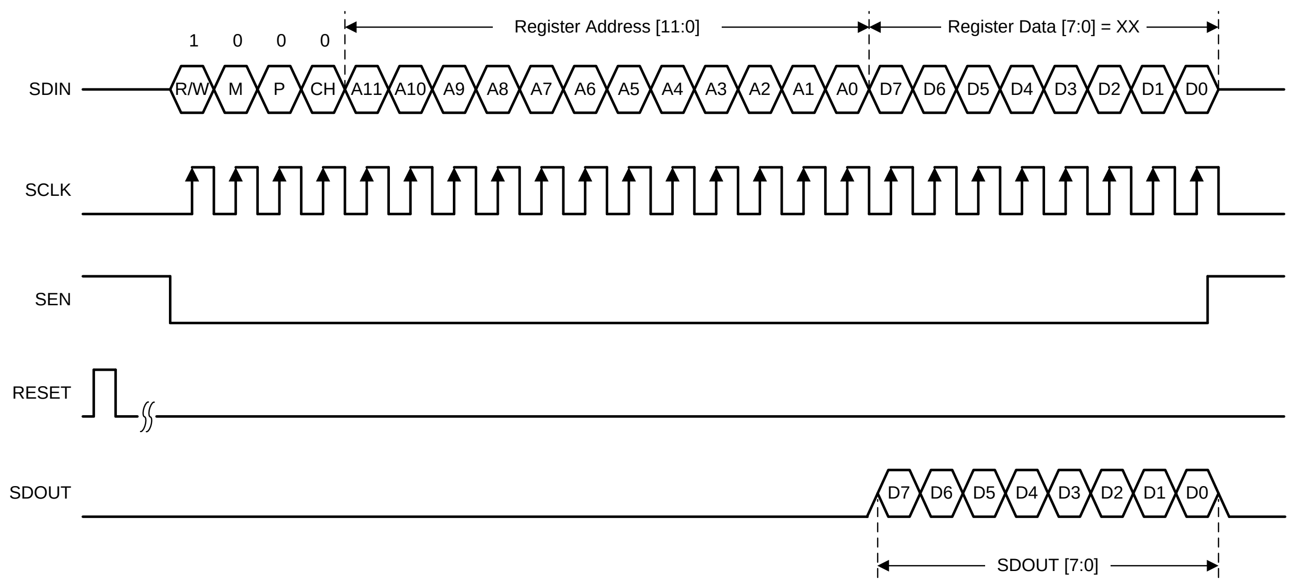



**Figure 137. SPI Read Timing Diagram for the Analog Bank**

#### 8.4.3.3 Serial Register Write: Digital Bank

The digital bank contains four pages (the offset corrector page, digital gain page, main digital page, and JESD digital page). Figure 138 shows the timing for the individual page selection. The registers located in the pages of the digital bank can be programmed by:

1. Driving the SEN pin low.
2. Setting the M bit to 1 and specifying the page with with the desired register. There are seven pages in Digital Bank. These pages can be selected by appropriately programming register bits DIGITAL BANK PAGE SEL, located in addresses 002h, 003h, and 004h, using three consecutive SPI cycles. Addressing in a SPI cycle begins with 4xxx when selecting a page from digital bank because the M bit must be set to 1.
   - To select the offset corrector page: write address 4004h with 61h, 4003h with 00h, and 4002h with 00h.
   - To select the digital gain page: write address 4004h with 61h, 4003h with 00h, and 4002h with 05h.
   - To select the main digital page: write address 4004h with 68h, 4003h with 00h, and 4002h with 00h.
   - To select the JESD digital page: write address 4004h with 69h, 4003h with 00h, and 4002h with 00h.

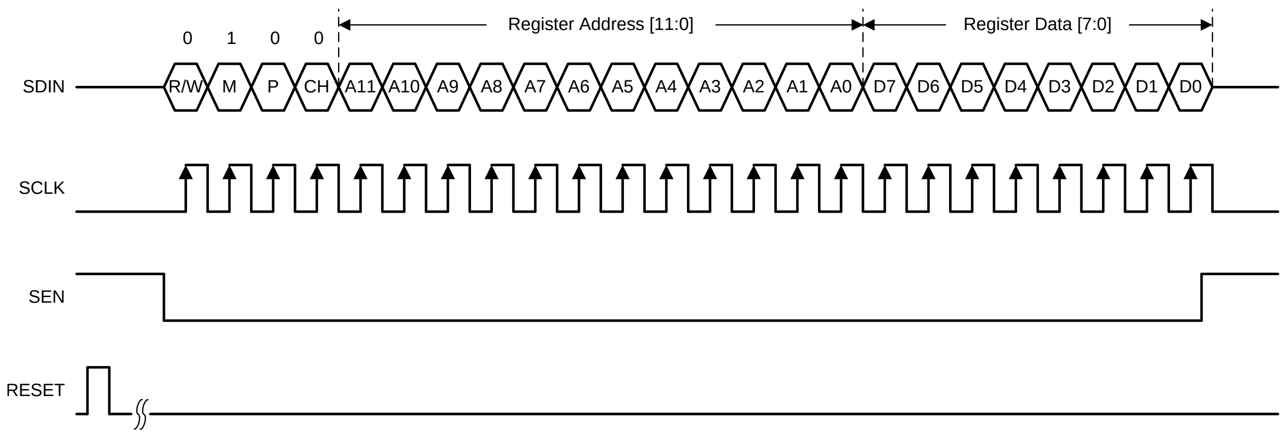



**Figure 138. SPI Write Timing Diagram for Digital Bank Page Selection**

3. Writing into the desired register by setting both the M bit and P bit to 1. Write register content. When a page is selected, multiple writes into the same page can be done. As shown in Figure 139, addressing in an SPI cycle begins with 6xxx when selecting a page from the digital bank because the M bit must be set to 1.

   Keep CH = 1 while programing registers in JESD digital page. Thus, an SPI cycle to program registers in JESD digital page begins with 7xxx.

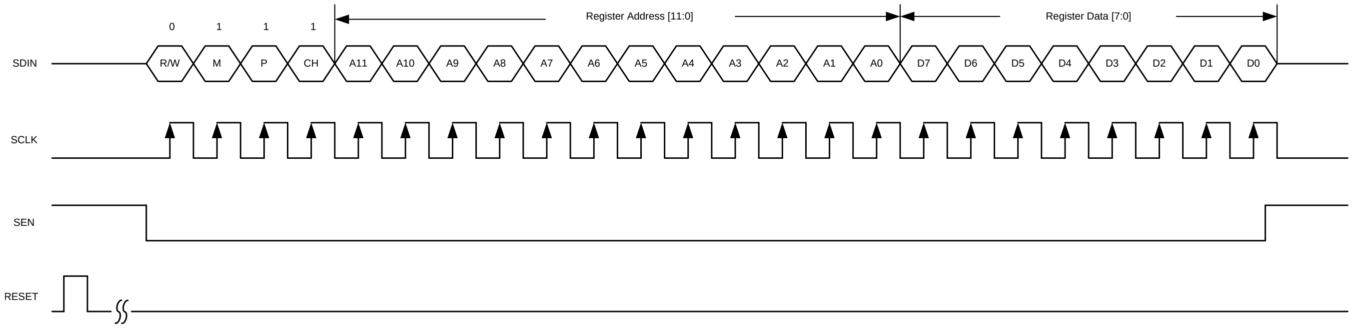



**Figure 139. SPI Write Timing Diagram for Digital Bank Register Write**

#### *8.4.3.4 Serial Register Readout: Digital Bank*

Readback of the register in one of the digital banks (as shown in Figure 140) can be accomplished by:

1. Driving the SEN pin low.
2. Selecting the page in the digital page: follow step 2 in the *Serial Register Write: Digital Bank* section.
3. Set the R/W, M, P, and CH bits to 1, and write the address to be read back.
4. Read back the register content on the SDOUT pin. When a page is selected, multiple read backs from the same page can be done.

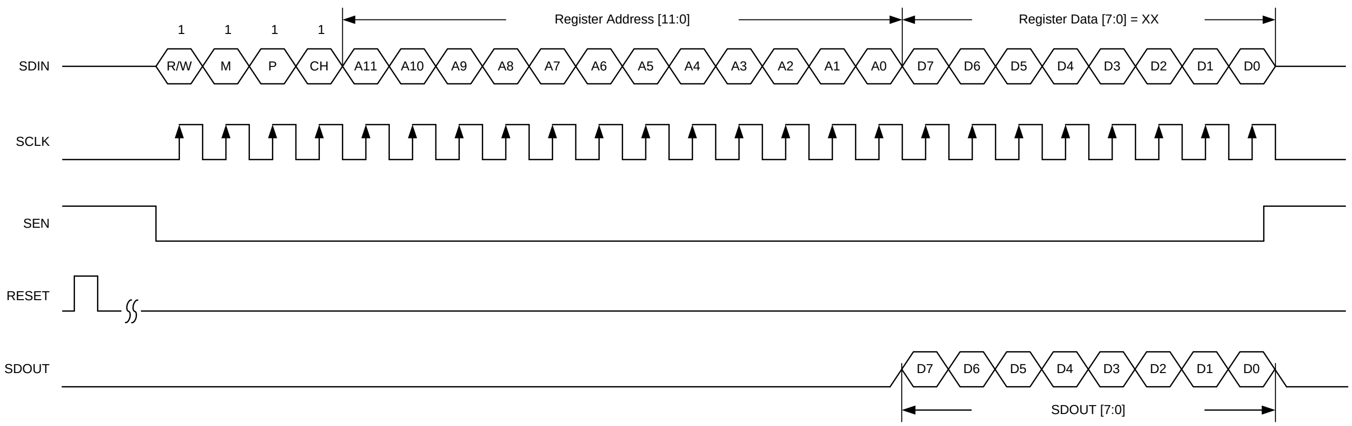



**Figure 140. SPI Read Timing Diagram for the Digital Bank**

#### *8.4.3.5 Serial Register Write: Decimation Filter and Power Detector Pages*

The decimation filter and power detector pages are special pages that accept direct addressing. The sampling clock and SYSREF signal are required to properly configure the decimation settings. Registers located in these pages can be programmed in one SPI cycle (Figure 141).

1. Drive the SEN pin low.
2. Directly write to the decimation filter or power detector pages. To program registers in these pages, set M = 1 and CH = 1. Additionally, address bit A[10] selects the decimation filter page (A[10] = 0) or the power detector page (A[10] = 1).
   - Decimation filter page: SPI cycle begins with 50xxh.
   - Power detector page: SPI cycle begins with 54xxh.

Example: Writing address 5001h with 02h selects the decimation filter page and programs a decimation factor of divide-by-8 (complex output).

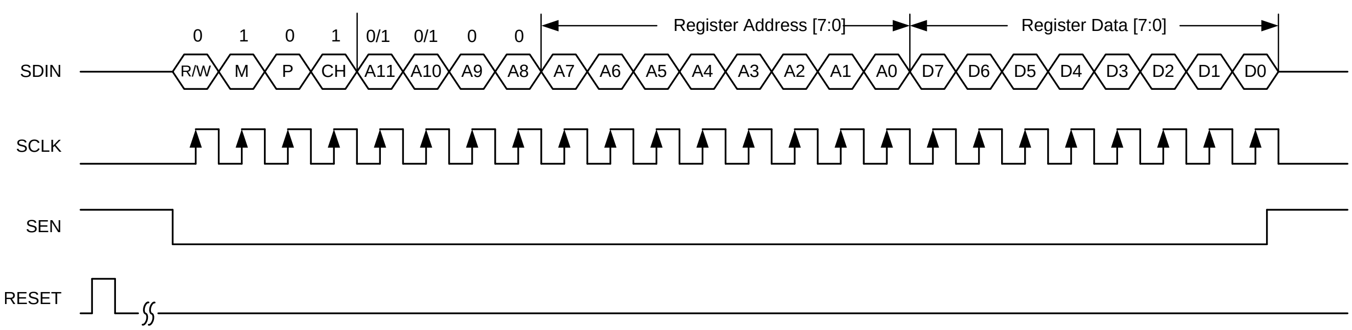
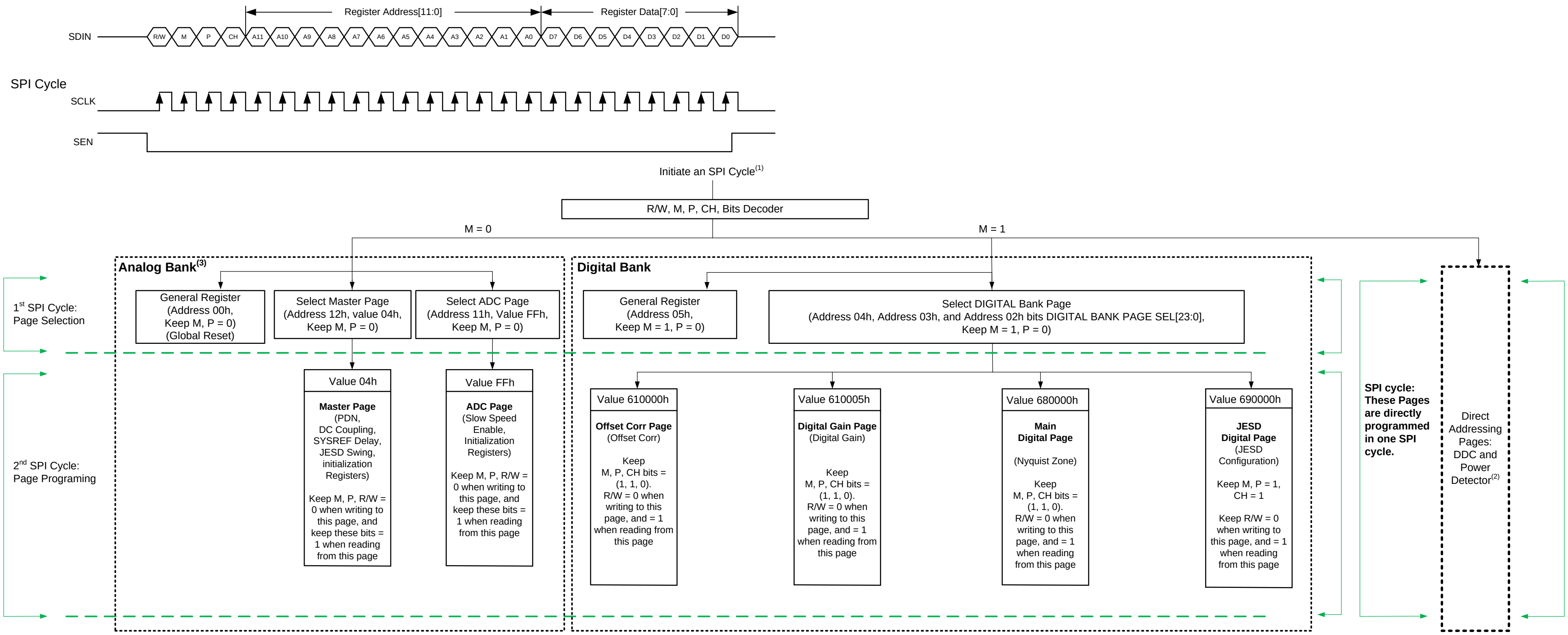



**Figure 141. SPI Write Timing Diagram for the Decimation and Power Detector Pages**

## 8.5 Register Maps

The ADC31RF80 contains two main SPI banks. The analog SPI bank provides access to the ADC core and the digital SPI bank controls the digital blocks (including the serial JESD interface). Figure 142 and Figure 143 provide a conceptual view of the SPI registers inside the ADC31RF80. The analog SPI bank contains the master and ADC pages. The digital SPI bank is divided into multiple pages (the main digital, digital gain, decimation filter, JESD digital, and power detector pages).



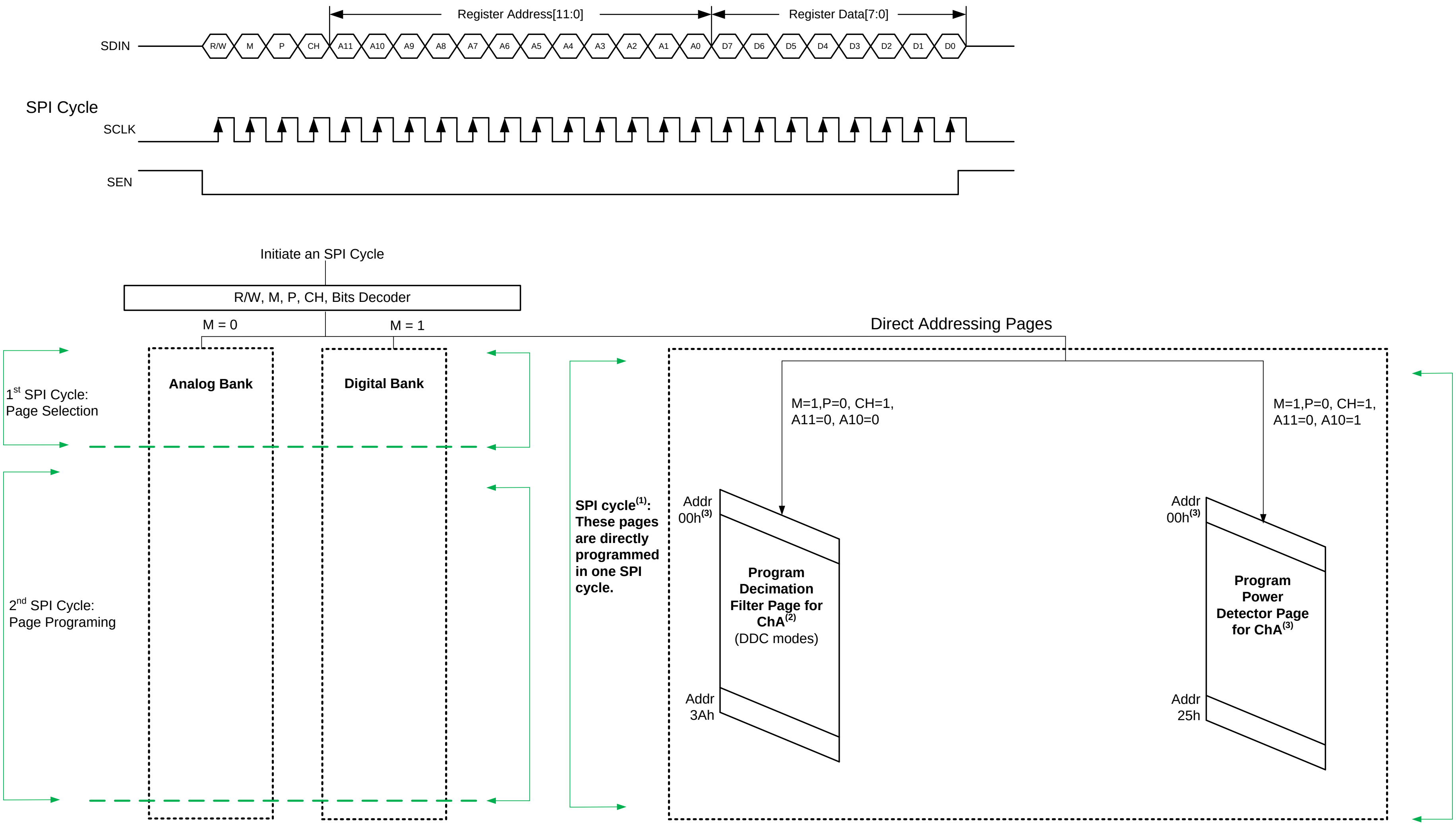

(1) In general, SPI writes are completed in two steps. The first step is to access the necessary page. The second step is to program the desired register in that page. When a page is accessed, the registers in that page can be programmed and read back multiple times.

(2) Registers in the decimation filter page and the power detector page can be directly programmed in one SPI cycle.

(3) The CH bit is a *don't care* bit and is recommended to be kept at 0.

**Figure 142. SPI Registers, Two-Step Addressing**

## Register Maps (continued)




(1) Registers in the decimation filter page and the power detector page can be directly programmed in one SPI cycle.
(2) To program registers in the decimation filter page.
(3) To program registers in power detector page.

**Figure 143. SPI Registers: Direct Addressing**

## Register Maps (continued)

Table 26 lists the register map for the ADC31RF80.

**Table 26. Register Map**

| REGISTER ADDRESS A[11:0] (Hex) | REGISTER DATA | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **GENERAL REGISTERS** | | | | | | | | |
| 000 | RESET | 0 | 0 | 0 | 0 | 0 | 0 | RESET |
| 002 | DIGITAL BANK PAGE SEL[7:0] | | | | | | | |
| 003 | DIGITAL BANK PAGE SEL[15:8] | | | | | | | |
| 004 | DIGITAL BANK PAGE SEL[23:16] | | | | | | | |
| 010 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3 or 4 WIRE |
| 011 | ADC PAGE SEL | | | | | | | |
| 012 | 0 | 0 | 0 | 0 | 0 | MASTER PAGE SEL | 0 | 0 |
| **MASTER PAGE (M = 0)** | | | | | | | | |
| 020 | 0 | 0 | 0 | PDN SYSREF | 0 | 0 | 0 | GLOBAL PDN |
| 032 | 0 | 0 | INCR CM IMPEDANCE | 0 | 0 | 0 | 0 | 0 |
| 039 | 0 | ALWAYS WRITE 1 | 0 | ALWAYS WRITE 1 | 0 | 0 | 0 | SYNC TERM DIS |
| 03C | 0 | SYSREF DEL EN | 0 | 0 | 0 | 0 | SYSREF DEL[4:3] | |
| 03D | 0 | 0 | 0 | 0 | 0 | JESD OUTPUT SWING | | |
| 05A | SYSREF DEL[2:0] | | | 0 | 0 | 0 | 0 | 0 |
| 057 | 0 | 0 | 0 | SEL SYSREF REG | ASSERT SYSREF REG | 0 | 0 | 0 |
| 058 | 0 | 0 | SYNCB POL | 0 | 0 | 0 | 0 | 0 |
| **ADC PAGE (FFh, M = 0)** | | | | | | | | |
| 03F | 0 | 0 | 0 | 0 | 0 | SLOW SP EN1 | 0 | 0 |
| 042 | 0 | 0 | 0 | SLOW SP EN2 | 0 | 0 | 1 | 1 |
| **Offset Corr Page (610000h, M = 1)** | | | | | | | | |
| 68 | FREEZE OFFSET CORR | ALWAYS WRITE 1 | 0 | 0 | 0 | DIS OFFSET CORR | ALWAYS WRITE 1 | 0 |
| **Digital Gain Page (610005, M = 1)** | | | | | | | | |
| 0A6 | 0 | 0 | 0 | 0 | DIGITAL GAIN | | | |

## Register Maps (continued)

### Table 26. Register Map (continued)

| REGISTER ADDRESS A[11:0] (Hex) | REGISTER DATA | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Main Digital Page (680000h, M = 1)** | | | | | | | | |
| 000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DIG CORE RESET GBL |
| 0A2 | 0 | 0 | 0 | 0 | NQ ZONE EN | NYQUIST ZONE | | |
| 0A5 | Sampling Frequency | | | | | | | |
| 0A9 | 0 | 0 | 0 | 0 | Sampling Frequency Enable | 0 | 1 | 1 |
| 0B0 | Band1 Lower-Edge Frequency LSB Setting | | | | | | | |
| 0B1 | 0 | 0 | 0 | Band1 Lower-Edge Frequency MSB Setting | | | | |
| 0B2 | Band1 Upper-Edge Frequency LSB Setting | | | | | | | |
| 0B3 | 0 | 0 | Band1 Frequency Range Enable | Band1 Upper-Edge Frequency MSB Setting | | | | |
| 0B4 | Band2 Lower-Edge Frequency LSB Setting | | | | | | | |
| 0B5 | 0 | 0 | 0 | Band2 Lower-Edge Frequency MSB Setting | | | | |
| 0B6 | Band2 Upper-Edge Frequency LSB Setting | | | | | | | |
| 0B7 | 0 | 0 | Band2 Frequency Range Enable | Band2 Upper-Edge Frequency MSB Setting | | | | |
| 0B8 | Band3 Lower-Edge Frequency LSB Setting | | | | | | | |
| 0B9 | 0 | 0 | 0 | Band3 Lower-Edge Frequency MSB Setting | | | | |
| 0BA | Band3 Upper-Edge Frequency LSB Setting | | | | | | | |
| 0BB | 0 | 0 | Band3 Frequency Range Enable | Band3 Upper-Edge Frequency MSB Setting | | | | |
| **JESD DIGITAL PAGE (690000h, M = 1)** | | | | | | | | |
| 001 | CTRL K | 0 | 0 | TESTMODE EN | 0 | LANE ALIGN | FRAME ALIGN | TX LINK DIS |
| 002 | SYNC REG | SYNC REG EN | 0 | 0 | 12BIT MODE | | JESD MODE0 | |
| 003 | LINK LAYER TESTMODE | | | LINK LAY RPAT | LMFC MASK RESET | JESD MODE1 | JESD MODE2 | RAMP 12BIT |
| 004 | 0 | 0 | 0 | 0 | 0 | 0 | REL ILA SEQ | |
| 006 | SCRAMBLE EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 007 | 0 | 0 | 0 | FRAMES PER MULTIFRAME (K) | | | | |
| 016 | 0 | 40X MODE | | | 0 | 0 | 0 | 0 |
| 017 | 0 | 0 | 0 | 0 | LANE0 POL | LANE1 POL | LANE2 POL | LANE3 POL |

## Register Maps (continued)

### Table 26. Register Map (continued)

| REGISTER ADDRESS A[11:0] (Hex) | REGISTER DATA | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 032 | SEL EMP LANE 0 | | | | | | 0 | 0 |
| 033 | SEL EMP LANE 1 | | | | | | 0 | 0 |
| 034 | SEL EMP LANE 2 | | | | | | 0 | 0 |
| 035 | SEL EMP LANE 3 | | | | | | 0 | 0 |
| 036 | 0 | CMOS SYNCB | 0 | 0 | 0 | 0 | 0 | 0 |
| 037 | 0 | 0 | 0 | 0 | 0 | 0 | PLL MODE | |
| 03C | 0 | 0 | 0 | 0 | 0 | 0 | 0 | EN CMOS SYNCB |
| 03E | 0 | MASK CLKDIV SYSREF | MASK NCO SYSREF | 0 | 0 | 0 | 0 | 0 |
| **DECIMATION FILTER PAGE (Direct Addressing, 16-Bit Address, 5000h)** | | | | | | | | |
| 000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDC EN |
| 001 | 0 | 0 | 0 | 0 | DECIM FACTOR | | | |
| 002 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DUAL BAND EN |
| 005 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | REAL OUT EN |
| 007 | DDC0 NCO1 LSB | | | | | | | |
| 008 | DDC0 NCO1 MSB | | | | | | | |
| 009 | DDC0 NCO2 LSB | | | | | | | |
| 00A | DDC0 NCO2 MSB | | | | | | | |
| 00B | DDC0 NCO3 LSB | | | | | | | |
| 00C | DDC0 NCO3 MSB | | | | | | | |
| 00D | DDC1 NCO4 LSB | | | | | | | |
| 00E | DDC1 NCO4 MSB | | | | | | | |
| 00F | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NCO SEL PIN |
| 010 | 0 | 0 | 0 | 0 | 0 | 0 | NCO SEL | |
| 011 | 0 | 0 | 0 | 0 | 0 | 0 | LMFC RESET MODE | |
| 014 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDC0 6DB GAIN |
| 016 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDC1 6DB GAIN |
| 01E | 0 | DDC DET LAT | | | 0 | 0 | 0 | 0 |
| 01F | 0 | 0 | 0 | 0 | 0 | 0 | 0 | WBF 6DB GAIN |
| 033 | CUSTOM PATTERN1[7:0] | | | | | | | |
| 034 | CUSTOM PATTERN1[15:8] | | | | | | | |

## Register Maps (continued)

### Table 26. Register Map (continued)

| REGISTER ADDRESS A[11:0] (Hex) | REGISTER DATA 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 035 | CUSTOM PATTERN2[7:0] | | | | | | | |
| 036 | CUSTOM PATTERN2[15:8] | | | | | | | |
| 037 | TEST PATTERN DDC1 Q-DATA | | | | TEST PATTERN DDC1 I-DATA | | | |
| 038 | TEST PATTERN DDC2 Q-DATA | | | | TEST PATTERN DDC2 I -DATA | | | |
| 039 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | USE COMMON TEST PATTERN |
| 03A | 0 | 0 | 0 | 0 | 0 | 0 | TEST PAT RES | TP RES EN |
| **POWER DETECTOR PAGE (Direct Addressing, 16-Bit Address, 5400h)** | | | | | | | | |
| 000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PKDET EN |
| 001 | BLKPKDET [7:0] | | | | | | | |
| 002 | BLKPKDET [15:8] | | | | | | | |
| 003 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLKPKDET [16] |
| 007 | BLKTHHH | | | | | | | |
| 008 | BLKTHHL | | | | | | | |
| 009 | BLKTHLH | | | | | | | |
| 00A | BLKTHLL | | | | | | | |
| 00B | DWELL[7:0] | | | | | | | |
| 00C | DWELL[15:8] | | | | | | | |
| 00D | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FILT0LPSEL |
| 00E | 0 | 0 | 0 | 0 | TIMECONST | | | |
| 00F | FIL0THH[7:0] | | | | | | | |
| 010 | FIL0THH[15:8] | | | | | | | |
| 011 | FIL0THL[7:0] | | | | | | | |
| 012 | FIL0THL[15:8] | | | | | | | |
| 013 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IIR0 2BIT EN |
| 016 | FIL1THH[7:0] | | | | | | | |
| 017 | FIL1THH[15:8] | | | | | | | |
| 018 | FIL1THL[7:0] | | | | | | | |
| 019 | FIL1THL[15:8] | | | | | | | |
| 01A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IIR1 2BIT EN |
| 01D | DWELLIIR[7:0] | | | | | | | |

## Register Maps (continued)

**Table 26. Register Map (continued)**

| REGISTER ADDRESS A[11:0] (Hex) | REGISTER DATA | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 01E | DWELLIIR[15:8] | | | | | | | |
| 020 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IIR0 2BIT EN |
| 021 | 0 | 0 | 0 | PWRDETACCU | | | | |
| 022 | PWRDETH[7:0] | | | | | | | |
| 023 | PWRDETH[15:8] | | | | | | | |
| 024 | PWRDETL[7:0] | | | | | | | |
| 025 | PWRDETL[15:8] | | | | | | | |
| 027 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RMS 2BIT EN |
| 02B | 0 | 0 | 0 | RESET AGC | 0 | 0 | 0 | 0 |
| 032 | OUTSEL GPIO4 | | | | | | | |
| 033 | OUTSEL GPIO1 | | | | | | | |
| 034 | OUTSEL GPIO3 | | | | | | | |
| 035 | OUTSEL GPIO2 | | | | | | | |
| 037 | 0 | 0 | 0 | 0 | IODIR GPIO2 | IODIR GPIO3 | IODIR GPIO1 | IODIR GPIO4 |
| 038 | 0 | 0 | INSEL1 | | 0 | 0 | INSEL0 | |

### 8.5.1 Example Register Writes

This section provides three different example register writes. Table 27 describes a global power-down register write, Table 28 describes the register writes when the scrambler is enabled, and Table 29 describes the register writes for 8x decimation (complex output, 1 DDC mode) with the NCO set to 1.8 GHz ($f_S$ = 3 GSPS) and the JESD format configured to LMFS = 4421.

**Table 27. Global Power-Down**

| ADDRESS | DATA | COMMENT |
|---|---|---|
| 12h | 04h | Set the master page |
| 20h | 01h | Set the global power-down |

**Table 28. Scrambler Enable**

| ADDRESS | DATA | COMMENT |
|---|---|---|
| 4004h | 69h | Select the digital JESD page |
| 4003h | 00h | |
| 6006h | 80h | Scrambler enable |

**Table 29. 8x Decimation**

| ADDRESS | DATA | COMMENT |
|---|---|---|
| 4004h | 68h | Select the main digital page |
| 4003h | 00h | |
| 6000h | 01h | Issue a digital reset |
| 6000h | 00h | Clear the digital reset |
| 4004h | 69h | Select the digital JESD page |
| 4003h | 00h | |
| 6002h | 01h | Set JESD MODE0 = 1 |
| 5000h | 01h | Enable the DDC |
| 5001h | 02h | Set decimation to 8x complex |
| 5007h | 9Ah | Set the LSB of DDC0, NCO1 to 9Ah ($f_{NCO}$ = 1.8 GHz, $f_S$ = 3 GSPS) |
| 5008h | 99h | Set the MSB of DDC0, NCO1 to 99h ($f_{NCO}$ = 1.8 GHz, $f_S$ = 3 GSPS) |
| 5014h | 01h | Enable the 6-dB digital gain of DDC0 |

### 8.5.2 Register Descriptions

Table 30 lists the access codes for the ADC31RF80 registers.

**Table 30. ADC31RF80 Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| R | R | Read |
| R-W | R/W | Read or Write |
| W | W | Write |
| *-n* | | Value after reset or the default value |

#### *8.5.2.1 General Registers*

##### 8.5.2.1.1 Register 000h (address = 000h), General Registers

**Figure 144. Register 000h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | RESET |
| R/W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 31. Register 000h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESET | R/W | 0h | 0 = Normal operation<br>1 = Internal software reset, clears back to 0 |
| 6-1 | 0 | W | 0h | Must write 0 |
| 0 | RESET | R/W | 0h | 0 = Normal operation (1)<br>1 = Internal software reset, clears back to 0 |

(1) Both bits (7, 0) must be set simultaneously to perform a reset.

##### 8.5.2.1.2 Register 002h (address = 002h), General Registers

**Figure 145. Register 002h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DIGITAL BANK PAGE SEL[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Table 32. Register 002h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DIGITAL BANK PAGE SEL[7:0] | R/W | 0h | Program the JESD BANK PAGE SEL[23:0] bits to access the desired page in the JESD bank.<br>680000h = Main digital page<br>610000h = Digital function page<br>690000h = JESD digital page selected |

#### 8.5.2.1.3 Register 003h (address = 003h), General Registers

**Figure 146. Register 003h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DIGITAL BANK PAGE SEL[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Table 33. Register 003h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DIGITAL BANK PAGE SEL[15:8] | R/W | 0h | Program the JESD BANK PAGE SEL[23:0] bits to access the desired page in the JESD bank.<br>680000h = Main digital page<br>610000h = Digital function page<br>690000h = JESD digital page selected |

#### 8.5.2.1.4 Register 004h (address = 004h), General Registers

**Figure 147. Register 004h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DIGITAL BANK PAGE SEL[23:16] | | | | | | | |
| R/W-0h | | | | | | | |

**Table 34. Register 004h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DIGITAL BANK PAGE SEL[23:16] | R/W | 0h | Program the JESD BANK PAGE SEL[23:0] bits to access the desired page in the JESD bank.<br>680000h = Main digital page<br>610000h = Digital function page<br>690000h = JESD digital page selected |

#### 8.5.2.1.5 Register 010h (address = 010h), General Registers

**Figure 148. Register 010h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3 or 4 WIRE |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 35. Register 010h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | 3 or 4 WIRE | R/W | 0h | 0 = 4-wire SPI (default)<br>1 = 3-wire SPI where SDIN become input or output |

#### 8.5.2.1.6 Register 011h (address = 011h), General Registers

**Figure 149. Register 011h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADC PAGE SEL | | | | | | | |
| R/W-0h | | | | | | | |

**Table 36. Register 011h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | ADC PAGE SEL | R/W | 0h | 00000000 = Normal operation, ADC page is not selected<br>11111111 = ADC page is selected; MASTER PAGE SEL must be set to 0 |

#### 8.5.2.1.7 Register 012h (address = 012h), General Registers

**Figure 150. Register 012h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | MASTER PAGE SEL | 0 | 0 |
| W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | W-0h | W-0h |

**Table 37. Register 012h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | W | 0h | Must write 0 |
| 2 | MASTER PAGE SEL | R/W | 0h | 0 = Normal operation<br>1 = Selects the master page address; ADC PAGE must be set to 0 |
| 1-0 | 0 | W | 0h | Must write 0 |

### 8.5.3 Master Page (M = 0)

#### *8.5.3.1 Register 020h (address = 020h), Master Page*

**Figure 151. Register 020h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | PDN SYSREF | 0 | 0 | 0 | GLOBAL PDN |
| W-0h | W-0h | W-0h | R/W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 38. Register 020h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | W | 0h | Must write 0 |
| 4 | PDN SYSREF | R/W | 0h | This bit powers down the SYSREF input buffer.<br>0 = Normal operation<br>1 = SYSREF input capture buffer is powered down and further SYSREF input pulses are ignored |
| 3-1 | 0 | W | 0h | Must write 0 |
| 0 | GLOBAL PDN | R/W | 0h | This bit enables the global power-down.<br>0 = Normal operation<br>1 = Global power-down enabled |

#### *8.5.3.2 Register 032h (address = 032h), Master Page*

**Figure 152. Register 032h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | INCR CM IMPEDANCE | 0 | 0 | 0 | 0 | 0 |
| W-0h | W-0h | R/W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

**Table 39. Register 032h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | W | 0h | Must write 0 |
| 5 | INCR CM IMPEDANCE | R/W | 0h | Only use this bit when analog inputs are dc-coupled to the driver.<br>0 = VCM buffer directly drives the common point of biasing resistors.<br>1 = VCM buffer drives the common point of biasing resistors with > 5 kΩ |
| 4-0 | 0 | W | 0h | Must write 0 |

### 8.5.3.3 Register 039h (address = 039h), Master Page

**Figure 153. Register 039h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | ALWAYS WRITE 1 | 0 | ALWAYS WRITE 1 | 0 | 0 | 0 | SYNC TERM DIS |
| W-0h | R/W-0h | W-0h | R/W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 40. Register 039h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | W | 0h | Must write 0 |
| 6 | ALWAYS WRITE 1 | R/W | 0h | Always set this bit to 1 |
| 5 | 0 | W | 0h | Must write 0 |
| 4 | ALWAYS WRITE 1 | R/W | 0h | Always set this bit to 1 |
| 3-1 | 0 | W | 0h | Must write 0 |
| 0 | SYNC TERM DIS | R/W | 0h | This bit disables the on-chip, 100-Ω termination resistors on the SYNCB input.<br>0 = On-chip, 100-Ω termination enabled<br>1 = On-chip, 100-Ω termination disabled |

### 8.5.3.4 Register 03Ch (address = 03Ch), Master Page

**Figure 154. Register 03Ch**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SYSREF DEL EN | 0 | 0 | 0 | 0 | SYSREF DEL[4:3] | |
| W-0h | R/W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | |

**Table 41. Register 03Ch Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | W | 0h | Must write 0 |
| 6 | SYSREF DEL EN | R/W | 0h | This bit allows an internal delay to be added to the SYSREF input.<br>0 = SYSREF delay disabled<br>1 = SYSREF delay enabled through register settings [3Ch (bits 1-0), 5Ah (bits 7-5)] |
| 5-2 | 0 | W | 0h | Must write 0 |
| 1-0 | SYSREF DEL[4:3] | R/W | 0h | When the SYSREF delay feature is enabled (3Ch, bit 6) the delay can be adjusted in 25-ps steps; the first step is 175 ps. The PVT variation of each 25-ps step is ±10 ps. The 175-ps step is ±50 ps; see Table 43. |

### 8.5.3.5 Register 05Ah (address = 05Ah), Master Page

**Figure 155. Register 05Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SYSREF DEL[2:0] | | | 0 | 0 | 0 | 0 | 0 |
| R/W-0h | | | W-0h | W-0h | W-0h | W-0h | W-0h |

**Table 42. Register 05Ah Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SYSREF DEL2 | R/W | 0h | When the SYSREF delay feature is enabled (3Ch, bit 6) the delay can be adjusted in 25-ps steps; the first step is 175 ps. The PVT variation of each 25-ps step is ±10 ps. The 175-ps step is ±50 ps; see Table 43. |
| 6 | SYSREF DEL1 | | | |
| 5 | SYSREF DEL0 | | | |
| 4-0 | 0 | W | 0h | Must write 0 |

**Table 43. SYSREF DEL[2:0] Bit Settings**

| STEP | SETTING | STEP (NOM) | TOTAL DELAY (NOM) |
|---|---|---|---|
| 1 | 01000 | 175 ps | 175 ps |
| 2 | 00111 | 25 ps | 200 ps |
| 3 | 00110 | 25 ps | 225 ps |
| 4 | 00101 | 25 ps | 250 ps |
| 5 | 00100 | 25 ps | 275 ps |
| 6 | 00011 | 25 ps | 300 ps |

### 8.5.3.6 Register 03Dh (address = 3Dh), Master Page

**Figure 156. Register 03Dh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | JESD OUTPUT SWING | | |
| W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | | |

**Table 44. Register 03Dh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | W | 0h | Must write 0 |
| 2-0 | JESD OUTPUT SWING | R/W | 0h | These bits select the output amplitude, $V_{OD}$ ($mV_{PP}$), of the JESD transmitter for all lanes.<br>0 = 860 $mV_{PP}$<br>1= 810 $mV_{PP}$<br>2 = 770 $mV_{PP}$<br>3 = 745 $mV_{PP}$<br>4 = 960 $mV_{PP}$<br>5 = 930 $mV_{PP}$<br>6 = 905 $mV_{PP}$<br>7 = 880 $mV_{PP}$ |

#### 8.5.3.7 Register 057h (address = 057h), Master Page

**Figure 157. Register 057h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | SEL SYSREF REG | ASSERT SYSREF REG | 0 | 0 | 0 |
| W-0h | W-0h | W-0h | R/W-0h | R/W-0h | W-0h | W-0h | W-0h |

**Table 45. Register 057h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | W | 0h | Must write 0 |
| 4 | SEL SYSREF REG | R/W | 0h | SYSREF can be asserted using this bit. Ensure that the SEL SYSREF REG register bit is set high before using this bit; see Using SYSREF .<br>0 = SYSREF is logic low<br>1 = SYSREF is logic high |
| 3 | ASSERT SYSREF REG | R/W | 0h | Set this bit to use the SPI register to assert SYSREF.<br>0 = SYSREF is asserted by device pins<br>1 = SYSREF can be asserted by the ASSERT SYSREF REG register bit<br>Other bits = 0 |
| 2-0 | 0 | W | 0h | Must write 0 |

#### 8.5.3.8 Register 058h (address = 058h), Master Page

**Figure 158. Register 058h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | SYNCB POL | 0 | 0 | 0 | 0 | 0 |
| W-0h | W-0h | R/W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

**Table 46. Register 058h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | W | 0h | Must write 0 |
| 5 | SYNCB POL | R/W | 0h | This bit inverts the SYNCB polarity.<br>0 = Polarity is not inverted; this setting matches the timing diagrams in this document and is the proper setting to use<br>1 = Polarity is inverted |
| 4-0 | 0 | W | 0h | Must write 0 |

### 8.5.4 ADC Page (FFh, M = 0)

#### *8.5.4.1 Register 03Fh (address = 03Fh), ADC Page*

**Figure 159. Register 03Fh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | SLOW SP EN1 | 0 | 0 |
| W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | W-0h | W-0h |

**Table 47. Register 03Fh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | W | 0h | Must write 0 |
| 2 | SLOW SP EN1 | R/W | 0h | This bit must be enabled for clock rates below 2.5 GSPS.<br>0 = ADC sampling rates are faster than 2.5 GSPS<br>1 = ADC sampling rates are slower than 2.5 GSPS |
| 1-0 | 0 | W | 0h | Must write 0 |

#### *8.5.4.2 Register 042h (address = 042h), ADC Page*

**Figure 160. Register 042h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | SLOW SP EN2 | 0 | 0 | 1 | 1 |
| W-0h | W-0h | W-0h | R/W-0h | W-0h | W-0h | R/W-0h | R/W-0h |

**Table 48. Register 042h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | W | 0h | Must write 0 |
| 4 | SLOW SP EN2 | R/W | 0h | This bit must be enabled for clock rates below 2.5 GSPS.<br>0 = ADC sampling rates are faster than 2.5 GSPS<br>1 = ADC sampling rates are slower than 2.5 GSPS |
| 3-2 | 0 | W | 0h | Must write 0 |
| 1-0 | 1 | R/W | 0h | Must write 1 |

### 8.5.5 Digital Function Page (610000h, M = 1)

#### *8.5.5.1 Register A6h (address = 0A6h), Digital Function Page*

**Figure 161. Register 0A6h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DIG GAIN | | | |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | | | |

**Table 49. Register 0A6h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3-0 | DIG GAIN | R/W | 0h | These bits set the digital gain of the ADC output data prior to decimation up to 11 dB; see Table 50. |

**Table 50. DIG GAIN Bit Settings**

| SETTING | DIGITAL GAIN |
|---|---|
| 0000 | 0 dB |
| 0001 | 1 dB |
| 0010 | 2 dB |
| … | … |
| 1010 | 10 dB |
| 1011 | 11 dB |

### 8.5.6 Offset Corr Page (610000h, M = 1)

#### *8.5.6.1 Register 034h (address = 034h), Offset Corr Page*

**Figure 162. Register 034h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SEL EXT EST |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 51. Register 034h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | SEL EXT EST | R/W | 0h | This bit selects the external estimate for the offset correction block; see the *Using DC Coupling in the ADC31RF80* section. |

### 8.5.6.2 Register 068h (address = 068h), Offset Corr Page

**Figure 163. Register 068h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FREEZE OFFSET CORR | ALWAYS WRITE 1 | 0 | 0 | 0 | DIS OFFSET CORR | ALWAYS WRITE 1 | 0 |
| R/W-0h | R/W-0h | W-0h | W-0h | W-0h | R/W-0h | R/W-0h | W-0h |

**Table 52. Register 068h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | FREEZE OFFSET CORR | R/W | 0h | Use this bit and bits 5 and 1 to freeze the offset estimation process of the offset corrector; see the *Using DC Coupling in the ADC31RF80* section.<br>011 = Apply this setting after powering up the device<br>111 = Offset corrector is frozen, does not estimate offset anymore, and applies the last computed value.<br>Others = Do not use |
| 6 | ALWAYS WRITE 1 | R/W | 0h | Always write this bit as 1 for the offset correction block to work properly. |
| 5-3 | 0 | W | 0h | Must write 0 |
| 2 | DIS OFFSET CORR | R/W | 0h | 0 = Offset correction block works and removes $f_S$ / 8, $f_S$ / 4, $3f_S$ / 8, and $f_S$ / 2 spurs<br>1 = Offset correction block is disabled |
| 1 | ALWAYS WRITE 1 | R/W | 0h | Always write this bit as 1 for the offset correction block to work properly. |
| 0 | 0 | W | 0h | Must write 0 |

### 8.5.7 Digital Gain Page (610005h, M = 1)

#### *8.5.7.1 Register 0A6h (address = 0A6h), Digital Gain Page*

**Figure 164. Register 0A6h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DIGITAL GAIN | | | |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | | | |

**Table 53. Register 0A6h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3-0 | DIGITAL GAIN | R/W | 0h | These bits apply a digital gain to the ADC data (before the DDC) up to 11 dB.<br>0000 = Default<br>0001 = 1 dB<br>1011 = 11 dB<br>Others = Do not use |

### 8.5.8 Main Digital Page (680000h, M = 1)

#### *8.5.8.1 Register 000h (address = 000h), Main Digital Page*

**Figure 165. Register 000h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | DIG CORE RESET GBL |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 54. Register 000h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | DIG CORE RESET GBL | R/W | 0h | Pulse this bit (0 →1 →0) to reset the digital core.<br>All Nyquist zone settings take effect when this bit is pulsed. |

#### 8.5.8.2 Register 0A2h (address = 0A2h), Main Digital Page

**Figure 166. Register 0A2h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | NQ ZONE EN | NYQUIST ZONE | | |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | R/W-0h | | |

**Table 55. Register 0A2h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3 | NQ ZONE EN | R/W | 0h | This bit allows for specification of the operating Nyquist zone.<br>0 = Nyquist zone specification disabled<br>1 = Nyquist zone specification enabled |
| 2-0 | NYQUIST ZONE | R/W | 0h | These bits specify the operating Nyquist zone for the analog correction loop.<br>Set the NQ ZONE EN bit before programming these bits.<br>For example, at s 3-GSPS chip clock, the first Nyquist zone is from dc to 1.5 GHz, the second Nyquist zone is from 1.5 GHz to 3 GHz, and so on.<br>000 = First Nyquist zone (dc – $f_S$ / 2)<br>001 = Second Nyquist zone ($f_S$ / 2 – $f_S$)<br>010 = Third Nyquist zone<br>011 = Fourth Nyquist zone |

### 8.5.8.3 Register 0A5h (address = 0A5h), Main Digital Page

**Figure 167. Register 0A5h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Sampling Frequency | | | | | | | |
| R/W-0h | | | | | | | |

**Table 56. Register 0A5h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | Sampling Frequency | R/W | 0h | These bits specify the ADC sampling frequency .<br>Value = $f_S$ / 24; for example, if $f_S$ = 3000 MSPS, then value = round (3000 / 24) = 125. |

### 8.5.8.4 Register 0A9h (address = 0A9h), Main Digital Page

**Figure 168. Register 0A9h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Sampling Frequency Enable | 0 | 1 | 1 |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | W-0h | R/W-0h | R/W-0h |

**Table 57. Register 0A9h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3 | Sampling Frequency Enable | R/W | 0h | This bit allows for specification of operating sampling frequency.<br>0 = Sampling frequency specification disabled<br>1 = Sampling frequency specification enabled |
| 2 | 0 | W | 0h | Must write 0 |
| 1-0 | 1 | R/W | 0h | Must write 0 |

### 8.5.8.5 Register 0B0h (address = 0B0h), Main Digital Page

**Figure 169. Register 0B0h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Band1 Lower-Edge Frequency LSB Setting | | | | | | | |
| R/W-0h | | | | | | | |

**Table 58. Register 0B0h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | Band1 Lower-Edge Frequency LSB Setting | R/W | 0h | These bits specify the lower edge of the Band1 frequency (LSB 8-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz<br>The absolute frequency values should be entered here and not the aliased frequency values. |

### 8.5.8.6 Register 0B1h (address = 0B1h), Main Digital Page

**Figure 170. Register 0B1h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Band1 Lower-Edge Frequency MSB Setting | | | | |
| W-0h | W-0h | W-0h | R/W-0h | | | | |

**Table 59. Register 0B1h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | W | 0h | Must write 0 |
| 4-0 | Band1 Lower-Edge Frequency MSB Setting | R/W | 0h | These bits specify the lower edge of the Band1 frequency (MSB 5-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz |

### 8.5.8.7 Register 0B2h (address = 0B2h), Main Digital Page

**Figure 171. Register 0B2h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Band1 Upper-Edge Frequency LSB Setting | | | | | | | |
| R/W-0h | | | | | | | |

**Table 60. Register 0B2h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | Band1 Upper-Edge Frequency LSB Setting | R/W | 0h | These bits specify the upper edge of the Band1 frequency (LSB 8-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz<br>The absolute frequency values should be entered here and not the aliased frequency values. |

### 8.5.8.8 Register 0B3h (address = 0B3h), Main Digital Page

**Figure 172. Register 0B3h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | Band1 Frequency Range Enable | Band1 Upper-edge Frequency MSB setting | | | | |
| W-0h | W-0h | R/W-0h | R/W-0h | | | | |

**Table 61. Register 0B3h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | W | 0h | Must write 0 |
| 5 | Band1 Frequency Range Enable | R/W | 0h | This bit enables the Band1 frequency range settings.<br>The lower and upper frequency edge specifications for Band1 are used only if this bit is set to 1. |
| 4-0 | Band1 Upper-Edge Frequency MSB Setting | R/W | 0h | These bits specify the upper edge of the Band1 frequency (MSB 5-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz |

### 8.5.8.9 Register 0B4h (address = 0B4h), Main Digital Page

**Figure 173. Register 0B4h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Band2 Lower-Edge Frequency LSB Setting | | | | | | | |
| R/W-0h | | | | | | | |

**Table 62. Register 0B4h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | Band2 Lower-Edge Frequency LSB Setting | R/W | 0h | These bits specify the lower edge of the Band2 frequency (LSB 8-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz<br>The absolute frequency values should be entered here and not the aliased frequency values. |

### 8.5.8.10 Register 0B5h (address = 0B5h), Main Digital Page

**Figure 174. Register 0B5h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Band2 Lower-Edge Frequency MSB Setting | | | | |
| W-0h | W-0h | W-0h | R/W-0h | | | | |

**Table 63. Register 0B5h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | W | 0h | Must write 0 |
| 4-0 | Band2 Lower-Edge Frequency MSB Setting | R/W | 0h | These bits specify the lower edge of the Band2 frequency (MSB 5-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz |

### 8.5.8.11 Register 0B6h (address = 0B6h), Main Digital Page

**Figure 175. Register 0B6h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Band2 Upper-Edge Frequency LSB Setting | | | | | | | |
| R/W-0h | | | | | | | |

**Table 64. Register 0B6h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | Band2 Upper-Edge Frequency LSB Setting | R/W | 0h | These bits specify the upper edge of the Band2 frequency (LSB 8-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz<br>The absolute frequency values should be entered here and not the aliased frequency values. |

### 8.5.8.12 Register 0B7h (address = 0B7h), Main Digital Page

**Figure 176. Register 0B7h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | Band2 Frequency Range Enable | Band2 Upper-Edge Frequency MSB Setting | | | | |
| W-0h | W-0h | R/W-0h | R/W-0h | | | | |

**Table 65. Register 0B7h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | W | 0h | Must write 0 |
| 5 | Band2 Frequency Range Enable | R/W | 0h | This bit enables the Band2 frequency range settings.<br>The lower and upper frequency edge specifications for Band2 are used only if this bit is set to 1. |
| 4-0 | Band2 Upper-Edge Frequency MSB Setting | R/W | 0h | These bits specify the upper edge of the Band2 frequency (MSB 5-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz |

#### 8.5.8.13 Register 0B8h (address = 0B8h), Main Digital Page

**Figure 177. Register 0B8h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Band3 Lower-Edge Frequency LSB Setting | | | | | | | |
| R/W-0h | | | | | | | |

**Table 66. Register 0B8h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | Band3 Lower-Edge Frequency LSB Setting | R/W | 0h | These bits specify the lower edge of the Band3 frequency (LSB 8-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz<br>The absolute frequency values should be entered here and not the aliased frequency values. |

#### 8.5.8.14 Register 0B9h (address = 0B9h), Main Digital Page

**Figure 178. Register 0B9h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Band3 Lower-Edge Frequency MSB Setting | | | | |
| W-0h | W-0h | W-0h | R/W-0h | | | | |

**Table 67. Register 0B9h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | W | 0h | Must write 0 |
| 4-0 | Band3 Lower-Edge Frequency MSB Setting | R/W | 0h | These bits specify the lower edge of the Band3 frequency (MSB 5-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz |

### 8.5.8.15 Register 0BAh (address = 0BAh), Main Digital Page

**Figure 179. Register 0BAh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Band3 Upper-Edge Frequency LSB Setting | | | | | | | |
| R/W-0h | | | | | | | |

**Table 68. Register 0BAh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | Band3 Upper-Edge Frequency LSB Setting | R/W | 0h | These bits specify the upper edge of the Band3 frequency (LSB 8-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz<br>The absolute frequency values should be entered here and not the aliased frequency values. |

### 8.5.8.16 Register 0BBh (address = 0BBh), Main Digital Page

**Figure 180. Register 0BBh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | Band3 Frequency Range Enable | Band3 Upper-edge Frequency MSB setting | | | | |
| W-0h | W-0h | R/W-0h | R/W-0h | | | | |

**Table 69. Register 0BBh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | W | 0h | Must write 0 |
| 5 | Band3 Frequency Range Enable | R/W | 0h | This bit enables the Band3 frequency range settings.<br>The lower and upper frequency edge specifications for Band3 are used only if this bit is set to 1. |
| 4-0 | Band3 Upper-Edge Frequency MSB Setting | R/W | 0h | These bits specify the upper edge of the Band3 frequency (MSB 5-bit settings).<br>1 LSB = 1 MHz<br>Range = 8191 MHz |

### 8.5.9 JESD Digital Page (6900h, M = 1)

#### *8.5.9.1 Register 001h (address = 001h), JESD Digital Page*

**Figure 181. Register 001h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CTRL K | 0 | 0 | TESTMODE EN | 0 | LANE ALIGN | FRAME ALIGN | TX LINK DIS |
| R/W-0h | W-0h | W-0h | R/W-0h | W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 70. Register 001h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CTRL K | R/W | 0h | This bit is the enable bit for the number of frames per multiframe.<br>0 = Default is five frames per multiframe<br>1 = Frames per multiframe can be set in register 07h |
| 6-5 | 0 | W | 0h | Must write 0 |
| 4 | TESTMODE EN | R/W | 0h | This bit generates a long transport layer test pattern mode according to section 5.1.6.3 of the JESD204B specification.<br>0 = Test mode disabled<br>1 = Test mode enabled |
| 3 | 0 | W | 0h | Must write 0 |
| 2 | LANE ALIGN | R/W | 0h | This bit inserts a lane alignment character (K28.3) for the receiver to align to the lane boundary per section 5.3.3.5 of the JESD204B specification.<br>0 = Normal operation<br>1 = Inserts lane alignment characters |
| 1 | FRAME ALIGN | R/W | 0h | This bit inserts a frame alignment character (K28.7) for the receiver to align to the frame boundary per section 5.3.35 of the JESD204B specification.<br>0 = Normal operation<br>1 = Inserts frame alignment characters |
| 0 | TX LINK DIS | R/W | 0h | This bit disables sending the initial link alignment (ILA) sequence when SYNC is deasserted.<br>0 = Normal operation<br>1 = ILA disabled |

#### 8.5.9.2 Register 002h (address = 002h ), JESD Digital Page

**Figure 182. Register 002h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SYNC REG | SYNC REG EN | 0 | 0 | 12BIT MODE | | JESD MODE0 | |
| R/W-0h | R/W-0h | W-0h | W-0h | R/W-0h | | R/W-0h | |

**Table 71. Register 002h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SYNC REG | R/W | 0h | This bit provides SYNC control through the SPI.<br>0 = Normal operation<br>1 = ADC output data are replaced with K28.5 characters |
| 6 | SYNC REG EN | R/W | 0h | This bit is the enable bit for SYNC control through the SPI.<br>0 = Normal operation<br>1 = SYNC control through the SPI is enabled (ignores the SYNCB input pins) |
| 5-4 | 0 | W | 0h | Must write 0 |
| 3-2 | 12BIT MODE | R/W | 0h | This bit enables the 12-bit output mode for more efficient data packing.<br>00 = Normal operation, 14-bit output<br>01, 10 = Unused<br>11 = High-efficient data packing enabled |
| 1-0 | JESD MODE0 | R/W | 0h | These bits select the configuration register to configure the correct LMFS frame assemblies for different decimation settings; see the JESD frame assembly tables in the *JESD204B Frame Assembly* section.<br>00 = 0<br>01 = 1<br>10 = 2<br>11 = 3 |

#### 8.5.9.3 Register 003h (address = 003h), JESD Digital Page

**Figure 183. Register 003h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LINK LAYER TESTMODE | | | LINK LAY RPAT | LMFC MASK RESET | JESD MODE1 | JESD MODE2 | RAMP 12BIT |
| R/W-0h | | | R/W-0h | R/W-0h | R/W-1h | R/W-0h | R/W-0h |

**Table 72. Register 003h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | LINK LAYER TESTMODE | R/W | 0h | These bits generate a pattern according to section 5.3.3.8.2 of the JESD204B document.<br>000 = Normal ADC data<br>001 = D21.5 (high-frequency jitter pattern)<br>010 = K28.5 (mixed-frequency jitter pattern)<br>011 = Repeat initial lane alignment (generates a K28.5 character and repeats lane alignment sequences continuously)<br>100 = 12-octet RPAT jitter pattern |
| 4 | LINK LAY RPAT | R/W | 0h | This bit changes the running disparity in a modified RPAT pattern test mode (only when link layer test mode = 100).<br>0 = Normal operation<br>1 = Changes disparity |
| 3 | LMFC MASK RESET | R/W | 0h | 0 = Normal operation |
| 2 | JESD MODE1 | R/W | 1h | These bits select the configuration register to configure the correct LMFS frame assemblies for different decimation settings; see the JESD frame assembly tables in the *JESD204B Frame Assembly* section |
| 1 | JESD MODE2 | R/W | 0h | These bits select the configuration register to configure the correct LMFS frame assemblies for different decimation settings; see the JESD frame assembly tables in the *JESD204B Frame Assembly* section |
| 0 | RAMP 12BIT | R/W | 0h | 12-bit RAMP test pattern.<br>0 = Normal data output<br>1 = Digital output is the RAMP pattern |

#### 8.5.9.4 Register 004h (address = 004h), JESD Digital Page

**Figure 184. Register 004h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | REL ILA SEQ | |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | |

**Table 73. Register 004h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1-0 | REL ILA SEQ | R/W | 0h | These bits delay the generation of the lane alignment sequence by 0, 1, 2, or 3 multiframes after the code group synchronization.<br>00 = 0 multiframe delays<br>01 = 1 multiframe delay<br>10 = 2 multiframe delays<br>11 = 3 multiframe delays |

#### 8.5.9.5 Register 006h (address = 006h), JESD Digital Page

**Figure 185. Register 006h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCRAMBLE EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

**Table 74. Register 006h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SCRAMBLE EN | R/W | 0h | This bit is the scramble enable bit in the JESD204B interface.<br>0 = Scrambling disabled<br>1 = Scrambling enabled |
| 6-0 | 0 | W | 0h | Must write 0 |

#### 8.5.9.6 Register 007h (address = 007h), JESD Digital Page

**Figure 186. Register 007h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | FRAMES PER MULTIFRAME (K) | | | | |
| W-0h | W-0h | W-0h | R/W-0h | | | | |

**Table 75. Register 007h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | W | 0h | Must write 0 |
| 4-0 | FRAMES PER MULTIFRAME (K) | R/W | 0h | These bits set the number of multiframes.<br>Actual K is the value in hex + 1 (that is, 0Fh is K = 16). |

#### 8.5.9.7 Register 016h (address = 016h), JESD Digital Page

**Figure 187. Register 016h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 40x MODE | | | 0 | 0 | 0 | 0 |
| W-0h | R/W-0h | | | W-0h | W-0h | W-0h | W-0h |

**Table 76. Register 016h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | W | 0h | Must write 0 |
| 6-4 | 40x MODE | R/W | 0h | This register must be set for 40x mode operation.<br>000 = Register is set for 20x and 80x mode<br>111 = Register must be set for 40x mode |
| 3-0 | 0 | W | 0h | Must write 0 |

### 8.5.9.8 Register 017h (address = 017h), JESD Digital Page

**Figure 188. Register 017h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Lane0 POL | Lane1 POL | Lane2 POL | Lane3 POL |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 77. Register 017h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3-0 | Lane[3:0] POL | R/W | 0h | These bits set the polarity of the individual JESD output lanes.<br>0 = Polarity as given in the pinout (noninverted)<br>1 = Inverts polarity (positive, P, or negative, M) |

### 8.5.9.9 Register 032h-035h (address = 032h-035h), JESD Digital Page

**Figure 189. Register 032h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SEL EMP LANE 0 | | | | | | 0 | 0 |
| R/W-0h | | | | | | W-0h | W-0h |

**Figure 190. Register 033h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SEL EMP LANE 1 | | | | | | 0 | 0 |
| R/W-0h | | | | | | W-0h | W-0h |

**Figure 191. Register 034h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SEL EMP LANE 2 | | | | | | 0 | 0 |
| R/W-0h | | | | | | W-0h | W-0h |

**Figure 192. Register 035h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SEL EMP LANE 3 | | | | | | 0 | 0 |
| R/W-0h | | | | | | W-0h | W-0h |

**Table 78. Register 032h-035h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | SEL EMP LANE | R/W | 0h | These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period.<br>0 = 0 dB<br>1 = –1 dB<br>3 = –2 dB<br>7 = –4.1 dB<br>15 = –6.2 dB<br>31 = –8.2 dB<br>63 = –11.5 dB |
| 1-0 | 0 | W | 0h | Must write 0 |

### 8.5.9.10 Register 036h (address = 036h), JESD Digital Page

**Figure 193. Register 036h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | CMOS SYNCB | 0 | 0 | 0 | 0 | 0 | 0 |
| W-0h | R/W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

**Table 79. Register 036h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | W | 0h | Must write 0 |
| 6 | CMOS SYNCB | R/W | 0h | This bit enables single-ended control of SYNCB using the GPIO4 pin (pin 63). The differential SYNCB input is ignored. Set the EN CMOS SYNCB bit and keep the CH bit high to make this bit effective.<br>0 = Differential SYNCB input<br>1 = Single-ended SYNCB input using pin 63 |
| 5-0 | 0 | W | 0h | Must write 0 |

### 8.5.9.11 Register 037h (address = 037h), JESD Digital Page

**Figure 194. Register 037h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | PLL MODE | |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | |

**Table 80. Register 037h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1-0 | PLL MODE | R/W | 0h | These bits select the PLL multiplication factor; see the JESD tables in the *JESD204B Frame Assembly* section for settings.<br>00 = 20x mode<br>01 = 16x mode<br>10 = 40x mode (the 40x MODE bit in register 16h must also be set)<br>11 = 80x mode |

### 8.5.9.12 Register 03Ch (address = 03Ch), JESD Digital Page

**Figure 195. Register 03Ch**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | EN CMOS SYNCB |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 81. Register 03Ch Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | EN CMOS SYNCB | R/W | 0h | Set this bit and the CMOS SYNCB bit high to provide a single-ended SYNC input to the device instead of differential. Also, keep the CH bit high. Thus:<br>1. Select the JESD digital page.<br>2. Write address 7036h with value 40h.<br>3. Write address 703Ch with value 01h. |

#### 8.5.9.13 Register 03Eh (address = 03Eh), JESD Digital Page

**Figure 196. Register 03Eh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | MASK CLKDIV SYSREF | MASK NCO SYSREF | 0 | 0 | 0 | 0 | 0 |
| W-0h | R/W-0h | R/W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

**Table 82. Register 03Eh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | W | 0h | Must write 0 |
| 6 | MASK CLKDIV SYSREF | R/W | 0h | Use this bit to mask the SYSREF going to the input clock divider.<br>0 = Input clock divider is reset when SYSREF is asserted (that is, when SYSREF transitions from low to high)<br>1 = Input clock divider ignores SYSREF assertions |
| 5 | MASK NCO SYSREF | R/W | 0h | Use this bit to mask the SYSREF going to the NCO in the DDC block and LMFC counter of the JESD interface.<br>0 = NCO phase and LMFC counter are reset when SYSREF is asserted (that is, when SYSREF transitions from low to high)<br>1 = NCO and LMFC counter ignore SYSREF assertions |
| 4-0 | 0 | W | 0h | Must write 0 |

### 8.5.10 Decimation Filter Page

**Direct Addressing, 16-Bit Address, 5000h**

#### 8.5.10.1 Register 000h (address = 000h), Decimation Filter Page

**Figure 197. Register 000h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDC EN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 83. Register 000h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | DDC EN | R/W | 0h | This bit enables the decimation filter.<br>0 = Do not use<br>1 = Decimation filter enabled |

#### 8.5.10.2 Register 001h (address = 001h), Decimation Filter Page

**Figure 198. Register 001h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DECIM FACTOR | | | |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | | | |

**Table 84. Register 001h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3-0 | DECIM FACTOR | R/W | 0h | These bits configure the decimation filter setting.<br>0000 = Divide-by-4 complex<br>0001 = Divide-by-6 complex<br>0010 = Divide-by-8 complex<br>0011 = Divide-by-9 complex<br>0100 = Divide-by-10 complex<br>0101 = Divide-by-12 complex<br>0110 = Not used<br>0111 = Divide-by-16 complex<br>1000 = Divide-by-18 complex<br>1001 = Divide-by-20 complex<br>1010 = Divide-by-24 complex<br>1011 = Not used<br>1100 = Divide-by-32 complex |

#### 8.5.10.3 Register 002h (address = 2h), Decimation Filter Page

**Figure 199. Register 002h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | DUAL BAND EN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 85. Register 002h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | DUAL BAND EN | R/W | 0h | This bit enables the dual-band DDC filter for the corresponding channel.<br>0 = Single-band DDC; available in both ADC32RF80 and ADC32RF83<br>1 = Dual-band DDC; available in ADC32RF80 only |

#### 8.5.10.4 Register 005h (address = 005h), Decimation Filter Page

**Figure 200. Register 005h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | REAL OUT EN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 86. Register 005h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | REAL OUT EN | R/W | 0h | This bit converts the complex output to real output at 2x the output rate.<br>0 = Complex output format<br>1 = Real output format |

#### 8.5.10.5 Register 007h (address = 007h), Decimation Filter Page

**Figure 201. Register 007h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DDC0 NCO1 LSB | | | | | | | |
| R/W-0h | | | | | | | |

**Table 87. Register 007h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DDC0 NCO1 LSB | R/W | 0h | These bits are the LSB of the NCO frequency word for NCO1 of DDC0 (band 1).<br>The LSB represents $f_S$ / ($2^{16}$), where $f_S$ is the ADC sampling frequency. |

### 8.5.10.6 Register 008h (address = 008h), Decimation Filter Page

**Figure 202. Register 008h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DDC0 NCO1 MSB | | | | | | | |
| R/W-0h | | | | | | | |

**Table 88. Register 008h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DDC0 NCO1 MSB | R/W | 0h | These bits are the MSB of the NCO frequency word for NCO1 of DDC0 (band 1).<br>The LSB represents $f_S$ / ($2^{16}$), where $f_S$ is the ADC sampling frequency. |

### 8.5.10.7 Register 009h (address = 009h), Decimation Filter Page

**Figure 203. Register 009h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DDC0 NCO2 LSB | | | | | | | |
| R/W-0h | | | | | | | |

**Table 89. Register 009h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DDC0 NCO2 MSB | R/W | 0h | These bits are the LSB of the NCO frequency word for NCO2 of DDC0 (band 1).<br>The LSB represents $f_S$ / ($2^{16}$), where $f_S$ is the ADC sampling frequency. |

### 8.5.10.8 Register 00Ah (address = 00Ah), Decimation Filter Page

**Figure 204. Register 00Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DDC0 NCO2 MSB | | | | | | | |
| R/W-0h | | | | | | | |

**Table 90. Register 00Ah Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DDC0 NCO2 MSB | R/W | 0h | These bits are the MSB of the NCO frequency word for NCO2 of DDC0 (band 1).<br>The LSB represents $f_S$ / ($2^{16}$), where $f_S$ is the ADC sampling frequency. |

#### 8.5.10.9 Register 00Bh (address = 00Bh), Decimation Filter Page

**Figure 205. Register 00Bh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DDC0 NCO3 LSB | | | | | | | |
| R/W-0h | | | | | | | |

**Table 91. Register 00Bh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DDC0 NCO3 LSB | R/W | 0h | These bits are the LSB of the NCO frequency word for NCO3 of DDC0 (band 1).<br>The LSB represents $f_S$ / ($2^{16}$), where $f_S$ is the ADC sampling frequency. |

#### 8.5.10.10 Register 00Ch (address = 00Ch), Decimation Filter Page

**Figure 206. Register 00Ch**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DDC0 NCO3 MSB | | | | | | | |
| R/W-0h | | | | | | | |

**Table 92. Register 00Ch Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DDC0 NCO3 MSB | R/W | 0h | These bits are the MSB of the NCO frequency word for NCO3 of DDC0 (band 1).<br>The LSB represents $f_S$ / ($2^{16}$), where $f_S$ is the ADC sampling frequency. |

#### 8.5.10.11 Register 00Dh (address = 00Dh), Decimation Filter Page

**Figure 207. Register 00Dh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DDC1 NCO4 LSB | | | | | | | |
| R/W-0h | | | | | | | |

**Table 93. Register 00Dh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DDC1 NCO4 LSB | R/W | 0h | These bits are the LSB of the NCO frequency word for NCO4 of DDC1 (band 2, only when dual-band mode is enabled).<br>The LSB represents $f_S$ / ($2^{16}$), where $f_S$ is the ADC sampling frequency. |

#### 8.5.10.12 Register 00Eh (address = 00Eh), Decimation Filter Page

**Figure 208. Register 00Eh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DDC1 NCO4 MSB | | | | | | | |
| R/W-0h | | | | | | | |

**Table 94. Register 00Eh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DDC1 NCO4 MSB | R/W | 0h | These bits are the MSB of the NCO frequency word for NCO4 of DDC1 (band 2, only when dual-band mode is enabled).<br>The LSB represents $f_S$ / ($2^{16}$), where $f_S$ is the ADC sampling frequency. |

#### 8.5.10.13 Register 00Fh (address = 00Fh), Decimation Filter Page

**Figure 209. Register 00Fh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | NCO SEL PIN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 95. Register 00Fh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | NCO SEL PIN | R/W | 0h | This bit enables NCO selection through the GPIO pins.<br>0 = NCO selection through SPI (see address 0h10)<br>1 = NCO selection through GPIO pins |

#### 8.5.10.14 Register 010h (address = 010h), Decimation Filter Page

**Figure 210. Register 010h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | NCO SEL | |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | |

**Table 96. Register 010h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1-0 | NCO SEL | R/W | 0h | These bits enable NCO selection through register setting.<br>00 = NCO1 selected for DDC 1<br>01 = NCO2 selected for DDC 1<br>10 = NCO3 selected for DDC 1 |

### 8.5.10.15 Register 011h (address = 011h), Decimation Filter Page

**Figure 211. Register 011h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | LMFC RESET MODE | |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | |

**Table 97. Register 011h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1-0 | LMFC RESET MODE | R/W | 0h | These bits reset the configuration for all DDCs and NCOs.<br>00 = All DDCs and NCOs are reset with every LMFC RESET<br>01 = Reset with first LMFC RESET after DDC start. Afterwards, reset only when analog clock dividers are resynchronized.<br>10 = Reset with first LMFC RESET after DDC start. Afterwards, whenever analog clock dividers are resynchronized, use two LMFC resets.<br>11 = Do not use an LMFC reset at all. Reset the DDCs only when a DDC start is asserted and afterwards continue normal operation. Deterministic latency is not ensured. |

### 8.5.10.16 Register 014h (address = 014h), Decimation Filter Page

**Figure 212. Register 014h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDC0 6DB GAIN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 98. Register 014h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | DDC0 6DB GAIN | R/W | 0h | This bit scales the output of DDC0 by 2 (6 dB) to compensate for real-to-complex conversion and image suppression. This scaling does not apply to the high-bandwidth filter path (divide-by-4 and -6); see register 1Fh.<br>0 = Normal operation<br>1 = 6-dB digital gain is added |

### *8.5.10.17 Register 016h (address = 016h), Decimation Filter Page*

**Figure 213. Register 016h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | DDC1 6DB GAIN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 99. Register 016h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | DDC1 6DB GAIN | R/W | 0h | This bit scales the output of DDC1 by 2 (6 dB) to compensate for real-to-complex conversion and image suppression. This scaling does not apply to the high-bandwidth filter path (divide-by-4 and -6); see register 1Fh.<br>0 = Normal operation<br>1 = 6-dB digital gain is added |

### *8.5.10.18 Register 01Eh (address = 01Eh), Decimation Filter Page*

**Figure 214. Register 01Eh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DDC DET LAT | | | 0 | 0 | 0 | 0 |
| W-0h | R/W-0h | | | W-0h | W-0h | W-0h | W-0h |

**Table 100. Register 01Eh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | W | 0h | Must write 0 |
| 6-4 | DDC DET LAT | R/W | 0h | These bits ensure deterministic latency depending on the decimation setting used; see Table 101. |
| 3-0 | 0 | W | 0h | Must write 0 |

**Table 101. DDC DET LAT Bit Settings**

| SETTING | COMPLEX DECIMATION SETTING |
|---|---|
| 10h | Divide-by-24, -32 complex |
| 20h | Divide-by-16, -18, -20 complex |
| 40h | Divide-by-by 6, -12 complex |
| 50h | Divide-by-4, -8, -9, -10 complex |

#### 8.5.10.19 Register 01Fh (address = 01Fh), Decimation Filter Page

**Figure 215. Register 01Fh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | WBF 6DB GAIN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 102. Register 01Fh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | WBF 6DB GAIN | R/W | 0h | This bit scales the output of the wide bandwidth DDC filter by 2 (6 dB) to compensate for real-to-complex conversion and image suppression. This setting only applies to the high-bandwidth filter path (divide-by-4 and -6).<br>0 = Normal operation<br>1 = 6-dB digital gain is added |

#### 8.5.10.20 Register 033h-036h (address = 033h-036h), Decimation Filter Page

**Figure 216. Register 033h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUSTOM PATTERN1[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 217. Register 034h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUSTOM PATTERN1[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 218. Register 035h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUSTOM PATTERN2[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 219. Register 036h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUSTOM PATTERN2[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Table 103. Register 033h-036h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CUSTOM PATTERN | R/W | 0h | These bits set the custom test pattern in address 33h, 34h, 35h, or 36h. |

#### 8.5.10.21 Register 037h (address = 037h), Decimation Filter Page

**Figure 220. Register 037h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TEST PATTERN DDC1 Q-DATA | | | | TEST PATTERN DDC1 I-DATA | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 104. Register 037h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | TEST PATTERN DDC1 Q-DATA | W | 0h | These bits select the test patten for the Q stream of the DDC1.<br>0000 = Normal operation using ADC output data<br>0001 = Outputs all 0s<br>0010 = Outputs all 1s<br>0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101<br>0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 65535<br>0110 = Single pattern: output data are a custom pattern 1 (75h and 76h)<br>0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2<br>1000 = Deskew pattern: output data are AAAAh<br>1001 = SYNC pattern: output data are FFFFh |
| 3-0 | TEST PATTERN DDC1 I-DATA | R/W | 0h | These bits select the test patten for the I stream of the DDC1.<br>0000 = Normal operation using ADC output data<br>0001 = Outputs all 0s<br>0010 = Outputs all 1s<br>0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101<br>0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 65535<br>0110 = Single pattern: output data are a custom pattern 1 (75h and 76h)<br>0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2<br>1000 = Deskew pattern: output data are AAAAh<br>1001 = SYNC pattern: output data are FFFFh |

### 8.5.10.22 Register 038h (address = 038h), Decimation Filter Page

**Figure 221. Register 038h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TEST PATTERN DDC2 Q-DATA | | | | TEST PATTERN DDC2 I -DATA | | | |
| R/W-0h | | | | R/W-0h | | | |

**Table 105. Register 038h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | TEST PATTERN DDC2 Q-DATA | R/W | 0h | These bits select the test patten for the Q stream of the DDC2.<br>0000 = Normal operation using ADC output data<br>0001 = Outputs all 0s<br>0010 = Outputs all 1s<br>0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101<br>0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 65535<br>0110 = Single pattern: output data are a custom pattern 1 (75h and 76h)<br>0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2<br>1000 = Deskew pattern: output data are AAAAh<br>1001 = SYNC pattern: output data are FFFFh |
| 3-0 | TEST PATTERN DDC2 I -DATA | R/W | 0h | These bits select the test patten for the I stream of the DDC2.<br>0000 = Normal operation using ADC output data<br>0001 = Outputs all 0s<br>0010 = Outputs all 1s<br>0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101<br>0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 65535<br>0110 = Single pattern: output data are a custom pattern 1 (75h and 76h)<br>0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2<br>1000 = Deskew pattern: output data are AAAAh<br>1001 = SYNC pattern: output data are FFFFh |

### 8.5.10.23 Register 039h (address = 039h), Decimation Filter Page

**Figure 222. Register 039h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | USE COMMON TEST PATTERN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 106. Register 039h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | USE COMMON TEST PATTERN | R/W | 0h | 0 = Each data stream sends test patterns programmed by bits[3:0] of register 37h.<br>1 = Test patterns are individually programmed for the I and Q stream of each DDC using the TEST PATTERN DDCx y-DATA register bits (where x = 1 or 2 and y = I or Q). |

### 8.5.10.24 Register 03Ah (address = 03Ah), Decimation Filter Page

**Figure 223. Register 03Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | TEST PAT RES | TP RES EN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | R/W-0h |

**Table 107. Register 03Ah Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1 | TEST PAT RES | R/W | 0h | Pulsing this bit resets the test pattern. The test pattern reset must be enabled first (bit D0).<br>0 = Normal operation<br>1 = Reset the test pattern |
| 0 | TP RES EN | R/W | 0h | This bit enables the test pattern reset.<br>0 = Reset disabled<br>1 = Reset enabled |

### 8.5.11 Power Detector Page

#### *8.5.11.1 Register 000h (address = 000h), Power Detector Page*

**Figure 224. Register 000h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | PKDET EN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 108. Register 000h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | PKDET EN | R/W | 0h | This bit enables the peak power and crossing detector.<br>0 = Power detector disabled<br>1 = Power detector enabled |

#### *8.5.11.2 Register 001h-002h (address = 001h-002h), Power Detector Page*

**Figure 225. Register 001h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BLKPKDET [7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 226. Register 002h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BLKPKDET [15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Table 109. Register 001h-002h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | BLKPKDET | R/W | 0h | This register specifies the block length in terms of number of samples (S`) used for peak power computation. Each sample S` is a peak of 8 actual ADC samples. This parameter is a 17-bit value directly in linear scale. In decimation mode, the block length must be a multiple of a divide-by-4 or -6 complex: length = 5 × decimation factor.<br>The divide-by-8 to -32 complex: length = 10 × decimation factor. |

#### *8.5.11.3 Register 003h (address = 003h), Power Detector Page*

**Figure 227. Register 003h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLKPKDET[16] |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 110. Register 003h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | BLKPKDET[16] | R/W | 0h | This register specifies the block length in terms of number of samples (S`) used for peak power computation. Each sample S` is a peak of 8 actual ADC samples. This parameter is a 17-bit value directly in linear scale. In decimation mode, the block length must be a multiple of a divide-by-4 or -6 complex: length = 5 × decimation factor.<br>The divide-by-8 to -32 complex: length = 10 × decimation factor. |

#### *8.5.11.4 Register 007h-00Ah (address = 007h-00Ah), Power Detector Page*

**Figure 228. Register 007h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BLKTHHH | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 229. Register 008h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BLKTHHL | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 230. Register 009h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BLKTHLH | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 231. Register 00Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BLKTHLL | | | | | | | |
| R/W-0h | | | | | | | |

**Table 111. Register 007h-00Ah Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | BLKTHHH<br>BLKTHHL<br>BLKTHLH<br>BLKTHLL | R/W | 0h | These registers set the four different thresholds for the hysteresis function threshold values from 0 to 256 (2TH), where 256 is equivalent to the peak amplitude.<br>Example: BLKTHHH is set to –2 dBFS from peak: $10^{(-2\ /\ 20)\ \times\ 256}$ = 203, then set 5407h = CBh. |

### 8.5.11.5 Register 00Bh-00Ch (address = 00Bh-00Ch), Power Detector Page

**Figure 232. Register 00Bh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DWELL[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 233. Register 00Ch**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DWELL[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Table 112. Register 00Bh-00Ch Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DWELL | R/W | 0h | DWELL time counter.<br>When the computed block peak crosses the upper thresholds BLKTHHH or BLKTHLH, the peak detector output flags are set. In order to be reset, the computed block peak must remain continuously lower than the lower threshold (BLKTHHL or BLKTHLL) for the period specified by the DWELL value. This threshold is 16 bits, is specified in terms of $f_S$ / 8 clock cycles, and must be set to 0 for the crossing detector. Example: if $f_S$ = 3 GSPS, $f_S$ / 8 = 375 MHz, and DWELL = 0100h then the DWELL time = $2^9$ / 375 MHz = 1.36 µs. |

### 8.5.11.6 Register 00Dh (address = 00Dh), Power Detector Page

**Figure 234. Register 00Dh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | FILT0LPSEL |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 113. Register 00Dh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | FILT0LPSEL | R/W | 0h | This bit selects either the block detector output or 2-bit output as the input to the IIR filter.<br>0 = Use the output of the high comparators (HH and HL) as the input of the IIR filter<br>1 = Combine the output of the high (HH and HL) and low (LH and LL) comparators to generate a 3-level input to the IIR filter (–1, 0, 1) |

#### 8.5.11.7 Register 00Eh (address = 00Eh), Power Detector Page

**Figure 235. Register 00Eh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | TIMECONST | | | |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | | | |

**Table 114. Register 00Eh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3-0 | TIMECONST | R/W | 0h | These bits set the crossing detector time period for N = 0 to 15 as $2^N \times f_S$ / 8 clock cycles. The maximum time period is 32768 × $f_S$ / 8 clock cycles (approximately 87 µs at 3 GSPS). |

#### 8.5.11.8 Register 00Fh, 010h-012h, and 016h-019h (address = 00Fh, 010h-012h, and 016h-019h), Power Detector Page

**Figure 236. Register 00Fh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FIL0THH[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 237. Register 010h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FIL0THH[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 238. Register 011h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FIL0THL[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 239. Register 012h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FIL0THL[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 240. Register 016h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FIL1THH[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 241. Register 017h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FIL1THH[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 242. Register 018h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FIL1THL[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 243. Register 019h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FIL1THL[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Table 115. Register 00Fh, 010h, 011h, 012h, 016h, 017h, 018h, and 019h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | FIL0THH<br>FIL0THL<br>FIL1THH<br>FIL1THL | R/W | 0h | Comparison thresholds for the crossing detector counter. This threshold is 16 bits in 2.14 signed notation. A value of 1 (4000h) corresponds to 100% crossings, a value of 0.125 (0800h) corresponds to 12.5% crossings. |

### *8.5.11.9 Register 013h-01Ah (address = 013h-01Ah), Power Detector Page*

**Figure 244. Register 013h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | IIR0 2BIT EN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Figure 245. Register 01Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | IIR1 2BIT EN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 116. Register 013h and 01Ah Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | IIR0 2BIT EN<br>IIR1 2BIT EN | R/W | 0h | This bit enables 2-bit output format of the IIR0 and IIR1 output comparators.<br>0 = Selects 1-bit output format<br>1 = Selects 2-bit output format |

#### 8.5.11.10 Register 01Dh-01Eh (address = 01Dh-01Eh), Power Detector Page

**Figure 246. Register 01Dh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DWELLIIR[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 247. Register 01Eh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DWELLIIR[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Table 117. Register 01Dh-01Eh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DWELLIIR | R/W | 0h | DWELL time counter for the IIR output comparators. When the IIR filter output crosses the upper thresholds FIL0THH or FIL1THH, the IIR peak detector output flags are set. In order to be reset, the output of the IIR filter must remain continuously lower than the lower threshold (FIL0THL or FIL1THL) for the period specified by the DWELLIIR value. This threshold is 16 bits and is specified in terms of $f_S$ / 8 clock cycles.<br>Example: if $f_S$ = 3 GSPS, $f_S$ / 8 = 375 MHz, and DWELLIIR = 0100h, then the DWELL time = 29 / 375 MHz = 1.36 µs. |

#### 8.5.11.11 Register 020h (address = 020h), Power Detector Page

**Figure 248. Register 020h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | RMSDET EN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 118. Register 020h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | RMSDET EN | R/W | 0h | This bit enables the RMS power detector.<br>0 = Power detector disabled<br>1 = Power detector enabled |

#### 8.5.11.12 Register 021h (address = 021h), Power Detector Page

**Figure 249. Register 021h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | PWRDETACCU | | | | |
| W-0h | W-0h | W-0h | R/W-0h | | | | |

**Table 119. Register 021h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | W | 0h | Must write 0 |
| 4-0 | PWRDETACCU | R/W | 0h | These bits program the block length to be used for RMS power computation.<br>The block length is defined in terms of $f_S$ / 8 clocks and can be programmed as 2M, where M = 0 to 16. |

#### 8.5.11.13 Register 022h-025h (address = 022h-025h), Power Detector Page

**Figure 250. Register 022h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PWRDETH[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 251. Register 023h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PWRDETH[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 252. Register 024h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PWRDETL[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 253. Register 025h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PWRDETL[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**Table 120. Register 022h-025h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PWRDETH[15:0]<br>PWRDETL[15:0] | R/W | 0h | The computed average power is compared against these high and low thresholds. One LSB of the thresholds represents $1 / 2^{16}$.<br>Example: if PWRDETH is set to –14 dBFS from peak, $(10^{(-14 / 20)})^2 \times 2^{16} = 2609$, then set 5422h, 5423h = 0A31h. |

#### 8.5.11.14 Register 027h (address = 027h), Power Detector Page

**Figure 254. Register 027h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | RMS 2BIT EN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

**Table 121. Register 027h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | RMS 2BIT EN | R/W | 0h | This bit enables 2-bit output format on the RMS output comparators.<br>0 = Selects 1-bit output format<br>1 = Selects 2-bit output format |

#### 8.5.11.15 Register 02Bh (address = 02Bh), Power Detector Page

**Figure 255. Register 02Bh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | RESET AGC | 0 | 0 | 0 | 0 |
| W-0h | W-0h | W-0h | R/W-0h | W-0h | W-0h | W-0h | W-0h |

**Table 122. Register 02Bh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | W | 0h | Must write 0 |
| 4 | RESET AGC | R/W | 0h | After configuration, the AGC module must be reset and then brought out of reset to start operation.<br>0 = Clear AGC reset<br>1 = Set AGC reset<br>Example: set 542Bh to 10h and then to 00h. |
| 3-0 | 0 | W | 0h | Must write 0 |

#### 8.5.11.16 Register 032h-035h (address = 032h-035h), Power Detector Page

**Figure 256. Register 032h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUTSEL GPIO4 | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 257. Register 033h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUTSEL GPIO1 | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 258. Register 034h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUTSEL GPIO3 | | | | | | | |
| R/W-0h | | | | | | | |

**Figure 259. Register 035h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OUTSEL GPIO2 | | | | | | | |
| R/W-0h | | | | | | | |

**Table 123. Register 032h-035h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OUTSEL GPIO1<br>OUTSEL GPIO2<br>OUTSEL GPIO3<br>OUTSEL GPIO4 | R/W | 0h | These bits set the function or signal for each GPIO pin.<br>0 = IIR PK DET0[0]<br>1 = IIR PK DET0[1] (2-bit mode)<br>2 = IIR PK DET1[0]<br>3 = IIR PK DET1[1] (2-bit mode)<br>4 = BLKPKDETH<br>5 = BLKPKDETL<br>6 = PWR Det[0]<br>7 = PWR Det[1] (2-bit mode)<br>8 = FOVR<br>Others = Do not use |

#### 8.5.11.17 Register 037h (address = 037h), Power Detector Page

**Figure 260. Register 037h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | IODIR GPIO2 | IODIR GPIO3 | IODIR GPIO1 | IODIR GPIO4 |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 124. Register 037h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3-0 | IODIRGPIO[4:1] | R/W | 0h | These bits select the output direction for the GPIO[4:1] pins.<br>0 = Input (for the NCO control)<br>1 = Output (for the AGC alarm function) |

#### 8.5.11.18 Register 038h (address = 038h), Power Detector Page

**Figure 261. Register 038h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | INSEL1 | | 0 | 0 | INSEL0 | |
| W-0h | W-0h | R/W-0h | | W-0h | W-0h | R/W-0h | |

**Table 125. Register 038h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | W | 0h | Must write 0 |
| 5-4 | INSEL1 | R/W | 0h | These bits select which GPIO pin is used for the INSEL1 bit.<br>00 = GPIO4<br>01 = GPIO1<br>10 = GPIO3<br>11 = GPIO2<br>Table 126 lists the NCO selection, based on the bit settings of the INSEL pins; see the section NCO Switching for details. |
| 3-2 | 0 | W | 0h | Must write 0 |
| 1-0 | INSEL0 | R/W | 0h | These bits select which GPIO pin is used for the INSEL0 bit.<br>00 = GPIO4<br>01 = GPIO1<br>10 = GPIO3<br>11 = GPIO2<br>Table 126 lists the NCO selection, based on the bit settings of the INSEL pins; see the section NCO Switching for details. |

**Table 126. INSEL Bit Settings**

| INSELx[1:0] (Where x = 0 or 1) | NCO SELECTED |
|---|---|
| 00 | NCO1 |
| 01 | NCO2 |
| 10 | NCO3 |
| 11 | n/a |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Start-Up Sequence

The steps in Table 127 are recommended as the power-up sequence when the ADC31RF80 is in the decimation-by-4 complex output mode.

**Table 127. Initialization Sequence**

| STEP | DESCRIPTION | PAGE, REGISTER ADDRESS AND DATA | COMMENT |
|---|---|---|---|
| 1 | Supply all supply voltages. There is no required power-supply sequence for the 1.15 V, 1.2 V, and 1.9 V supplies, and can be supplied in any order. | — | — |
| 2 | Provide the SYSREF signal. | — | — |
| 3 | Pulse a hardware reset (low-to-high-to-low) on pins 33 and 34. | — | — |
| 4 | Write the register addresses described in the *PowerUpConfig* file. | See the files located in SBAA226 | The *Power-up config* file contains analog trim registers that are required for best performance of the ADC. Write these registers every time after power up. |
| 5 | Write the register addresses mentioned in the ILConfigNyqX file, where X is the Nyquist zone. | See the files located in SBAA226 | Based on the signal band of interest, provide the Nyquist zone information to the device. |
| 6.1 | Wait for 50 ms for the device to estimate the interleaving errors. | — | — |
| 7 | Depending upon the Nyquist band of operation, choose and write the registers from the appropriate file, *NLConfigNyqX*, where X is the Nyquist zone. | See the files located in SBAA226 | Third-order nonlinearity of the device is optimized by this step for channel A. |
| 8 | Configure the JESD interface and DDC block by writing the registers mentioned in the *DDC Config* file. | See the files located in SBAA226 | Determine the DDC and JESD interface LMFS options. Program these options in this step. |

### 9.1.2 Hardware Reset

Figure 262 and Table 128 provide the timing information for the hardware reset.

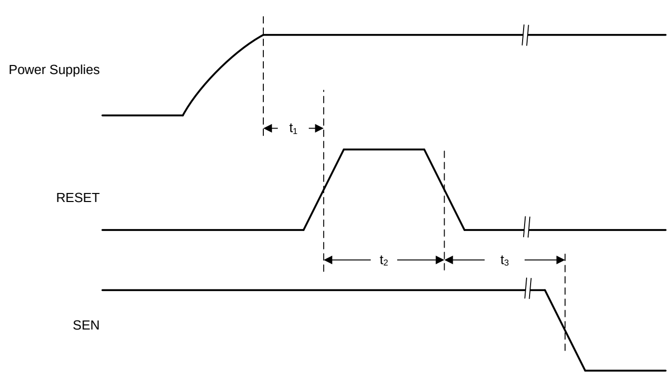



**Figure 262. Hardware Reset Timing Diagram**

**Table 128. Hardware Reset Timing Information**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_1$ | Power-on delay from power-up to active high RESET pulse | 1 | | | ms |
| $t_2$ | Reset pulse duration: active high RESET pulse duration | 1 | | | µs |
| $t_3$ | Register write delay from RESET disable to SEN active | 100 | | | ns |

### 9.1.3 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors, as shown in Equation 5: quantization noise, thermal noise, and jitter. The quantization noise is typically not noticeable in pipeline converters and is 84 dB for a 14-bit ADC. The thermal noise limits the SNR at low input frequencies and the clock jitter sets the SNR for higher input frequencies.

$$SNRADC[dBc] = -20\log\sqrt{\left(10^{-\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (5)$$

Equation 6 calculates the SNR limitation resulting from sample clock jitter:

$$SNR_{Jitter}[dBc] = -20\log(2\pi \times f_{IN} \times t_{Jitter}) \quad (6)$$

The total clock jitter ($T_{Jitter}$) has two components: the internal aperture jitter (90 $f_S$) is set by the noise of the clock input buffer and the external clock jitter. Equation 7 calculates $T_{Jitter}$:

$$t_{Jitter} = \sqrt{(t_{Jitter,\ Ext\_Clock\_Input})^2 + (t_{Aperture\_ADC})^2} \quad (7)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input. A faster clock slew rate also improves the ADC aperture jitter.

The ADC31RF80 has a thermal noise of approximately 63 dBFS and an internal aperture jitter of 90 $f_S$. Figure 263 shows the SNR in relation to the amount of external jitter for different input frequencies.

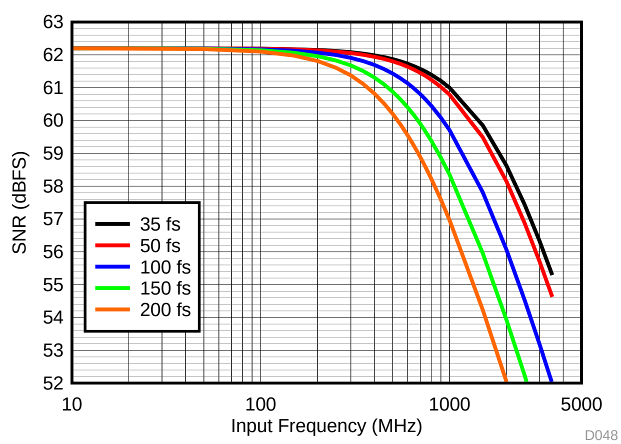



**Figure 263. ADC SNR vs Input Frequency and External Clock Jitter**

### *9.1.3.1 External Clock Phase Noise Consideration*

As shown in Figure 264, external clock jitter can be calculated by integrating the phase noise of the clock source out to approximately two times of the ADC sampling rate (2 × $f_S$), . In order to maximize the ADC SNR, an external band-pass filter is recommended to be used on the clock input. This filter reduces the jitter contribution from the broadband clock phase noise floor by effectively reducing the integration bandwidth to the pass band of the band-pass filter. This method is suitable when estimating the overall ADC SNR resulting from clock jitter at a certain input frequency.

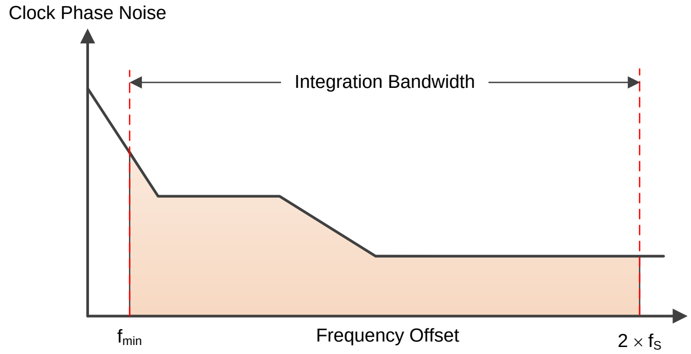



**Figure 264. Integration Bandwidth for Extracting Jitter From Clock Phase Noise**

However, when estimating the affect of a nearby blocker (such as a strong in-band interferer to the sensitivity), as shown in Figure 265, the phase noise information can be used directly to estimate the noise budget contribution at a certain offset frequency.

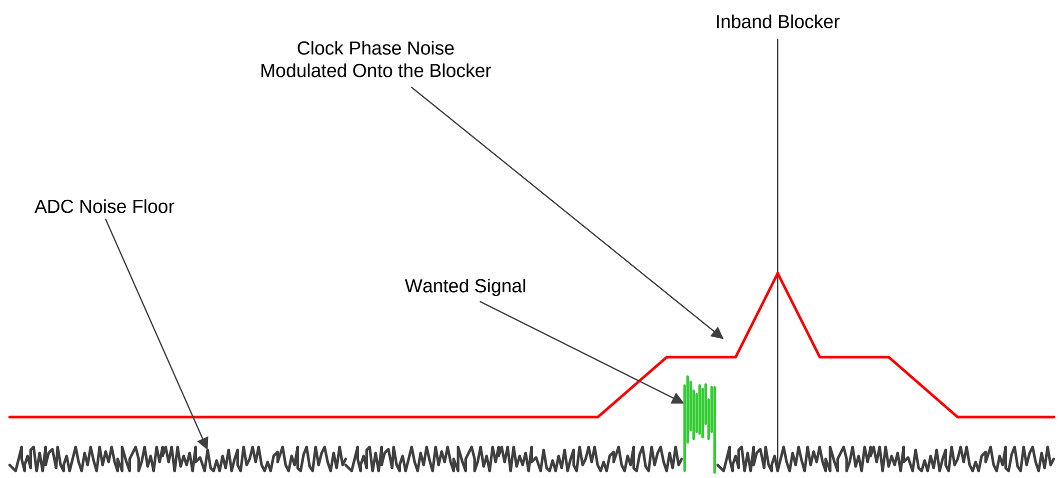



**Figure 265. Small Wanted Signal in Presence of Interferer**

At the sampling instant, the phase noise profile of the clock source convolves with the input signal (for example, the small wanted signal and the strong interferer merge together). If the power of the clock phase noise in the signal band of interest is too large, the wanted signal cannot not be recovered.

The resulting equivalent phase noise at the ADC input is also dependent on the sampling rate of the ADC and frequency of the input signal. Equation 8 shows how the ADC sampling rate scales the clock phase noise.

$$ADC_{NSD}\left(dBc / Hz\right) = PN_{CLK}\left(dBc / Hz\right) - 20 \times \log\left(\frac{f_S}{f_{IN}}\right) \quad (8)$$

Using this information, the noise contribution resulting from the phase noise profile of the ADC sampling clock can be calculated.

### 9.1.4 Power Consumption in Different Modes

The ADC31RF80 consumes approximately 4 W with a divide-by-4 complex output. When different DDC options are used, the power consumption on the DVDD supply changes by a small amount but remains unaffected on other supplies.

Table 129 and Table 130 show power consumption in different DDC modes.

**Table 129. Power Consumption in Different DDC Modes (Sampling Clock Frequency, $f_S$ = 2457.6 MSPS)**

| DECIMATION OPTION | ACTIVE DDC | AVDD1P9 (mA) | AVDD1P2 (mA) | DVDD1P2 (mA) | TOTAL POWER (mW) |
|---|---|---|---|---|---|
| Divide-by-4 | Single | 914 | 447 | 817 | 3190 |
| Divide-by-8 | Dual | 913 | 449 | 890 | 3275 |
| Divide-by-8 | Single | 914 | 449 | 789 | 3160 |
| Divide-by-16 | Dual | 914 | 450 | 880 | 3266 |
| Divide-by-16 | Single | 914 | 449 | 777 | 3147 |
| Divide-by-24 | Dual | 911 | 450 | 864 | 3242 |
| Divide-by-24 | Single | 911 | 449 | 747 | 3106 |
| Divide-by-32 | Dual | 910 | 450 | 810 | 3178 |
| Divide-by-32 | Single | 910 | 449 | 710 | 3062 |

**Table 130. Power Consumption in Different DDC Modes (Sampling Clock Frequency, $f_S$ = 2949.12 MSPS)**

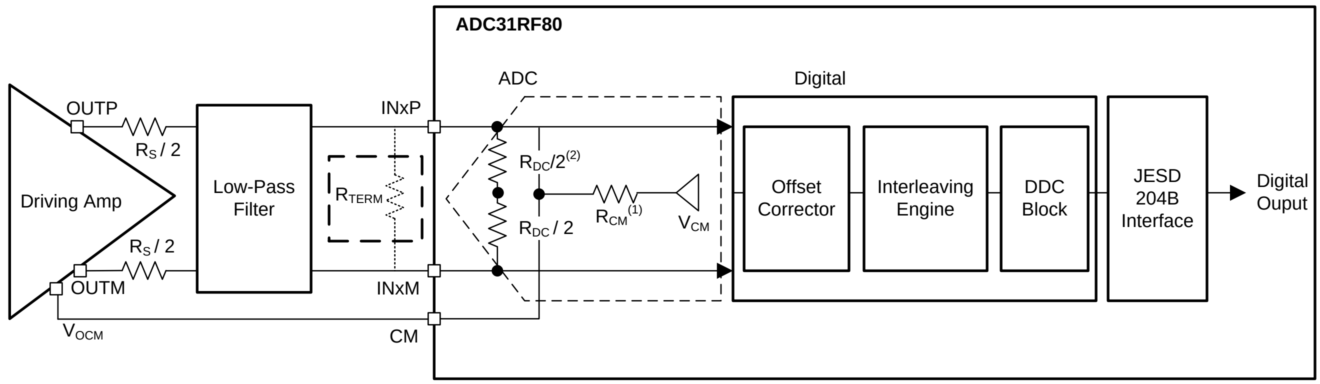
| DECIMATION OPTION | ACTIVE DDC | AVDD1P9 (mA) | AVDD1P2 (mA) | DVDD1P2 (mA) | TOTAL POWER (mW) |
|---|---|---|---|---|---|
| Divide-by-4 | Single | 956 | 499 | 975 | 3512 |
| Divide-by-8 | Dual | 957 | 500 | 1060 | 3612 |
| Divide-by-8 | Single | 957 | 500 | 945 | 3480 |
| Divide-by-16 | Dual | 958 | 525 | 1061 | 3644 |
| Divide-by-16 | Single | 958 | 524 | 938 | 3502 |
| Divide-by-24 | Dual | 955 | 524 | 1027 | 3598 |
| Divide-by-24 | Single | 955 | 523 | 904 | 3456 |
| Divide-by-32 | Dual | 954 | 523 | 976 | 3536 |
| Divide-by-32 | Single | 954 | 522 | 860 | 3402 |

### 9.1.5 Using DC Coupling in the ADC31RF80

The ADC31RF80 can be used in dc-coupling applications. However, the following points must be considered when designing the system:

1. Ensure that the correct common-mode voltage is used at the ADC analog inputs.

   The analog inputs are internally self-biased to $V_{CM}$ through approximately a 33-Ω resistor. The internal biasing resistors also function as a termination resistor. However, if a different termination is required, as shown in Figure 266, the external resistor $R_{TERM}$ can be differentially placed between the analog inputs. The amplifier $V_{OCM}$ pin is recommended to be driven from the CM pin of the ADC to help the amplifier output common-mode voltage track the required common-mode voltage of the ADC.




(1) Set the INCR CM IMPEDANCE bit to increase the RCM from 0 Ω to > 5000 Ω.

(2) $R_{DC}$ is approximately 65 Ω.

**Figure 266. The ADC31RF80 in a DC-Coupling Application**

2. Ensure that the correct SPI settings are written to the ADC.

   As shown in Figure 267, the ADC31RF80 has a digital block that estimates and corrects the offset mismatch among four interleaving ADC cores.

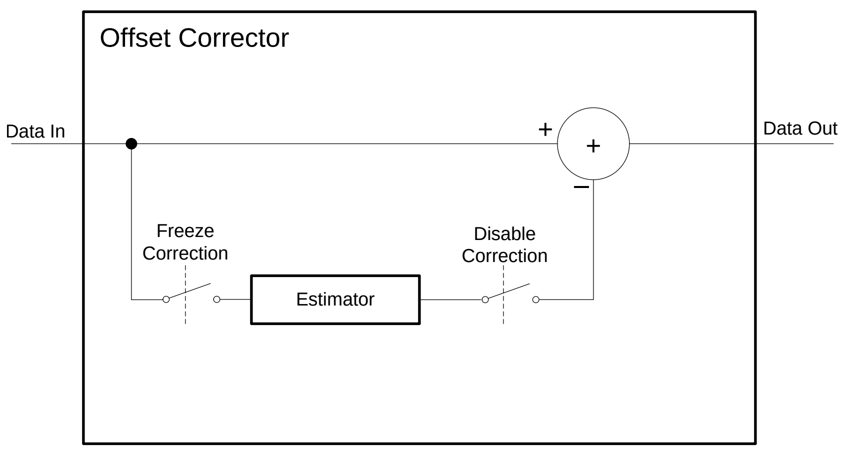



**Figure 267. Offset Corrector in the ADC31RF80**

The offset corrector block nullifies dc, $f_S$ / 8, $f_S$ / 4, 3 $f_S$ / 8, and $f_S$ / 2. The resulting spectrum becomes free from static spurs at these frequencies. The corrector continuously processes the data coming from the interleaving ADC cores and cannot distinguish if the tone at these frequencies is part of signal or if the tone originated from a mismatch among the interleaving ADC cores. Thus, in applications where the signal is present at these frequencies, the offset corrector block can be bypassed.

### 9.1.5.1 *Bypassing the Offset Corrector Block*

When the offset corrector is bypassed, offset mismatch among interleaving ADC cores appears in the ADC output spectrum. To correct the effects of mismatch, place the ADC in an idle channel state (no signal at the ADC inputs) and the corrector must be allowed to run for some time to estimate the mismatch, then the corrector is frozen so that the last estimated value is held. Required register writes are provided in Table 131.

**Table 131. Freezing and Bypassing the Offset Corrector Block**

| STEP | REGISTER WRITE | COMMENT |
|---|---|---|
| **STEPS FOR FREEZING THE CORRECTOR BLOCK** | | |
| 1 | — | Signal source is turned off. The device detects an idle channel at its input. |
| 2 | — | Wait for at least 0.4 ms for the corrector to estimate the internal offset |
| 3 | Address 4001h, value 00h | Select the offset corr page |
| | Address 4002h, value 00h | |
| | Address 4003h, value 00h | |
| | Address 4004h, value 61h | |
| | Address 6068h, value C2h | Freeze the corrector |
| 4 | — | Signal source can now be turned on |
| **STEPS FOR BYPASSING THE CORRECTOR BLOCK** | | |
| 1 | Address 4001h, value 00h | — |
| | Address 4002h, value 00h | |
| | Address 4003h, value 00h | |
| | Address 4004h, value 61h | Select the offset corr page |
| | Address 6068h, value 46h | Disable the corrector |

#### 9.1.5.1.1 Effect of Temperature

Figure 268 and Figure 269 show the behavior of $nf_S$ / 8 tones with respect to temperature when the offset corrector block is frozen or disabled.

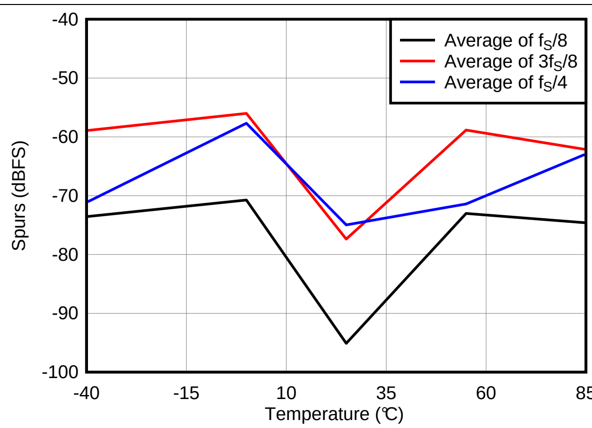



**Figure 268. Offset Corrector Block Frozen at Room Temperature**

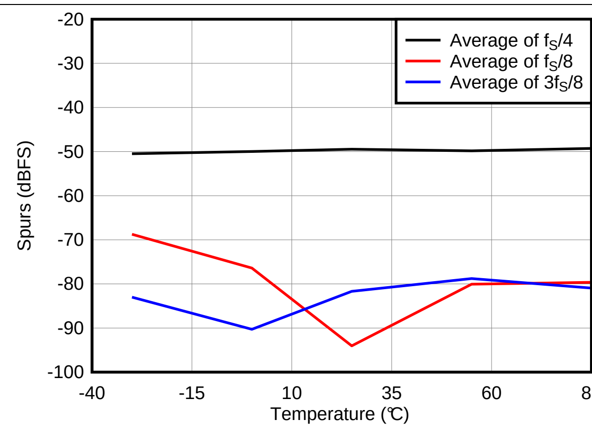



**Figure 269. Offset Corrector Block Disabled**

## 9.2 Typical Application

The ADC31RF80 is designed for wideband receiver applications demanding high dynamic range over a large input frequency range. Figure 270 shows a typical schematic for an ac-coupled receiver.

Decoupling capacitors with low ESL are recommended to be placed as close as possible at the pins indicated in Figure 270. Additional capacitors can be placed on the remaining power pins.

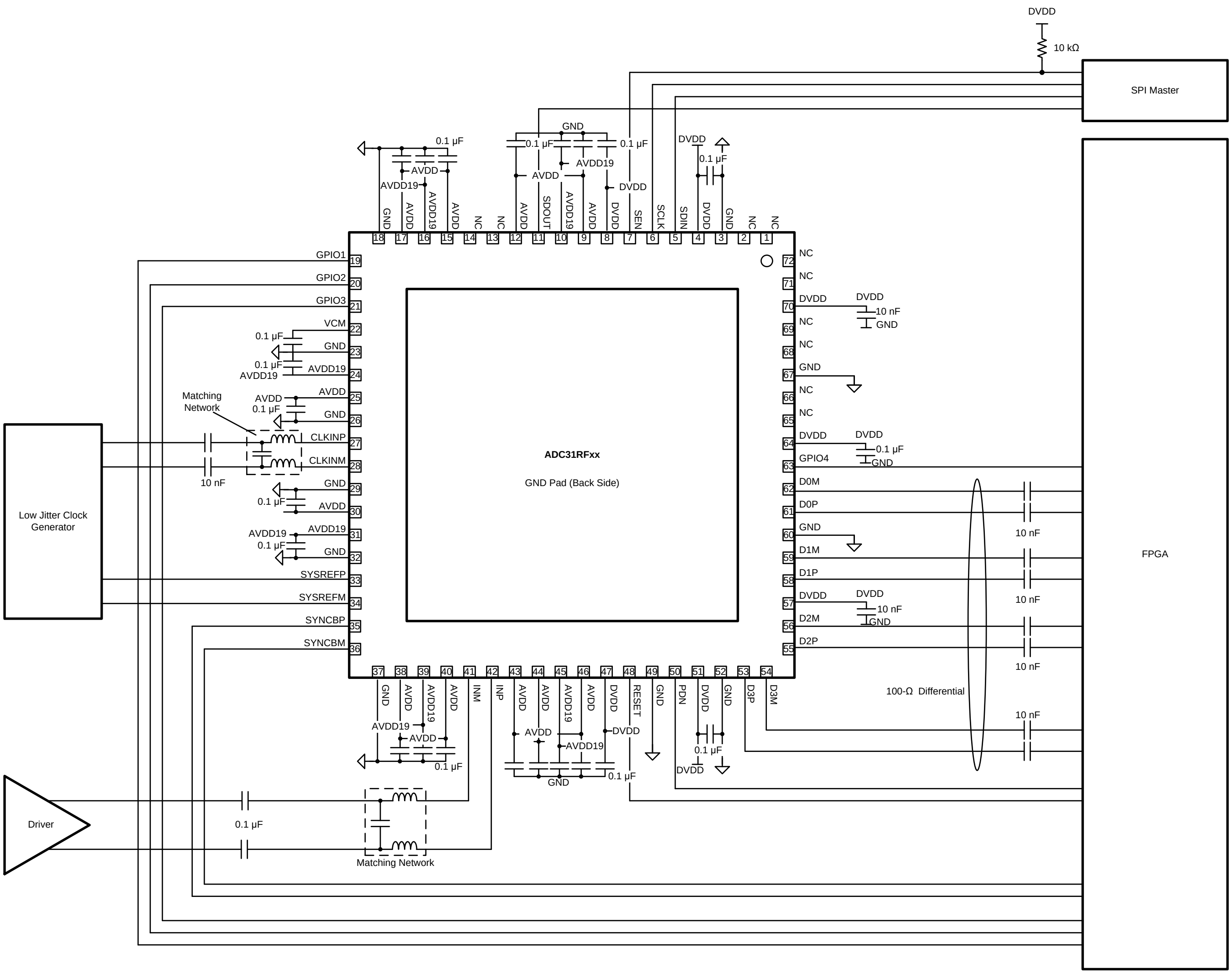





**Figure 270. Typical Application Implementation Diagram**

## Typical Application (continued)

### 9.2.1 Design Requirements

#### *9.2.1.1 Transformer-Coupled Circuits*

Typical applications involving transformer-coupled circuits are discussed in this section. To ensure good amplitude and phase balance at the analog inputs, transformers (such as TC1-1-13 and TC1-1-43) can be used from the dc to 1000-MHz range and from the 1000-MHz to 4-GHz range of input frequencies, respectively. When designing the driving circuits, the ADC input impedance (or SDD11) must be considered.

By using the simple drive circuit of Figure 271, uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

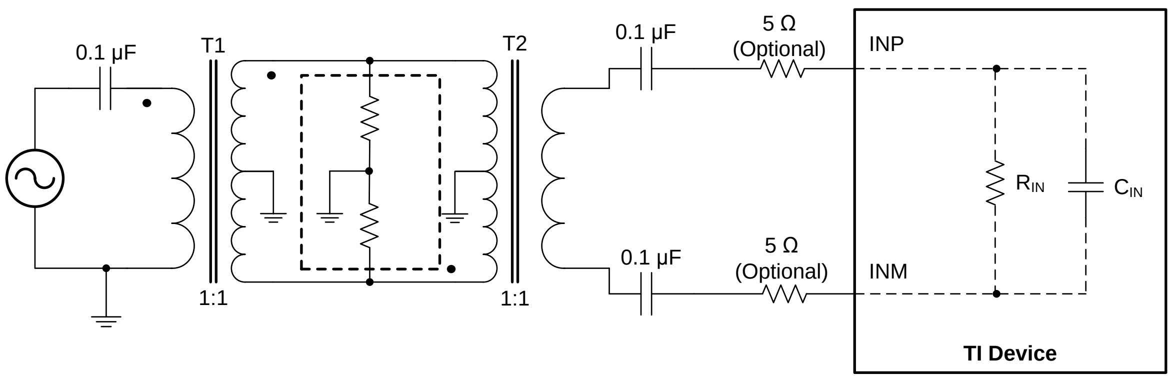




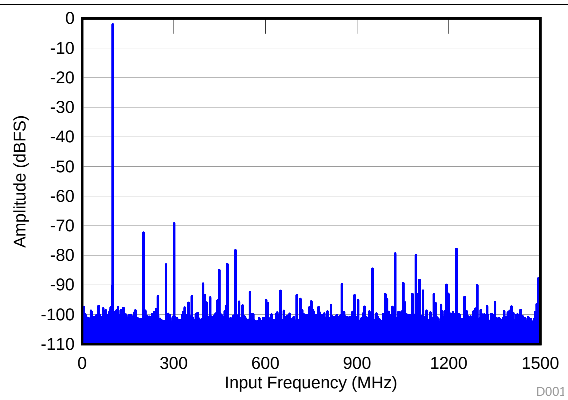

**Figure 271. Input Drive Circuit**

### 9.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin, as shown in Figure 271, is recommended to damp out ringing caused by package parasitics.

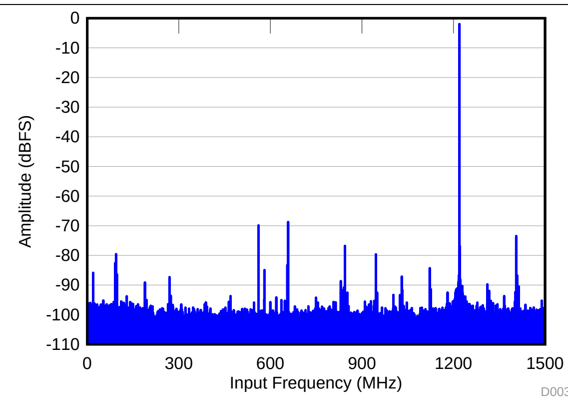
### 9.2.3 Application Curves

Figure 272 and Figure 273 show the typical performance at 100 MHz and 1780 MHz, respectively.




SNR = 61.8 dBFS, SINAD = 61.2 dBFS,
HD2 = 71 dBc, HD3 = 75 dBc, SFDR = 71 dBc,
THD = 68 dBc, IL spur = 77 dBc, worst spur = 73 dBc

**Figure 272. FFT for 100-MHz Input Frequency**




SNR = 57.9 dBFS, SINAD = 57.1 dBFS,
HD2 = 63 dBc, HD3 = 66 dBc, SFDR = 63 dBc,
THD = 60 dBc, IL spur = 79 dBc, worst spur = 77 dBc

**Figure 273. FFT for 1780-MHz Input Frequency**

# 10 Power Supply Recommendations

As shown in Figure 274, the DVDD power supply (1.15 V) must be stable before ramping up the AVDD19 supply (1.9 V). The AVDD supply (1.15 V) can come up in any order during the power sequence. The power supplies can ramp up at any rate and there is no hard requirement for the time delay between DVDD (1.15 V) ramping up to AVDD (1.9 V) ramping up (which can be in orders of microseconds but is recommended to be a few milliseconds).

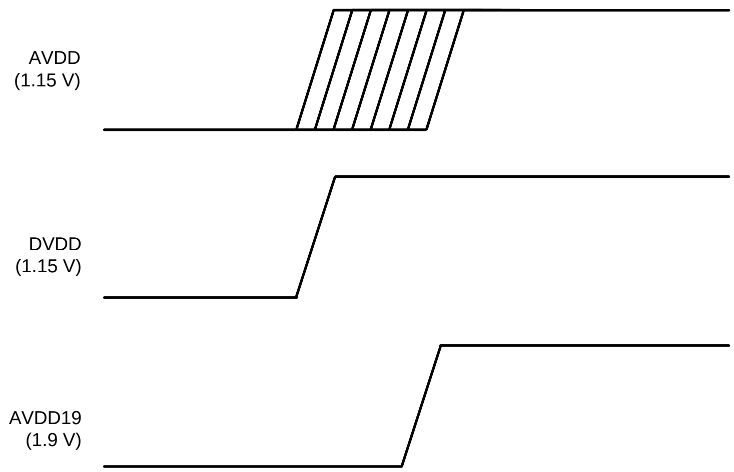



**Figure 274. Power Sequencing for the ADC31RF80 Family of Devices**

# 11 Layout

## 11.1 Layout Guidelines

The device evaluation module (EVM) layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 275. The *ADC32RF45/RF80 EVM Quick Startup Guide* provides a complete layout of the EVM. Some important points to remember during board layout are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pinout in opposite directions, as shown in the reference layout of Figure 275 as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling. This configuration is also maintained on the reference layout of Figure 275 as much as possible.
- Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as field-programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs)] must be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD, DVDD, or AVDD19), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

## 11.2 Layout Example

Figure 275 is an example for the dual-channel device, the ADC32RF80, which shares the same pin-out. For the ADC31RF80, the unused channel is not required to be connected to the board and can be left floating.

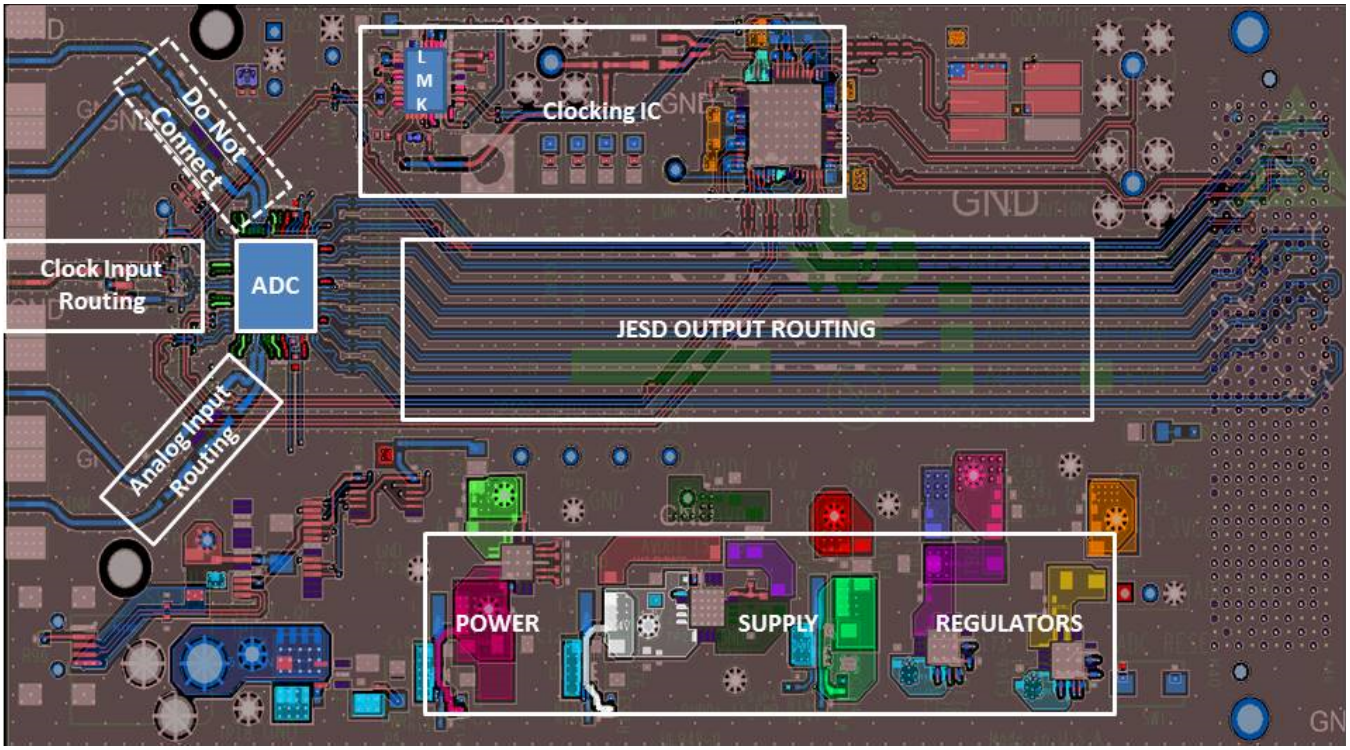



**Figure 275. ADC32RF80EVM Layout**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- *ADC32RF45/RF80 EVM Quick Startup Guide*
- *Configuration Files for the ADC32RF45*

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ADC31RF80IRMP | Active | Production | VQFN (RMP) \| 72 | 168 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ31RF80 |
| ADC31RF80IRMP.A | Active | Production | VQFN (RMP) \| 72 | 168 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ31RF80 |
| ADC31RF80IRMPT | Active | Production | VQFN (RMP) \| 72 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ31RF80 |
| ADC31RF80IRMPT.A | Active | Production | VQFN (RMP) \| 72 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ31RF80 |
| ADC31RF80IRMPTG4 | Active | Production | VQFN (RMP) \| 72 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ31RF80 |
| ADC31RF80IRMPTG4.A | Active | Production | VQFN (RMP) \| 72 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ31RF80 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

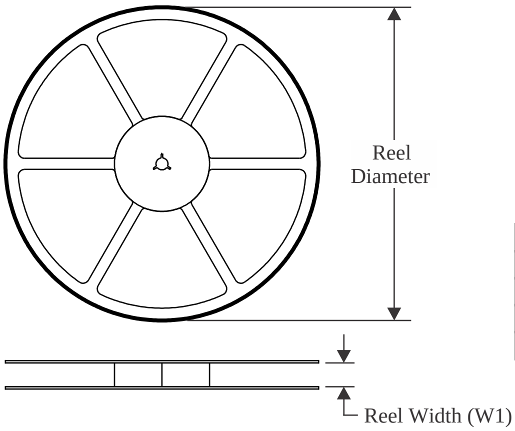
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

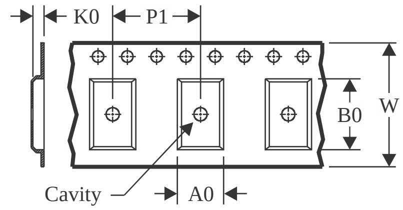
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

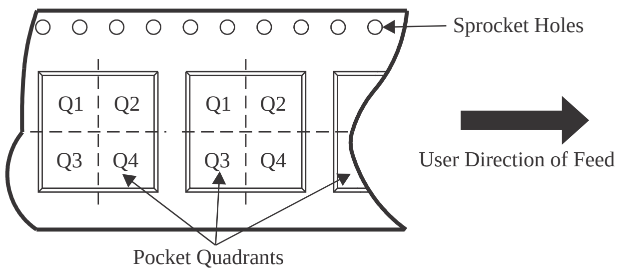



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

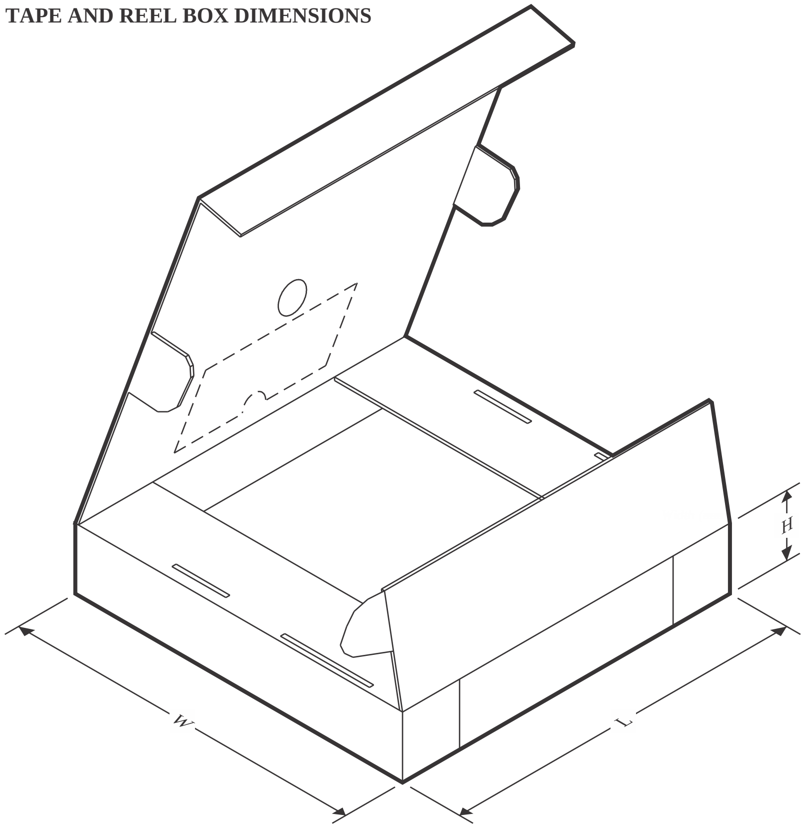
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC31RF80IRMPT | VQFN | RMP | 72 | 250 | 180.0 | 24.4 | 10.25 | 10.25 | 2.25 | 16.0 | 24.0 | Q2 |
| ADC31RF80IRMPTG4 | VQFN | RMP | 72 | 250 | 180.0 | 24.4 | 10.25 | 10.25 | 2.25 | 16.0 | 24.0 | Q2 |

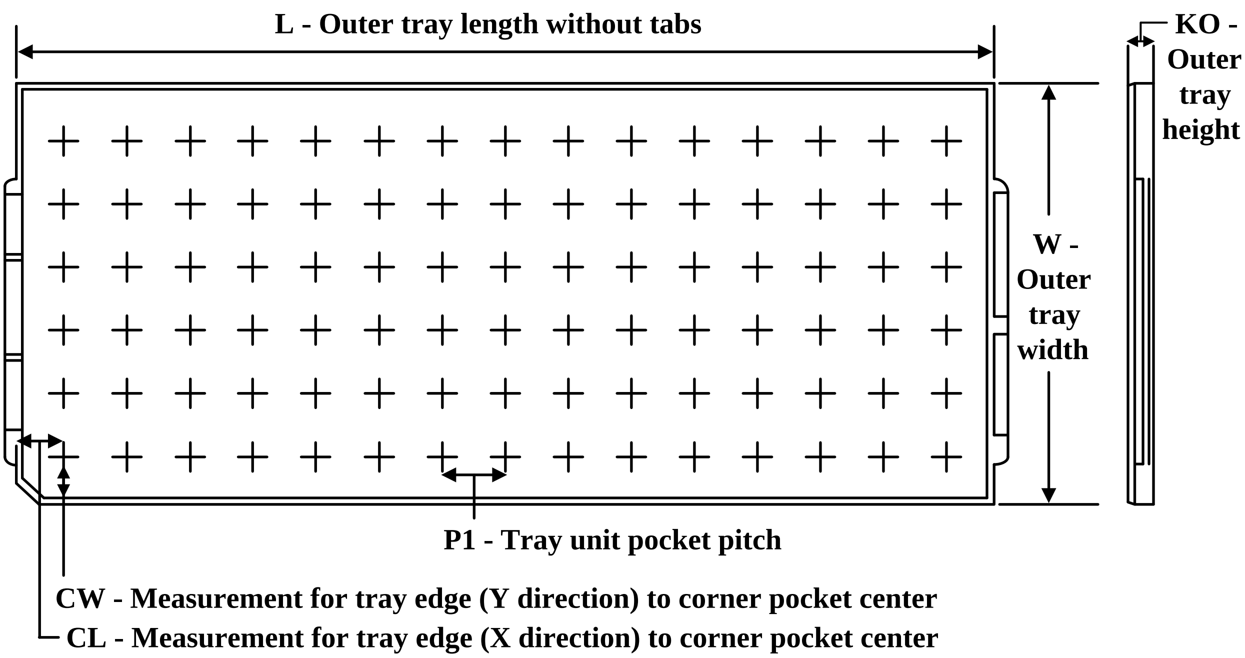
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADC31RF80IRMPT | VQFN | RMP | 72 | 250 | 213.0 | 191.0 | 55.0 |
| ADC31RF80IRMPTG4 | VQFN | RMP | 72 | 250 | 213.0 | 191.0 | 55.0 |

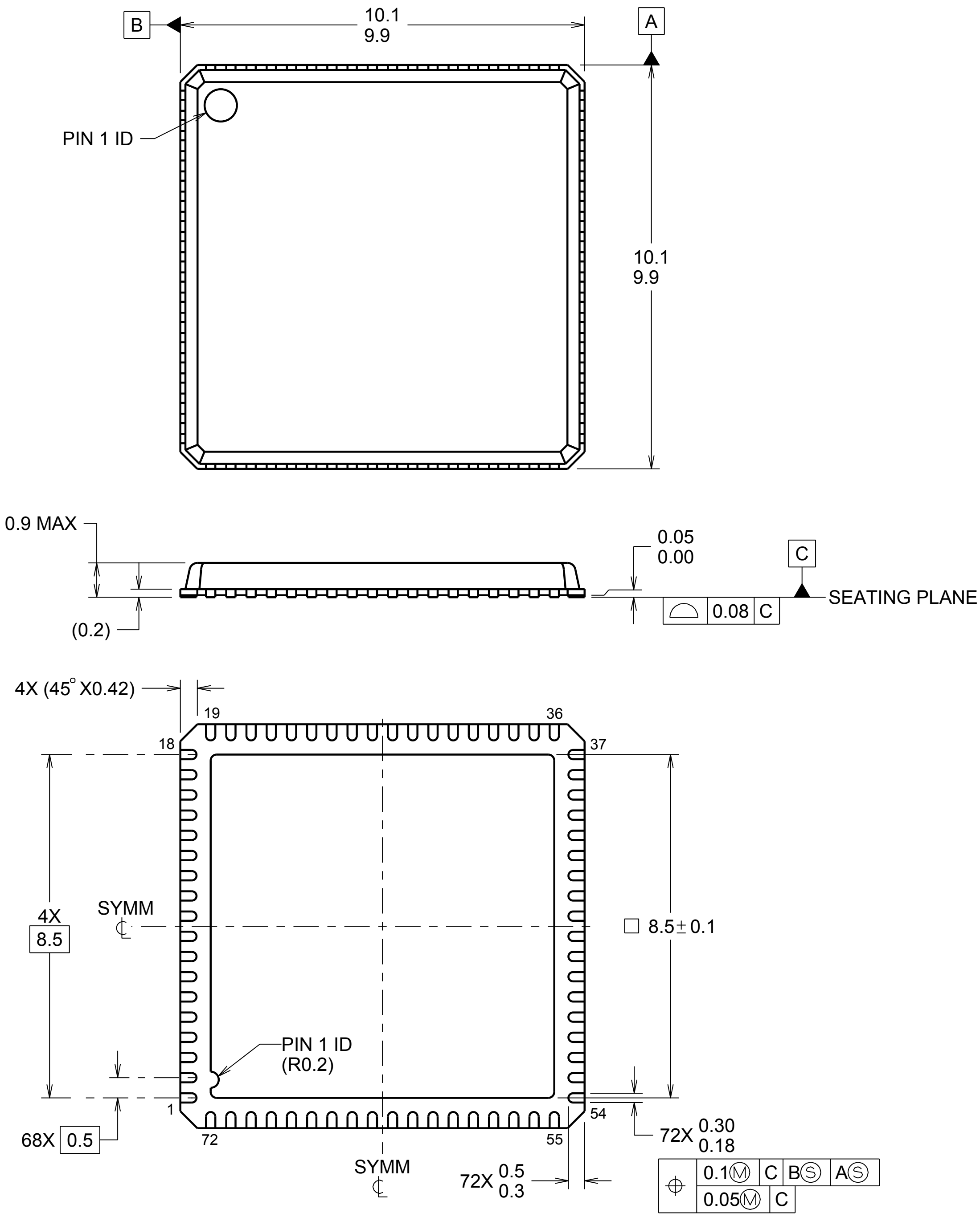
## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC31RF80IRMP | RMP | VQFNP | 72 | 168 | 8 X 21 | 150 | 315 | 135.9 | 7620 | 14.65 | 11 | 11.95 |
| ADC31RF80IRMP.A | RMP | VQFNP | 72 | 168 | 8 X 21 | 150 | 315 | 135.9 | 7620 | 14.65 | 11 | 11.95 |

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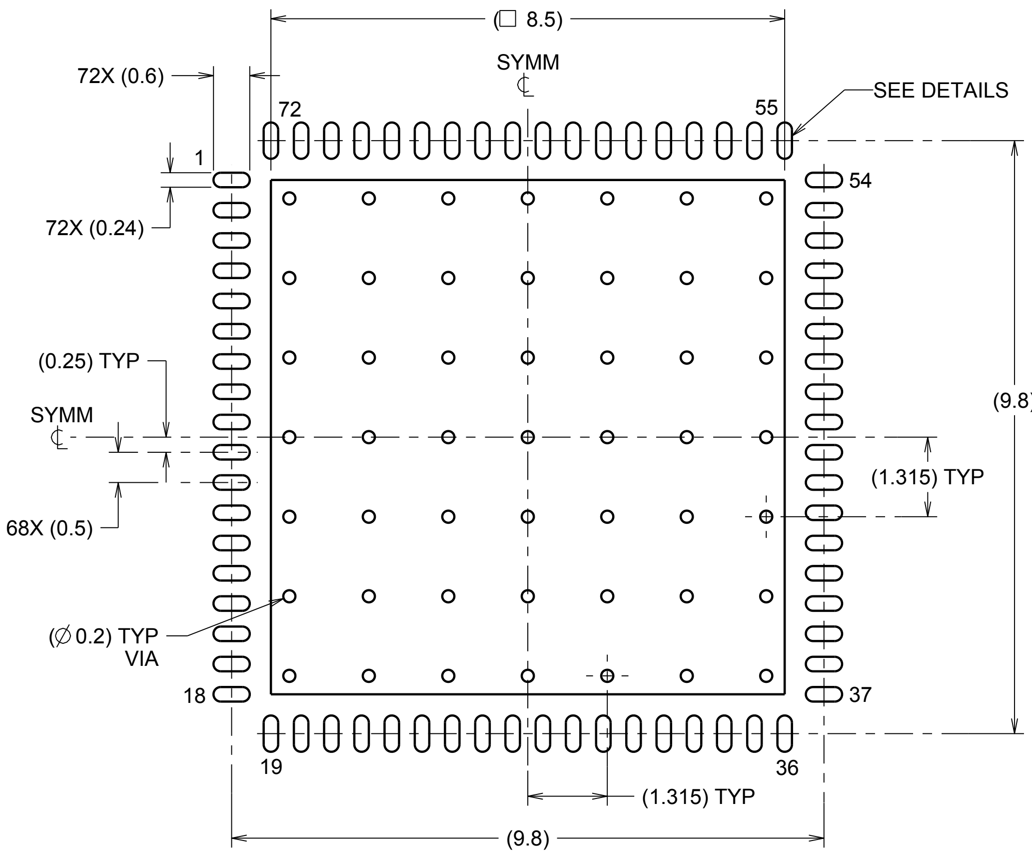
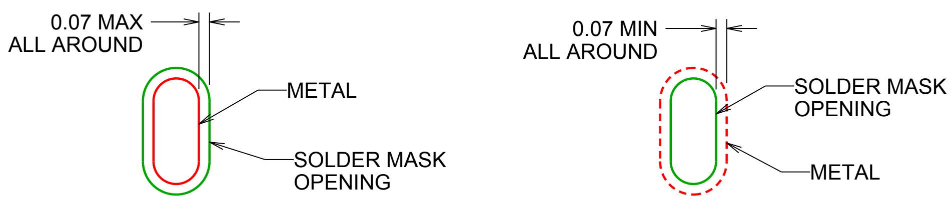
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:8X




NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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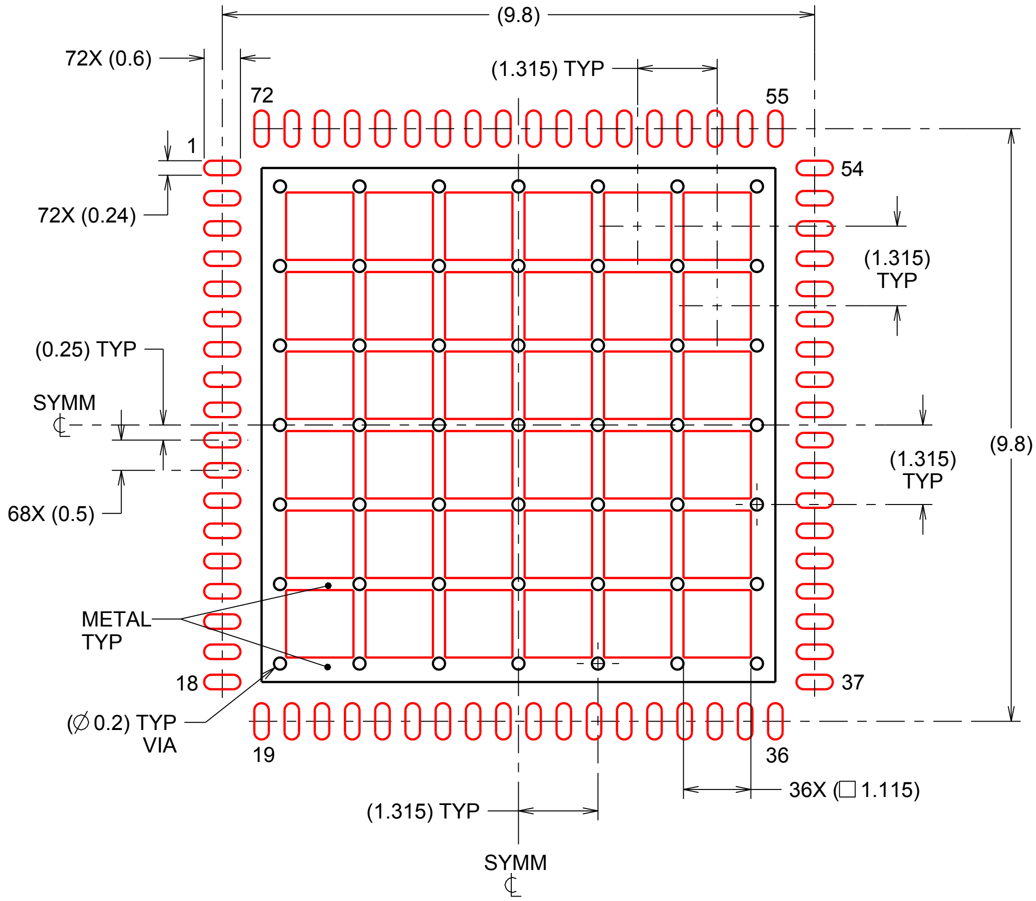
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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