ADC14155QML-SP, radiation hardened, 14-Bit, 155-MSPS, 1.1-GHz bandwidth A/D converter

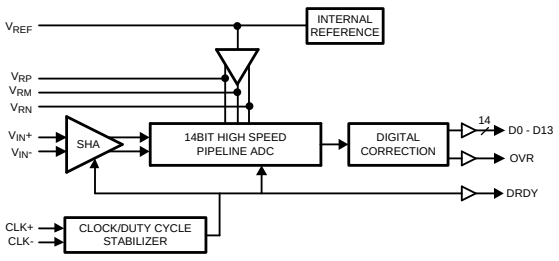
1 Features

- 5962R0626201VXC
  - Total Ionizing Dose (TID) 100 krad(Si)
  - Single Event Latch-up 120 MeV-cm^2/mg (See Radiation Reports)
- 1.1-GHz Full-Power Bandwidth
- Internal Sample-and-Hold Circuit
- Low-Power Consumption
- Internal Precision 1-V Reference
- Single-Ended or Differential Clock Modes
- Data Ready Output Clock
- Clock Duty Cycle Stabilizer
- Dual 3.3-V and 1.8-V Supply Operation (±10%)
- Power-Down Mode
- Offset Binary or 2's Complement Output Data Format
- 48-pin CFP Package (11.5-mm × 11.5-mm, 0.635-mm Pin-Pitch)
- Key Specifications
  - Resolution 14 Bits
  - Conversion Rate 155 MSPS
  - SNR (f_{IN} = 70 MHz) 70.1 dBFS (typ)
  - SFDR (f_{IN} = 70 MHz) 82.3 dBFS (typ)
  - ENOB (f_{IN} = 70 MHz) 11.3 Bits (typ)
  - Full-Power Bandwidth 1.1 GHz (typ)
  - Power Consumption 967 mW (typ)

2 Applications

- High IF Sampling Receivers
- Power Amplifier Linearization
- Multi-Carrier, Multi-Mode Receivers
- Test and Measurement Equipment
- Communications Instrumentation
- Radar Systems

Block Diagram



3 Description

The ADC14155QML-SP is a high-performance CMOS analog-to-digital converter capable of converting analog input signals into 14-bit digital words at rates up to 155 MSPS. This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and the external component count, while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1.1 GHz. The ADC14155 operates from dual 3.3-V and 1.8-V power supplies and consumes 967 mW of power at 155 MSPS.

The separate 1.8-V supply for the digital output interface allows lower power operation with reduced noise. A power-down feature reduces the power consumption to 5 mW with the clock input disabled, while still allowing fast wake-up time to full operation. The differential inputs provide a full scale differential input swing equal to 2 times the reference voltage. A stable 1-V internal voltage reference is provided, or the ADC14155 can be operated with an external reference. The Clock mode (differential versus single-ended) and output data format (offset binary versus 2's complement) are pin-selectable. A duty cycle stabilizer maintains performance over a wide range of clock duty cycles.

The ADC14155QML-SP is available in a 48-lead thermally enhanced multi-layer ceramic quad package and operates over the military temperature range of –55°C to +125°C.

Device Information(1)

PART NUMBER	GRADE	PACKAGE
5962R0626201VXC	QMLV RHA (SMD part) [100 krad]	CQFP (48)
ADC14155W-MLS	Flight RHA (non-SMD part) [100 krad]	CQFP (48)
ADC14155W-MPR	Engineering Samples(2)	CQFP (48)
ADC14155LCVAL	Low-Frequency Ceramic Evaluation Board	—
ADC14155HCVAL	High-Frequency Ceramic Evaluation Board	—

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (September 2018) to Revision L — **Page**

- Added Figure 20 ... 17

Changes from Revision J (March 2018) to Revision K — **Page**

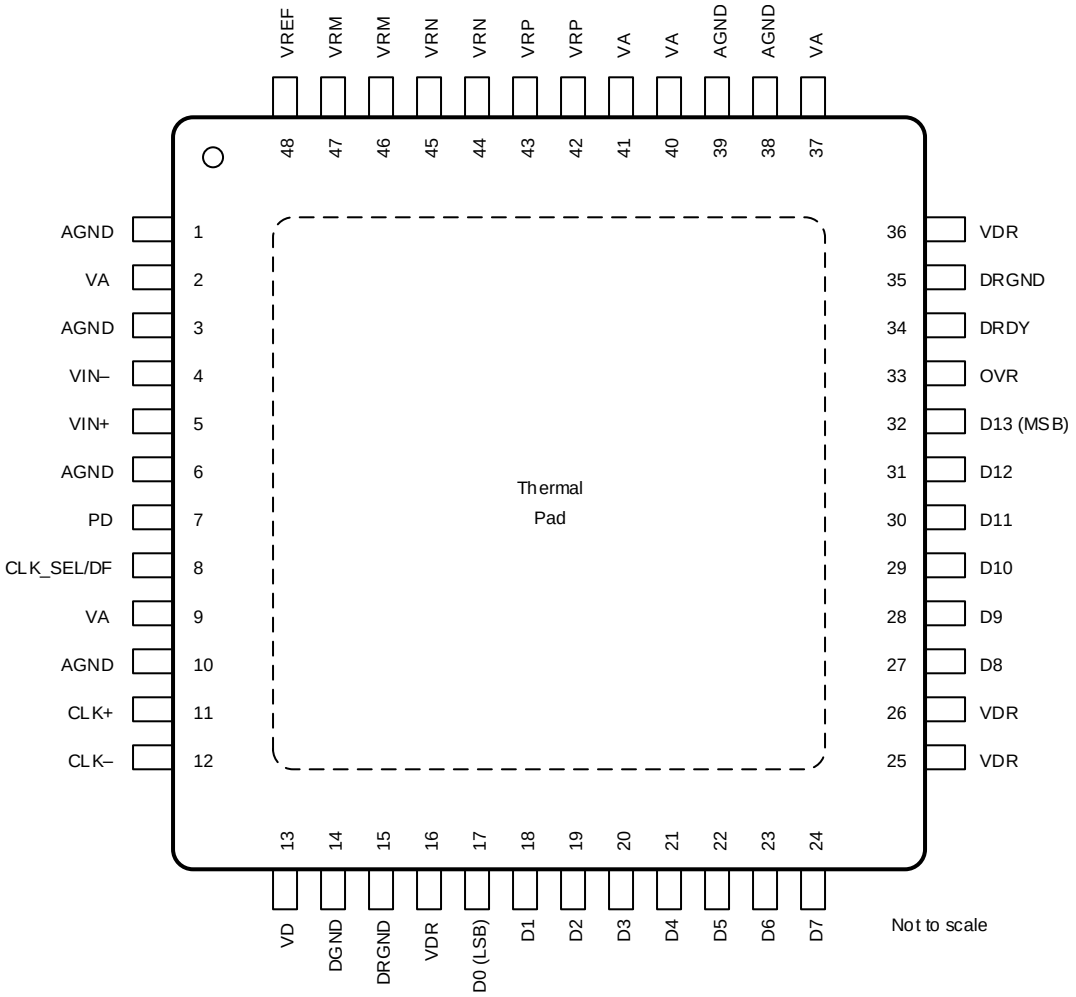
- Deleted inconsistent footnotes ... 6
- Added standardized thermal values ... 6
- Changed formatting of temperature conditions in the spec tables ... 7
- Added subgroups to all applicable specs ... 7
- Changed location of 12.1-Ω capacitor on V_{IN-} pin in the circuit diagram of the *Typical Application* section ... 24

Changes from Revision I (March 2013) to Revision J — **Page**

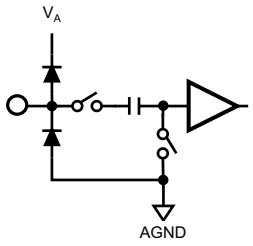
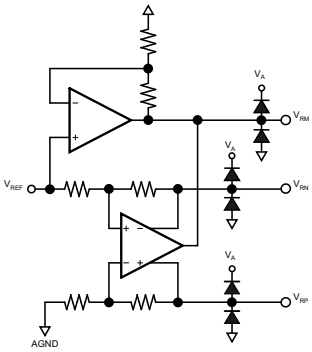
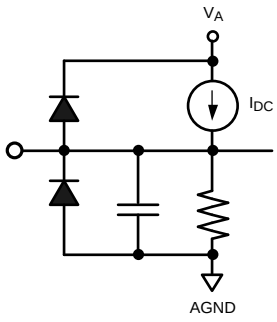
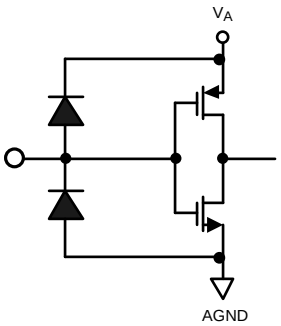
- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted DYNAMIC CONVERTER CHARACTERISTICS, A_{IN} = –1 dBFS duplicate specs ... 9

5 Pin Configuration and Functions

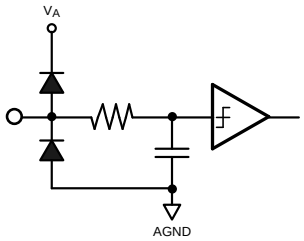
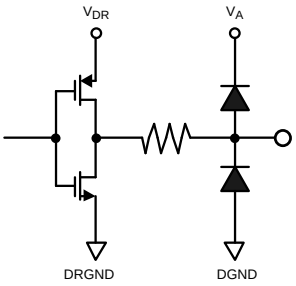
NBA Package
48-Pin CFP
Top View



Pin Descriptions and Equivalent Circuits

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
ANALOG I/O			
4	V_{IN-}		Differential analog input pins. The differential full-scale input signal level is two times the reference voltage with each input pin signal centered on a common mode voltage, V_{CM}.
5	V_{IN+}		
42, 43	V_{RP}		These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 0.1-µF capacitor placed very close to the pin to minimize stray inductance. A 0.1-µF capacitor should be placed between V_{RP} and V_{RN} as close to the pins as possible, and a 10-µF capacitor should be placed in parallel. V_{RP} and V_{RN} should not be loaded. V_{RM} may be loaded to 1mA for use as a temperature stable 1.5-V reference. It is recommended to use V_{RM} to provide the common mode voltage, V_{CM}, for the differential analog inputs, V_{IN}+ and V_{IN}–.
46, 47	V_{RM}		
44, 45	V_{RN}		
48	V_{REF}		This pin can be used as either the 1-V internal reference voltage output (internal reference operation) or as the external reference voltage input (external reference operation). To use the internal reference, V_{REF} should be decoupled to AGND with a 0.1-µF, low equivalent series inductance (ESL) capacitor. In this mode, V_{REF} defaults as the output for the internal 1.0-V reference. To use an external reference, overdrive this pin with a low noise external reference voltage. The output impedance of the internal reference at this pin is 9kΩ. Therefore, to overdrive this pin, the impedance of the external reference source should be << 9 kΩ. This pin should not be used to source or sink current. The full scale differential input voltage range is 2 * V_{REF}.
DIGITAL I/O			
11	CLK+		The clock input pins can be configured to accept either a single-ended or a differential clock input signal. When the single-ended clock mode is selected through CLK_SEL/DF (pin 8), connect the clock input signal to the CLK+ pin and connect the CLK– pin to AGND. When the differential clock mode is selected through CLK_SEL/DF (pin 8), connect the positive and negative clock inputs to the CLK+ and CLK– pins, respectively. The analog input is sampled on the falling edge of the clock input.
12	CLK–		

Pin Descriptions and Equivalent Circuits (continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
8	CLK_SEL/DF		This is a four-state pin controlling the input clock mode and output data format. CLK_SEL/DF = V_A, CLK+ and CLK– are configured as a differential clock input. The output data format is 2's complement. CLK_SEL/DF = (2 / 3) * V_A, CLK+ and CLK– are configured as a differential clock input. The output data format is offset binary. CLK_SEL/DF = (1 / 3) * V_A, CLK+ is configured as a single-ended clock input and CLK– should be tied to AGND. The output data format is 2's complement. CLK_SEL/DF = AGND, CLK+ is configured as a single-ended clock input and CLK– should be tied to AGND. The output data format is offset binary.
7	PD		This is a two-state input controlling Power Down. PD = V_A, Power Down is enabled. In the Power Down state only the reference voltage circuitry remains active and power dissipation is reduced. PD = AGND, Normal operation.
17-24, 27-32	D0–D13		Digital data output pins that make up the 14-bit conversion result. D0 (pin 17) is the LSB, while D13 (pin 32) is the MSB of the output word. Output levels are CMOS compatible.
33	OVR		Over-Range Indicator. This output is set HIGH when the input amplitude exceeds the 14-bit conversion range (0 to 16383).
34	DRDY		Data Ready Strobe. This pin is used to clock the output data. It has the same frequency as the sampling clock. One word of data is output in each cycle of this signal. The rising edge of this signal should be used to capture the output data.
ANALOG POWER			
2, 9, 37, 40, 41	V_A		Positive analog supply pins. These pins should be connected to a quiet 3.3-V source and be bypassed to AGND with 100-pF and 0.1-µF capacitors located close to the power pins.
1, 3, 6, 10, 38, 39	AGND		The ground return for the analog supply.
DIGITAL POWER			
13	V_D		Positive digital supply pin. This pin should be connected to a quiet 3.3-V source and be bypassed to DGND with a 100-pF and 0.1-µF capacitor located close to the power pin.
14	DGND		The ground return for the digital supply.
16, 25, 26, 36	V_{DR}		Positive driver supply pin for the output drivers. This pin should be connected to a quiet voltage source of 1.8 V and be bypassed to DRGND with 100-pF and 0.1-µF capacitors located close to the power pins.
15, 35	DRGND		The ground return for the digital output driver supply. These pins should be connected to the system digital ground. See Layout Guidelines (Layout and Grounding) for more details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply voltage (V_A, V_D)	–0.3	4.2	V
Supply voltage (V_{DR})	–0.3	2.35	V
$\|V_A–V_D\|$		100	mV
Voltage on any input pin (not to exceed 4.2 V)	–0.3	V_A + 0.3	V
Voltage on any output pin (not to exceed 2.35 V)	–0.3	V_{DR} + 0.2	V
Input current at any pin other than supply pins	–5	5	mA
Package input current	–50	50	mA
Max junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = AGND = DGND = DRGND = 0 V, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	NOM	MAX	UNIT
Operating temperature	–55		125	°C
Supply voltage (V_A, V_D)	3		3.6	V
Output driver supply (V_{DR})	1.6		2	V
CLK	–0.05		V_A + 0.05	V
Clock duty cycle	30%		70%	
Analog input pins	0		2.6	V
V_{CM}	1.4		1.6	V
|AGND-DGND|(2)			100	mV

(1) All voltages are measured with respect to GND = AGND = DGND = DRGND = 0 V, unless otherwise specified.
(2) All GND voltages should be within 100mv of each other.

6.4 Thermal Information

THERMAL METRIC		ADC14155QML NBA (CFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.1	°C/W
$R_{\theta JC(bottom)}$(1)	Junction-to-case (bottom) thermal resistance	3.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

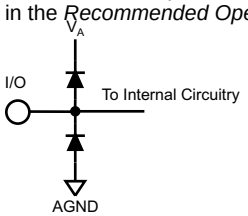
6.5 ADC14155 Converter Electrical Characteristics DC Parameters(1)

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0 V, V_A = V_D = 3.3 V, V_{DR} = 1.8 V, Internal V_{REF} = 1 V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Differential Analog Input, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. (2)(3)(4)(5)

PARAMETER		TEST CONDITIONS	NOTES	TYP(6)	MIN	MAX	UNITS	SUB-GROUPS
STATIC CONVERTER CHARACTERISTICS								
	Resolution with no missing codes				14		Bits	[1, 2, 3]
INL	Integral non linearity		See(7)	2.3	–5.0	5.0	LSB	[1, 2, 3]
DNL	Differential non linearity			±0.5	–0.9	1.1	LSB	[1, 2, 3]
PGE	Maximum positive gain error			0.1	–3.3	3.5	%FS	[1, 2, 3]
NGE	Maximum negative gain error			0.3	–3.3	3.9	%FS	[1, 2, 3]
TC GE	Gain error tempco	–55°C ≤ T_A ≤ +125°C		0.007			Δ%FS/°C	
V_{OFF}	Offset error (V_{IN+} = $V_{IN–}$)			–0.1	0.7	–0.9	%FS	[1, 2, 3]
TC V_{OFF}	Offset error tempco	–55°C ≤ T_A ≤ +125°C		0.0001			Δ%FS/°C	
	Under range output code			0	0	0		
	Over range output code			16383	16383	16383		
REFERENCE AND ANALOG INPUT CHARACTERISTICS								
V_{CM}	Common mode input voltage			1.5			V	
V_{RM}	Reference ladder midpoint output voltage	Output load = 1 mA		1.5			V	
C_{IN}	V_{IN} input capacitance (each pin to GND)	V_{IN} = 1.5 Vdc ± 0.5 V(CLK LOW)	See(8)	9			pF	
		V_{IN} = 1.5 Vdc ± 0.5 V(CLK HIGH)	See(8)	6			pF	
V_{REF}	Reference voltage		See(9)	1.00			V	
	Reference input resistance			9			kΩ	

(1) Pre and post irradiation limits are identical to those listed in the *Electrical Characteristics* tables. Radiation testing is performed per MIL-STD-883, Test Method 1019.

(2) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per Note 5. However, errors in the A/D conversion can occur if the input goes above 2.6 V or below GND as described in the *Recommended Operating Conditions* section.



(3) To ensure accuracy, it is required that $|V_A – V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.

(4) With the test condition for V_{REF} = 1 V (2-V_{P-P} differential input), the 14-bit LSB is 122.1 µV.

(5) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to ±5 mA. The ±50-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

(6) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

(7) Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.

(8) The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.

(9) Optimum performance will be obtained by keeping the reference input in the 0.9-V to 1.1-V range. The LM4051CIM3-ADJ (SOT-23 package) is recommended for external reference applications.

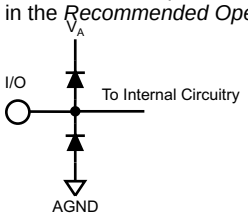
6.6 ADC14155 Converter Electrical Characteristics (Continued) DYNAMIC Parameters(1)

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0 V, V_A = V_D = 3.3 V, V_{DR} = 1.8 V, Internal V_{REF} = 1 V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Differential Analog Input, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. (2)(3)(4)(5)

PARAMETER		TEST CONDITIONS	NOTES	TYP(6)	MIN	MAX	UNITS	SUB-GROUPS
DYNAMIC CONVERTER CHARACTERISTICS, A_{IN} = -1 dBFS								
FPBW	Full power bandwidth	-1 dBFS Input, -3 dB Corner		1.1			GHz	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		69			dBFS	
		f_{IN} = 70 MHz		70.1	66.7		dBFS	[4, 5, 6]
		f_{IN} = 169 MHz		68.5			dBFS	
		f_{IN} = 238 MHz		68.5			dBFS	
		f_{IN} = 398 MHz		66.4			dBFS	
SFDR	Spurious free dynamic range	f_{IN} = 10 MHz		82			dBFS	
		f_{IN} = 70 MHz		82.3	68.2		dBFS	[4, 5, 6]
		f_{IN} = 169 MHz		80.5			dBFS	
		f_{IN} = 238 MHz		77.3			dBFS	
		f_{IN} = 398 MHz		63.5			dBFS	
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.3			Bits	
		f_{IN} = 70 MHz		11.3	10.7		Bits	[4, 5, 6]
		f_{IN} = 169 MHz		11.0			Bits	
		f_{IN} = 238 MHz		11.0			Bits	
		f_{IN} = 398 MHz		10.0			Bits	
THD	Total harmonic disortion	f_{IN} = 10 MHz		–81			dBFS	
		f_{IN} = 70 MHz		–79.9		–67	dBFS	[4, 5, 6]
		f_{IN} = 169 MHz		–82.4			dBFS	
		f_{IN} = 238 MHz		–76.6			dBFS	
		f_{IN} = 398 MHz		–63.2			dBFS	
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		–95.4			dBFS	
		f_{IN} = 70 MHz		–88.5		–70	dBFS	[4, 5, 6]
		f_{IN} = 169 MHz		–88.3			dBFS	
		f_{IN} = 238 MHz		–77.3			dBFS	
		f_{IN} = 398 MHz		–60.9			dBFS	

(1) Pre and post irradiation limits are identical to those listed in the *Electrical Characteristics* tables. Radiation testing is performed per MIL-STD-883, Test Method 1019.

(2) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per Note 5. However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the *Recommended Operating Conditions* section.



(3) To ensure accuracy, it is required that $|V_A – V_D| \leq 100$ mV and separate bypass capacitors are used at each power supply pin.

(4) With the test condition for V_{REF} = 1 V (2-V_{P-P} differential input), the 14-bit LSB is 122.1 µV.

(5) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

(6) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

ADC14155 Converter Electrical Characteristics (Continued) DYNAMIC Parameters[1] (continued)

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0 V, V_A = V_D = 3.3 V, V_{DR} = 1.8 V, Internal V_{REF} = 1 V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Differential Analog Input, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. [2][3][4][5]

PARAMETER		TEST CONDITIONS	NOTES	TYP[6]	MIN	MAX	UNITS	SUB-GROUPS
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		–81.6			dBFS	
		f_{IN} = 70 MHz		–82.3		–68	dBFS	[4, 5, 6]
		f_{IN} = 169 MHz		–86.4			dBFS	
		f_{IN} = 238 MHz		–89.0			dBFS	
		f_{IN} = 398 MHz		–80.5			dBFS	
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		68.2			dBFS	
		f_{IN} = 70 MHz		69.9	66.2		dBFS	[4, 5, 6]
		f_{IN} = 169 MHz		68.3			dBFS	
		f_{IN} = 238 MHz		67.8			dBFS	
		f_{IN} = 398 MHz		61.5			dBFS	

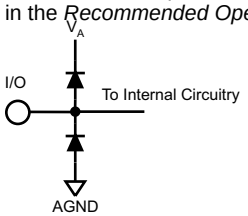
6.7 ADC14155 Converter Electrical Characteristics (Continued) Logic and Power Supply Electrical Characteristics[1]

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0 V, V_A = V_D = 3.3 V, V_{DR} = 1.8 V, Internal V_{REF} = 1 V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Differential Analog Input, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. [2][3][4][5]

PARAMETER		TEST CONDITIONS	NOTES	TYP[6]	MIN	MAX	UNITS	SUB-GROUPS
DIGITAL INPUT CHARACTERISTICS (CLK, PD/DCS, CLK_SEL/DF)								
$V_{IN(1)}$	Logical “1” input voltage	V_D = 3.6 V	See[7]		2.0		V	[1, 2, 3]
$V_{IN(0)}$	Logical “0” input voltage	V_D = 3.0 V				0.8	V	[1, 2, 3]
$I_{IN(1)}$	Logical “1” input current	V_{IN} = 3.3 V		10			µA	
$I_{IN(0)}$	Logical “0” input current	V_{IN} = 0 V		–10			µA	
C_{IN}	Digital input capacitance			5			pF	
DIGITAL OUTPUT CHARACTERISTICS (D0–D13, DRDY, OVR)								
V_{OH}	Output logic high	I_{OUT} = –0.5 mA , V_{DR} = 1.8 V	See[7]	1.55	1.2		V	[1, 2, 3]
V_{OL}	Output logic low	I_{OUT} = 1.6 mA, V_{DR} = 1.8 V	See[7]	0.15		0.4	V	[1, 2, 3]
$+I_{SC}$	Output short circuit source current	V_{OUT} = 0 V		–10			mA	
$–I_{SC}$	Output short circuit sink current	V_{OUT} = V_{DR}		10			mA	
C_{OUT}	Digital output capacitance			5			pF	
POWER SUPPLY CHARACTERISTICS								
I_A	Analog supply current	Full operation		283		350	mA	[1, 2, 3]
I_D	Digital supply current	Full operation		10		11	mA	[1, 2, 3]
I_{DR}	Digital output supply current	Full operation	See[8]	15			mA	
	Power consumption	Excludes I_{DR}		967		1170	mW	[1, 2, 3]
	Power down power consumption	Clock disabled		5			mW	

(1) Pre and post irradiation limits are identical to those listed in the *Electrical Characteristics* tables. Radiation testing is performed per MIL-STD-883, Test Method 1019.

(2) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per Note 5. However, errors in the A/D conversion can occur if the input goes above 2.6 V or below GND as described in the *Recommended Operating Conditions* section.



(3) To ensure accuracy, it is required that $|V_A – V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.

(4) With the test condition for V_{REF} = 1 V (2-V_{P-P} differential input), the 14-bit LSB is 122.1 µV.

(5) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to ±5 mA. The ±50-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

(6) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

(7) Specified by characterization.

(8) I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). I_{DR} = V_{DR}(C_0 × f_0 + C_1 × f_1 +....C_{11} × f_{11}) where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.

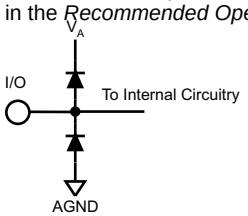
6.8 ADC14155 Converter Electrical Characteristics (Continued) Timing and AC Characteristics[1]

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0 V, V_A = V_D = 3.3 V, V_{DR} = 1.8 V, Internal V_{REF} = 1 V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Differential Analog Input, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C[2][3][4][5]

PARAMETER		TEST CONDITIONS	NOTES	TYP[6]	MIN	MAX	UNITS	SUB-GROUPS
	Maximum clock frequency					155	MHz	[7, 8A, 8B]
	Minimum clock frequency				5		MHz	
	Clock high time			3.0			ns	
	Clock low time			3.0			ns	
	Conversion latency		See[7]			8	Clock cycles	[4, 5, 6]
t_{OD}	Output delay of CLK to DATA	Relative to falling edge of CLK		2.0			ns	
t_{SU}	Data output setup time	Relative to DRDY	See[8]	2.1	**1.22**		ns	
t_H	Data output hold time	Relative to DRDY	See[8]	2.1	**1.83**		ns	
t_{AD}	Aperture delay			0.5			ns	
t_{AJ}	Aperture jitter			0.08			ps rms	
	Power down recovery time	0.1 µF to GND on pins 43, 44; 10 µF and 0.1 µF between pins 43, 44; 0.1 µF and 10 µF to GND on pins 47, 48		3.0			ms	

(1) Pre and post irradiation limits are identical to those listed in the *Electrical Characteristics* tables. Radiation testing is performed per MIL-STD-883, Test Method 1019.

(2) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per Note 5. However, errors in the A/D conversion can occur if the input goes above 2.6 V or below GND as described in the *Recommended Operating Conditions* section.



(3) To ensure accuracy, it is required that $|V_A - V_D| \le 100$ mV and separate bypass capacitors are used at each power supply pin.

(4) With the test condition for V_{REF} = 1 V (2-V_{P-P} differential input), the 14-bit LSB is 122.1 µV.

(5) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

(6) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

(7) Specified by design.

(8) Specified by characterization.

6.9 Timing Diagram

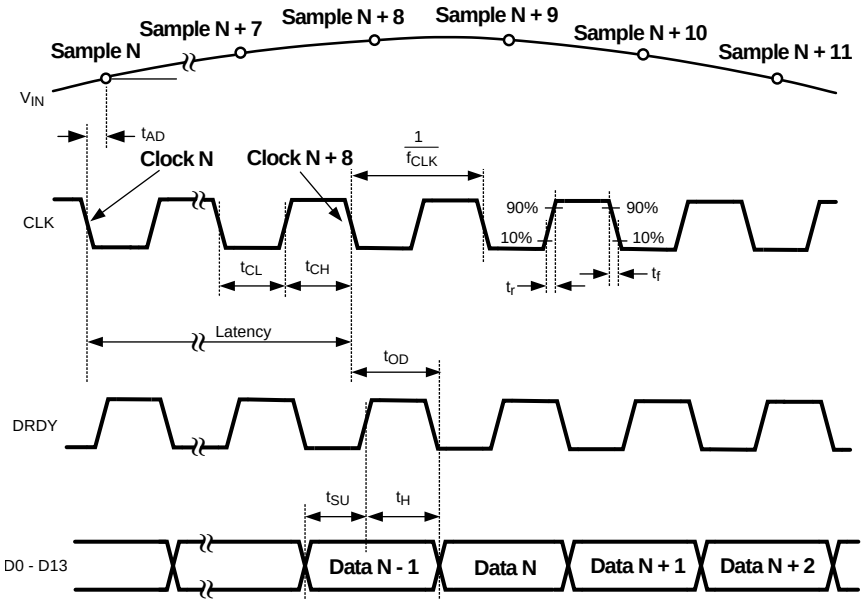


Figure 1. Output Timing

6.10 Transfer Characteristic

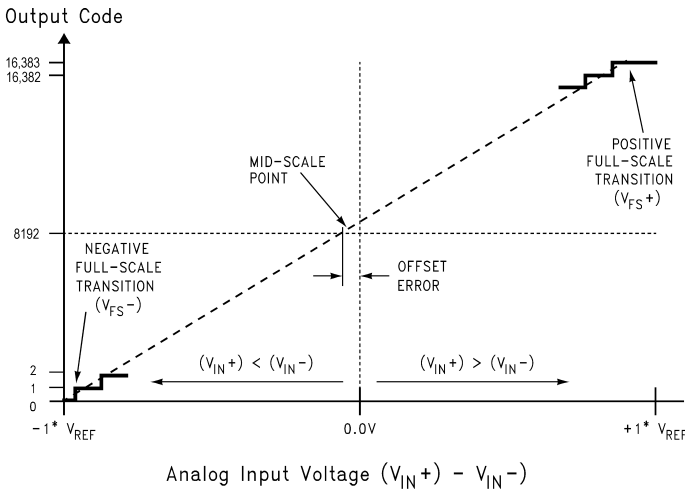


Figure 2. Transfer Characteristic

Transfer Characteristic (continued)

Table 1. Quality Conformance Inspection(1)

Subgroup	Description	Temp (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

(1) MIL-STD-883, Method 5005 - Group A

6.11 Typical Performance Characteristics, DNL, INL

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0 V, V_A = V_D = 3.3 V, V_{DR} = 1.8 V, Internal V_{REF} = 1 V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Differential Analog Input, Single-Ended Clock Mode, Offset Binary Format. Typical values are for TA = 25°C.(1)(2)(3)

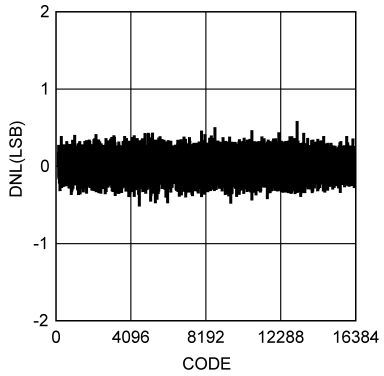


Figure 3. DNL

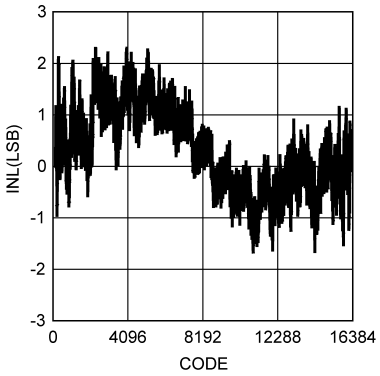
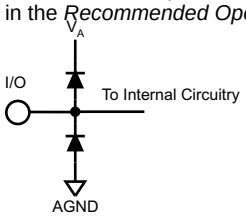


Figure 4. INL

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per Note 5. However, errors in the A/D conversion can occur if the input goes above 2.6 V or below GND as described in the *Recommended Operating Conditions* section.



(2) To ensure accuracy, it is required that $|V_A – V_D| \leq 100$ mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = 1 V (2-V_{P-P} differential input), the 14-bit LSB is 122.1 µV.

6.12 Typical Performance Characteristics, Dynamic Performance

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0 V, V_A = V_D = 3.3 V, V_{DR} = 1.8 V, Internal V_{REF} = 1 V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Differential Analog Input, Single-Ended Clock Mode, Offset Binary Format. Typical values are for TA = 25°C

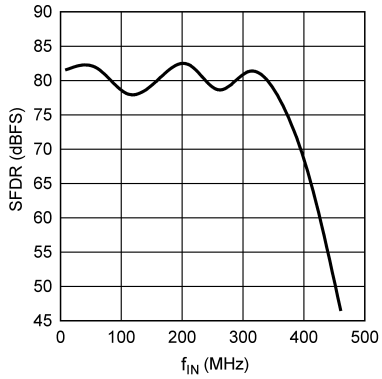


Figure 5. SFDR vs f_{IN}

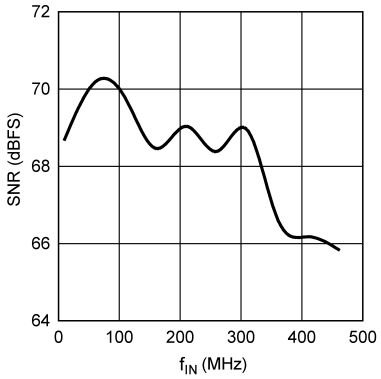


Figure 6. SNR vs f_{IN}

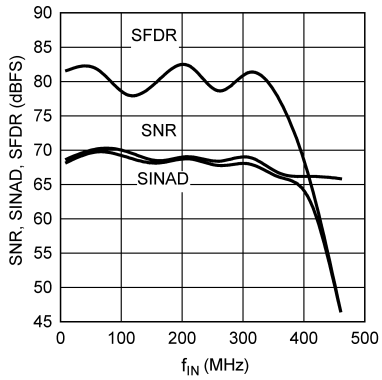


Figure 7. SNR, SINAD, SFDR vs f_{IN}

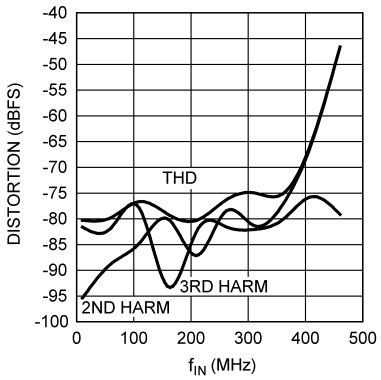


Figure 8. Distortion vs f_{IN}

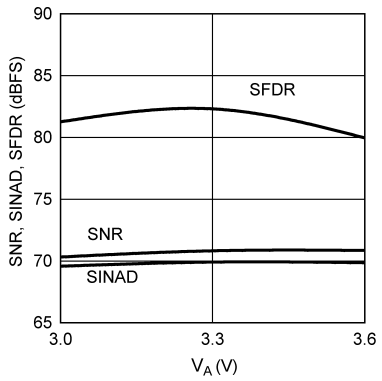


Figure 9. SNR, SINAD, SFDR vs V_A

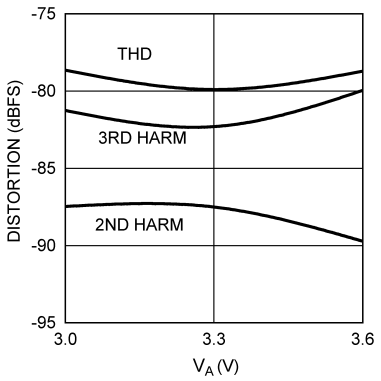


Figure 10. Distortion vs V_A

Typical Performance Characteristics, Dynamic Performance (continued)

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0 V, V_A = V_D = 3.3 V, V_{DR} = 1.8 V, Internal V_{REF} = 1 V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Differential Analog Input, Single-Ended Clock Mode, Offset Binary Format. Typical values are for TA = 25°C

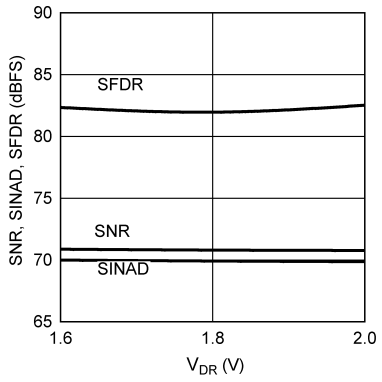


Figure 11. SNR, SINAD, SFDR vs V_{DR}

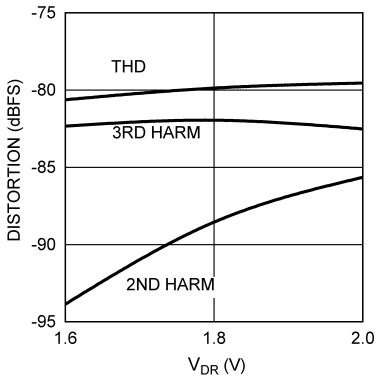


Figure 12. Distortion vs V_{DR}

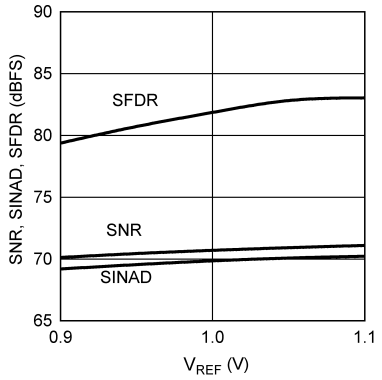


Figure 13. SNR, SINAD, SFDR vs V_{REF}

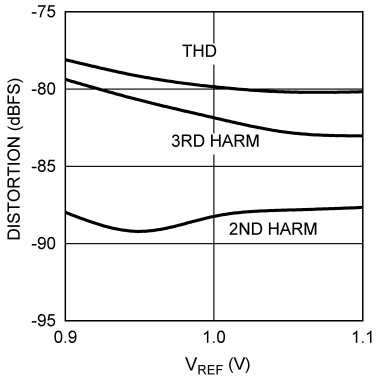


Figure 14. Distortion vs V_{REF}

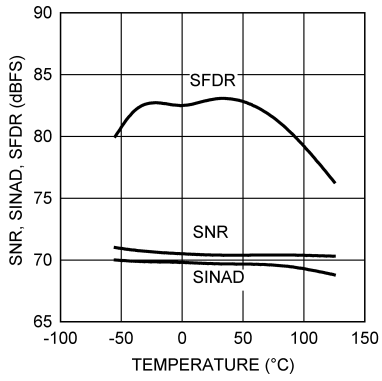


Figure 15. SNR, SINAD, SFDR vs Temperature

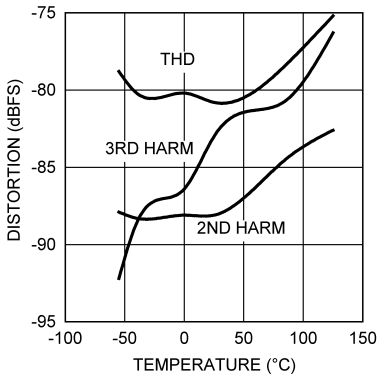


Figure 16. Distortion vs Temperature

Typical Performance Characteristics, Dynamic Performance (continued)

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0 V, V_A = V_D = 3.3 V, V_{DR} = 1.8 V, Internal V_{REF} = 1 V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Differential Analog Input, Single-Ended Clock Mode, Offset Binary Format. Typical values are for TA = 25°C

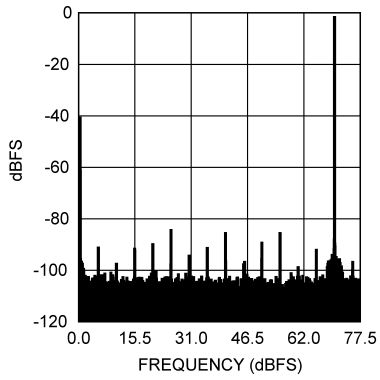


Figure 17. Spectral Response at 70-MHz Input

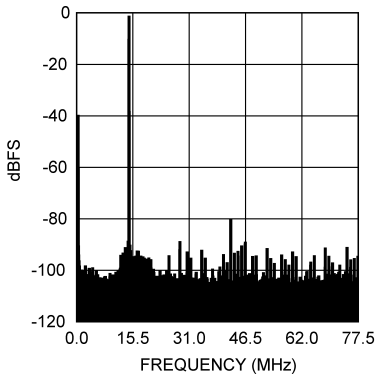


Figure 18. Spectral Response at 169-MHz Input

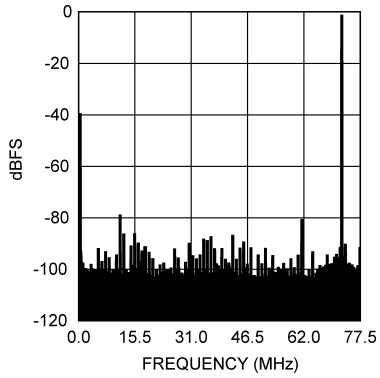


Figure 19. Spectral Response at 238-MHz Input

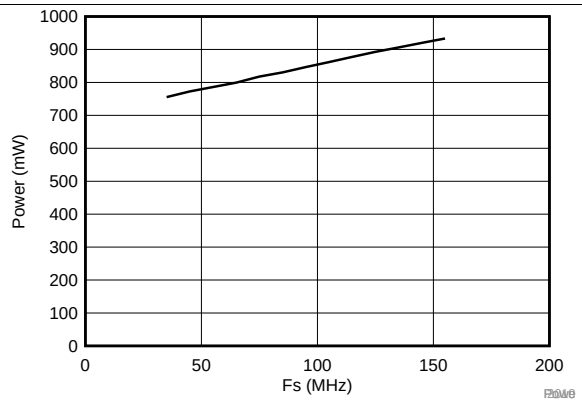


Figure 20. Power vs Sample Rate

7 Detailed Description

7.1 Overview

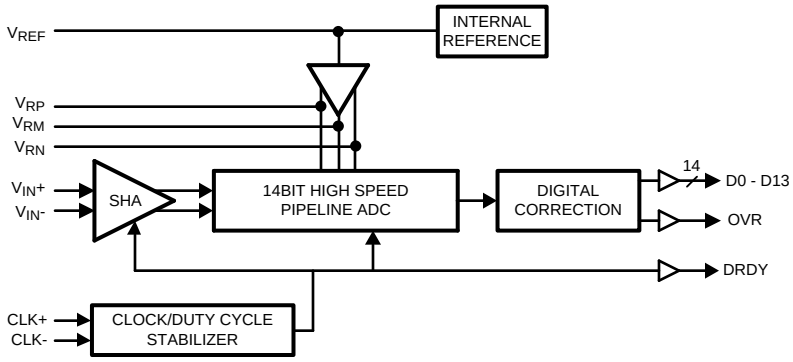
Operating on dual 3.3-V and 1.8-V supplies, the ADC14155 digitizes a differential analog input signal to 14 bits, using a differential pipelined architecture with error correction circuitry and an on-chip sample-and-hold circuit to ensure maximum performance.

The user has the choice of using an internal 1-V stable reference, or using an external reference. The ADC14155 will accept an external reference between 0.9 V and 1.1 V (1-V recommended) which is buffered on-chip to ease the task of driving that pin. The 1.8-V output driver supply reduces power consumption and decreases the noise at the output of the converter.

The quad state function pin CLK_SEL/DF (pin 8) allows the user to choose between using a single-ended or a differential clock input and between offset binary or 2's complement output data format. The digital outputs are CMOS compatible signals that are clocked by a synchronous data ready output signal (DRDY, pin 34) at the same rate as the clock input. For the ADC14155 the clock frequency can be between 5 MSPS and 155 MSPS with fully specified performance at 155 MSPS. The analog input is acquired at the falling edge of the clock and the digital data for a given sample is output on the falling edge of the DRDY signal and is delayed by the pipeline for 8 clock cycles. The data should be captured on the rising edge of the DRDY signal.

Power-down is selectable using the PD pin (pin 7). A logic high on the PD pin disables everything except the voltage reference circuitry and reduces the converter power consumption to 5 mW with no clock running. For normal operation, the PD pin should be connected to the analog ground (AGND). A duty cycle stabilizer maintains performance over a wide range of clock duty cycles.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs

7.3.1.1 Differential Analog Input Pins

The ADC14155QML-SP has one pair of analog signal input pins, V_{IN+} and $V_{IN–}$, which form a differential input pair. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN+}) – (V_{IN–}) \quad (1)$$

Figure 21 shows the expected input signal range. Note that the common mode input voltage, V_{CM}, should be 1.5 V. Using V_{RM} (pin 46 or 47) for V_{CM} will ensure the proper input common mode level for the analog input signal. The peaks of the individual input signals should each never exceed 2.6 V. Each analog input pin of the differential pair should have a peak-to-peak voltage equal to the reference voltage, V_{REF}, be 180° out of phase with each other and be centered around V_{CM}.The peak-to-peak voltage swing at each analog input pin should not exceed the value of the reference voltage or the output data will be clipped.

Feature Description (continued)

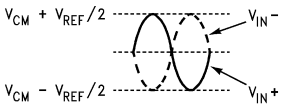


Figure 21. Expected Input Signal Range

For single frequency sine waves the full scale error, E_{FS}, in LSB can be described as approximately

$$E_{FS} = 16384 (1 – \sin (90° + dev)) \quad (2)$$

Where dev is the angular difference in degrees between the two signals having a 180° relative phase relationship to each other (see Figure 22). For single frequency inputs, angular errors result in a reduction of the effective full scale input. For complex waveforms, however, angular errors will result in distortion.

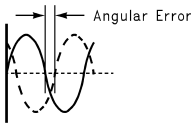


Figure 22. Angular Errors Between The Two Input Signals Will Reduce The Output Level Or Cause Distortion

It is recommended to drive the analog inputs with a source impedance less than 100 Ω. Matching the source impedance for the differential inputs will improve even ordered harmonic performance (particularly second harmonic).

Table 2 indicates the input to output relationship of the ADC14155.

Table 2. Input To Output Relationship

V_{IN+}	$V_{IN–}$	Binary Output	2's Complement Output	
$V_{CM} – V_{REF} / 2$	$V_{CM} + V_{REF} / 2$	00 0000 0000 0000	10 0000 0000 0000	Negative Full-Scale
$V_{CM} – V_{REF} / 4$	$V_{CM} + V_{REF} / 4$	01 0000 0000 0000	11 0000 0000 0000	
V_{CM}	V_{CM}	10 0000 0000 0000	00 0000 0000 0000	Mid-Scale
$V_{CM} + V_{REF} / 4$	$V_{CM} – V_{REF} / 4$	11 0000 0000 0000	01 0000 0000 0000	
$V_{CM} + V_{REF} / 2$	$V_{CM} – V_{REF} / 2$	11 1111 1111 1111	01 1111 1111 1111	Positive Full-Scale

7.3.1.2 Driving The Analog Inputs

The V_{IN+} and the $V_{IN–}$ inputs of the ADC14155QML-SP have an internal sample-and-hold circuit which consists of an analog switch followed by a switched-capacitor amplifier. The analog inputs are connected to the sampling capacitors through NMOS switches, and each analog input has parasitic capacitances associated with it.

When the clock is high, the converter is in the sample phase. The analog inputs are connected to the sampling capacitor through the NMOS switches, which causes the capacitance at the analog input pins to appear as the pin capacitance plus the internal sample and hold circuit capacitance (approximately 9 pF). While the clock level remains high, the sampling capacitor will track the changing analog input voltage. When the clock transitions from high to low, the converter enters the hold phase, during which the analog inputs are disconnected from the sampling capacitor. The last voltage that appeared at the analog input before the clock transition will be held on the sampling capacitor and will be sent to the ADC core. The capacitance seen at the analog input during the hold phase appears as the sum of the pin capacitance and the parasitic capacitances associated with the sample and hold circuit of each analog input (approximately 6 pF). Once the clock signal transitions from low to high, the analog inputs will be reconnected to the sampling capacitor to capture the next sample. Usually, there will be a difference between the held voltage on the sampling capacitor and the new voltage at the analog input. This will cause a charging glitch that is proportional to the voltage difference between the two samples to appear at the analog input pin. The input circuitry must be fast enough to allow the sampling capacitor to fully charge before the clock signal goes high again, as incomplete settling can degrade the SFDR performance.

A single-ended to differential conversion circuit is shown in Figure 24. A transformer is preferred for high frequency input signals. Terminating the transformer on the secondary side provides two advantages. First, it presents a real broadband impedance to the ADC inputs and second, it provides a common path for the charging glitches from each side of the differential sample-and-hold circuit.

One short-coming of using a transformer to achieve the single-ended to differential conversion is that most RF transformers have poor low frequency performance. A differential amplifier can be used to drive the analog inputs for low frequency applications. The amplifier must be fast enough to settle from the charging glitches on the analog input resulting from the sample-and-hold operation before the clock goes high and the sample is passed to the ADC core.

The SFDR performance of the converter depends on the external signal conditioning circuity used, as this affects how quickly the sample-and-hold charging glitch will settle. An external resistor and capacitor network as shown in Figure 24 should be used to isolate the charging glitches at the ADC input from the external driving circuit and to filter the wideband noise at the converter input. These filtering components should be placed close to the ADC inputs in order to absorb the sampling glitches as close to the source of the glitches as possible. For Nyquist applications the RC pole should be at the ADC sample rate. The ADC input capacitance in the sample mode should be considered when setting the RC pole. For wideband undersampling applications, the RC pole should be set at about 1.5 to 2 times the maximum input frequency to maintain a linear delay response.

7.3.1.3 Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be in the range of 1.4 V to 1.6 V and be a value such that the peak excursions of the analog signal do not go more negative than ground or more positive than 2.6 V. It is recommended to use V_{RM} (pin 46 or 47) as the input common mode voltage.

7.3.2 Reference Pins

The ADC14155QML-SP is designed to operate with an internal 1-V reference, or an external 1-V reference, but performs well with external reference voltages in the range of 0.9 V to 1.1 V. The internal 1-V reference is the default condition when no external reference input is applied to the V_{REF} pin. If a voltage in the range of 0.9 V to 1.1 V is applied to the V_{REF} pin, then that voltage is used for the reference. The V_{REF} pin should always be bypassed to ground with a 0.1-µF capacitor close to the reference input pin. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC14155. Increasing the reference voltage (and the input signal swing) beyond 1.1-V may degrade THD for a full-scale input, especially at higher input frequencies.

It is important that all grounds associated with the reference voltage and the analog input signal make connection to the ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

The Reference Bypass Pins (V_{RP}, V_{RM}, and V_{RN}) are made available for bypass purposes. Each of these pins should be bypassed to ground with a 0.1-µF capacitor. A 0.1-µF and a 10-µF capacitor should be placed between the V_{RP} and V_{RN} pins, as shown in Figure 24. This configuration is necessary to avoid reference oscillation, which could result in reduced SFDR and/or SNR. V_{RM} may be loaded to 1 mA for use as a temperature stable 1.5-V reference. The V_{RP} and V_{RN} pins should not be loaded.

Smaller capacitor values than those specified will allow faster recovery from the power down mode, but may result in degraded noise performance. Loading any of these pins, other than V_{RM}, may result in performance degradation.

The nominal voltages for the reference bypass pins are as follows:

$V_{RM} = 1.5$ V

$V_{RP} = V_{RM} + V_{REF} / 2$

$V_{RN} = V_{RM} – V_{REF} / 2$

7.3.3 Digital Inputs

Digital CMOS compatible inputs consist of CLK+, CLK–, PD and CLK_SEL/DF.

7.3.3.1 Clock Inputs

The CLK+ and CLK– signals control the timing of the sampling process. The CLK_SEL/DF pin (pin 8) allows the user to configure the ADC for either differential or single-ended clock mode (see Clock Mode Select/Data Format (CLK_SEL/DF)). In differential clock mode, the two clock signals should be exactly 180° out of phase from each other and of the same amplitude. In the single-ended clock mode, the clock signal should be routed to the CLK+ input and the CLK– input should be tied to AGND in combination with the correct setting from Table 4.

To achieve the optimum noise performance, the clock inputs should be driven with a stable, low jitter clock signal. The clock input signal should also have a short transition region. This can be achieved by passing a low-jitter sinusoidal clock source through a high speed buffer gate. This configuration is shown in Figure 24. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°. Figure 24 shows the recommended clock input circuit.

The clock signal also drives an internal state machine. If the clock is interrupted, or its frequency is too low, the charge on the internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This will limit the minimum sample rate.

The clock line should be terminated at its source in the characteristic impedance of that line. Care should be taken to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 (SNLA035) for information on setting characteristic impedance.

It is highly desirable that the source driving the ADC clock pins only drive that pin. However, if that source is used to drive other devices, then each driven pin should be AC terminated with a series RC to ground, such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PD} \times L}{Z_o} \tag{3}$$

where t_{PD} is the signal propagation rate down the clock line, "L" is the line length and Z_O is the characteristic impedance of the clock line. This termination should be as close as possible to the ADC clock pin but beyond it as seen from the clock source. Typical t_{PD} is about 150 ps/in (60 ps/cm) on FR-4 board material. The units of "L" and t_{PD} should be the same (inches or centimeters).

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC14155 has a Duty Cycle Stabilizer. It is designed to maintain performance over a clock duty cycle range of 30% to 70%.

7.3.3.2 Power-Down (PD)

Power-down can be enabled through this two-state input pin. Table 3 shows how to power-down the ADC14155.

Table 3. Power Down Selection Table

PD Input Voltage	Power State
V_A	Power-down
AGND	On

The power-down mode allows the user to conserve power when the converter is not being used. In the power-down state all bias currents of the analog circuitry, excluding the reference are shut down which reduces the power consumption to 5 mW with no clock running. The output data pins are undefined and the data in the pipeline is corrupted while in the power-down mode.

The Power-down Mode Exit Cycle time is determined by the value of the capacitors on the V_{RP} (pin 42, 43), V_{RM} (pin 46, 47) and V_{RN} (pin 44, 45) reference bypass pins (pins 43, 44 and 45) and is approximately 3 ms with the recommended component values. These capacitors lose their charge in the power-down mode and must be recharged by on-chip circuitry before conversions can be accurate. Smaller capacitor values allow slightly faster recovery from the power down mode, but can result in a reduction in SNR, SINAD and ENOB performance.

7.3.3.3 Clock Mode Select/Data Format (CLK_SEL/DF)

Single-ended versus differential clock mode and output data format are selectable using this quad-state function pin. Table 4 shows how to select between the clock modes and the output data formats.

Table 4. Clock Mode And Data Format Selection Table

CLK_SEL/DF Input Voltage	Clock Mode	Output Data Format
V_A	Differential	2's Complement
(2 / 3) * V_A	Differential	Offset Binary
(1 / 3) * V_A	Single-Ended	2's Complement
AGND	Single-Ended	Offset Binary

7.4 Device Functional Modes

This devices has no specific functional modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To achieve the best dynamic performance, the clock source driving the CLK input must have a sharp transition region and be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in Figure 23. The gates used in the clock tree must be capable of operating at frequencies much higher than those used if added jitter is to be prevented. Best performance will be obtained with a differential clock input drive, compared with a single-ended drive.

As mentioned in Power Supply Recommendations, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

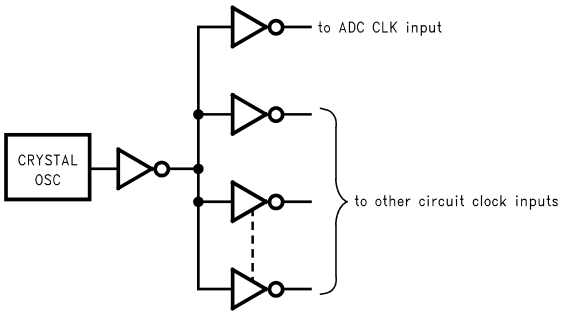


Figure 23. Isolating the ADC Clock From Other Circuitry With a Clock Tree

8.2 Typical Application

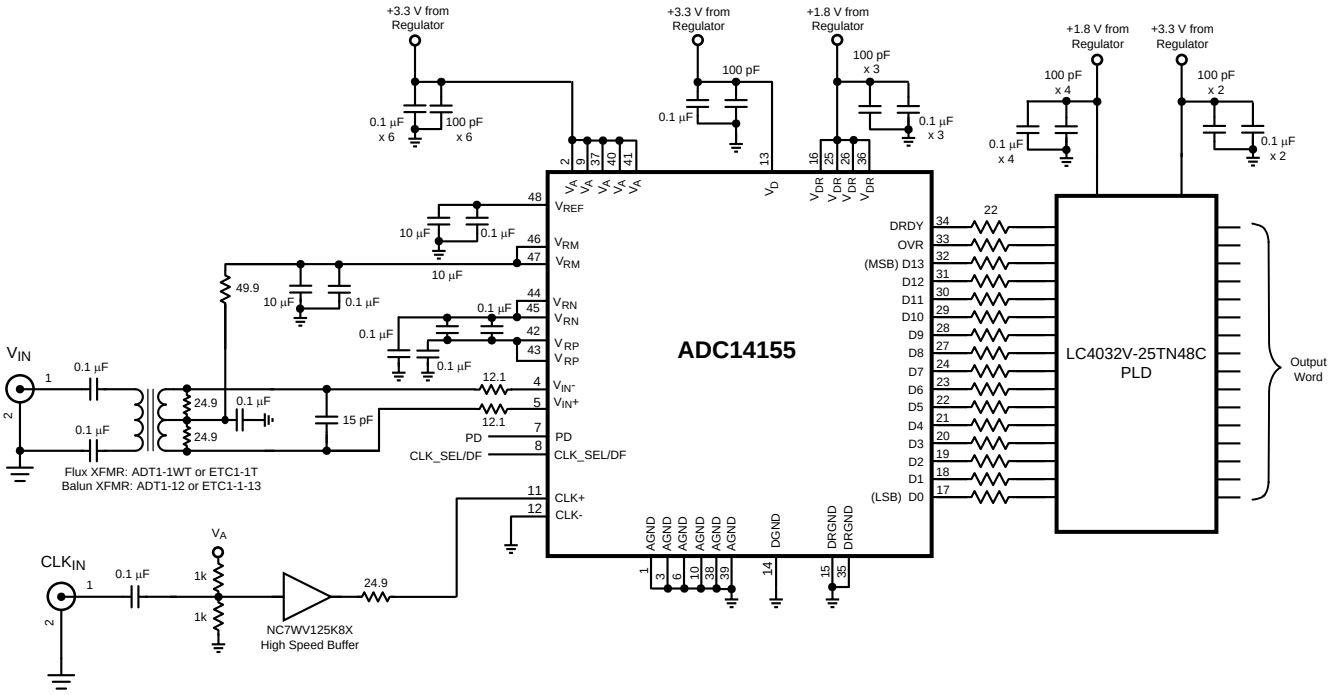


Figure 24. Application Circuit Using Transformer Drive Circuit

8.2.1 Design Requirements

We recommend that the following conditions be observed for operation of the ADC14155:

$3\ V \le V_A \le 3.6\ V$

$V_D = V_A$

$V_{DR} = 1.8\ V$

$5\ MHz \le f_{CLK} \le 155\ MHz$

1-V internal reference

$0.9\ V \le V_{REF} \le 1.1\ V$ (for an external reference)

$V_{CM} = 1.5\ V$ (from V_{RM})

8.2.2 Detailed Design Procedure

Digital outputs consist of the 1.8 V CMOS signals D0-D13, DRDY and OVR.

The ADC14155 has 16 CMOS compatible data output pins: 14 data output bits corresponding to the converted input value, a data ready (DRDY) signal that should be used to capture the output data and an over-range indicator (OVR) which is set high when the sample amplitude exceeds the 14-bit conversion range. Valid data is present at these outputs while the PD pin is low.

Data should be captured and latched with the rising edge of the DRDY signal. Depending on the setup and hold time requirements of the receiving circuit (ASIC), either the rising edge or the falling edge of the DRDY signal can be used to latch the data. Generally, rising-edge capture would maximize setup time with minimal hold time; while falling-edge-capture would maximize hold time with minimal setup time. However, actual timing for the falling-edge case depends greatly on the CLK frequency and both cases also depend on the delays inside the ASIC. Refer to the *ADC14155 Converter Electrical Characteristics (Continued) Timing and AC Characteristics*(1) table.

(1) Pre and post irradiation limits are identical to those listed in the *Electrical Characteristics* tables. Radiation testing is performed per MIL-STD-883, Test Method 1019.

Typical Application (continued)

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DRGND. These large charging current spikes can cause on-chip ground noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 5 pF/pin will cause t_{OD} to increase, reducing the setup and hold time of the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, the load currents at the digital outputs should be minimized. This can be done by using a programmable logic device (PLD) such as the LC4032V-25TN48C to level translate the ADC output data from 1.8 V to 3.3 V for use by any other circuitry. Only one load should be connected to each output pin. Additionally, inserting series resistors of about 22 Ω at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. See Figure 24.

8.2.3 Application Curve

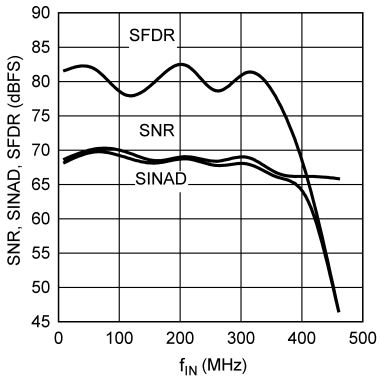


Figure 25. SNR, SINAD, SFDR vs f_{IN}

8.3 Radiation Environments

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

8.3.1 Total Ionizing Dose (TID)

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the table on the front page. Testing and qualification of these products is done according to MIL-STD-883, Test Method 1019. Additional information on how to download lot-specific TID data can be found in SBOA140 "QML Class V/Q and Enhanced Products Lot Documents".

8.3.2 Single Event Effects

One time single event latch-up testing (SEL) was preformed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LET_{th}) shown in the Key Specifications table on the front page is the maximum LET tested. Test reports are available on the TI estore at SNAA153 and SNAA183.

9 Power Supply Recommendations

The power supply pins should be bypassed with a 0.1-µF capacitor and with a 100-pF ceramic chip capacitor close to each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC14155 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

The V_{DR} pin provides power for the output drivers and may be operated from a supply in the range of 1.6 V to 2 V. This enables lower power operation, reduces the noise coupling effects from the digital outputs to the analog circuitry and simplifies interfacing to lower voltage devices and systems. Note, however, that t_{OD} increases with reduced V_{DR}. A level translator may be required to interface the digital output signals of the ADC14155 to non-1.8-V CMOS devices.

Care should be taken to avoid extremely rapid power supply ramp up rate. Excessive power supply ramp up rate may damage the device.

10 Layout

10.1 Layout Guidelines

For best dynamic performance, the center die attach pad of the device should be connected to ground with low inductive path.

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC14155 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DRGND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, it is recommended to use a single common ground plane with managed return current paths instead of a split ground plane. The key is to make sure that the supply current in the ground plane does not return under a sensitive node (e.g., caps to ground in the analog input network). This is done by routing a trace from the ADC to the regulator / bulk capacitor for the supply so that it does not run under a critical node.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

The effects of the noise generated from the ADC output switching can be minimized through the use of 22-Ω resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane area.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors and transformers. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors and transformers should *not* be placed side by side, even with just a small part of their bodies beside each other. For instance, place transformers for the analog input and the clock input at 90° to one another to avoid magnetic coupling.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and dynamic I/O lines should be placed in the digital area of the board. The ADC14155 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

10.2 Layout Example

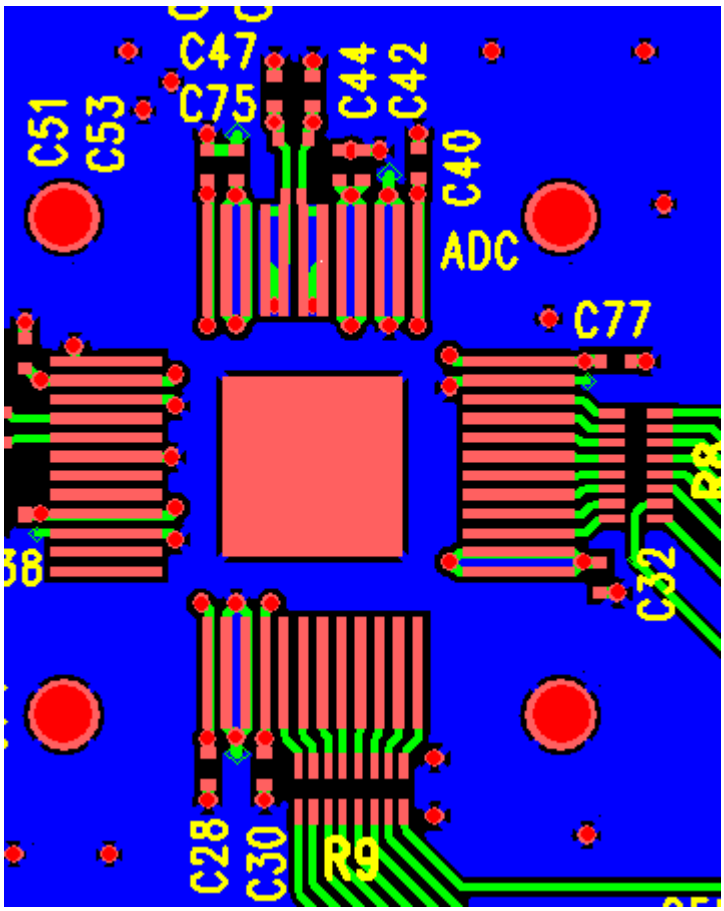


Figure 26. ADC14155QML Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

APERTURE DELAY is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Negative Full Scale Error (4)

It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

PGE = Positive Full Scale Error – Offset Error NGE = Offset Error – Negative Full Scale Error (5)

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS} / 2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC14155QML is ensured not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages [(V_{IN}+) – (V_{IN}–)] required to cause a transition from code 8191 to 8192.

OUTPUT DELAY is the time delay after the falling edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

Device Support (continued)

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. PSRR is the ratio of the Full-Scale output of the ADC with the supply at the minimum DC supply limit to the Full-Scale output of the ADC with the supply at the maximum DC supply limit, expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}} \tag{6}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R0626201VXC	Active	Production	CFP (NBA) | 48	14 | TUBE	-	Call TI	Level-1-NA-UNLIM	-55 to 125	5962 R0626201VXC ADC14155-RHA
5962R0626201VXC.A	Active	Production	CFP (NBA) | 48	14 | TUBE	-	Call TI	Level-1-NA-UNLIM	-55 to 125	5962 R0626201VXC ADC14155-RHA
ADC14155W-MLS	Active	Production	CFP (NBA) | 48	14 | TUBE	-	Call TI	Level-1-NA-UNLIM	-55 to 125	ADC14155W -MLS
ADC14155W-MLS.A	Active	Production	CFP (NBA) | 48	14 | TUBE	-	Call TI	Level-1-NA-UNLIM	-55 to 125	ADC14155W -MLS
ADC14155W-MPR	Active	Production	CFP (NBA) | 48	14 | TUBE	-	Call TI	Level-1-NA-UNLIM	25 to 25	ADC14155W -MPR ES
ADC14155W-MPR.A	Active	Production	CFP (NBA) | 48	14 | TUBE	-	Call TI	Level-1-NA-UNLIM	25 to 25	ADC14155W -MPR ES

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

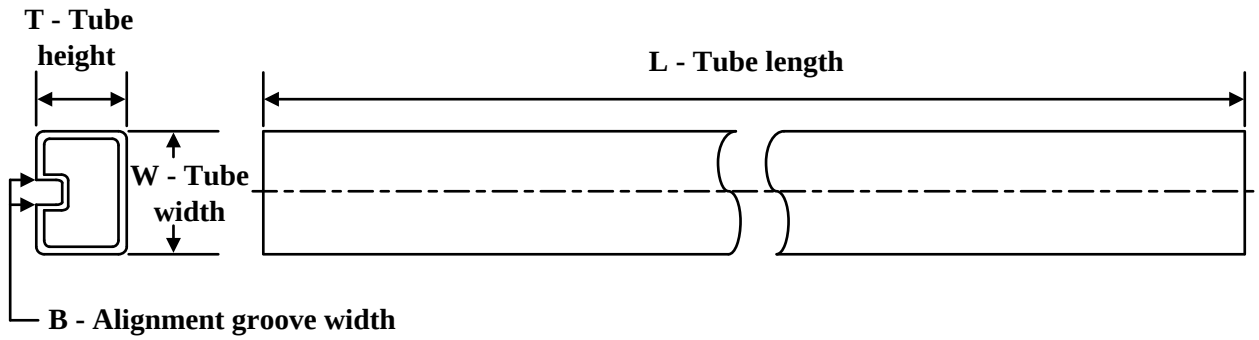
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

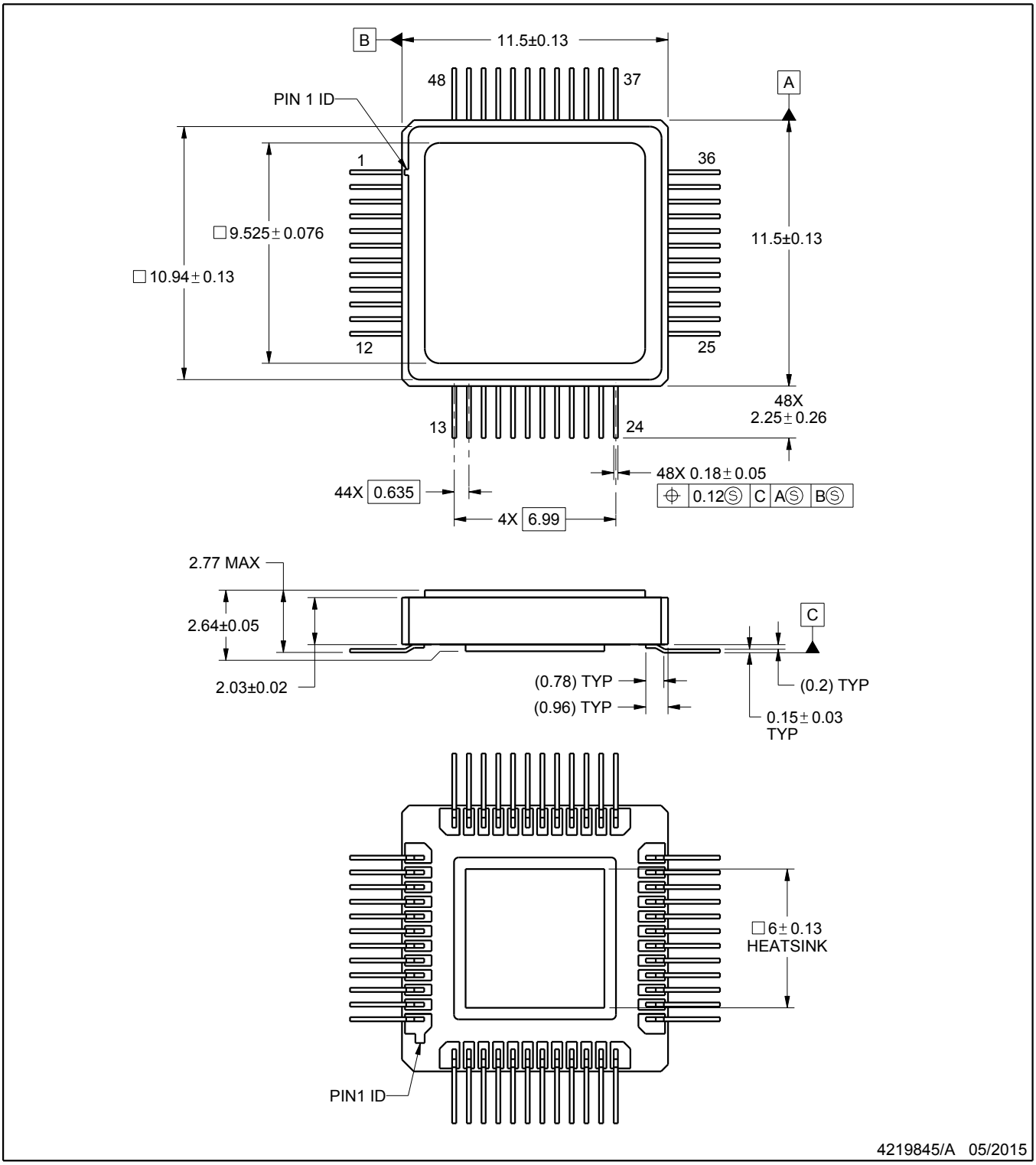
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R0626201VXC	NBA	CFP	48	14	495	33	11176	16.51
5962R0626201VXC.A	NBA	CFP	48	14	495	33	11176	16.51
ADC14155W-MLS	NBA	CFP	48	14	495	33	11176	16.51
ADC14155W-MLS.A	NBA	CFP	48	14	495	33	11176	16.51
ADC14155W-MPR	NBA	CFP	48	14	495	33	11176	16.51
ADC14155W-MPR.A	NBA	CFP	48	14	495	33	11176	16.51

PACKAGE OUTLINE

NBA0048A

CFP - 2.77 mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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