ADC12130/ADC12132/ADC12138 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converters with MUX and Sample/Hold

Check for Samples: ADC12130, ADC12132, ADC12138

FEATURES

- **Serial I/O (MICROWIRE, SPI and QSPI Compatible)**
- **Power Down Mode**
- **Programmable Acquisition Time**
- **Variable Digital Output Word Length and Format**
- **No Zero or Full Scale Adjustment Required**
- **0V to 5V Analog Input Range with Single 5V Power Supply**

APPLICATIONS

- **Pen-Based Computers**
- **Digitizers**
- **Global Positioning Systems**

KEY SPECIFICATIONS

- **Resolution 12-bit plus sign**
- **12-Bit plus sign conversion time 8.8 µs (max)**
- **12-Bit plus sign throughput time 14 µs (max)**
- **Integral Linearity Error ±2 LSB (max)**
- **Single Supply 3.3V or 5V ±10%**
- **Power Consumption**
  - **+3.3V 15 mW (max)**
  - **+3.3V power down 40 µW (typ)**
  - **+5V 33 mW (max)**
  - **+5V power down 100 µW (typ)**

DESCRIPTION

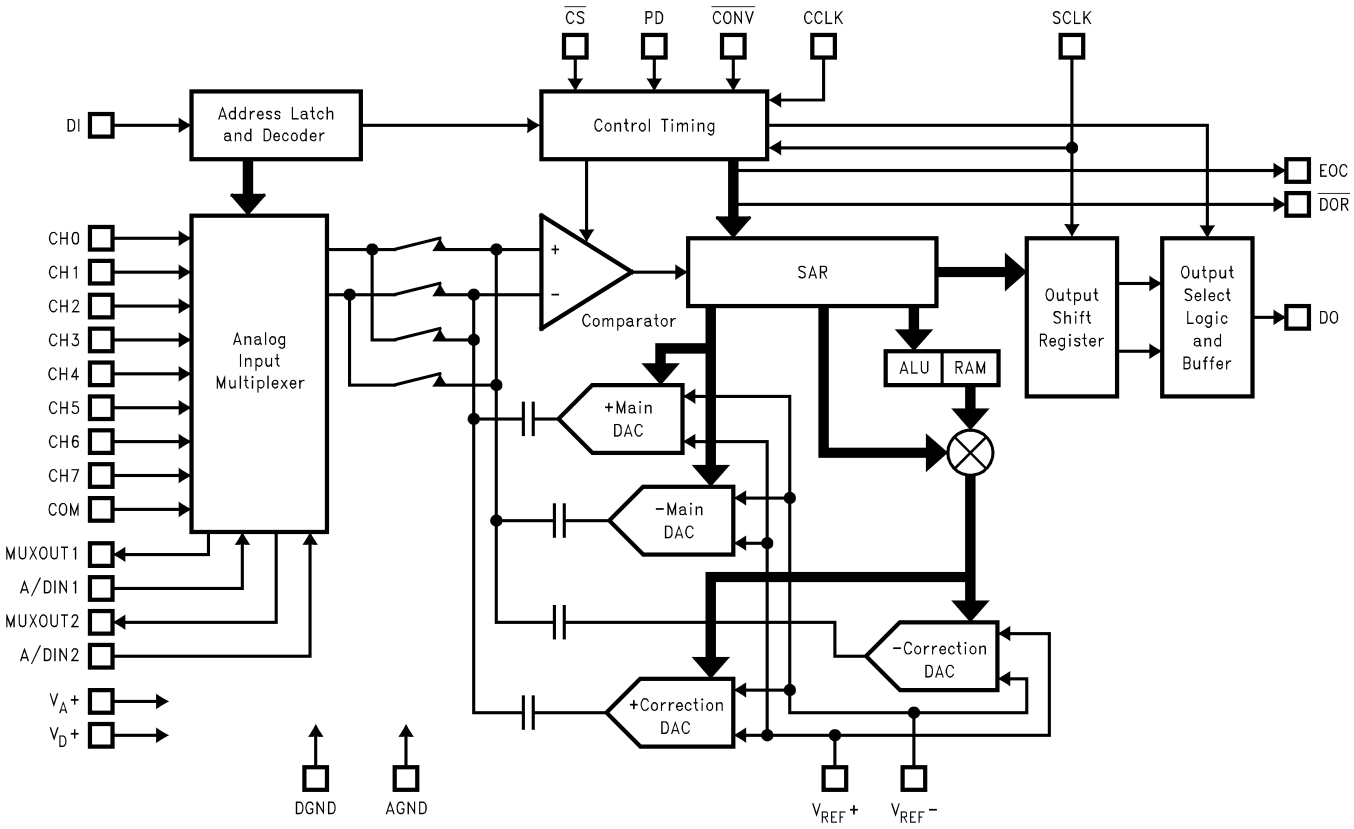
NOTE: Some device/package combinations are obsolete and are described and shown here for reference only. See our web site for product availability.

The ADC12130, ADC12132 and ADC12138 are 12-bit plus sign successive approximation Analog-to-Digital converters with serial I/O and configurable input multiplexer. The ADC12132 and ADC12138 have a 2 and an 8 channel multiplexer, respectively. The differential multiplexer outputs and ADC inputs are available on the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 pins. The ADC12130 has a two channel multiplexer with the multiplexer outputs and ADC inputs internally connected. The ADC12130 family is tested and specified with a 5 MHz clock. On request, these ADCs go through a self calibration process that adjusts linearity, zero and full-scale errors to typically less than ±1 LSB each.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. A fully differential unipolar analog input range (0V to +5V) can be accommodated with a single +5V supply. In the differential modes, valid outputs are obtained even when the negative inputs are greater than the positive because of the 12-bit plus sign output data format.

The serial I/O is configured to comply with NSC MICROWIRE. For voltage references, see the LM4040, LM4050 or LM4041.

ADC12138 Simplified Block Diagram



Connection Diagrams

Top View

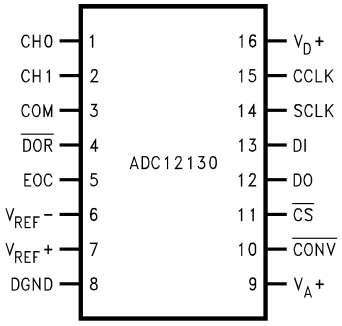


Figure 1. 16-Pin MDIP and Wide Body SOIC Packages See Package Number NFG0016E and DW0016B

Top View

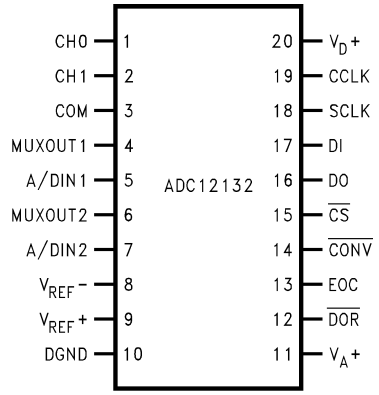


Figure 2. 20-Pin SSOP Package See Package Number DB0020A

Top View

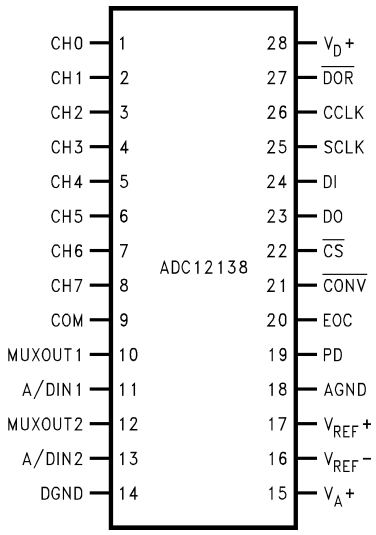


Figure 3. 28-Pin MDIP, SSOP and Wide Body SOIC Packages
See Package Numbers N28B, DB0028A, and DW0028B

Some of these product/package combinations are obsolete and are shown here for reference only. Check the TI web site for availability.

PIN DESCRIPTIONS

Pin Name	Pin Description
CH0 thru CH7	Analog Inputs to the MUX (multiplexer). A channel input is selected by the address information at the DI pin, which is loaded at the rising edge of SCLK into the address register (see Table 2 and Table 3). The voltage applied to these inputs should not exceed V_A+ or go below V_A- or below GND. Exceeding this range on an unselected channel may corrupt the reading of a selected channel.
COM	Analog input pin that is used as a pseudo ground when the analog multiplexer is single-ended.
MUXOUT1 MUXOUT2	Multiplexer Output pins. If the multiplexer is used, these pins should be connected to the A/DIN pins, directly or through an amplifier and/of filter.
A/DIN1 A/DIN2	Converter Input pins. MUXOUT1 is usually tied to A/DIN1. MUXOUT2 is usually tied to A/DIN2. If external circuitry is placed between MUXOUT1 and A/DIN1, or MUXOUT2 and A/DIN2, it may be necessary to protect these pins against voltage overload. The voltage at these pins should not exceed V_A^+ or go below AGND (see Figure 64).
DO	Data Output pin. This pin is an active push/pull output when $\overline{CS}$ is low. When $\overline{CS}$ is high, this output is TRI-STATE. The conversion result (DB0–DB12) and converter status data are clocked out at the falling edge of SCLK on this pin. The word length and format of this result can vary (see Table 1). The word length and format are controlled by the data shifted into the multiplexer address and mode select register (see Table 4).
DI	Serial Data Input pin. The data applied to this pin is shifted at the rising edge of SCLK into the multiplexer address and mode select register. Table 2 through Table 4 show the assignment of the multiplexer address and the mode select data.
EOC	This pin is an active push/pull output which indicates the status of the ADC12130/2/8.A logic low on this pin indicates that the ADC is busy with a conversion, Auto Calibration, Auto Zero or power down cycle. The rising edge of EOC signals the end of one of these cycles
$\overline{CONV}$	A logic low is required at this pin to program any mode or to change the ADC's configuration as listed in Mode Programming (Table 4). When this pin is high, the ADC is placed in the read data only mode. While in the read data only mode, bringing $\overline{CS}$ low and pulsing SCLK will only clock out the data stored in the ADCs output shift register. The data at DI will be ignored. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto Cal or Auto Zero are in progress.

PIN DESCRIPTIONS (continued)

Pin Name	Pin Description
$\overline{CS}$	Chip Select input pin. When a logic low is applied to this pin, the rising edge of SCLK shifts the data at the DI input into the address register and brings DO out of TRI-STATE. With $\overline{CS}$ low, the falling edge of SCLK shifts the data resulting from the previous ADC conversion out at the DO output, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled, the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low while SCLK is low. The falling edge of $\overline{CS}$ interrupts a conversion in progress and starts the sequence for a new conversion. When $\overline{CS}$ is brought low during a conversion, that conversion is prematurely terminated and the data in the output latches may be corrupted. Therefore, when $\overline{CS}$ is brought low during a conversion in progress, the data output at that time should be ignored. $\overline{CS}$ may also be left continuously low. In this case, it is imperative that the correct number of SCLK pulses be applied to the ADC in order to remain synchronous. After the ADC supply power is applied, the device expects to see 13 clock pulses for each I/O sequence. The number of clock pulses the ADC expects is the same as the digital output word length. This word length can be modified by the data shifted in at the DO pin. Table 4 details the data required.
DOR	Data Output Ready pin. This pin is an active push/pull output which is low when the conversion result is being shifted out and goes high to signal that all the data has been shifted out.
SCLK	Serial Data Clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. The rising edge loads the information at the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the ADC. With $\overline{CS}$ low, the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled, the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The rise and fall times of the clock edges should not exceed 1 µs.
CCLK	Conversion Clock input. The clock applied to this input controls the successive approximation conversion time interval and the acquisition time. The rise and fall times of the clock edges should not exceed 1 µs.
$V_{REF}+$	Positive analog voltage reference input. In order to maintain accuracy, the voltage range of V_{REF} ($V_{REF} = V_{REF}+ - V_{REF}-$) is 1.0 V_{DC} to 5.0 V_{DC} and the voltage at $V_{REF}+$ cannot exceed V_A+. See Figure 63 for recommended bypassing.
$V_{REF}-$	The negative analog voltage reference input. In order to maintain accuracy, the voltage at this pin must not go below GND or exceed $V_{REF}+$. (See Figure 63).
PD	Power Down pin. When PD is high the ADC is powered down; when PD is low the ADC is powered up, or active. The ADC takes a maximum of 700 µs to power up after the command is given.
V_A^+ V_D^+	These are the analog and digital power supply pins. V_A^+ and V_D^+ are not connected together on the chip. These pins should be tied to the same supply voltage and bypassed separately (see Figure 63). The operating voltage range of V_A+ and V_D+ is 3.0 V_{DC} to 5.5 V_{DC}.
DGND	The digital ground pin (see Figure 63).
AGND	The analog ground pin (see Figure 63).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Positive Supply Voltage ($V^+ = V_A+ = V_D+$)		6.5V
Voltage at Inputs and Outputs except CH0–CH7 and COM		−0.3V to V^+ +0.3V
Voltage at Analog Inputs CH0–CH7 and COM		GND −5V to V^+ +5V
$\lvert V_A+ - V_D+\rvert$		300 mV
Input Current at Any Pin (3)		±30 mA
Package Input Current (3)		±120 mA
Package Dissipation at T_A = 25°C (4)		500 mW
ESD Susceptibility (5)		
Human Body Model		1500V
Soldering Information		
PDIP Packages (10 seconds)		260°C
SOIC Package (6)		
Vapor Phase (60 seconds)		215°C
Infrared (15 seconds)		220°C
Storage Temperature		−65°C to +150°C

(1) All voltages are measured with respect to GND, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A+ or V_D+), the current at that pin should be limited to 30 mA. The 120 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 30 mA to four.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J\text{max} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_J$max = 150°C.
(5) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
(6) See AN450 “Surface Mounting Methods and Their Effect on Product Reliability” or the section titled “Surface Mount” found in any post 1986 Texas Instruments Linear Data Book for other methods of soldering surface mount devices.

Operating Ratings (1)(2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$ −40°C ≤ T_A ≤ +85°C
Supply Voltage ($V^+ = V_A+ = V_D+$)	+3.0V to +5.5V
$\lvert V_A+ - V_D+\rvert$	≤ 100 mV
$V_{REF}+$	0V to V_A+
$V_{REF}-$	0V to ($V_{REF}+$ −1V)
V_{REF} ($V_{REF}+ - V_{REF}-$)	1V to V_A+
V_{REF} Common Mode Voltage Range [($V_{REF}+$) − ($V_{REF}-$)] / 2	0.1 V_A+ to 0.6 V_A+
A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 Voltage Range	0V to V_A+
ADC IN Common Mode Voltage Range [($V_{IN}+$) − ($V_{IN}-$)] / 2	0V to V_A+

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND, unless otherwise specified.

Package Thermal Resistance

Part Number	Thermal Resistance (θ_{JA})
ADC12130CIN	53°C/W
ADC12130CIWM	70°C/W
ADC12132CIMSA	134°C/W
ADC12132CIWM	64°C/W
ADC121038CIN	40°C/W
ADC121038CIMSA	97°C/W
ADC12138CIWM	50°C/W

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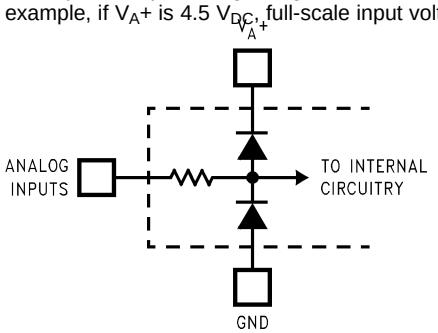
Converter Electrical Characteristics

The following specifications apply for ($V^+ = V_A+ = V_D+ = +5V$, $V_{REF}+ = +4.096V$, and fully differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A+ = V_D+ = 3.3V$, $V_{REF}+ = 2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}- = 0V$, 12-bit + sign conversion mode(1), source impedance for analog inputs, V_{REF}^- and $V_{REF}^+ \leq 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (2)(3)(4)

Parameter		Test Conditions	Typical (5)	Limits (6)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**12 + sign**	Bits (min)
ILE	Integral Linearity Error	After Auto Cal (7) (8)	±1/2	**±2**	LSB (max)
DNL	Differential Non-Linearity	After Auto Cal		**±1.5**	LSB (max)
	Positive Full-Scale Error	After Auto Cal (7) (8)	±1/2	**±3.0**	LSB (max)
	Negative Full-Scale Error	After Auto Cal (7)(8)	±1/2	**±3.0**	LSB (max)
	Offset Error	After Auto Cal (9)(8) $V_{IN}(+) = V_{IN}(-) = 2.048V$	±1/2	**±2**	LSB (max)

(1) The "12-Bit Conversion of Offset" and "12-Bit Conversion of Full-Scale" modes are intended to test the functionality of the device. Therefore, the output data from these modes are not an indication of the accuracy of a conversion result.

(2) Two on-chip diodes are tied to each analog input through a series resistor as shown below. Input voltage magnitude up to 5V above V_A+ or 5V below GND will not damage this device. However, errors in conversion can occur (if these diodes are forward biased by more than 50 mV) if the input voltage magnitude of selected or unselected analog input go above V_A+ or below GND by more than 50 mV. As an example, if V_A+ is 4.5 V_{DC}, full-scale input voltage must be ≤4.55 V_{DC} to ensure accurate conversions.



(3) To ensure accuracy, it is required that the V_A+ and V_D+ be connected together to the same power supply with separate bypass capacitors at each V^+ pin.

(4) With the test condition for V_{REF} ($V_{REF}+ - V_{REF}-$) given as +4.096V, the 12-bit LSB is 1.0 mV. For $V_{REF} = 2.5V$, the 12-bit LSB is 610 µV.

(5) Typical figures are at $T_J = T_A = 25°C$ and represent most likely parametric norm.

(6) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

(7) Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error, the straight line passes through negative full-scale and zero (see Figure 5 and Figure 6).

(8) The ADC12130 family's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a maximum repeatability uncertainty of 0.2 LSB.

(9) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Converter Electrical Characteristics (continued)

The following specifications apply for ($V^+ = V_A+ = V_D+ = +5V$, $V_{REF}+ = +4.096V$, and fully differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A+ = V_D+ = 3.3V$, $V_{REF}+ = 2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}- = 0V$, 12-bit + sign conversion mode(1), source impedance for analog inputs, V_{REF}^- and $V_{REF}^+ \le 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (2)(3)(4)

Parameter		Test Conditions	Typical (5)	Limits (6)	Units (Limits)
	DC Common Mode Error	After Auto Cal (10)	±2		LSB (max)
TUE	Total Unadjusted Error	After Auto Cal (7)(11) (12)	±1		LSB
	Multiplexer Chan-to-Chan Matching	$V^+ = +5V$ ±10%, $V_{REF} = +4.096V$	±0.05		LSB
	Power Supply Sensitivity				
	Offset Error + Full-Scale Error − Full-Scale Error Integral Linearity Error		±0.5 ±0.5 ±0.5 ±0.5		LSB LSB LSB LSB
UNIPOLAR DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = 5\ V_{PP}$, $V_{REF}^+ = 5.0V$	69.4		dB
		$f_{IN} = 20$ kHz, $V_{IN} = 5\ V_{PP}$, $V_{REF}^+ = 5.0V$	68.3		dB
		$f_{IN} = 40$ kHz, $V_{IN} = 5\ V_{PP}$, $V_{REF}+ = 5.0V$	65.7		dB
	−3 dB Full Power Bandwidth	$V_{IN} = 5\ V_{PP}$, where S/(N+D) drops 3 dB	31		kHz
DIFFERENTIAL DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = \pm5V$, $V_{REF}^+ = 5.0V$	77.0		dB
		$f_{IN} = 20$ kHz, $V_{IN} = \pm5V$, $V_{REF}^+ = 5.0V$	73.9		dB
		$f_{IN} = 40$ kHz, $V_{IN} = \pm5V$, $V_{REF}^+ = 5.0V$	67.0		dB
	−3 dB Full Power Bandwidth	$V_{IN} = \pm5V$, where S/(N+D) drops 3 dB	40		kHz
REFERENCE INPUT, ANALOG INPUTS AND MULTIPLEXER CHARACTERISTICS					
C_{REF}	Reference Input Capacitance		85		pF
$C_{A/D}$	A/DIN1 and A/DIN2 Analog Input Capacitance		75		pF
	A/DIN1 and A/DIN2 Analog Input Leakage Current	$V_{IN} = +5.0V$ or $V_{IN} = 0V$	±0.1		µA
	CH0–CH7 and COM Input Voltage		**GND − 0.05** **(V_A+) + 0.05**		V (min) V (max)
C_{CH}	CH0–CH7 and COM Input Capacitance		10		pF
C_{MUXOUT}	MUX Output Capacitance		20		pF
	Off Channel Leakage (13) CH0–CH7 and COM Pins	On Channel = 5V and Off Channel = 0V	−0.01		µA
		On Channel = 0V and Off Channel = 5V	0.01		µA
	On Channel Leakage (13) CH0–CH7 and COM Pins	On Channel = 5V and Off Channel = 0V	0.01		µA
		On Channel = 0V and Off Channel = 5V	−0.01		µA
	MUXOUT1 and MUXOUT2 Leakage Current	$V_{MUXOUT} = 5.0V$ or $V_{MUXOUT} = 0V$	0.01		µA
R_{ON}	MUX On Resistance	$V_{IN} = 2.5V$ and $V_{MUXOUT} = 2.4V$	850	**1900**	Ω (max)
	R_{ON} Matching Channel to Channel	$V_{IN} = 2.5V$ and $V_{MUXOUT} = 2.4V$	5		%

(10) The DC common-mode error is measured in the differential multiplexer mode with the assigned positive and negative input channels shorted together.
(11) Offset or Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the average value of the code transitions between −1 to 0 and 0 to +1 (see Figure 7).
(12) Total unadjusted error includes offset, full-scale, linearity and multiplexer errors.
(13) Channel leakage current is measured after the channel selection.

Converter Electrical Characteristics (continued)

The following specifications apply for ($V^+ = V_A+ = V_D+ = +5V$, $V_{REF}+ = +4.096V$, and fully differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A+ = V_D+ = 3.3V$, $V_{REF}+ = 2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}- = 0V$, 12-bit + sign conversion mode(1), source impedance for analog inputs, V_{REF}^- and $V_{REF}^+ \le 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (2)(3)(4)

Parameter		Test Conditions	Typical (5)	Limits (6)	Units (Limits)
	Channel-to-Channel Crosstalk	$V_{IN} = 5\ V_{PP}$, $f_{IN} = 40$ kHz	−72		dB
	MUX Bandwidth		90		kHz

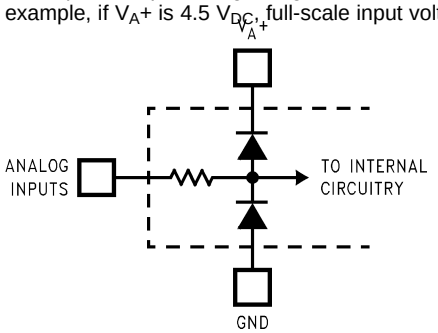
DC and Logic Electrical Characteristics

The following specifications apply for ($V^+ = V_A+ = V_D+ = +5V$, $V_{REF}+ = +4.096V$, and fully-differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A+ = V_D+ = +3.3V$, $V_{REF}+ = +2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}- = 0V$, 12-bit + sign conversion mode(1), source impedance for analog inputs, $V_{REF}-$ and $V_{REF}+ \le 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (2)(3)(4)

Parameter		Test Conditions	Typical (5)	$V^+ = V_A+ = V_D+ = 3.3V$ Limits (6)	$V^+ = V_A+ = V_D+ = 5V$ Limits (6)	Units (Limits)
CCLK, $\overline{CS}$, $\overline{CONV}$, DI, PD AND SCLK INPUT CHARACTERISTICS						
$V_{IN(1)}$	Logical “1” Input Voltage	$V_A+ = V_D+ = V^+ +10\%$		**2.0**	**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	$V_A+ = V_D+ = V^+ -10\%$		**0.8**	**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	$V_{IN} = V^+$	0.005	**1.0**	**1.0**	µA (max)
$I_{IN(0)}$	Logical `“0” Input Current	$V_{IN} = 0V$	−0.005	**−1.0**	**−1.0**	µA (min)
DO, EOC AND $\overline{DOR}$ DIGITAL OUTPUT CHARACTERISTICS						
$V_{OUT(1)}$	Logical “1” Output Voltage	$V_A+ = V_D+ = V^+ - 10\%$, $I_{OUT} = -360$ µA		**2.4**	**2.4**	V (min)
		$V_A+ = V_D+ = V^+ - 10\%$, $I_{OUT} = -10$ µA		**2.9**	**4.25**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	$V_A+ = V_D+ = V^+ - 10\%$ $I_{OUT} = 1.6$ mA		**0.4**	**0.4**	V (max)
I_{OUT}	TRI-STATE Output Current	$V_{OUT} = 0V$ $V_{OUT} = V^+$	−0.1 −0.1	**−3.0** **3.0**	**−3.0** **3.0**	µA (max) µA (max)
$+I_{SC}$	Output Short Circuit Source Current	$V_{OUT} = 0V$	−14			mA
$-I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = V_D+$	16			mA

(1) The “12-Bit Conversion of Offset” and “12-Bit Conversion of Full-Scale” modes are intended to test the functionality of the device. Therefore, the output data from these modes are not an indication of the accuracy of a conversion result.

(2) Two on-chip diodes are tied to each analog input through a series resistor as shown below. Input voltage magnitude up to 5V above V_A+ or 5V below GND will not damage this device. However, errors in conversion can occur (if these diodes are forward biased by more than 50 mV) if the input voltage magnitude of selected or unselected analog input go above V_A+ or below GND by more than 50 mV. As an example, if V_A+ is 4.5 V_{DC}, full-scale input voltage must be ≤4.55 V_{DC} to ensure accurate conversions.



(3) To ensure accuracy, it is required that the V_A+ and V_D+ be connected together to the same power supply with separate bypass capacitors at each V^+ pin.

(4) With the test condition for V_{REF} ($V_{REF}+ - V_{REF}-$) given as +4.096V, the 12-bit LSB is 1.0 mV. For $V_{REF} = 2.5V$, the 12-bit LSB is 610 µV.

(5) Typical figures are at $T_J = T_A = 25°C$ and represent most likely parametric norm.

(6) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

DC and Logic Electrical Characteristics (continued)

The following specifications apply for ($V^+ = V_A+ = V_D+ = +5V$, $V_{REF}+ = +4.096V$, and fully-differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A+ = V_D+ = +3.3V$, $V_{REF}+ = +2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}- = 0V$, 12-bit + sign conversion mode(1), source impedance for analog inputs, $V_{REF}-$ and $V_{REF}+ \leq 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (2)(3)(4)

Parameter		Test Conditions	Typical (5)	$V^+ = V_A+ = V_D+ = 3.3V$ Limits (6)	$V^+ = V_A+ = V_D+ = 5V$ Limits (6)	Units (Limits)
POWER SUPPLY CHARACTERISTICS						
I_D+	Digital Supply Current	Awake (Active)		**1.5**	**2.5**	mA (max)
		$\overline{CS}$ = HIGH, Powered Down, CCLK on	600			µA
		$\overline{CS}$ = HIGH, Powered Down, CCLK off	20			µA
I_A+	Positive Analog Supply Current	Awake (Active)		**3.0**	**4.0**	mA (max)
		$\overline{CS}$ = HIGH, Powered Down, CCLK on	10			µA
		$\overline{CS}$ = HIGH, Powered Down, CCLK off	0.1			µA
I_{REF}	Reference Input Current	$\overline{CS}$ = HIGH, Powered Down, CCLK on	70			µA
		$\overline{CS}$ = HIGH, Powered Down, CCLK off	0.1			µA

AC Electrical Characteristics

The following specifications apply for ($V^+ = V_A+ = V_D+ = +5V$, $V_{REF}+ = +4.096V$, and fully-differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A+ = V_D+ = +3.3V$, $V_{REF}+ = +2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}- = 0V$, 12-bit + sign conversion mode(1), source impedance for analog inputs, $V_{REF}-$ and $V_{REF}+ \leq 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (2)

Parameter		Test Conditions	Typical (3)	Limits (4)	Units (Limits)
f_{CK}	Conversion Clock (CCLK) Frequency		10 1	**5**	MHz (max) MHz (min)
f_{SK}	Serial Data Clock SCLK Frequency		10 0	**5**	MHz (max) Hz (min)
	Conversion Clock Duty Cycle			**40** **60**	% (min) % (max)
	Serial Data Clock Duty Cycle			**40** **60**	% (min) % (max)
t_C	Conversion Time	12-Bit + Sign or 12-Bit	44(t_{CK})	**44(t_{CK})**	(max)
				8.8	µs (max)

(1) The "12-Bit Conversion of Offset" and "12-Bit Conversion of Full-Scale" modes are intended to test the functionality of the device. Therefore, the output data from these modes are not an indication of the accuracy of a conversion result.
(2) Timing specifications are tested at the TTL logic levels, $V_{OL} = 0.4V$ for a falling edge and $V_{OL} = 2.4V$ for a rising edge. TRI-STATE output voltage is forced to 1.4V.
(3) Typical figures are at $T_J = T_A = 25°C$ and represent most likely parametric norm.
(4) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

AC Electrical Characteristics (continued)

The following specifications apply for ($V^+ = V_A+ = V_D+ = +5V$, $V_{REF}+ = +4.096V$, and fully-differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A+ = V_D+ = +3.3V$, $V_{REF}+ = +2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}-$ = 0V, 12-bit + sign conversion mode(1), source impedance for analog inputs, $V_{REF}-$ and $V_{REF}+ \leq 25\Omega$, $f_{CK} = f_{SK}$ = 5 MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C. (2)

Parameter		Test Conditions	Typical (3)	Limits (4)	Units (Limits)
t_A	Acquisition Time (5)	6 Cycles Programmed	6(t_{CK})	**6(t_{CK})**	(min)
				7(t_{CK})	(max)
				1.2	µs (min)
				1.4	µs (max)
		10 Cycles Programmed	10(t_{CK})	**10(t_{CK})**	(min)
				11(t_{CK})	(max)
				2.0	µs (min)
				2.2	µs (max)
		18 Cycles Programmed	18(t_{CK})	**18(t_{CK})**	(min)
				19(t_{CK})	(max)
				3.6	µs (min)
				3.8	µs (max)
		34 Cycles Programmed	34(t_{CK})	**34(t_{CK})**	(min)
				35(t_{CK})	(max)
				6.8	µs (min)
				7.0	µs (max)
t_{CAL}	Self-Calibration Time		4944(t_{CK})	**4944(t_{CK})**	(max)
				988.8	µs (max)
t_{AZ}	Auto Zero Time		76(t_{CK})	**76(t_{CK})**	(max)
				15.2	µs (max)
t_{SYNC}	Self-Calibration or Auto Zero Synchronization Time from DOR		2(t_{CK})	**2(t_{CK})**	(min)
				3(t_{CK})	(max)
				0.40	µs (min)
				0.60	µs (max)
$t_{\overline{DOR}}$	DOR High Time when $\overline{CS}$ is Low Continuously for Read Data and Software Power Up/Down		9(t_{SK})	**9(t_{SK})**	(max)
				1.8	µs (max)
$t_{\overline{CONV}}$	$\overline{CONV}$ Valid Data Time		8(t_{SK})	**8(t_{SK})**	(max)
				1.6	µs (max)

(5) If SCLK and CCLK are driven from the same clock source, then t_A is 6, 10, 18 or 34 clock periods minimum and maximum.

AC Electrical Characteristics

The following specifications apply for ($V^+ = V_A+ = V_D+ = +5V$, $V_{REF}+ = +4.096V$, and fully-differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A+ = V_D+ = +3.3V$, $V_{REF}+ = +2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}-$ = 0V, 12-bit + sign conversion mode(1), source impedance for analog inputs, $V_{REF}-$ and $V_{REF}+ \leq 25\Omega$, $f_{CK} = f_{SK}$ = 5 MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C. (2) (Continued)

(1) The "12-Bit Conversion of Offset" and "12-Bit Conversion of Full-Scale" modes are intended to test the functionality of the device. Therefore, the output data from these modes are not an indication of the accuracy of a conversion result.

(2) Timing specifications are tested at the TTL logic levels, V_{OL} = 0.4V for a falling edge and V_{OL} = 2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

AC Electrical Characteristics (continued)

The following specifications apply for ($V^+ = V_A+ = V_D+ = +5V$, $V_{REF}+ = +4.096V$, and fully-differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A+ = V_D+ = +3.3V$, $V_{REF}+ = +2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}- = 0V$, 12-bit + sign conversion mode(1), source impedance for analog inputs, $V_{REF}-$ and $V_{REF}+ \leq 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (2) (Continued)

Parameter		Test Conditions	Typical (3)	Limits (4)	Units (Limits)
t_{HPU}	Hardware Power-Up Time, Time from PD Falling Edge to EOC Rising Edge		500	**700**	µs (max)
t_{SPU}	Software Power-Up Time, Time from Serial Data Clock Falling Edge to EOC Rising Edge		500	**700**	µs (max)
t_{ACC}	Access Time Delay from $\overline{CS}$ Falling Edge to DO Data Valid		25	**60**	ns (max)
t_{SET-UP}	Set-Up Time of $\overline{CS}$ Falling Edge to Serial Data Clock Rising Edge			**50**	ns (min)
t_{DELAY}	Delay from SCLK Falling Edge to $\overline{CS}$ Falling Edge		0	**5**	ns (min)
t_{1H}, t_{0H}	Delay from $\overline{CS}$ Rising Edge to DO TRI-STATE	R_L = 3k, C_L = 100 pF	70	**100**	ns (max)
t_{HDI}	DI Hold Time from Serial Data Clock Rising Edge		5	**15**	ns (max)
t_{SDI}	DI Set-Up Time from Serial Data Clock Rising Edge		5	**10**	ns (min)
t_{HDO}	DO Hold Time from Serial Data Clock Falling Edge	R_L = 3k, C_L = 100 pF	35	**65** **5**	ns (max) ns (min)
t_{DDO}	Delay from Serial Data Clock Falling Edge to DO Data Valid		50	**90**	ns (max)
t_{RDO}	DO Rise Time, TRI-STATE to High DO Rise Time, Low to High	R_L = 3k, C_L = 100 pF	10 10	**40** **40**	ns (max) ns (max)
t_{FDO}	DO Fall Time, TRI-STATE to Low DO Fall Time, High to Low	R_L = 3k, C_L = 100 pF	15 15	**40** **40**	ns (max) ns (max)
t_{CD}	Delay from $\overline{CS}$ Falling Edge to $\overline{DOR}$ Falling Edge		45	**80**	ns (max)
t_{SD}	Delay from Serial Data Clock Falling Edge to $\overline{DOR}$ Rising Edge		45	**80**	ns (max)
C_{IN}	Capacitance of Logic Inputs		20		pF
C_{OUT}	Capacitance of Logic Outputs		20		pF

(3) Typical figures are at $T_J = T_A = 25°C$ and represent most likely parametric norm.
(4) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

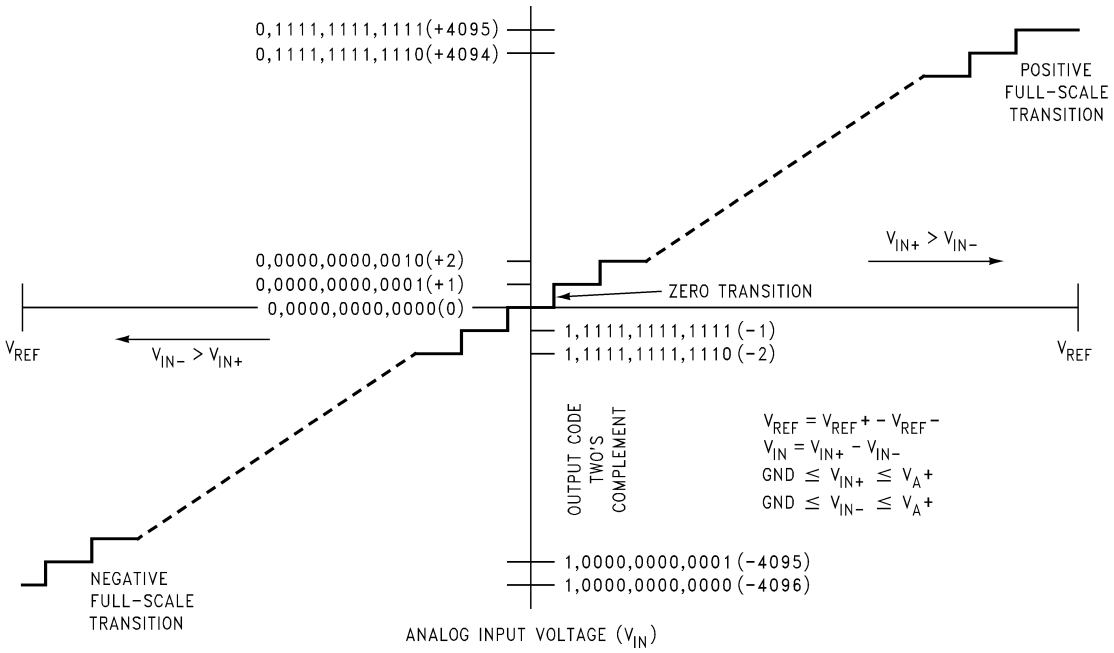


Figure 4. Transfer Characteristic

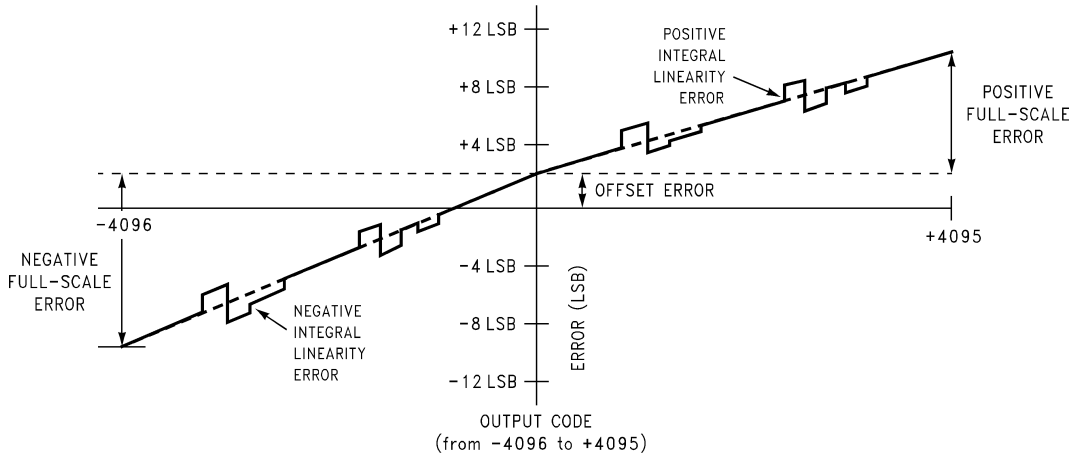


Figure 5. Simplified Error Curve vs. Output Code without Auto Calibration or Auto Zero Cycles

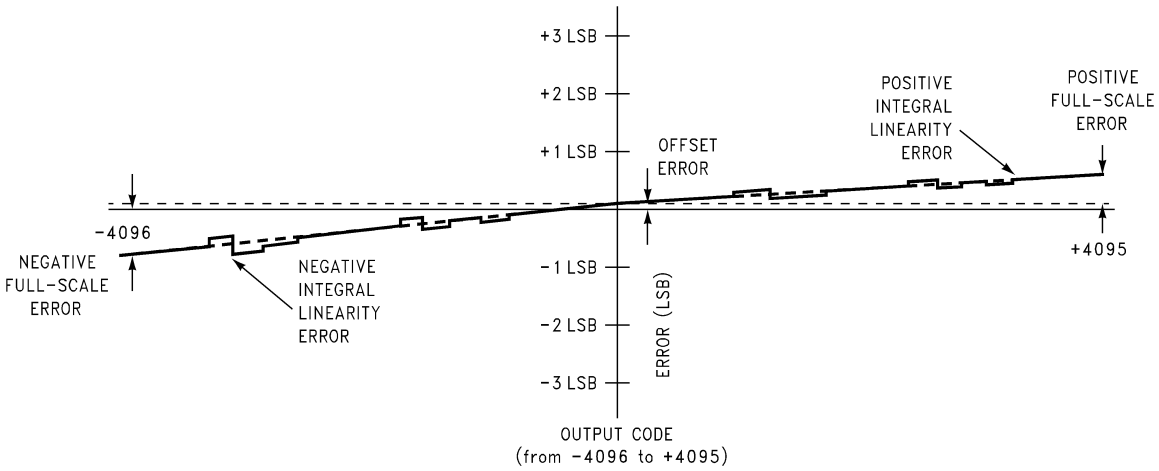


Figure 6. Simplified Error Curve vs. Output Code after Auto Calibration Cycle

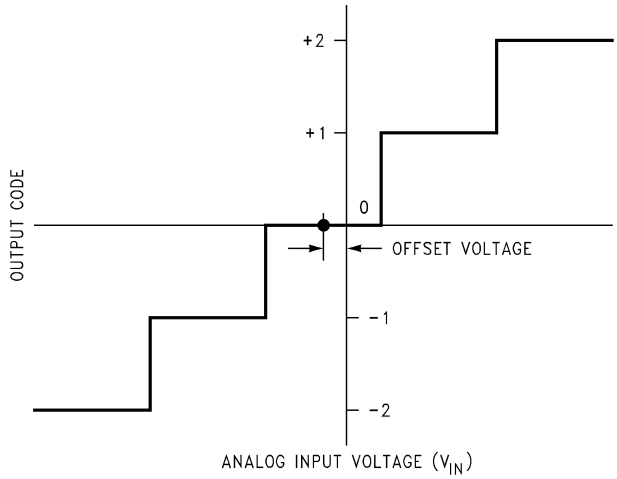


Figure 7. Offset or Zero Error Voltage

Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after Auto Calibration unless otherwise specified.

Linearity Error Change vs. Clock Frequency

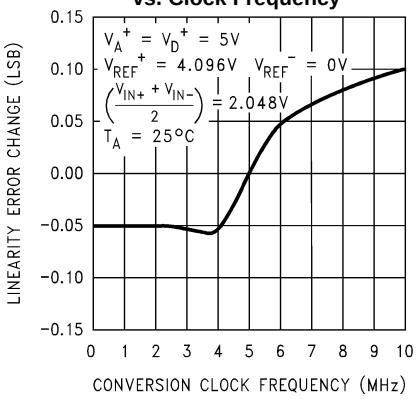


Figure 8.

Linearity Error Change vs. Temperature

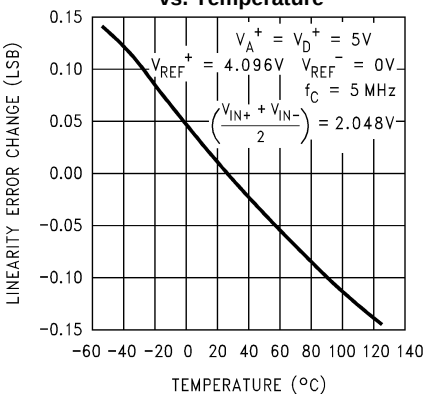


Figure 9.

Linearity Error Change vs. Reference Voltage

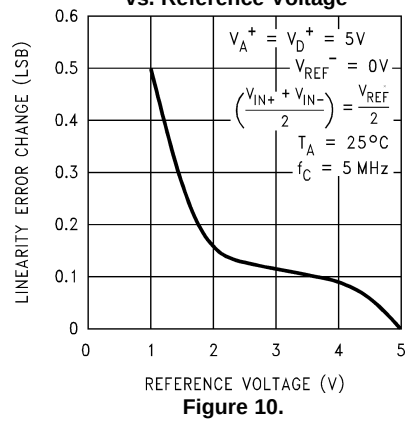


Figure 10.

Linearity Error Change vs. Supply Voltage

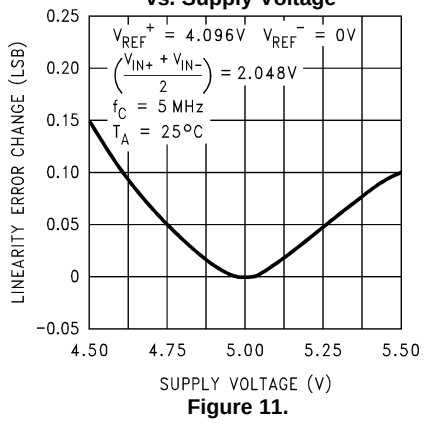


Figure 11.

Full-Scale Error Change vs. Clock Frequency

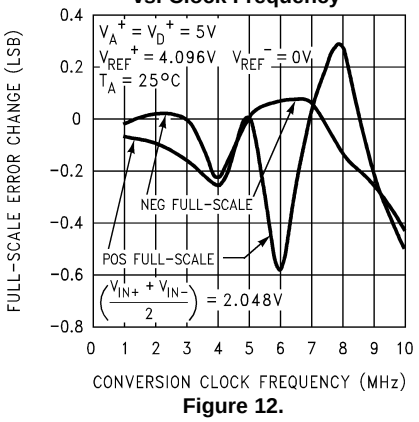


Figure 12.

Full-Scale Error Change vs. Temperature

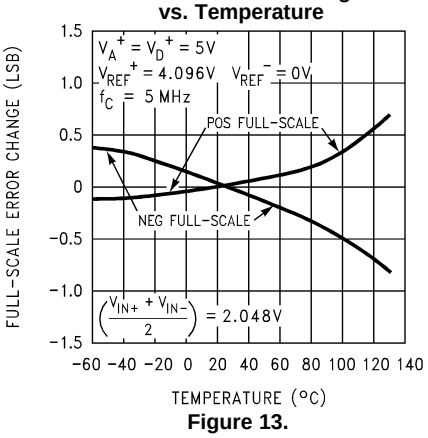


Figure 13.

Typical Performance Characteristics (continued)

The following curves apply for 12-bit + sign mode after Auto Calibration unless otherwise specified.

Full-Scale Error Change vs. Reference Voltage

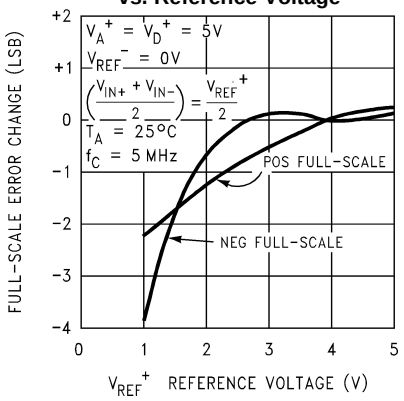


Figure 14.

Full-Scale Error Change vs. Supply Voltage

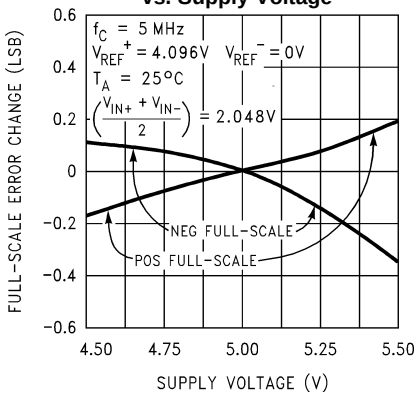


Figure 15.

Offset or Zero Error Change vs. Clock Frequency

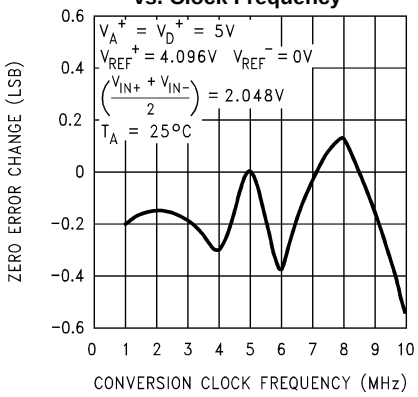


Figure 16.

Offset or Zero Error Change vs. Temperature

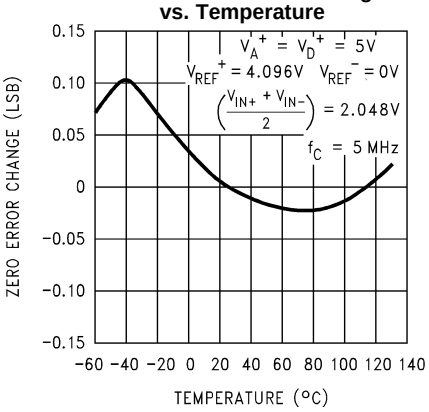


Figure 17.

Offset or Zero Error Change vs. Reference Voltage

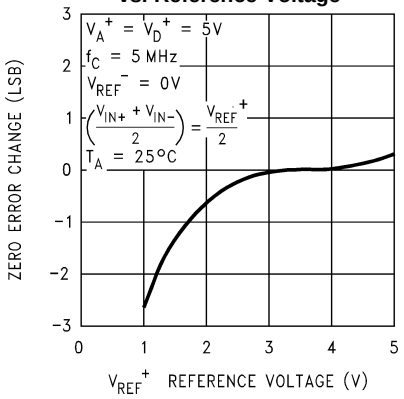


Figure 18.

Offset or Zero Error Change vs. Supply Voltage

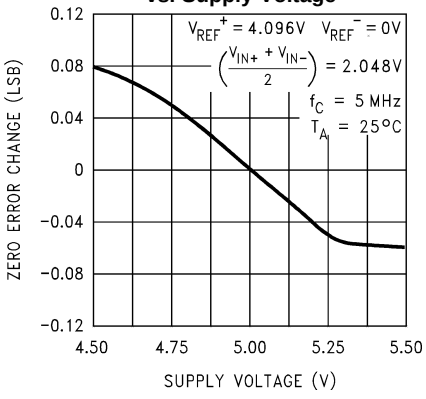


Figure 19.

Typical Performance Characteristics (continued)

The following curves apply for 12-bit + sign mode after Auto Calibration unless otherwise specified.

Analog Supply Current vs. Temperature

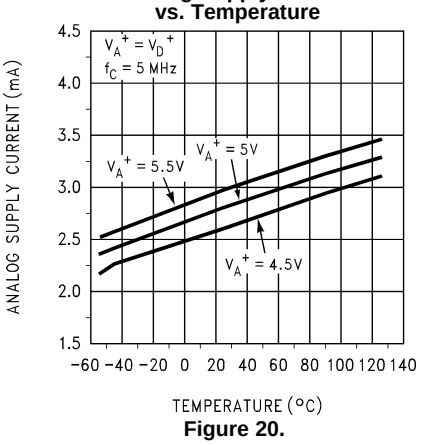


Figure 20.

Digital Supply Current vs. Clock Frequency

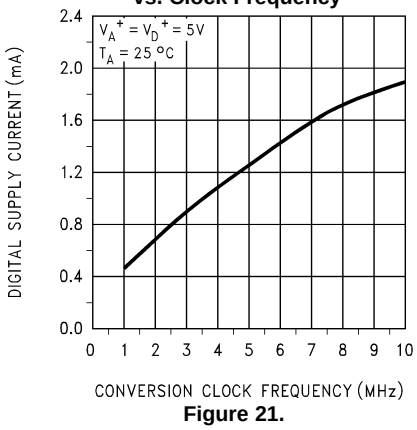


Figure 21.

Digital Supply Current vs. Temperature

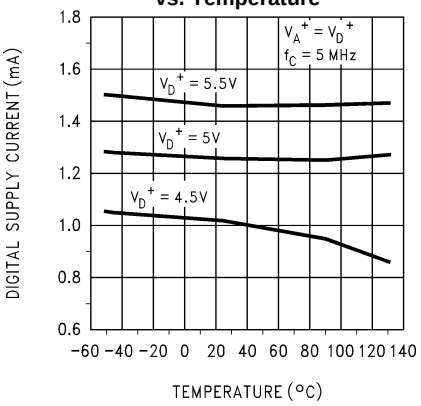


Figure 22.

Linearity Error Change vs. Temperature

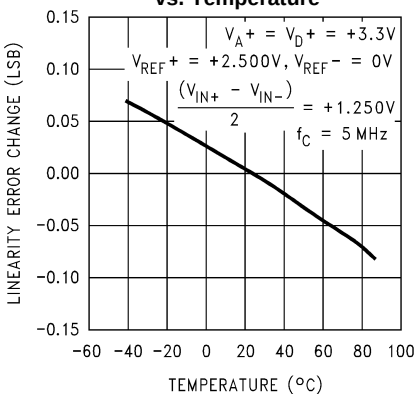


Figure 23.

Full-Scale Error Change vs. Temperature

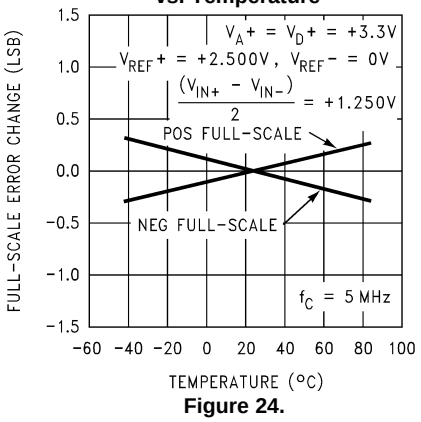


Figure 24.

Full-Scale Error Change vs. Supply Voltage

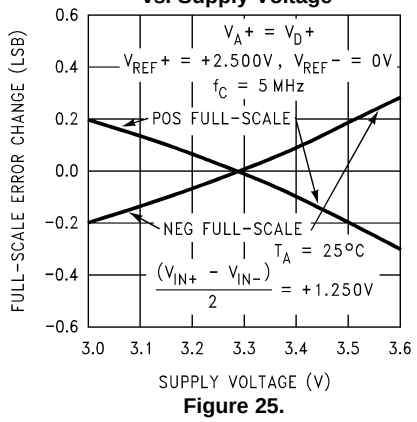


Figure 25.

Typical Performance Characteristics (continued)

The following curves apply for 12-bit + sign mode after Auto Calibration unless otherwise specified.

Offset or Zero Error Change vs. Temperature

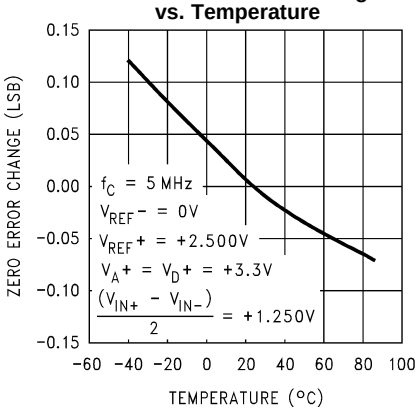


Figure 26.

Offset or Zero Error Change vs. Supply Voltage

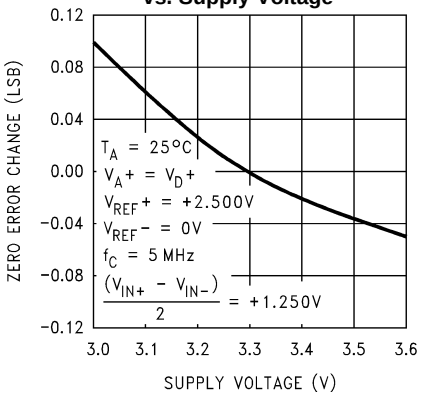


Figure 27.

Analog Supply Current vs. Temperature

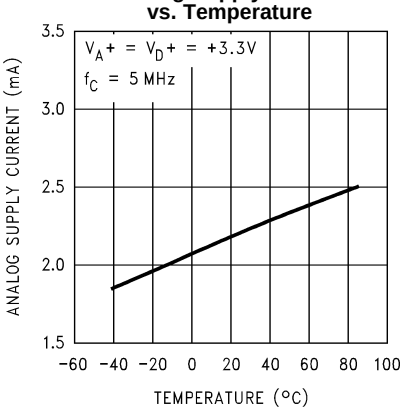


Figure 28.

Digital Supply Current vs. Temperature

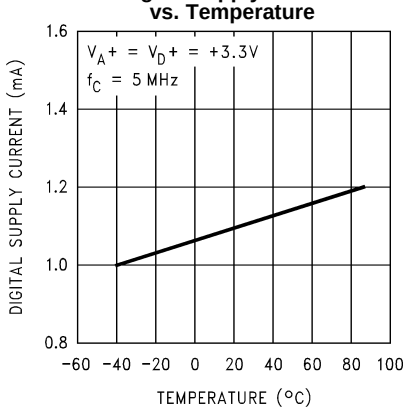


Figure 29.

Typical Dynamic Performance Characteristics

The following curves apply for 12-bit + sign mode after Auto Calibration unless otherwise specified.

Bipolar Spectral Response with 1 kHz Sine Wave Input

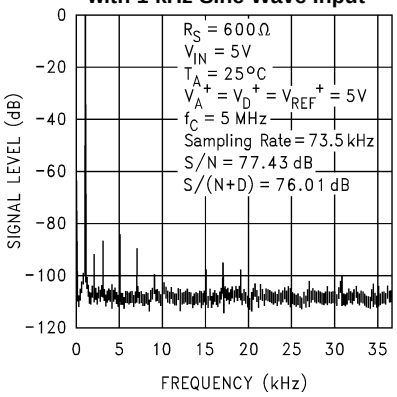


Figure 30.

Bipolar Spectral Response with 10 kHz Sine Wave Input

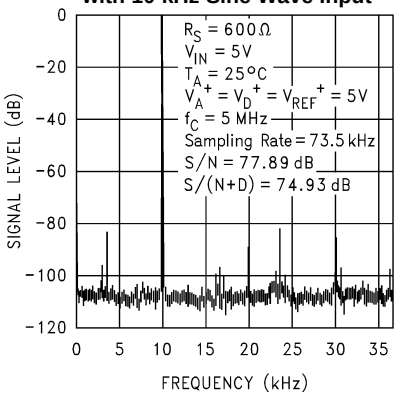


Figure 31.

Bipolar Spectral Response with 20 kHz Sine Wave Input

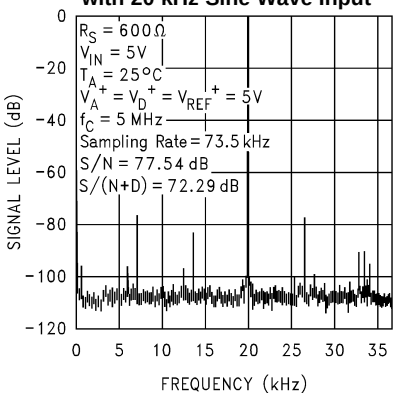


Figure 32.

Bipolar Spectral Response with 30 kHz Sine Wave Input

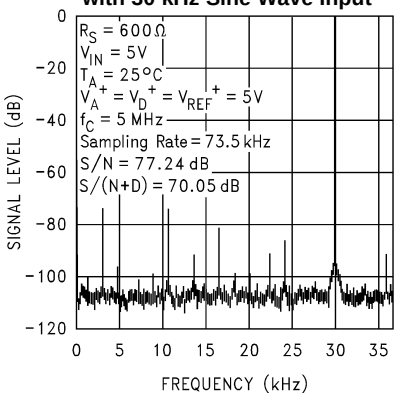


Figure 33.

Bipolar Spectral Response with 40 kHz Sine Wave Input

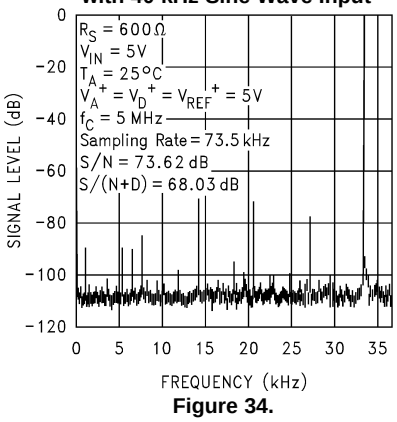


Figure 34.

Bipolar Spectral Response with 50 kHz Sine Wave Input

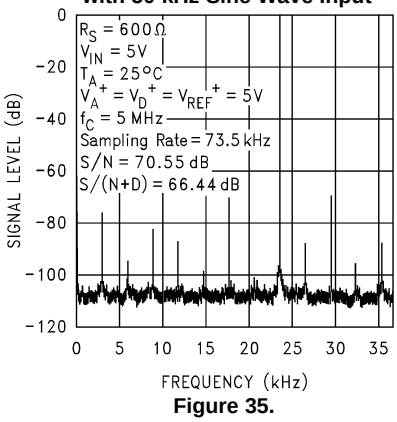


Figure 35.

Typical Dynamic Performance Characteristics (continued)

The following curves apply for 12-bit + sign mode after Auto Calibration unless otherwise specified.

Bipolar Spurious Free Dynamic Range

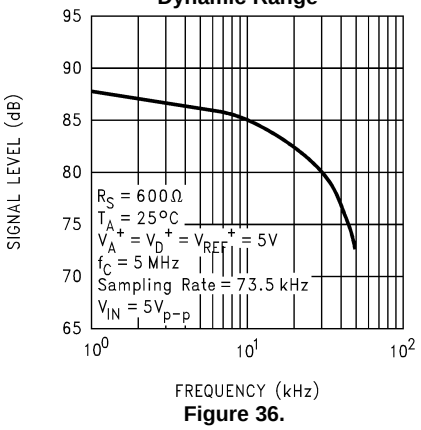


Figure 36.

Unipolar Signal-to-Noise Ratio vs. Input Frequency

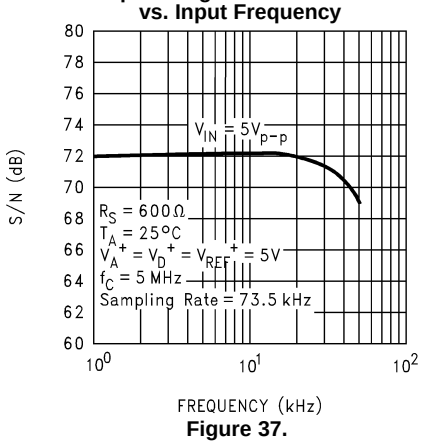


Figure 37.

Unipolar Signal-to-Noise + Distortion Ratio vs. Input Frequency

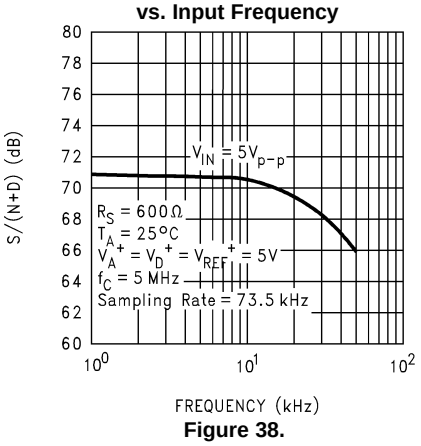


Figure 38.

Unipolar Signal-to-Noise + Distortion Ratio vs. Input Signal Level

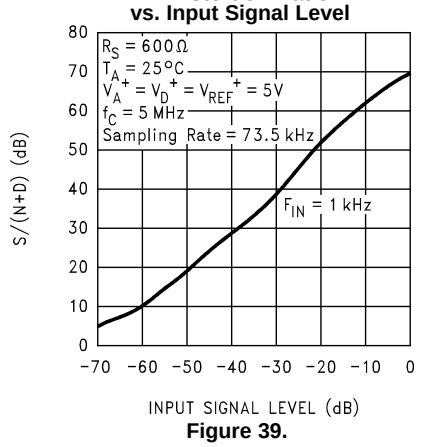


Figure 39.

Unipolar Spectral Response with 1 kHz Sine Wave Input

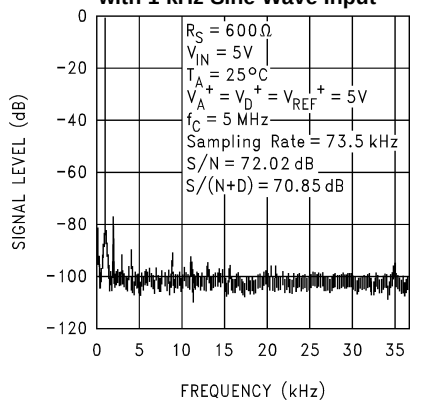


Figure 40.

Unipolar Spectral Response with 10 kHz Sine Wave Input

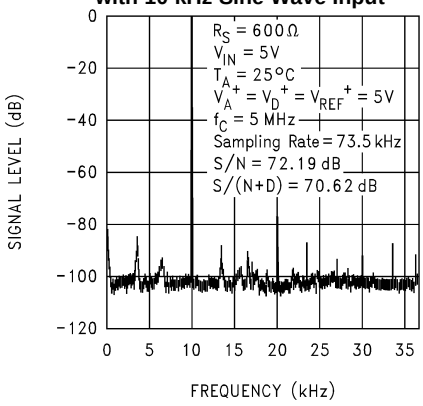


Figure 41.

Typical Dynamic Performance Characteristics (continued)

The following curves apply for 12-bit + sign mode after Auto Calibration unless otherwise specified.

Unipolar Spectral Response with 20 kHz Sine Wave Input

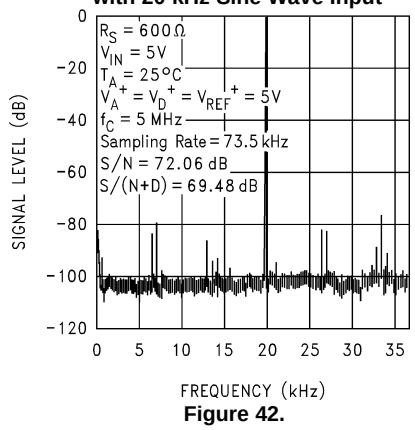


Figure 42.

Unipolar Spectral Response with 30 kHz Sine Wave Input

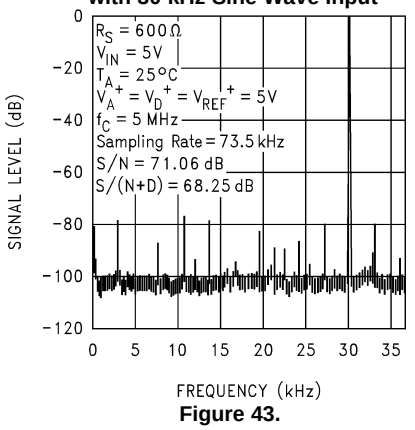


Figure 43.

Unipolar Spectral Response with 40 kHz Sine Wave Input

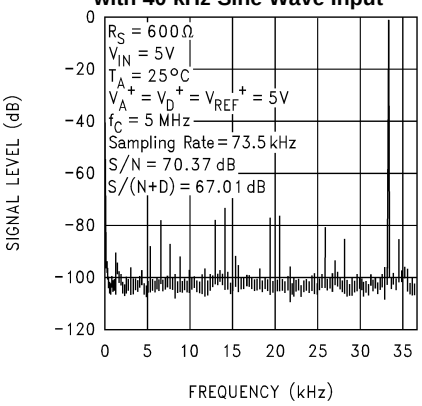


Figure 44.

Unipolar Spectral Response with 50 kHz Sine Wave Input

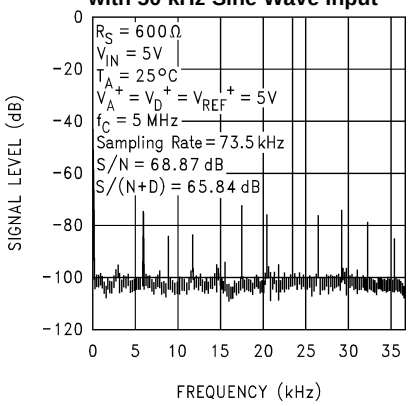


Figure 45.

Test Circuits

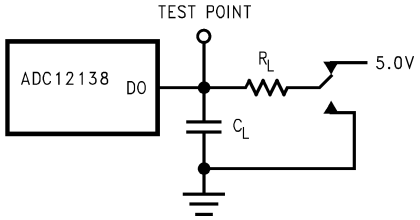


Figure 46. DO "TRI-STATE" (t_{1H}, t_{0H})

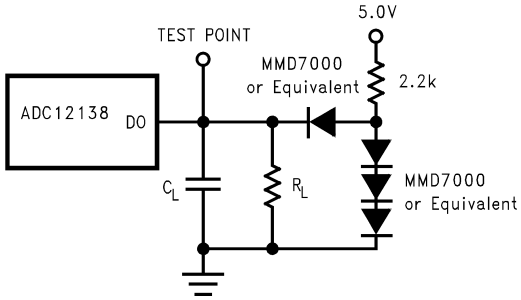


Figure 47. DO except "TRI-STATE"

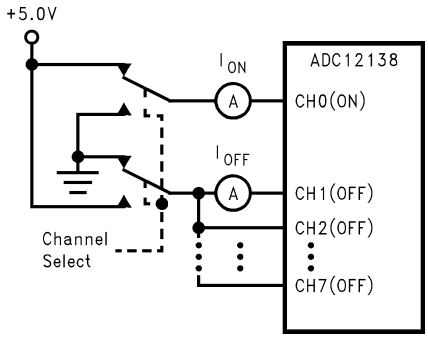


Figure 48. Leakage Current

Timing Diagrams

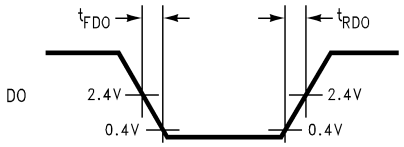


Figure 49. DO Falling and Rising Edge

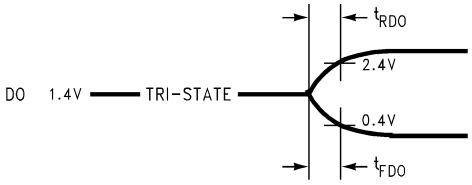


Figure 50.

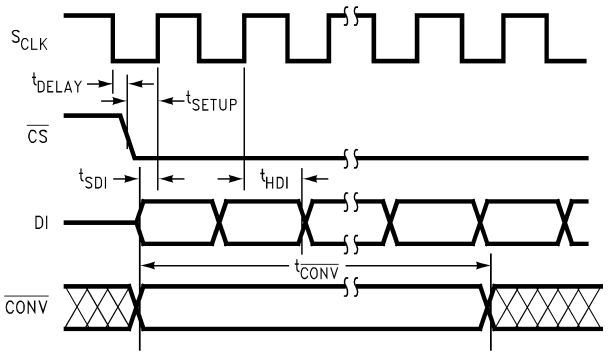


Figure 51. DI Data Input Timing

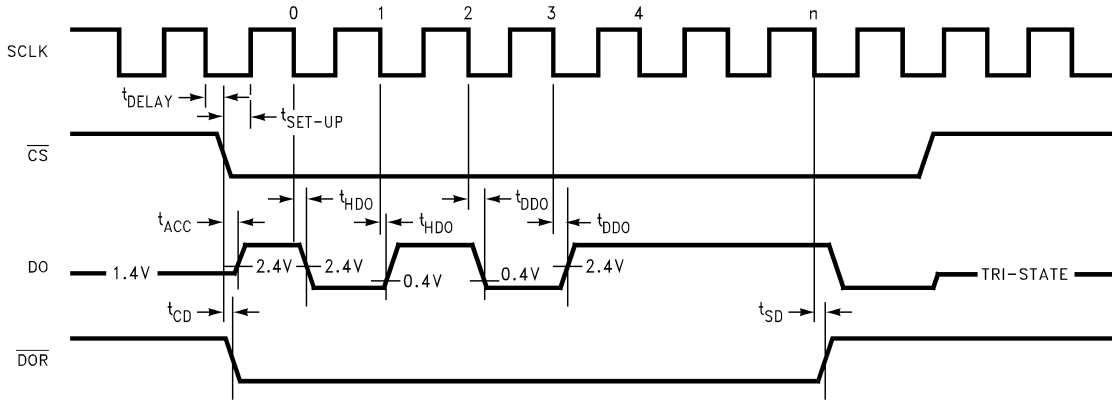


Figure 52. DO Data Output Timing Using $\overline{CS}$

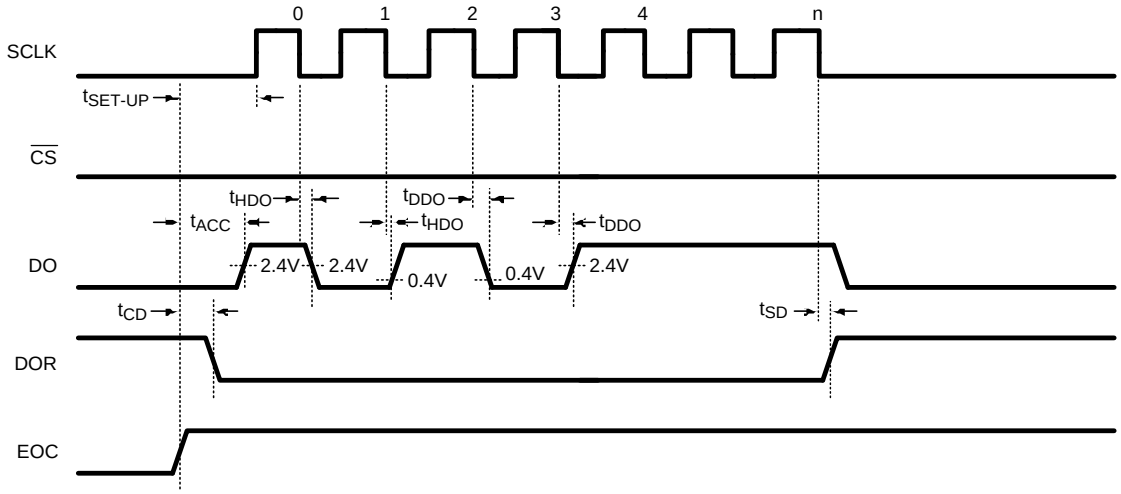
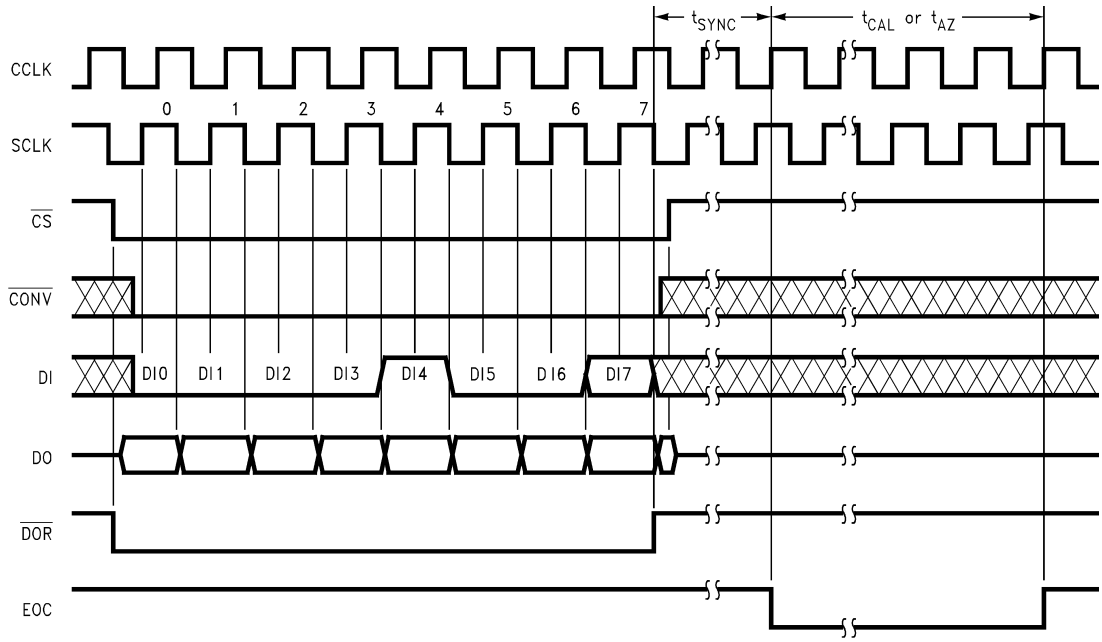


Figure 53. DO Data Output Timing with $\overline{CS}$ Continuously Low



Note: DO output data is not valid during this cycle.

Figure 54. ADC12138 Auto Cal or Auto Zero

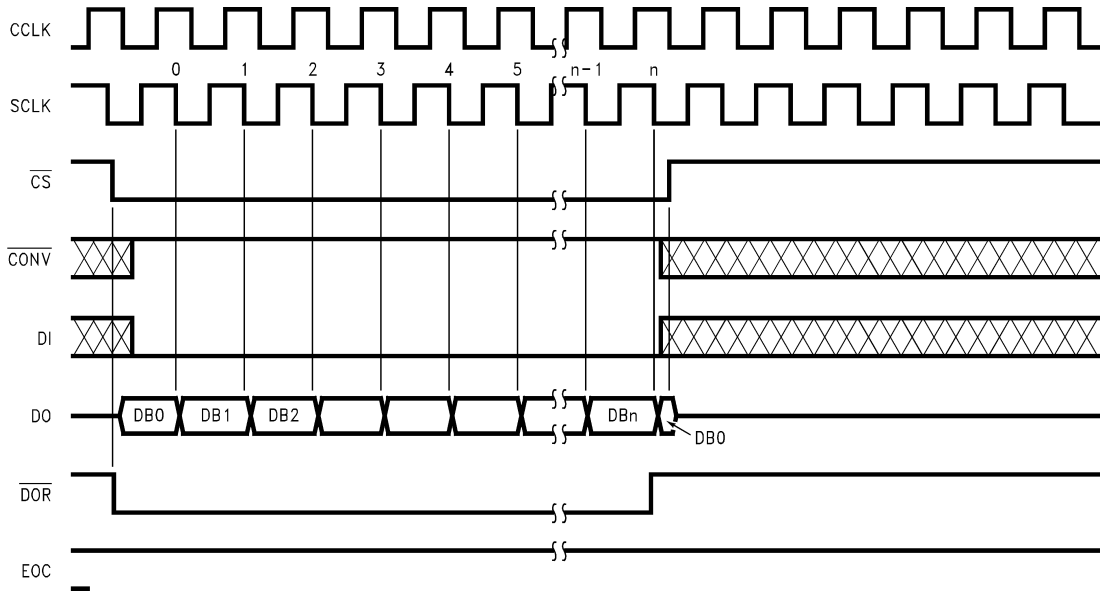


Figure 55. ADC12138 Read Data without Starting a Conversion Using $\overline{CS}$

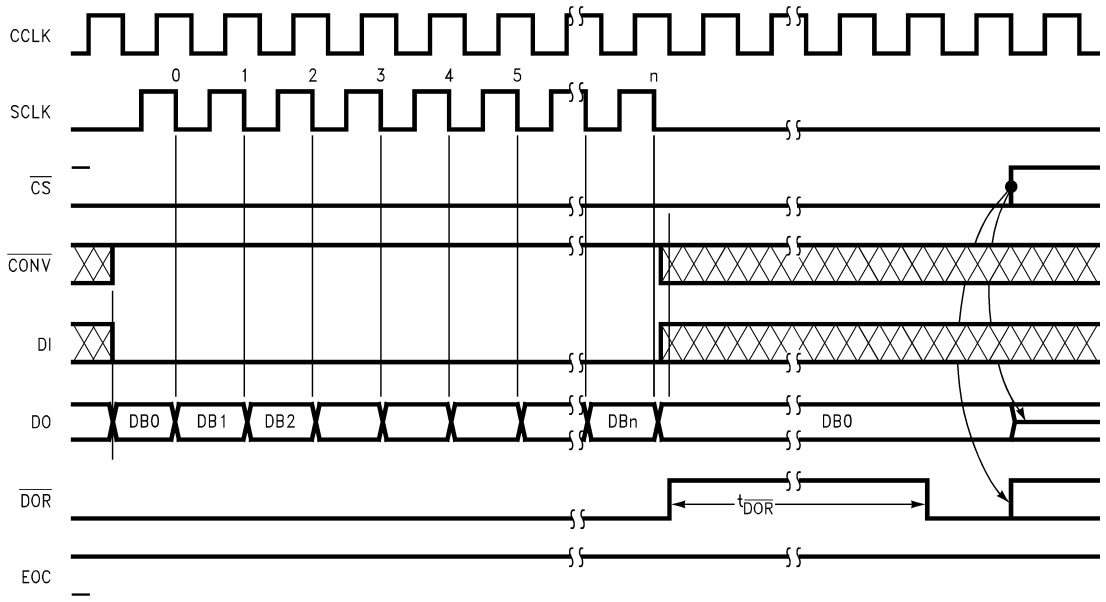


Figure 56. ADC12138 Read Data without Starting a Conversion with $\overline{CS}$ Continuously Low

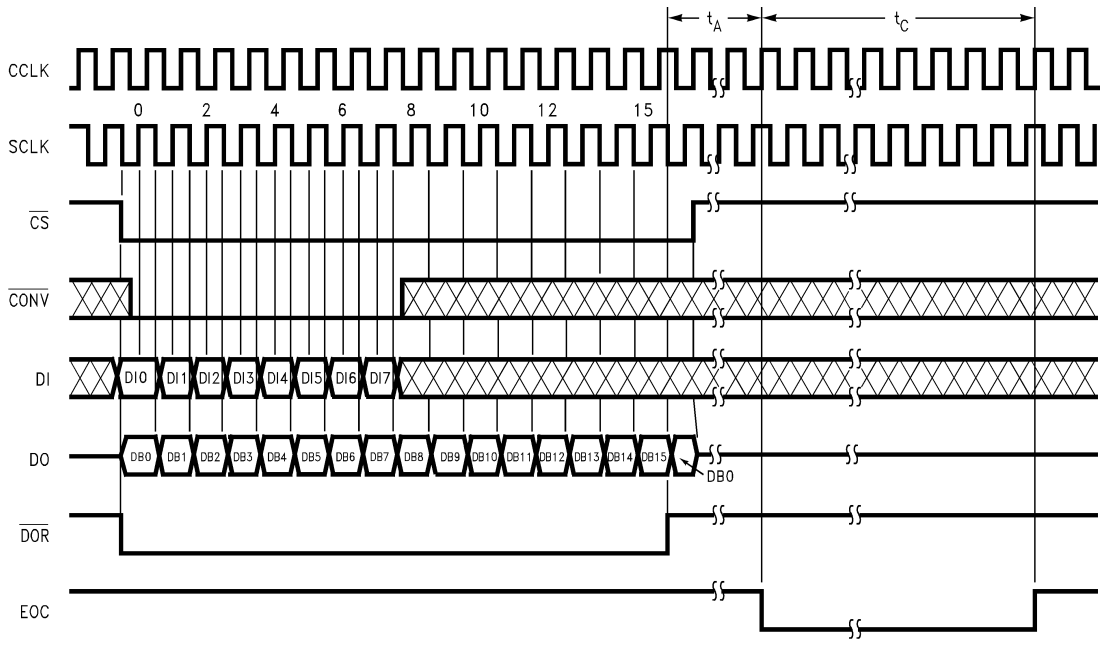


Figure 57. ADC12138 Conversion Using $\overline{CS}$ with 16-Bit Digital Output Format

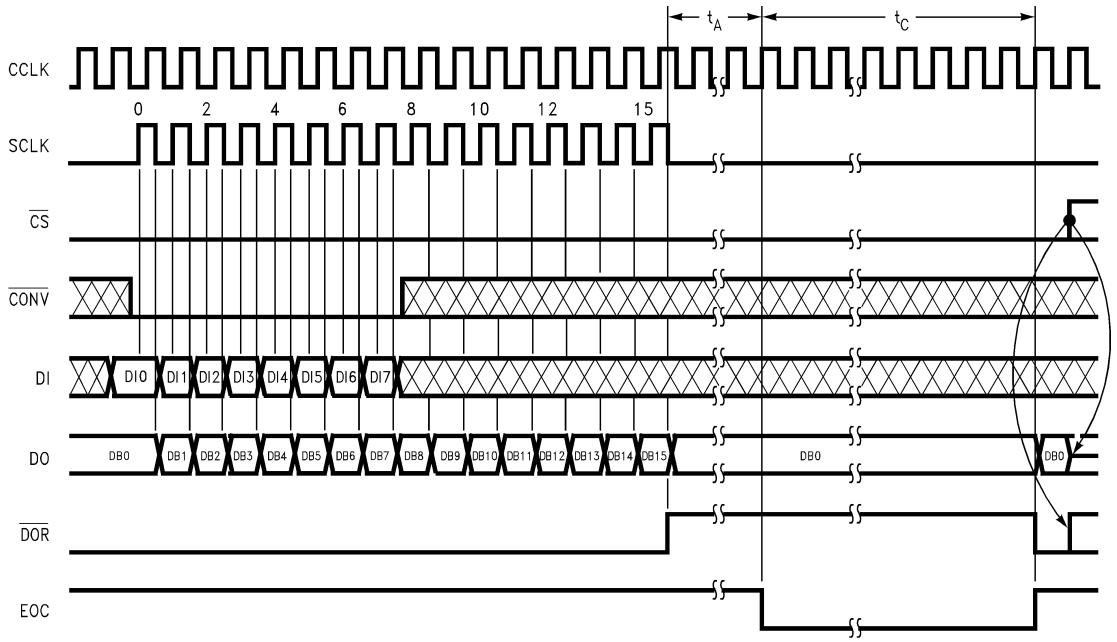


Figure 58. ADC12138 Conversion with $\overline{CS}$ Continuously Low and 16-Bit Digital Output Format

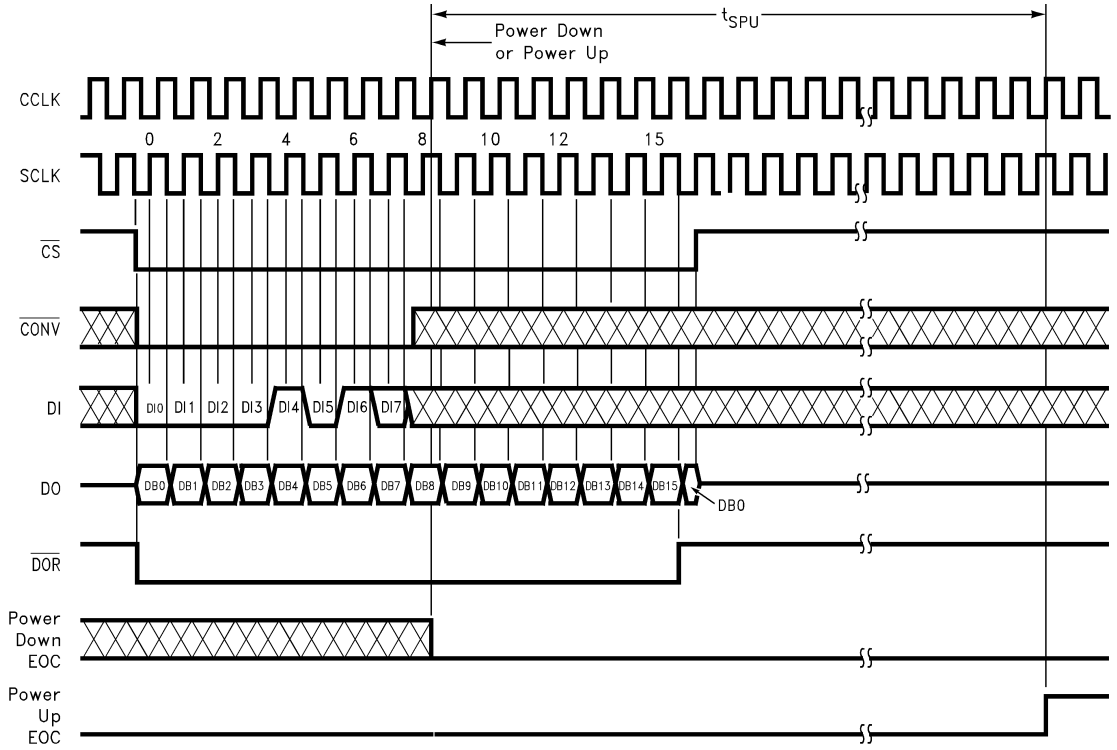


Figure 59. ADC12138 Software Power Up/Down Using $\overline{CS}$ with 16-Bit Digital Output Format

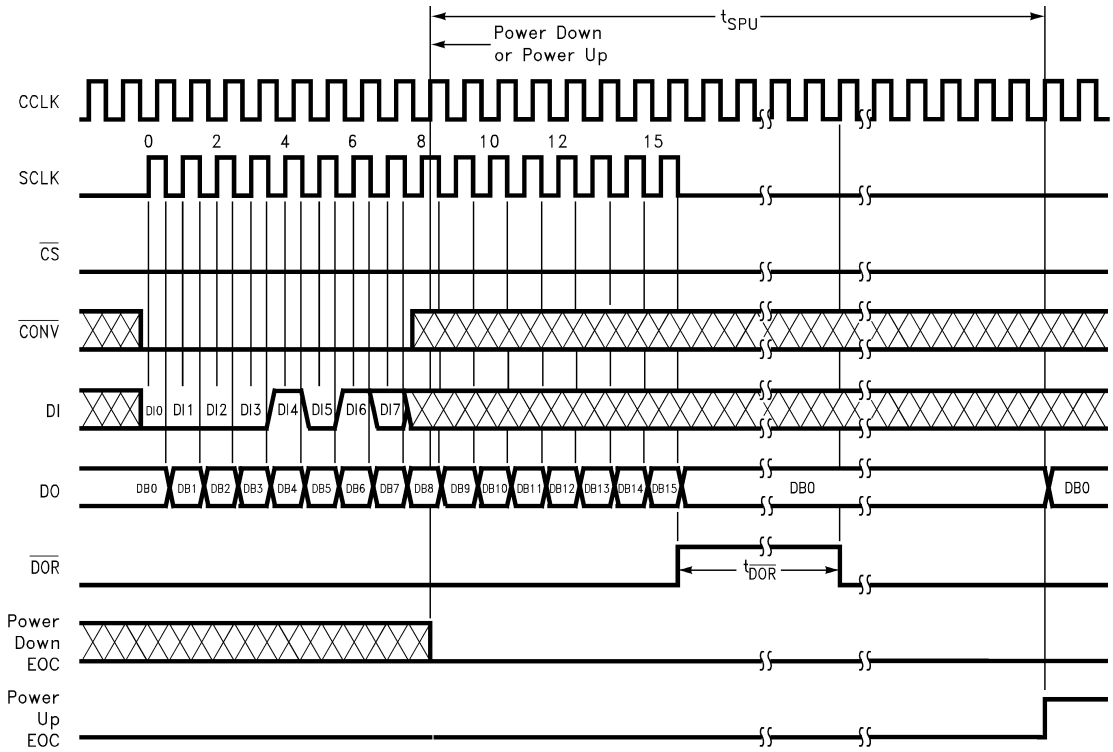
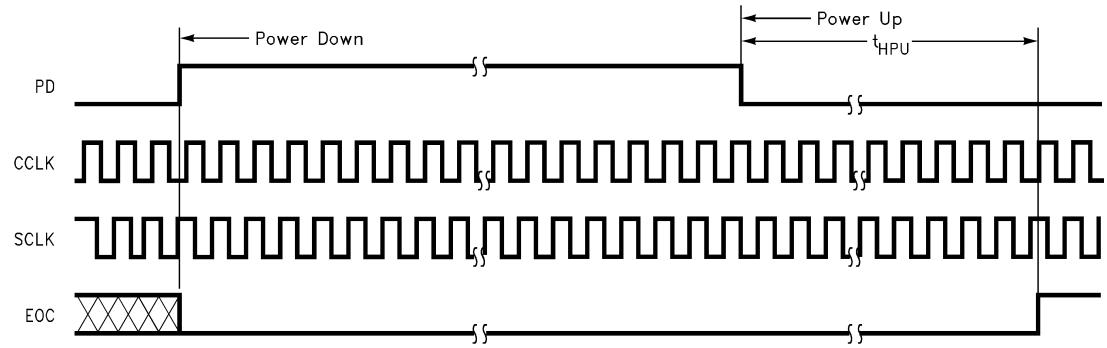


Figure 60. ADC12138 Software Power Up/Down with $\overline{CS}$ Continuously Low and 16-Bit Digital Output Format



Note: Hardware power up/down may occur at any time. If PD is high while a conversion is in progress that conversion will be corrupted and erroneous data will be stored in the output shift register.

Figure 61. ADC12138 Hardware Power Up/Down

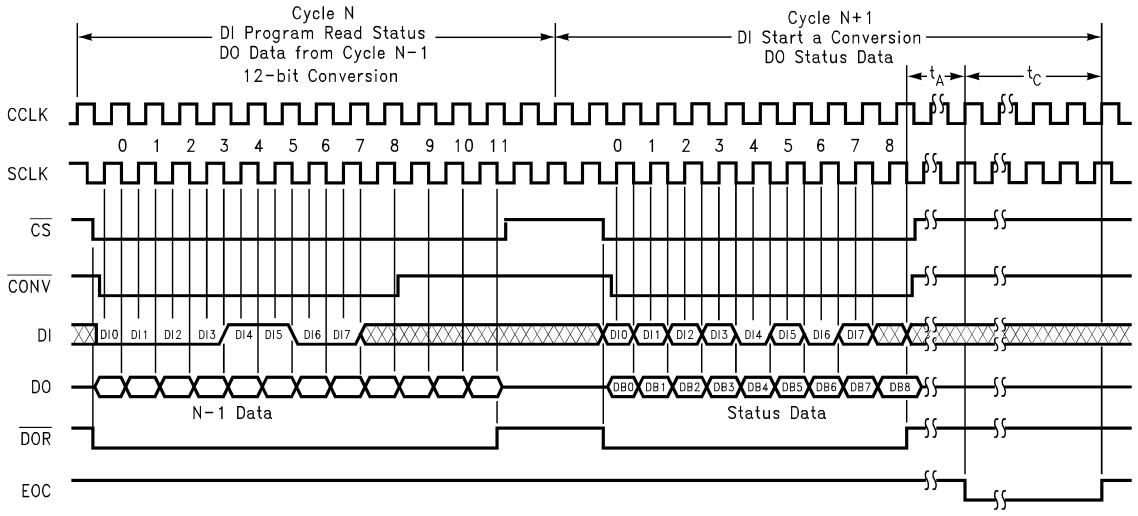
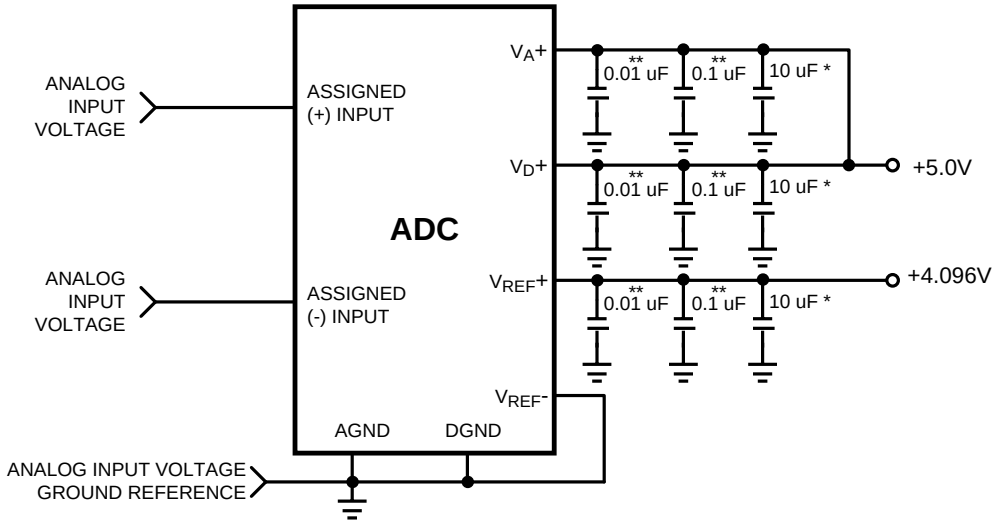


Figure 62. ADC12138 Configuration Modification—Example of a Status Read



*Tantalum
**Monolithic Ceramic or better

Figure 63. Recommended Power Supply Bypassing and Grounding

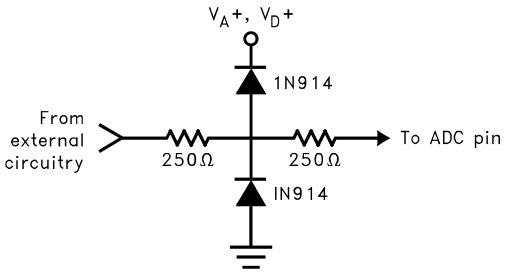


Figure 64. Protecting the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 Analog Pins

Format and Set-Up Tables

Table 1. Data Out Formats(1)

DO Formats			DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB 10	DB 11	DB 12	DB 13	DB 14	DB 15	DB 16
with Sign	MSB First	17 Bits	X	X	X	X	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB
		13 Bits	Sing	MSB	10	9	8	7	6	5	4	3	2	1	LSB				
	LSB First	17 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign	X	X	X	X
		13 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign				
with-out Sign	MSB First	16 Bits	0	0	0	0	MSB	10	9	8	7	6	5	4	3	2	1	LSB	
		12 Bits	MSB	10	9	8	7	6	5	4	3	2	1	LSB					
	LSB First	16 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	0	0	0	0	
		12 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB					

(1) X = High or Low state.

Table 2. ADC12138 Multiplexer Addressing

MUX Address				Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2									ADC Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	DI3	CH 0	CH 1	CH 2	CH 3	CH 4	CH 5	CH 6	CH 7	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	L	L	+	−								+	−	CH0	CH1	Differential
L	L	L	H			+	−						+	−	CH2	CH3	
L	L	H	L					+	−				+	−	CH4	CH5	
L	L	H	H							+	−		+	−	CH6	CH7	
L	H	L	L	−	+								−	+	CH0	CH1	
L	H	L	H			−	+						−	+	CH2	CH3	
L	H	H	L					−	+				−	+	CH4	CH5	
L	H	H	H							−	+		−	+	CH6	CH7	
H	L	L	L	+								−	+	−	CH0	COM	Single-Ended
H	L	L	H			+						−	+	−	CH2	COM	
H	L	H	L					+				−	+	−	CH4	COM	
H	L	H	H							+		−	+	−	CH6	COM	
H	H	L	L		+							−	+	−	CH1	COM	
H	H	L	H				+					−	+	−	CH3	COM	
H	H	H	L						+			−	+	−	CH5	COM	
H	H	H	H								+	−	+	−	CH7	COM	

Table 3. ADC12130 and ADC12132 Multiplexer Addressing(1)

MUX Address		Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2			ADC Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	CH0	CH1	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	+	−		+	−	CH0	CH1	Differential
L	H	−	+		−	+	CH0	CH1	
H	L	+		−	+	−	CH0	COM	Single-Ended
H	H		+	−	+	−	CH1	COM	

(1) ADC12130 do not have A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 pins.

Table 4. Mode Programming(1)

ADC12138	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7	Mode Selected (Current)	DO Format (next Conversion Cycle)
ADC12130 and ADC12132	DI0	DI1			DI2	DI3	DI4	DI5		
	See Table 2 or Table 3				L	L	L	L	12 Bit Conversion	12 or 13 Bit MSB First
	See Table 2 or Table 3				L	L	L	H	12 Bit Conversion	16 or 17 Bit MSB First
	See Table 2 or Table 3				L	H	L	L	12 Bit Conversion	12 or 13 Bit LSB First
	See Table 2 or Table 3				L	H	L	H	12 Bit Conversion	16 or 17 Bit LSB First
	L	L	L	L	H	L	L	L	Auto Cal	No Change
	L	L	L	L	H	L	L	H	Auto Zero	No Change
	L	L	L	L	H	L	H	L	Power Up	No Change
	L	L	L	L	H	L	H	H	Power Down	No Change
	L	L	L	L	H	H	L	L	Read Status Register	No Change
	L	L	L	L	H	H	L	H	Data Out without Sign	No Change
	H	L	L	L	H	H	L	H	Data Out with Sign	No Change
	L	L	L	L	H	H	H	L	Acquisition Time—6 CCLK Cycles	No Change
	L	H	L	L	H	H	H	L	Acquisition Time—10 CCLK Cycles	No Change
	H	L	L	L	H	H	H	L	Acquisition Time—18 CCLK Cycles	No Change
	H	H	L	L	H	H	H	L	Acquisition Time—34 CCLK Cycles	No Change
	L	L	L	L	H	H	H	H	User Mode	No Change
	H	X	X	X	H	H	H	H	Test Mode (CH1–CH7 become Active Outputs)	No Change

(1) The ADC powers up with no Auto Cal, no Auto Zero, 10 CCLK acquisition time, 12-bit + sign conversion, power up, 12- or 13-bit MSB First, and user mode.
X = Don't Care

Table 5. Conversion/Read Data Only Mode Programming(1)

$\overline{CS}$	$\overline{CONV}$	PD	Mode
L	L	L	See Table 4 for Mode
L	H	L	Read Only (Previous DO Format). No Conversion.
H	X	L	Idle
X	X	H	Power Down

(1) X = Don't Care

Table 6. Status Register

Status Bit Location	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
Status Bit	**PU**	**PD**	**Cal**		**12 or 13**	**16 or 17**	**Sign**	**Justification**	**Test Mode**
Function	**Device Status**			**DO Output Format Status**					
	"High" indicates a Power Up Sequence is in progress	"High" indicates a Power Down Sequence is in progress	"High" indicates an Auto Cal Sequence is in progress	Not used	"High" indicates a 12 or 13 bit format	"High" indicates a 16 or 17 bit format	"High" indicates that the sign bit is included. When "Low" the sign bit is not included.	When "High" the conversion result will be output MSB first. When "Low" the result will be output LSB first.	When "High" the device is in test mode. When "Low" the device is in user mode.

APPLICATION INFORMATION

NOTE: Some of the device/package combinations are obsolete and are shown and described here for reference only. Please see the TI web site for availability.

1.0 DIGITAL INTERFACE

1.1 Interface Concepts

The example in Figure 65 shows a typical sequence of events after the power is applied to the ADC12130/2/8:

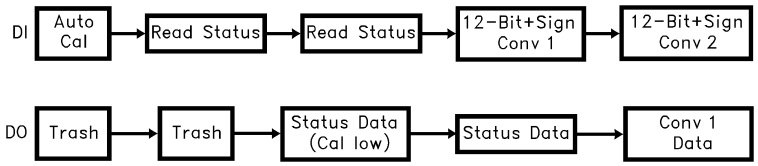


Figure 65. Typical Power Supply Power Up Sequence

The first instruction input to the ADC via DI initiates Auto Cal. The data output on DO at that time is meaningless and is completely random. To determine whether the Auto Cal has been completed, a read status instruction should be issued to the ADC. Again the data output at that time has no significance since the Auto Cal procedure modifies the data in the output shift register. To retrieve the status information, an additional read status instruction should be issued to the ADC. At this time the status data is available on DO. If the Cal signal in the status word is low, Auto Cal has been completed. Therefore, the next instruction issued can start a conversion. The data output at this time is again status information.

To keep noise from corrupting the conversion, status can not be read during a conversion. If $\overline{CS}$ is strobed and is brought low during a conversion, that conversion is prematurely ended. EOC can be used to determine the end of a conversion or the ADC controller can keep track in software of when it would be appropriate to communicate to the ADC again. Once it has been determined that the ADC has completed a conversion, another instruction can be transmitted to the ADC. The data from this conversion can be accessed when the next instruction is issued to the ADC.

Note, when $\overline{CS}$ is low continuously it is important to transmit the exact number of SCLK cycles, as shown in the timing diagrams. Not doing so will desynchronize the serial communication to the ADC. (See 1.3 $\overline{CS}$ Low Continuously Considerations.)

1.2 Changing Configuration

The configuration of the ADC12130/2/8 on power up defaults to 12-bit plus sign resolution, 12- or 13-bit MSB First, 10 CCLK acquisition time, user mode, no Auto Cal, no Auto Zero, and power up mode. Changing the acquisition time and turning the sign bit on and off requires an 8-bit instruction to be issued to the ADC. This instruction will not start a conversion. The instructions that select a multiplexer address and format the output data do start a conversion. Figure 66 describes an example of changing the configuration of the ADC12130/2/8.

During I/O sequence 1, the instruction at DI configures the ADC to do a conversion with 12-bit +sign resolution. Notice that, when the 6 CCLK Acquisition and Data Out without Sign instructions are issued to the ADC, I/O sequences 2 and 3, a new conversion is not started. The data output during these instructions is from conversion N, which was started during I/O sequence 1. The Figure 62 describes in detail the sequence of events necessary for a Data Out without Sign, Data Out with Sign, or 6/10/18/34 CCLK Acquisition time mode selection. Table 4 describes the actual data necessary to be loaded into the ADC to accomplish this configuration modification. The next instruction, shown in Figure 66, issued to the ADC starts conversion N+1 with 16-bit format and 12 bits of resolution formatted MSB first. Again the data output during this I/O cycle is the data from conversion N.

The number of SCLKs applied to the ADC during any conversion I/O sequence should vary in accord with the data out word format chosen during the previous conversion I/O sequence. The various formats and resolutions available are shown in Table 1. In Figure 66, since 16-bit without sign MSB first format was chosen during I/O sequence 4, the number of SCLKs required during I/O sequence 5 is sixteen. In the following I/O sequence the format changes to 12-bit without sign MSB first; therefore the number of SCLKs required during I/O sequence 6 changes accordingly to 12.

1.3 $\overline{CS}$ Low Continuously Considerations

When $\overline{CS}$ is continuously low, it is important to transmit the exact number of SCLK pulses that the ADC expects. Not doing so will desynchronize the serial communications to the ADC. When the supply power is first applied to the ADC, it will expect to see **13 SCLK pulses** for each I/O transmission. The number of SCLK pulses that the ADC expects to see is the same as the digital output word length. The digital output word length is controlled by the Data Out (DO) format. The DO format maybe changed any time a conversion is started or when the sign bit is turned on or off. The table below details out the number of clock periods required for different DO formats:

DO Format		Number of SCLKs Expected
12-Bit MSB or LSB First	SIGN OFF	12
	SIGN ON	13
16-Bit MSB or LSB first	SIGN OFF	16
	SIGN ON	17

If erroneous SCLK pulses desynchronize the communications, the simplest way to recover is by cycling the power supply to the device. Not being able to easily resynchronize the device is a shortcoming of leaving $\overline{CS}$ low continuously.

The number of clock pulses required for an I/O exchange may be different for the case when $\overline{CS}$ is left low continuously vs. the case when $\overline{CS}$ is cycled. Take the I/O sequence detailed in Figure 65 as an example. The table below lists the number of SCLK pulses required for each instruction:

Instruction	$\overline{CS}$ Low Continuously	$\overline{CS}$ Strobed
Auto Cal	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 1	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 2	13 SCLKs	13 SCLKs

1.4 Analog Input Channel Selection

The data input at DI also selects the channel configuration (see Table 2, Table 3, and Table 4). In Figure 66 the only times when the channel configuration could be modified would be during I/O sequences 1, 4, 5 and 6. Input channels are reselected before the start of each new conversion. Shown below is the data bit stream required at DI during I/O sequence number 4 in Figure 66 to set CH1 as the positive input and CH0 as the negative input for the different ADC versions.

Part Number	DI Data(1)							
	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7
ADC12130andADC12132	L	H	L	L	H	L	X	X
ADC12138	L	H	L	L	L	L	H	L

(1) X can be a logic high (H) or low (L).

1.5 Power Up/Down

The ADC may be powered down by taking the PD pin HIGH or by the instruction input at DI (see Table 4, Table 5, Figure 59, Figure 60, and Figure 61). When the ADC is powered down in this way, the ADC conversion circuitry is deactivated but the digital I/O circuitry is kept active.

Hardware power up/down is controlled by the state of the PD pin. Software power-up/down is controlled by the instruction issued to the ADC. If a software power up instruction is issued to the ADC while a hardware power down is in effect (PD pin high) the device will remain in the power-down state. If a software power down instruction is issued to the ADC while a hardware power up is in effect (PD pin low), the device will power down. When the device is powered down by software, it may be powered up by either issuing a software power up instruction or by taking PD pin high and then low. If the power down command is issued during a conversion, that conversion is interrupted, so the data output after power up cannot be relied upon.

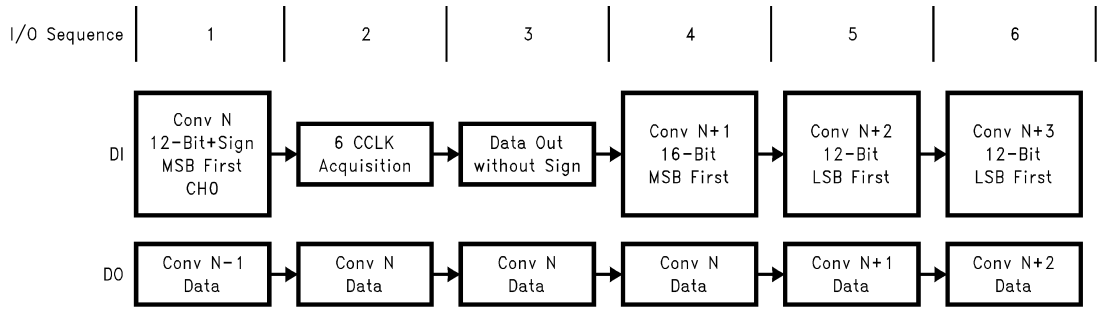


Figure 66. Changing the ADC's Conversion Configuration

1.6 User Mode and Test Mode

An instruction may be issued to the ADC to put it into test mode, which is used by the manufacturer to verify complete functionality of the device. During test mode CH0–CH7 become active outputs. If the device is inadvertently put into the test mode with $\overline{CS}$ continuously low, the serial communications may be desynchronized. Synchronization may be regained by cycling the power supply voltage to the device. Cycling the power supply voltage will also set the device into user mode. If $\overline{CS}$ is used in the serial interface, the ADC may be queried to see what mode it is in. This is done by issuing a "read STATUS register" instruction to the ADC. When bit 9 of the status register is high, the ADC is in test mode; when bit 9 is low the ADC, is in user mode. As an alternative to cycling the power supply, an instruction sequence may be used to return the device to user mode. This instruction sequence must be issued to the ADC using $\overline{CS}$. The following table lists the instructions required to return the device to user mode. Note that this **entire sequence**, including both Test Mode and User Mode values, should be sent to recover from the test mode.

Instruction	DI Data(1)							
	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7
TEST MODE	**H**	**X**	**X**	**X**	**H**	**H**	**H**	**H**
Reset Test Mode Instructions	L	L	L	L	H	H	H	L
	L	L	L	L	H	L	H	L
	L	L	L	L	H	L	H	H
USER MODE	L	L	L	L	H	H	H	H
Power Up	L	L	L	L	H	L	H	L
Set DO with or without Sign	H or L	L	L	L	H	H	L	H
Set Acquisition Time	H or L	H or L	L	L	H	H	H	L
Start a Conversion	H or L	H or L	H or L	H or L	L	H or L	H or L	H or L

(1) X = Don't Care

The power up, data with or without sign, and acquisition time instructions should be resent after returning to the user mode. This is to ensure that the ADC is in the required state before a conversion is started.

1.7 Reading the Data Without Starting a Conversion

The data from a particular conversion may be accessed without starting a new conversion by ensuring that the $\overline{CONV}$ line is taken high during the I/O sequence. See Figure 55 and Figure 56.Table 5 describes the operation of the $\overline{CONV}$ pin. It is not necessary to read the data as soon as $\overline{DOR}$ goes low. The data will remain in the output register *if* $\overline{CS}$ is brought high right after $\overline{DOR}$ goes high. A single conversion may be read as many times as desired before $\overline{CS}$ is brought low.

1.8 Brown Out Conditions

When the supply voltage dips below about 2.7V, the internal registers, including the calibration coefficients and all of the other registers, may lose their contents. When this happens the ADC will not perform as expected or not at all after power is fully restored. While writing the desired information to all registers and performing a calibration *might sometimes* cause recovery to full operation, the only sure recovery method is to reduce the supply voltage to below 0.5V, then reprogram the ADC and perform a calibration after power is fully restored.

2.0 THE ANALOG MULTIPLEXER

For the ADC12138, the analog input multiplexer can be configured with 4 differential channels or 8 single ended channels with the COM input as the zero reference or any combination thereof (see Figure 67). The difference between the voltages at the V_{REF}^+ and V_{REF}^- pins determines the input voltage span (V_{REF}). The analog input voltage range is 0 to V_A^+. Negative digital output codes result when $V_{IN}^- > V_{IN}^+$. The actual voltage at V_{IN}^- or V_{IN}^+ cannot go below AGND.

Figure 67. Input Multiplexer Options

A/DIN1 and A/DIN2 can be assigned as the + or − input

A/DIN1 is + input
A/DIN2 is − input

Figure 68. MUXOUT connections for multiplexer option

CH0, CH2, CH4, and CH6 can be assigned to the MUXOUT1 pin in the differential configuration, while CH1, CH3, CH5, and CH7 can be assigned to the MUXOUT2 pin. In the differential configuration, the analog inputs are paired as follows: CH0 with CH1, CH2 with CH3, CH4 with CH5 and CH6 with CH7. The A/DIN1 and A/DIN2 pins can be assigned positive or negative polarity.

With the single-ended multiplexer configuration, CH0 through CH7 can be assigned to the MUXOUT1 pin. The COM pin is always assigned to the MUXOUT2 pin. A/DIN1 is assigned as the positive input; A/DIN2 is assigned as the negative input. (See Figure 68).

The Multiplexer assignment tables for these ADCs (Table 2 and Table 3) summarize the aforementioned functions for the different versions of ADCs.

2.1 Biasing for Various Multiplexer Configurations

Figure 69 is an example of device connections for single-ended operation. The sign bit is always low. The digital output range is 0 0000 0000 0000 to 0 1111 1111 1111. One LSB is equal to 1 mV (4.1V/4096 LSBs).

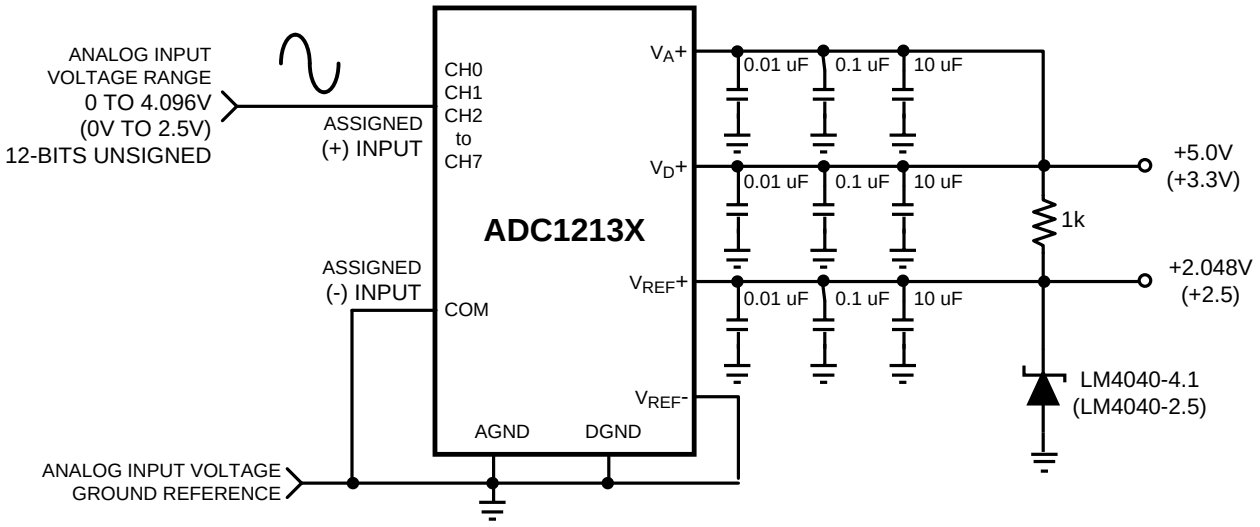


Figure 69. Single-Ended Biasing

For pseudo-differential signed operation, the circuit of Figure 70 shows a signal AC coupled to the ADC. This gives a digital output range of −4096 to +4095. With a 2.5V reference, 1 LSB is equal to 610 µV. Although the ADC is not production tested with a 2.5V reference, when V_A^+ and V_D^+ are +5.0V, linearity error typically will not change more than 0.1 LSB (see the curves in Typical Performance Characteristics). With the ADC set to an acquisition time of 10 clock periods, the input biasing resistor needs to be 600Ω or less. Notice though that the input coupling capacitor needs to be made fairly large to bring down the high pass corner. Increasing the acquisition time to 34 clock periods (with a 5 MHz CCLK frequency) would allow the 600Ω to increase to 6k, which would set the high pass corner at 26 Hz. Increasing R, to 6k would allow R_2 to be 2k with a 1 µF coupling capacitor.

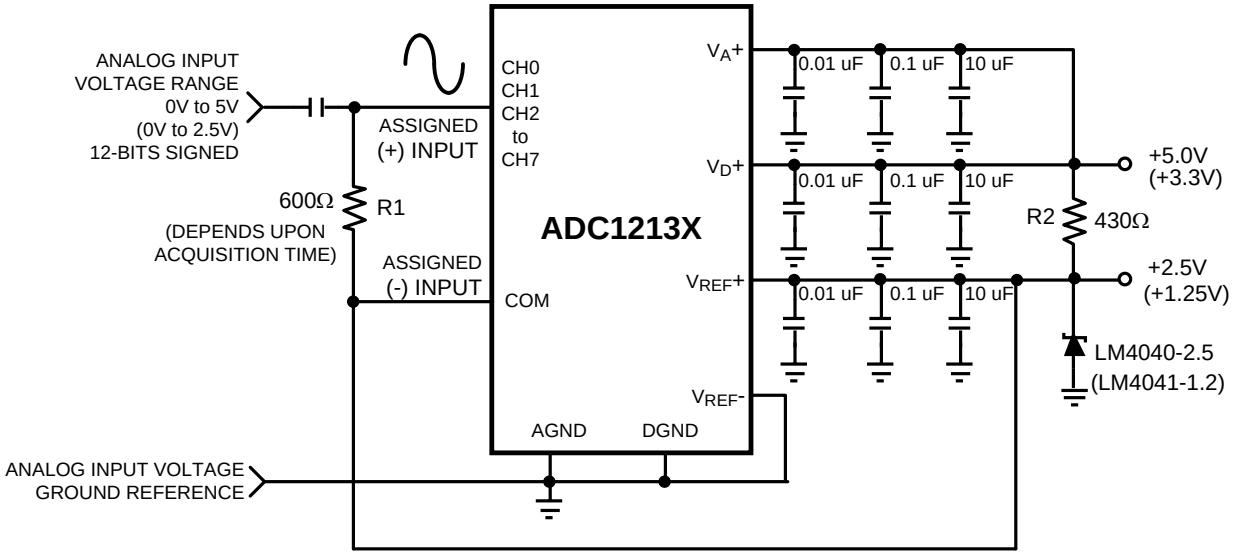


Figure 70. Pseudo-Differential Biasing with the Signal Source AC Coupled Directly into the ADC

An alternative method for biasing pseudo-differential operation is to use the +2.5V from the LM4040 to bias any amplifier circuits driving the ADC as shown in Figure 71. The value of the resistor pull-up biasing the LM4040-2.5 will depend upon the current required by the op amp biasing circuitry.

In the circuit of Figure 71, some voltage range is lost since the amplifier will not be able to swing to +5V and GND with a single +5V supply. Using an adjustable version of the LM4041 to set the full scale voltage at exactly 2.048V and a lower grade LM4040D-2.5 to bias up everything to 2.5V as shown in Figure 72 will allow the use of all the ADC's digital output range of −4096 to +4095 while leaving plenty of head room for the amplifier.

Fully differential operation is shown in Figure 73. One LSB for this case is equal to (4.1V/4096) = 1 mV.

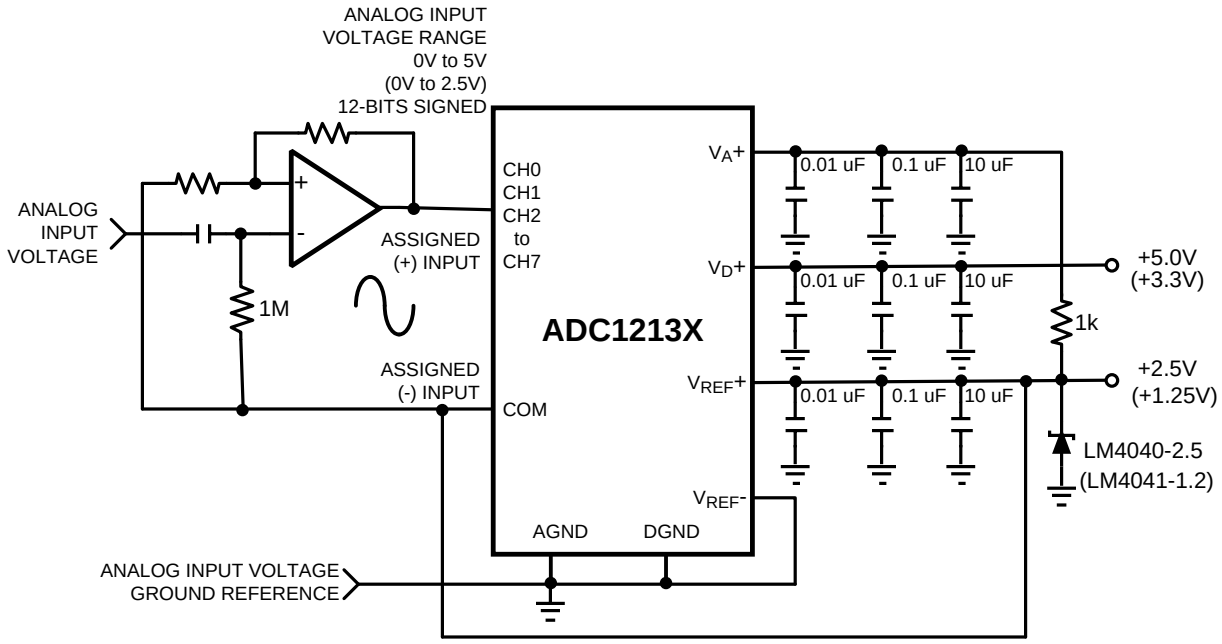


Figure 71. Alternative Pseudo-Differential Biasing

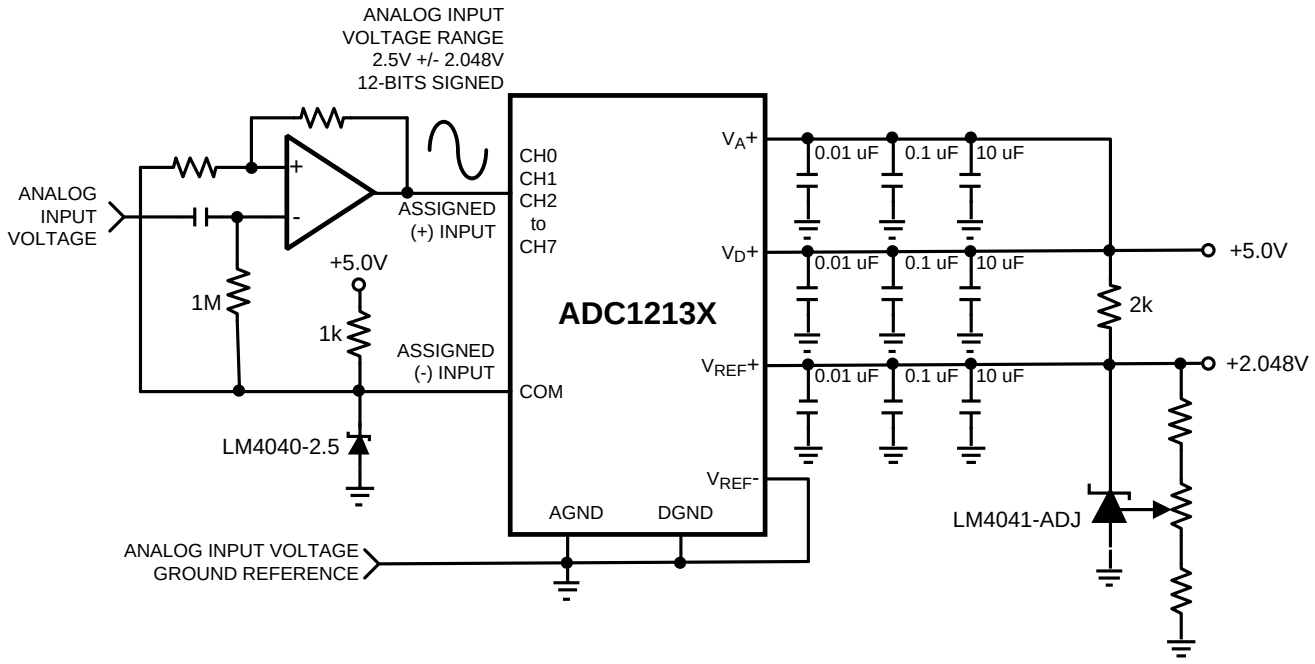


Figure 72. Pseudo-Differential Biasing without the Loss of Digital Output Range

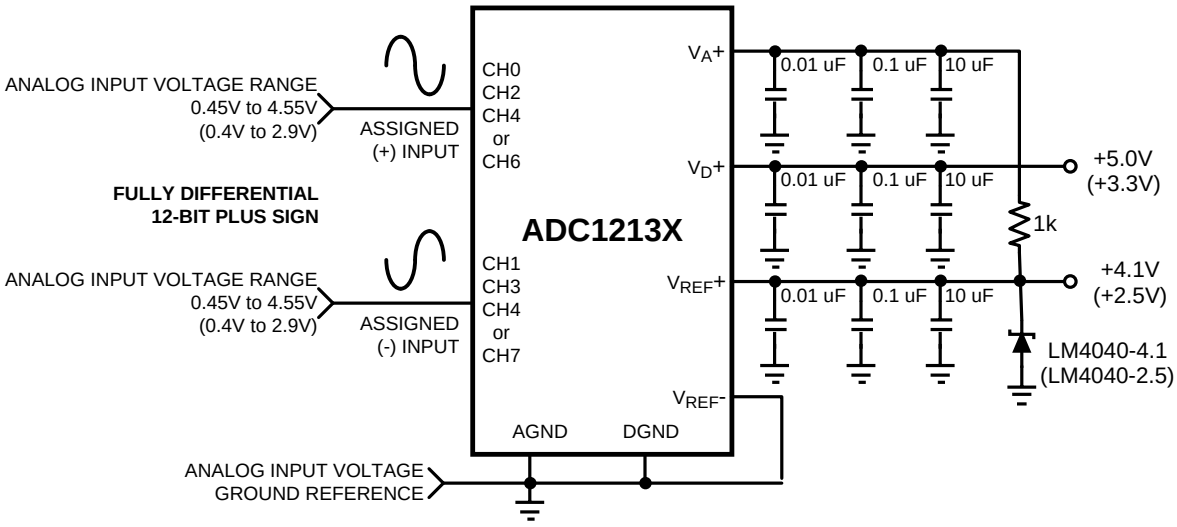
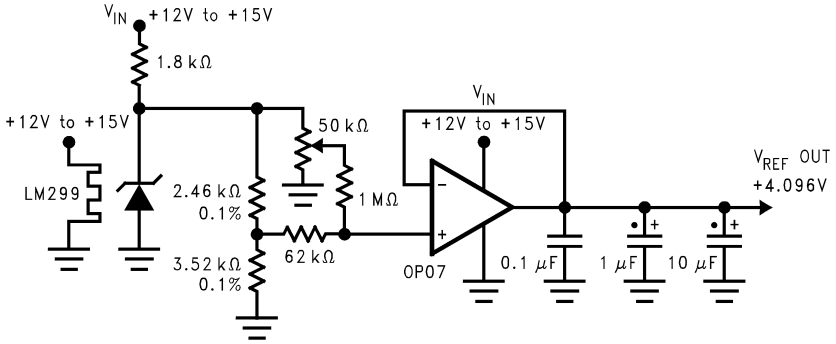


Figure 73. Fully Differential Biasing

3.0 REFERENCE VOLTAGE

The difference in the voltages applied to the V_{REF}^+ and V_{REF}^- defines the analog input span (the difference between the voltage applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground) over which 4095 positive and 4096 negative codes exist. The voltage sources driving V_{REF}^+ and V_{REF}^- must have very low output impedance and noise. The circuit in Figure 74 is an example of a very stable reference appropriate for use with the device.



*Tantalum

Figure 74. Low Drift Extremely Stable Reference Circuit

The ADC12130/2/8 can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the V_{REF}^+ pin is connected to V_A^+ and V_{REF}^- is connected to ground. This technique relaxes the system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions. For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

Below are recommended references along with some key specifications.

Part Number	Output Voltage Tolerance	Temperature Coefficient
LM4041CI-Adj	±0.5%	±100ppm/°C
LM4040AI-4.1	±0.1%	±100ppm/°C
LM4120AI-4.1	±0.2%	±50ppm/°C
LM4121AI-4.1	±0.2%	±50ppm/°C
LM4050AI-4.1	±0.1%	±50ppm/°C
LM4030AI-4.1	±0.05%	±10ppm/°C
LM4040AI-4.1	±0.1%	±3.0ppm/°C
Circuit of Figure 74	Adjustable	±2ppm/°C

The reference voltage inputs are not fully differential. The ADC12130/2/8 will not generate correct conversions or comparisons if V_{REF}^+ is taken below V_{REF}^-. Correct conversions result when V_{REF}^+ and V_{REF}^- differ by 1V or more and remain at all times between ground and V_A^+. The V_{REF} common mode range, $(V_{REF}^+ + V_{REF}^-)/2$, is restricted to $(0.1 \times V_A^+)$ to $(0.6 \times V_A^+)$. Therefore, with $V_A^+ = 5V$, the center of the reference ladder should not go below 0.5V or above 3.0V. Figure 75 is a graphic representation of the voltage restrictions on V_{REF}^+ and V_{REF}^-.

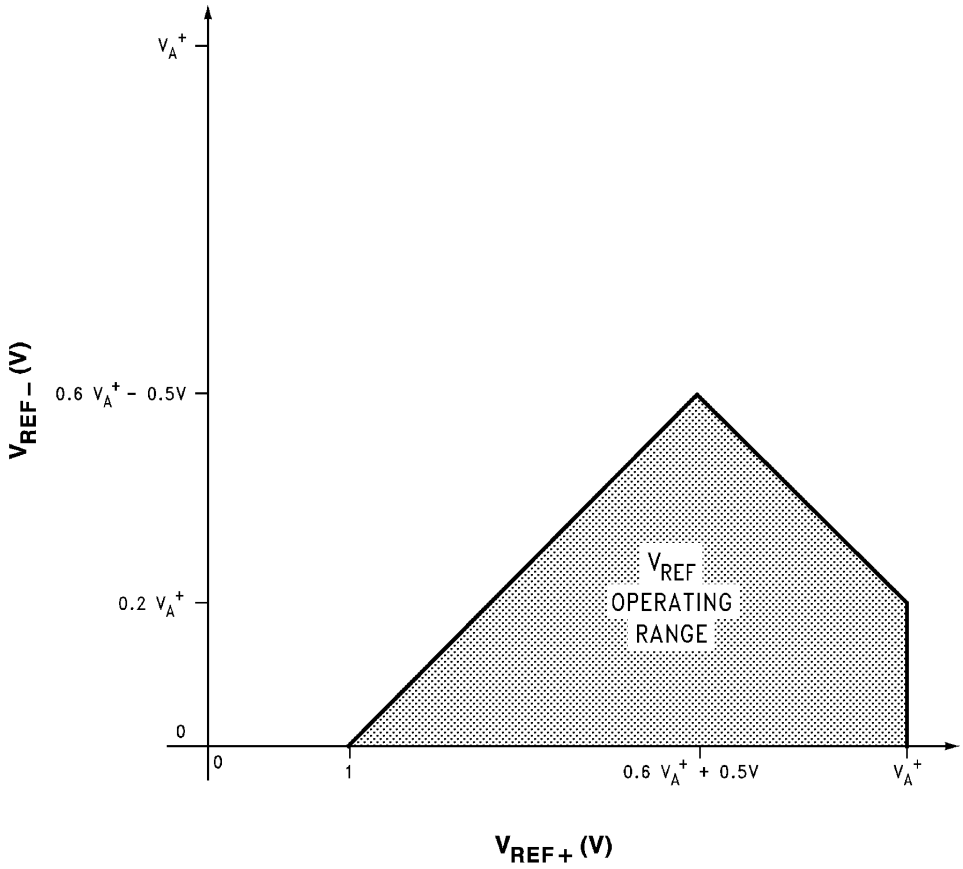


Figure 75. V_{REF} Operating Range

4.0 ANALOG INPUT VOLTAGE RANGE

The ADC12130/2/8's fully differential ADC generate a two's complement output that is found by using the equation shown below:

for (12-bit) resolution the Output Code =

$$\frac{(V_{IN}^+ - V_{IN}^-)\,(4096)}{(V_{REF}^+ - V_{REF}^-)} \quad (1)$$

Round off to the nearest integer value between −4096 to 4095 if the result of the above equation is not a whole number.

Examples are shown in the table below:

V_{REF}^+	V_{REF}^-	V_{IN}^+	V_{IN}^-	Code Output Digital
+2.5V	+1V	+1.5V	0V	0,1111,1111,1111
+4.096V	0V	+3V	0V	0,1011,1011,1000
+4.096V	0V	+2.499V	+2.500V	1,1111,1111,1111
+4.096V	0V	0V	+4.096V	1,0000,0000,0000

5.0 INPUT CURRENT

At the start of the acquisition window (t_A) a charging current flows into or out of the analog input pins (A/DIN1 and A/DIN2) depending upon the input voltage polarity. The analog input pins are CH0–CH7 and COM when A/DIN1 is tied to MUXOUT1 and A/DIN2 is tied to MUXOUT2. The peak value of this input current will depend upon the actual input voltage applied, the source impedance and the internal multiplexer switch on resistance. With MUXOUT1 tied to A/DIN1 and MUXOUT2 tied to A/DIN2 the internal multiplexer switch on resistance is typically 1.6 kΩ. The A/DIN1 and A/DIN2 mux on resistance is typically 750Ω.

6.0 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<600Ω), the input charging current will decay, before the end of the S/H's acquisition time of 2 µs (10 CCLK periods with f_{CK} = 5 MHz), to a value that will not introduce any conversion errors. For high source impedances, the S/H's acquisition time can be increased to 18 or 34 CCLK periods. For less ADC accuracy and/or slower CCLK frequencies the S/H's acquisition time may be decreased to 6 CCLK periods. To determine the number of clock periods (N_c) required for the acquisition time with a specific source impedance for the various resolutions the following equations can be used:

12 Bit + Sign $N_C = [R_S + 2.3] \times f_{CK} \times 0.824$

Where f_{CK} is the conversion clock (CCLK) frequency in MHz and R_S is the external source resistance in kΩ. As an example, operating with a resolution of 12 Bits + sign, a 5 MHz clock frequency and maximum acquisition time of 34 conversion clock periods the ADC's analog inputs can handle a source impedance as high as 6 kΩ. The acquisition time may also be extended to compensate for the settling or response time of external circuitry connected between the MUXOUT and A/DIN pins.

An acquisition starts at a falling edge of SCLK and ends at a rising edge of CCLK (see timing diagrams). If SCLK and CCLK are asynchronous, one extra CCLK clock period may be inserted into the programmed acquisition time for synchronization. Therefore, with asynchronous SCLK and CCLK, the acquisition time will change from conversion to conversion.

7.0 INPUT BYPASS CAPACITANCE

External capacitors (0.01 µF–0.1 µF) can be connected between the analog input pins, CH0–CH7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. These capacitors will not degrade the conversion accuracy.

8.0 NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

9.0 POWER SUPPLIES

Noise spikes on the V_A^+ and V_D^+ supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any power supply spikes that occur during the Auto Zero or linearity correction. The minimum power supply bypassing capacitors recommended are low inductance tantalum capacitors of 10 µF or greater paralleled with 0.1 µF monolithic ceramic capacitors. More or different bypassing may be necessary depending upon the overall system requirements. Separate bypass capacitors should be used for the V_A^+ and V_D^+ supplies and placed as close as possible to these pins.

10.0 GROUNDING

The ADC12130/2/8's performance can be maximized through proper grounding techniques. These include the use of separate analog and digital areas of the board with analog and digital components and traces located only in their respective areas. Bypass capacitors of 0.01 µF and 0.1 µF surface mount capacitors and a 10 µF are recommended at each of the power supply pins for best performance. These capacitors should be located as close to the bypassed pin as practical, especially the smaller value capacitors.

11.0 CLOCK SIGNAL LINE ISOLATION

The ADC12130/2/8's performance is optimized by routing the analog input/output and reference signal conductors as far as possible from the conductors that carry the clock signals to the CCLK and SCLK pins. Maintaining a separation of at least 7 to 10 times the height of the clock trace above its reference plane is recommended.

12.0 THE CALIBRATION CYCLE

A calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize after initial turn-on. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full-scale, offset, and linearity errors down to the specified limits. Full-scale error typically changes ±0.4 LSB over temperature and linearity error changes even less; therefore, it should be necessary to go through the calibration cycle only once after power up if the Power Supply Voltage and the ambient temperature do not change significantly (see the curves in the Typical Performance Characteristics).

13.0 THE Auto Zero CYCLE

To correct for any change in the zero (offset) error of the ADC, the Auto Zero cycle can be used. It may be desirable to do an Auto Zero cycle whenever the ambient temperature or the power supply voltage change significantly. (See the curves, Figure 17 and Figure 19, in the Typical Performance Characteristics.)

14.0 DYNAMIC PERFORMANCE

Many applications require the converter to digitize AC signals, but the standard DC integral and differential nonlinearity specifications will not accurately predict the converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise (S/N), signal-to-noise + distortion ratio or S/(N + D), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the converter's capability.

An ADC's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the ADC's input, and the transform is then performed on the digitized waveform. S/(N + D) and S/N are calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/N are shown in Converter Electrical Characteristics, and spectral plots of S/(N + D) are included in Typical Performance Characteristics.

The ADC's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N + D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N + D) or S/N drops 3 dB).

Effective number of bits can also be useful in describing the ADC's noise and distortion performance. An ideal ADC will have some amount of quantization noise, determined by its resolution, and no distortion, which will yield an optimum S/(N + D) ratio given by the following equation:

$$S/(N + D) = (6.02 \times n + 1.76)\ dB \quad (2)$$

where

- "n" is the ADC's resolution in bits

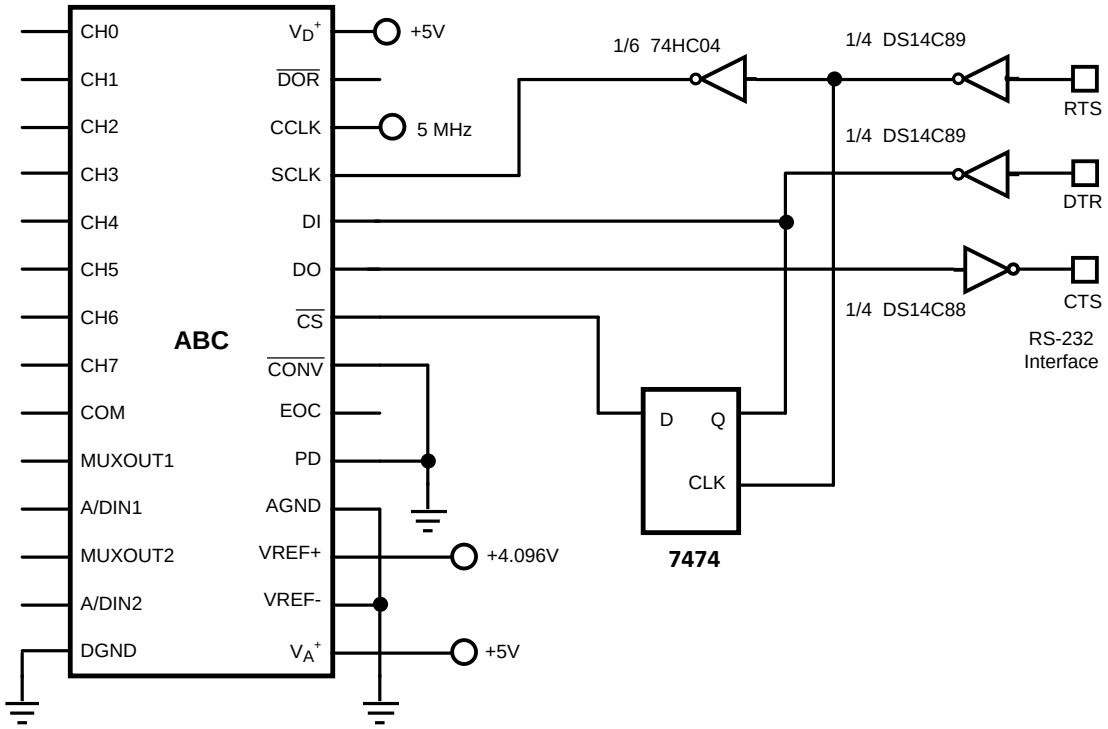
The effective bits of an actual ADC can be found by:

$$n(effective) = ENOB = (S/(N + D) - 1.76) / 6.02 \quad (3)$$

As an example, this device with a differential signed 5V, 1 kHz sine wave input signal will typically have a S/(N + D) of 77 dB, which is equivalent to 12.5 effective bits.

15.0 AN RS232 SERIAL INTERFACE

Shown on the following page is a schematic for an RS232 interface to any IBM and compatible PCs. The DTR, RTS, and CTS RS232 signal lines are buffered via level translators and connected to the ADC12138's DI, SCLK, and DO pins, respectively. The D flip-flop is used to generate the $\overline{CS}$ signal.



Note: V_A^+, V_D^+, and V_{REF}^+ on the ADC12138 each have 0.01 µF and 0.1 µF chip caps, and 10 µF tantalum caps. All logic devices are bypassed with 0.1 µF caps.

Figure 76. RS232 Serial Interface Schematic

The assignment of the RS232 port is shown below

			B7	B6	B5	B4	B3	B2	B1	B0
COM1	Input Address	3FE	X	X	X	CTS	X	X	X	X
	Output Address	3FC	X	X	X	0	X	X	RTS	DTR

A sample program, written in Microsoft QuickBasic, is shown on the next page. The program prompts for data mode select instruction to be sent to the ADC. This can be found from the Mode Programming table shown earlier. The data should be entered in “1”s and “0”s as shown in the table with DI0 first. Next, the program prompts for the number of SCLK cycles required for the programmed mode select instruction. For instance, to send all “0”s to the ADC, selects CH0 as the +input, CH1 as the −input, 12-bit conversion, and 13-bit MSB first data output format (if the sign bit was not turned off by a previous instruction). This would require 13 SCLK periods since the output data format is 13 bits.

The ADC powers up with No Auto Cal, No Auto Zero, 10 CCLK Acquisition Time, 12-bit conversion, data out with sign, power up, 12- or 13-bit MSB First, and user mode. Auto Cal, Auto Zero, Power Up and Power Down instructions do not change these default settings. The following power up sequence should be followed:

1. Run the program
2. Prior to responding to the prompt apply the power to the ADC12138
3. Respond to the program prompts

It is recommended that the first instruction issued to the ADC12138 be Auto Cal (See 1.1 Interface Concepts).

Code Listing:

```
'variables DOL=Data Out word length, DI=Data string for the DI input,
'           DO=ADC result string
'SET CS# HIGH
OUT &H3FC, (&H2 OR INP (&H3FC)                    'set RTS HIGH
OUT &H3FC, (&HFE AND INP(&H3FC)                   'SET DTR LOW
OUT &H3FC, (&HFD AND INP (&H3FC)                  'SET RTS LOW
OUT &H3FC, (&HEF AND INP(&H3FC))                  'set B4 low
10
LINE INPUT “DI data for ADC12138 (see Mode Table on data sheet)”; DI$
INPUT “ADC12138 output word length (12,13,16 or 17)”; DOL
20
'SET CS# HIGH
OUT &H3FC, (&H2 OR INP (&H3FC)                    'set RTS HIGH
OUT &H3FC, (&HFE AND INP(&H3FC)                   'SET DTR LOW
OUT &H3FC, (&HFD AND INP (&H3FC)                  'SET RTS LOW
'SET CS# LOW
OUT &H3FC, (&H2 OR INP (&H3FC)                    'set RTS HIGH
OUT &H3FC, (&H1 OR INP(&H3FC)                     'SET DTR HIGH
OUT &H3FC, (&HFD AND INP (&H3FC)                  'SET RTS LOW
DO$=“ ”                                           'reset DO variable
    OUT &H3FC, (&H1 OR INP(&H3FC)                     'SET DTR HIGH
    OUT &H3FC, (&HFD AND INP(&H3FC))                  'SCLK low
FOR N = 1 TO 8
    Temp$ = MID$(DI$, N, 1)
    IF Temp$=“0” THEN
        OUT &H3FC, (&H1 OR INP(&H3FC))
    ELSE OUT &H3FC, (&HFE AND INP(&H3FC))
    END IF                                        'out DI
    OUT &H3FC, (&H2 OR INP(&H3FC))                'SCLK high
    IF (INP(&H3FE) AND 16) = 16 THEN
        DO$ = DO$ + “0”
        ELSE
        DO$ = DO$ + “1”
    END IF                                        'Input DO
    OUT &H3FC, (&H1 OR INP(&H3FC)                 'SET DTR HIGH
    OUT &H3FC, (&HFD AND INP(&H3FC))              'SCLK low
NEXT N
IF DOL  > 8 THEN
    FOR N=9 TO DOL
    OUT &H3FC, (&H1 OR INP(&H3FC)                 'SET DTR HIGH
    OUT &H3FC, (&HFD AND INP(&H3FC))              'SCLK low
    OUT &H3FC, (&H2 OR INP(&H3FC))                'SCLK high
    IF (INP(&H3FE) AND &H1O) = &H1O THEN
        DO$ = DO$ + “0”
    ELSE
        DO$ = DO$ + “1”
    END IF
    NEXT N
END IF
OUT &H3FC, (&HFA AND INP(&H3FC))              'SCLK low and DI high
FOR N = 1 TO 500
NEXT N
PRINT DO$
INPUT “Enter “C” to convert else “RETURN” to alter DI data”; s$
IF s$ = “C” OR s$ = “c” THEN
GOTO 20
ELSE
GOTO 10
END IF
END
```

REVISION HISTORY

Changes from Revision F (March 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	42

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC12130CIWM/NOPB	Active	Production	SOIC (DW) | 16	45 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12130 CIWM
ADC12130CIWM/NOPB.A	Active	Production	SOIC (DW) | 16	45 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12130 CIWM
ADC12130CIWM/NOPB.B	Active	Production	SOIC (DW) | 16	45 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12130 CIWM
ADC12130CIWMX/NOPB	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12130 CIWM
ADC12130CIWMX/NOPB.A	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12130 CIWM
ADC12130CIWMX/NOPB.B	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12130 CIWM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

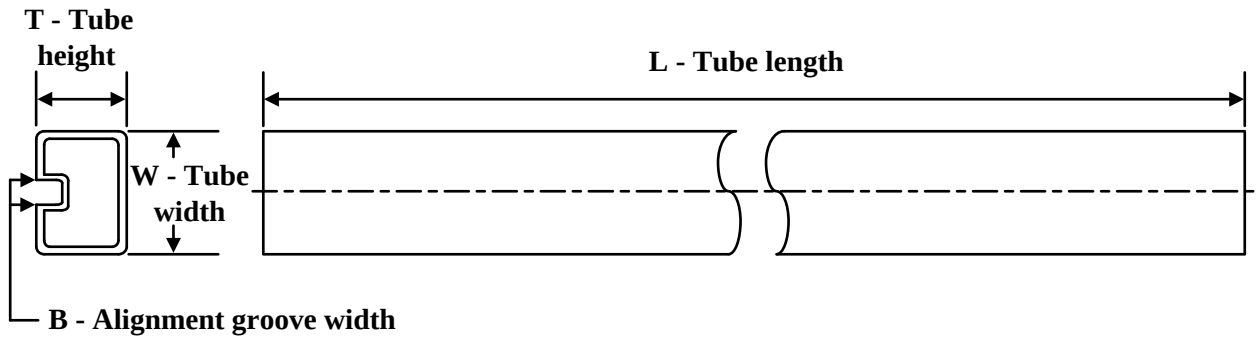
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADC12130CIWM/NOPB	DW	SOIC	16	45	495	15	5842	7.87
ADC12130CIWM/NOPB.A	DW	SOIC	16	45	495	15	5842	7.87
ADC12130CIWM/NOPB.B	DW	SOIC	16	45	495	15	5842	7.87

GENERIC PACKAGE VIEW

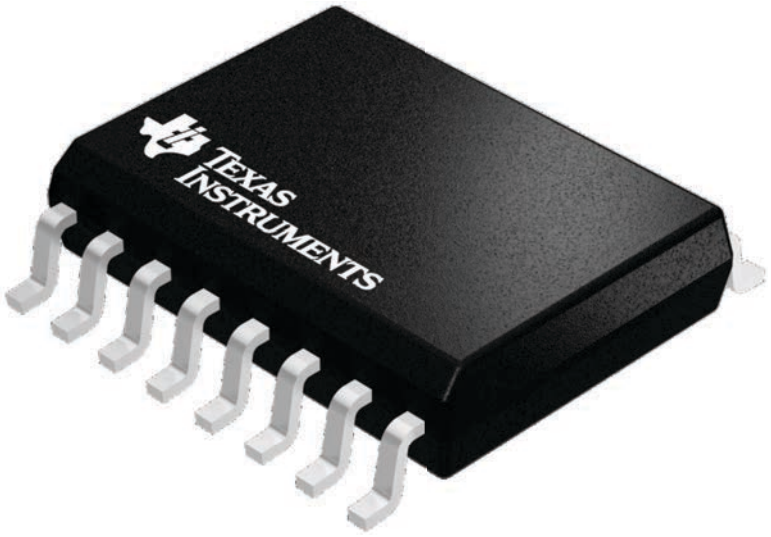
DW 16

SOIC - 2.65 mm max height

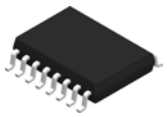
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

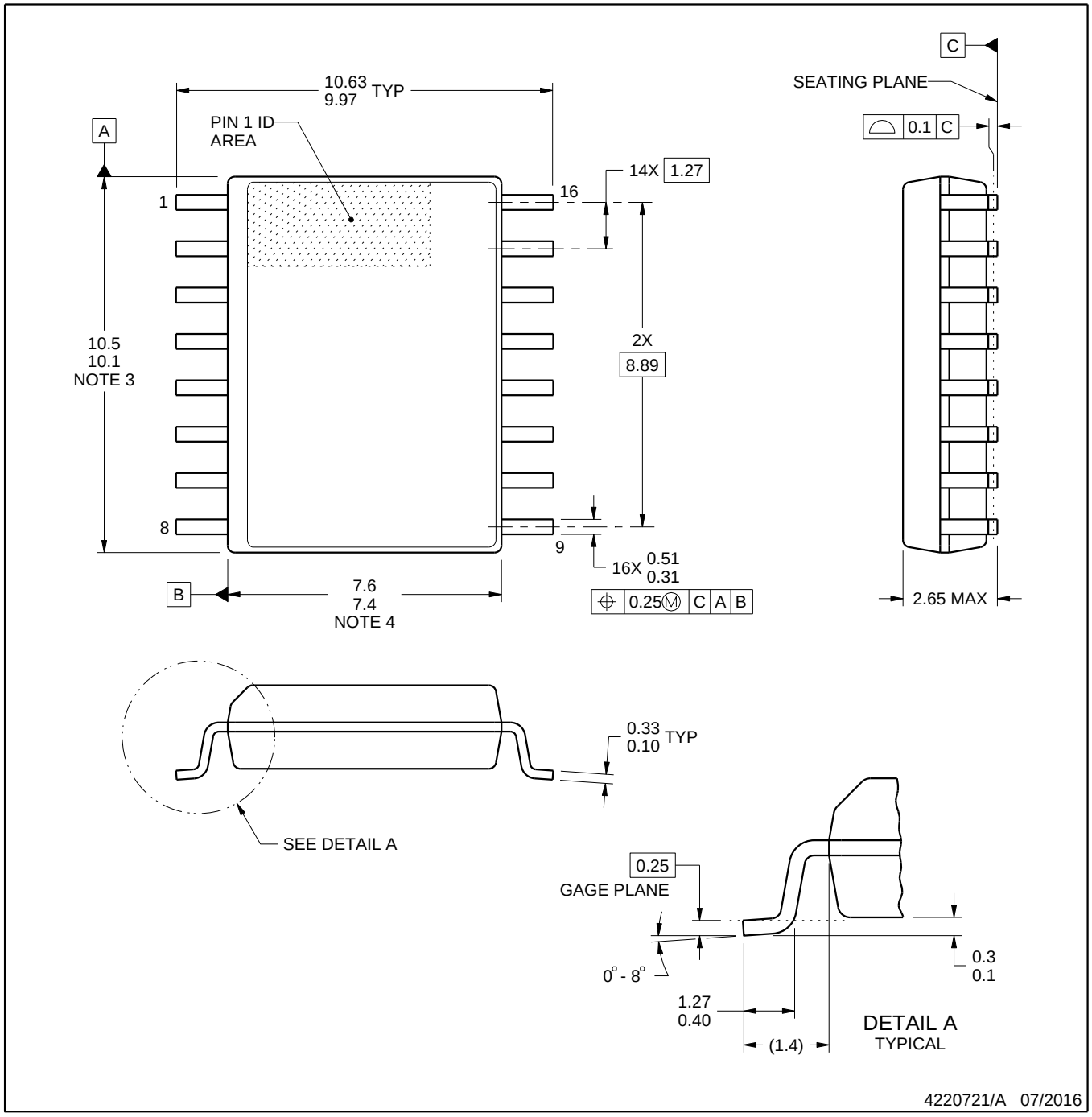


PACKAGE OUTLINE

DW0016A

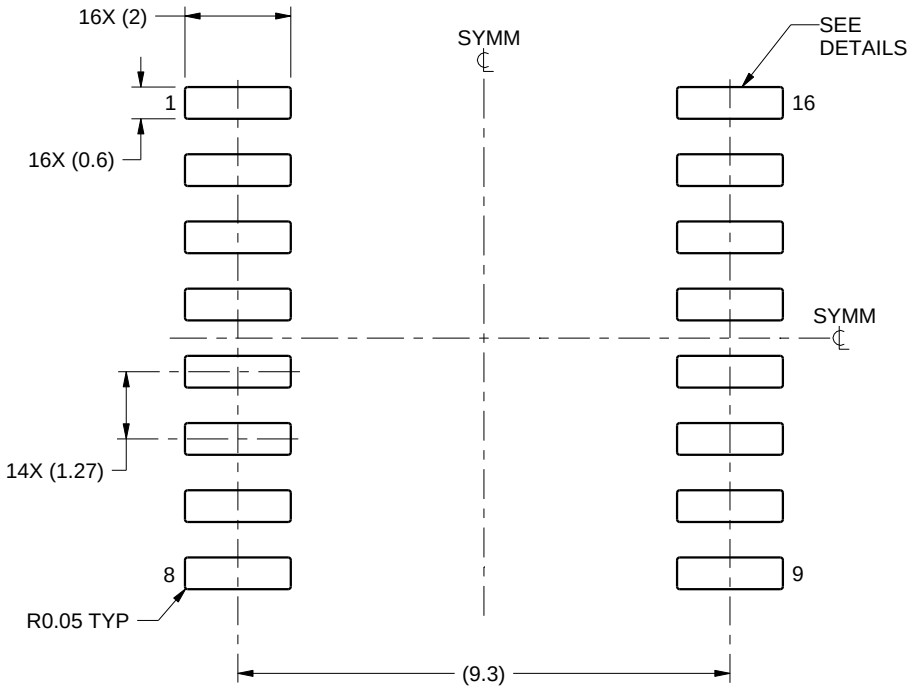
SOIC - 2.65 mm max height

SOIC

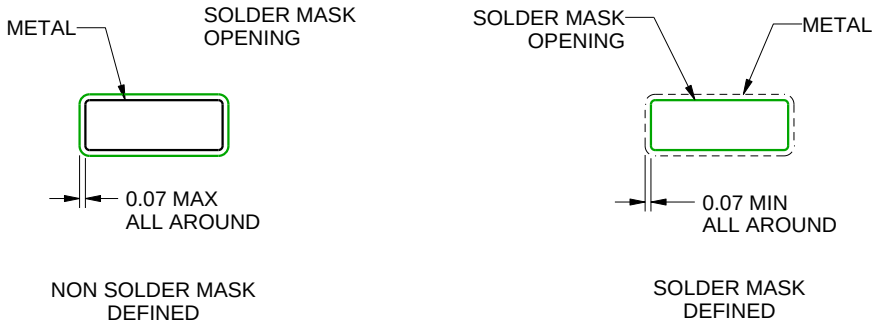


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

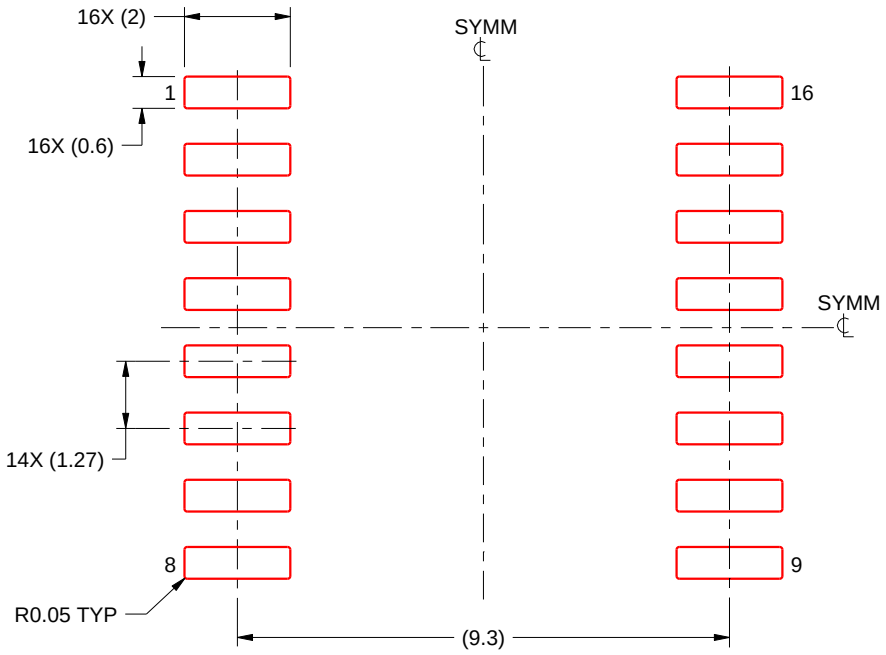


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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