10-Channel Level Shifter and VCOM Buffer

FEATURES

- **10-Channel Level Shifter, Organized as Two Groups of 8 + 2 Channels**
- **Separate Positive Supplies (V_{GH}) for Each Group**
- **V_{GH} Levels up to 38V**
- **V_{GL} Levels down to –13V**
- **Logic Level Inputs**
- **High Peak Output Currents**
- **High-Speed V_{COM} Buffer**
- **28-Pin 5x5 mm QFN Package**

APPLICATIONS

- **Large Format LCD Displays using GIP Technology**

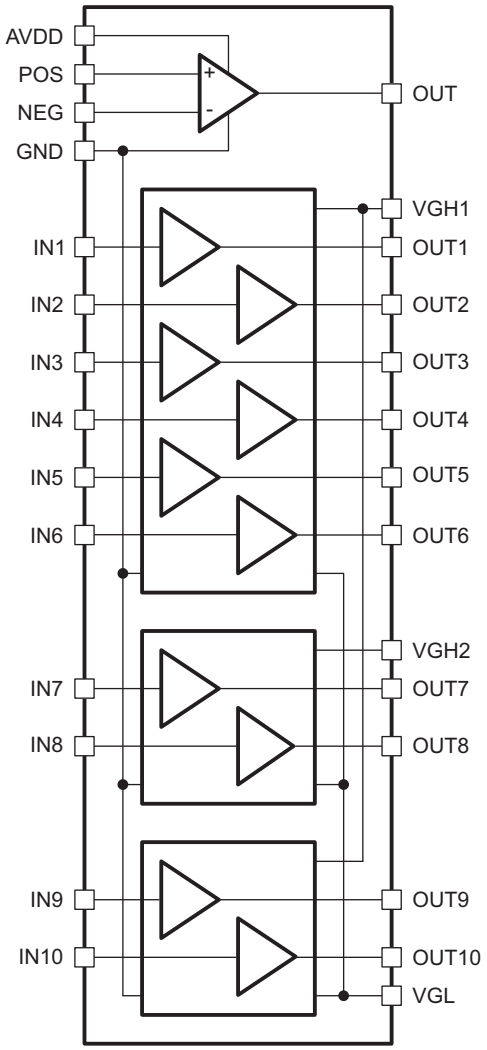
DESCRIPTION

The TPS65190 is a combined multi-channel level-shifter and V_{COM} buffer intended for use in large format LCD display applications such as TVs and monitors. The device converts the logic-level signals generated by the Timing Controller (T-CON) to the high-level gate drive signals used by the display panel and amplifies/buffers an externally generated V_{COM} voltage.

The 10 level shifter channels are organized as 2 groups, each with its own positive supply. Channels 1-6 and 9-10 are supplied by V_{GH1} and channels 7-8 are supplied by V_{GH2}. The two positive supplies can be tied together if one positive supply voltage is used for all level shifter channels. Both level shifter groups use the same negative supply V_{GL}.

The level-shifters feature low impedance output stages that achieve fast rise and fall times even when driving significant capacitive loads.

The uncommitted high-speed operational amplifier features a high slew rate and high peak current capability that make it particularly suitable for driving the panel's common rail (V_{COM}).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	ORDERING	PACKAGE	PACKAGE MARKING
–40 to 85°C	TPS65190RHDR	28-Pin QFN	TPS65190

(1) The device is supplied taped and reeled, with 3000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
	Voltage on VGH1, VGH2(2)	45	V
	Voltage on VGL(2)	–15	V
	Voltage on AVDD(2)	20	V
	Voltage on IN1 through IN10 (2)	–0.3 to 7.0	V
	Voltage on POS, NEG(2)	–0.3 to V_{AVDD} + 0.3	V
	Differential voltage between POS and NEG	$\pm V_{AVDD}$	V
	ESD Rating HBM	2	kV
	ESD Rating MM	200	V
	ESD Rating CDM	700	V
	Continuous power dissipation	See Dissipation Rating Table	
T_A	Operating ambient temperature range	–40 to 85	°C
T_J	Operating junction temperature range	–40 to 150	°C
T_{STG}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the GND pin

DISSIPATION RATINGS

PACKAGE	θ_{JA}	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
28-Pin QFN(1)	35 °C/W	3.57 W	2.29 W	1.86 W

(1) Refer to application section on how to improve thermal resistance θ_{JA}.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{GH1}	Positive supply voltage range	12	30	38	V
V_{GH2}		12	30	38	
V_{GL}	Negative supply voltage range	–2	–6.2	-13	V
V_{IN}	Level shifter input voltage range	3	3.3	5	V
V_{AVDD}	Operational amplifier positive supply voltage range	8	15	20	V
V_{POS}, V_{NEG}	Operational amplifier common-mode input voltage range	1	0.5 x V_{AVDD}	V_{AVDD}-1	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

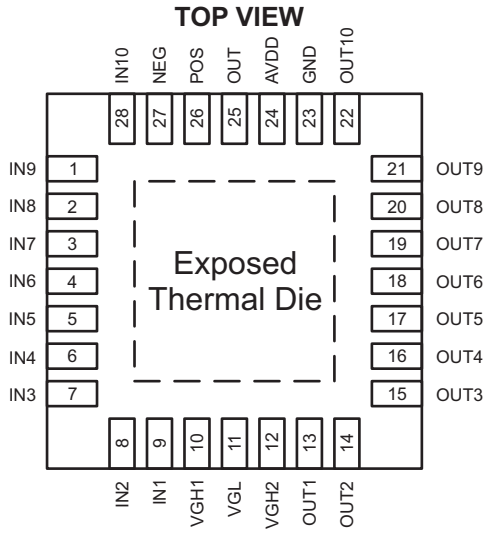
V_{GH1} = V_{GH2} = 30 V; V_{GL} = –6.2 V; V_{AVDD} = 15 V; T_A = –40 °C to 85 °C; typical values are at 25 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LEVEL SHIFTER						
I_{GH1}	V_{GH1} Supply current	IN1 to IN10 = GND		0.18	1	mA
I_{GH2}	V_{GH2} Supply current	IN1 to IN10 = GND		0.012	0.1	mA
I_{GL}	V_{GL} Supply current	IN1 to IN10 = GND		0.015	0.1	mA
I_{OUTX}	Peak output current	Channels 1-8, sourcing		490		mA
		Channels 1-8, sinking		850		
		Channels 9-10, sourcing		250		
		Channels 9-10, sinking		450		
I_{INX}	Input current	Channels 1-10, inputs connected to GND		-0.003	±1	µA
		Channels 1-10, inputs connected to 3.3 V		-0.002	±1	
V_{IH}	High level input threshold	Channels 1 through 10			2.0	V
V_{IL}	Low level input threshold	Channels 1 through 10	0.5			V
V_{DROPH}	Output voltage drop high	Channels 1 through 8, I_{OUT} = 10 mA		0.19	0.4	V
		Channels 9 and 10, I_{LOAD} = 10 mA		0.36	1	
V_{DROPL}	Output voltage drop low	Channels 1 through 8, I_{OUT} = –10 mA		0.06	0.4	V
		Channels 9 and 10, I_{OUT} = –10 mA		0.11	1	
t_R	Rise time	Channels 1 through 8. C_{OUT} = 4.7 nF (1)		404	600	ns
		Channels 9 and 10. C_{OUT} = 4.7 nF (1)		740	950	
t_F	Fall time	Channels 1 through 8. C_{OUT} = 4.7 nF (1)		192	370	ns
		Channels 9 and 10. C_{OUT} = 4.7 nF (1)		377	700	
t_{PH}	Propagation delay	Rising edge, C_{OUT} = 150 pF		27		ns
t_{PL}		Falling edge, C_{OUT} = 150 pF		40		
OPERATIONAL AMPLIFIER						
I_{AVDD}	Supply current	V_{CM} = 7.5 V, unity gain, no load		5.4		mA
V_{OS}	Input offset voltage	V_{CM} = 7.5 V		1	±20	mV
I_{IB}	Input bias current	V_{CM} = 7.5 V		0.001	±0.1	µA
V_{CM}	Common-mode input voltage range	V_{AVDD} = 8 V to 20 V	1		V_{AVDD} –1	V
CMRR	Common mode rejection ratio	V_{CM} = 1 V to 14 V, 1 Hz, no load		93		dB
A_{VOL}	Open loop gain	V_{OUT} = 0.5 V to 14.5 V, no load		88		dB
V_{DROPL}	Output voltage drop low	I_O = –10 mA		52	200	mV
V_{DROPH}	Output voltage drop high	I_O = 10 mA		85	200	mV
PSRR	Power supply rejection ratio	Measured at 1 Hz		90		dB
BW	Small signal unity gain bandwidth	–3 dB, V_{IN} = 100 mV_{PP}		76		MHz
SR	Slew rate, rising	A_V = 1, V_{CM}=7.5 V, V_{IN} = 2 V_{PP}		66		V/µs
	Slew rate, falling			53		
I_O	Output current	Peak. V_{CM} = 7.5 V	±200	±450		mA
		V_{OUT} = 13 V, sourcing	100	225		
		V_{OUT} = 2 V, sinking	–100	317		
I_{SC}	Short circuit current	OUT shorted to GND or AVDD (2)	±250	±498	±900	mA

(1) Rise and fall times are measured between 10% and 90% of the waveform's maximum amplitude.
(2) To prevent overheating, short-circuit conditions must not be allowed to persist indefinitely. The maximum allowable duration of short-circuit conditions will be determined by the IC's junction-to-ambient thermal resistance (θ_{JA}) and the ambient temperature of the application.

DEVICE INFORMATION

PIN ASSIGNMENT



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
IN9	1	I	Level shifter channel 9 input
IN8	2	I	Level shifter channel 8 input
IN7	3	I	Level shifter channel 7 input
IN6	4	I	Level shifter channel 6 input
IN5	5	I	Level shifter channel 5 input
IN4	6	I	Level shifter channel 4 input
IN3	7	I	Level shifter channel 3 input
IN2	8	I	Level shifter channel 2 input
IN1	9	I	Level shifter channel 1 input
VGH1	10	P	Positive supply for level shifter channels 1-6 and 9-10
VGL	11	P	Negative supply voltage for all level shifter channels
VGH2	12	P	Positive supply for level shifter channels 7-8
OUT1	13	O	Level shifter channel 1 output
OUT2	14	O	Level shifter channel 2 output
OUT3	15	O	Level shifter channel 3 output
OUT4	16	O	Level shifter channel 4 output
OUT5	17	O	Level shifter channel 5 output
OUT6	18	O	Level shifter channel 6 output
OUT7	19	O	Level shifter channel 7 output
OUT8	20	O	Level shifter channel 8 output
OUT9	21	O	Level shifter channel 9 output
OUT10	22	O	Level shifter channel 10 output
GND	23	P	Ground connection for level shifter and operational amplifier.
AVDD	24	P	Operational amplifier positive supply
OUT	25	O	Operational amplifier output
NEG	26	I	Operational amplifier inverting input
POS	27	I	Operational amplifier non-inverting input

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
IN10	28	I	Level shifter channel 10 input
Exposed Thermal Die		P	Connect to the system V_{GL} connection.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

LEVEL SHIFTER		
Rise time	Channels 1-8, C_{OUT} = 8 pF	Figure 1
	Channels 1-8, C_{OUT} = 4.7 nF	Figure 2
	Channels 9-10, C_{OUT} = 8 pF	Figure 3
	Channels 9-10, C_{OUT} = 4.7 nF	Figure 4
Fall time	Channels 1-8, C_{OUT} = 8 pF	Figure 5
	Channels 1-8, C_{OUT} = 4.7 nF	Figure 6
	Channels 9-10, C_{OUT} = 8 pF	Figure 7
	Channels 9-10, C_{OUT} = 4.7 nF	Figure 8
Propagation delay, channels 1 to 8	Channels 1-8, rising, C_{OUT} = 8 pF	Figure 9
	Channels 1-8, falling, C_{OUT} = 8 pF	Figure 10
	Channels 9-10, rising, C_{OUT} = 8 pF	Figure 11
	Channels 9-10, falling, C_{OUT} = 8 pF	Figure 12
Peak output current	Channels 1-8, C_{OUT} = 10 nF	Figure 13
	Channels 9-10, C_{OUT} = 10 nF	Figure 14
Output voltage drop	Output low	Figure 15
	Output high	Figure 16
OPERATIONAL AMPLIFIER		
Small signal frequency response	V_{CM} = 7.5 V, V_{IN} = 100 mV_{PP}	Figure 17
Output voltage drop		Figure 18
Slew rate	Output rising, C_{OUT} = 150 pF	Figure 19
	Output falling, C_{OUT} = 150 pF	Figure 20

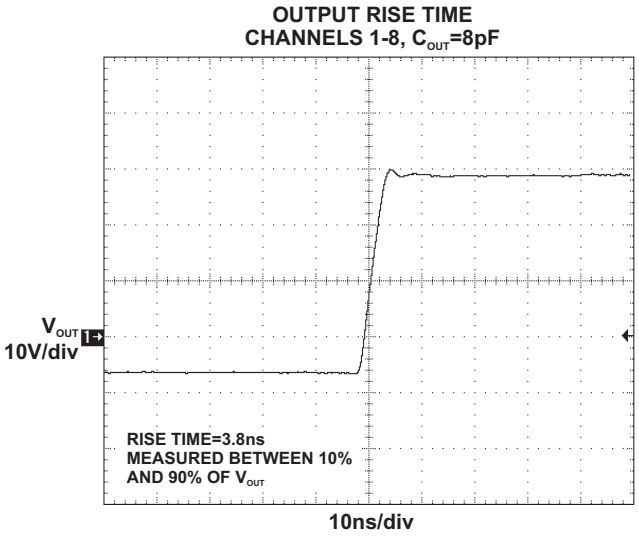


Figure 1.

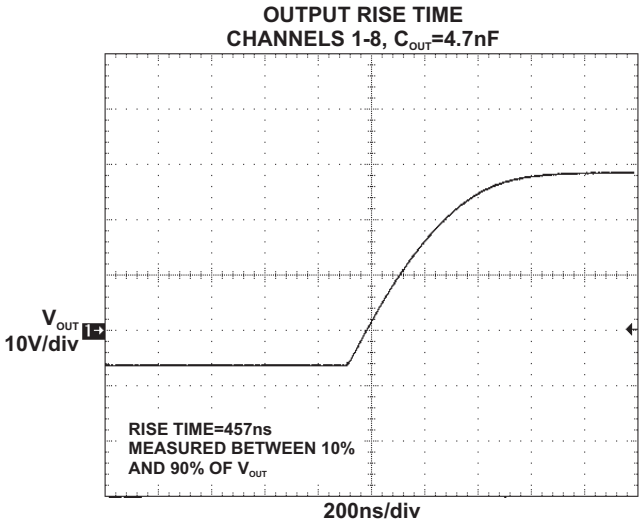


Figure 2.

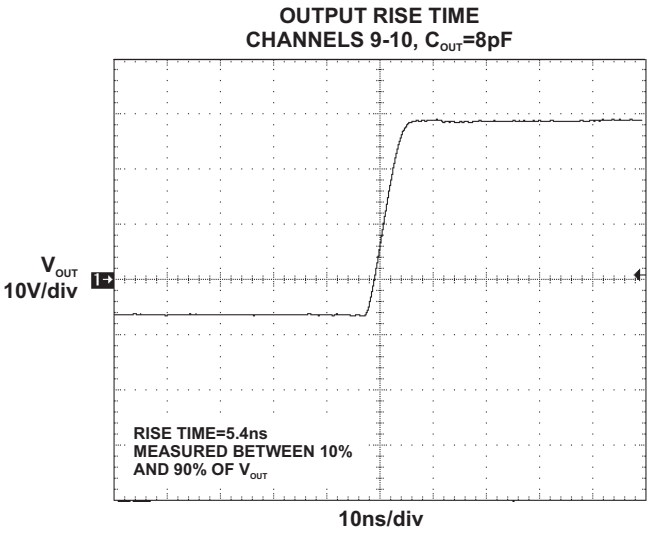


Figure 3.

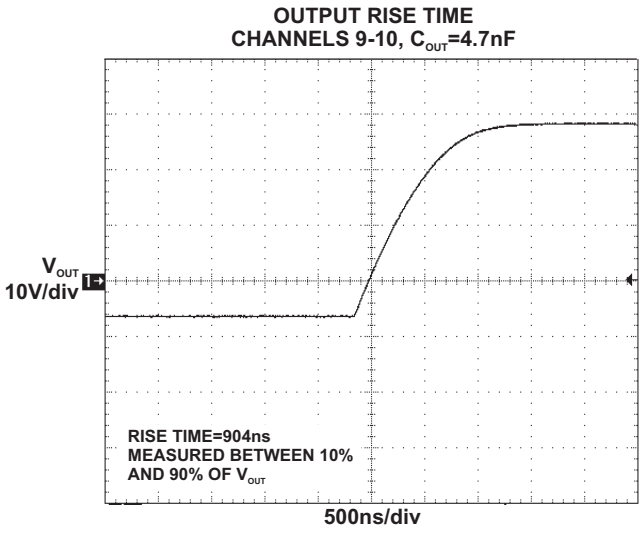


Figure 4.

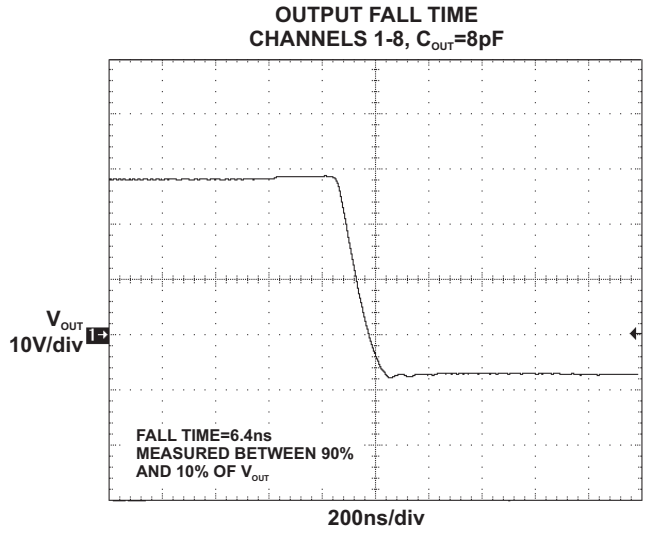


Figure 5.

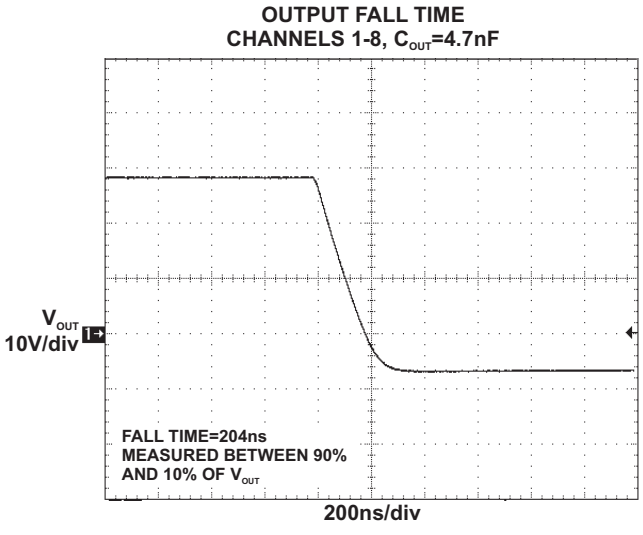


Figure 6.

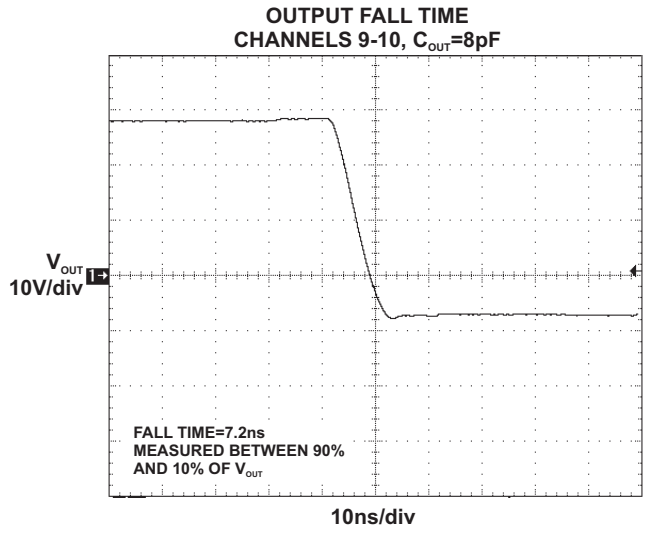


Figure 7.

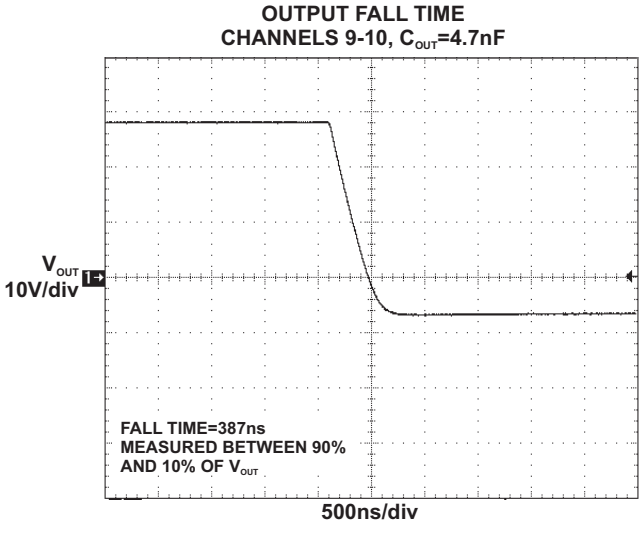


Figure 8.

PROPAGATION DELAY – RISING
IN-OUT, CHANNELS 1-8, C_{OUT}=8pF

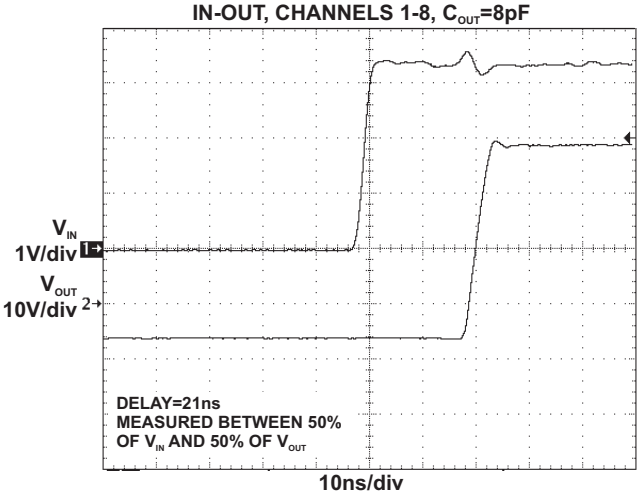


Figure 9.

PROPAGATION DELAY – FALLING
IN-OUT, CHANNELS 1-8, C_{OUT}=8pF

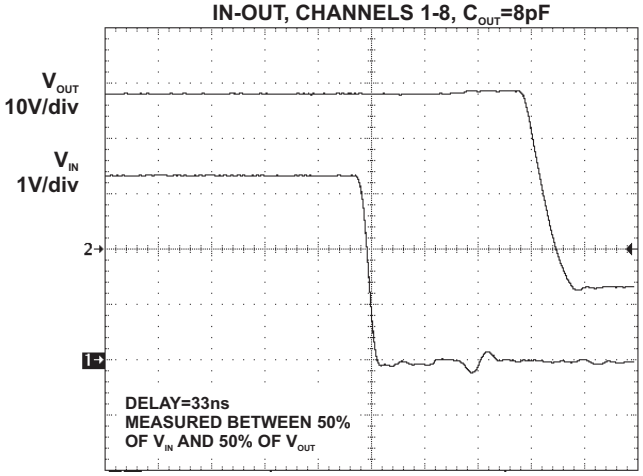


Figure 10.

PROPAGATION DELAY – RISING
IN-OUT, CHANNELS 9-10, C_{OUT}=8pF

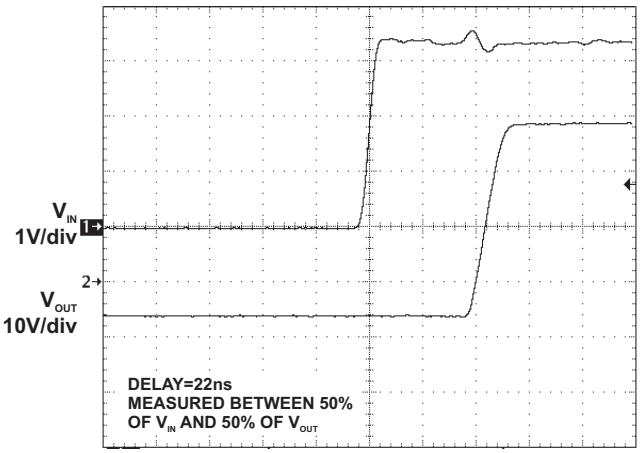


Figure 11.

PROPAGATION DELAY – FALLING
IN-OUT, CHANNELS 9-10, C_{OUT}=8pF

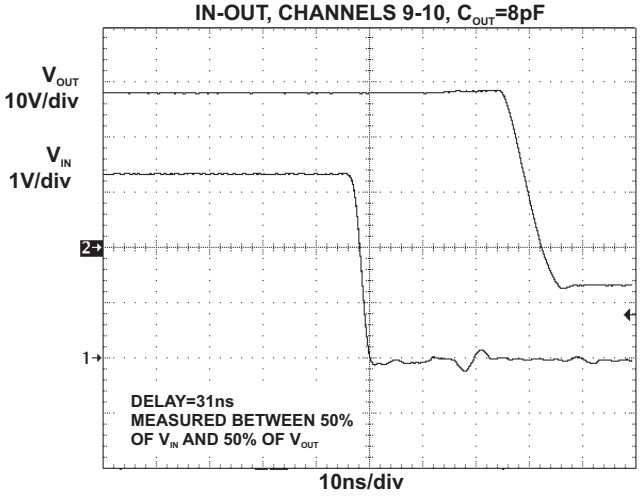


Figure 12.

PEAK OUTPUT CURRENT
CHANNELS 1-8, C_{OUT}=10nF

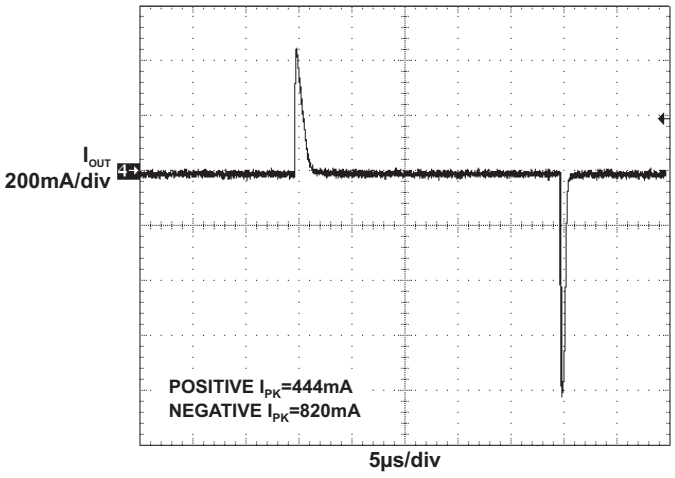


Figure 13.

PEAK OUTPUT CURRENT
CHANNELS 9-10, C_{OUT}=10nF

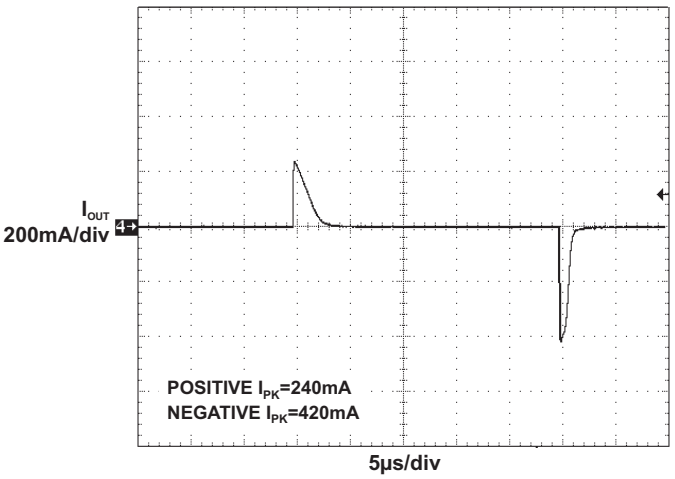


Figure 14.

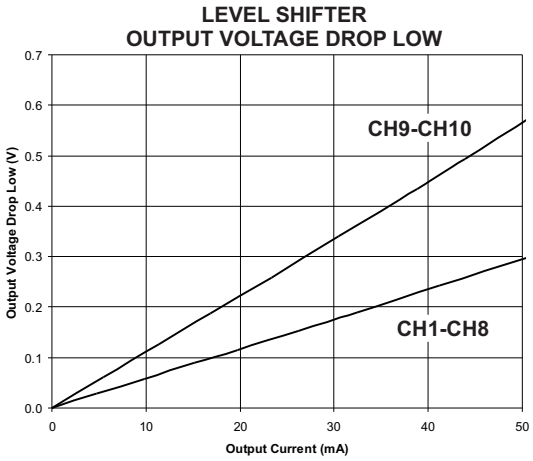


Figure 15.

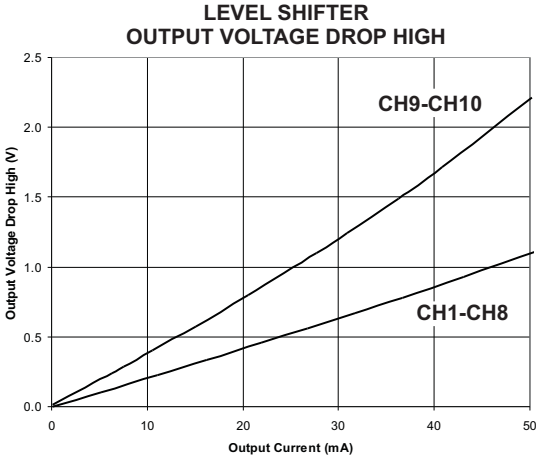


Figure 16.

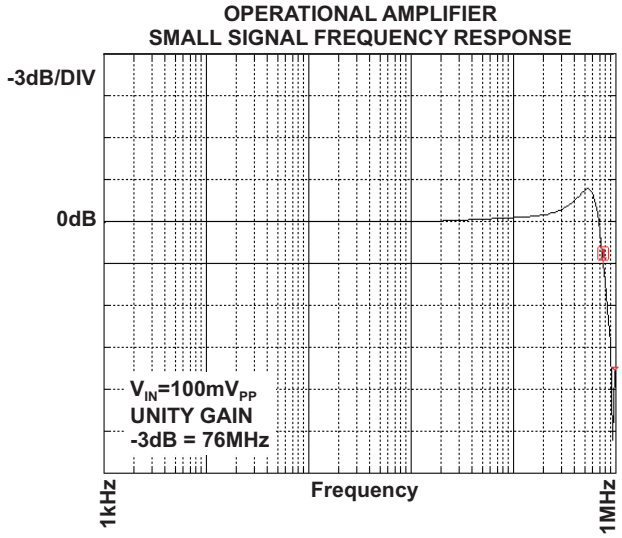


Figure 17.

OPERATIONAL AMPLIFIER
OUTPUT VOLTAGE DROP

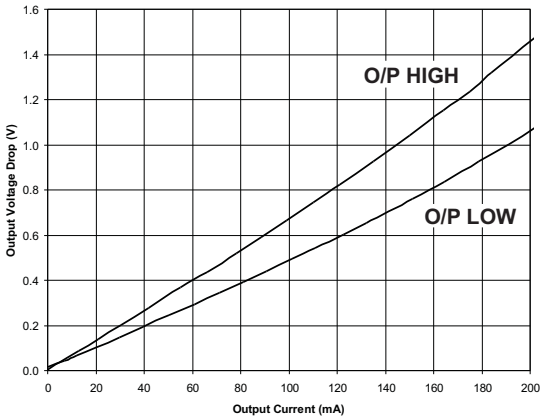


Figure 18.

OPERATIONAL AMPLIFIER
POSITIVE SLEW RATE, C_{OUT}=150pF

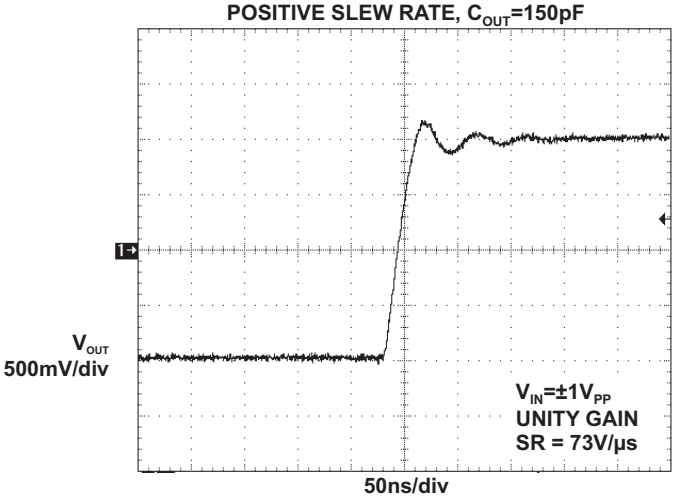


Figure 19.

OPERATIONAL AMPLIFIER
NEGATIVE SLEW RATE, C_{OUT}=150pF

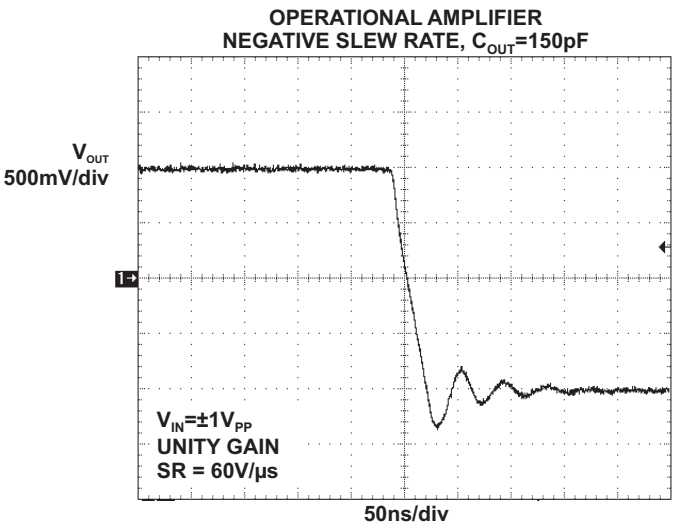


Figure 20.

DETAILED DESCRIPTION

The TPS65190 contains 10 level shifter channels and one high-speed operational amplifier.

The 10 level shifter channels are organized in two groups: the first group, comprising channels 1-6 and 9-10 is powered from V_{VGH1} and V_{GL}; the second group, comprising channels 7 and 8 is powered from V_{GH2} and V_{GL}. Channels 1 to 8 are optimized for high speed operation while channels 9 and 10 operate a little slower.

All level shifter channels feature the same input circuitry and are compatible with the standard logic-level signals generated by timing controllers in typical applications. The output circuitry has been designed to achieve high rise and fall times when driving the capacitive loads typically encountered in LCD display applications

The input and output stages of the operational amplifier extend close to both supply rails and the output stage has been optimized to supply the fast transient currents typical in V_{COM} applications.

APPLICATION INFORMATION

It is recommended to use high quality ceramic capacitors to decouple each supply pin. In typical applications 10 µF is recommended for V_{GH1} and V_{GL}, while 1 µF is normally sufficient for V_{GH2}.

Use level shifter channels 1 to 8 for high-speed clock signals and use channels 9 to 10 for lower-speed signals (see Figure 14). The inputs of any unused level shifter channels should be tied to GND. The outputs of any unused level shifter channels should be left floating.

It is recommended to use low-value feedback resistors with the VCOM buffer to minimize the effects of stray capacitance at its inverting input. Using high value feedback resistors can cause excessive peaking in the amplifier's gain response (caused by pole formed by the feedback resistor and the stray capacitance). If the VCOM buffer is used in a unity gain configuration, the flattest gain response is achieved using a direct connection between the amplifier's output and inverting input.

If the VCOM buffer is not used, tie AVDD, its inverting and non-inverting inputs, and its output to GND.

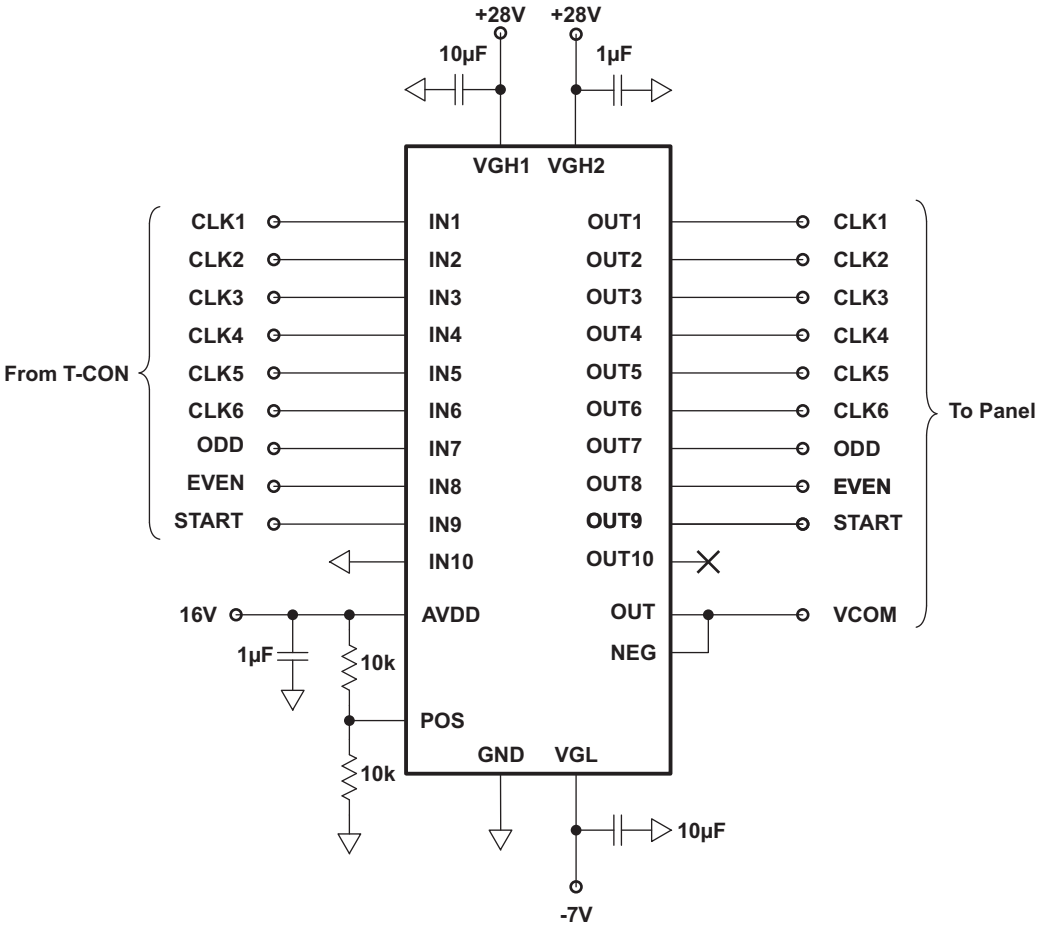


Figure 21. Typical Application Circuit

PCB LAYOUT

Proper PCB layout is essential if the TPS65190's specified performance is to be achieved, and the following basic steps should be followed as a minimum:

1. Use high quality ceramic decoupling capacitors, placed as close as possible to the IC pins they are decoupling
2. Use short, wide tracks to route power to the IC
3. Ensure that the PCB's thermal design is adequate to dissipate power away from the IC

The TPS65190 is supplied in a 28-Pin QFN thermally enhanced package designed to eliminate the use of bulky heat sinks and slugs. In order to benefit from these superior thermal properties PCB layout and manufacturing should follow the guidelines contained in the following application reports, available for free download from http://www.ti.com.

- Application Report – QFN Layout Guidelines (SLOA122)
- Application Report – QFN/SON PCB Attachment (SLUA271A)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65190RHDR	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65190
TPS65190RHDR.A	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65190
TPS65190RHDRG4	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65190
TPS65190RHDRG4.A	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65190

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

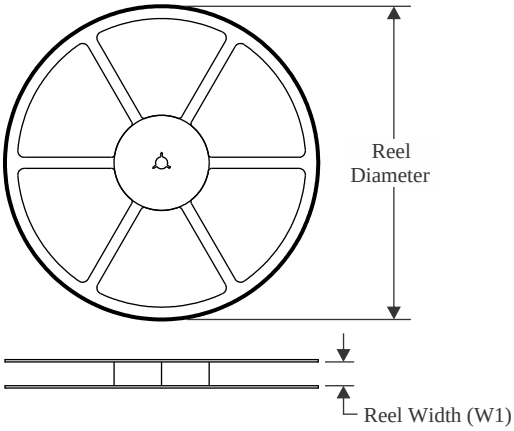
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

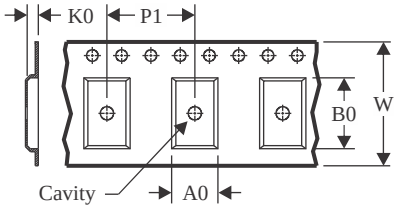
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

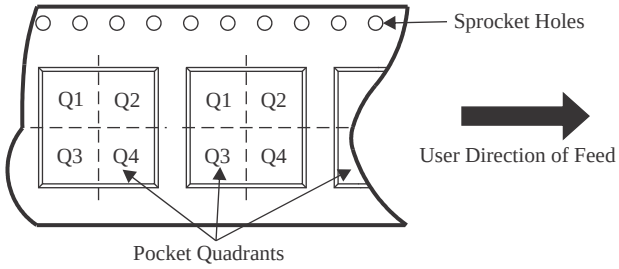


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

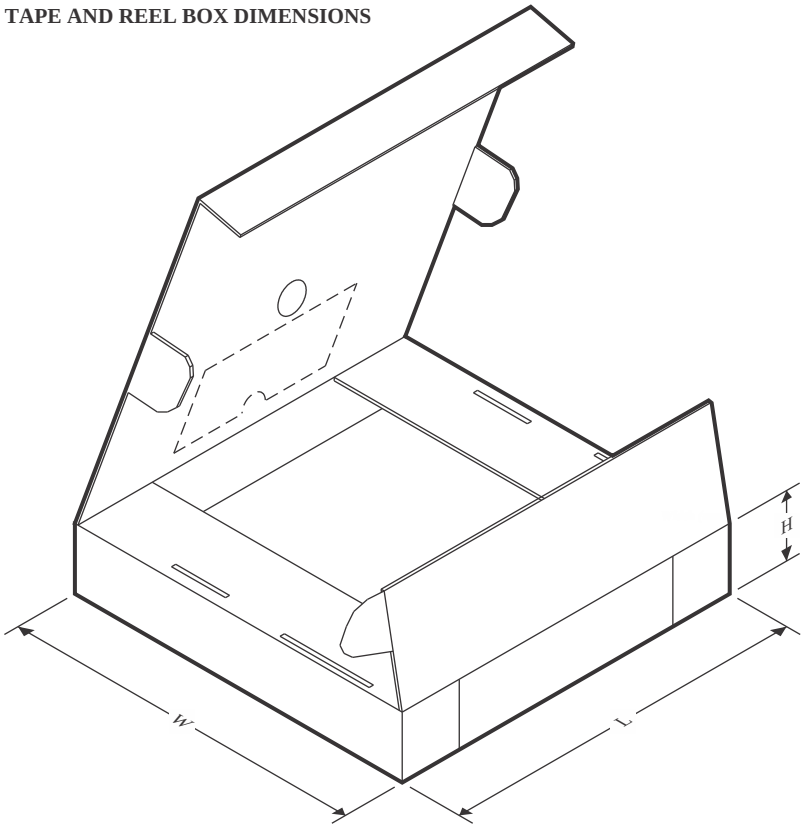
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65190RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS65190RHDRG4	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65190RHDR	VQFN	RHD	28	3000	353.0	353.0	32.0
TPS65190RHDRG4	VQFN	RHD	28	3000	353.0	353.0	32.0

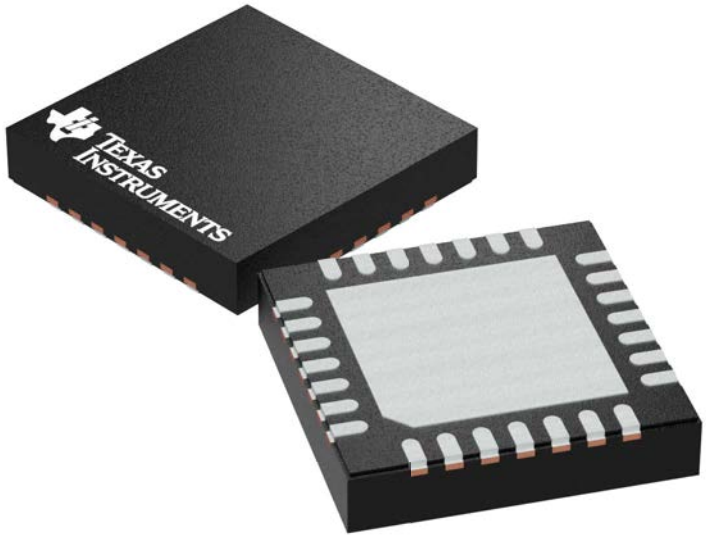
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

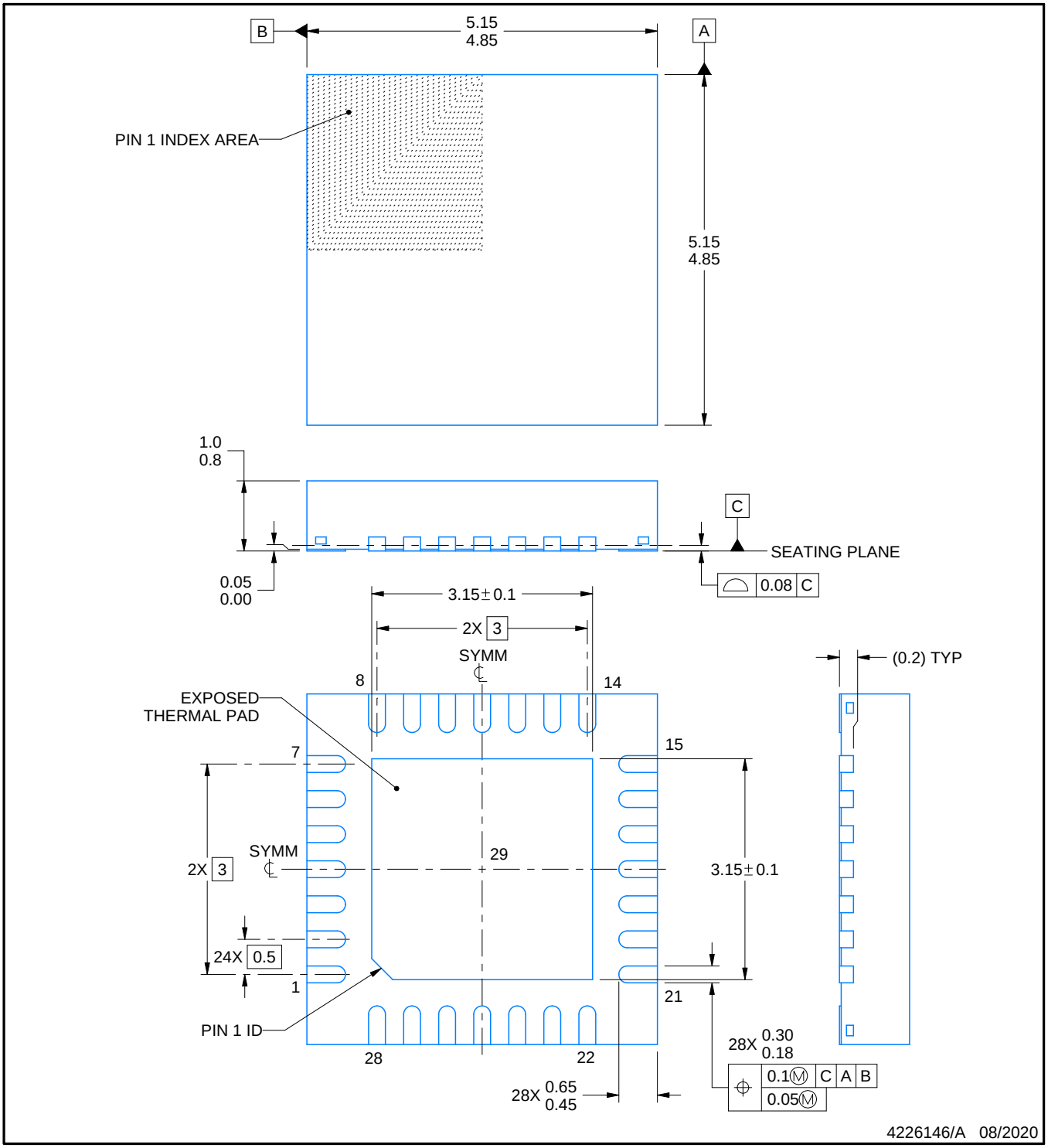
4204400/G

RHD0028B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

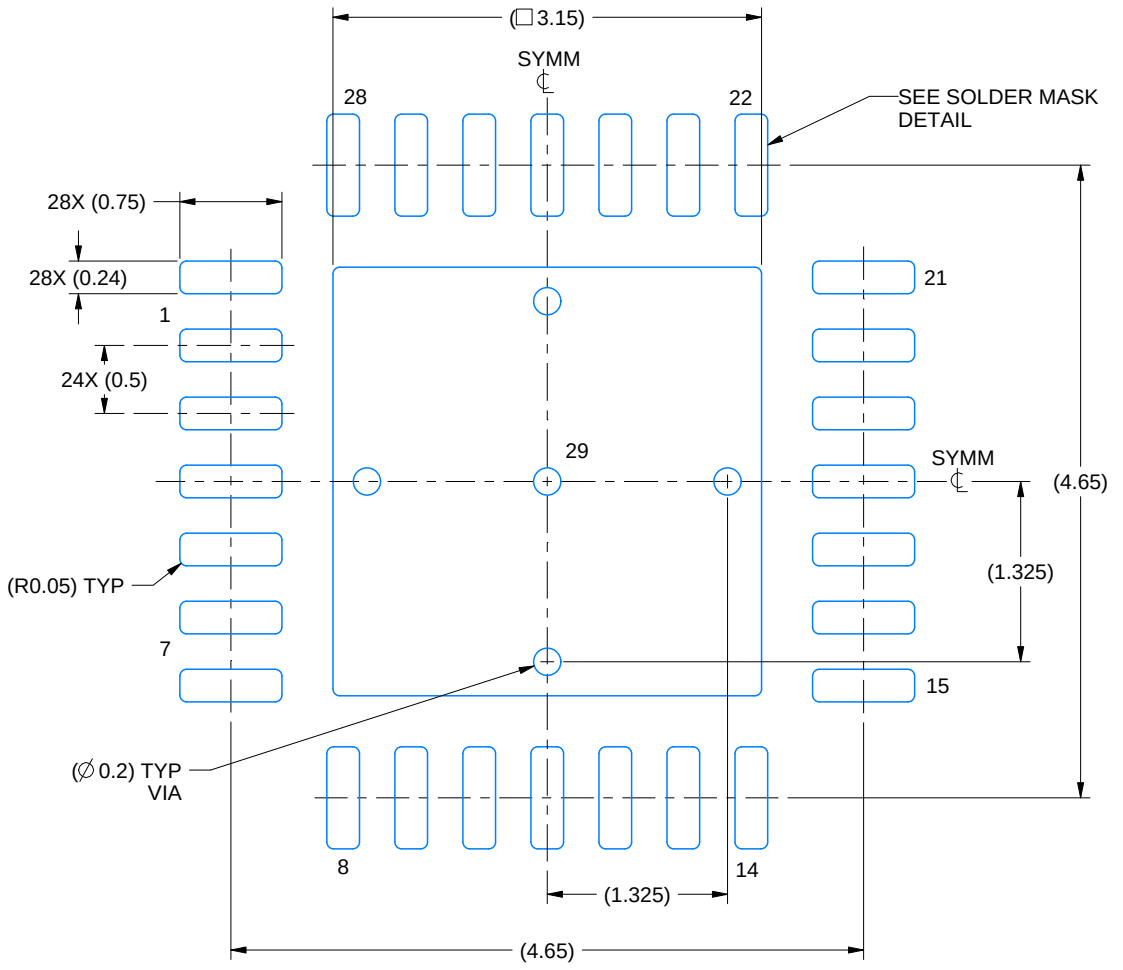
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

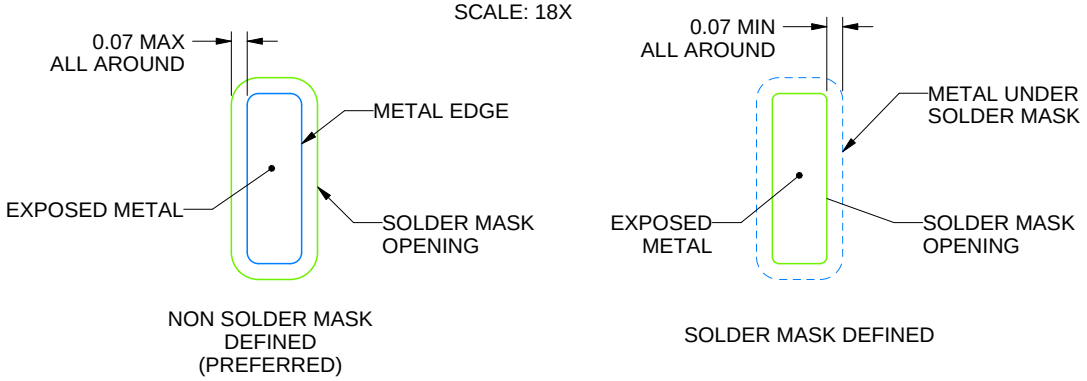
RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

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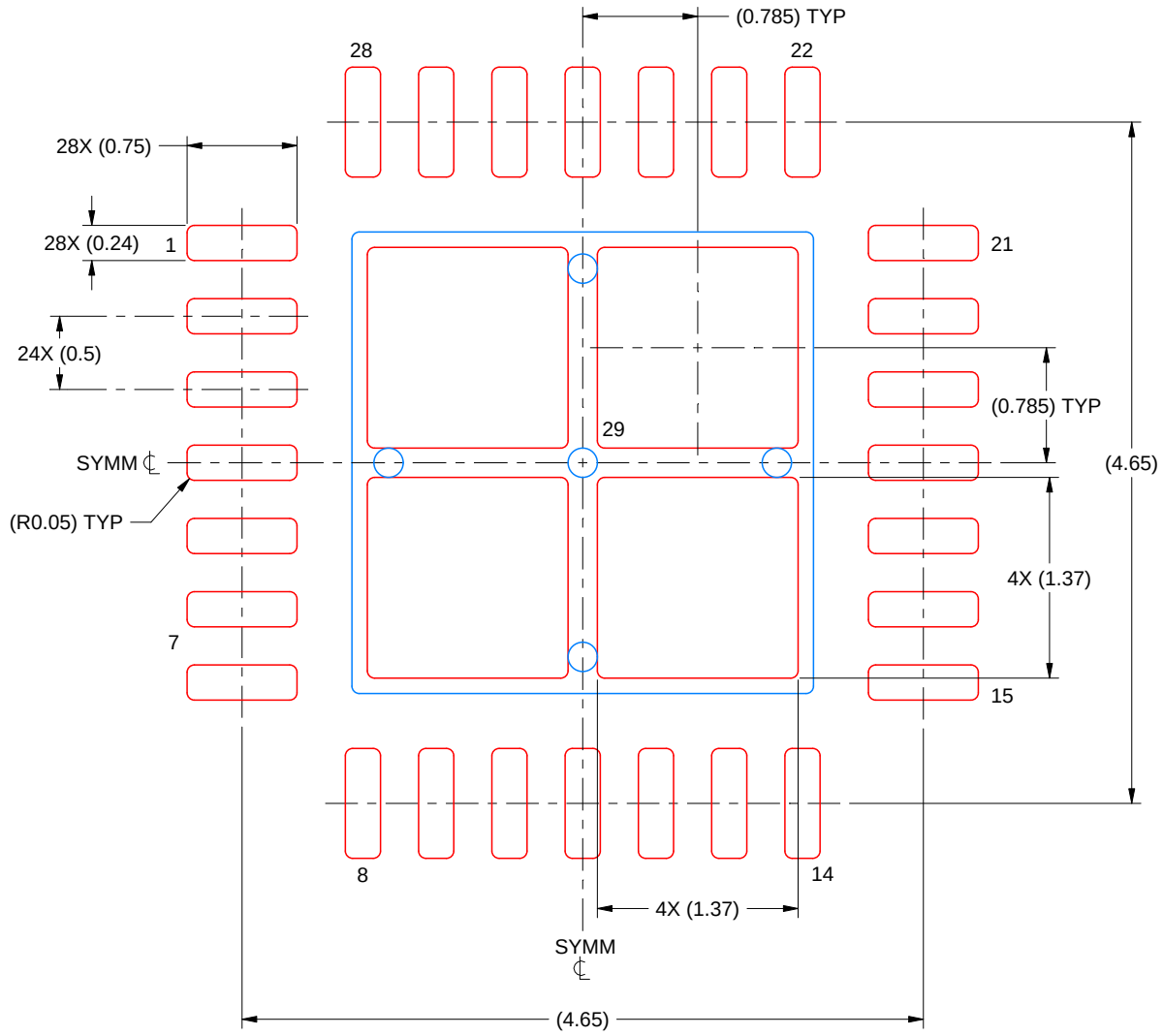
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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