DLP473TE 0.47-Inch 4K UHD Digital Micromirror Device

1 Features

- 0.47-inch diagonal micromirror array
  - 4K UHD (3840 × 2160) display resolution
  - 5.4µm micromirror pitch
  - ±14.5° micromirror tilt (relative to flat surface)
  - Corner illumination
- SubLVDS input data bus
- Supports 4K UHD at 60Hz
- Supports 1080p up to 240Hz
- RGB laser, LED and Laser Phosphor operation supported by DLPC8455 display controller

2 Applications

- Smart projector
- Enterprise projector
- Laser TV
- Gaming projectors
- Home theaters
- Golf simulators

3 Description

The DLP473TE digital micromirror device (DMD) is a digitally controlled micro-electromechanical system (MEMS) spatial light modulator (SLM) that enables bright 4K UHD display systems. The TI DLP® Products 0.47-inch 4K UHD chipset is composed of the DMD and DLPC8455 display controller, the DLPA3082 PMIC, and the DLPA100 color wheel driver. The compact physical size of the chipset provides a complete system solution that enables small form factor 4K UHD displays.

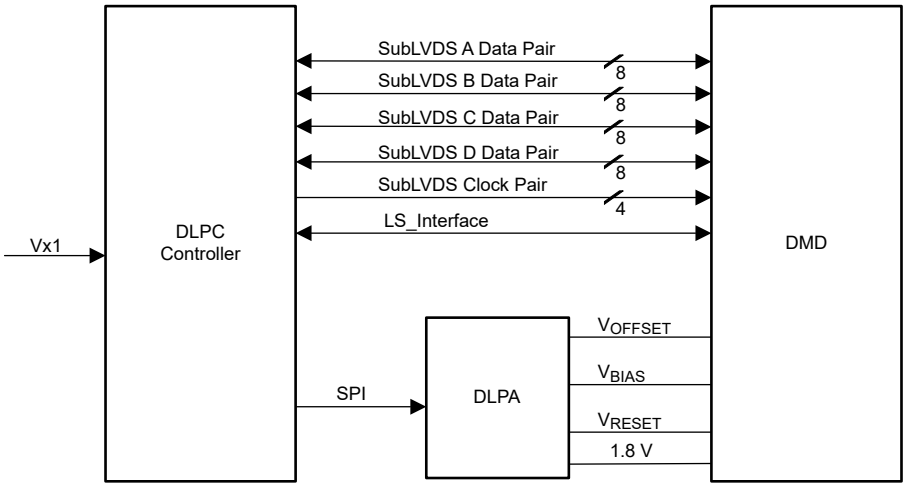
The DMD ecosystem includes established resources to help the user accelerate the design cycle, visit the DLP® Products third-party search tools to find approved optical module manufacturers and third-party providers.

Visit the Getting Started with TI DLP display technology page to learn more about how to start designing with the DMD.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE
DLP473TE	FXL (173)	32.2mm × 22.3mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.



Simplified Application

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4 Pin Configuration and Functions

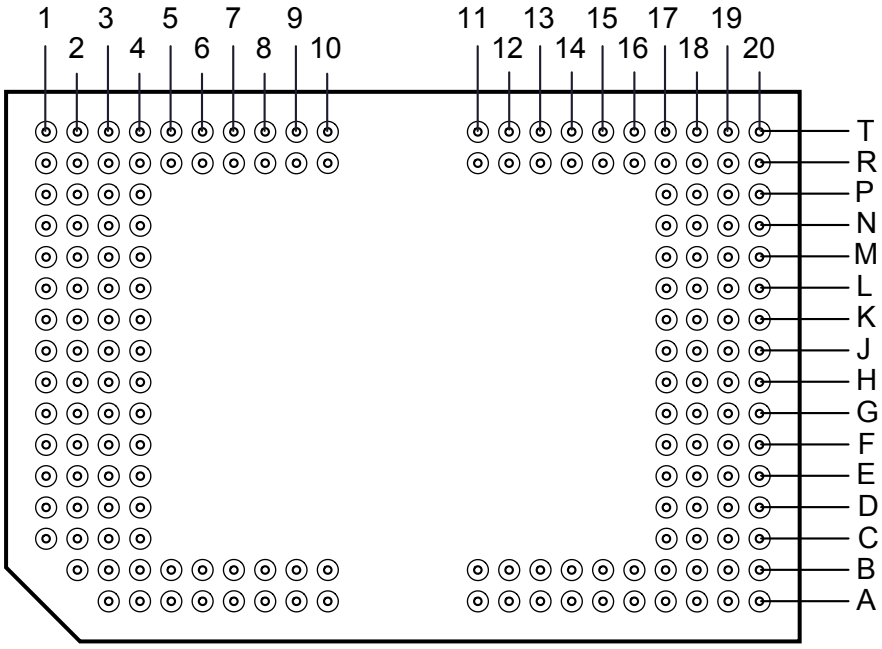


Figure 4-1. FXL Package 173-Pin PGA Bottom View

CAUTION

Properly manage the layout and the operation of signals identified in the Pin Functions table to make sure there is reliable, long-term operation of the 0.47" 4K UHD S460 DMD. Refer to the *PCB Design Requirements for TI DLP Digital Micromirror Devices* application report for specific details and guidelines before designing the board.

Table 4-1. Pin Functions

PIN		INPUT-OUTPUT[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	ID				
D_AP(0)	R2	I	High-speed Differential Data Pair lane A0	Differential 100Ω	8.204
D_AN(0)	P2	I	High-speed Differential Data Pair lane A0	Differential 100Ω	8.201
D_AP(1)	T4	I	High-speed Differential Data Pair lane A1	Differential 100Ω	9.95
D_AN(1)	T3	I	High-speed Differential Data Pair lane A1	Differential 100Ω	9.95
D_AP(2)	P1	I	High-speed Differential Data Pair lane A2	Differential 100Ω	8.439
D_AN(2)	N1	I	High-speed Differential Data Pair lane A2	Differential 100Ω	8.44
D_AP(3)	R5	I	High-speed Differential Data Pair lane A3	Differential 100Ω	10.166
D_AN(3)	R6	I	High-speed Differential Data Pair lane A3	Differential 100Ω	10.167
D_AP(4)	T5	I	High-speed Differential Data Pair lane A4	Differential 100Ω	12.672
D_AN(4)	T6	I	High-speed Differential Data Pair lane A4	Differential 100Ω	12.673
D_AP(5)	K2	I	High-speed Differential Data Pair lane A5	Differential 100Ω	5.097
D_AN(5)	L2	I	High-speed Differential Data Pair lane A5	Differential 100Ω	5.094
D_AP(6)	T7	I	High-speed Differential Data Pair lane A6	Differential 100Ω	13.416
D_AN(6)	T8	I	High-speed Differential Data Pair lane A6	Differential 100Ω	13.416
D_AP(7)	J1	I	High-speed Differential Data Pair lane A7	Differential 100Ω	6.356

Table 4-1. Pin Functions (continued)

PIN		INPUT-OUTPUT[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	ID				
D_AN(7)	K1	I	High-speed Differential Data Pair lane A7	Differential 100Ω	6.356
DCLK_AP	L1	I	High-speed Differential Clock A	Differential 100Ω	7.247
DCLK_AN	M1	I	High-speed Differential Clock A	Differential 100Ω	7.247
D_BP(0)	T13	I	High-speed Differential Data Pair lane B0	Differential 100Ω	9.167
D_BN(0)	T14	I	High-speed Differential Data Pair lane B0	Differential 100Ω	9.168
D_BP(1)	T17	I	High-speed Differential Data Pair lane B1	Differential 100Ω	10.163
D_BN(1)	T18	I	High-speed Differential Data Pair lane B1	Differential 100Ω	10.163
D_BP(2)	T12	I	High-speed Differential Data Pair lane B2	Differential 100Ω	12.753
D_BN(2)	T11	I	High-speed Differential Data Pair lane B2	Differential 100Ω	12.756
D_BP(3)	T15	I	High-speed Differential Data Pair lane B3	Differential 100Ω	14.679
D_BN(3)	T16	I	High-speed Differential Data Pair lane B3	Differential 100Ω	14.684
D_BP(4)	P20	I	High-speed Differential Data Pair lane B4	Differential 100Ω	10.903
D_BN(4)	N20	I	High-speed Differential Data Pair lane B4	Differential 100Ω	10.901
D_BP(5)	M20	I	High-speed Differential Data Pair lane B5	Differential 100Ω	10.043
D_BN(5)	L20	I	High-speed Differential Data Pair lane B5	Differential 100Ω	10.042
D_BP(6)	L19	I	High-speed Differential Data Pair lane B6	Differential 100Ω	8.167
D_BN(6)	K19	I	High-speed Differential Data Pair lane B6	Differential 100Ω	8.167
D_BP(7)	K20	I	High-speed Differential Data Pair lane B7	Differential 100Ω	7.373
D_BN(7)	J20	I	High-speed Differential Data Pair lane B7	Differential 100Ω	7.373
DCLK_BP	R19	I	High-speed Differential Clock B	Differential 100Ω	10.517
DCLK_BN	P19	I	High-speed Differential Clock B	Differential 100Ω	10.516
D_CP(0)	H1	I	High-speed Differential Data Pair lane C0	Differential 100Ω	6.308
D_CN(0)	G1	I	High-speed Differential Data Pair lane C0	Differential 100Ω	6.308
D_CP(1)	H2	I	High-speed Differential Data Pair lane C1	Differential 100Ω	4.941
D_CN(1)	G2	I	High-speed Differential Data Pair lane C1	Differential 100Ω	4.939
D_CP(2)	F1	I	High-speed Differential Data Pair lane C2	Differential 100Ω	7.011
D_CN(2)	E1	I	High-speed Differential Data Pair lane C2	Differential 100Ω	7.009
D_CP(3)	E2	I	High-speed Differential Data Pair lane C3	Differential 100Ω	6.959
D_CN(3)	D2	I	High-speed Differential Data Pair lane C3	Differential 100Ω	6.959
D_CP(4)	A4	I	High-speed Differential Data Pair lane C4	Differential 100Ω	10.185
D_CN(4)	A5	I	High-speed Differential Data Pair lane C4	Differential 100Ω	10.185
D_CP(5)	A7	I	High-speed Differential Data Pair lane C5	Differential 100Ω	9.34
D_CN(5)	A6	I	High-speed Differential Data Pair lane C5	Differential 100Ω	9.34
D_CP(6)	B7	I	High-speed Differential Data Pair lane C6	Differential 100Ω	9.109
D_CN(6)	B8	I	High-speed Differential Data Pair lane C6	Differential 100Ω	9.11
D_CP(7)	B5	I	High-speed Differential Data Pair lane C7	Differential 100Ω	7.548
D_CN(7)	B4	I	High-speed Differential Data Pair lane C7	Differential 100Ω	7.551
DCLK_CP	A9	I	High-speed Differential Clock C	Differential 100Ω	11.431
DCLK_CN	A8	I	High-speed Differential Clock C	Differential 100Ω	11.429
D_DP(0)	H19	I	High-speed Differential Data Pair lane D0	Differential 100Ω	5.531
D_DN(0)	G19	I	High-speed Differential Data Pair lane D0	Differential 100Ω	5.53
D_DP(1)	H20	I	High-speed Differential Data Pair lane D1	Differential 100Ω	7.153
D_DN(1)	G20	I	High-speed Differential Data Pair lane D1	Differential 100Ω	7.152
D_DP(2)	F20	I	High-speed Differential Data Pair lane D2	Differential 100Ω	7.449

Table 4-1. Pin Functions (continued)

PIN		INPUT-OUTPUT[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	ID				
D_DN(2)	E20	I	High-speed Differential Data Pair lane D2	Differential 100Ω	7.449
D_DP(3)	E19	I	High-speed Differential Data Pair lane D3	Differential 100Ω	7.592
D_DN(3)	D19	I	High-speed Differential Data Pair lane D3	Differential 100Ω	7.592
D_DP(4)	B19	I	High-speed Differential Data Pair lane D4	Differential 100Ω	9.968
D_DN(4)	B18	I	High-speed Differential Data Pair lane D4	Differential 100Ω	9.967
D_DP(5)	A18	I	High-speed Differential Data Pair lane D5	Differential 100Ω	10.435
D_DN(5)	A17	I	High-speed Differential Data Pair lane D5	Differential 100Ω	10.435
D_DP(6)	B16	I	High-speed Differential Data Pair lane D6	Differential 100Ω	9.291
D_DN(6)	B15	I	High-speed Differential Data Pair lane D6	Differential 100Ω	9.293
D_DP(7)	A16	I	High-speed Differential Data Pair lane D7	Differential 100Ω	9.269
D_DN(7)	A15	I	High-speed Differential Data Pair lane D7	Differential 100Ω	9.274
DCLK_DP	D20	I	High-speed Differential Clock D	Differential 100Ω	9.019
DCLK_DN	C20	I	High-speed Differential Clock D	Differential 100Ω	9.02
LS_WDATA	L3	I	Low speed interface (LSIF) write data		3.907
LS_CLK	P4	I	Low speed interface (LSIF) clock		4.52
LS_RDATA_A	N4	O	LPSDR Output		2.812
LS_RDATA_B	M3	O	LPSDR Output		2.925
LS_RDATA_C	J4	O	LPSDR Output		3.54
LS_RDATA_D	K3	O	LPSDR Output		3.094
DMD_DEN_ARSTZ	H4	I	ARSTZ		5.06
TP0	D18	I			4.175
TP1	C17	I			4.334
TP2	C18	I			0.34971
TEMP_N	E17	I	Temp Diode N		2.676
TEMP_P	F17	I	Temp Diode P		2.146
VDD	A10, A12, A13, A20, B2, B10, B11, B14, C4, D1, D4, E3, E18, F3, F4, G17, J3, J18, M18, N3, N18, R3, R8, R10, R12, R13, R18, T9	P	Digital Core Supply Voltage		
VDDI	D3, F18, G4, H18, K4, K18, L18, M4	P			
VRESET	T2, T19	P			
VBIAS	R1, R20	P			
VOFFSET	D17, E4, T1, T20	P			

Table 4-1. Pin Functions (continued)

PIN		INPUT-OUTPUT[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	ID				
VSS	A3, A11, A14, A19, B3, B6, B9, B12, B13, B17, B20, C1, C2, C3, C19, F2, F19, G3, G18, H3, J2, J19, L4, M2, M19, N2, N19, P3, P18, R4, R7, R9, R11, R14, R17, T10	G	Ground		
N/C	H17, R16, R15, P17, N17, M17, L17, K17, J17,	NC	No Connect Pin		None

(1) I=Input, O=Output, P=Power, G=Ground, NC = No Connect

5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, which may affect device reliability, functionality, and performance, and shorten the device's lifetime.

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
V_{DD}	Supply voltage for LVCMOS core logic and LPSDR low-speed interface (LSIF) (1)	–0.5	2.3	V
V_{DDI}	Supply voltage for SubLVDS receivers(1)	–0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(1) (2)	–0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode(1)	–0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode(1)	–15	0.5	V
$\lvert V_{DDI} – V_{DD} \rvert$	Supply voltage delta (absolute value)(3)		0.3	V
$\lvert V_{BIAS} – V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(4)		11	V
$\lvert V_{BIAS} – V_{RESET} \rvert$	Supply voltage delta (absolute value)(5)		34	V
INPUT VOLTAGE				
	Input voltage for other inputs – LSIF and LVCMOS(1)	–0.5	V_{DD}+0.5	V
	Input voltage for other inputs – SubLVDS(1) (6)	–0.5	V_{DDI}+0.5	V
SUBLVDS INTERFACE (HSIF)				
$\lvert V_{ID} \rvert$	SubLVDS differential input voltage (absolute value)(6)		810	mV
$\lvert I_{ID} \rvert$	SubLVDS input differential current(6)		10	mA
CLOCK FREQUENCY				
f_{CLOCK}	LSIF clock frequency (LS_CLK)	100	130	MHz
TEMPERATURE DIODE				
I_{TEMP_DIODE}	Max current source into temperature diode		120	µA
ENVIRONMENTAL				
T_{ARRAY}	Temperature, operating(7)	0	90	°C
	Temperature, non-operating(7)	–40	90	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) All voltage values are concerning the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{DDI} and V_{DD} may result in excessive current draw.
(4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. SubLVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(7) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), as shown in Figure 6-1 and Section 6.6.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD temperature	–40	80	°C
T_{DP-AVG}	Average dew point temperature, non-condensing(1)		28	°C
T_{DP-ELR}	Elevated dew point temperature range, non-condensing(2)	28	36	°C

5.2 Storage Conditions (continued)

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	months

(1) The average temperature over time (including storage and operating temperatures) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

5.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE RANGE					
V_{DD}	Supply voltage for LVCMOS core logic(1) (2) Supply voltage for LPSDR low-speed interface	1.71	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers(1) (2)	1.71	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(1) (2) (3)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for mirror electrode(1) (2)	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode(1) (2)	–14.5	–14	–13.5	V
$\lvert V_{DDI} - V_{DD} \rvert$	Supply voltage delta (absolute value)(1) (2) (4)			0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(1) (2) (5)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta (absolute value)(1) (2) (6)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK(7)	108		120	MHz
	Clock frequency for high-speed interface DCLK(8)			720	MHz
DCD_{IN}	Duty cycle distortion	48%		52%	
DCD_{OUT}	Duty cycle distortion	44%	50%	56%	
SUBLVDS INTERFACE					
$\lvert V_{ID} \rvert$	LVDS differential input voltage magnitude(8)	150	250	350	mV
V_{CM}	Common mode voltage(8)	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage(8)	525		1275	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance(10)	80	100	120	Ω
	100Ω differential PCB trace	6.35		152.4	mm
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operation(9) (10) (11) (12)	10		40 to 70	°C
	Array temperature, short-term operation, 500 hr max(10) (13)	0		10	°C
T_{DP-AVG}	Average dew point temperature, (non-condensing)(14)			28	°C

5.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
T_{DP-ELR}	Elevated dew point temperature range, (non-condensing)(15)		28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			28	Months
Q_{AP-LL}	Window Aperture illumination overfill(16) (17) (18)			17	W/cm^2
ILLUMINATION LPCW, RGB Laser and LED					
ILL_{UV}	Illumination, wavelength < 410nm(9) (20)			10	mW/cm^2
ILL_{VIS}	Illumination power at wavelengths ≥ 410nm and ≤ 800nm(19) (20)			60	W/cm^2
ILL_{IR}	Illumination, wavelength between > 800nm(20)			10	mW/cm^2
ILL_{BLU}	Illumination power at wavelengths ≥ 410nm and ≤ 475nm(19) (20)			19.5	W/cm^2
ILL_{BLU1}	Illumination power at wavelengths ≥ 410nm and ≤ 440nm(19) (20)			3.06	W/cm^2

(1) The following power supplies are required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(2) All voltage values are with respect to the V_{SS} ground pins.
(3) V_{OFFSET} supply transients must fall within the specified max voltages.
(4) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(5) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
(6) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit.
(7) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(8) Refer to the SubLVDS timing requirements in *Timing Requirements*.
(9) Simultaneous exposure of the DMD to the maximum Recommended Operating Conditions for temperature and UV illumination will reduce device lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) and the package thermal resistance using the Micromirror Array Temperature Calculation.
(11) The maximum operational array temperature is derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See the Section 6.9.1 section for a definition of micromirror landed duty cycle.
(12) Long-term is defined as the usable life of the device.
(13) Short-term is the total cumulative time over the useful life of the device.
(14) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(15) Exposure to dew point temperatures in the elevated range during storage and operation is limited to less than a total cumulative time of CT_{ELR}.
(16) Applies to the region defined in the Figure 5-2.
(17) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. Minimizing the light flux incident outside the active array is a design requirement of the illumination optical system. Depending on the particular optical architecture and assembly tolerances of the optical system, the amount of overfill light on the outside of the active array may cause system performance degradation.
(18) To calculate, see the Section 6.8.
(19) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
(20) To calculate, see the Section 6.7.

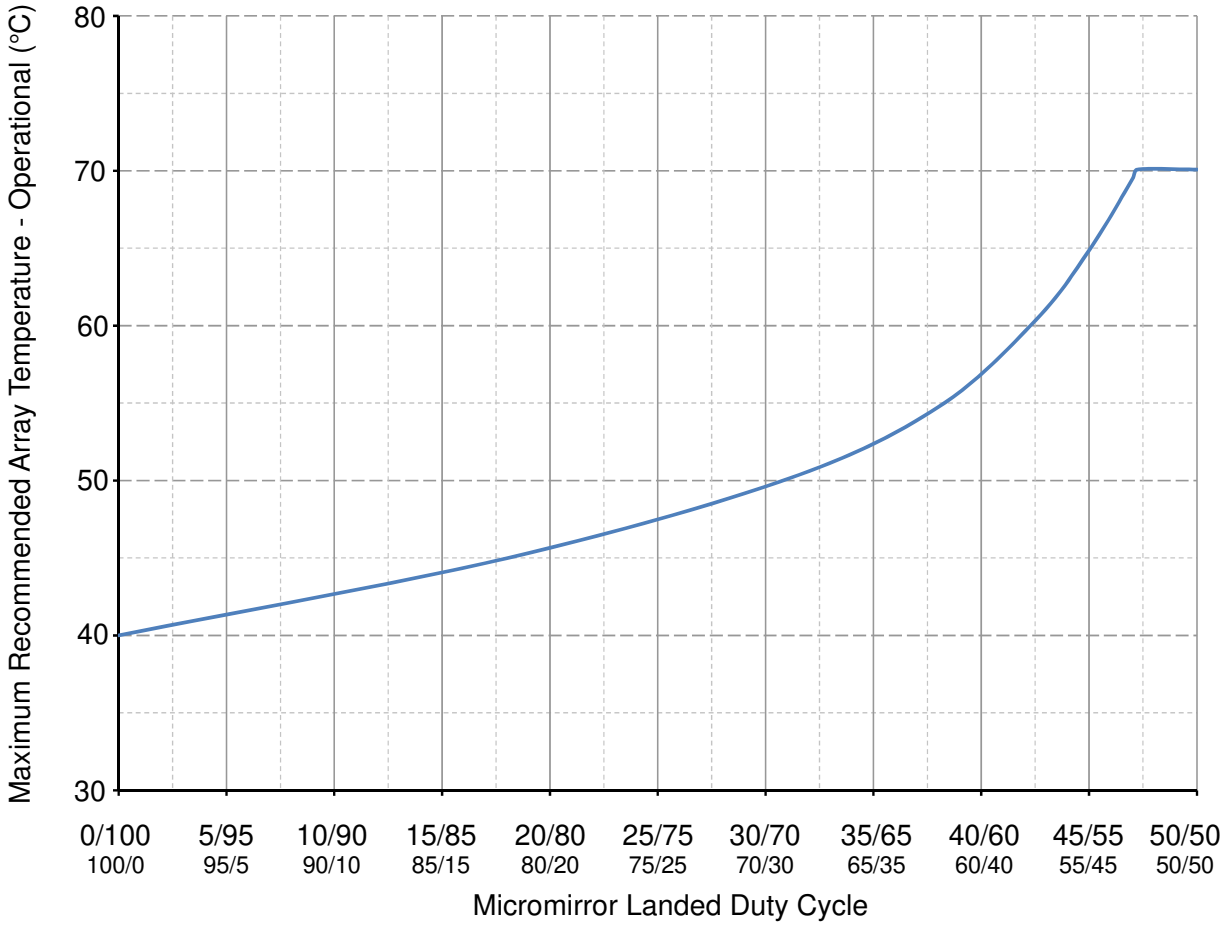


Figure 5-1. Maximum Recommended Array Temperature—Derating Curve

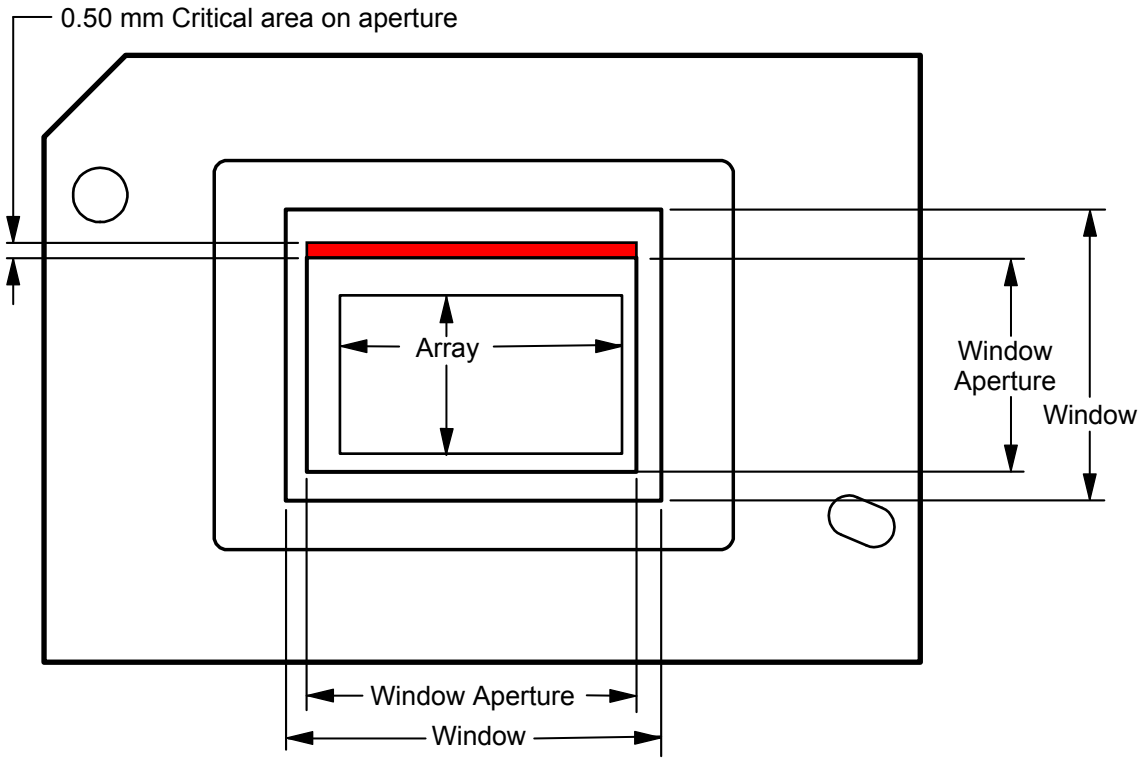


Figure 5-2. Illumination Overfill Diagram—Critical Area

5.5 Thermal Information

THERMAL METRIC	DLP473TE FXL PACKAGE 173 PINS	UNIT
Thermal Resistance, active area to test point 1 (TP1)(1)	1.0	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems must be designed to minimize the light energy falling outside the window's clear aperture, since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER(7)		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: V_{DD} (3) (4)	Typical		70		mA
I_{DDI}	Supply current: V_{DDI} (3) (4)	Typical		28		mA
I_{OFFSET}	Supply current: V_{OFFSET} (5) (6)	Typical		7		mA
I_{BIAS}	Supply current: V_{BIAS} (5) (6)	Typical		1.5		mA
I_{RESET}	Supply current: V_{RESET} (6)	Typical		3		mA
POWER						
P_{DD}	Supply power dissipation: V_{DD} (3) (4)	Typical		126		mW
P_{DDI}	Supply power dissipation: V_{DDI} (3) (4)	Typical		51		mW

5.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER(7)		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
P_{OFFSET}	Supply power dissipation: V_{OFFSET} (5) (6)	Typical		70		mW
P_{BIAS}	Supply power dissipation: V_{BIAS} (5) (6)	Typical		27		mW
P_{RESET}	Supply power dissipation: V_{RESET} (6)	Typical		42		mW
P_{TOTAL}	Supply power dissipation Total	Typical		316		mW
LPSDR INPUT						
V_{IH}	High-level input voltage(8) (9)		0.7 × V_{DD}		V_{DD} + 0.3	x VDD
V_{IL}	Low-level input voltage(8) (9)		–0.3		0.3 x V_{DD}	x VDD
$V_{IH(AC)}$	AC input high voltage(8) (9)		0.8 × V_{DD}		V_{DD} + 0.3	x VDD
$V_{IL(AC)}$	AC input low voltage(8) (9)		–0.3		0.2 × V_{DD}	x VDD
VHyst	Input Hysteresis (V_{T+} – $V_{T–}$)		0.1 × V_{DD}		0.4 × V_{DD}	V
I_{IL}	Low level input current	V_{DD} = 1.95V, V_I = 0V	–100			nA
I_{IH}	High level input current	V_{DD} = 1.95V, V_I = 1.95V			135	uA
LPSDR OUTPUT						
V_{OH}	DC output high voltage(10)	I_{OH} = –2mA	0.8 × V_{DD}			X VDD
V_{OL}	DC output low voltage(10)	I_{OL} = 2mA			0.2 × V_{DD}	X VDD
CAPACTIANCE						
C_{IN}	Input capacitance LVCMOS	F = 1MHz			10	pF
C_{IN}	Input capacitance SubLVDS	F = 1MHz			20	pF
C_{OUT}	Output capacitance	F = 1MHz			10	pF

(1) Device electrical characteristics are over Section 5.4 unless otherwise noted.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta | V_{DDI} – V_{DD} | must be less than the specified limit.
(4) Supply power dissipation based on non-compressed commands and data.
(5) To prevent excess current, the supply voltage delta | V_{BIAS} – V_{OFFSET} | must be less than the specified limit.
(6) Supply power dissipation based on three global resets in 200µs.
(7) All power supply connections are required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, V_{RESET}. All V_{SS} connections are also required.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, Low-Power Double Data Rate (LPDDR) JESD209B.
(10) LPSDR output specification is for pins LS_RDATA_A, LS_RDATA_B, LS_RDATA_C, LS_RDATA_D.

5.7 Switching Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q, rising edge of LS_CLK input to LS_RDATA output	C_L = 45pF			15	ns
	Slew rate, LS_RDATA		0.3			V/ns
	Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B		40%		60%	

5.8 Timing Requirements

Over operating free-air temperature range and supply voltages (unless otherwise noted)

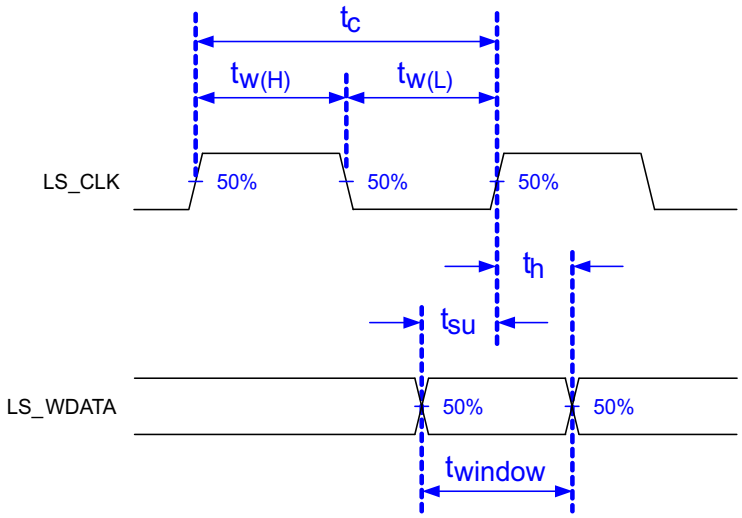
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LPSDR						
t_f	Fall slew rate(2)	(80% to 20%) × V_{DD} (5)	0.25			V/ns

5.8 Timing Requirements (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	Cycle time LS_CLK(5)	50% to 50% reference points(5)	7.7	8.3		ns
t_r	Rise slew rate(1)	(30% to 80%) × V_{DD} (6)	1		3	V/ns
t_f	Fall slew rate(1)	(70% to 20%) × V_{DD} (6)	1		3	V/ns
t_r	Rise slew rate(2)	(20% to 80%) × V_{DD} (6)	0.25			V/ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points(5)	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points(5)	3.1			ns
t_{WINDOW}	Window time(1) (3)	Setup time + Hold time(5)	3			ns
$t_{DERATING}$	Window time derating(1) (3)	For each 0.25V/ns reduction in slew rate below 1 V/ns(8)		0.35		ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK(5)			1.5	ns
t_h	Hold time	LS_WDATA valid after LS_CLK(5)			1.5	ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points(7)	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points(7)	0.7	1		V/ns
t_c	Cycle time D_CLK(9)	50% to 50% reference points(9)	1.35	1.39		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points(9)	0.7			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points(9)	0.7			ns
t_{su}	Setup time	DATA valid before D_CLK(9)			0.17	ns
t_h	Hold time	DATA valid after D_CLK(9)			0.17	ns
t_{WINDOW}	Window time	Setup time + Hold time(9) (10)			0.25	ns
t_{POWER}	Power-up receiver(4)				200	ns

(1) The specification is for the LS_CLK and LS_WDATA pins. Refer to the LPSDR input rise and fall slew rate in Figure 5-4.
(2) The specification is for the DMD_DEN_ARSTZ pin. Refer to the LPSDR input rise and fall slew rate in Figure 5-4.
(3) Window time derating example: 0.5V/ns slew rate increases the window time by 0.7ns, from 3 to 3.7ns.
(4) The specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.
(5) See Figure 5-3.
(6) See Figure 5-4.
(7) See Figure 5-5.
(8) See Figure 5-6.
(9) See Figure 5-7.
(10) See Figure 5-8.



The low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

Figure 5-3. LPSDR Switching Parameters

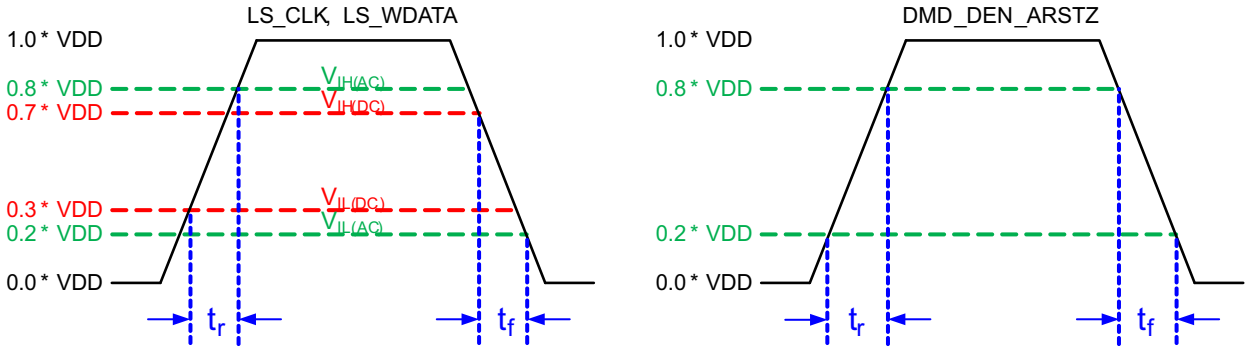


Figure 5-4. LPSDR Input Rise and Fall Slew Rate

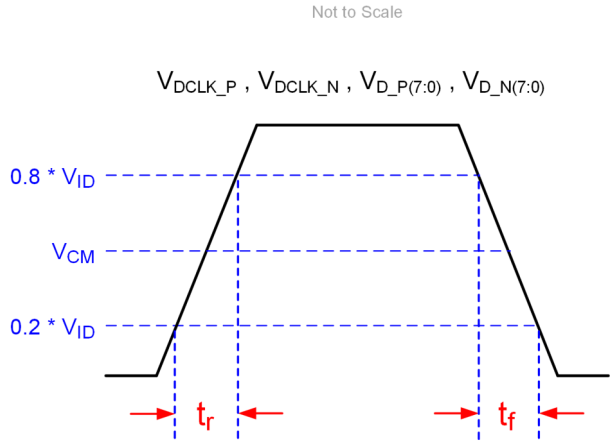


Figure 5-5. SubLVDS Input Rise and Fall Slew Rate

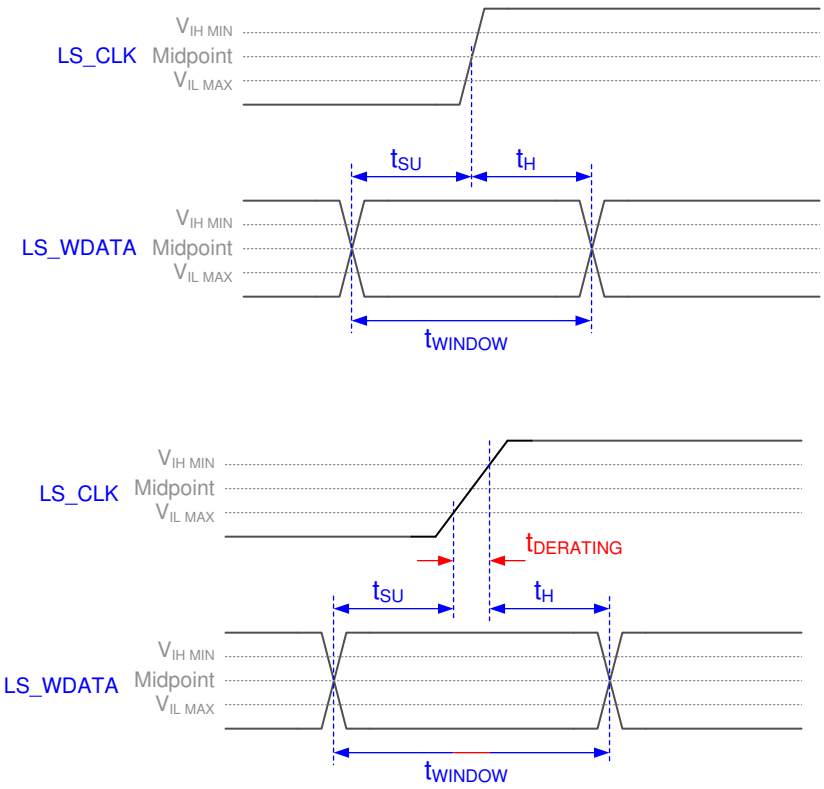


Figure 5-6. Window Time Derating Concept

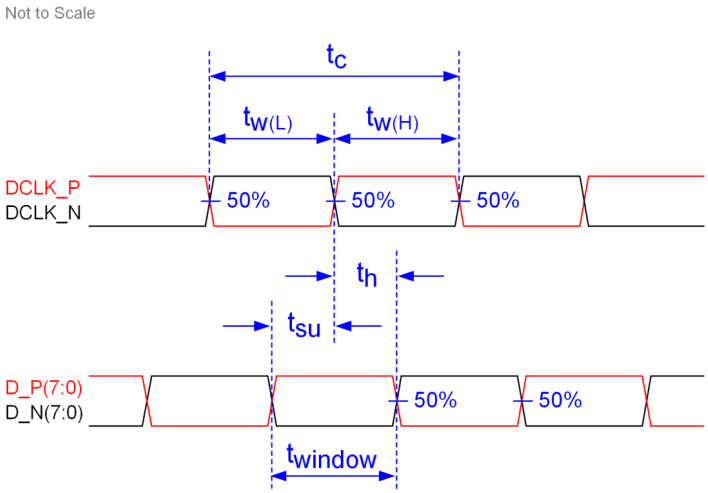
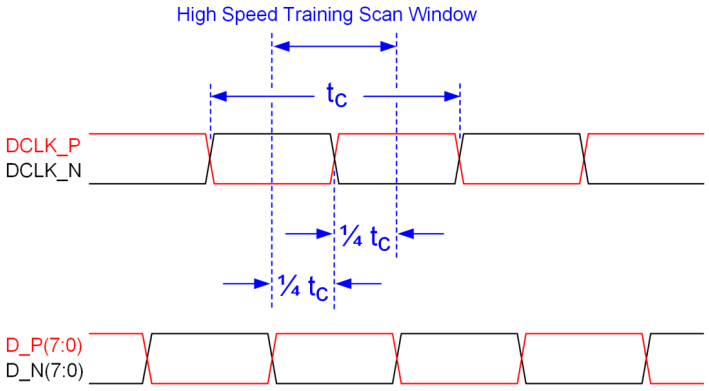


Figure 5-7. SubLVDS Switching Parameters



Note: Refer to the timing requirements for details.

Figure 5-8. High-Speed Training Scan Window

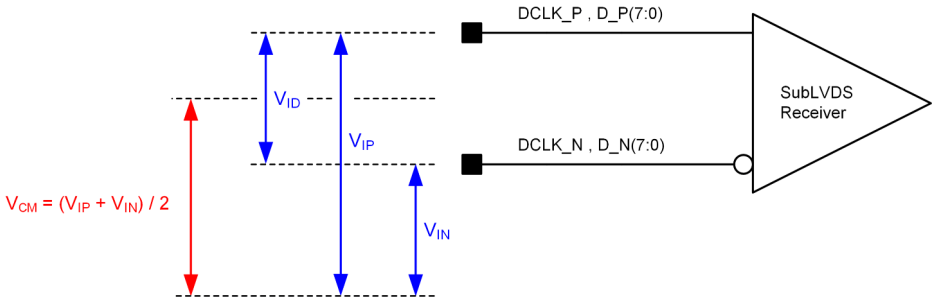


Figure 5-9. SubLVDS Voltage Parameters

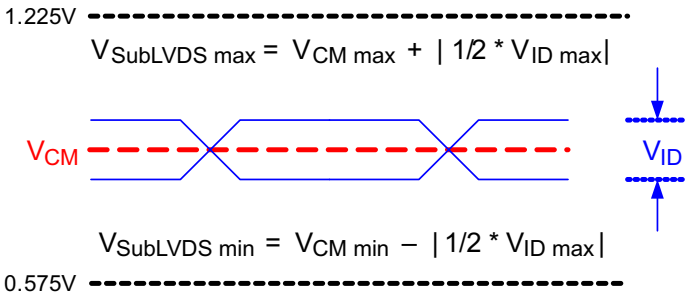


Figure 5-10. SubLVDS Waveform Parameters

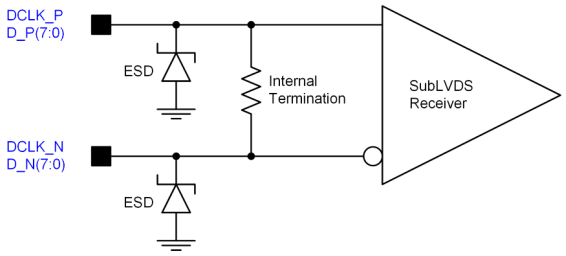


Figure 5-11. SubLVDS Equivalent Input Circuit

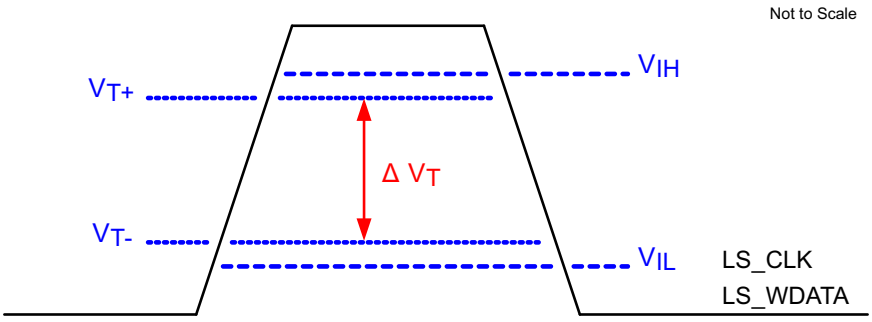


Figure 5-12. LPSDR Input Hysteresis

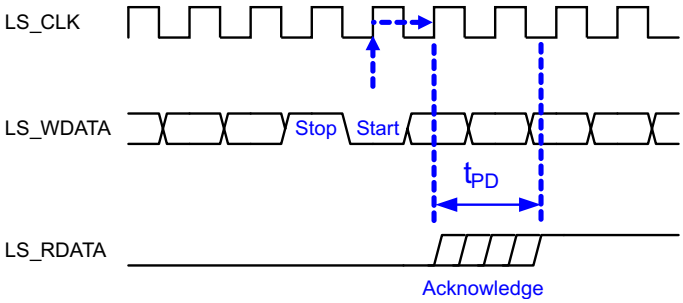
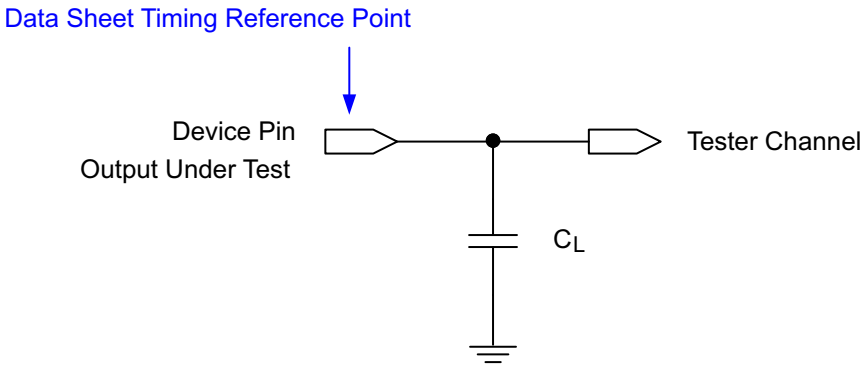


Figure 5-13. LPSDR Read Out



See the timing section for more information.

Figure 5-14. Test Load Circuit for Output Propagation Measurement

5.9 System Mounting Interface Loads

PARAMETER	MIN	TYP	MAX	UNIT
When loads are applied to the electrical and thermal interface areas				
Maximum load to be applied to the electrical interface area(1)			111	N
Maximum load to be applied to the thermal interface area(1)			111	N
When a load is applied to only the electrical interface area				
Maximum load to be applied to the electrical interface area(1)			222	N
Maximum load to be applied to the thermal interface area(1)			0	N

(1) The load should be uniformly applied in the corresponding areas shown in Figure 5-15.

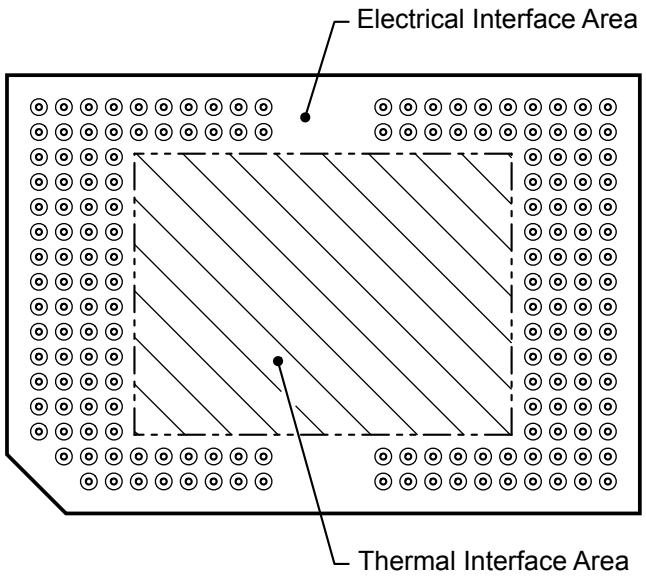


Figure 5-15. System Mounting Interface Loads

5.10 Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns(1) (2)	M	1920	micromirrors
Number of active rows(1) (2)	N	1080	micromirrors
Micromirror (pixel) pitch(1)	P	5.4	µm
Micromirror active array width(1)	Micromirror pitch × number of active columns	10.368	mm
Micromirror active array height(1)	Micromirror pitch × number of active rows	5.832	mm
Micromirror active border(3)	Pond of micromirror (POM)	20	micromirrors/side

(1) See Figure 5-16.
(2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed.
(3) The structure and qualities of the border around the active array include a band of partially functional micromirrors referred to as the pond of micromirrors (POM). These micromirrors are structurally and electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.

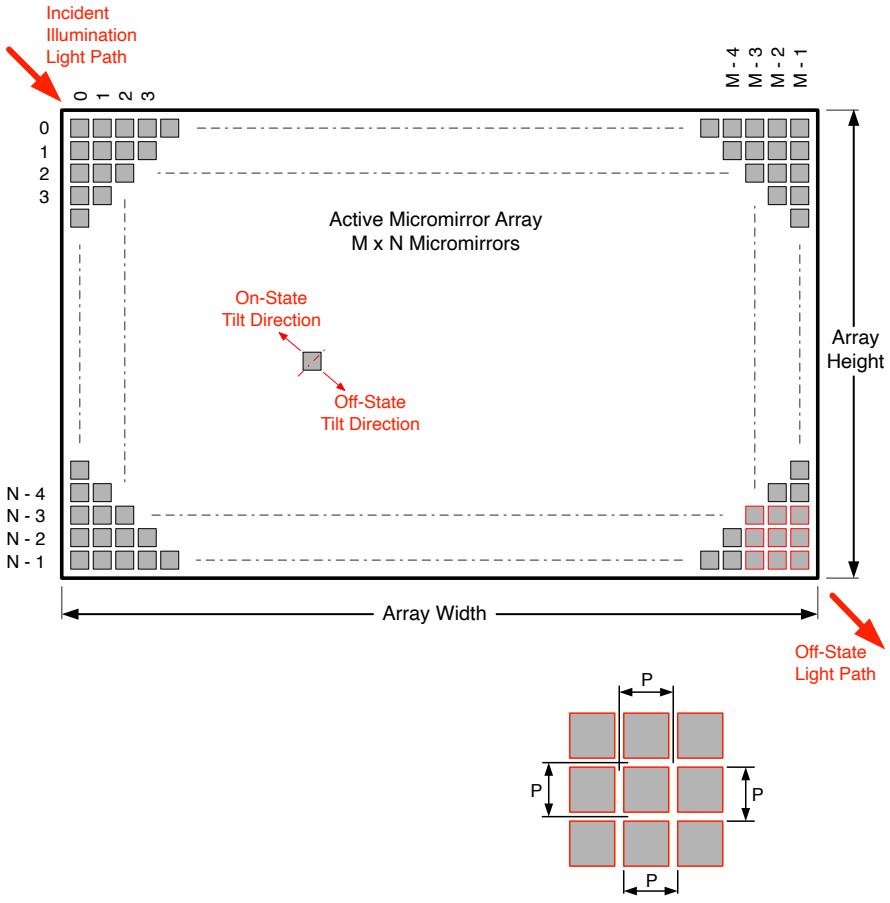


Figure 5-16. Micromirror Array Physical Characteristics

5.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micromirror tilt angle(1) (2) (3) (4)			13.5	14.5	15.5	degrees
Micromirror crossover time(5)		Typical Performance		3		µs
Micromirror switching time(6)		Typical Performance	6			
Image Performance (7)	Bright pixel(s) in active area(8)	Gray 10 Screen (9)			0	micromirrors
	Bright pixel(s) in the POM(10)	Gray 10 Screen (9)			1	
	Dark pixel(s) in the active area(11)	White Screen			4	
	Adjacent pixel(s)(12)	Any Screen			0	
	Unstable pixel(s) in active area(13)	Any Screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Represents the variation that can occur between any two individual micromirrors, located on the same device or on different devices.
(3) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(4) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(5) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(6) The minimum time between successive transitions of a micromirror.
(7) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
Test set degamma shall be linear
Test set brightness and contrast shall be set to nominal
The diagonal size of the projected image shall be a minimum of 20 inches
The projections screen shall be 1X gain
The projected image shall be inspected from a 38 inch minimum viewing distance
The image shall be in focus during all image quality tests
(8) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(9) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(10) POM definition: Rectangular border of off-state mirrors surrounding the active area
(11) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
(13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

5.12 Window Characteristics

DESCRIPTION(1)		MIN	TYP	MAX
Window material			Corning Eagle XG	
Window refractive index	At wavelength 546.1nm		1.5119	

(1) See Section 6.5 for more information.

5.13 Chipset Component Usage Specification

Reliable function and operation of the DLP473TE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding the limits described previously.

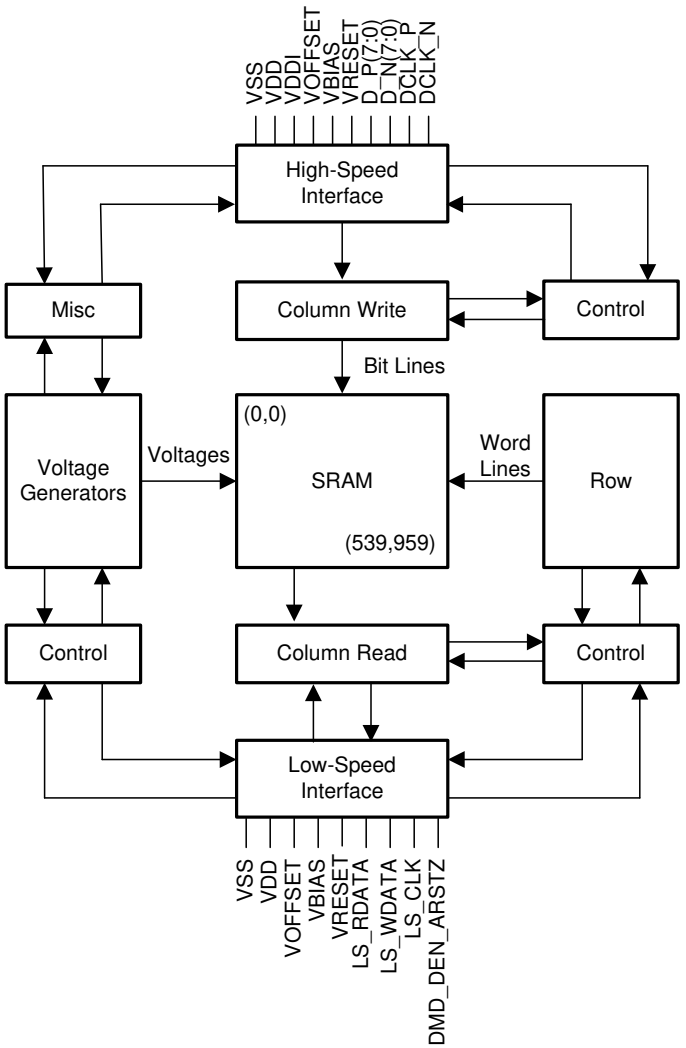
6 Detailed Description

6.1 Overview

The DLP473TE digital micromirror device (DMD) is a 0.47-inch diagonal spatial light modulator, which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed. The electrical interface is low-voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the *Functional Block Diagram*. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of the underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.47” 4K UHD chipset is comprised of the DLP473TE DMD, the DLPC8455 display controller, and the DLPA3082 PMIC. For reliable operation, always use the DLP473TE DMD with the DLP display controller and the PMIC specified in the chipset.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power Interface

The DMD requires four DC voltages: 1.8V source, V_{OFFSET}, V_{RESET}, and V_{BIAS}. In a typical configuration, all required voltages are generated by DLPA3082 PMIC.

6.3.2 Timing

The data sheet specifies the timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. Use the specified load capacitance value for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC8455 display controller. See the DLPC8455 display controller data sheet or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance are contingent on compliance with the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines the DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD, such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and or active area could occur.

6.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light on the window aperture may have to be further reduced below the suggested 10% maximum level in order to be acceptable.

6.6 Micromirror Array Temperature Calculation

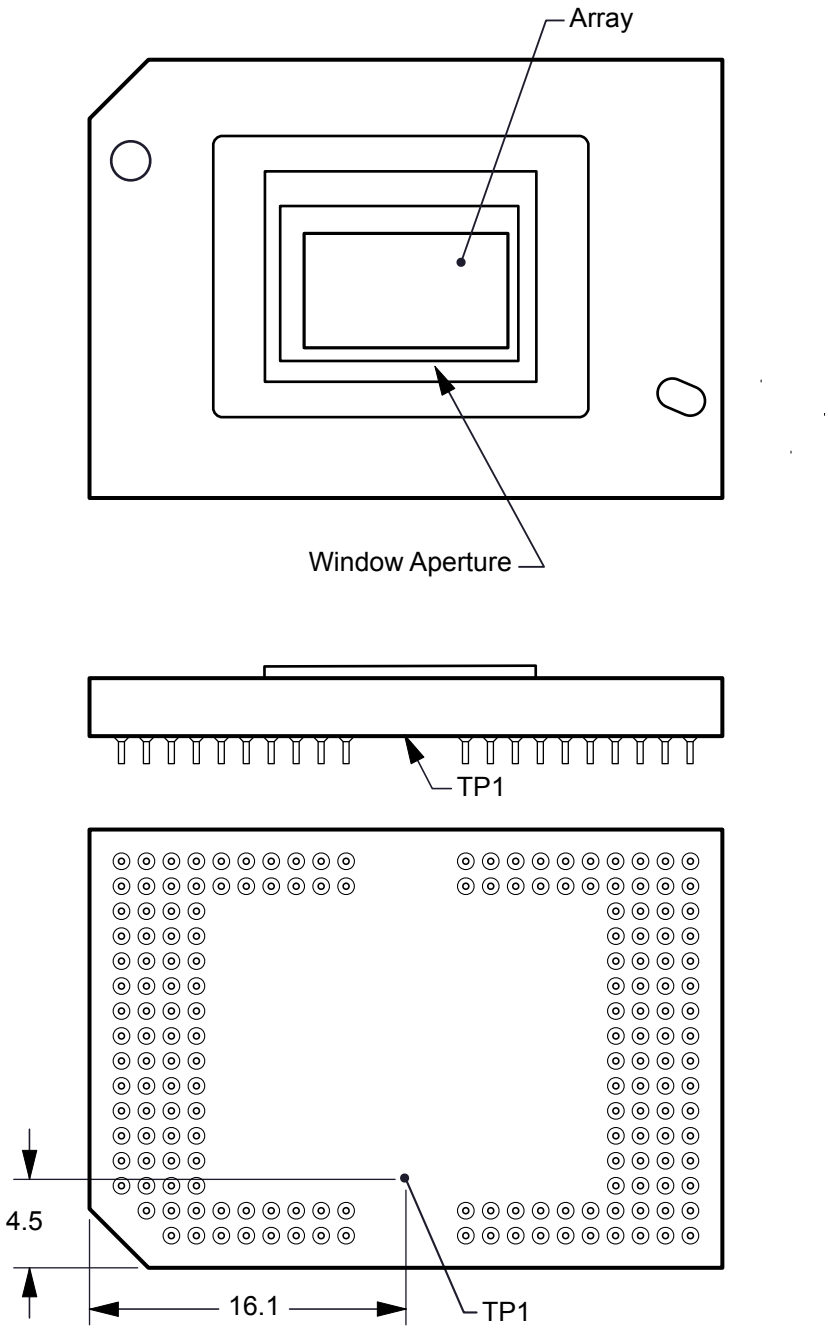


Figure 6-1. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly; therefore, it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations show the relationship between array temperature and the reference ceramic temperature, thermal test TP1, shown above.

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of the package specified in Section 5.5 from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.54

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.6W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single-chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{INCIDENT} = 35W \text{ (measured)} \quad (3)$$

$$T_{CERAMIC} = 50.0°C \text{ (measured)} \quad (4)$$

$$Q_{ELECTRICAL} = 0.6W \quad (5)$$

$$Q_{ARRAY} = 0.6W + (0.54 \times 35\ W) = 19.5W \quad (6)$$

$$T_{ARRAY} = 50.0°C + (19.5W \times 1.0°C/W) = 69.5°C \quad (7)$$

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, the percent illumination overfill, the area of the active array, and the ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000mW/W \div A_{ILL}$ (mW/cm^2)
- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000mW/W \div A_{ILL}$ (mW/cm^2)
- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})$ (cm^2)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm^2) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV\text{-}RATIO}$ = ratio of the optical power for wavelengths <410nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR\text{-}RATIO}$ = ratio of the optical power for wavelengths >800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤475nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤440nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and the overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values, the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$Q_{INCIDENT}$ = 35W (measured) (8)

A_{ARRAY} = (10.368mm × 5.832mm) ÷ $100mm^2/cm^2$ = $0.6047cm^2$ (data sheet) (9)

OV_{ILL} = 16.3% (optical model) (10)

$OP_{UV\text{-}RATIO}$ = 0.00017 (spectral measurement) (11)

$OP_{VIS\text{-}RATIO}$ = 0.99977 (spectral measurement) (12)

$OP_{IR\text{-}RATIO}$ = 0.00006 (spectral measurement) (13)

$OP_{BLU\text{-}RATIO}$ = 0.28100 (spectral measurement) (14)

$OP_{BLU1\text{-}RATIO}$ = 0.03200 (spectral measurement) (15)

A_{ILL} = $0.6047cm^2$ ÷ (1 - 0.163) = $0.7224cm^2$ (16)

$$ILL_{UV} = [0.00017 \times 35W] \times 1000\ mW/W \div 0.7224cm^2 = 8.236mW/cm^2 \quad (17)$$

$$ILL_{VIS} = [0.99977 \times 35W] \div 0.7224cm^2 = 48.44W/cm^2 \quad (18)$$

$$ILL_{IR} = [0.00006 \times 35W] \times 1000mW/W \div 0.7224cm^2 = 2.907mW/cm^2 \quad (19)$$

$$ILL_{BLU} = [0.28100 \times 35W] \div 0.7224cm^2 = 13.61W/cm^2 \quad (20)$$

$$ILL_{BLU1} = [0.03200 \times 35W] \div 0.7224cm^2 = 1.55W/cm^2 \quad (21)$$

6.8 Window Aperture Illumination Overfill Calculation

The amount of optical overfill on the critical area of the window aperture cannot be measured directly. For systems with uniform illumination on the array, the amount is determined using the total measured incident optical power on the DMD and the ratio of the total optical power on the DMD that is on the defined critical area. The optical model is used to determine the percent of optical power on the window aperture critical area and estimate the size of the area.

- $Q_{AP\text{-}ILL} = [Q_{INCIDENT} \times OP_{AP\_ILL\_RATIO}] \div A_{AP\_ILL}\ (W/cm^2)$

where:

- $Q_{AP\text{-}ILL}$ = window aperture illumination overfill (W/cm^2)
- $Q_{INCIDENT}$ = total incident optical power on the DMD (Watts) (measured)
- $OP_{AP\_ILL\_RATIO}$ = ratio of the optical power on the critical area of the window aperture to the total optical power on the DMD (optical model)
- $A_{AP\text{-}ILL}$ = size of the window aperture critical area (cm^2) (data sheet)
- OP_{CA_RATIO} = percent of the window aperture critical area with incident optical power (%) (optical model)

Sample calculation:

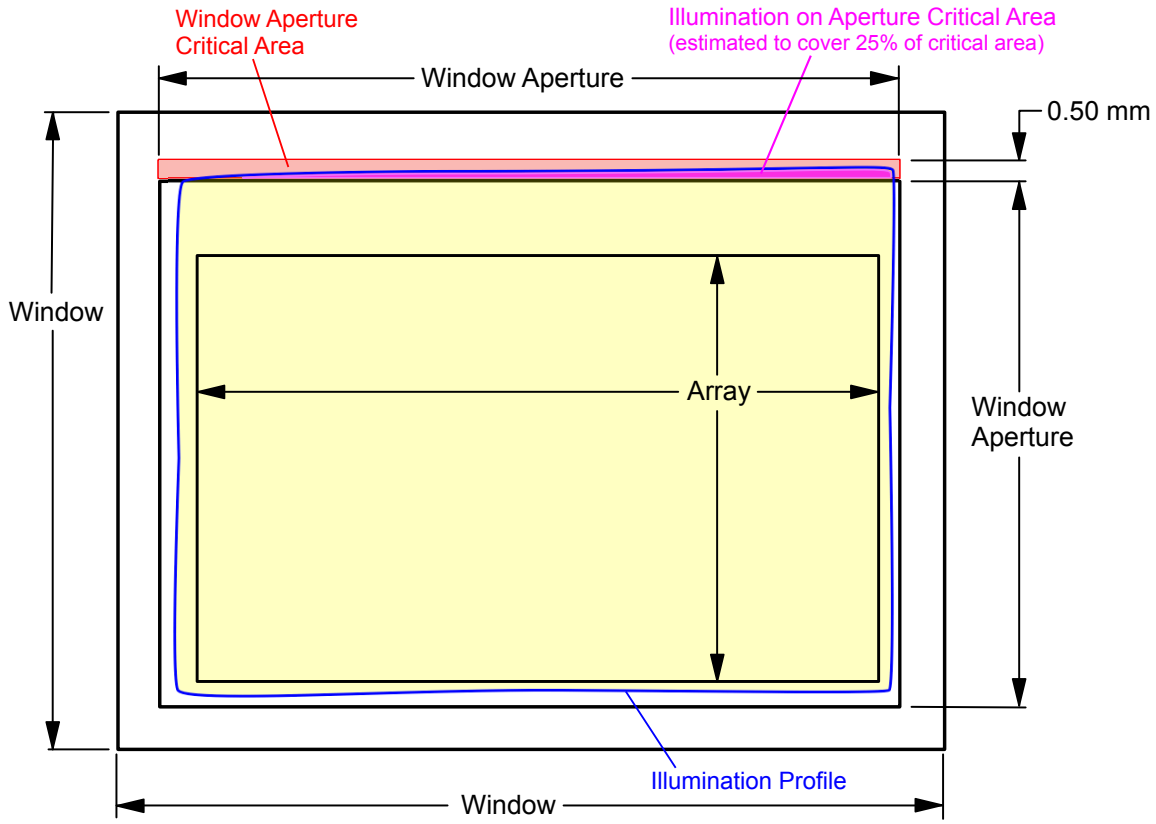


Figure 6-2. Window Aperture Overfill Example

See the figure for the length of the critical aperture.

$Q_{INCIDENT}$ = 35W (measured) (22)

$OP_{AP\_ILL\_RATIO}$ = 0.312% (optical model) (23)

OV_{CA_RATIO} = 25% (optical model) (24)

Length of the window aperture for critical area = 1.2496cm (data sheet) (25)

Width of critical area = 0.050cm (data sheet) (26)

$A_{AP\text{-}ILL}$ = 1.2496cm × 0.050cm = 0.06248 (cm^2) (27)

$Q_{AP\text{-}ILL}$ = (35W × 0.00312) ÷ (0.06248cm^2 × 0.25) = 7.0(W/cm^2) (28)

6.9 Micromirror Landed-On/Landed-Off Duty Cycle

6.9.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 would indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

6.9.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.9.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the derating curve shown in Figure 5-1. The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent a lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent a higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

6.9.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring, for the moment, color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in Table 6-1.

Table 6-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use Equation 29 to calculate the landed duty cycle of a given pixel during a given time period.

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (29)$$

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point.
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point.
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point.

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities would be as shown in Table 6-2 and Table 6-3.

Table 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	GREEN	BLUE
30%	50%	20%

Table 6-3. Example Landed Duty Cycle for Full-Color

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	30/70
0%	100%	0%	50/50
0%	0%	100%	20/80
0%	12%	0%	6/94
0%	0%	35%	7/93
60%	0%	0%	18/82
0%	100%	100%	70/30
100%	0%	100%	50/50
100%	100%	0%	80/20
0%	12%	35%	13/87
60%	0%	35%	25/75
60%	12%	0%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC8455 controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC8455 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in Figure 6-3.

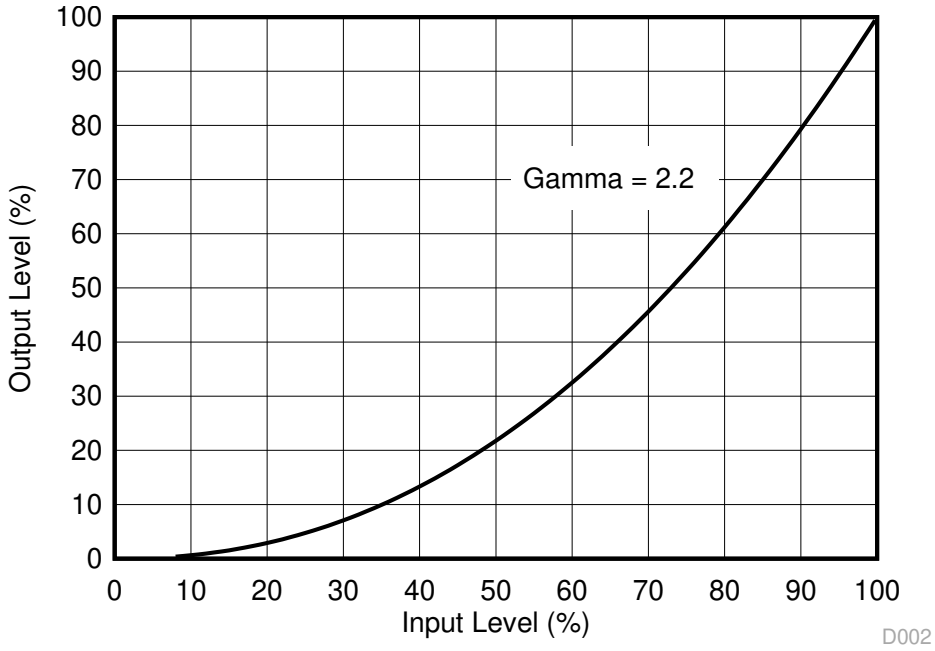


Figure 6-3. Example of Gamma = 2.2

From Figure 6-3, if the gray scale value of a given input pixel is 40% (before gamma is applied), then grayscale value is 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact on the displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing that occurs before the DLPC8455 controllers.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

DMDs are spatial light modulators that reflect incoming light from an illumination source in one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC8455 controller. The high-tilt pixel in the corner-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness-constrained applications. Typical applications using the DLP473TE include Laser TVs, home cinemas, and business projectors.

DMD power-up and power-down sequencing are strictly controlled by the DLPC8455 through the DLPA3082 PMIC. Refer to Section 8 for power-up and power-down specifications. To ensure reliable operation, the DLP473TE DMD must always be used with the DLPC8455 controller and the DLPA3082 PMIC.

7.2 Typical Application

The DLP473TE DMD combined with the DLPC8455 digital controller and a power management device provides full 4K UHD resolution for bright, colorful display applications. A typical RGB laser or LED system combines the DLP473TE DMD, DLPC8455 display controller, DLPA3082 voltage regulator, and the external illumination driver. In addition, the laser phosphor system includes the DLPA100 motor driver. Figure 7-1 shows a system block diagram for DLP 0.47" 4K UHD chipset.

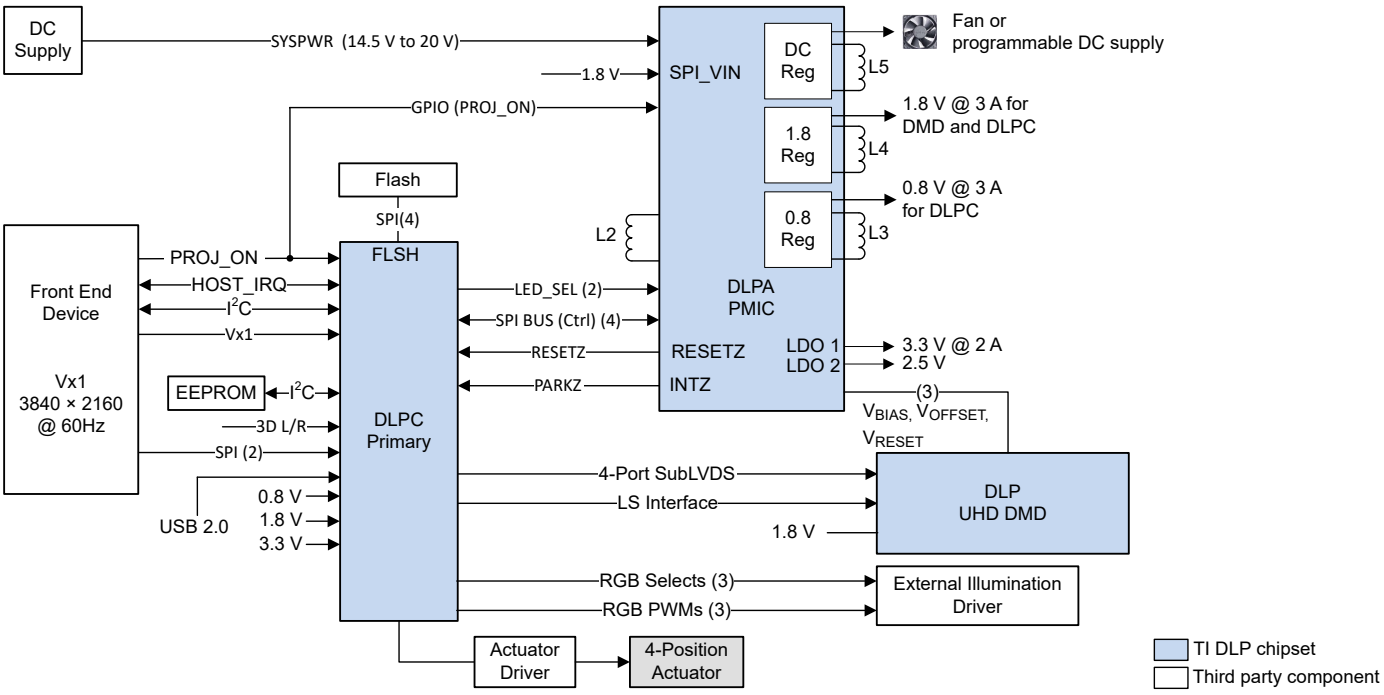


Figure 7-1. Typical 4K UHD System Diagram with External Illumination Driver

7.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness have a major effect on the overall system design and size.

The display system uses the DLP473TE as the core imaging device and contains a 0.47-inch array of micromirrors. The DLPC8455 controller is the digital interface between the DMD and the rest of the system, taking digital input from the front-end receiver and driving the DMD over a high-speed interface. The DLPA3082 PMIC serves as a voltage regulator for the controller, and DLPA100 is the color filter wheel and phosphor wheel motor control. The DLPA3082 PMIC also serves as a voltage regulator and provides the DMD reset, offset, and bias voltages.

7.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP473TE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with the DLPC8455 display controller and the DLPA3082 PMIC. Refer to PCB Design Requirements for TI DLP Digital Micromirror Devices for the DMD board design and manufacturing handling of the DMD sub-assemblies.

7.2.3 Application Curve

In a typical projector application, the luminous flux on the screen from the DMD depends on the optical design of the projector. The efficiency and total power of the illumination optical system and the projection optical system determine the overall light output of the projector. The DMD is inherently a linear spatial light modulator, so its efficiency just scales the light output. Figure 7-2 describes the relationship of laser input optical power to light output for a laser-phosphor illumination system, where the phosphor is not at its thermal quenching limit.

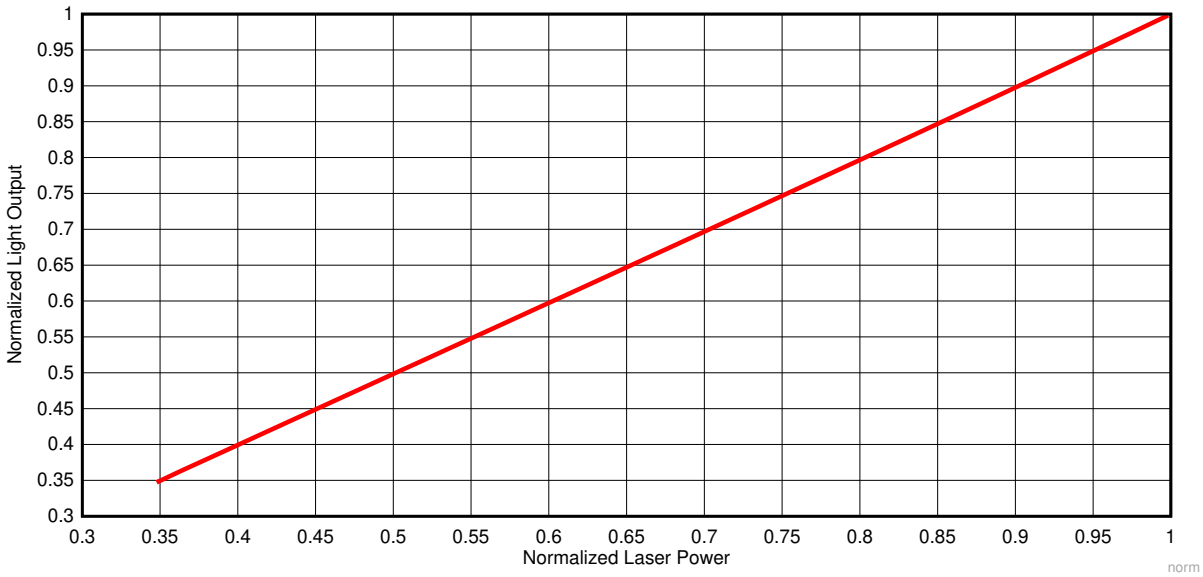
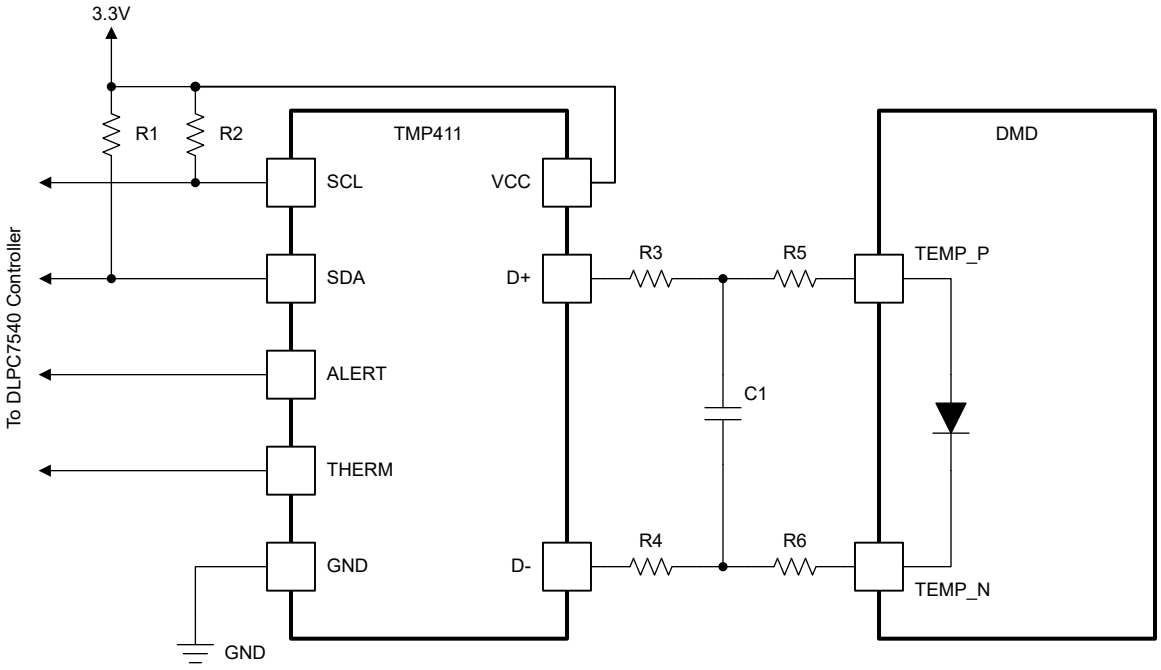


Figure 7-2. Normalized Light Output vs Normalized Laser Power for Laser Phosphor Illumination

7.3 Temperature Sensor Diode

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor, as shown in Figure 7-3. The software application contains functions to configure the TMP411 to read the DLP473TE DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, etc. All communication between the TMP411 and the DLPC8455 controller happens over the I^2C interface. The TMP411 connects to the DMD via pins outlined in Table 4-1.

If the temp sensor is not used, TEMP_N and TEMP_P pins should be left unconnected (NC).



A. Details omitted for clarity
B. See the TMP411 data sheet for the system board layout recommendation.
C. See the TMP411 data sheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.
D. R5 = 0Ω. R6 = 0Ω. Place 0Ω resistors close to the DMD package pins.

Figure 7-3. TMP411 Sample Schematic

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{DDI}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in Figure 8-1.

V_{BIAS}, V_{DD}, V_{DDI}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

Table 8-1. Power Supply Sequence Requirements

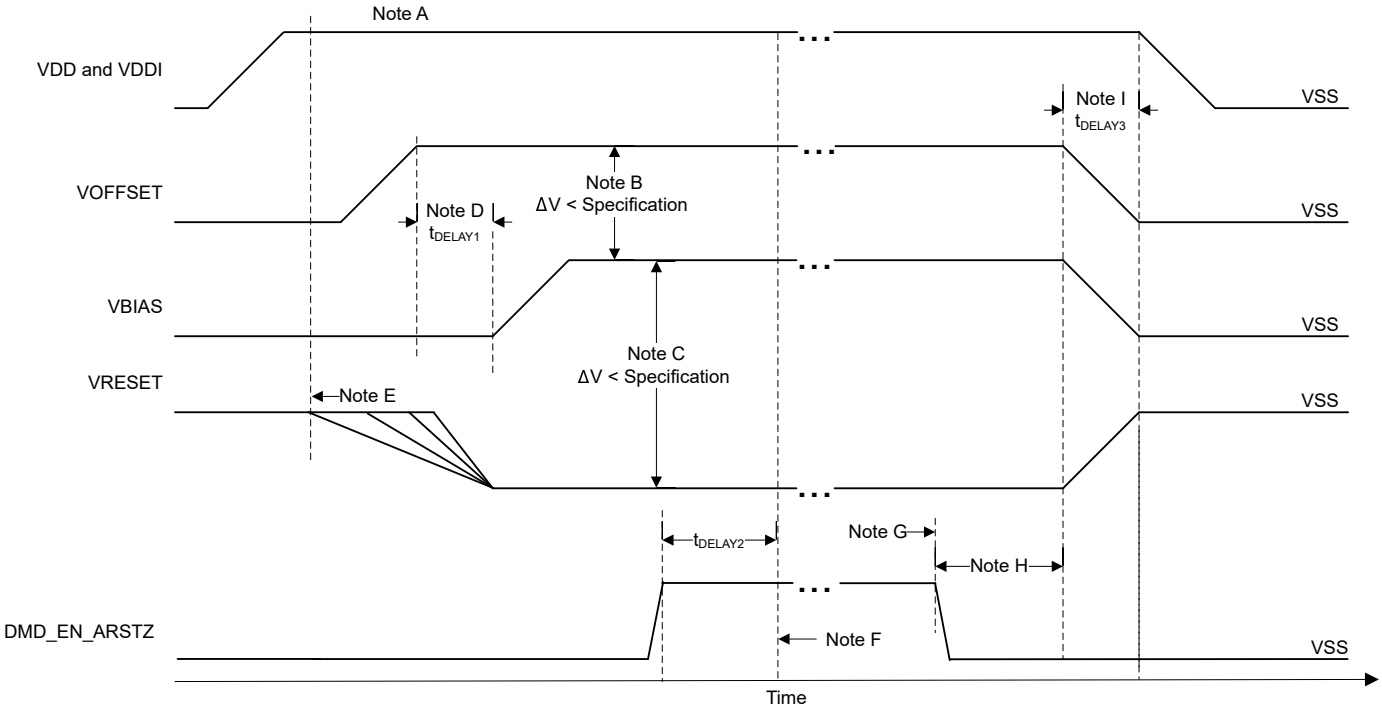
SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{DELAY}	Delay requirement	from V_{OFFSET} power up to V_{BIAS} power up	2			ms
V_{OFFSET}	Supply voltage level	at beginning of power-up sequence delay			6	V
V_{BIAS}	Supply voltage level	at end of power-up sequence delay			6	V

8.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} and V_{DDI} must always start and settle before V_{OFFSET} plus Delay1 specified in the *DMD power-supply requirements*, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in the *recommended operating conditions*.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in the *absolute maximum ratings*, *recommended operating conditions*, and the *DMD power-supply requirements*.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} have settled at operating voltages listed in the *recommended operating conditions*.

8.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} and V_{DDI} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground. See the *DMD power-supply requirements*.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in the *recommended operating conditions*.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in *absolute maximum ratings*, in the *recommended operating conditions*, and in the *DMD power-supply requirements*.
- During power-down, LVCMOS input pins must be less than specified in the *recommended operating conditions*.



A. See the *pin configuration and functions* section for the *Pin Functions Table*.
B. To prevent excess current, the supply voltage difference $|V_{OFFSET} – V_{BIAS}|$ must be less than the specified limit in the *recommended operating conditions*.
C. To prevent excess current, the supply difference $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit in the *recommended operating conditions*.
D. V_{BIAS} should power up after V_{OFFSET} has powered up, per the Delay1 specification in *DMD power-supply requirements*.
E. DLP controller software initiates the global V_{BIAS} command.
F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS}, V_{RESET}, and V_{OFFSET}.
G. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware DMD_EN_ARSTZ will go low.
H. V_{DD} must remain high until after V_{OFFSET}, V_{BIAS}, and V_{RESET} go low, per Delay2 specification in *DMD power-supply requirements*.
I. To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit in the *recommended operating conditions*.

Figure 8-1. DMD Power-Supply Requirements

Table 8-2. DMD Power-Supply Requirements

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1(1)	Delay from V_{OFFSET} settled at recommended operating voltage to V_{BIAS} and V_{RESET} power up	1	2		ms
Delay2(1)	Delay V_{DD} must be held high from V_{OFFSET}, V_{BIAS}, and V_{RESET} powering down.	50			µs

(1) See the *DMD power-supply requirements*.

9 Device and Documentation Support

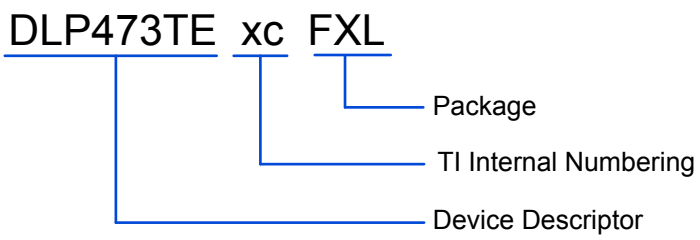
9.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Device Support

9.2.1 Device Nomenclature

Figure 9-1. Part Number Description

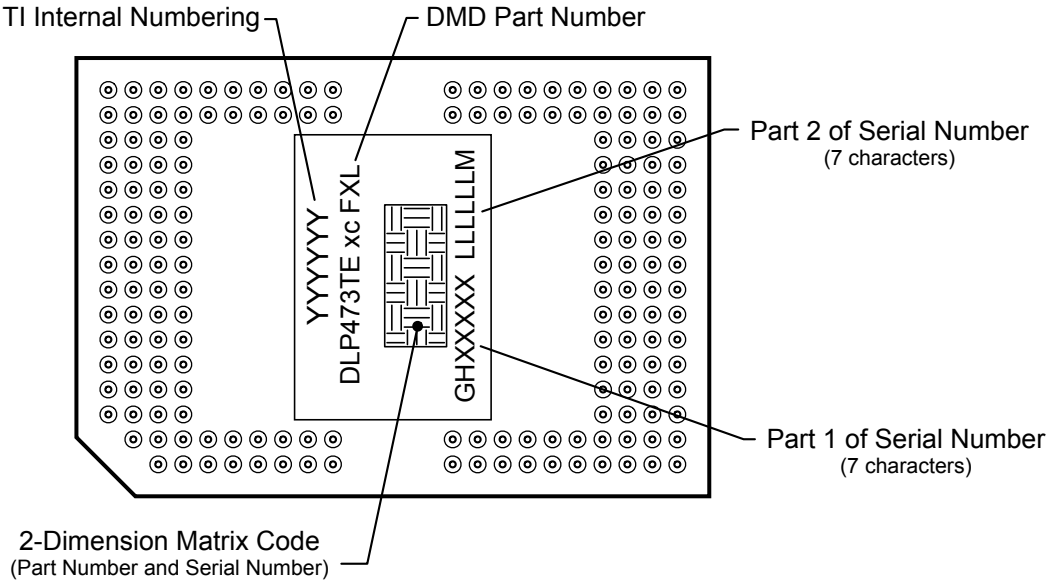


9.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 9-2. The 2-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

Example:

Figure 9-2. DMD Marking Locations



9.3 Documentation Support

9.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

- Texas Instruments, DLPC8455 controller data sheet
- Texas Instruments, DLPA3082 PMIC data sheet
- Texas Instruments, DLPA100 Motor Driver data sheet

9.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.8 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP473TE0FXL	Active	Production	CPGA (FXL) | 173	33 | JEDEC TRAY (5+1)	Yes	NI-PD-AU	N/A for Pkg Type	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

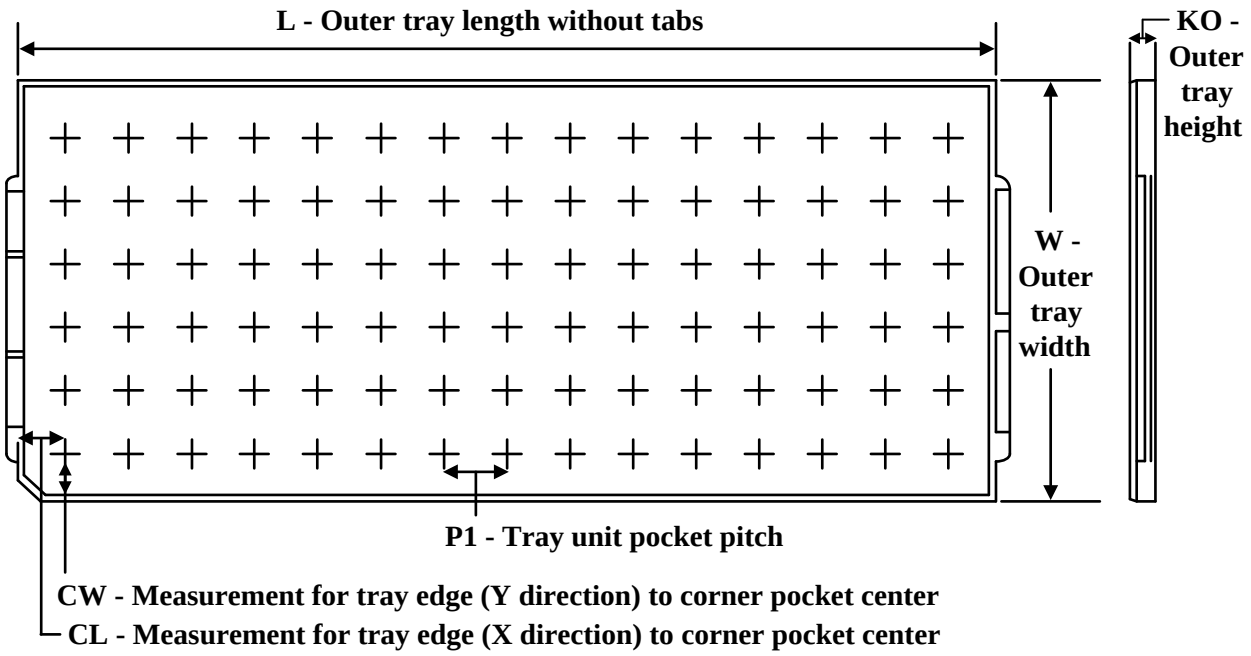
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

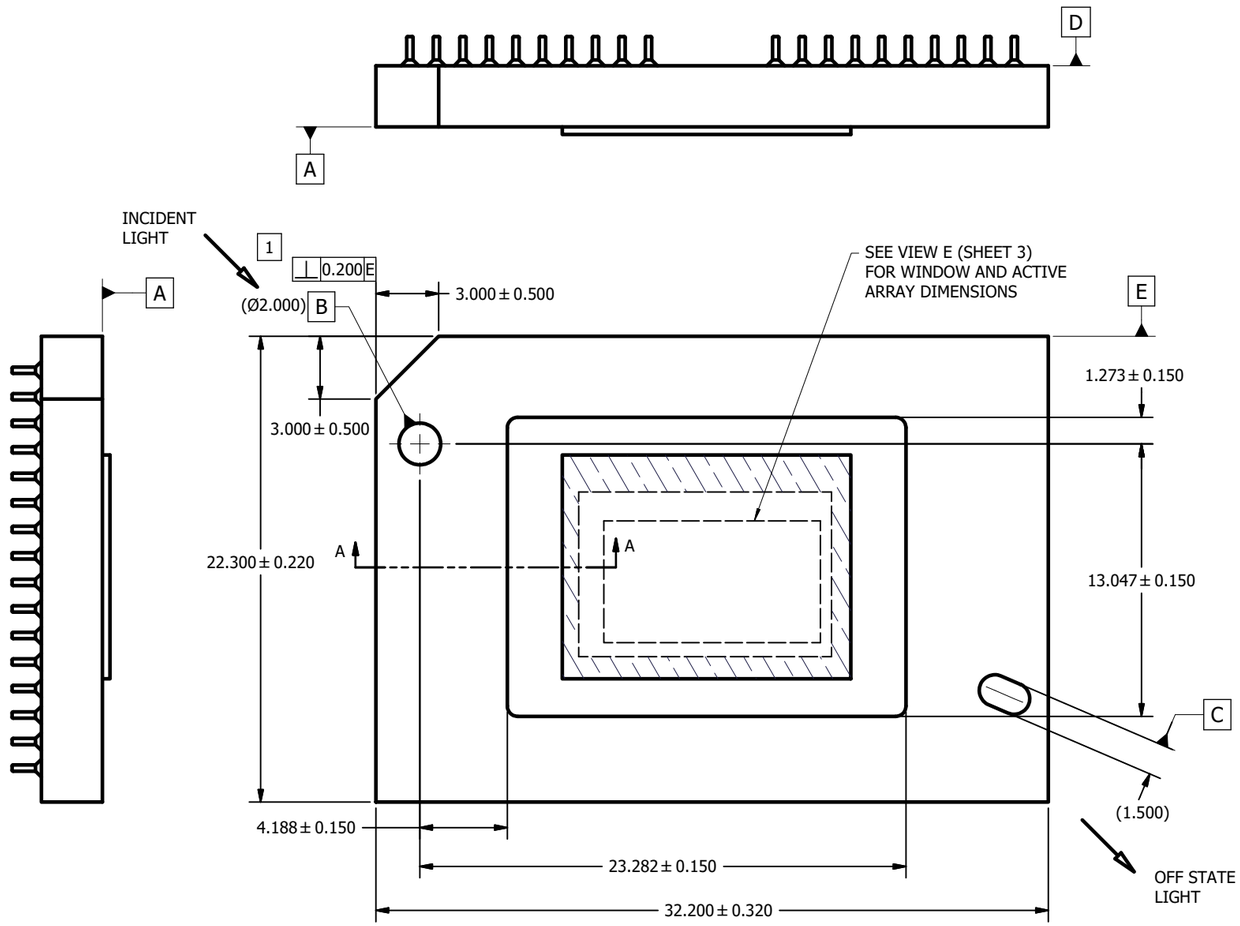
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP473TE0FXL	FXL	CPGA	173	33	3 x 11	150	315	135.9	12190	27.5	20	27.45

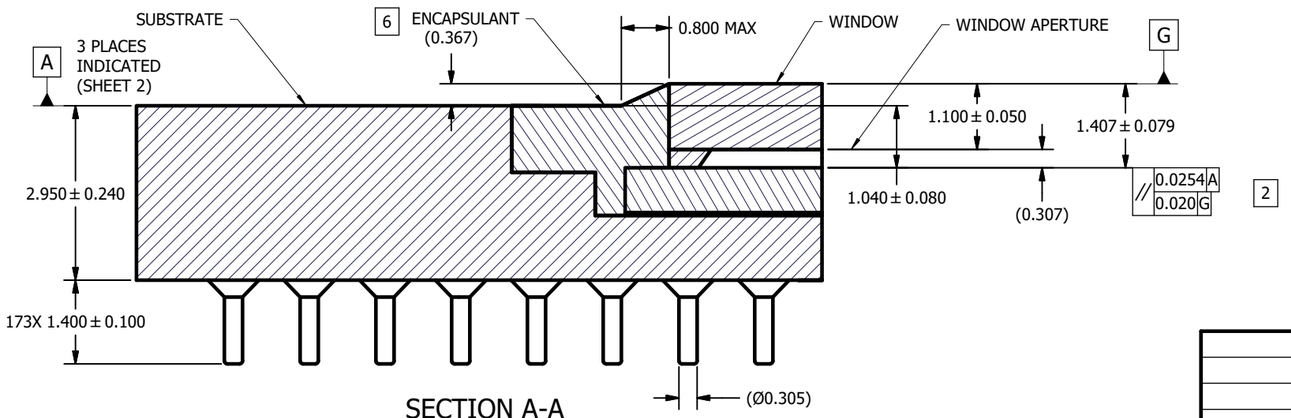
REVISIONS

REV	DESCRIPTION	DATE	BY
A	ECO 2209145: INITIAL RELEASE	07/01/2024	HG
B	ECO 2211621: UPDATE PoM DIMENSIONS	01/22/2025	PPC

NOTES UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE.
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM VALUE OF 0.8 DEGREES.
4. SUBSTRATE SYMBOLIZATION PAD AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE.
5. BOUNDARY MIRRORS SURROUNDING THE ACTIVE ARRAY.
6. MAXIMUM ENCAPSULANT PROFILE SHOWN.
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULATION SHALL NOT EXCEED 0.2 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.





SECTION A-A
SCALE 20 : 1

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	H. GAGLIARDI	7/1/2024
ENGINEER	H. GAGLIARDI	7/8/2024
QA/CE	M. DORAK	7/2/2024
CM	M. GARCIA	7/1/2024
APPROVED	J. MCKINLEY	7/3/2024

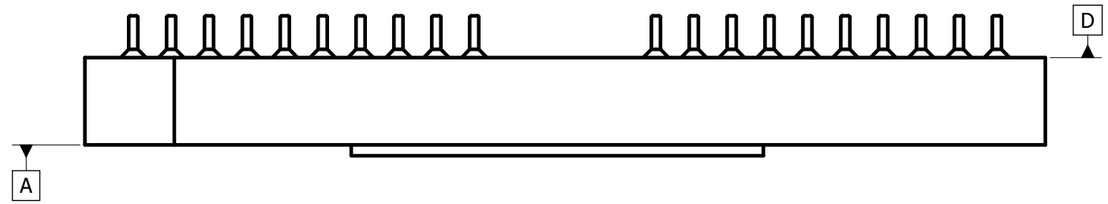
TEXAS INSTRUMENTS
Dallas Texas

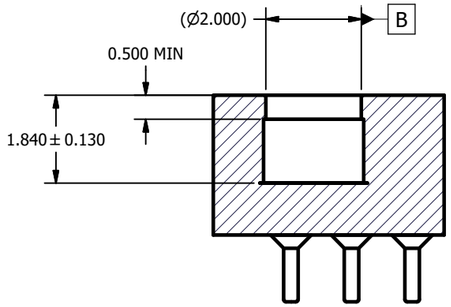
TITLE
ICD, MECHANICAL, DMD
.47" SST subLVDS SERIES 460
(FXL PACKAGE)

SIZE	DWG NO	REV
D	2519115	B

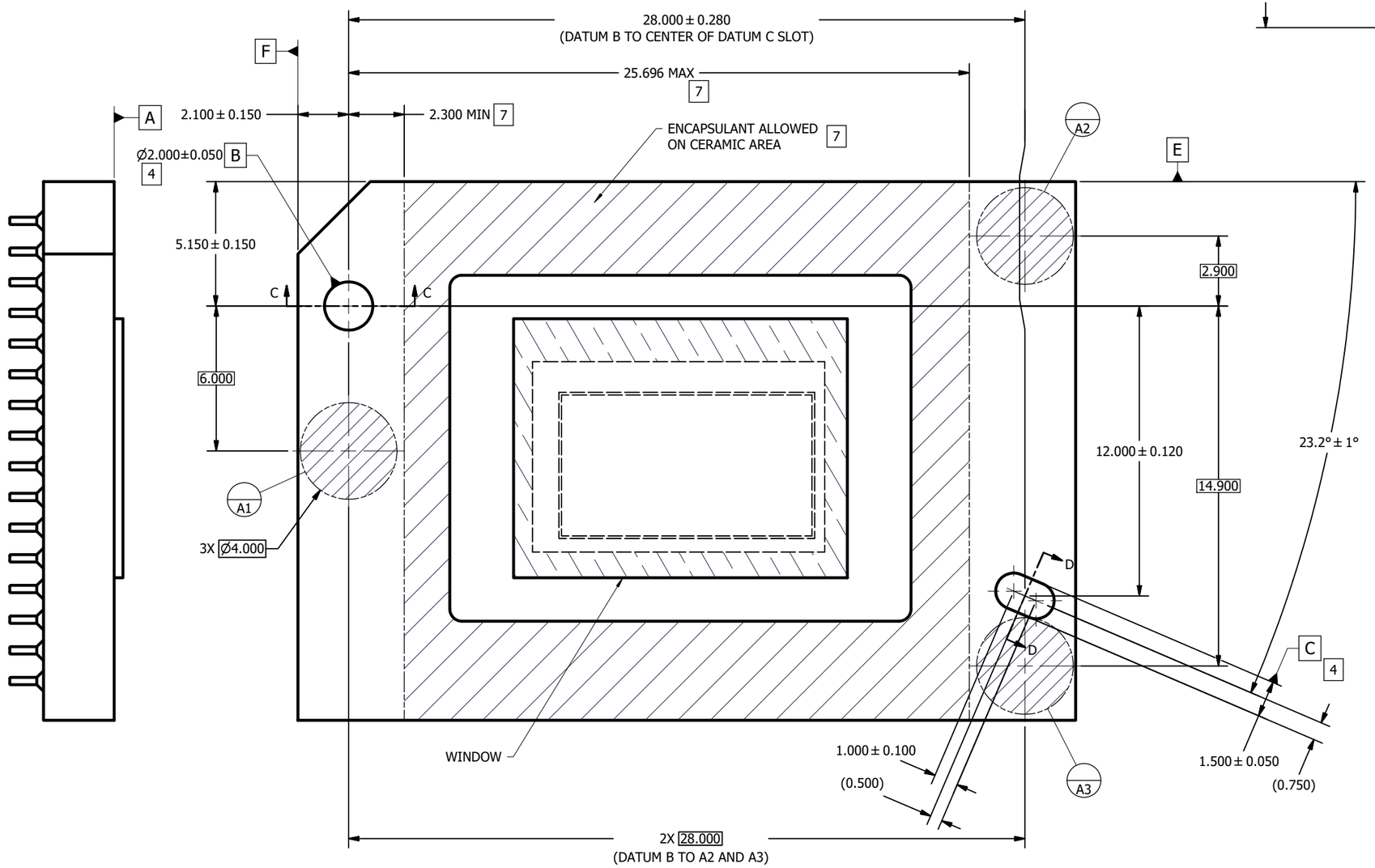
SCALE 4:1 SHEET 1 OF 4

INV2013-DLPa

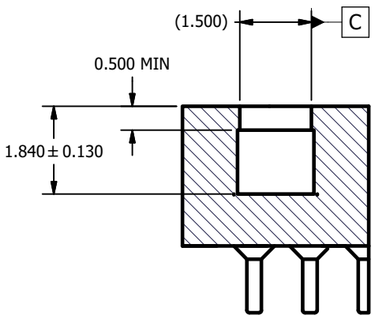




SECTION C-C
DATUM B
SCALE 16 : 1



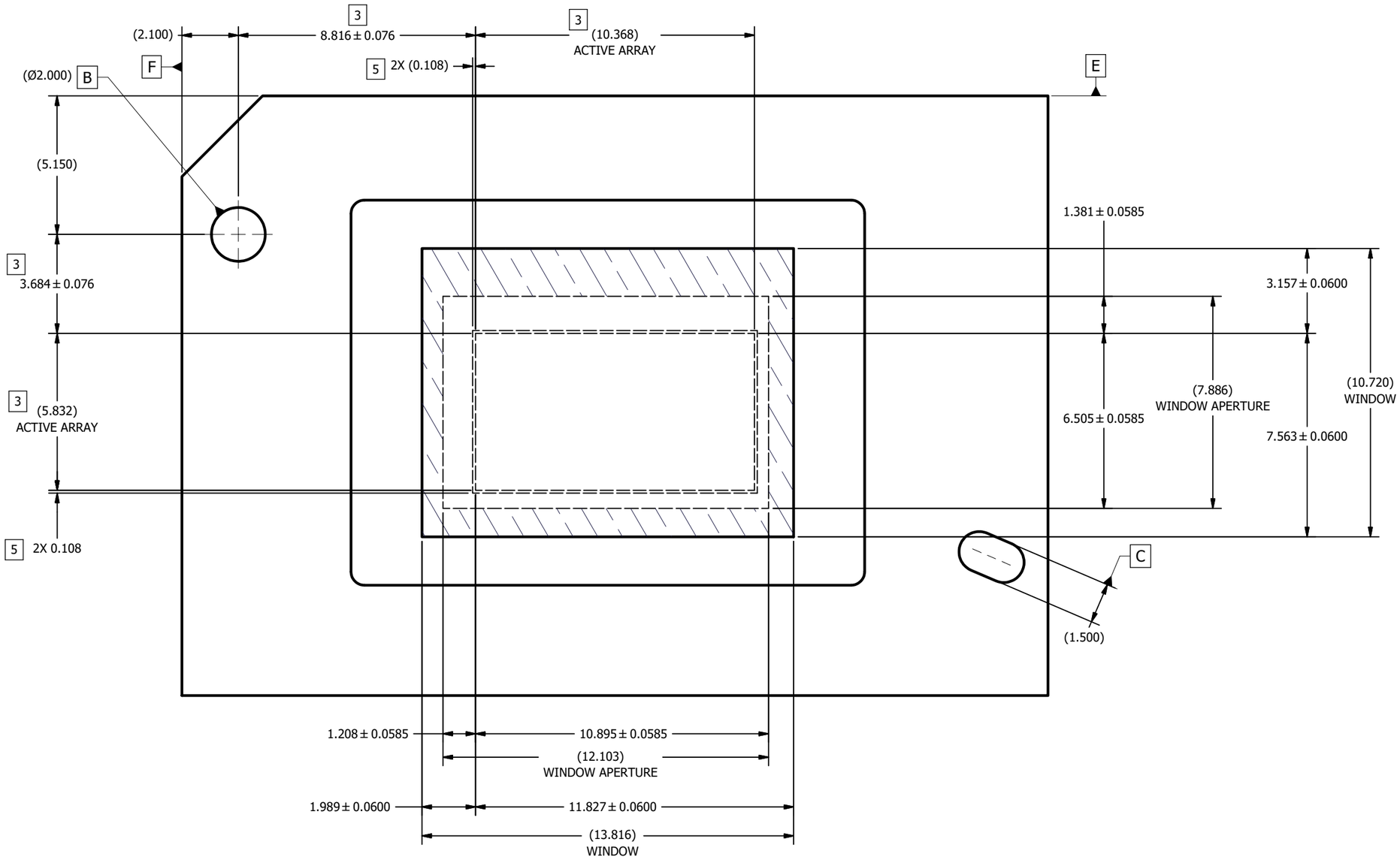
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 10 : 1



SECTION D-D
DATUM C
(VIEW ROTATED FOR CLARITY)
SCALE 16 : 1

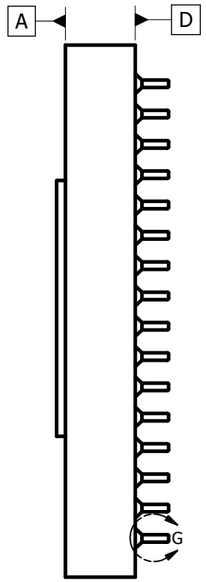
TEXAS INSTRUMENTS Dallas Texas	DRAWN H. GAGLIARDI	DATE 7/1/2024	SIZE D	DWG NO 2519115	REV B
			SCALE	SHEET 2 OF 4	

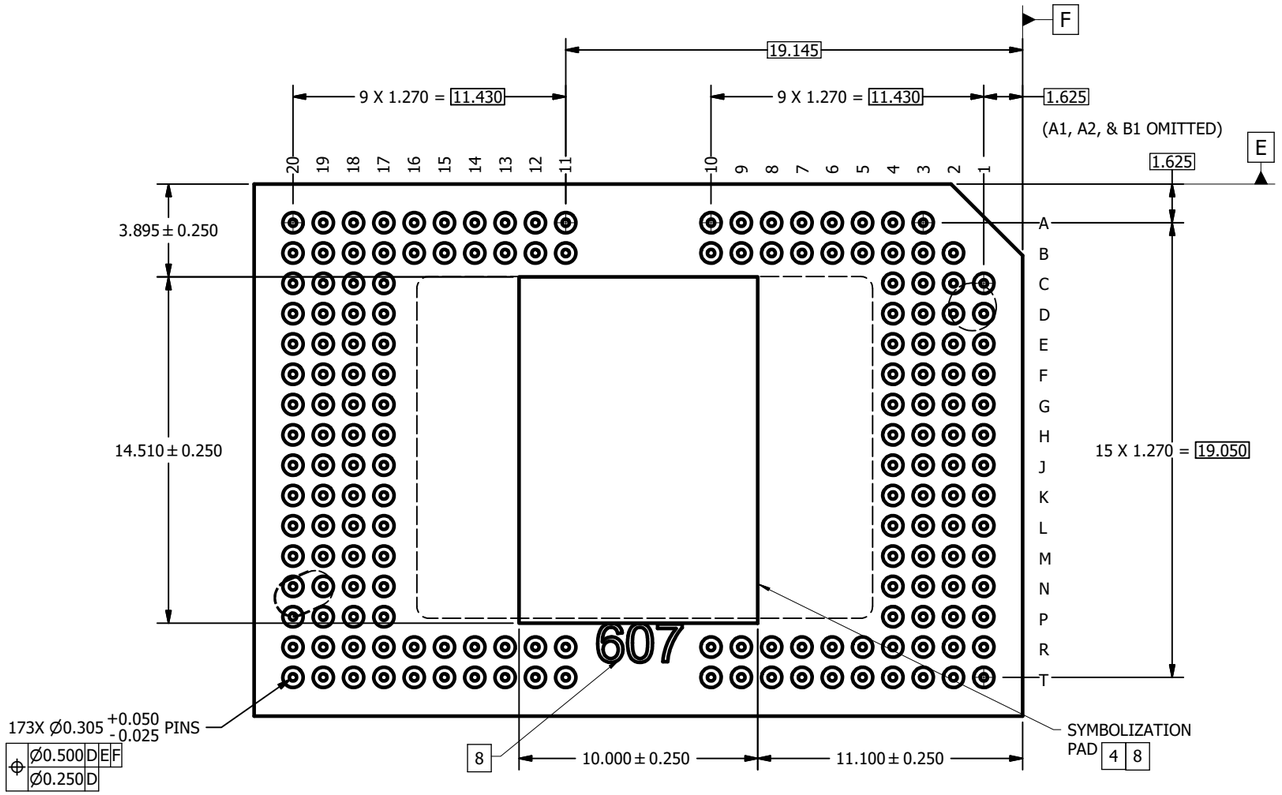
INV2013-DLPa



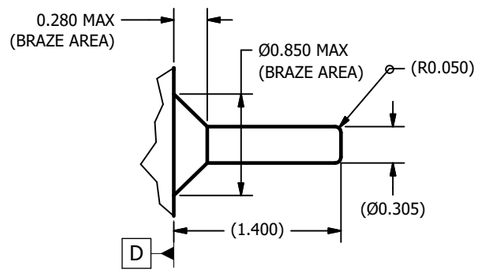
VIEW E
ACTIVE ARRAY AND WINDOW
SCALE 12 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN H. GAGLIARDI	DATE 7/1/2024	SIZE D		DWG NO 2519115	REV B
			SCALE		SHEET 3 OF 4	





VIEW F
PINS AND SYMBOLIZATION PAD
SCALE 8 : 1



DETAIL G
PIN AND BRAZE DIMENSIONS
173 PLACES
SCALE 40 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN H. GAGLIARDI	DATE 7/1/2024	SIZE D	DWG NO 2519115	REV B
			SCALE	SHEET 4 OF 4	

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265