Programmable Gamma-Voltage Generator and V_{COM} Calibrator with Integrated Two-Bank Memory

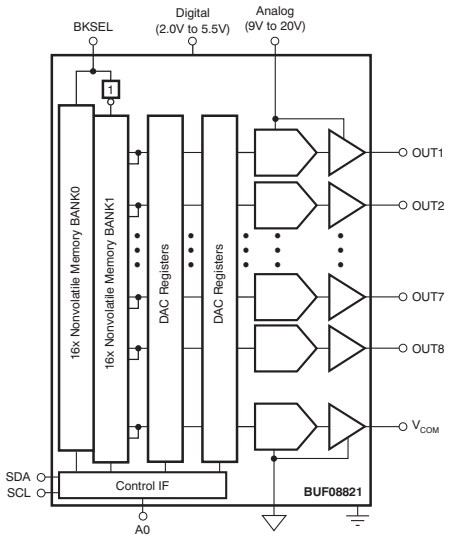
Check for Samples: BUF08821

FEATURES

- **10-BIT RESOLUTION**
- **8-CHANNEL P-GAMMA**
- **1-CHANNEL P-V_{COM}**
- **16x REWRITABLE NONVOLATILE MEMORY**
- **TWO INDEPENDENT PIN-SELECTABLE MEMORY BANKS**
- **RAIL-TO-RAIL OUTPUT: 300mV Minimum Swing-to-Rail (10mA) > 300mA Maximum I_{OUT}**
- **LOW SUPPLY CURRENT**
- **SUPPLY VOLTAGE: 9V to 20V**
- **DIGITAL SUPPLY: 2V to 5.5V**
- **I^2C™ INTERFACE: Supports 400kHz and 3.4MHz Clock Frequency**

APPLICATIONS

- **TFT-LCD REFERENCE DRIVERS**



DESCRIPTION

The BUF08821 offers eight programmable gamma channels plus one programmable V_{COM} channel.

The final gamma and V_{COM} values can be stored in the on-chip, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the BUF08821 supports up to 16 write operations to the on-chip memory.

The BUF08821 has two separate memory banks, allowing simultaneous storage of two different gamma curves to facilitate switching between gamma curves.

All gamma and V_{COM} channels offer a rail-to-rail output that typically swings to within 150mV of either supply rail with a 10mA load. All channels are programmed using an I^2C interface that supports standard operations up to 400kHz and high-speed data transfers up to 3.4MHz.

The BUF08821 is manufactured using Texas Instruments' proprietary, state-of-the-art, high-voltage CMOS process. This process offers very dense logic and HIGH supply voltage operation of up to 20V. The BUF08821 is offered in a HTSSOP-20 PowerPAD™ package. It is specified from –40°C to +85°C.

RELATED PRODUCTS

FEATURES	PRODUCT
22-Channel Gamma Correction Buffer	BUF22821
16-Channel Gamma Correction Buffer	BUF16821
12-Channel Gamma Correction Buffer	BUF12800
18-/20-Channel Programmable Buffer, 10-Bit, V_{COM}	BUF20800
18-/20-Channel Programmable Buffer with Memory	BUF20820
Programmable V_{COM} Driver	BUF01900
18V Supply, Traditional Gamma Buffers	BUF11704
22V Supply, Traditional Gamma Buffers	BUF11705

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING
BUF08821A	HTSSOP-20	PWP	BUF08821
BUF08821B	HTSSOP-20	PWP	BUF8821B

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		BUF08821	UNIT
Supply Voltage, V_S		+22	V
Supply Voltage, V_{SD}		+6	V
Digital Input Terminals, SCL, SDA, AO, BKSEL: Voltage		–0.5 to +6	V
Digital Input Terminals, SCL, SDA, AO, BKSEL: Current		±10	mA
Output Pins, OUT1 Through OUT8, V_{COM} (2)		(V–) – 0.5 to (V+) + 0.5	V
Output Short-Circuit(3)		Continuous	
Operating Temperature		–40 to +95	°C
Storage Temperature		–65 to +150	°C
Junction Temperature		+125	°C
ESD Ratings	Human Body Model (HBM)	4000	V
	Charged-Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) See the *Output Pins ESD Protection Current-Steering Diodes* section.
(3) Short-circuit to ground, one channel at a time.

ELECTRICAL CHARACTERISTICS

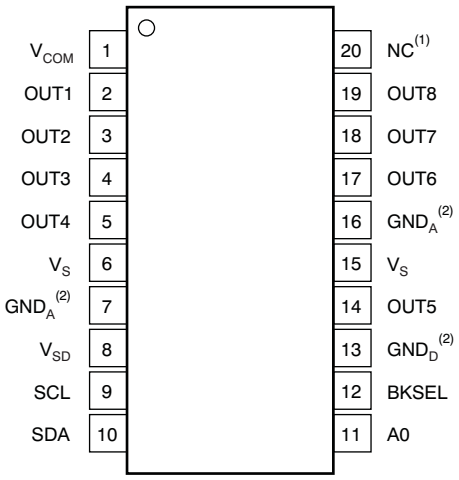
Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**
At T_A = +25°C, V_S = +18V, V_{SD} = +2V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF08821 MIN	BUF08821 TYP	BUF08821 MAX	UNIT
ANALOG GAMMA BUFFER CHANNELS						
Reset Value		Code 512		9		V
OUT 1–8 Output Swing: High		**Code = 1023, Sourcing 10mA**	**17.7**	**17.85**		**V**
OUT 1–8 Output Swing: Low		**Code = 0, Sinking 10mA**		**0.07**	**0.3**	**V**
V_{COM}1, 2 Output Swing: High						**V**
BUF08821A		**Code = 1023, Sourcing 100mA**	**13**	**16.2**		**V**
BUF08821B(1)		**Code = 511, Sourcing 100mA**		**8.96**		**V**
V_{COM}1, 2 Output Swing: Low						**V**
BUF08821A		**Code = 0, Sinking 100mA**		**0.6**	**2**	**V**
BUF08821B(1)		**Code = 384, Sinking 100mA**		**6.75**		**V**
Continuous Output Current		See Note (2)		30		mA
Output Accuracy				±20	±50	mV
vs Temperature		**Code 512**		**±25**		**µV/°C**
Integral Nonlinearity	INL			0.3		LSB
Differential Nonlinearity	DNL			0.3		LSB
Load Regulation, 10mA	REG	Code 512 or V_{CC}/2, I_{OUT} = +5mA to –5mA Step		0.5	1.5	mV/mA
OTP MEMORY						
Number of OTP Write Cycles					16	Cycles
Memory Retention				100		Years
ANALOG POWER SUPPLY						
Operating Range			9		20	V
Total Analog Supply Current	I_S	Outputs at Reset Values, No Load		4.6	7	mA
Over Temperature					**9**	**mA**
DIGITAL						
Logic 1 Input Voltage	V_{IH}		0.7 × V_{SD}		6	V
Logic 0 Input Voltage	V_{IL}		–0.5		0.3 × V_{SD}	V
Logic 0 Output Voltage	V_{OL}	I_{SINK} = 3mA		0.15	0.4	V
Input Leakage				±0.01	±10	µA
Clock Frequency	**f_{CLK}**	**Standard/Fast Mode**			**400**	**kHz**
		High-Speed Mode			**3.4**	**MHz**
DIGITAL POWER SUPPLY						
Operating Range	V_{SD}		2.0		5.5	V
Digital Supply Current(2)	I_{SD}	Outputs at Reset Values, No Load, Two-Wire Bus Inactive		115	150	µA
Over Temperature				**115**		**µA**
TEMPERATURE RANGE						
Specified Range			–40		+85	°C
Operating Range		Junction Temperature < +125°C	–40		+95	°C
Storage Range			–65		+150	°C
Thermal Resistance(3)	θ_{JA}					
HTSSOP-20		See Note (2)		+40		°C/W

(1) BUF08821B output swing is limited internally. Bits 7, 8, and 9 are fixed at '011'.
(2) Observe maximum junction temperature limit.
(3) Thermal pad attached to printed circuit board (PCB), 0lfm airflow, and 76mm × 76mm copper area.

PIN CONFIGURATION

PWP PACKAGE
HTSSOP-28
(TOP VIEW)



(1) NC = no connection.

(2) GND_A and GND_D must be connected together.

PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1	V_{COM}	V_{COM} channel
2	OUT1	DAC output 1
3	OUT2	DAC output 2
4	OUT3	DAC output 3
5	OUT4	DAC output 4
6	V_S	V_S connected to analog supply
7	GND_A	Analog ground; must be connected to digital ground (GND_D)
8	V_{SD}	Digital supply; connect to logic supply
9	SCL	Serial clock input; open-drain, connect to pull-up resistor
10	SDA	Serial data I/O; open-drain, connect to pull-up resistor
11	A0	A0 address pin for I^2C address; either connect to logic 1 or logic 0 (see Table 1)
12	BKSEL	Selects memory bank 0 or 1; either connect to logic 1 to select bank 1 or logic 0 to select bank 0
13	GND_D	Digital ground; must be connected to analog ground at the BUF08821
14	OUT5	DAC output 5
15	V_S	V_S connected to analog supply
16	GND_A	Analog ground
17	OUT6	DAC output 6
18	OUT7	DAC output 7
19	OUT8	DAC output 8
20	NC	This pin is not internally connected

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +18V, V_{SD} = +2V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

OUTPUT VOLTAGE vs OUTPUT CURRENT (V_{COM})

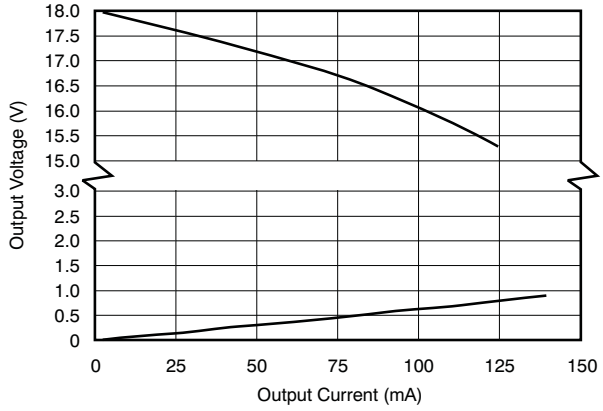


Figure 1.

OUTPUT VOLTAGE vs OUTPUT CURRENT (Channels 1–8)

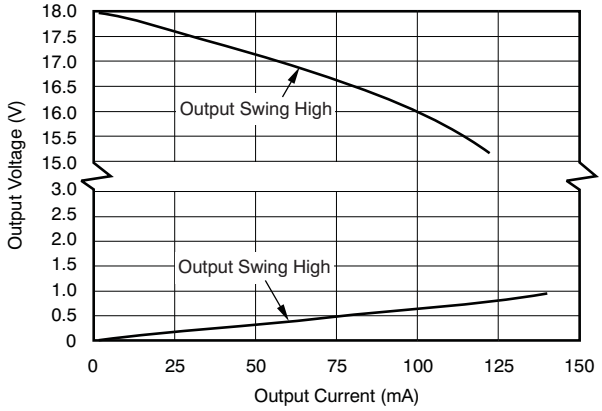


Figure 2.

DIGITAL SUPPLY CURRENT vs TEMPERATURE

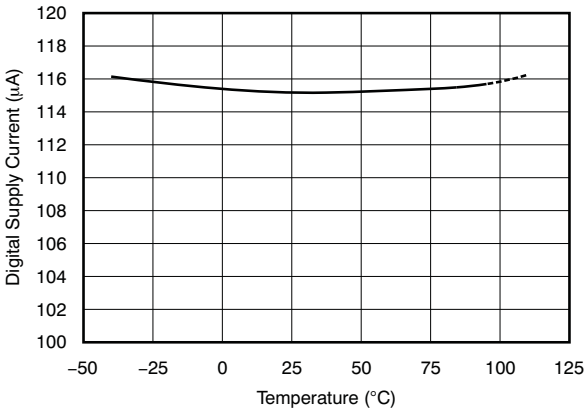


Figure 3.

ANALOG SUPPLY CURRENT vs TEMPERATURE

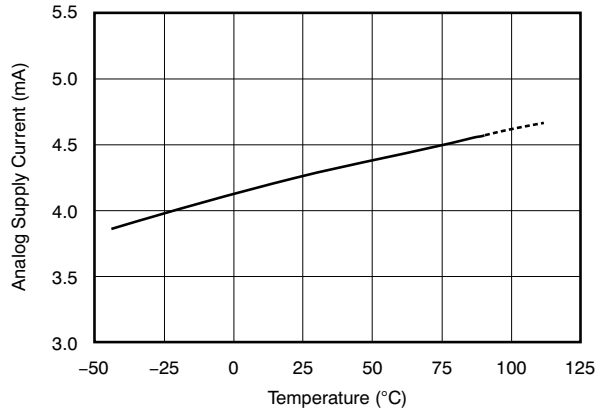


Figure 4.

OUTPUT VOLTAGE vs TEMPERATURE

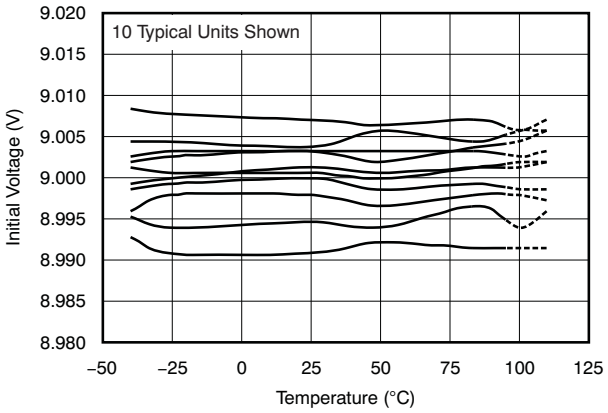


Figure 5.

DIFFERENTIAL LINEARITY ERROR

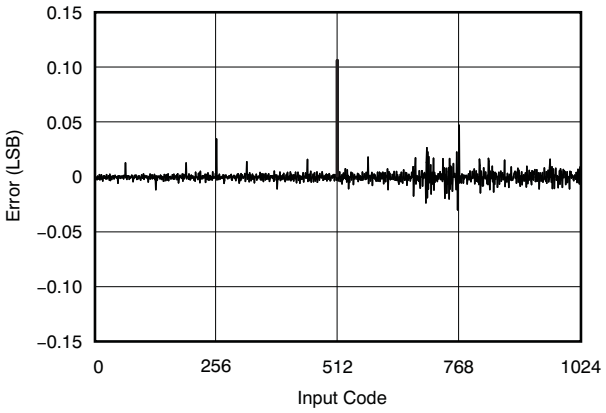


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +18V, V_{SD} = +2V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

INTEGRAL LINEARITY ERROR

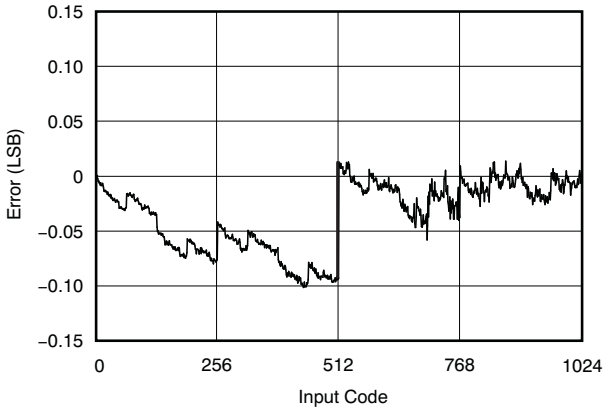


Figure 7.

BKSEL SWITCHING TIME DELAY

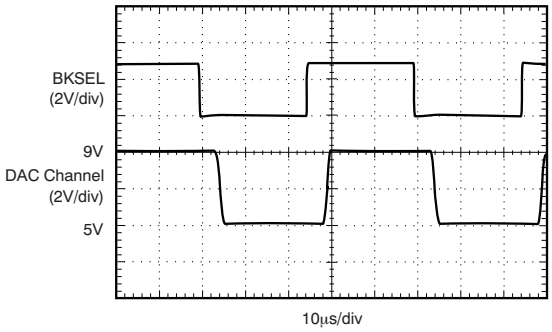


Figure 8.

LARGE-SIGNAL STEP RESPONSE

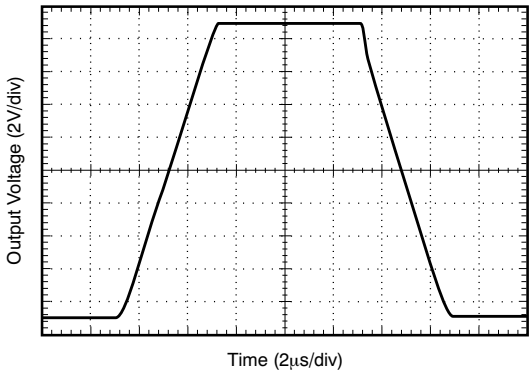


Figure 9.

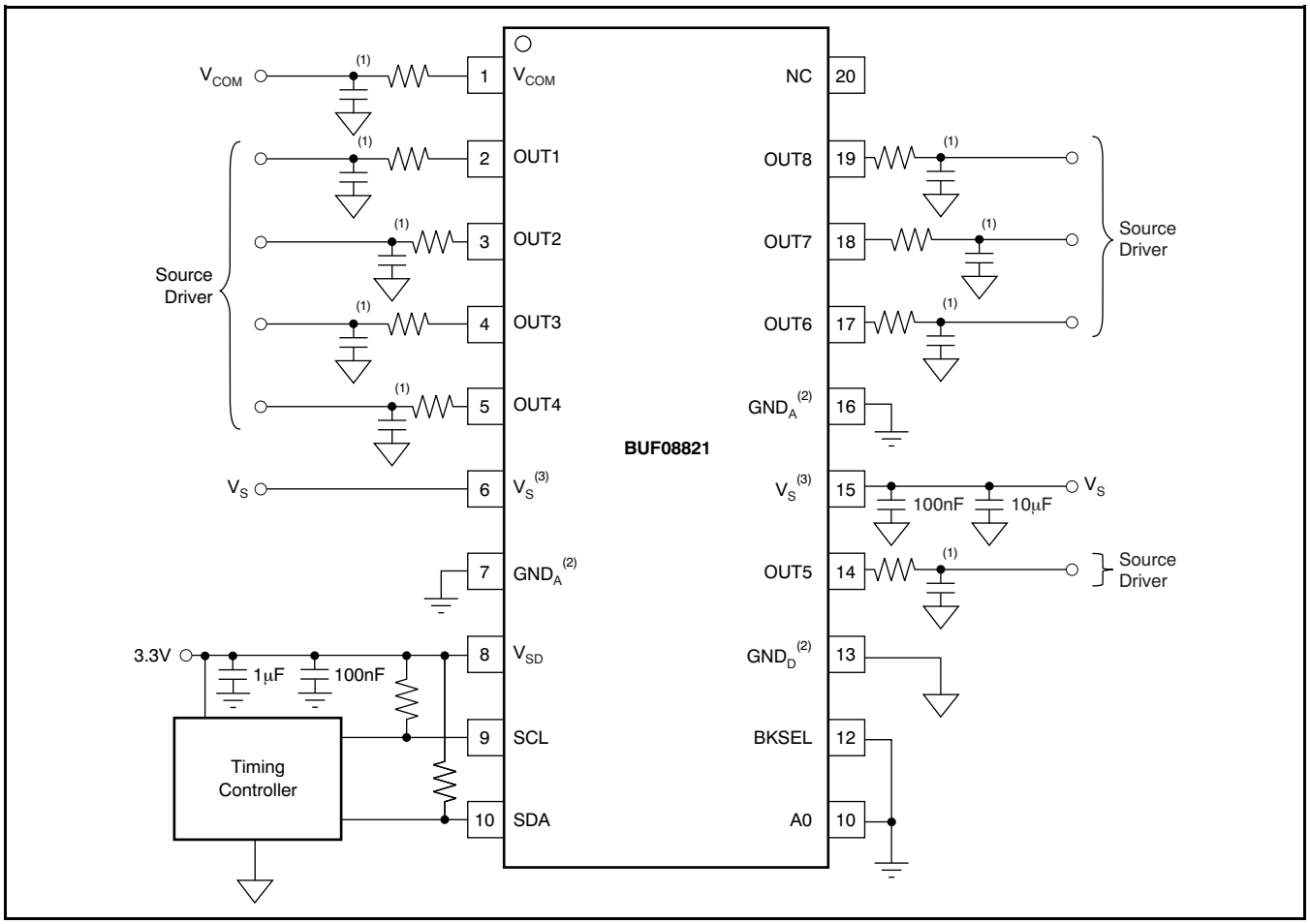
APPLICATION INFORMATION

GENERAL

The BUF08821 programmable voltage reference allows fast and easy adjustment of eight programmable gamma reference outputs and one V_{COM} output, each with 10-bit resolution. The BUF08821 is programmed through a high-speed, I^2C interface. The final gamma and V_{COM} values can be stored in the on-chip, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the BUF08821 supports up to 16 write operations to each word in the on-chip memory. The BUF08821 has two separate memory banks, allowing simultaneous storage of two different gamma curves to facilitate dynamic switching between gamma curves. The BUF08821 also has two storage registers for each digital-to-analog converter (DAC) channel to allow fast switching (less than 10µs) between gamma curves.

At power-on, the BUF08821 first updates all channels to midscale (code 1000000000) and then reads the data for both memory banks into the two sets of storage registers. This read process requires approximately 560µs. After this read is complete, the BUF08821 updates the DACs simultaneously with data for the bank selected by the BKSEL pin.

The BUF08821 can be powered using an analog supply voltage from 9V to 20V, and a digital supply from 2V to 5.5V. The digital supply must be applied before the analog supply to avoid excessive current and power consumption, or possibly even damage to the device if left connected only to the analog supply for extended periods of time. Figure 10 shows a typical configuration of the BUF08821.



(1) RC combination optional; see the *Output Pins ESD Protection Current-Steering Diodes* section.

(2) GND_A and GND_D must be connected together.

(3) Pins 6 and 15 are V_S. The one set of capacitors shown on pin 15 are common to both pins.

Figure 10. Typical Application Configuration

TWO-WIRE BUS OVERVIEW

The BUF08821 communicates over an industry-standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic LOW level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The BUF08821 can act only as a slave device; therefore, it never drives SCL. SCL is an input only for the BUF08821.

ADDRESSING THE BUF08821

The address of the BUF08821 is 111010x, where *x* is the state of the A0 pin. When the A0 pin is LOW, the device acknowledges on address 74h (1110100). If the A0 pin is HIGH, the device acknowledges on address 75h (1110101). Table 1 shows the A0 pin settings and BUF08821 address options.

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 1. Quick-Reference Table of BUF08821 Addresses

BUF08821 ADDRESS:	ADDRESS
A0 pin is LOW (device acknowledges on address 74h)	1110100
A0 pin is HIGH (device acknowledges on address 75h)	1110101

DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF08821 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001 xxx, with SCL = 400kHz, following the START condition; where *xxx* are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. Table 2 provides a reference for the High-speed mode command code. (Note that this configuration is different from normal address bytes—the LOW bit does not indicate read/write status.) The BUF08821 responds to the High-speed command regardless of the value of these last three bits. The BUF08821 does not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. Upon receiving a master code, the BUF08821 switches on its Hs mode filters, and communicates at up to 3.4MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF08821 switches out of Hs mode with the next STOP condition.

Table 2. Quick-Reference Table of Command Codes

COMMAND	CODE
General-Call Reset	Address byte of 00h followed by a data byte of 06h.
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.

GENERAL-CALL RESET AND POWER-UP

The BUF08821 responds to a General-Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF08821 acknowledges both bytes. Table 2 provides a reference for the General-Call Reset command code. Upon receiving a General-Call Reset, the BUF08821 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General-Call address byte of 00h (0000 0000), but does not acknowledge any General-Call data bytes other than 06h (0000 0110).

When the BUF08821 powers up, it automatically performs a reset. As part of the reset, the BUF08821 is configured for all outputs to change to the last programmed nonvolatile memory values, or *1000000000* if the nonvolatile memory values have not been programmed.

OUTPUT VOLTAGE

Buffer output values are determined by the analog supply voltage (V_S) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

$$V_{OUT} = V_S \times \left(\frac{CODE_{10}}{1024} \right) \quad (1)$$

The BUF08821 outputs are capable of a full-scale voltage output change in typically 5µs; no intermediate steps are required.

UPDATING THE DAC OUTPUT VOLTAGES

Because the BUF08821 features a double-buffered register structure, updating the digital-to-analog converter (DAC) and/or the V_{COM} **register** is not the same as updating the DAC and/or V_{COM} **output voltage**. There are two methods for updating the DAC/V_{COM} output voltages.

Method 1: Method 1 is used when it is desirable to have the DAC/V_{COM} output voltage change immediately after writing to a DAC register. For each write transaction, the master sets data bit 15 to a '1'. The DAC/V_{COM} output voltage update occurs after receiving the 16th data bit for the currently-written register.

Method 2: Method 2 is used when it is desirable to have all DAC/V_{COM} output voltages change at the same time. First, the master writes to the desired DAC/V_{COM} channels with data bit 15 a '0'. Then, when writing the last desired DAC/V_{COM} channel, the master sets data bit 15 to a '1'. All DAC/V_{COM} channels are updated at the same time after receiving the 16th data bit.

NONVOLATILE MEMORY

BKSEL Pin

The BUF08821 has 16x rewrite capability for each word in the nonvolatile memory. The BUF08821 has the ability to store two distinct gamma curves in two different nonvolatile memory banks, each of which has 16x rewrite capability. To facilitate fast switching between the two distinct gamma curves, two storage registers are implemented for each DAC channel so that there is no delay as a result of reading the nonvolatile memory when the banks are switched. One of the two available banks is selected using the external input pin, BKSEL. When this pin is LOW, BANK0 is selected; when this pin is HIGH, BANK1 is selected.

When the BKSEL pin changes state, the BUF08821 switches all DAC channels simultaneously from the values in the storage registers for the previously selected bank to the values in the storage registers for the new bank. The storage registers are not updated from the nonvolatile memory. This switching occurs within 5µs of the BKSEL pin state change, and the outputs settle in less than 5µs. The total time to switch from one gamma curve to the other gamma curve is less than 10µs. This fast switching allows for the easy implementation of dynamic gamma correction using the BUF08821.

Data from the nonvolatile memory may be fed into the storage registers by commands issued by the I^2C master. The bank to be acquired by the command from the I^2C master depends on the state of the BKSEL pin. At power-on, the BUF08821 reads the values from the nonvolatile memory into the storage registers. If the I^2C interface is used to update the storage registers through write operations, these values remain in the storage registers until the device powers off, they are overwritten by a write command on the I^2C interface, or a memory acquire command is issued on the I^2C interface. This architecture allows a controller to update the storage registers with two new gamma curves (one in each bank) without updating the nonvolatile memory, and continue to change quickly between the two new gamma curves by using the BKSEL pin.

General Acquire Command

A general acquire command is used to update all registers and DAC/V_{COM} outputs to the last programmed values stored in nonvolatile memory for the selected bank. A single-channel acquire command updates only the register and DAC/V_{COM} output of the DAC/V_{COM} that corresponds to the DAC/V_{COM} address used in the single-channel acquire command.

These are the steps of the sequence to initiate a general channel acquire:

1. BKSEL should be stable throughout the time of a general acquire. Be sure BKSEL is in its desired state, has been stable for at least 20µs, and that any previous general acquire has had time to complete.
2. Send a START condition on the bus.
3. Send the appropriate device address (based on A0) and the read/write bit = LOW. The BUF08821 acknowledges this byte.
4. Send a DAC/V_{COM} pointer address byte. Set bit D7 = 1 and D6 = 0. Bits D5–D0 are any valid DAC/V_{COM} address. The BUF08821 acknowledges, stores, and returns data only from these addresses:
   – 000000 through 000111
   – 010010
   See Table 4 for valid DAC/V_{COM} addresses.
5. Send a STOP condition on the bus.

Approximately 280µs (±30µs) after issuing this command, all DAC/V_{COM} registers and DAC/V_{COM} output voltages change to the respective, appropriate nonvolatile memory values.

The general acquire command only updates storage registers for the selected bank based on the state of the BKSEL pin. To update both banks, it is necessary to change the state of the BKSEL pin and issue another general acquire command.

Single-Channel Acquire Command

These are the steps to initiate a single-channel acquire:

1. BKSEL should be stable throughout the time of a single-channel acquire. Be sure BKSEL is in its desired state, has been stable for at least 20µs, and that any previous single-channel acquire has had time to complete.
2. Send a START condition on the bus.
3. Send the device address (based on A0) and read/write bit = LOW. The BUF08821 acknowledges this byte.
4. Send a DAC/V_{COM} pointer address byte using the DAC/V_{COM} address corresponding to the output and register to update with the OTP memory value. Set bit D7 = 0 and D6 = 1. Bits D5–D0 are the DAC/V_{COM} address. The BUF08821 acknowledges, stores, and returns data only from these addresses:
   – 000000 through 000111
   – 010010
   See Table 4 for valid DAC/V_{COM} addresses.
5. Send a STOP condition on the bus.

Approximately 36µs (±4µs) after issuing this command, the specified DAC/V_{COM} register and DAC/V_{COM} output voltage change to the appropriate OTP memory value.

MaxBank

The BUF08821 can provide the user with the number of times the nonvolatile memory of a particular DAC/V_{COM} channel nonvolatile memory has been written to for the current memory bank. This information is provided by reading the register at pointer address 111111.

There are two ways to update the MaxBank register:

1. After initiating a single acquire command, the BUF08821 updates the MaxBank register with a code corresponding to how many times that particular channel memory has been written to.
2. Following a general acquire command, the BUF08821 updates the MaxBank register with a code corresponding to the maximum number of times the most used channel (OUT1–8 and V_{COM}) has been written to.

MaxBank is a read-only register and is only updated by performing a general- or single-channel acquire.

Table 3 shows the relationship between the number of times the nonvolatile memory has been programmed and the corresponding state of the MaxBank Register.

Table 3. MaxBank Details

NUMBER OF TIMES WRITTEN TO	RETURNS CODE
0	0000
1	0000
2	0001
3	0010
4	0011
5	0100
6	0101
7	0110
8	0111
9	1000
10	1001
11	1010
12	1011
13	1100
14	1101
15	1110
16	1111

Parity Error Correction

The BUF08821 provides single-bit parity error correction for data stored in the nonvolatile memory to provide increased reliability of the nonvolatile memory. If a single bit of nonvolatile memory for a channel fails, the BUF08821 corrects for it and updates the appropriate DAC with the intended value when its memory is acquired.

If more than one bit of nonvolatile memory for a channel fail, the BUF08821 does not correct for it, and updates the appropriate DAC/V_{COM} with the default value of 1000000000.

DIE_ID AND DIE_REV REGISTERS

The user can verify the presence of the BUF08821 in the system by reading from address 111101. The BUF08821A returns *0010001001110101* when read at this address. The BUF08821B returns 0010001001111101 when read at this address.

The user can also determine the die revision of the BUF08821 by reading register 111100. The BUF08821 returns *0000000000000000* when a RevA die is present. RevB would be designated by *0000000000000001*, and so on.

READ/WRITE OPERATIONS

Read and write operations can be done for a single DAC/V_{COM} or for multiple DACs/V_{COM}. Writing to a DAC/V_{COM} register differs from writing to the nonvolatile memory. Bits D15–D14 of the most significant byte of data determines if data are written to the DAC/V_{COM} register or the nonvolatile memory.

Read/Write: DAC/V_{COM} Register (volatile memory)

The BUF08821 is able to read from a single DAC/V_{COM}, or multiple DACs/V_{COM}, or write to the register of a single DAC/V_{COM}, or multiple DACs/V_{COM} in a single communication transaction. DAC pointer addresses begin with 000000 (which corresponds to OUT1) through 000111 (which corresponds to OUT8). Address 010010 is for V_{COM}.

For writes to multiple channels in a single transaction, the register pointer increments directly from 000111 through 010010. This allows all eight gamma channels plus the V_{COM} channel to be updated in one transaction by sending nine words of data.

Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH performs a read transaction.

Writing: DAC/V_{COM} Register (Volatile Memory)

To write to a single DAC/V_{COM} register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08821 acknowledges this byte.
3. Send a DAC/V_{COM} pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC/V_{COM} address. The BUF08821 acknowledges, stores, and returns data only from these addresses:
   - 000000 through 000111
   - 010010

   See Table 4 for valid DAC/V_{COM} addresses.
4. Send two bytes of data for the specified register. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are used, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a STOP or START condition on the bus.

The BUF08821 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register is not updated. Updating the DAC/V_{COM} register is not the same as updating the DAC/V_{COM} output voltage; see the *Output Latch* section.

The process of updating multiple DAC/V_{COM} registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master continues to send data for the next register. The BUF08821 automatically and sequentially steps through subsequent registers as additional data are sent. The process continues until all desired registers have been updated or a STOP or START condition is sent.

To write to multiple DAC/V_{COM} registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08821 acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever DAC/V_{COM} is the first in the sequence of DACs/V_{COM} to be updated. The BUF08821 begins with this DAC/V_{COM} and steps through subsequent DACs/V_{COM} in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15–D8, of which only bits D9 and D8 have meaning, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The first two bytes are for the DAC/V_{COM} addressed in the previous step. The DAC/V_{COM} register is automatically updated after receiving the second byte. The next two bytes are for the following DAC/V_{COM}. That DAC/V_{COM} register is updated after receiving the fourth byte. This process continues until the registers of all following DACs/V_{COM} have been updated. The BUF08821 will continue to accept data for a total of 18 DACs; however, the ten data sets following the 8th data set will be meaningless. The 19th data set will apply to V_{COM}. The write disable bit cannot be accessed using this method. It must be written to using *the write to a single DAC register* procedure.
5. Send a STOP or START condition on the bus.

The BUF08821 acknowledges each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data are updated.

Reading: DAC/V_{COM}/OTHER Register (Volatile Memory)

Reading a register returns the data stored in that DAC/V_{COM}/OTHER register.

To read a single DAC/V_{COM}/OTHER register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08821 acknowledges this byte.
3. Send the DAC/V_{COM}/OTHER pointer address byte. Set bit D7 = 0 and D6 = 0; bits D5–D0 are the DAC/V_{COM}/OTHER address. The BUF08821 acknowledges, stores, and returns data only from these addresses:
   - 000000 through 000111
   - 010010
   - 111100 through 111111

   See Table 4 for valid DAC/V_{COM}/OTHER addresses.
4. Send a START or STOP/START condition.
5. Send the correct device address and read/write bit = HIGH. The BUF08821 acknowledges this byte.
6. Receive two bytes of data. They are for the specified register. The most significant byte (bits D15–D8) is received first; next is the least significant byte (bits D7–D0). In the case of DAC/V_{COM} channels, bits D15–D10 have no meaning.
7. Acknowledge after receiving the first byte.
8. Send a STOP or START condition on the bus or do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not acknowledging.

To read multiple registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08821 acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever register is the first in the sequence of DACs/V_{COM} to be read. The BUF08821 begins with this DAC/V_{COM} and steps through subsequent DACs/V_{COM} in sequential order.
4. Send a START or STOP/START condition on the bus.
5. Send the correct device address and read/write bit = HIGH. The BUF08821 acknowledges this byte.
6. Receive two bytes of data. They are for the specified DAC/V_{COM}. The first received byte is the most significant byte (bits D15–D8, only bits D9 and D8 have meaning), next is the least significant byte (bits D7–D0).
7. Acknowledge after receiving each byte of data.
8. When all desired DACs have been read, send a STOP or START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge bit. The reading of registers DieID, DieRev, and MaxBank is not supported in this mode of operation (they must be read using the single register read method).

The register pointer increments directly from 000111 through 010010 to allow all eight gamma channels plus the V_{COM} channel to be updated in one transaction.

Write: Nonvolatile Memory for the DAC Register

The BUF08821 is able to write to the nonvolatile memory of a single DAC/V_{COM} in a single communication transaction. In contrast to the BUF20820, writing to multiple nonvolatile memory words in a single transaction is not supported. Valid DAC/V_{COM} pointer addresses begin with 000000 (which corresponds to OUT1) through 000111 (which corresponds to OUT8). Address 010010 is for V_{COM}.

When programming the nonvolatile memory, the analog supply voltage must be between 9V and 20V. Write commands are performed by setting the read/write bit low.

To write to a single nonvolatile register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08821 acknowledges this byte. The BUF08821 acknowledges, stores, and returns data only from these addresses:
   - 000000 through 000111
   - 010010

   See Table 4 for DAC/V_{COM} addresses.
3. Send a DAC/V_{COM} pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC/V_{COM} address.
4. Send two bytes of data for the nonvolatile register of the specified DAC/V_{COM}. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are data bits, and bits D15–D14 must be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF08821 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified nonvolatile register is not updated. Writing a nonvolatile register also updates the DAC/V_{COM} register and output voltage.

The DAC/V_{COM} register and DAC/V_{COM} output voltage are updated immediately, while the programming of the nonvolatile memory takes up to 250µs. Once a nonvolatile register write command has been issued, no communication with the BUF08821 should take place for at least 250µs. Writing or reading over the serial interface while the nonvolatile memory is being written jeopardizes the integrity of the data being stored.

Read: Nonvolatile Memory for the DAC Register

To read the data present in nonvolatile register for a particular DAC/V_{COM} channel, the master must first issue a general acquire command, or a single acquire command with the appropriate DAC/V_{COM} channel chosen. This action updates both the DAC/V_{COM} register(s) and DAC/V_{COM} output voltage(s). The master may then read from the appropriate DAC/V_{COM} register as described earlier.

Table 4. DAC Register Pointer Addresses

DAC REGISTER	POINTER ADDRESS
OUT1	000000
OUT2	000001
OUT3	000010
OUT4	000011
OUT5	000100
OUT6	000101
OUT7	000110
OUT8	000111
V_{COM}	010010
OTHER REGISTER	**POINTER ADDRESS**
Die_Rev	111100
Die_ID	111101
MaxBank	111111

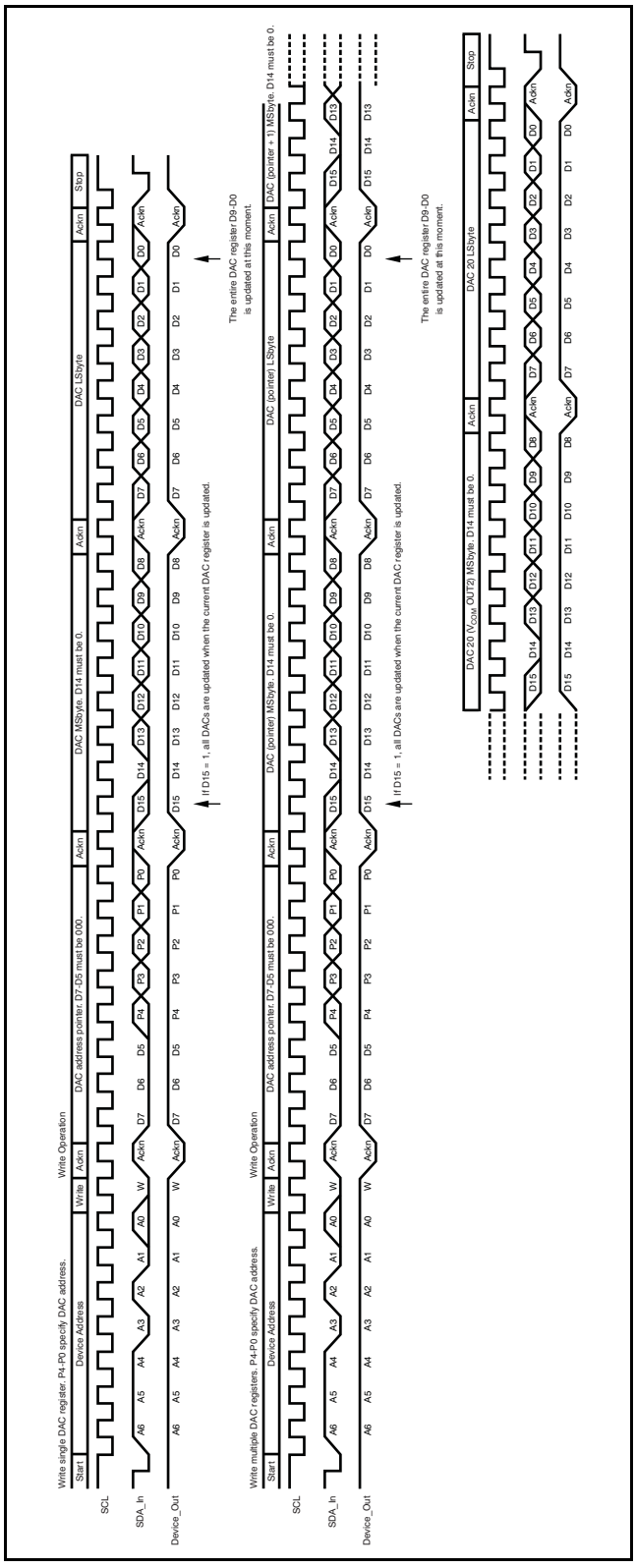


Figure 11. Write DAC Register Timing

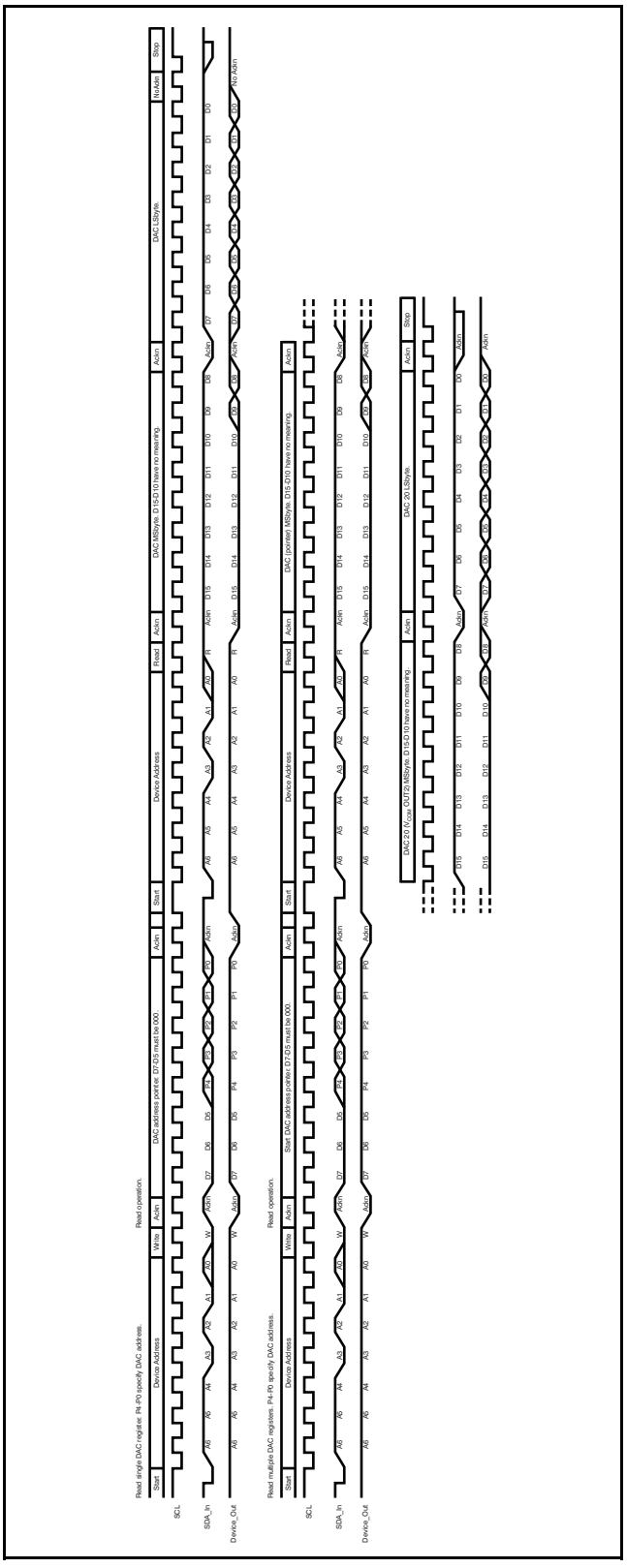


Figure 12. Read Register Timing

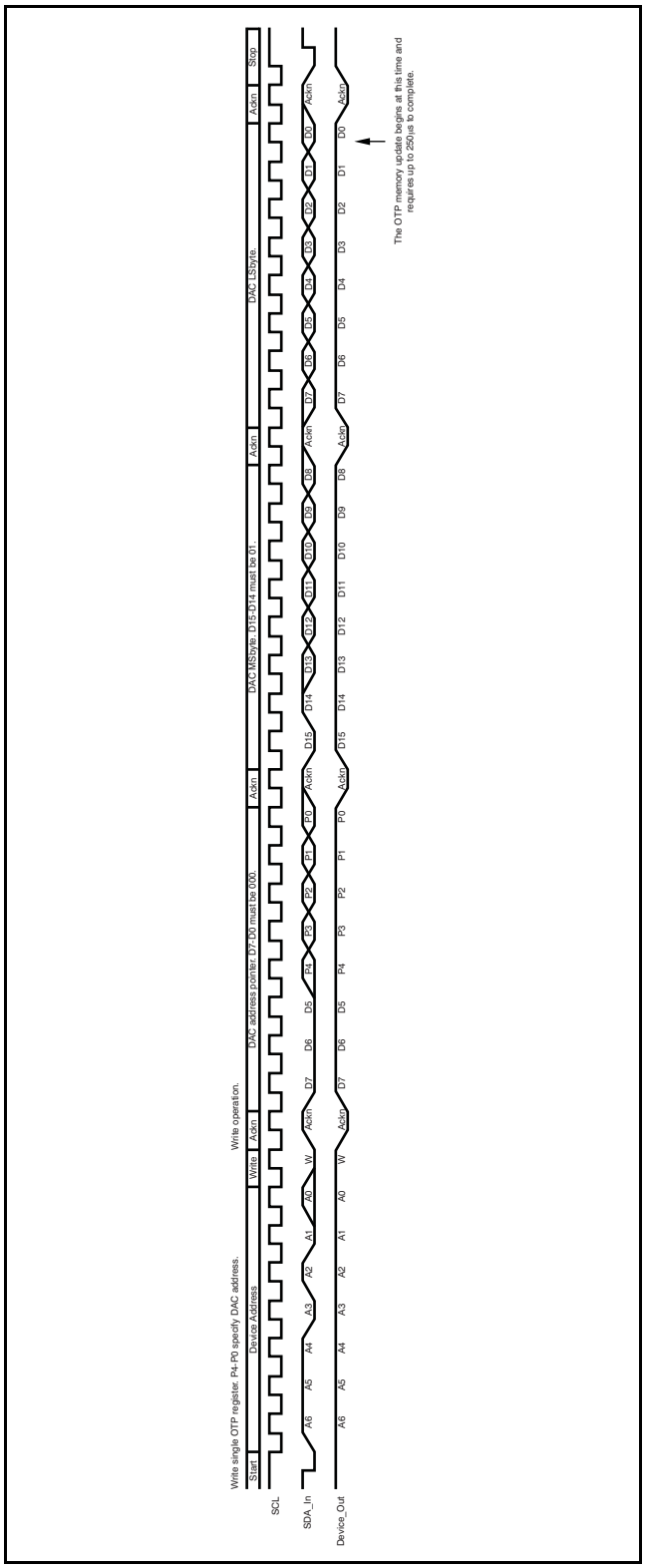


Figure 13. Write Nonvolatile Register Timing

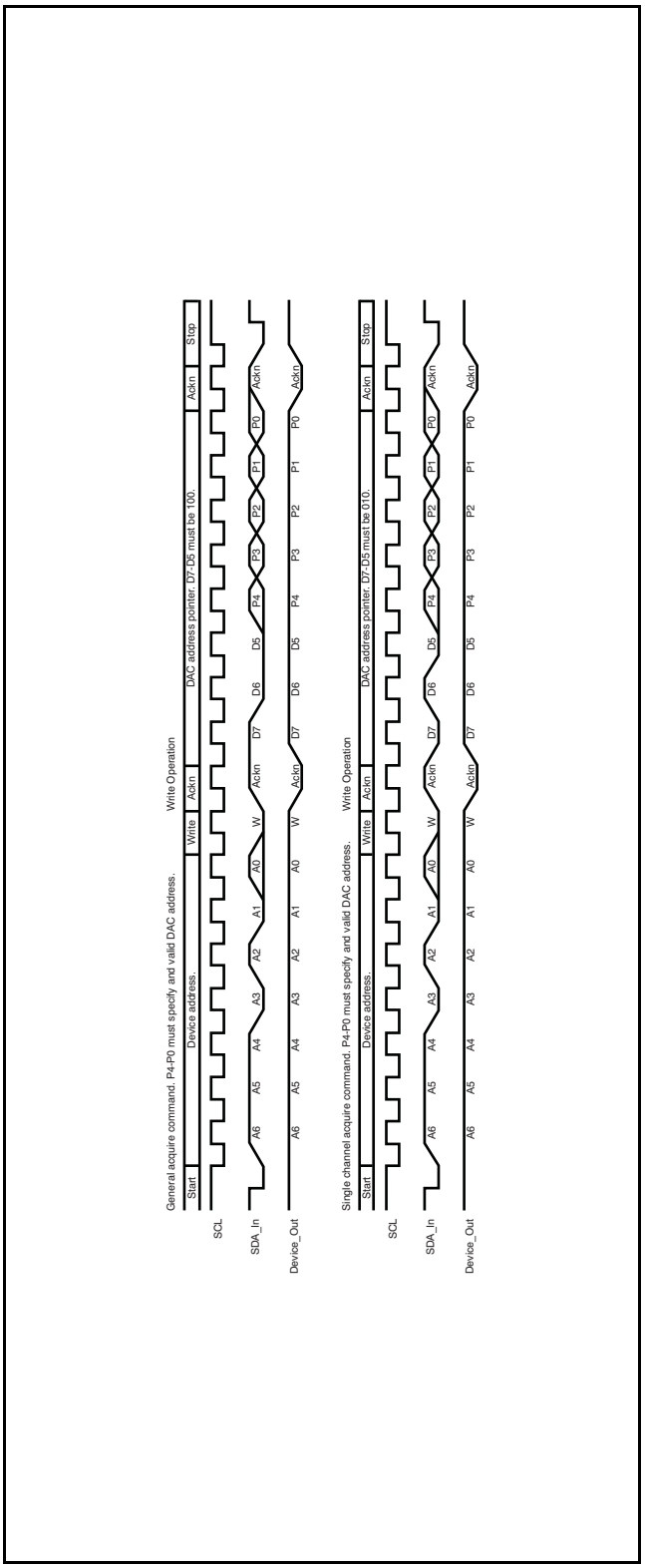


Figure 14. Acquire Operation Timing

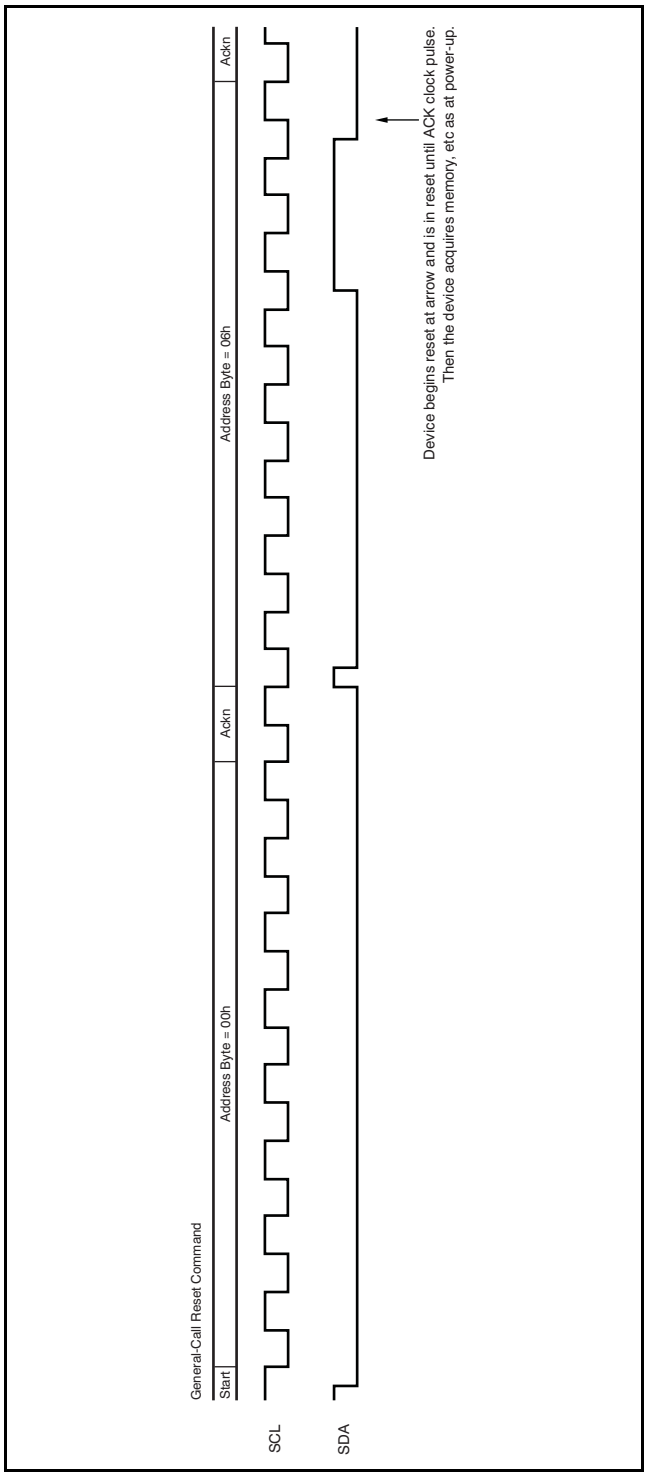


Figure 15. General-Call Reset Timing

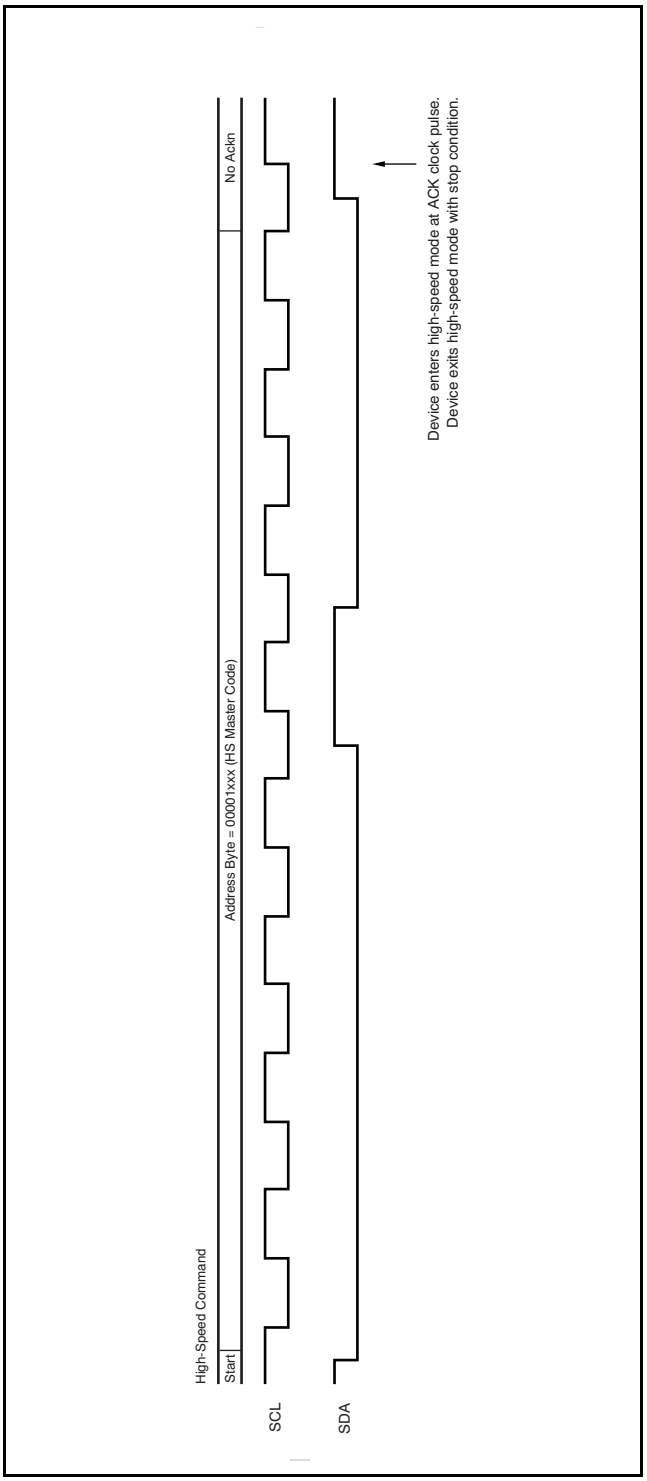


Figure 16. High-Speed Mode Timing

END-USER SELECTED GAMMA CONTROL

Because the BUF08821 has two banks of nonvolatile memory, it is well-suited for providing two levels of gamma control by using the BKSEL pin, as shown in Figure 17. When the state of the BKSEL pin changes, the BUF08821 updates all 9 programmable buffer outputs simultaneously in less than 10µs.

To update all nine programmable output voltages simultaneously via hardware; use this procedure:

Toggle the BKSEL pin to switch between Gamma Curve 0 (stored in Bank0) and Gamma Curve 1 (stored in Bank1).

All DAC/V_{COM} registers update in less than 5µs, and all output voltages settle within the next 5µs.

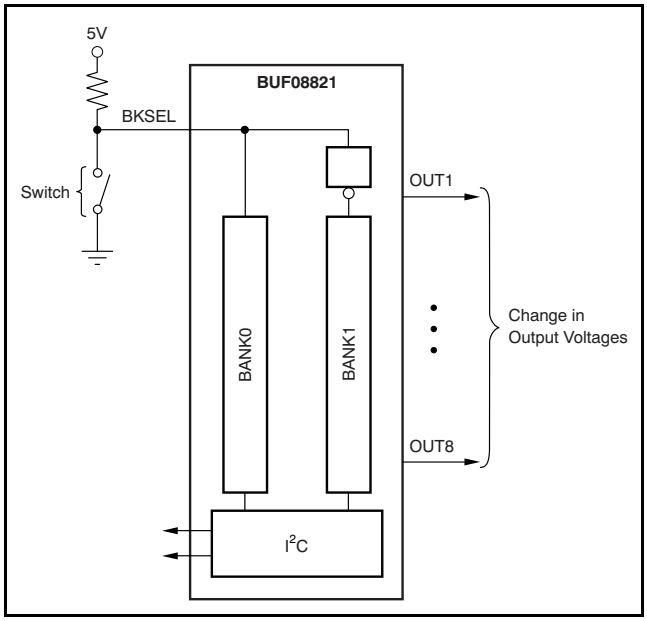


Figure 17. Gamma Control

DYNAMIC GAMMA CONTROL

Dynamic gamma control is a technique used to improve the picture quality in LCD television applications. This technique typically requires switching gamma curves between frames. The BUF08821 is well-suited to implementing dynamic gamma control. The BUF08821 has two banks of nonvolatile memory (one for each gamma curve), and two sets of storage registers (one for each gamma curve). The BKSEL pin enables the device to switch between gamma curves; the BUF08821 outputs fully settled within 10µs.

The BUF08821 reads gamma curve data from each nonvolatile memory bank into the respective storage registers upon power-on. The BKSEL pin toggles between the two gamma curves. It is also possible to update the gamma curves by writing new data to the storage registers via the I^2C interface. The BKSEL pin toggles between the new gamma curves after the data is updated. The gamma curve data in the nonvolatile memory may be restored for each curve individually by issuing a general acquire command for the desired bank. To restore both curves, a general acquire command must be issued for each bank.

OUTPUT PROTECTION

The BUF08821 output stages can safely source and sink the current levels indicated in Figure 1 and Figure 2. However, there are other modes where precautions must be taken to prevent to the output stages from being damaged by excessive current flow. The outputs (OUT1 through OUT8 and the V_{COM}) include ESD protection diodes, as shown in Figure 18. Normally, these diodes do not conduct and are passive during typical device operation. Unusual operating conditions can occur where the diodes may conduct, potentially subjecting them to high, even damaging current levels. These conditions are most likely to occur when a voltage applied to an output exceeds (V_S) + 0.5V, or drops below GND – 0.5V.

One common scenario where this condition can occur is when the output pin is connected to a sufficiently large capacitor, and the BUF08821 power-supply source (V_S) is suddenly removed. Removing the power-supply source allows the capacitor to discharge through the current-steering diodes. The energy released during the high current flow period causes the power dissipation limits of the diode to be exceeded. Protection against the high current flow may be provided by placing current-limiting resistors in series with the output, as shown in Figure 10. Select a resistor value that restricts the current level to the maximum rating for the particular pin.

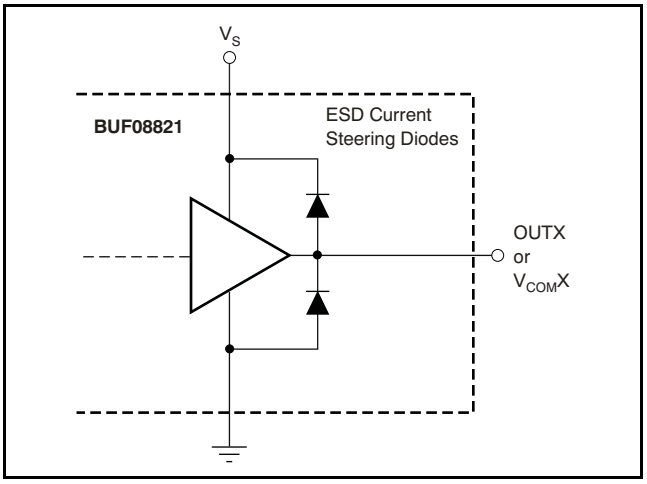


Figure 18. Output Pins ESD Protection Current-Steering Diodes

GENERAL POWERPAD DESIGN CONSIDERATIONS

The BUF08821 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted; see Figure 19(a) and Figure 19(b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 19(c). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. This technique provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device, GND_A and GND_D.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns for the HTSSOP-20 PWP package can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* (SLMA002), available for download at www.ti.com. These holes should be 13 mils (0,33mm) in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. An example thermal land pattern mechanical drawing is attached to the end of this data sheet.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area to help dissipate the heat generated by the BUF08821 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.
5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This configuration makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF08821 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its twelve holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, simply place the BUF08821 IC in position and run the chip through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

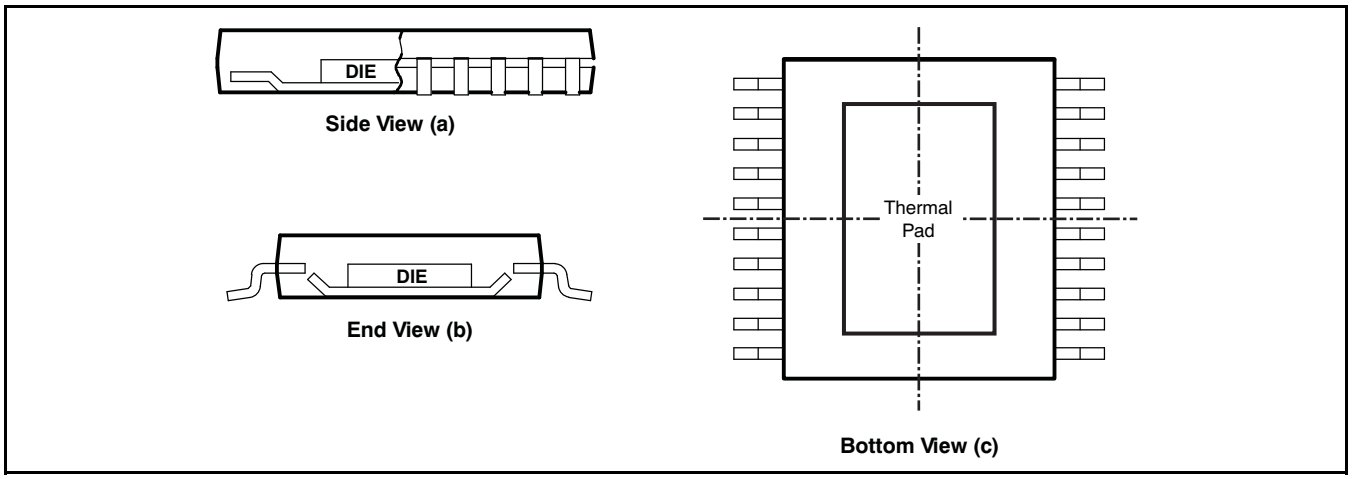


Figure 19. Views of Thermally-Enhanced PWP Package

For a given θ_{JA} (listed in the Electrical Characteristics table), the maximum power dissipation is shown in Figure 20, and is calculated by Equation 2:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right) \quad (2)$$

Where:

P_D = maximum power dissipation (W)

T_{MAX} = absolute maximum junction temperature (+125°C)

T_A = free-ambient air temperature (°C)

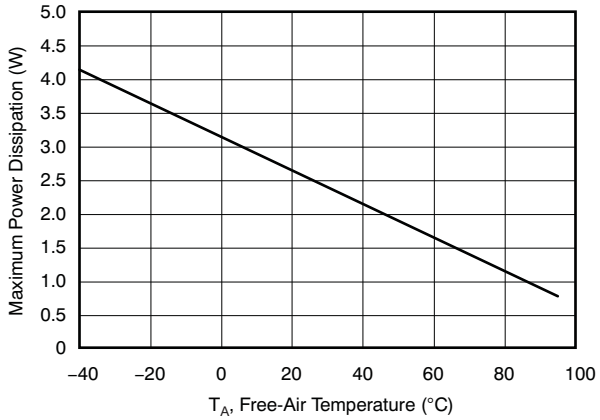


Figure 20. Maximum Power Dissipation vs Free-Air Temperature (with PowerPAD soldered down)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August. 2009) to Revision D **Page**

- Corrected error in x-axis value for Figure 9 6

Changes from Revision B (May, 2009) to Revision C **Page**

- Changed product status from Mixed Status to Production Data 1
- Moved BUF08821B from Product Preview to Production Data 2
- Deleted min and typ specifications for Analog Gamma Buffer Channels, V_{COM}*1, 2 Output Swing: High* parameter of the Electrical Characteristics table 3
- Deleted typ and max specifications for Analog Gamma Buffer Channels, *VCOM1, 2 Output Swing: Low* parameter of the Electrical Characteristics table 3

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BUF08821AIPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 95	BUF08821
BUF08821AIPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 95	BUF08821
BUF08821BIPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 95	BUF8821B
BUF08821BIPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 95	BUF8821B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

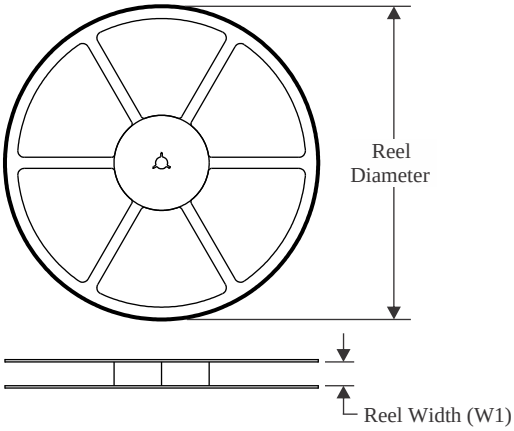
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

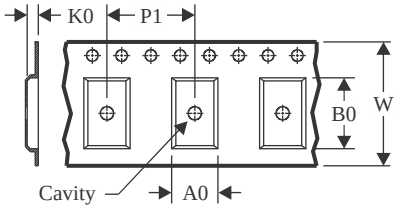
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

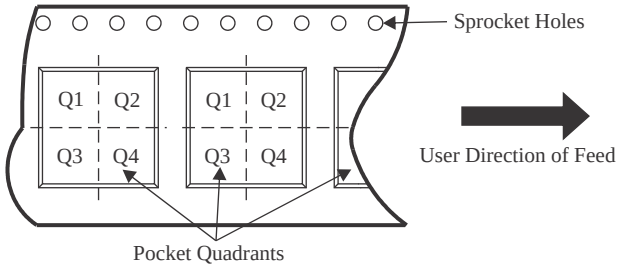


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

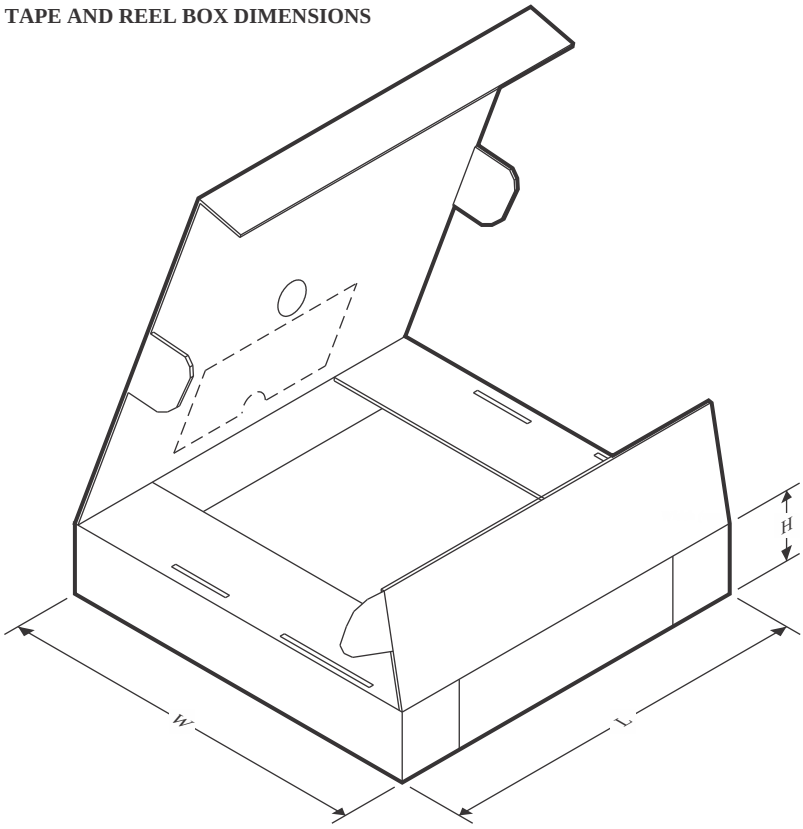
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF08821AIPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BUF08821BIPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF08821AIPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
BUF08821BIPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

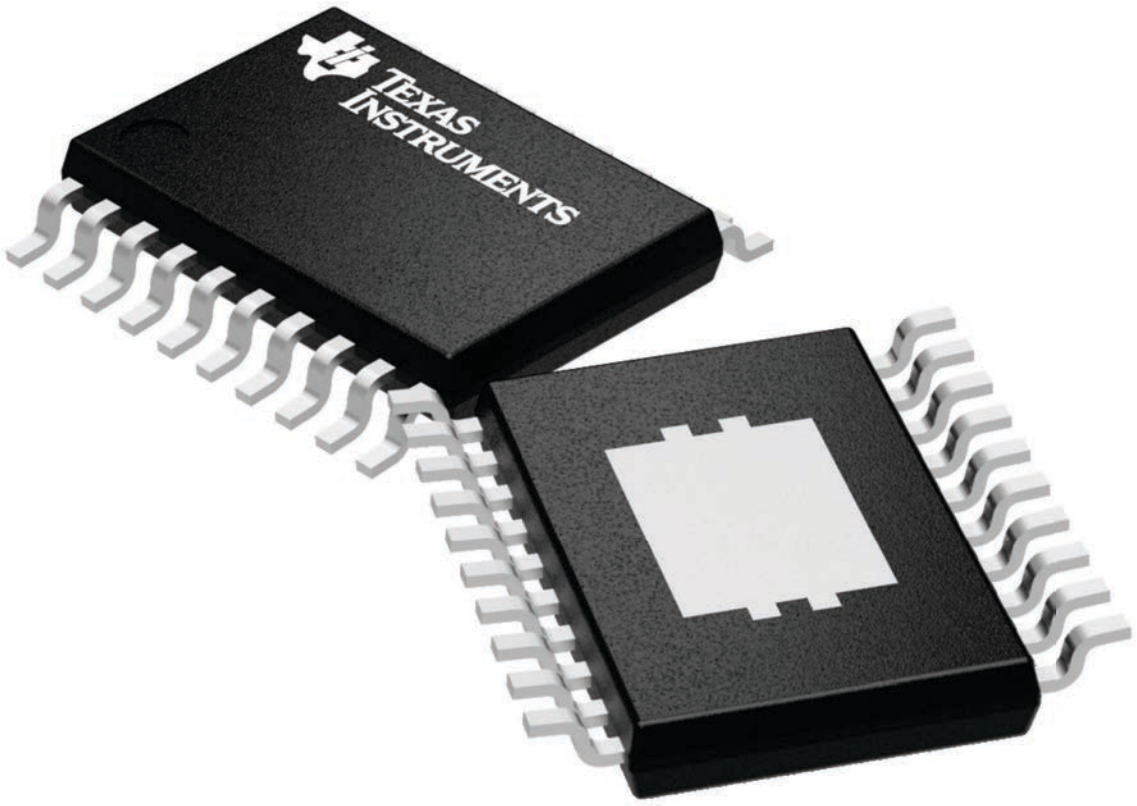
PWP 20

HTSSOP - 1.2 mm max height

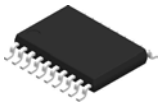
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

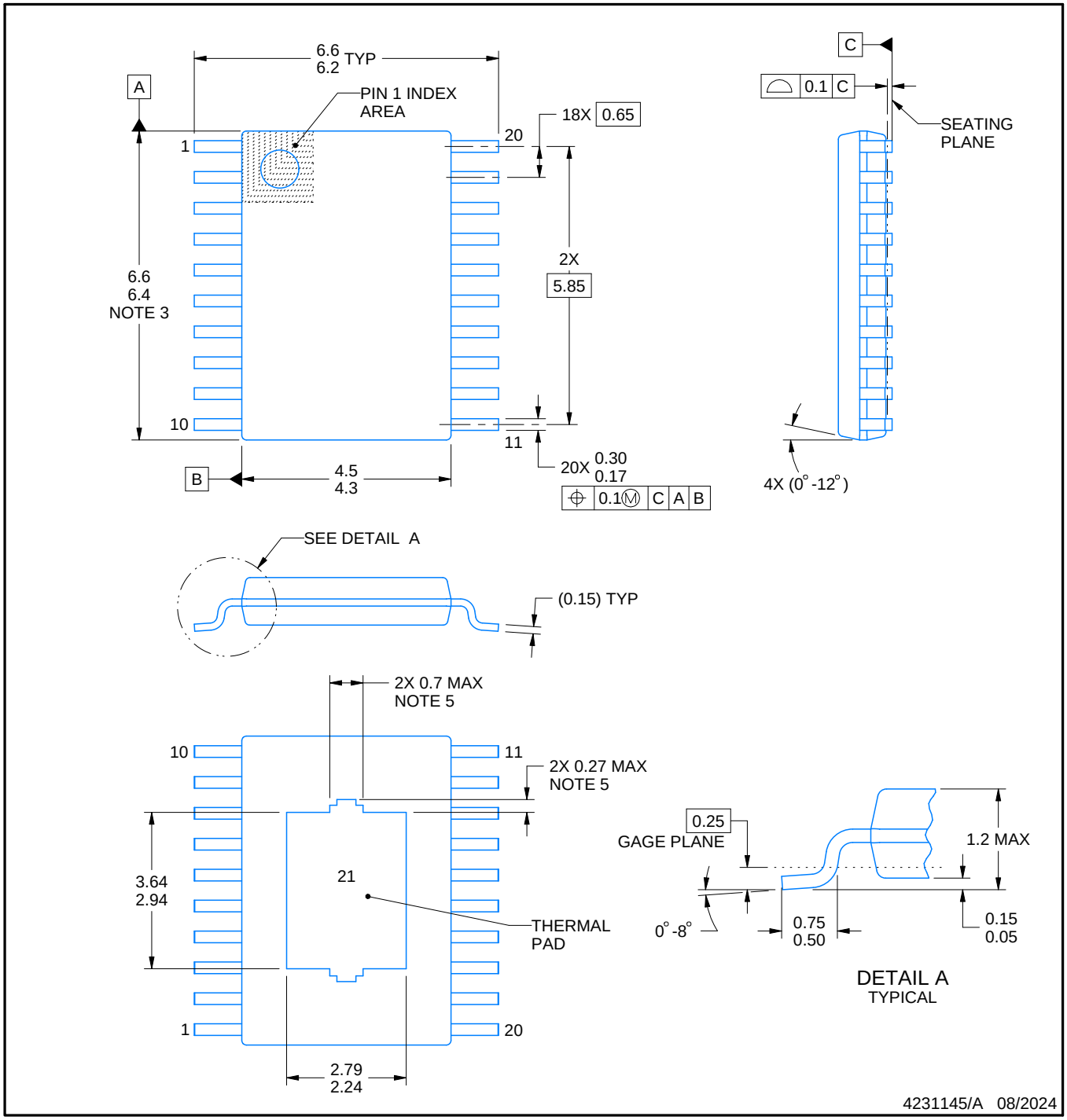


PACKAGE OUTLINE

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

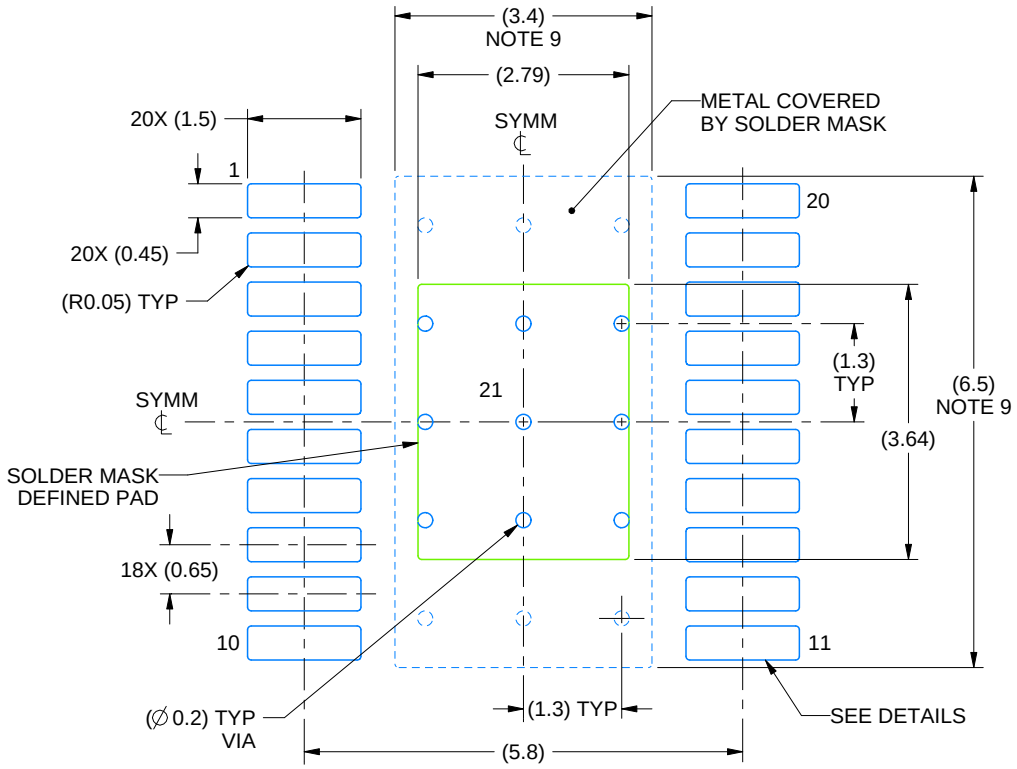
SMALL OUTLINE PACKAGE



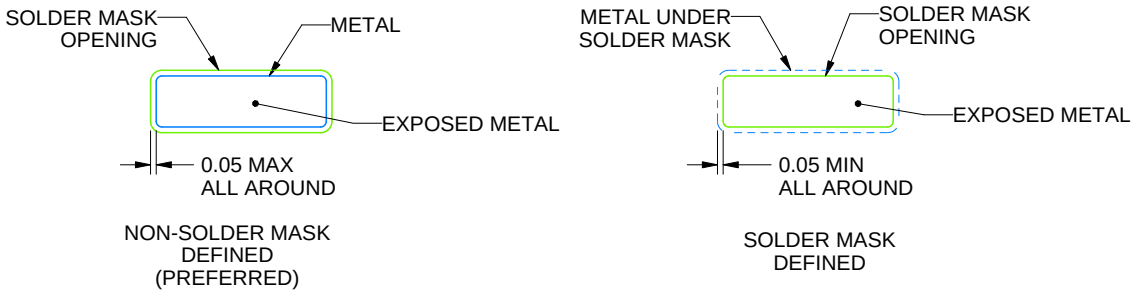
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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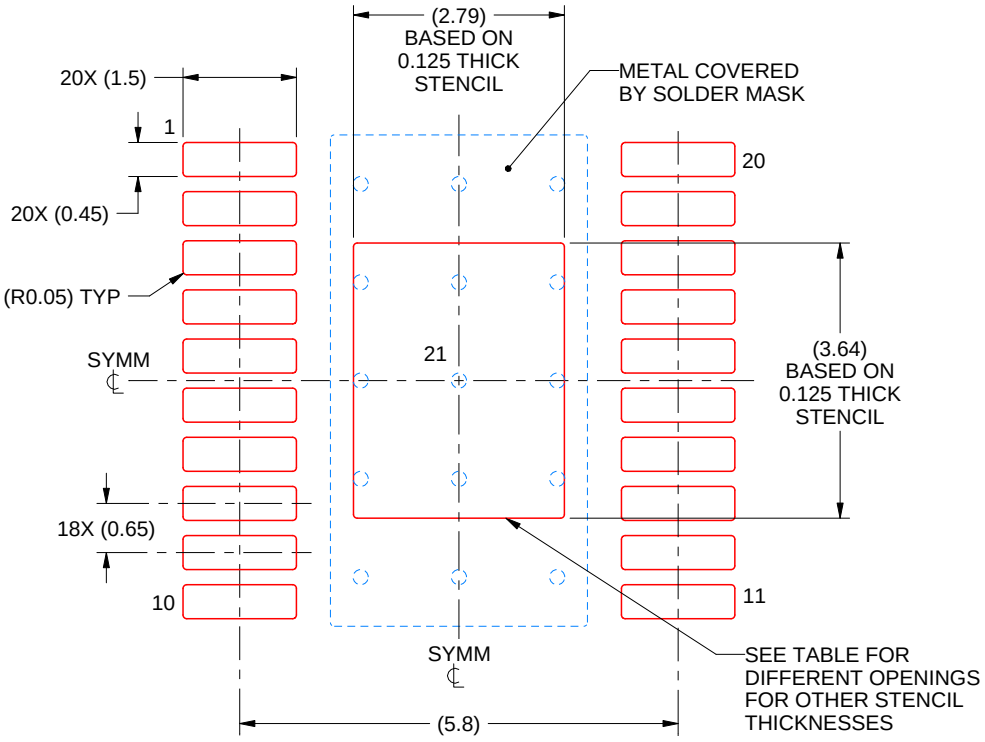
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.12 X 4.07
0.125	2.79 X 3.64 (SHOWN)
0.15	2.55 X 3.32
0.175	2.36 X 3.08

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265