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 Members of the Texas Instruments Widebus™ Family Inputs Are TTL-Voltage Compatible 	54ACT16841 WD PACKAGE 74ACT16841 DGG OR DL PACKAGE (TOP VIEW)
 3-State Outputs Drive Bus Lines Directly 	
 Provide Extra Bus Driving/Latches 	
Necessary for Wider Address/Data Paths or	1Q2 🛛 3 54 🗍 1D2
Buses With Parity	GND 🛛 4 53 🗋 GND
 Flow-Through Architecture Optimizes 	1Q3 🛛 5 52 🖓 1D3
PCB Layout	1Q4 🛛 6 🛛 51 🖸 1D4
 Distributed V_{CC} and GND Pin Configuration 	V _{CC} [] 7 50 [] V _{CC}
Minimizes High-Speed Switching Noise	1Q5 4 8 49 1D5
● EPIC [™] (Enhanced-Performance Implanted	
CMOS) 1-µm Process	
• 500-mA Typical Latch-Up Immunity at	GND 11 46 GND 1Q8 12 45 1D8
125°C	1Q8 12 45 1D8 1Q9 13 44 1D9
Package Options Include Plastic Thin	
Shrink Small-Outline (DGG) Packages,	2Q1 15 42 2D1
300-mil Shrink Small-Outline (DL) Packages	2Q2 [16 41] 2D2
Using 25-mil Center-to-Center Pin	2Q3 17 40 2D3
Spacings, and 380-mil Fine-Pitch Ceramic	GND 18 39 GND
Flat (WD) Packages Using 25-mil	2Q4 🛛 19 38 🕽 2D4
Center-to-Center Pin Spacings	2Q5 🛛 20 37 🕽 2D5
description	2Q6 🛛 21 36 🕽 2D6
uescription	V _{CC} [] 22 35 [] V _{CC}
These 20-bit latches feature 3-state outputs	2Q7 🛛 23 34 🗋 2D7
designed specifically for driving highly capacitive	2Q8 24 33 2D8
or relatively low-impedance loads. They are	GND 25 32 GND
particularly suitable for implementing buffer	2Q9 26 31 2D9

The 'ACT16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

registers, I/O ports, bidirectional bus drivers, and

working registers.

A buffered output-enable $(1\overline{OE} \text{ or } 2\overline{OE})$ input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

2Q10 🛛 27

28

2OE L

30 2D10

29 2LE

OE does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



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54ACT16841, 74ACT16841 20-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS SCAS174A – MAY 1991 – REVISED APRIL 1996

description (continued)

The 74ACT16841 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16841 is characterized for operation over the full military temperature range of -55° C to 125° C. The 74ACT16841 is characterized for operation from -40° C to 85° C.

FUNCTION TABLE
(each 10-bit latch)

	INPUTS	OUTPUT	
OE	LE	D	Q
L	Н	Н	Н
L	н	L	L
L	L	Х	Q ₀
н	Х	Х	Z

logic symbol[†]

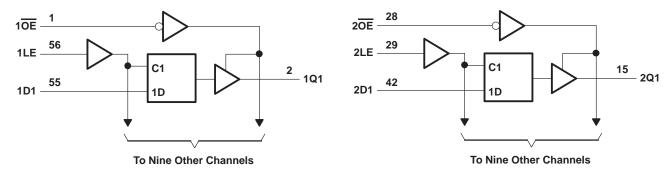
	4		_	
1 <mark>0E</mark>	1	EN2		
1LE	56	C1		
2 <mark>0E</mark>	28	EN4		
2LE	29	C3		
		5	┍┛	
1D1	55	1D 2		2 — 1Q1
1D2	54		-	3 — 1Q2
1D3	52		-	5 — 1Q3
1D3	51			6 — 1Q4
	49	 		8
1D5	48	ļ	-	— 1Q5 9
1D6	47		- 10	- 1Q6
1D7	45		- 1:	— 1Q7
1D8	44		- 1:	— 1Q8
1D9		-		— 1Q9
1D10	43	-	- 1 [,]	4 — 1Q10
2D1	42	3D 4	□ 1	5 — 2Q1
2D2	41		- 10	6 — 2Q2
	40		- 1	7
2D3	38	 	- 1	- 2Q3
2D4	37	ļ	2	2Q4
2D5	36		2	- 2Q5 1
2D6	34		2	— 2Q6 3
2D7	33		2	— 2Q7
2D8		-		— 2Q8
2D9	31	-	- 20	— 2Q9
2D10	30	-	2	7 — 2Q10

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$\dots \dots \dots -0.5$ V to V _{CC} + 0.5 V
Output voltage range, V _O (see Note 1)	–0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±500 mA
Maximum package power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note	2): DGG package 1 W
	DL package 1.4 W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16841			74	41	UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2		4	2			V
VIL	Low-level input voltage		VIV.	0.8			0.8	V
VI	Input voltage	0	RE	VCC	0		VCC	V
Vo	Output voltage	0	7	VCC	0		VCC	V
ЮН	High-level output current		22	-24			-24	mA
IOL	Low-level output current	20°.	5	24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
ТА	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	N	T,	A = 25°0	;	54ACT	16841	74ACT	16841	UNIT
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		4.5 V	4.4			4.4		4.4		
	I _{OH} =–50 μA	5.5 V	5.4			5.4		5.4		
VOH	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.8		3.8		V
	IOH = -24 IIIA	5.5 V	4.94			4.8	2	4.8		
	$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V				3.85	ĬE,	3.85		
	l _{OL} = 50 μA	4.5 V			0.1		Q 0.1		0.1	
	ΙΟΓ = 30 μΑ	5.5 V			0.1	L.	Q 0.1		0.1	V
VOL	lat = 24 mA	4.5 V			0.36	70	0.44		0.44	
	I _{OL} = 24 mA	5.5 V			0.36	00	0.44		0.44	
	$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V				40	1.65		1.65	
lj	$V_{I} = V_{CC} \text{ or } GND$	5.5 V			±0.1		±1		±1	μΑ
I _{OZ}	$V_{O} = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μA
Icc	$V_{I} = V_{CC} \text{ or GND}, \qquad I_{O} = 0$	5.5 V			8		80		80	μA
ΔI_{CC}^{\ddagger}	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			0.9		1		1	mA
Ci	$V_{I} = V_{CC} \text{ or } GND$	5 V		3						pF
Co	$V_{O} = V_{CC} \text{ or } GND$	5 V		11						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

					54ACT16841		74ACT16841		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
tw	Pulse duration, LE high		4		4	6	4		ns
t _{su}	Setup time, data before LE \downarrow		1.5		1.5	N. W	1.5		ns
t.	Hold time, data after LE↓	High	3		3		3		-
^t h		4.5		4.5		4.5		ns	

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	T,	T _A = 25°C			54ACT16841		74ACT16841	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
^t PLH	D	Q	4	7.1	10.3	4	11.8	4	11.8	ns
^t PHL	D	Q	3.2	6.9	11	3.2	12.2	3.2	12.2	115
^t PLH	LE	LE Q		7.7	11.3	4.5	12.7	4.5	12.7	20
^t PHL	LC	Q	4.3	7.8	11.4	4.3	² 12.7	4.3	12.7	ns
^t PZH	OE	0	3.1	6.4	10.1	3.	11.3	3.1	11.3	20
^t PZL	OE	Q	3.8	7.6	12.1	3.8	13.7	3.8	13.7	ns
^t PHZ	OE	0	4	7.3	9.5	2 4	10.2	4	10.2	
^t PLZ	OE	Q	4	6.8	8.9	4	9.6	4	9.6	ns

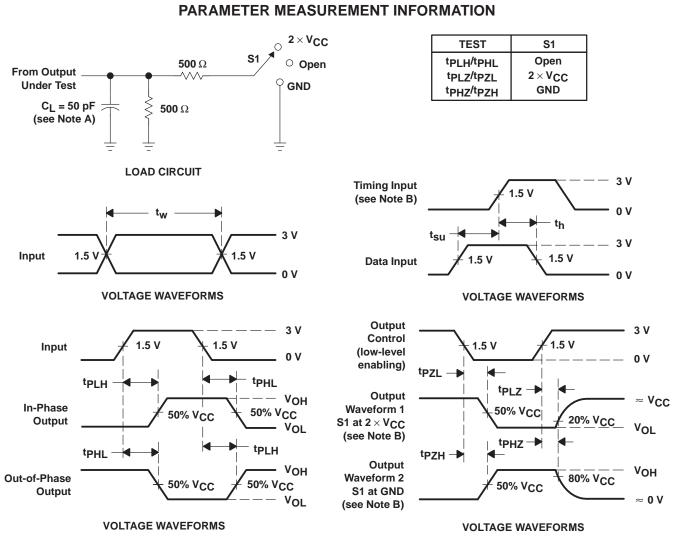
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operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CO	TYP	UNIT	
C _{pd} Power dissipation capacitance	Outputs enabled	C ₁ = 50 pF, f = 1 MHz		41	nE.
		Outputs disabled	CL = 50 pr,		10



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f = 3 ns, t_f = 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
74ACT16841DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16841
74ACT16841DL.A	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16841

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TEXAS INSTRUMENTS

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TUBE



- B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
74ACT16841DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
74ACT16841DL.A	DL	SSOP	56	20	473.7	14.24	5110	7.87

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