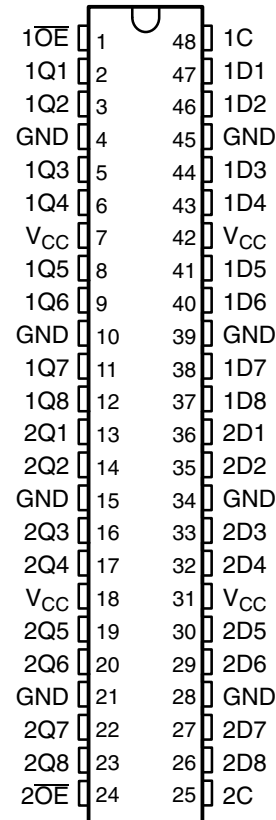


# SN54ACT16373, 74ACT16373 16-BIT D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus*™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Bus Driving True Outputs
- Full Parallel Access for Loading
- Flow-Through Architecture Optimizes PCB Layout
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Shrink Small-Outline (DL) 300-mil Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

SN54ACT16373 . . . WD PACKAGE  
74ACT16373 . . . DL PACKAGE  
(TOP VIEW)



## description

The SN54ACT16373 and 74ACT16373 are 16-bit D-type transparent latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. These devices can be used as two 8-bit latches or one 16-bit latch. The Q outputs of the latches follow the data (D) inputs if enable C is taken high. When C is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16373 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ACT16373 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT16373 is characterized for operation from -40°C to 85°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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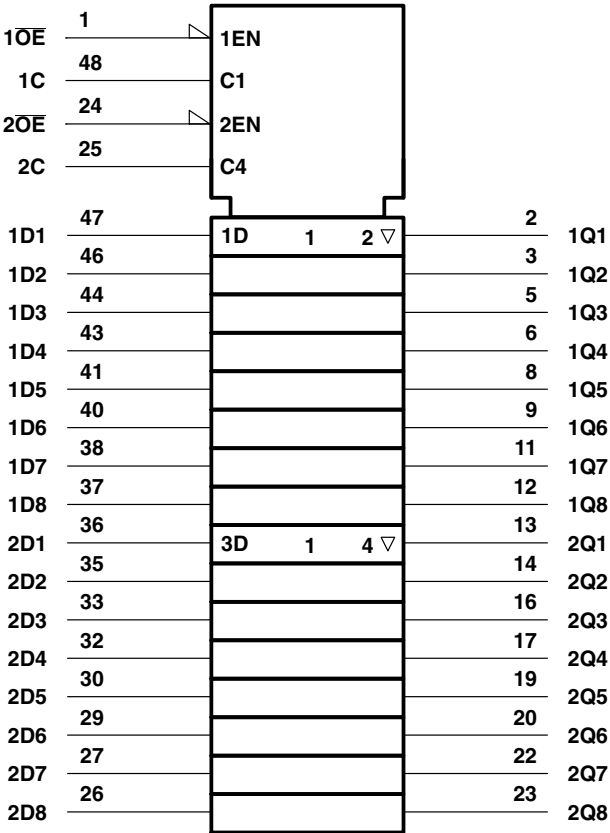
SN54ACT16373, 74ACT16373  
16-BIT D-TYPE TRANSPARENT LATCHES  
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

| INPUTS |   |   | OUTPUT<br>Q    |
|--------|---|---|----------------|
| OE     | C | D |                |
| L      | H | H | H              |
| L      | H | L | L              |
| L      | L | X | Q <sub>0</sub> |
| H      | X | X | Z              |

logic symbol†

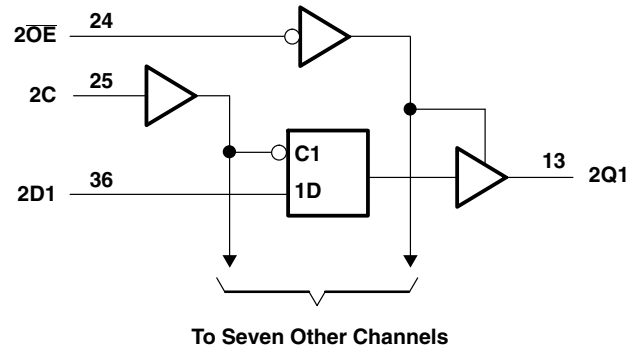
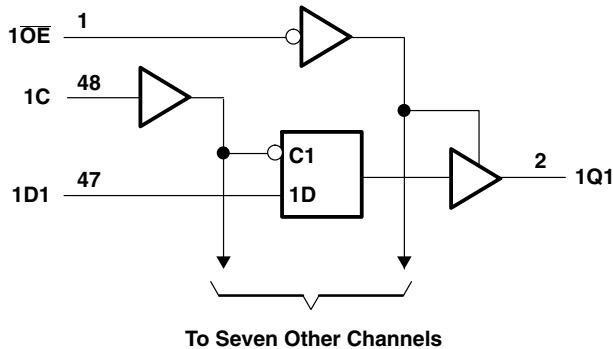


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ACT16373, 74ACT16373 16-BIT D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|   |                            |
|---|----------------------------|
| Supply voltage range, $V_{CC}$  | –0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)   | –0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, $V_O$ (see Note 1)  | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )                                 | ±20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )                                | ±50 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )                                    | ±50 mA                     |
| Continuous current through $V_{CC}$ or GND  | ±400 mA                    |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package | 1.2 W                      |
| Storage temperature range, $T_{stg}$  | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

## recommended operating conditions (see Note 3)

|  | SN54ACT16373 |          | 74ACT16373 |          | UNIT |
|--|--------------|----------|------------|----------|------|
|  | MIN          | MAX      | MIN        | MAX      |      |
| $V_{CC}$ Supply voltage (see Note 4)                   | 4.5          | 5.5      | 4.5        | 5.5      | V    |
| $V_{IH}$ High-level input voltage                      | 2            |          | 2          |          | V    |
| $V_{IL}$ Low-level input voltage                       |              | 0.8      |            | 0.8      | V    |
| $V_I$ Input voltage                                    | 0            | $V_{CC}$ | 0          | $V_{CC}$ | V    |
| $V_O$ Output voltage                                   | 0            | $V_{CC}$ | 0          | $V_{CC}$ | V    |
| $I_{OH}$ High-level output current                     |              | –24      |            | –24      | mA   |
| $I_{OL}$ Low-level output current                      |              | 24       |            | 24       | mA   |
| $\Delta t/\Delta v$ Input transition rise or fall rate | 0            | 10       | 0          | 10       | ns/V |
| $T_A$ Operating free-air temperature                   | –55          | 125      | –40        | 85       | °C   |

- NOTES: 3. Unused inputs should be tied to  $V_{CC}$  through a pullup resistor of approximately 5 k $\Omega$  or greater to prevent them from floating.  
4. All  $V_{CC}$  and GND pins must be connected to the proper voltage supply.

# SN54ACT16373, 74ACT16373

## 16-BIT D-TYPE TRANSPARENT LATCHES

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                     | TEST CONDITIONS   | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |      | SN54ACT16373 |      | 74ACT16373 |      | UNIT |
|-------------------------------|---|-----------------|-----------------------|-----|------|--------------|------|------------|------|------|
|                               |   |                 | MIN                   | TYP | MAX  | MIN          | MAX  | MIN        | MAX  |      |
| V <sub>OH</sub>               | I <sub>OH</sub> = -50 µA                                      | 4.5 V           | 4.4                   |     |      | 4.4          |      | 4.4        |      | V    |
|                               |   | 5.5 V           | 5.4                   |     |      | 5.4          |      | 5.4        |      |      |
|                               | I <sub>OH</sub> = -24 mA                                      | 4.5 V           | 3.94                  |     |      | 3.7          |      | 3.8        |      |      |
|                               |   | 5.5 V           | 4.94                  |     |      | 4.7          |      | 4.8        |      |      |
|                               | I <sub>OH</sub> = -50 mA <sup>†</sup>                         | 5.5 V           |                       |     |      | 3.85         |      |            |      |      |
|                               | I <sub>OH</sub> = -75 mA <sup>†</sup>                         | 5.5 V           |                       |     |      |              |      | 3.85       |      |      |
| V <sub>OL</sub>               | I <sub>OL</sub> = 50 µA                                       | 4.5 V           |                       |     | 0.1  |              | 0.1  |            | 0.1  | V    |
|                               |   | 5.5 V           |                       |     | 0.1  |              | 0.1  |            | 0.1  |      |
|                               | I <sub>OL</sub> = 24 mA                                       | 4.5 V           |                       |     | 0.36 |              | 0.5  |            | 0.44 |      |
|                               |   | 5.5 V           |                       |     | 0.36 |              | 0.5  |            | 0.44 |      |
|                               | I <sub>OL</sub> = 50 mA <sup>†</sup>                          | 5.5 V           |                       |     |      |              | 1.65 |            |      |      |
|                               | I <sub>OL</sub> = 75 mA <sup>†</sup>                          | 5.5 V           |                       |     |      |              |      |            | 1.65 |      |
| I <sub>I</sub>                | V <sub>I</sub> = V <sub>CC</sub> or GND                       | 5.5 V           |                       |     | ±0.1 |              | ±1   |            | ±1   | µA   |
| I <sub>OZ</sub>               | V <sub>O</sub> = V <sub>CC</sub> or GND                       | 5.5 V           |                       |     | ±0.5 |              | ±10  |            | ±5   | µA   |
| I <sub>CC</sub>               | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0   | 5.5 V           |                       |     | 8    |              | 160  |            | 80   | µA   |
| ΔI <sub>CC</sub> <sup>‡</sup> | One input at 3.4 V,<br>Other inputs at GND or V <sub>CC</sub> | 5.5 V           |                       |     | 0.9  |              | 1    |            | 1    | mA   |
| C <sub>i</sub>                | V <sub>I</sub> = V <sub>CC</sub> or GND                       | 5 V             |                       | 4.5 |      |              |      |            |      | pF   |
| C <sub>o</sub>                | V <sub>I</sub> = V <sub>CC</sub> or GND                       | 5 V             |                       | 12  |      |              |      |            |      | pF   |

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V<sub>CC</sub>.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

|                 |                             | T <sub>A</sub> = 25°C |     | SN54ACT16373 |     | 74ACT16373 |     | UNIT |
|-----------------|-----------------------------|-----------------------|-----|--------------|-----|------------|-----|------|
|                 |                             | MIN                   | MAX | MIN          | MAX | MIN        | MAX |      |
| t <sub>w</sub>  | Pulse duration, LE high     | 4                     |     | 4            |     | 1          |     | ns   |
| t <sub>su</sub> | Setup time, data before LE↓ | 1                     |     | 1            |     | 1          |     | ns   |
| t <sub>h</sub>  | Hold time, data after LE↓   | 5                     |     | 5            |     | 5          |     | ns   |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | T <sub>A</sub> = 25°C |     |      | SN54ACT16373 |      | 74ACT16373 |      | UNIT |
|------------------|--------------|-------------|-----------------------|-----|------|--------------|------|------------|------|------|
|                  |              |             | MIN                   | TYP | MAX  | MIN          | MAX  | MIN        | MAX  |      |
| t <sub>PLH</sub> | D            | Q           | 3.8                   | 7.9 | 9.4  | 3.8          | 11.8 | 3.8        | 11.1 | ns   |
| t <sub>PHL</sub> |              |             | 3.1                   | 8.2 | 9.7  | 3.1          | 13   | 3.1        | 12.3 |      |
| t <sub>PLH</sub> | LE           | Q           | 4.6                   | 9.3 | 10.8 | 4.6          | 13.7 | 4.6        | 12.8 | ns   |
| t <sub>PHL</sub> |              |             | 4.5                   | 9.1 | 10.5 | 4.5          | 13   | 4.5        | 12.2 |      |
| t <sub>PZH</sub> | OE           | Q           | 3.1                   | 8   | 9.5  | 3.1          | 13   | 3.1        | 12.1 | ns   |
| t <sub>PZL</sub> |              |             | 3.8                   | 9.4 | 11.1 | 3.8          | 15.1 | 3.8        | 14.2 |      |
| t <sub>PHZ</sub> | OE           | Q           | 5.3                   | 8.6 | 9.9  | 5.3          | 11   | 5.3        | 10.7 | ns   |
| t <sub>PLZ</sub> |              |             | 4.3                   | 7.4 | 8.7  | 4.3          | 9.8  | 4.3        | 9.4  |      |



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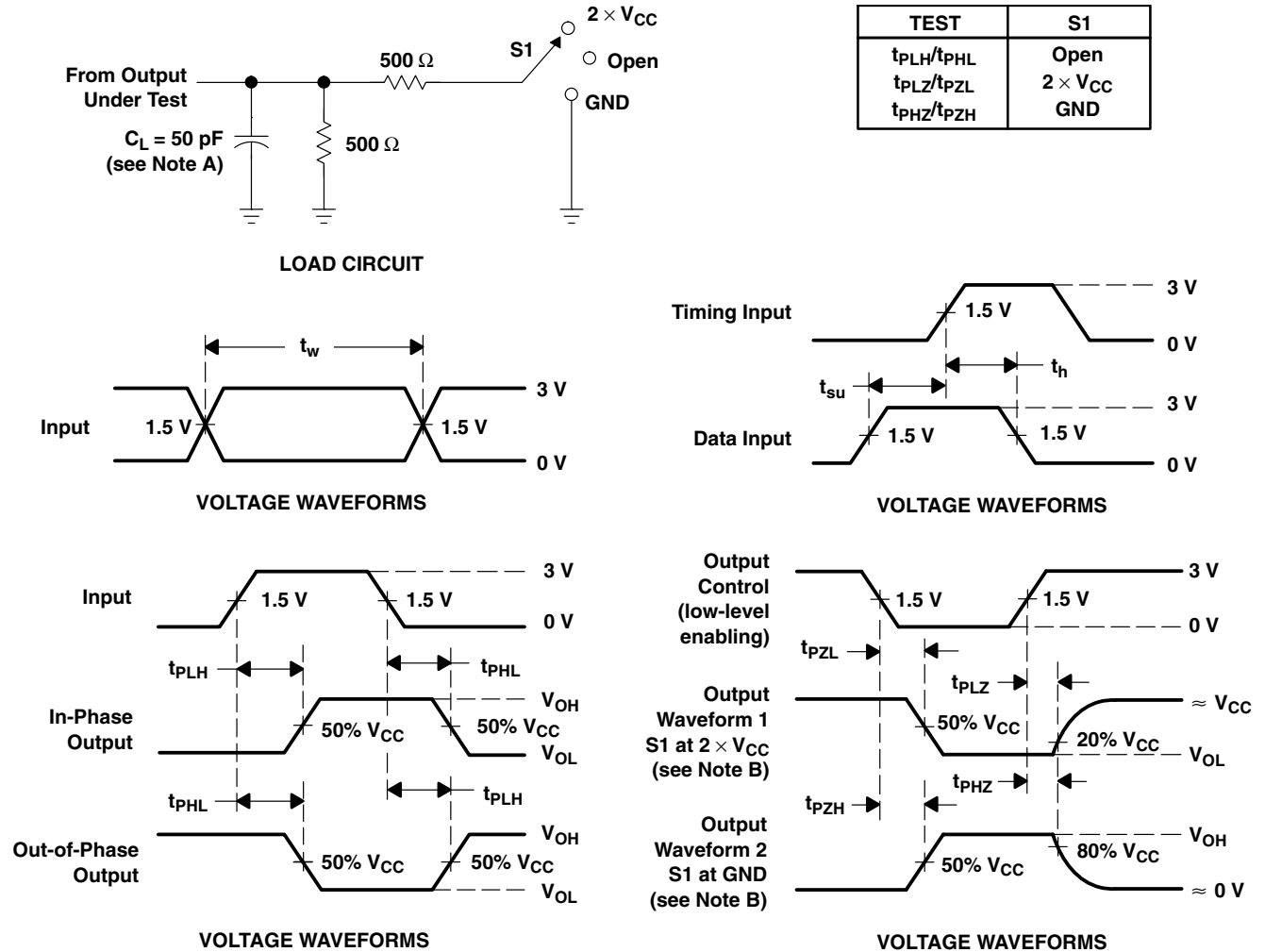
# SN54ACT16373, 74ACT16373 16-BIT D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |   | TEST CONDITIONS  |   | TYP | UNIT |
|-----------|---|------------------|---|-----|------|
| $C_{pd}$  | Power dissipation capacitance per latch | Outputs enabled  | $C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$ | 43  | pF   |
|           |   | Outputs disabled |   | 4.5 |      |

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                        |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--|
| <a href="#">5962-9202401MXA</a> | Active        | Production           | CFP (WD)   48  | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9202401MX<br>A<br>SNJ54ACT16373W<br>D |
| <a href="#">74ACT16373DL</a>    | Obsolete      | Production           | SSOP (DL)   48 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | ACT16373                                   |
| <a href="#">74ACT16373DLR</a>   | Active        | Production           | SSOP (DL)   48 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ACT16373                                   |
| 74ACT16373DLR.A                 | Active        | Production           | SSOP (DL)   48 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ACT16373                                   |
| 74ACT16373DLRG4                 | Active        | Production           | SSOP (DL)   48 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ACT16373                                   |
| <a href="#">SNJ54ACT16373WD</a> | Active        | Production           | CFP (WD)   48  | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -            | 5962-9202401MX<br>A<br>SNJ54ACT16373W<br>D |
| SNJ54ACT16373WD.A               | Active        | Production           | CFP (WD)   48  | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9202401MX<br>A<br>SNJ54ACT16373W<br>D |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74ACT16373DLR | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



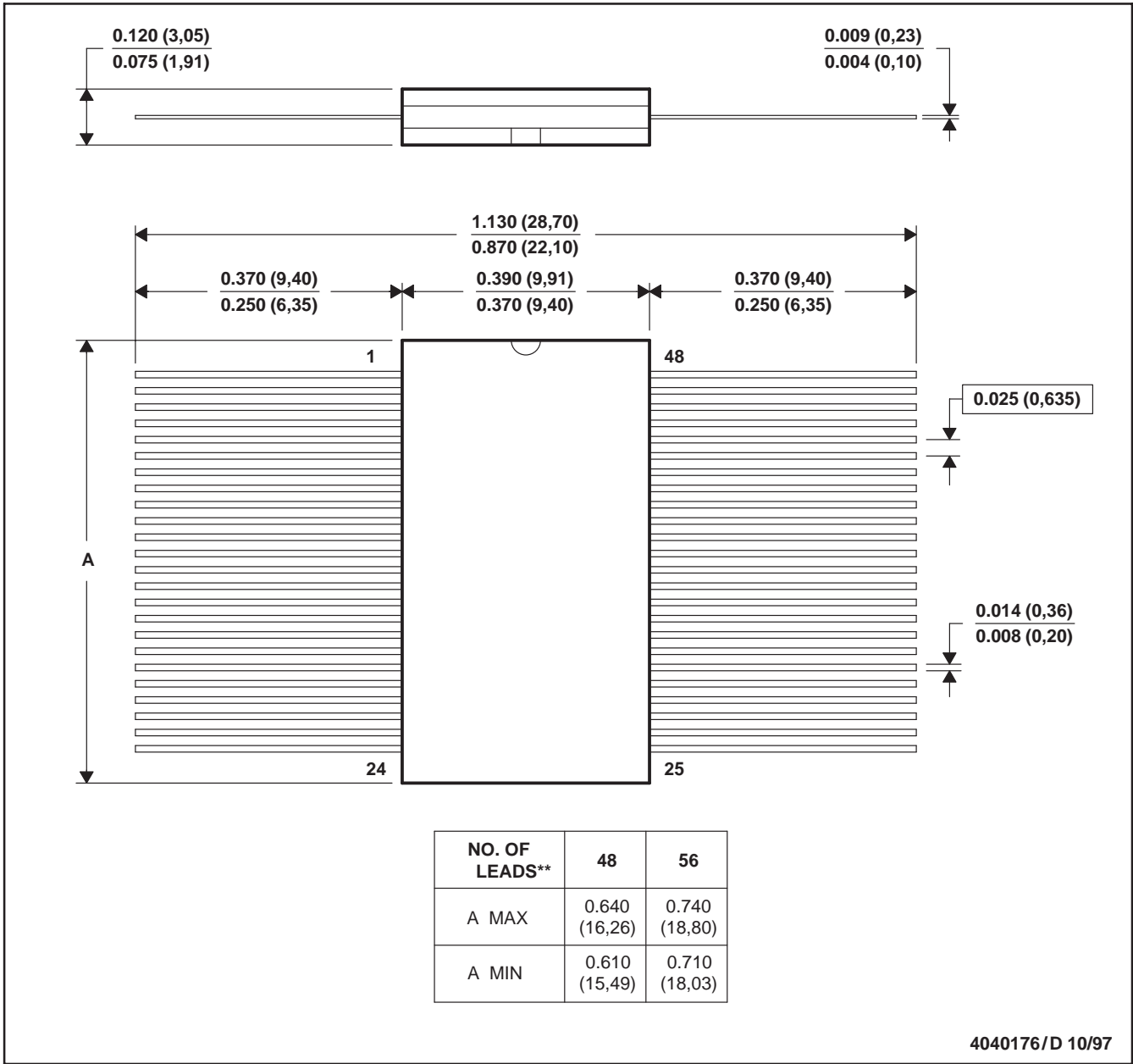
\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74ACT16373DLR | SSOP         | DL              | 48   | 1000 | 356.0       | 356.0      | 53.0        |

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

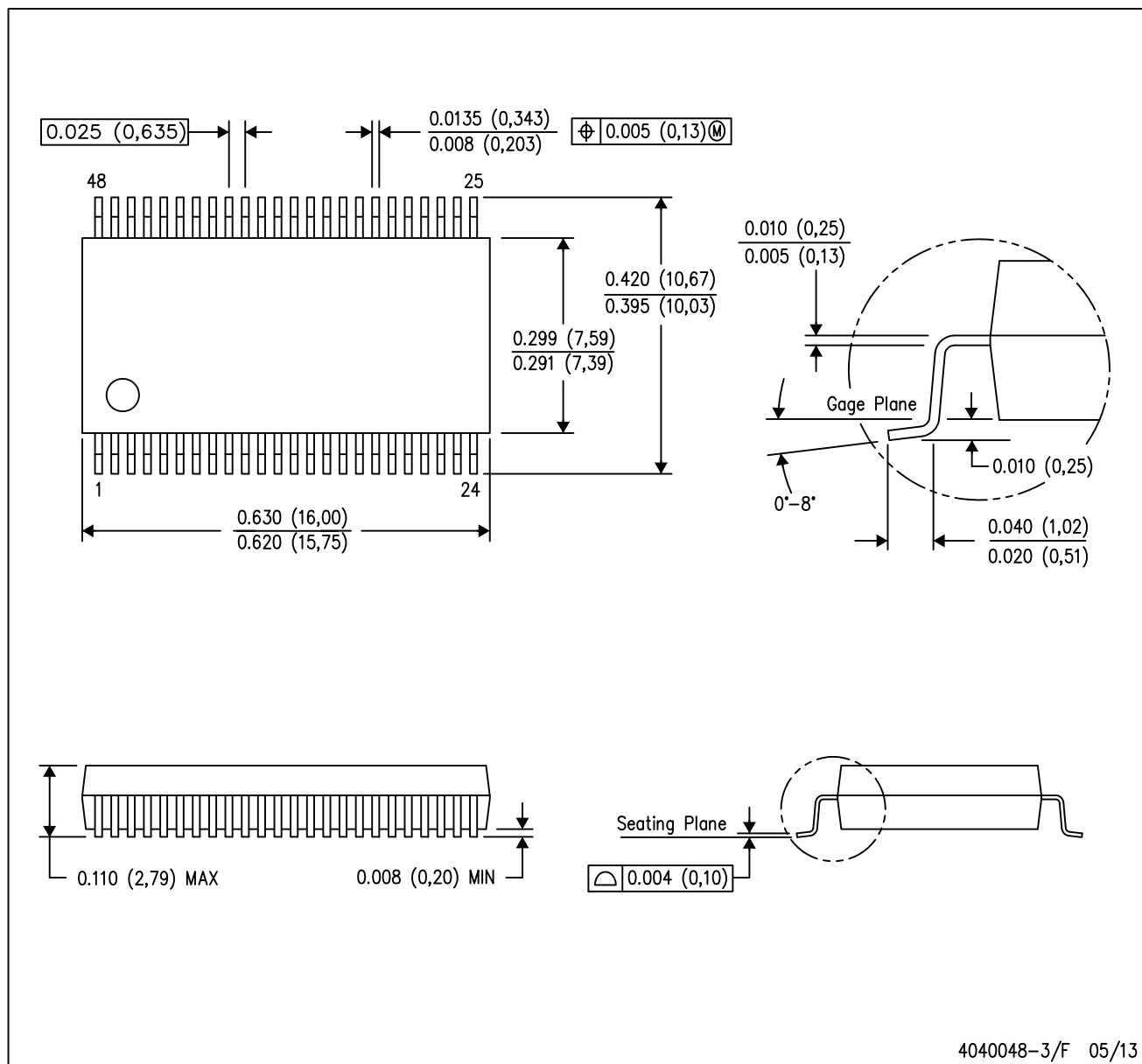
48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package can be hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only  
E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

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