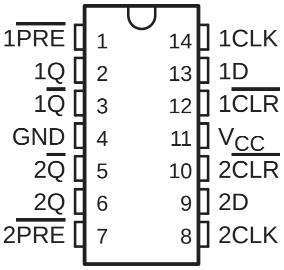
74AC11074
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS499A − DECEMBER 1986 − REVISED APRIL 1996

- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-µm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline (D) and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic 300-mil DIPs (N)**

D, N, OR PW PACKAGE
(TOP VIEW)



description

This device contains two independent positive-edge-triggered D-type flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) input sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input that meets the setup-time requirements are transferred to the outputs on the low-to-high transition of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The 74AC11074 is characterized for operation from −40°C to 85°C.

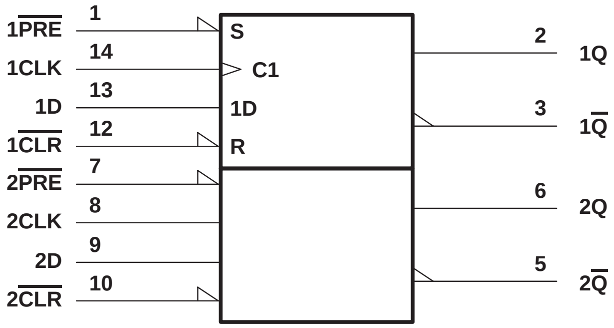
FUNCTION TABLE

INPUTS				OUTPUT	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H[†]	H[†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

[†] This configuration is nonstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)		−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)		±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±50 mA
Continuous current through V_{CC} or GND		±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2):	D package	1.25 W
	N package	1.1 W
	PW package	0.5 W
Storage temperature range, T_{stg}		−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
∆t/∆v	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
V_{OH}	I_{OH} = −50 µA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	µA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4		4		ns
		CLK low or high	5		5		
t_{su}	Setup time before CLK↑	Data high or low	5		5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	1		1		
t_h	Hold time after CLK↑		0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	125	0	125	MHz
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4		4		ns
		CLK low or CLK high	4		4		
t_{su}	Setup time before CLK↑	Data high or low	3.5		3.5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	1		1		
t_h	Hold time after CLK↑		0		0		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100	125		100		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	1.5	5.8	9.3	1.5	10	ns
t_{PHL}			1.5	6.5	11.4	1.5	12.2	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	1.5	7.7	10.5	1.5	11.3	ns
t_{PHL}			1.5	7.3	9.7	1.5	10.6	

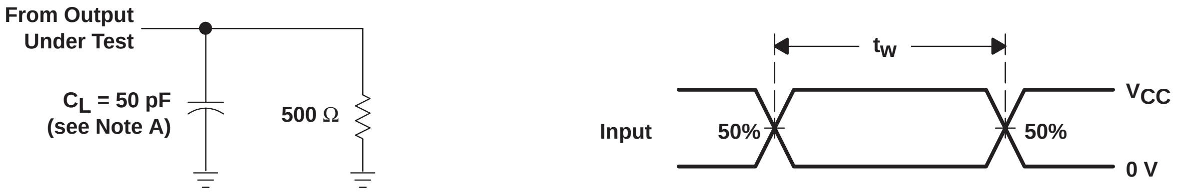
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			125	150		125		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	1.5	4.2	6.6	1.5	7.1	ns
t_{PHL}			1.5	4.7	8.2	1.5	9	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	1.5	5.4	7.5	1.5	8.2	ns
t_{PHL}			1.5	5	6.9	1.5	7.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

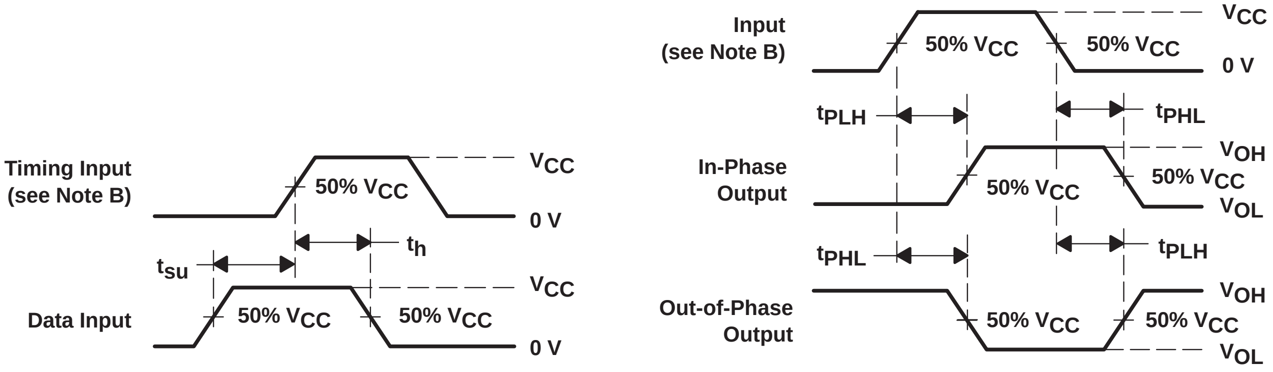
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	30	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AC11074D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	AC11074
74AC11074DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11074
74AC11074DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11074
74AC11074N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74AC11074N
74AC11074N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74AC11074N
74AC11074PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AE074
74AC11074PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AE074

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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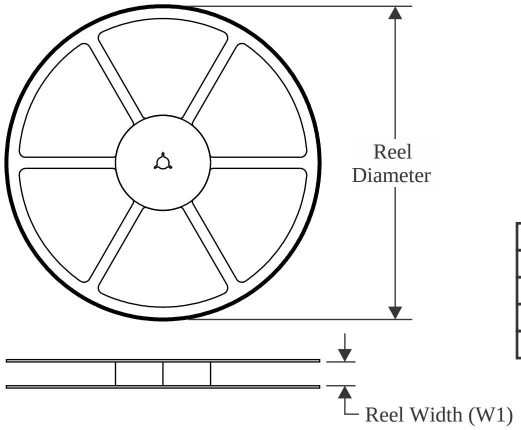
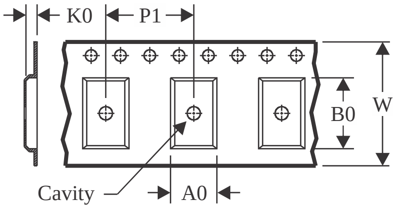
TAPE AND REEL INFORMATION

REEL DIMENSIONS

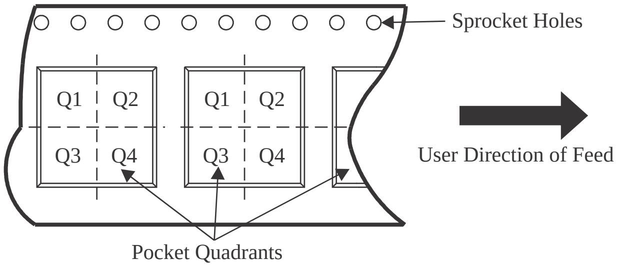


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

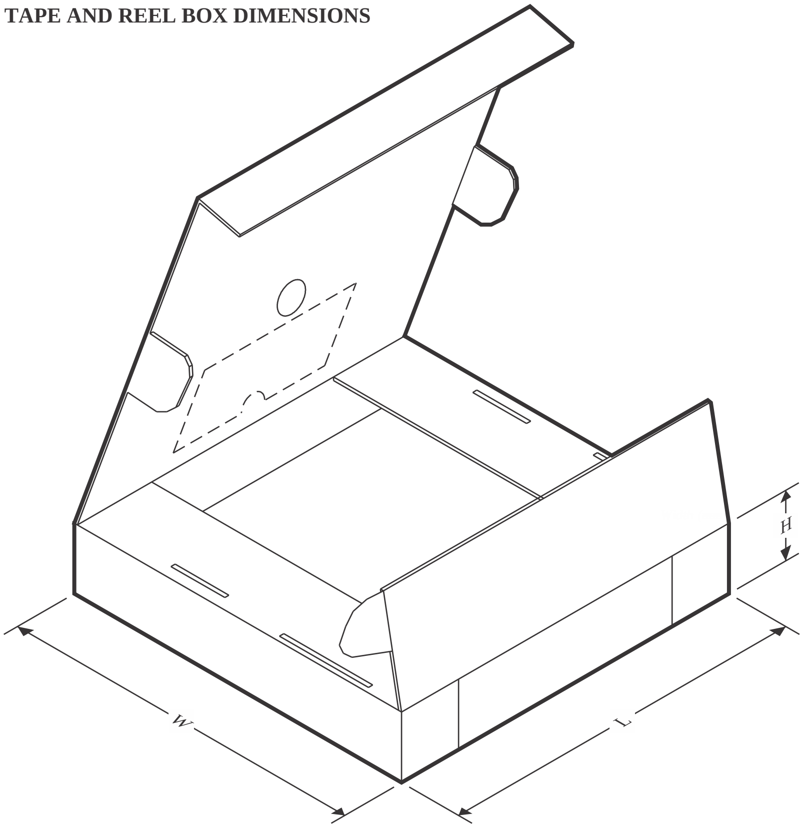
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AC11074DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
74AC11074PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

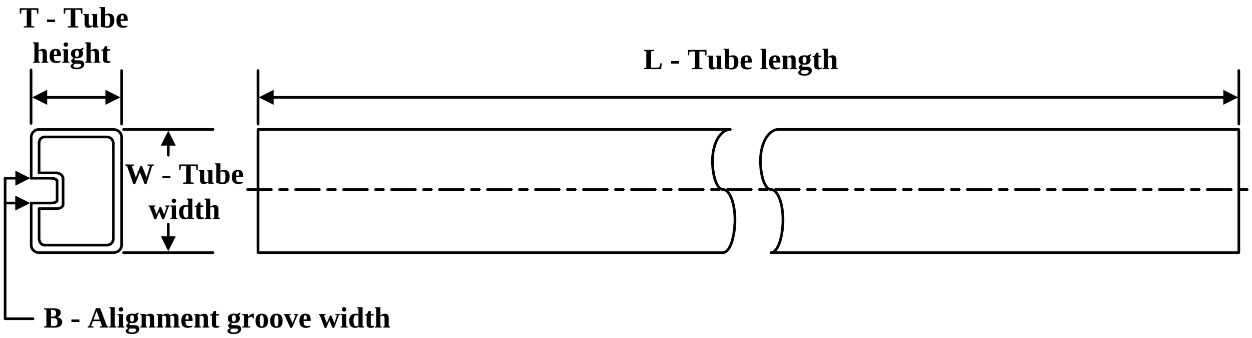
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AC11074DR	SOIC	D	14	2500	353.0	353.0	32.0
74AC11074PWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE

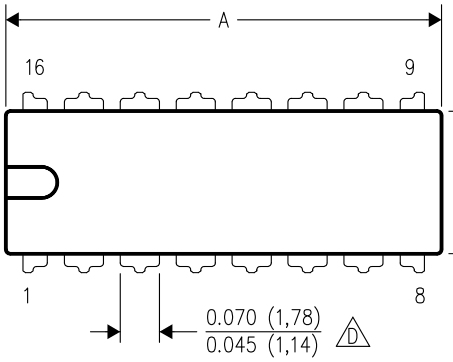


*All dimensions are nominal

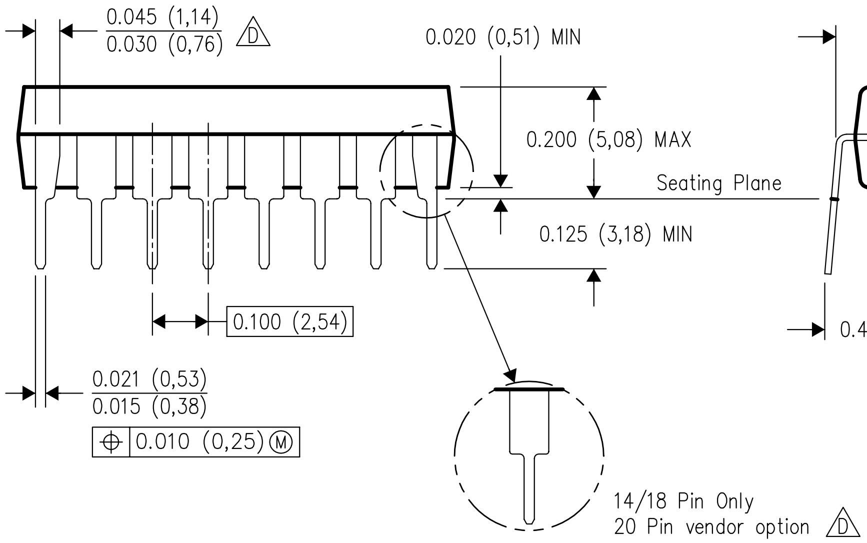
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
74AC11074N	N	PDIP	14	25	506	13.97	11230	4.32
74AC11074N	N	PDIP	14	25	506	13.97	11230	4.32
74AC11074N.A	N	PDIP	14	25	506	13.97	11230	4.32
74AC11074N.A	N	PDIP	14	25	506	13.97	11230	4.32

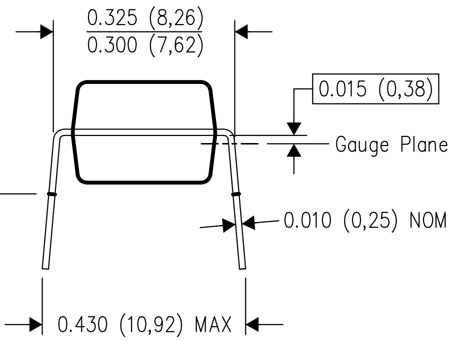
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



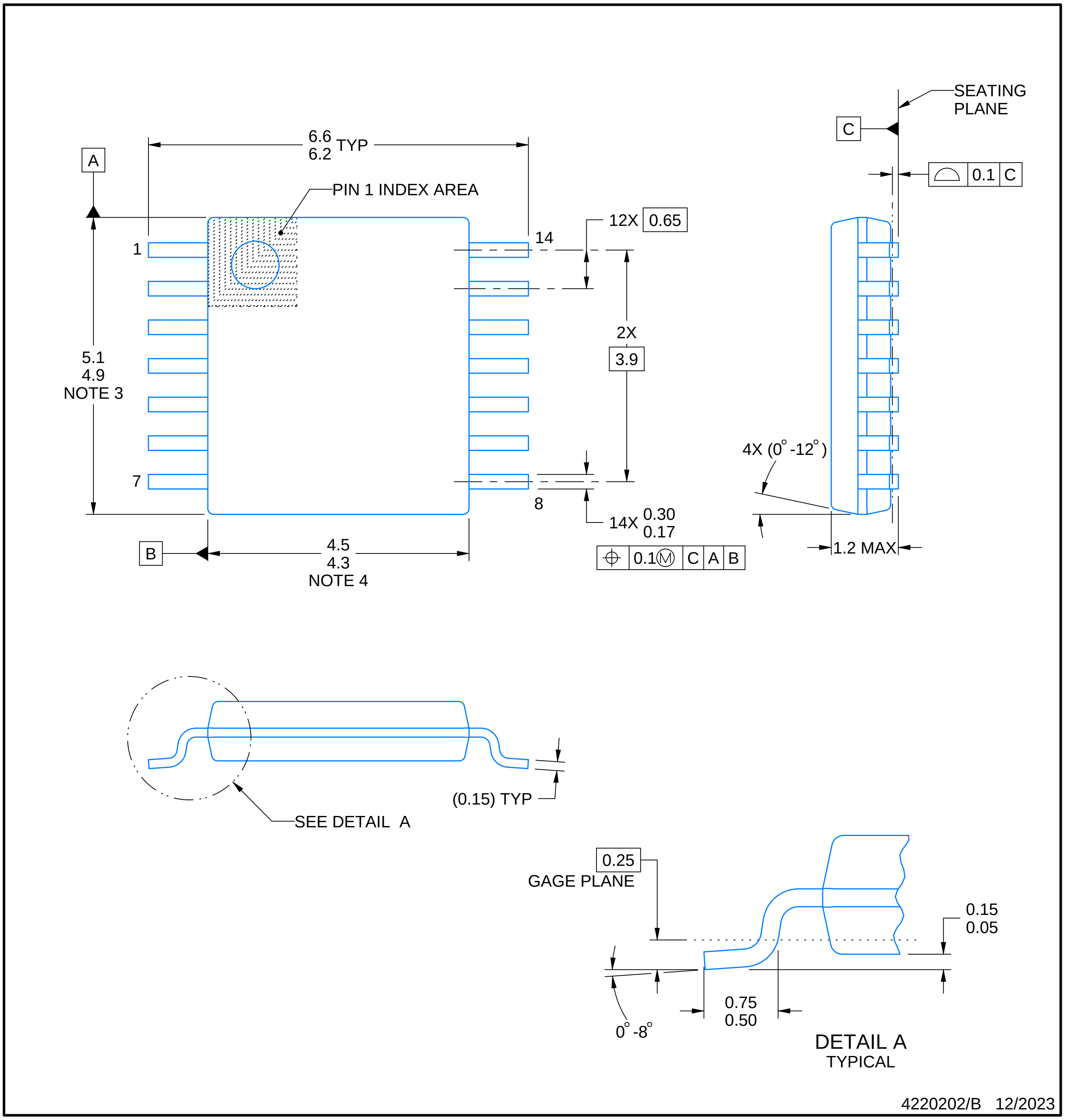
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD





4040049/E 12/2002

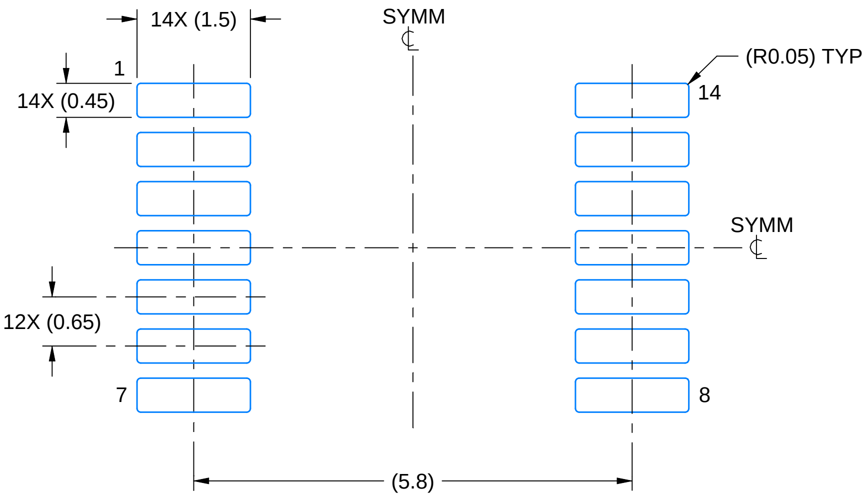
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

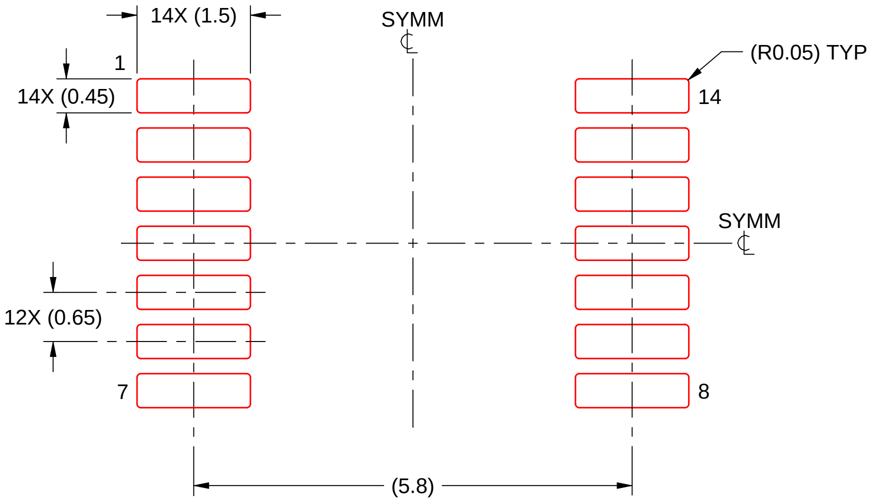
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

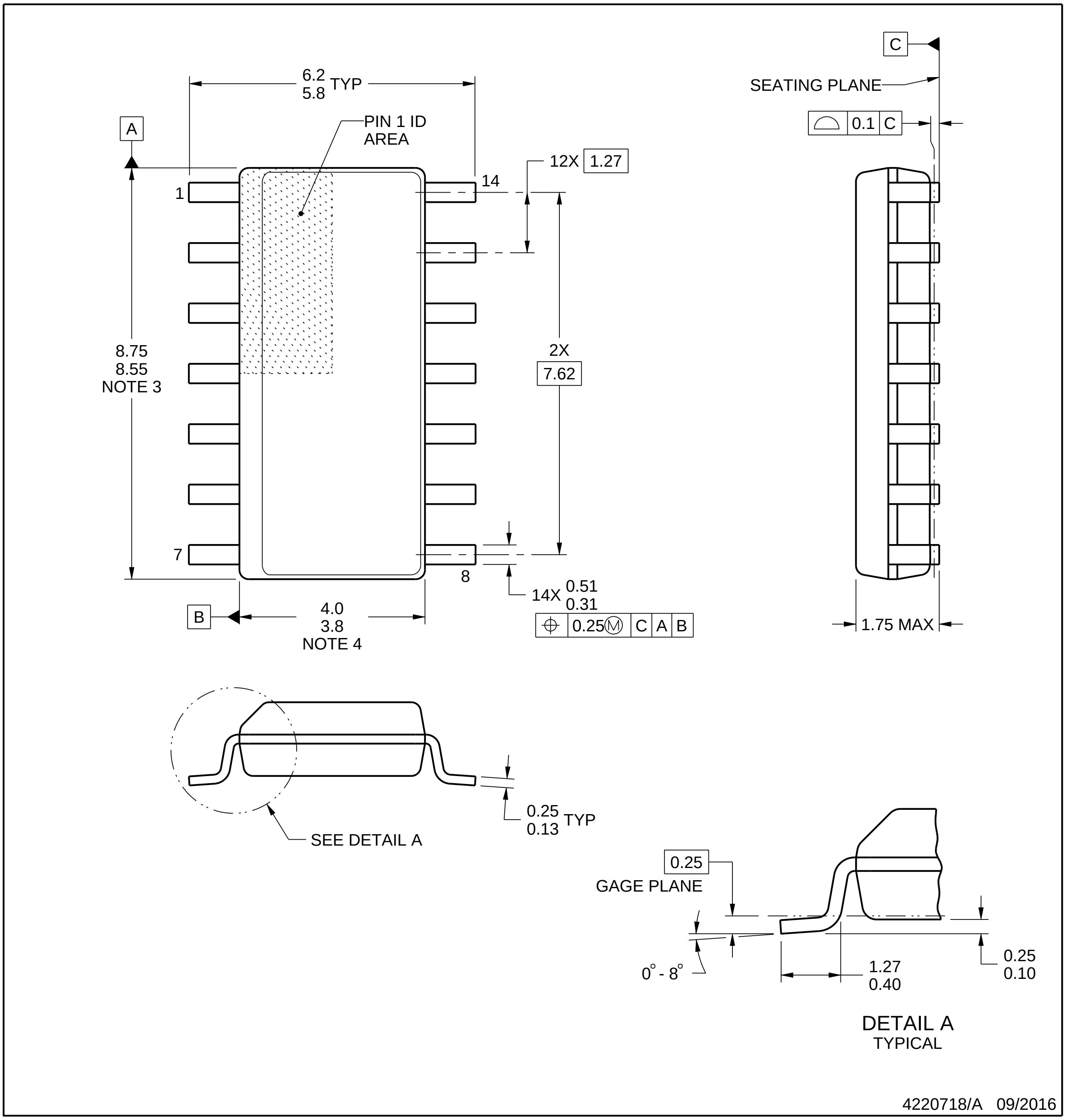


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

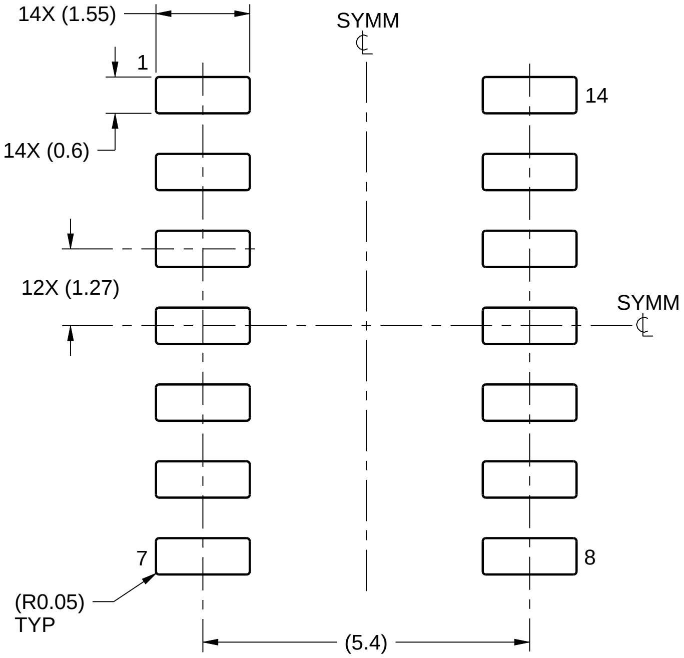
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

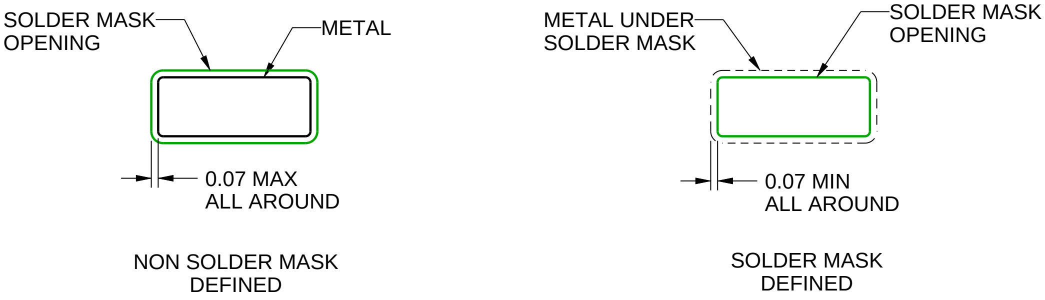


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

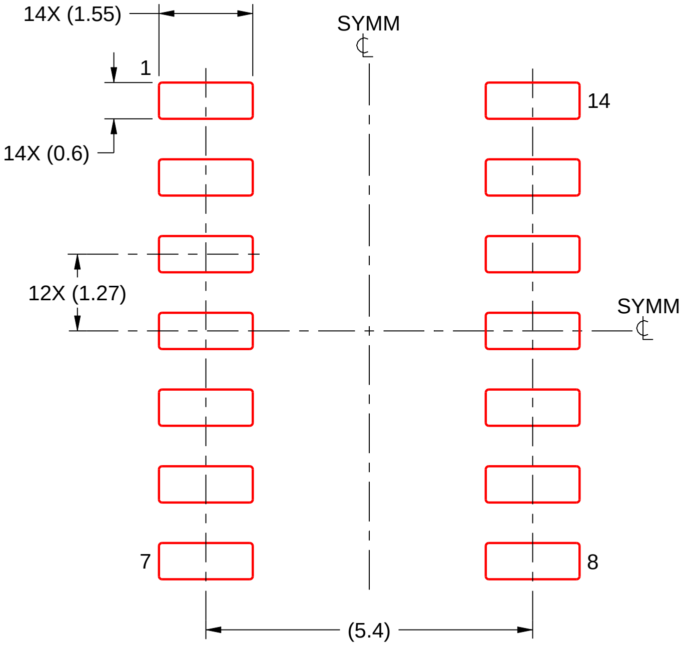


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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