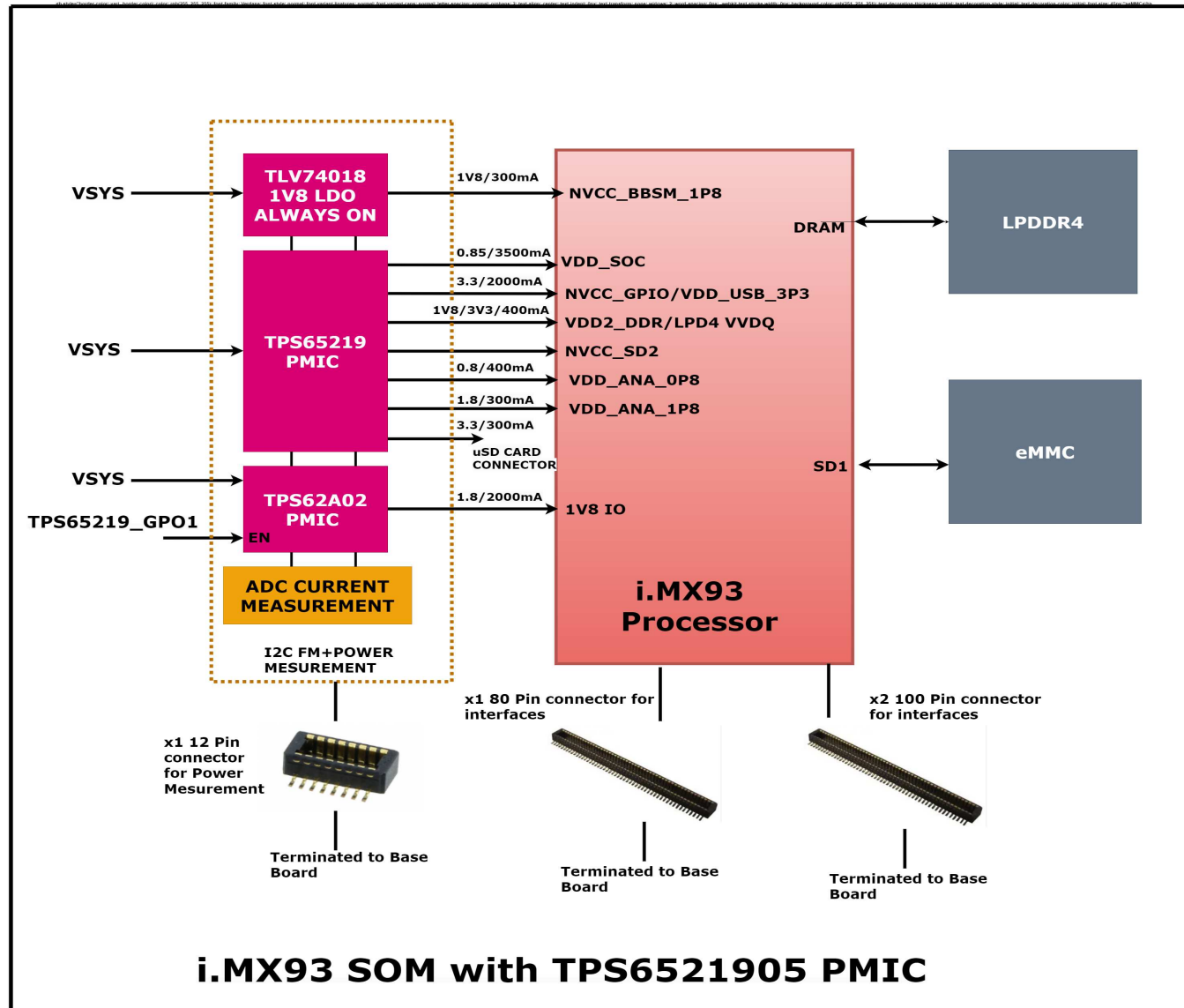


REV	Revision Notes	Designer	Approver	Date
A03	i.MX 93 SOM BOARD INITIAL RELEASE	ROHIT	CHETAN SINGH	12-02-2024
A04	TI COMMENTS IMPLEMENTATION	SHIVAM	CHETAN SINGH	29-02-2024
A1	PROTO RELEASE	ROHIT/SHIVAM	CHETAN SINGH	27-03-2024

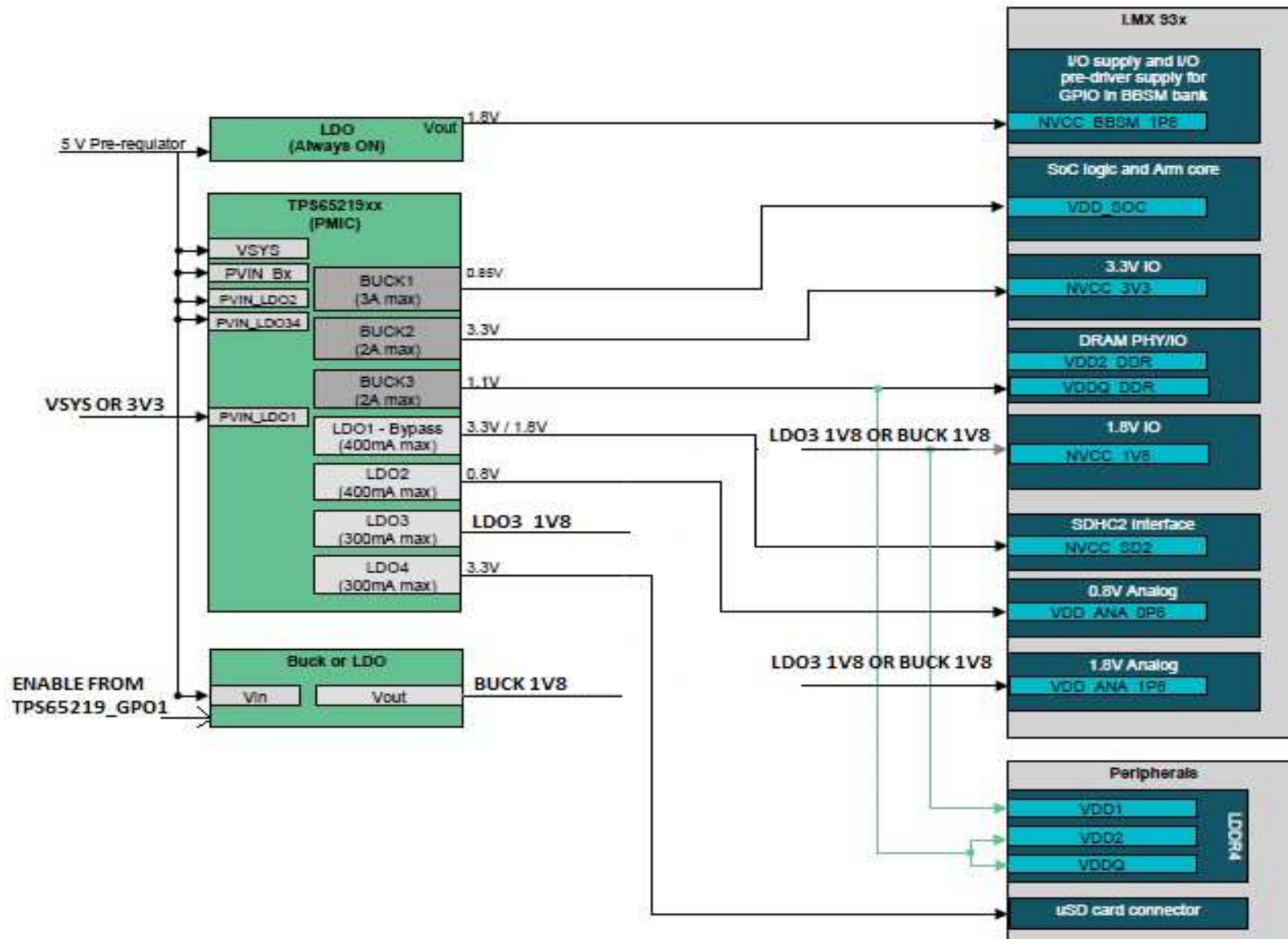
i.MX93 SOM Board with TPS6521905 TI PMIC

Contents	
Page No	Sheet Name
01	COVER PAGE
02	i.MX93 BLOCK DIAGRAM
03	POWER ARCHITECTURE
04	i.MX93 POWER
05	LPDDR4
06	i.MX93 IO/PHY
07	i.MX93 MISC
08	eMMC
09	BOOT CONFIG
10	PMIC TI AND EXT REGULATOR
11	HDR CONNECTORS
12	POWER MEASUREMENT

i.MX93 BLOCK DIAGRAM



POWER ARCHITECTURE

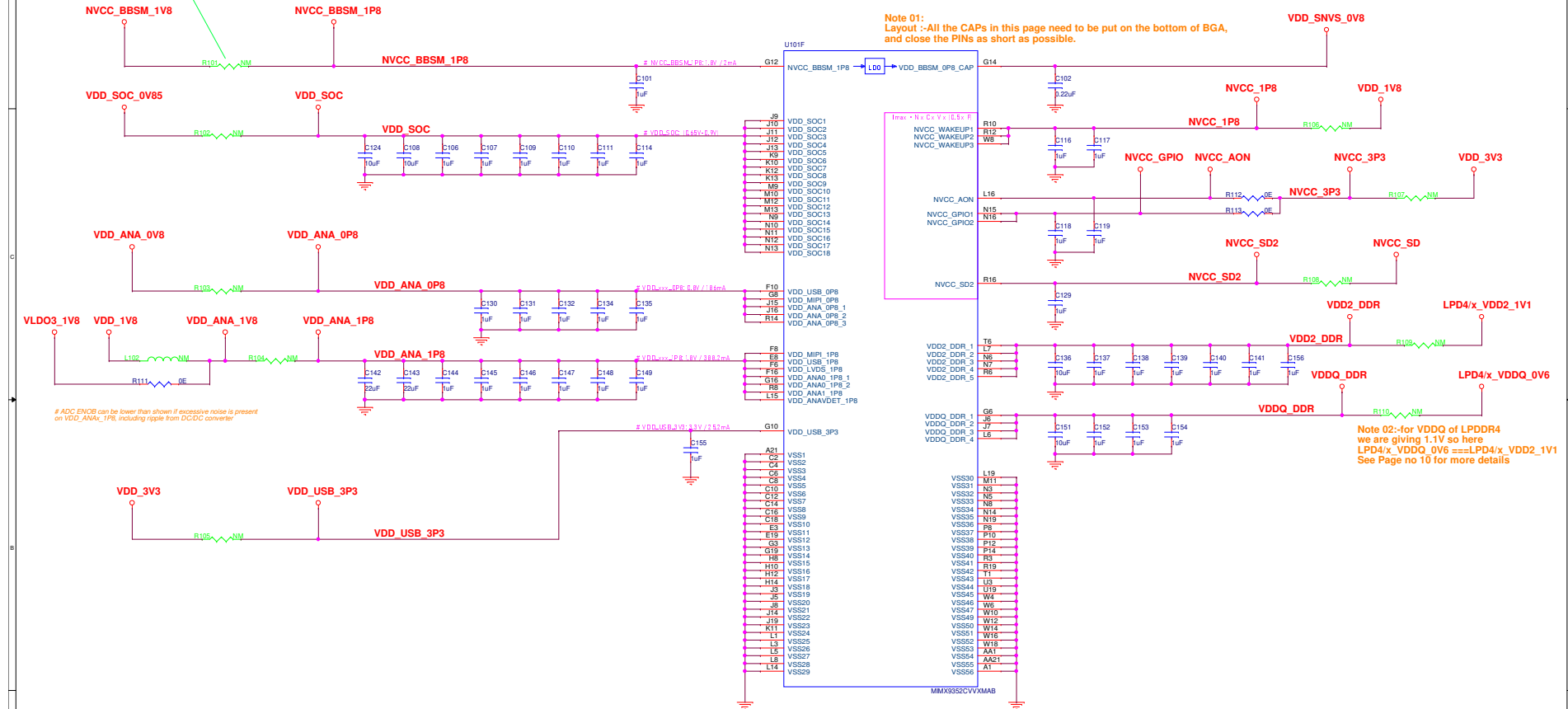


i.MX93 PWR


Note 1:- Placed all the green highlight RES (in this page 4) while no PWR MEAS required

Note 01:
Layout :-All the CAPs in this page need to be put on the bottom of BGA, and close the PINs as short as possible.

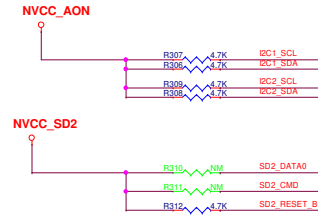
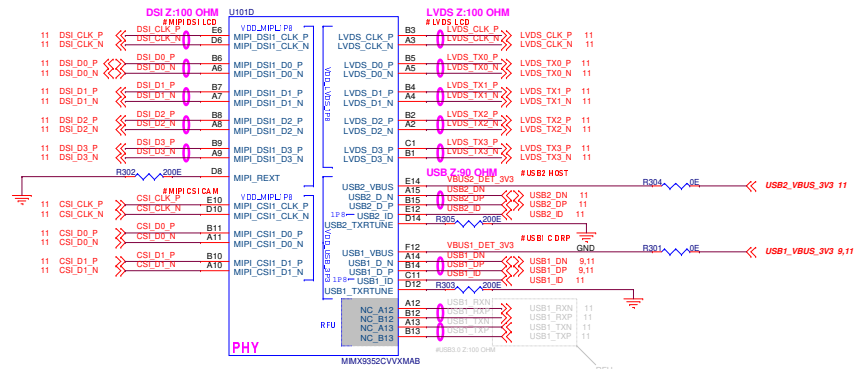
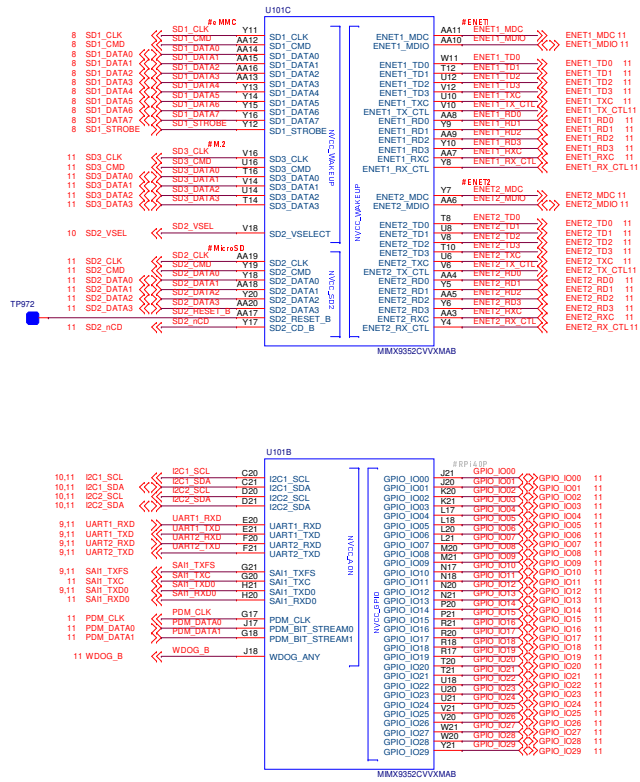
Note 02:-for VDDQ of LPDDR4
we are giving 1.1V so here
LPD4/x_VDDQ_0V6 ==LPD4/x_VDD2_1V1
See Page no 10 for more details



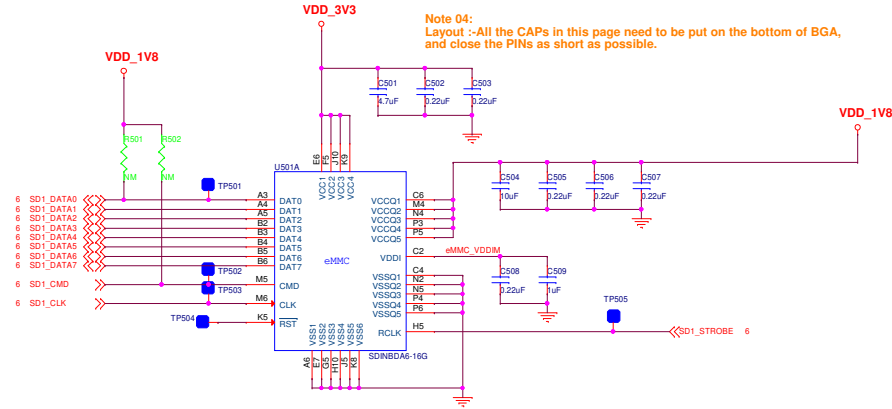
[illegible]

 VVDN TECHNOLOGIES		C	Title : LPDDR4
		Fab No : 501-1-03450	Rev: A1
		Asy No : 701-1-04331	Sheet 06 of 12

i.MX93 IO/PHY



FLASH: eMMC <5.1>

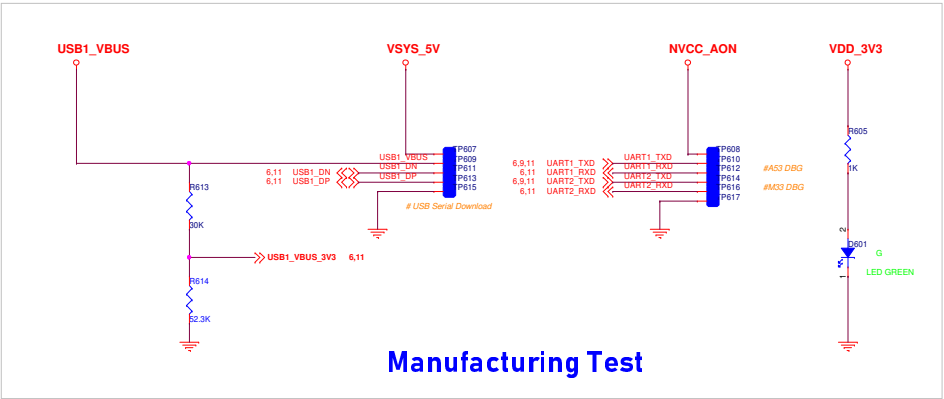
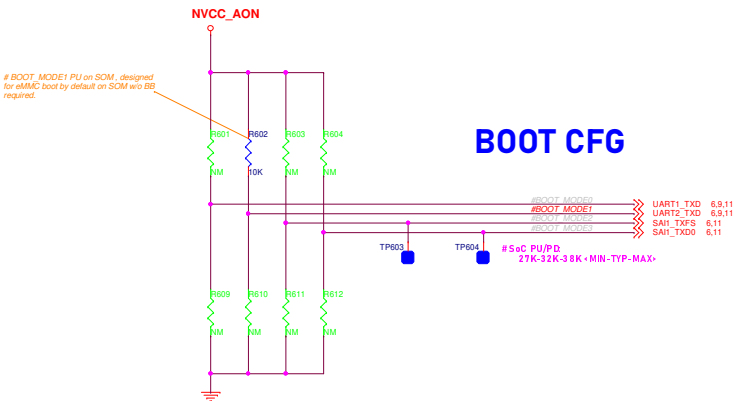


Boot Mode and CFG Switch

i.MX93 BOOT MODE

BOOT_MODE[3:0]	BOOT CORE	BOOT DEVICE
0010	Cortex-A55	USDHC1 8-bit eMMC 5.1

Note 05:
For more details: Please refer to the Page No: 85 for Boot Mode Configuration in i.MX93 datasheet



Title : BOOT CONFIG	
Fab No : 501-1-03450	Rev: A1
Asy No : 701-1-04331	Sheet 09 of 12

B2B CN for CPU SOM

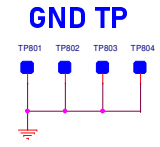
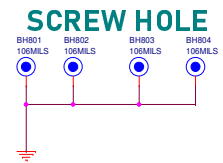
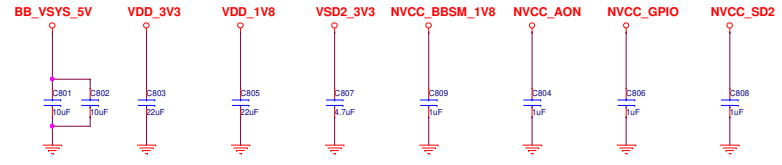
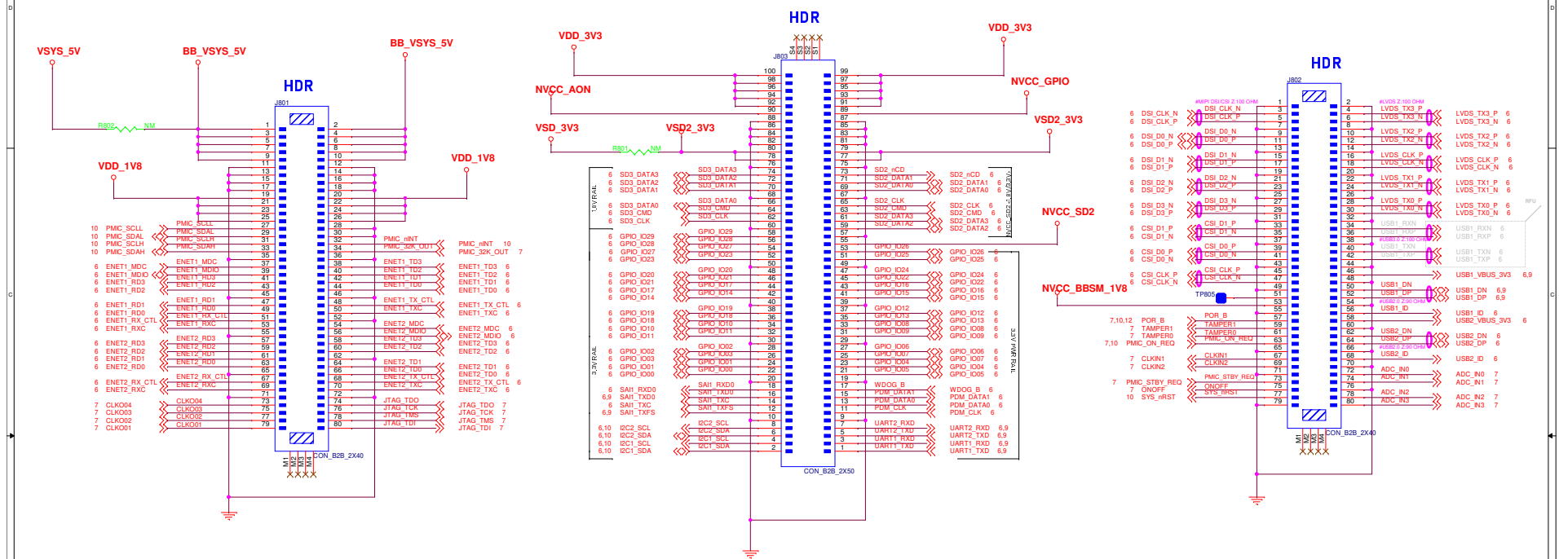


Figure 10: Current Sense Range Selection

The figure shows six circuit diagrams (a-f) for current sense range selection. Each diagram includes a load switch, a sense resistor (RS), and a sense amplifier (FSC). The diagrams are for:

- (a) VLS_3V3, DB_VSYS_5V, VSYS_5V
- (b) VLS_3V3, NVCC_BBSM_1V8, S1_NVCC_BBSM_1V8, NVCC_BBSM_1P8
- (c) VLS_3V3, VDD_SOC_0V85, S1_VDD_SOC_0V85, VDD_SOC
- (d) VLS_3V3, LPD4x_VDD2_1V1, S1_CPU_VDD2_DOR, VDD2_DOR
- (e) VLS_3V3, LPD4x_VDD0_0V6, S1_CPU_VDD0_DOR, VDD0_DOR
- (f) NVCC_SD, NVCC_SD2

Each diagram includes a table for FSC_CTRL register settings:

SW	SW OFF	SW OFF, small FSC
0	0	0
1	1	1

Power Measurement Equations:

$$I_{sense} = \frac{V_{sense}}{R_s}$$

$$V_{sense} = V_{sense} - V_{sense}$$

$$Power = I_{sense} \times V_{sense}$$

Part	Type	Device	Address	Voltage
U902	M1	PAC1934T	0x11(0010001x)	3.3V
U904	M2	PAC1934T	0x12(0010001x)	3.3V
U907	M3	PAC1934T	0x13(0010011x)	3.3V
U911	M4	PAC1934T	0x14(0010100x)	3.3V
U912	M5	PAC1934T	0x15(0010101x)	3.3V
U909	IO EXP	PCA9672BS	0x20(0100000x)	3.3V
U913	T-sensor	PCT2075	0x18(0010000x)	3.3V

[illegible][illegible][illegible][illegible]

The diagram illustrates the connection of the Fixed Current Sense Resistor (RES) to various power pins. The central component is the LPD4x_VDD01, LPD4x_VDD02, LPD4x_VDD03, and LPD4x_VDD04 chips. The RES pin of each chip is connected to a network of resistors and capacitors. The connections are as follows:

- LPD4x_VDD01:** RES pin connected to NVCC_SD (via 10k resistor), NVCC_SD2 (via 10k resistor), VDD_ANA_DVB (via 10k resistor), VDD_ANA_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), LPD4x_VDD01_DVB (via 10k resistor), LPD4x_VDD01_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), LPD4x_VDD01_DVB (via 10k resistor), LPD4x_VDD01_IVB (via 10k resistor).
- LPD4x_VDD02:** RES pin connected to NVCC_SD (via 10k resistor), NVCC_SD2 (via 10k resistor), VDD_ANA_DVB (via 10k resistor), VDD_ANA_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), LPD4x_VDD02_DVB (via 10k resistor), LPD4x_VDD02_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), LPD4x_VDD02_DVB (via 10k resistor), LPD4x_VDD02_IVB (via 10k resistor).
- LPD4x_VDD03:** RES pin connected to NVCC_SD (via 10k resistor), NVCC_SD2 (via 10k resistor), VDD_ANA_DVB (via 10k resistor), VDD_ANA_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), LPD4x_VDD03_DVB (via 10k resistor), LPD4x_VDD03_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), LPD4x_VDD03_DVB (via 10k resistor), LPD4x_VDD03_IVB (via 10k resistor).
- LPD4x_VDD04:** RES pin connected to NVCC_SD (via 10k resistor), NVCC_SD2 (via 10k resistor), VDD_ANA_DVB (via 10k resistor), VDD_ANA_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), LPD4x_VDD04_DVB (via 10k resistor), LPD4x_VDD04_IVB (via 10k resistor), VDD_IVB (via 10k resistor), VSS_IVB (via 10k resistor), LPD4x_VDD04_DVB (via 10k resistor), LPD4x_VDD04_IVB (via 10k resistor).

The diagram also includes a table for the Power Measurement Equations:

Power Measurement Equations:
$I_{sense} = V_{sense} / R_{sense}$
$V_{out} = V_{sense} \times R_{sense} / R_{sense}$
$P_{out} = I_{sense} \times V_{out}$

Power Measurement Equations:

$$I_{sense} = V_{sense} / R_s$$

$$V_{out} = V_{sense} - V_{(sense+)} - V_{sense-}$$

$$Power = I_{sense} \times V_{out}$$