

GESI EXPANSION BOARD

TABLE OF CONTENTS

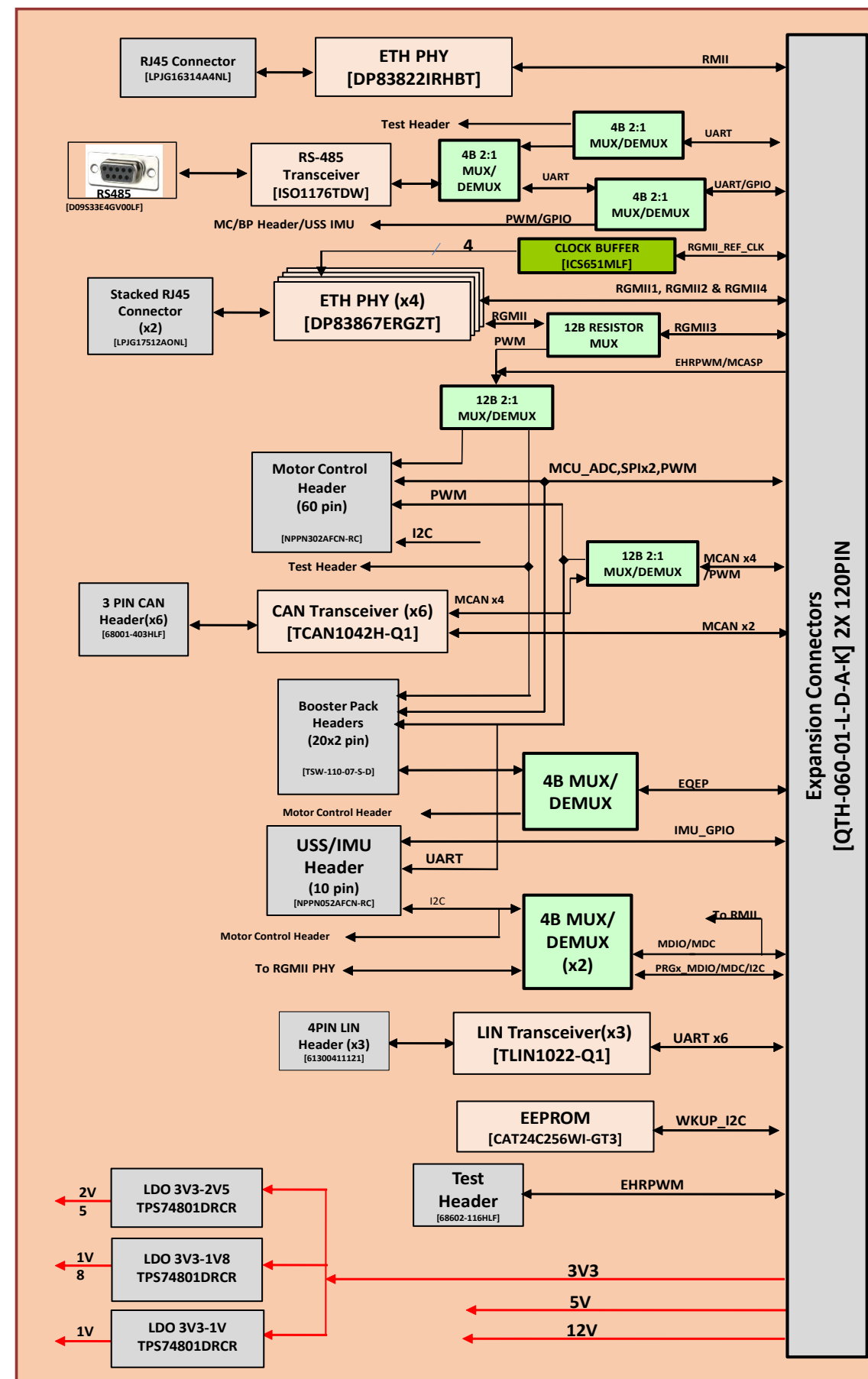
PAGE	CONTENTS
01	TABLE OF CONTENTS
02	REVISION HISTORY
03	BLOCK DIAGRAM
04	EXPANSION CONNECTOR
05	PRG1 MUX - 01
06	PRG1 MUX - 02
07	TEST CONNECTOR & EEPROM
08	MDIO MDC - MUX
09	PRG0 GB_ETHERNET RGMII 1
10	PRG0 GB_ETHERNET RGMII 2
11	PRG1 GB_ETHERNET RGMII 1
12	PRG1 GB_ETHERNET RGMII 2
13	CAN TRANSCEIVERS - 01
14	CAN TRANSCEIVERS - 02
15	LIN INTERFACE -01
16	LIN INTERFACE -02
17	LIN INTERFACE -03
18	RS485 INTERFACE
19	USS/IMU & MOTOR CONTROL
20	BOOSTERPACK HEADER
21	ADC IN
22	RMII PHY INTERFACE
23	POWER SUPPLY
24	HARDWARE SCHEMATICS

REV	E3A
VER	0.2

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	21-NOV-2019	Drafted from "PROC084E3_SCH, VER: 1.3". TP62 & TP63 moved to DNI and Hardware Schematic page Updated	Mistral Design Team		
0.2	26-NOV-2019	Updated the RGMII REF CLOCK Buffer U31 Part# to 651SDCGI	Mistral Design Team		

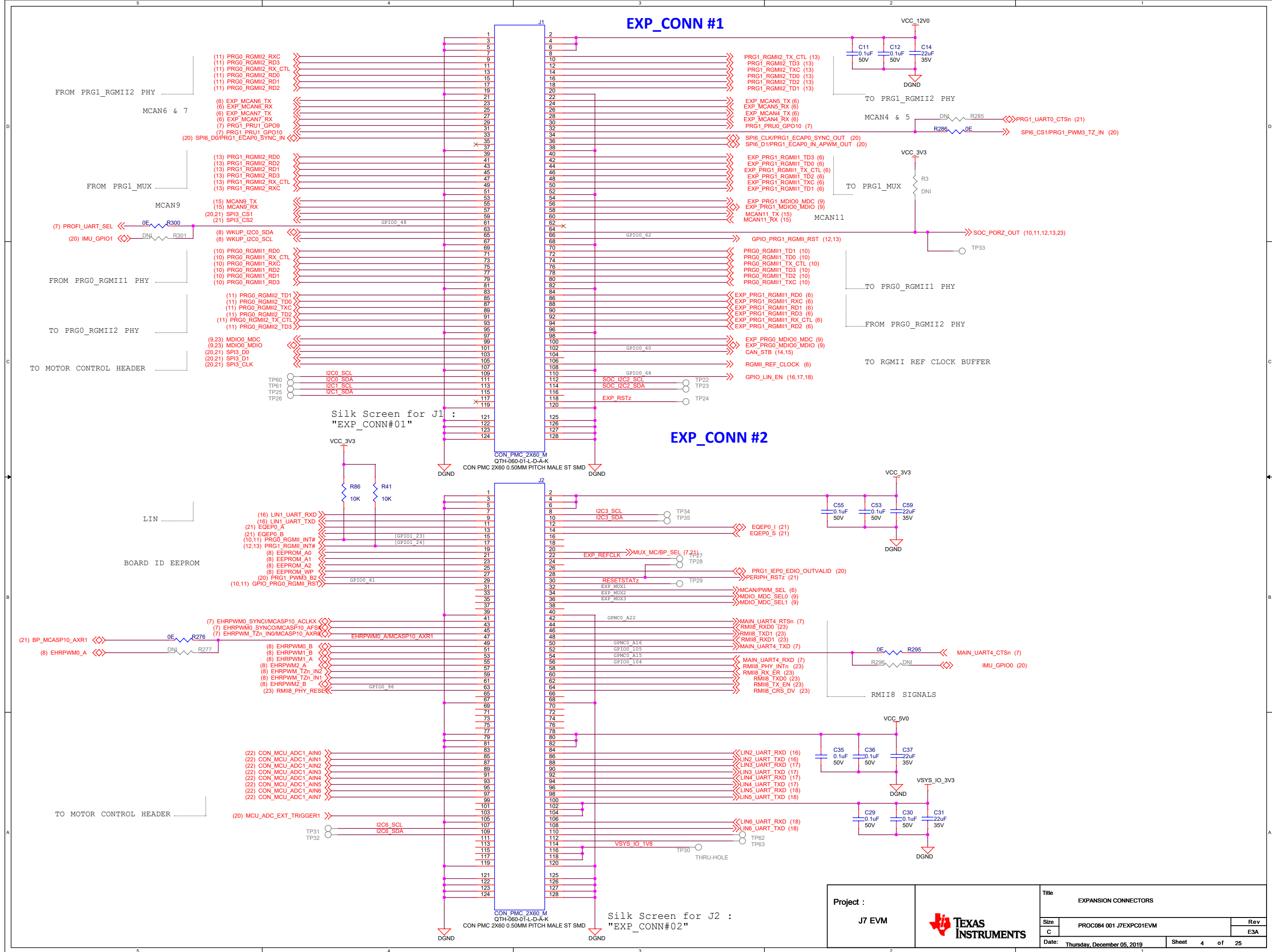
BLOCK DIAGRAM



Project : J7 EVM



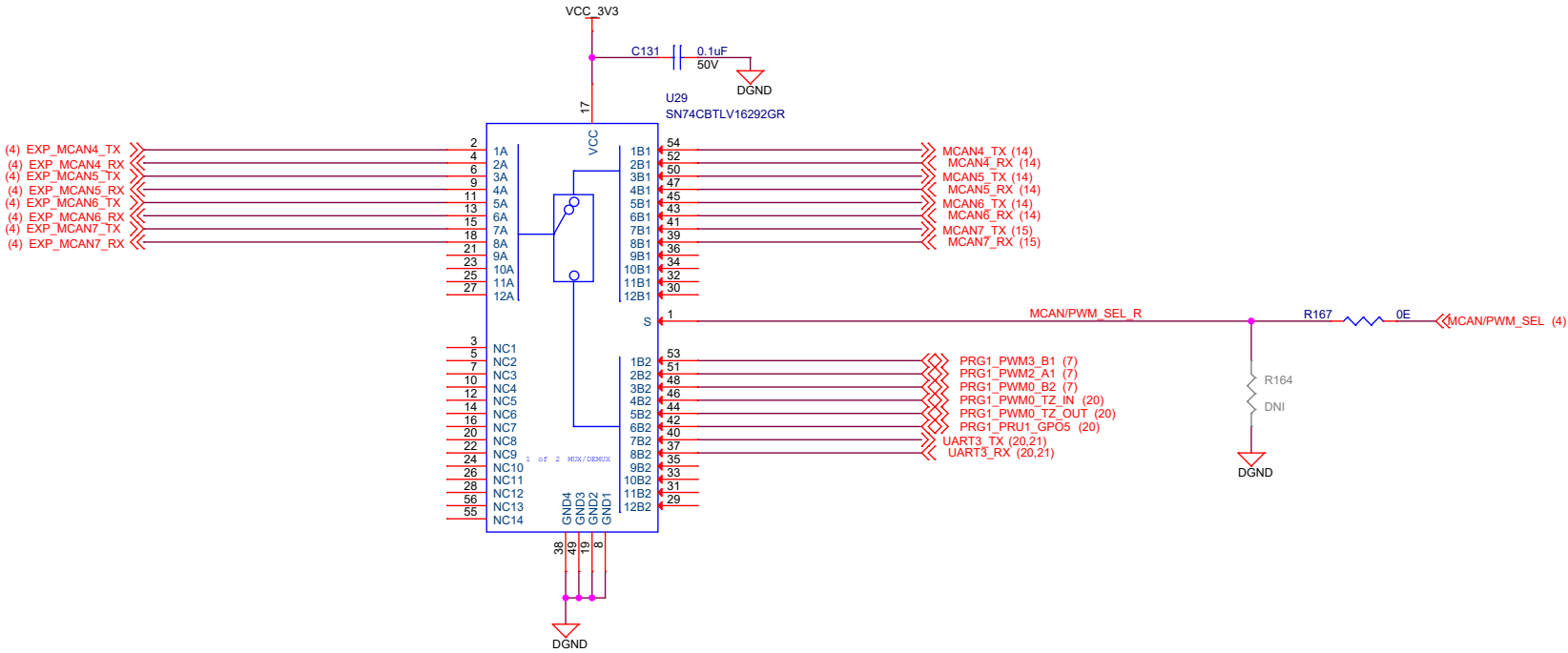
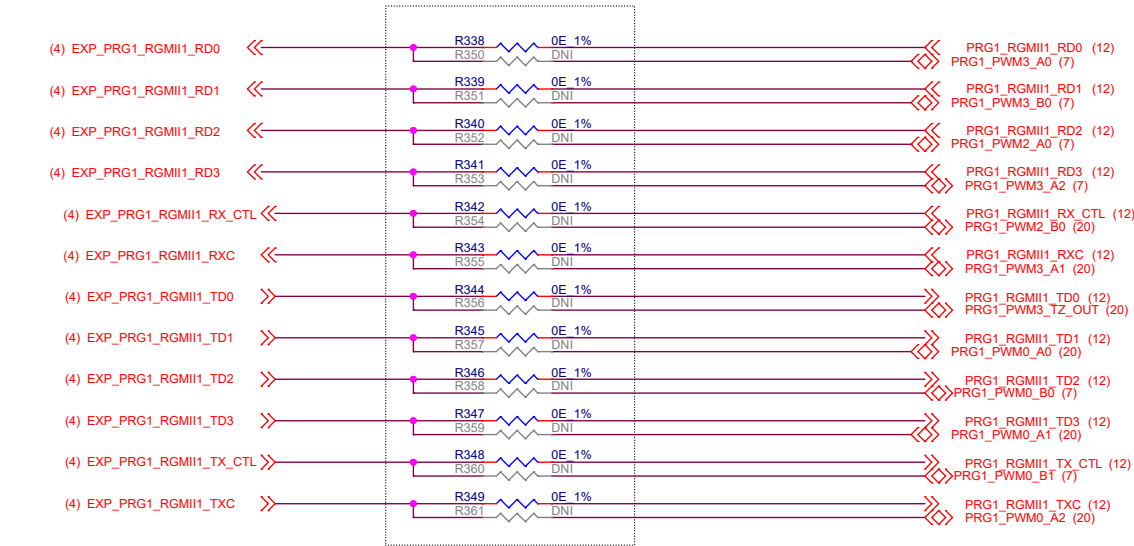
Title				
BLOCK DIAGRAM				
Size	PROC084 001 J7EXPC01EVM			Rev
C				E3A
Date:	Thursday, December 05, 2019	Sheet	3 of	25



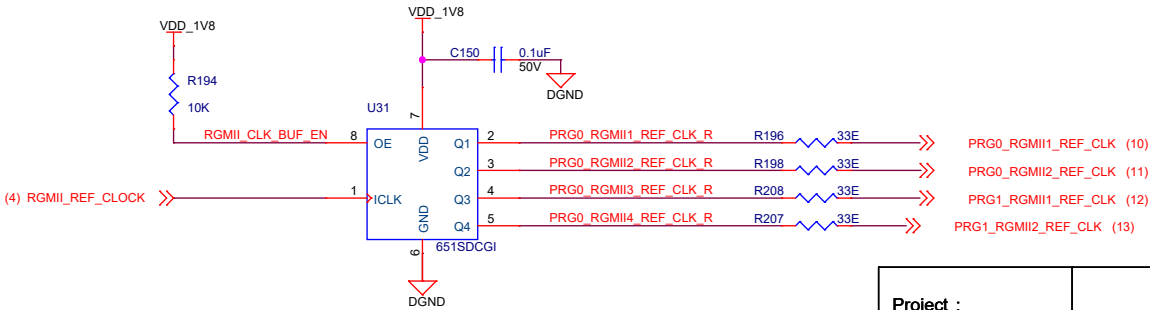
PRG1 MUX - 01



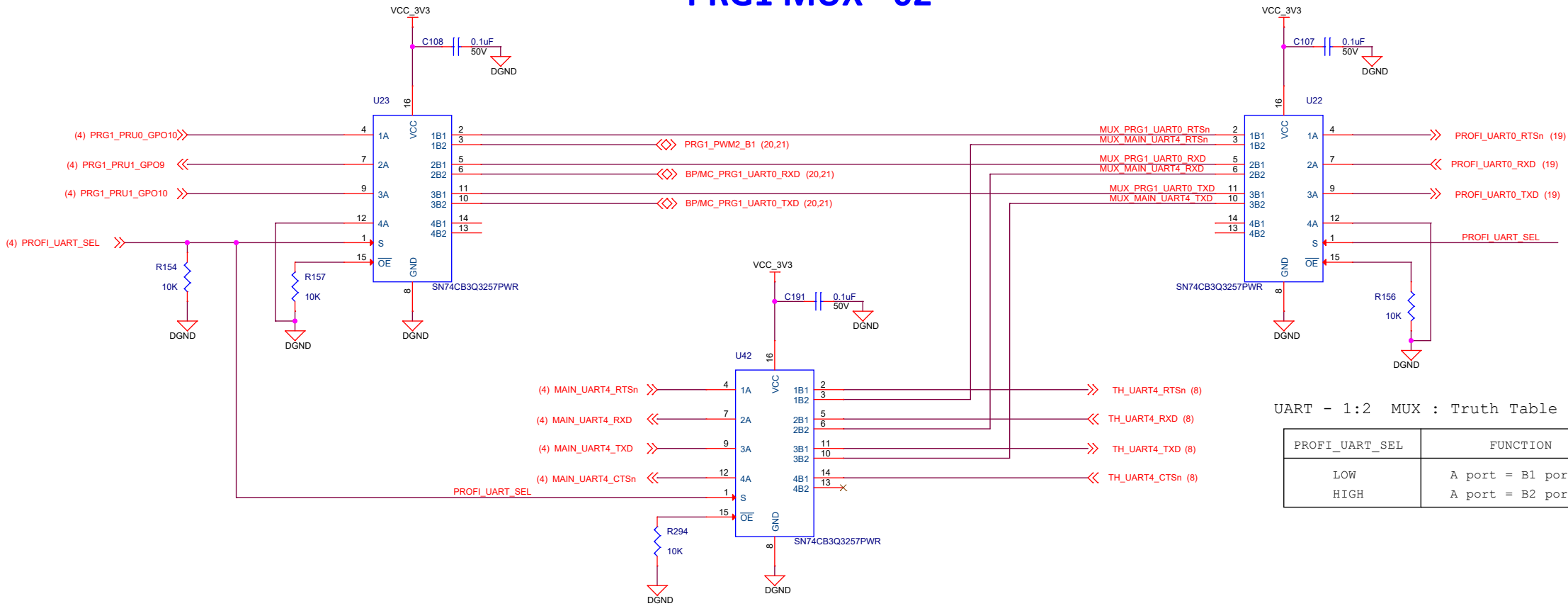
PCB NOTE: keep these resistors placement as Tripad without stub in PCB



RGMII REF CLOCK BUFFER



PRG1 MUX - 02

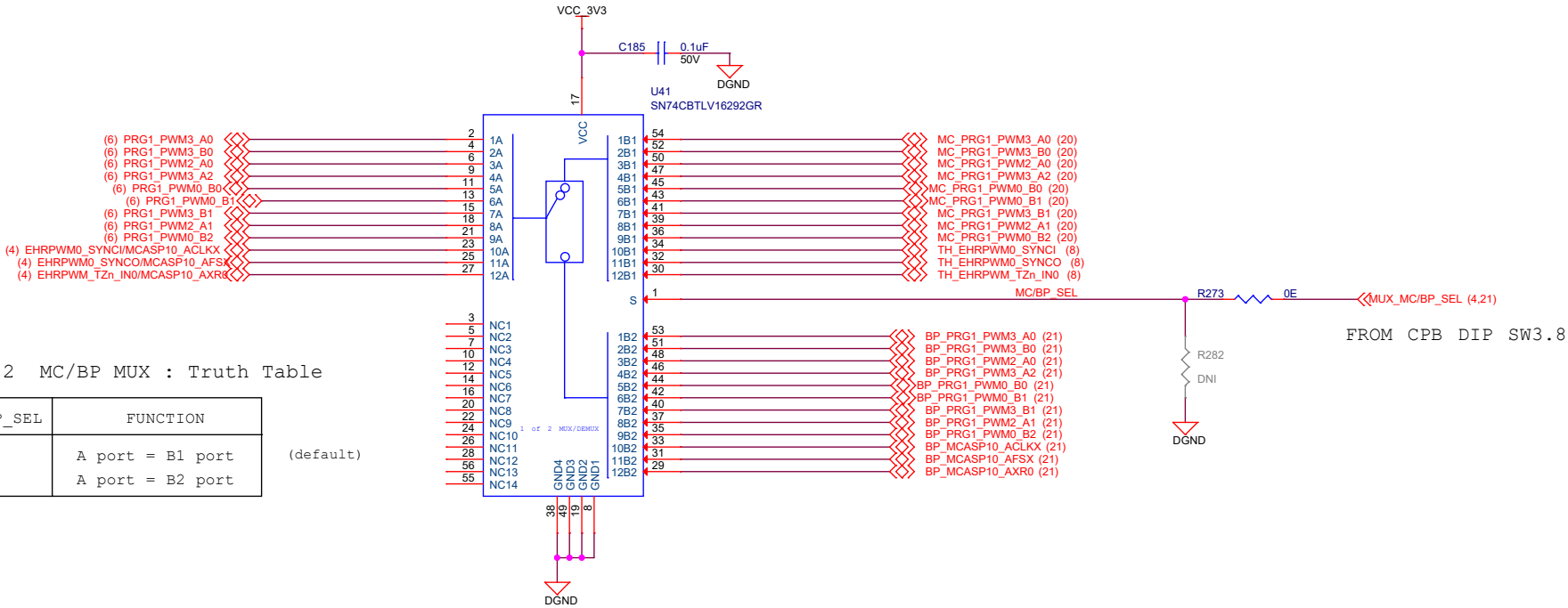


UART - 1:2 MUX : Truth Table

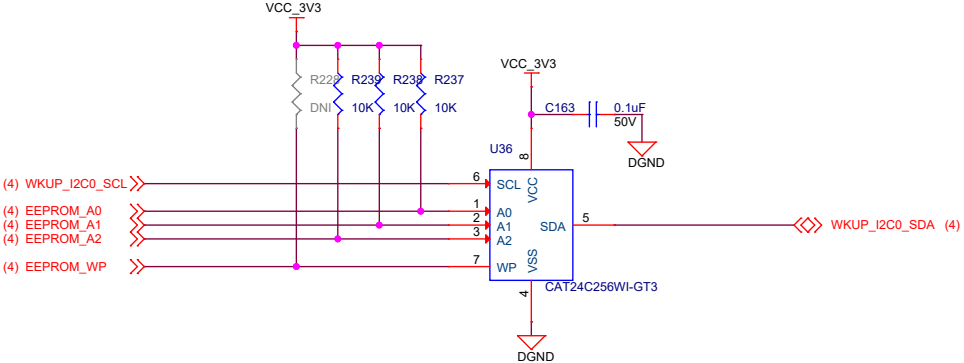
PROFI_UART_SEL	FUNCTION	
LOW	A port = B1 port	(default)
HIGH	A port = B2 port	

PRG1 - 1:2 MC/BP MUX : Truth Table

PRG1_MC/BP_SEL	FUNCTION	
LOW	A port = B1 port	(default)
HIGH	A port = B2 port	

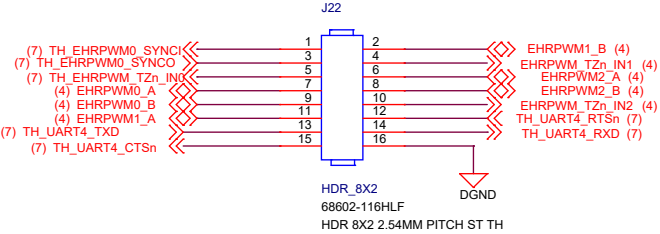


BOARD ID EEPROM

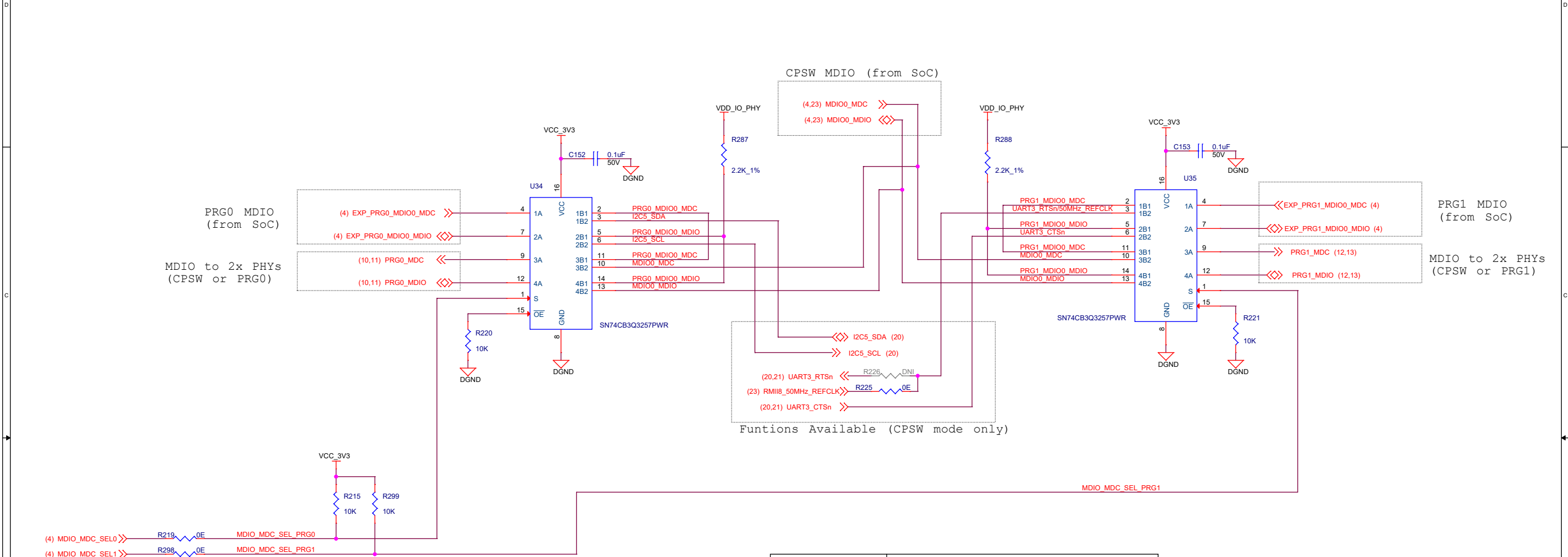


Note: EEPROM Address is 0x52 (set by base board)

Test Connector

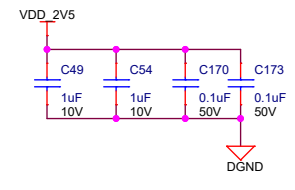


MDIO MDC MUX



MDIO_MDC_SEL	MDIO/MDC PORT CONNECTION TO PHY's
LOW	PRGx MDIO/MDC
HIGH	CPSW9G MDIO/MDC

PRG0 GB_ETHERNET RGMII 1



(default)

RJ45

The schematic diagram illustrates the RJ45 interface circuit for the LPJG17512A0N1 module. The module's pins (A9-A14) are connected to the PRG0_RGMII1 signals (D0_P, D0_N, D1_P, D1_N, D2_P, D2_N, D3_P, D3_N) and the ACT_LED signal. The module also includes a yellow LED (RIGHT LED) and an orange/green LED (LEFT LED). The circuit is powered by VCC_3V3 and grounded to DGND. The module is labeled CON_RJ45-28_LPJG17512A0N1.

RESET LOGIC

(4,11,12,13,23) SOC_PORZ_OUT

(4,11) GPIO_PRG0_RGMII_RST

R246 0E

R245 DNI

DGND

U38

1 2 4

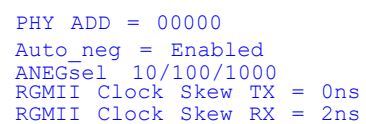
SN74LVC1G08DBVRE4

VDD_IO_PHY

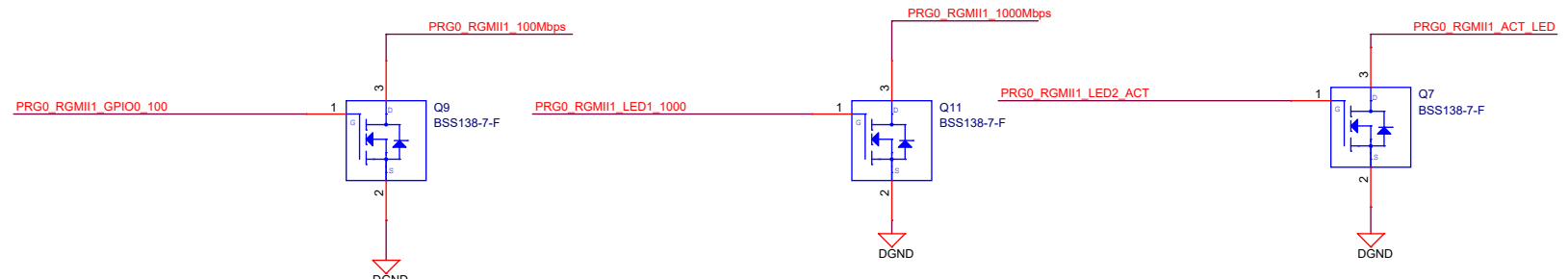
C50 0.1uF 50V

DGND

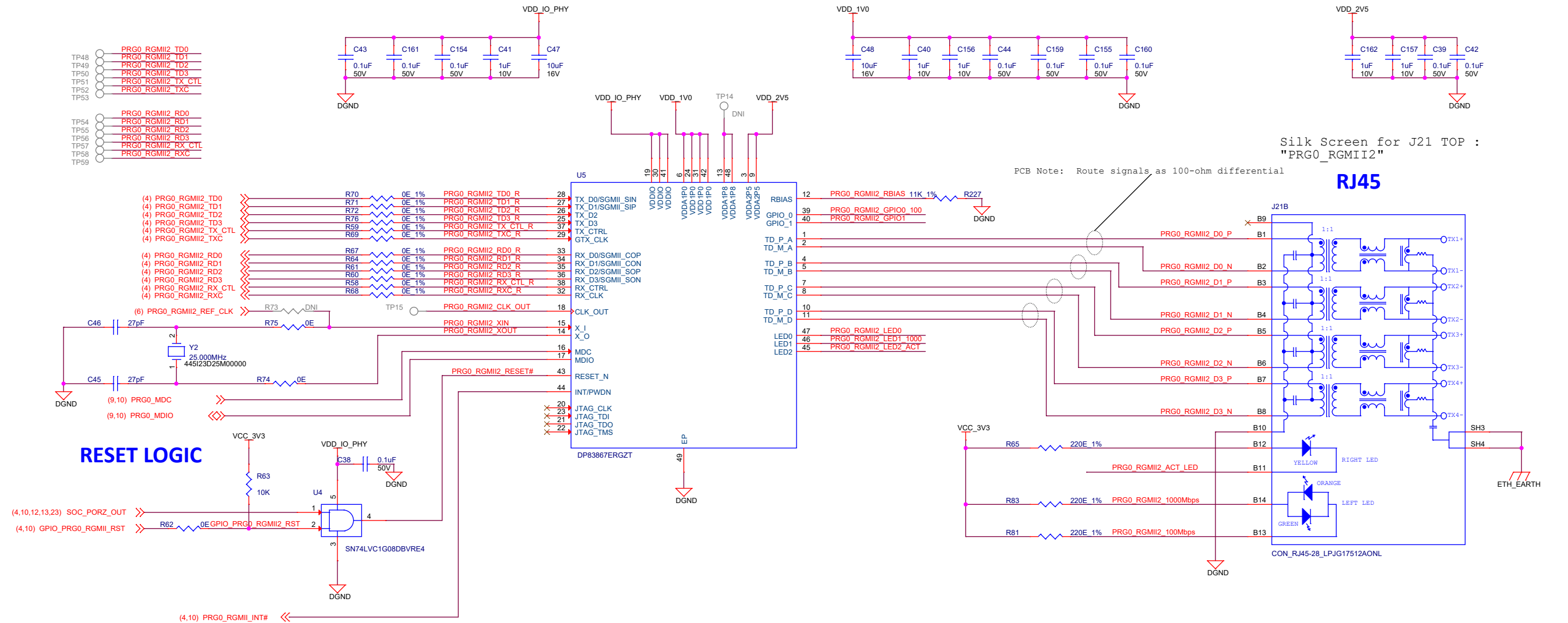
(4,11) PRG0_RGMII_INT#



RJ45-LED	FUNCTION
YELLOW	ACTIVITY
ORANGE	1000Mbps Speed
GREEN	100Mbps Speed

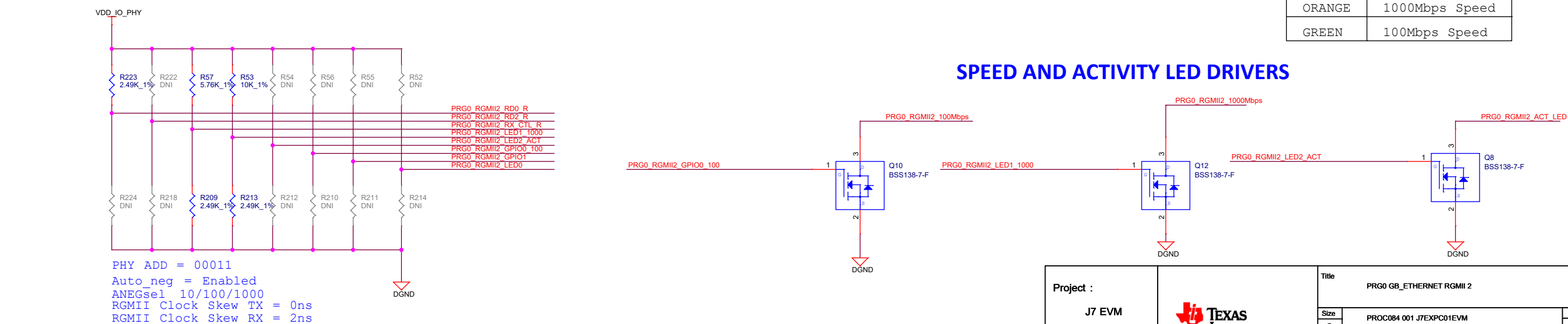


PRG0 GB_ETHERNET RGMII 2

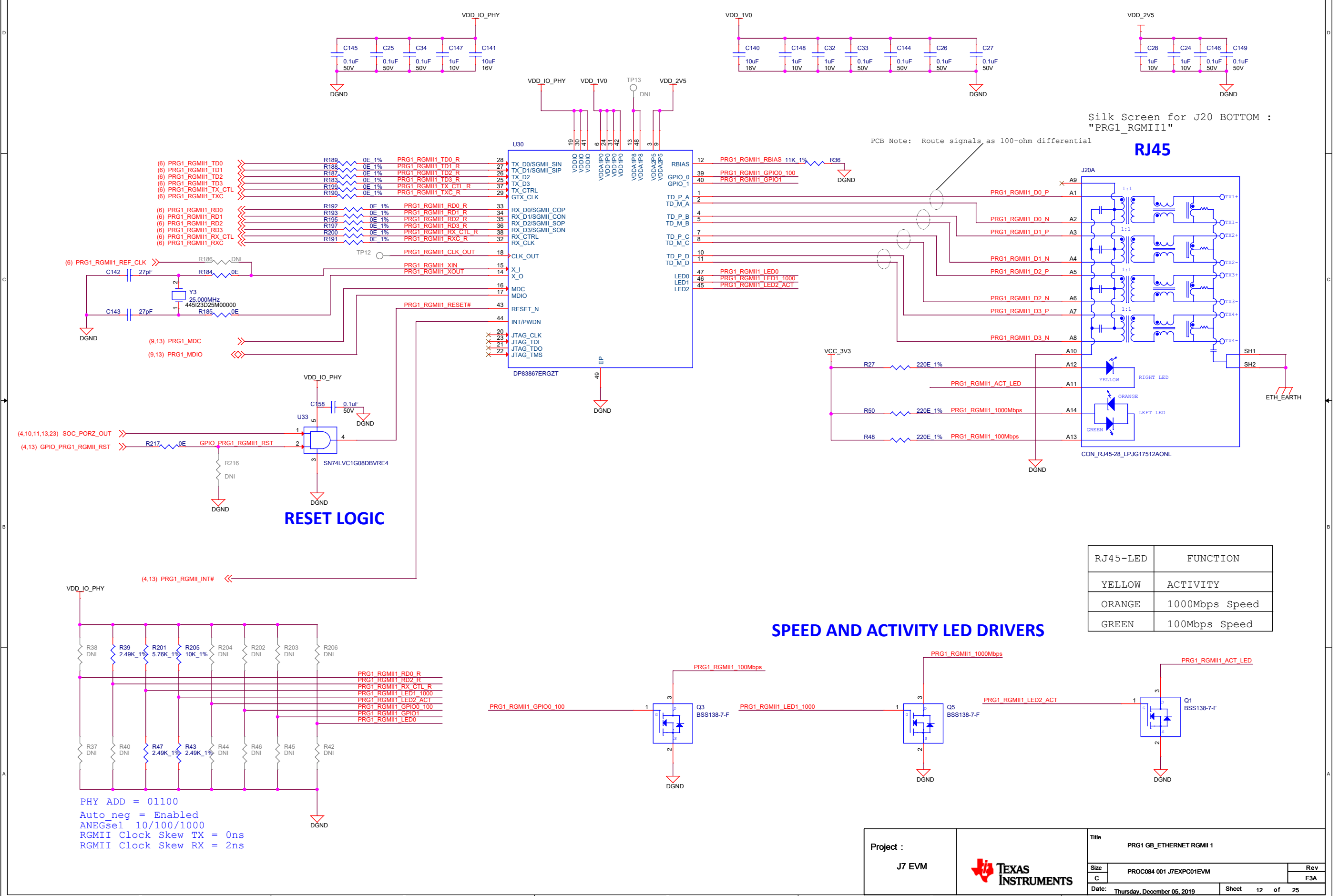


RJ45-LED	FUNCTION
YELLOW	ACTIVITY
ORANGE	1000Mbps Speed
GREEN	100Mbps Speed

SPEED AND ACTIVITY LED DRIVERS



PRG1 GB_ETHERNET RGMII 1



Silk Screen for J20 BOTTOM :
"PRG1_RGMII1"

PCB Note: Route signals as 100-ohm differential

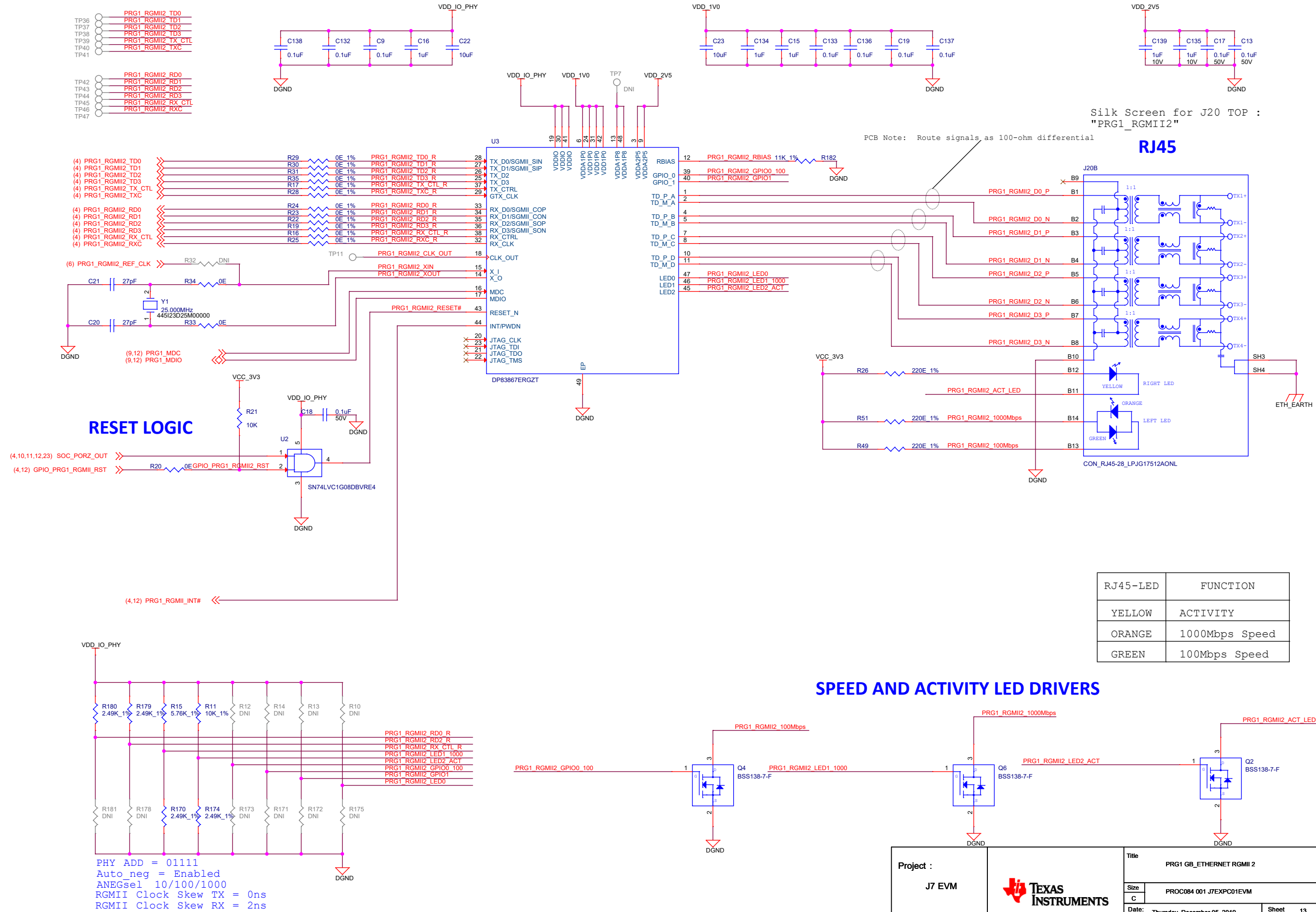
RJ45

RESET LOGIC

SPEED AND ACTIVITY LED DRIVERS

PHY ADD = 01100
Auto_neg = Enabled
ANEGsel 10/100/1000
RGMII Clock Skew TX = 0ns
RGMII Clock Skew RX = 2ns

PRG1_GB_ETHERNET RGMII 2



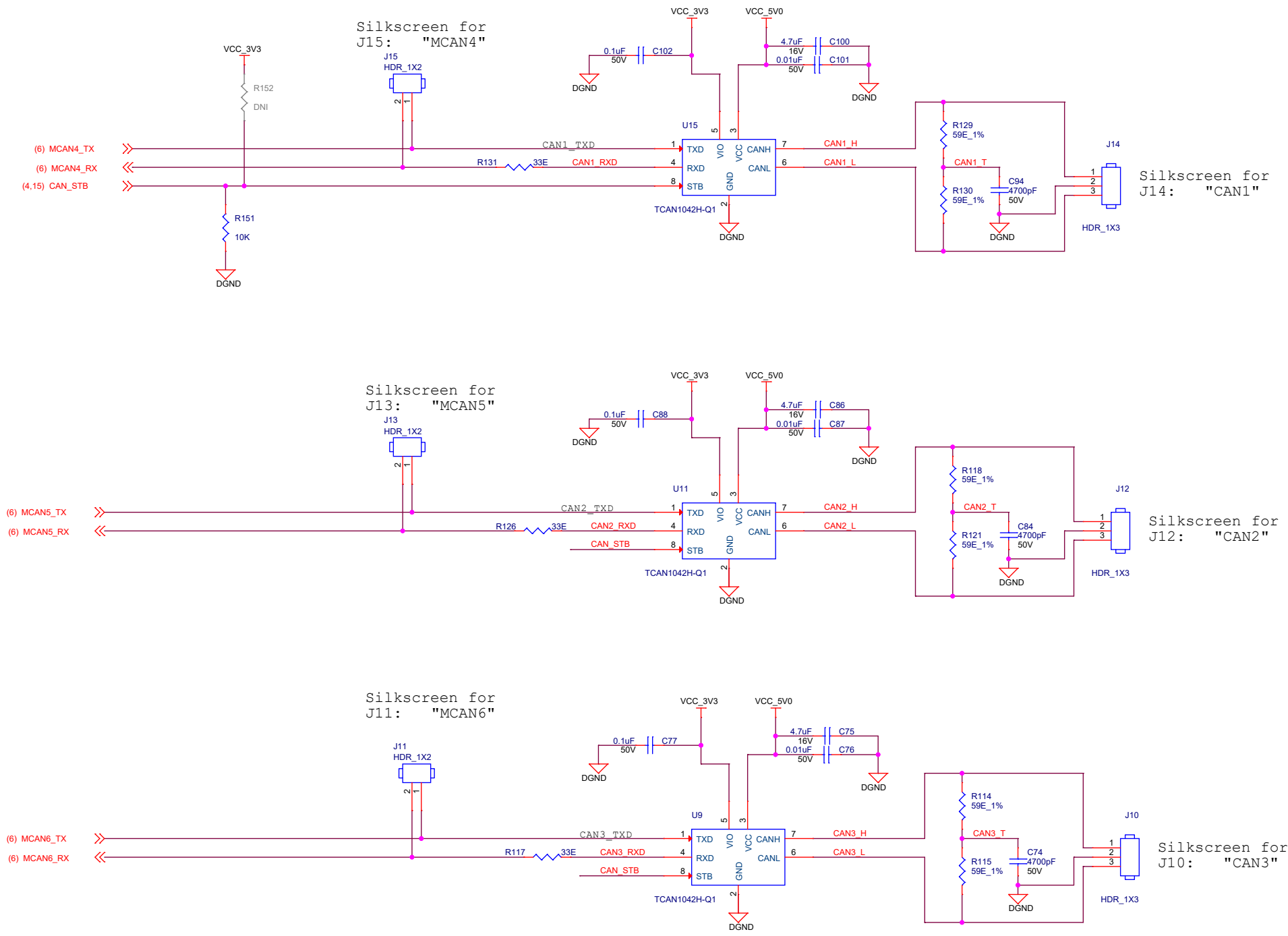
Silk Screen for J20 TOP :
"PRG1_RGMII2"

RJ45

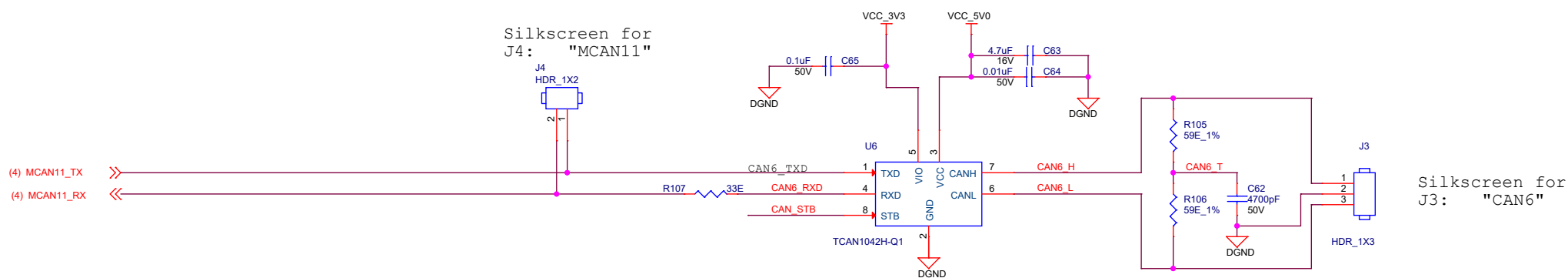
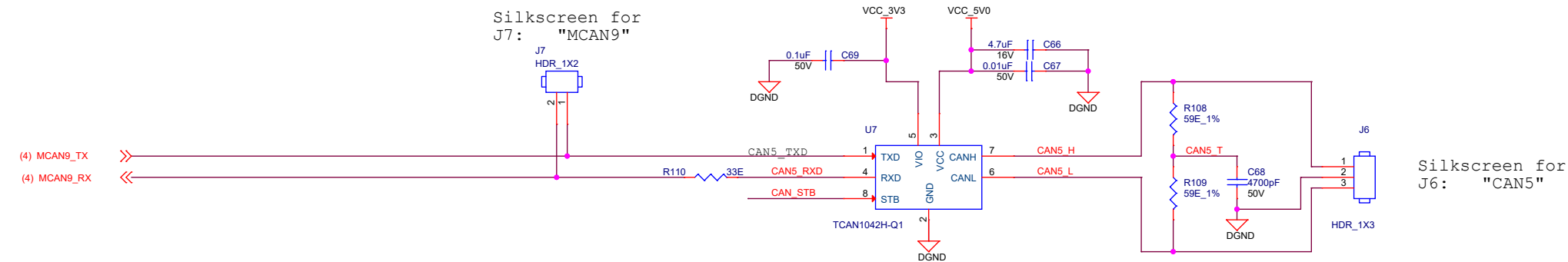
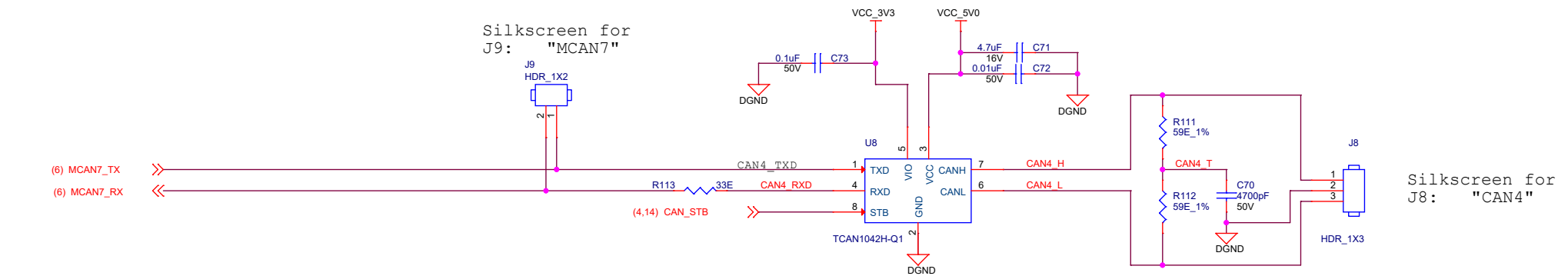
RJ45-LED	FUNCTION
YELLOW	ACTIVITY
ORANGE	1000Mbps Speed
GREEN	100Mbps Speed

SPEED AND ACTIVITY LED DRIVERS

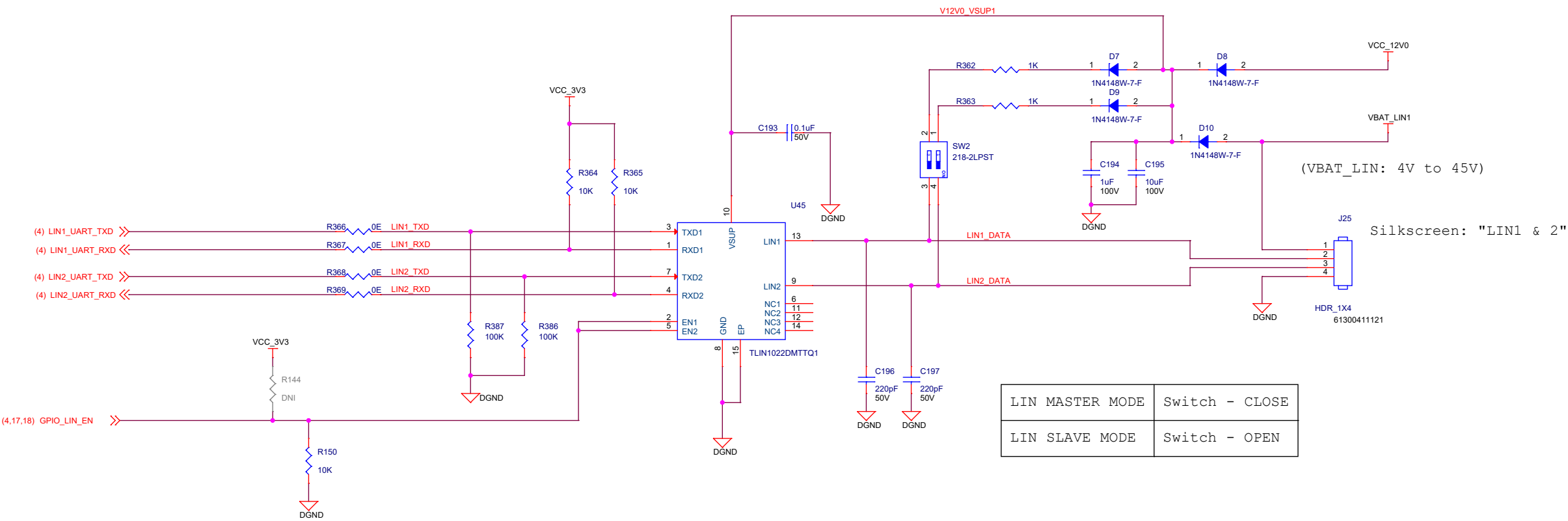
CAN TRANSCEIVERS - 01



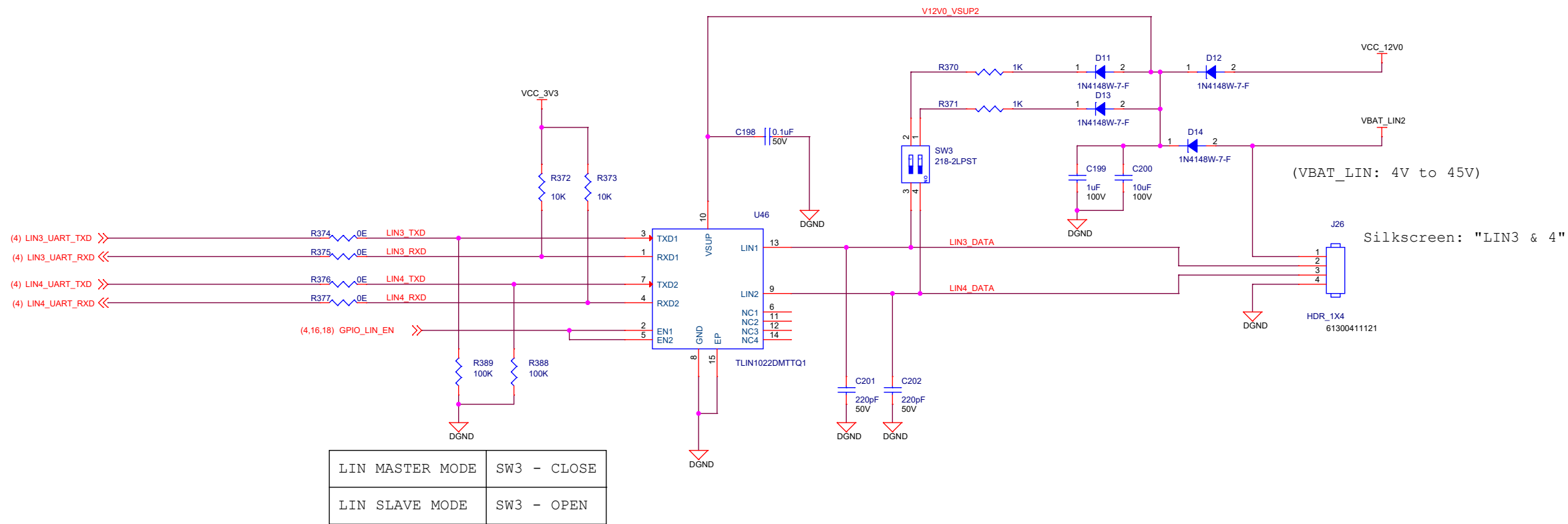
CAN TRANSCEIVERS - 02



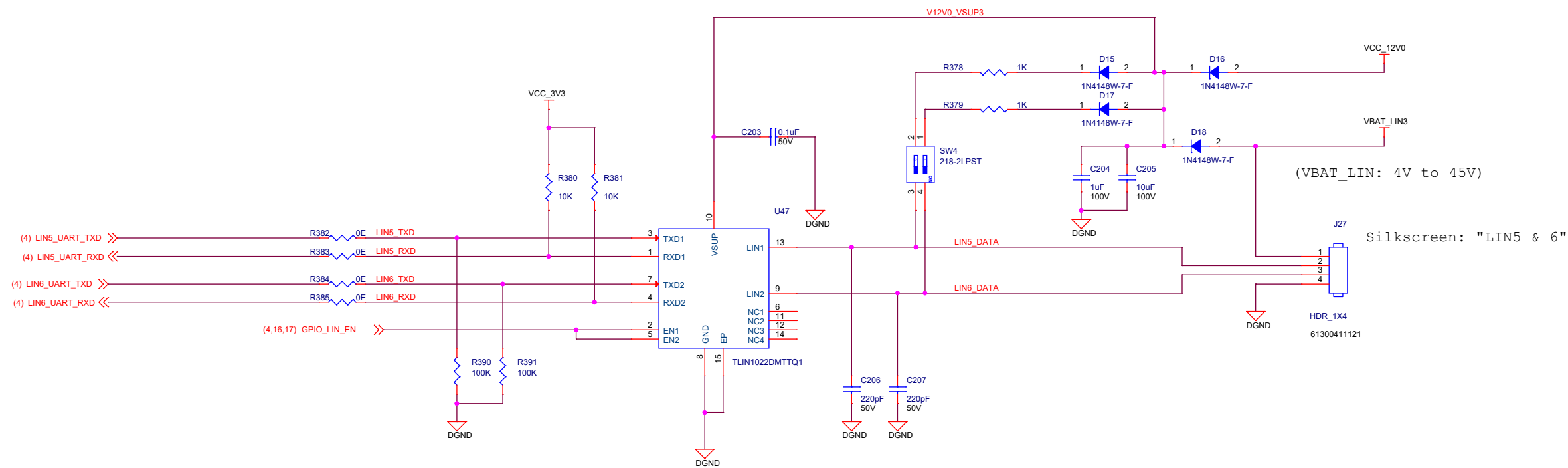
LIN INTERFACE - 01



LIN INTERFACE - 02

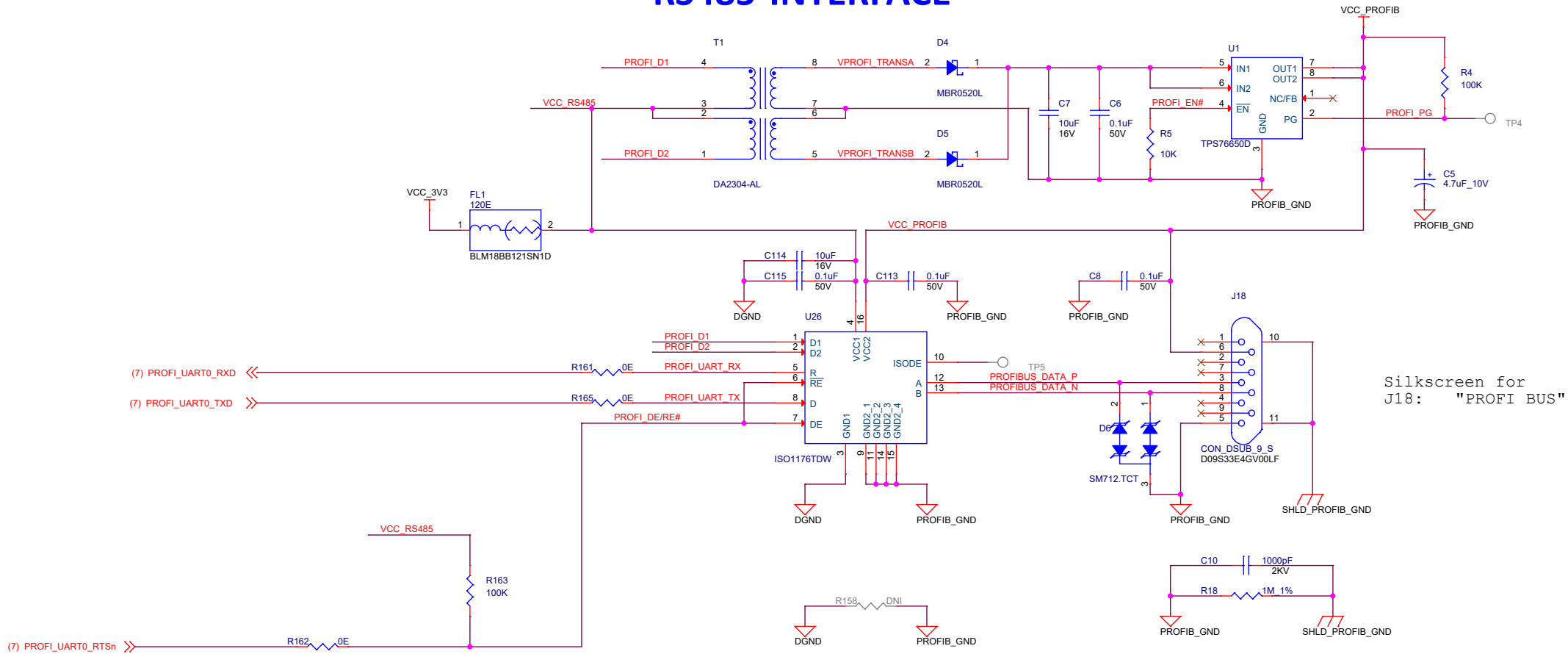


LIN INTERFACE - 03

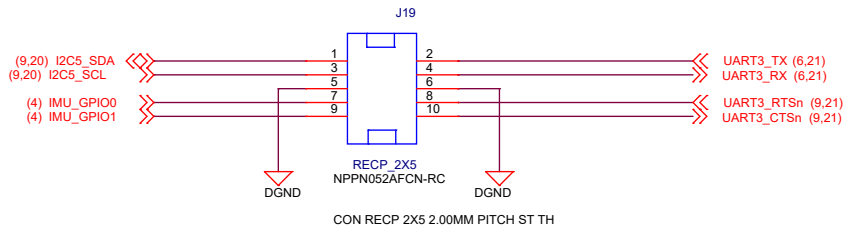


LIN MASTER MODE	SW4 - CLOSE
LIN SLAVE MODE	SW4 - OPEN

RS485 INTERFACE

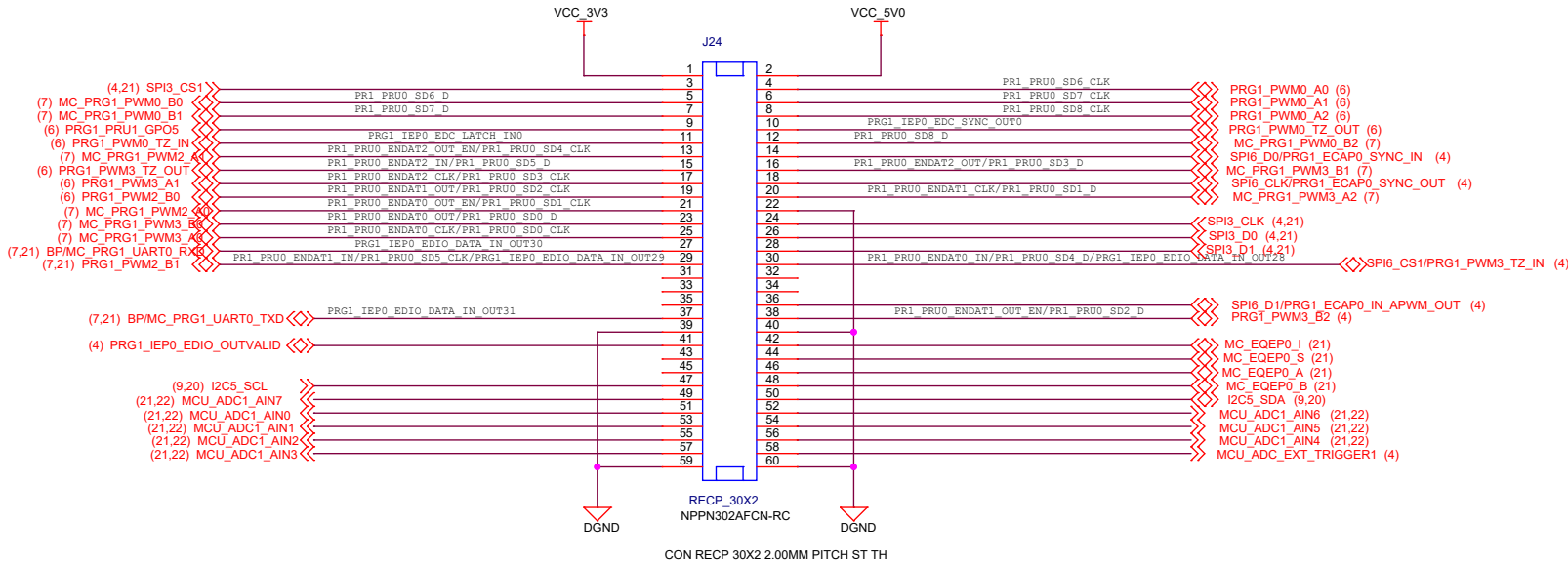


USS/IMU SENSOR HEADER



Silkscreen for J19:
"IMU/USS HDR"

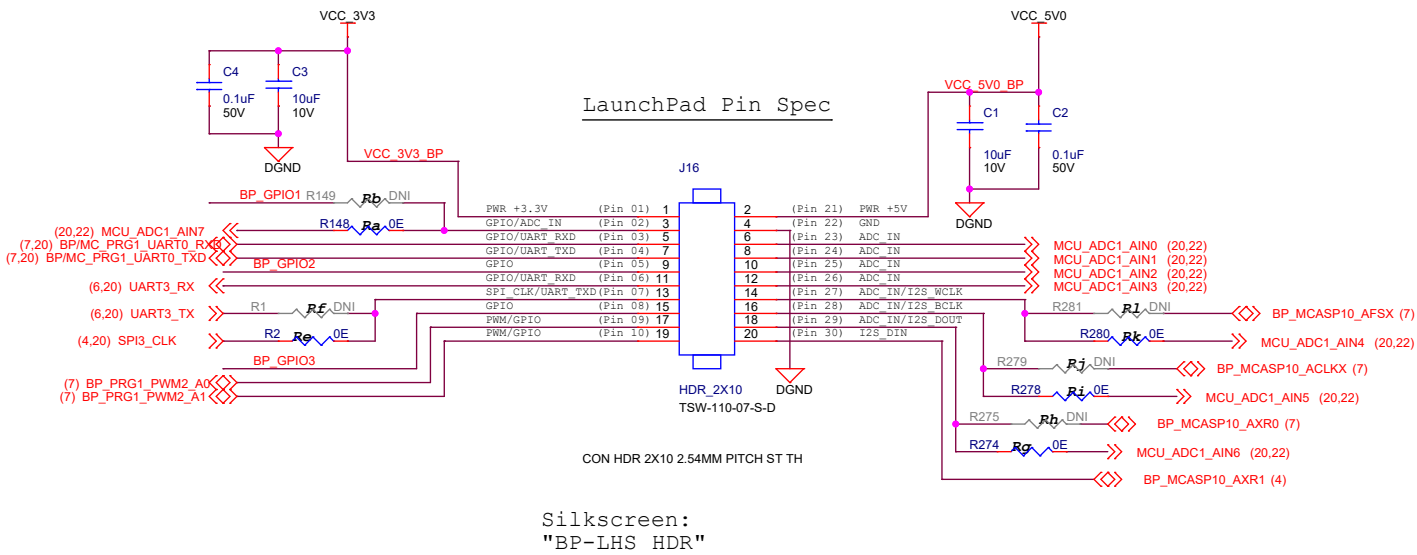
MOTOR CONTROL HEADER



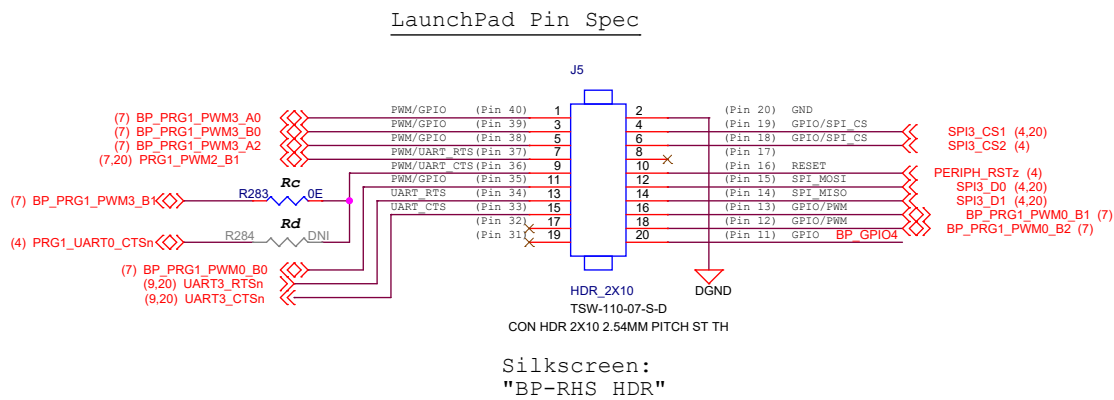
Silkscreen for J24:
"MOTOR CNTRL HDR"

GESI LAUNCHPAD- BOOSTERPACK INTERFACE HEADERS

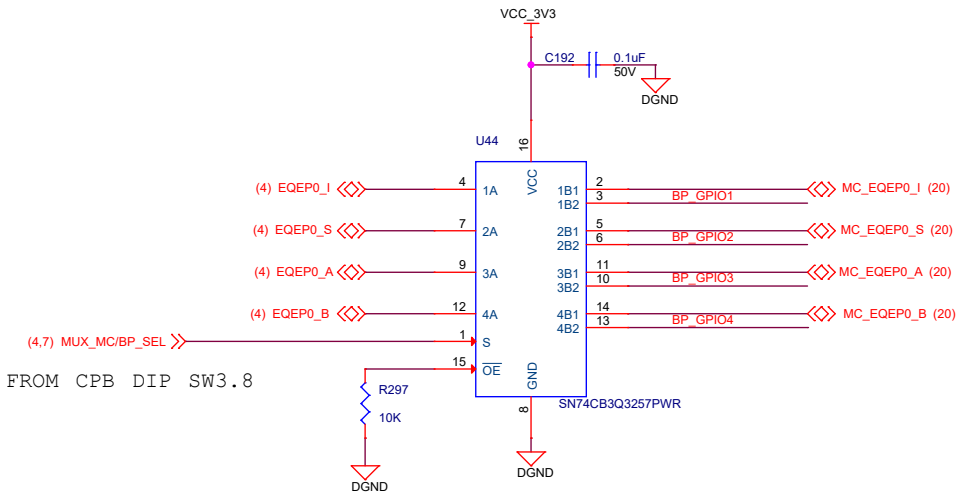
BOOSTER PACK I/F LHS CONN.



BOOSTER PACK I/F RHS CONN.

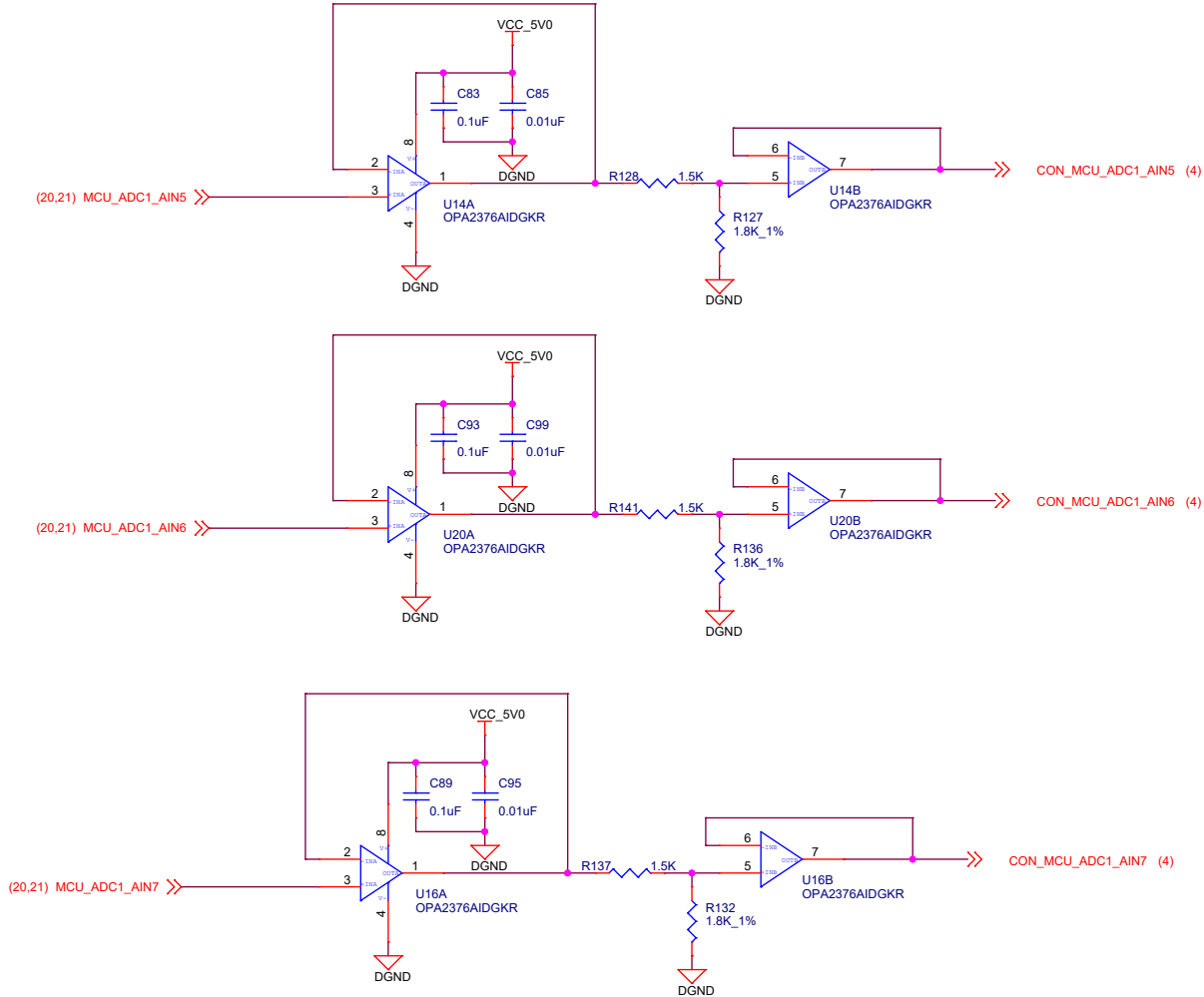
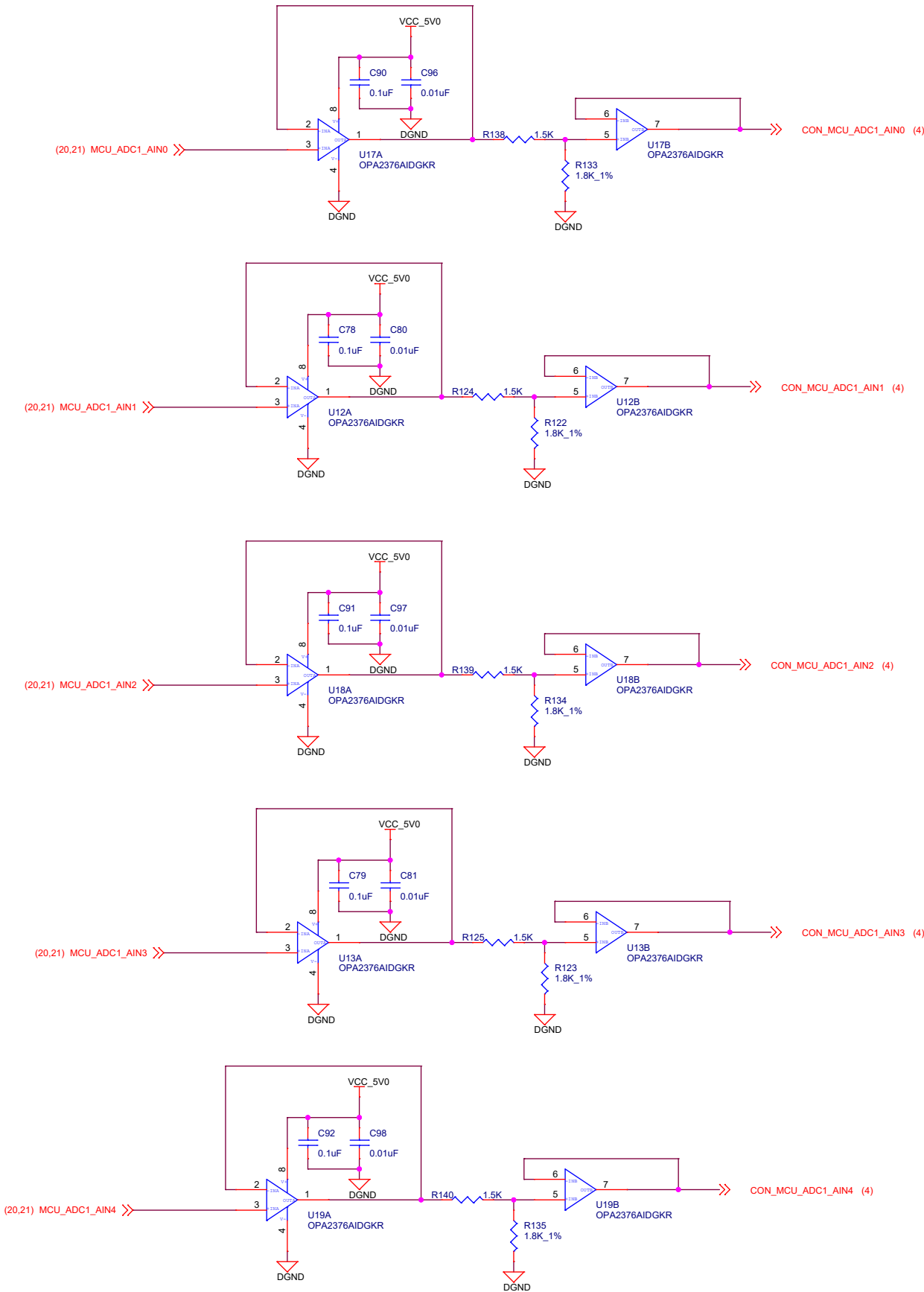


NOTE: Except BOOST-DRV8848 all other below listed BP interfaces supported similar to maxwell EVM

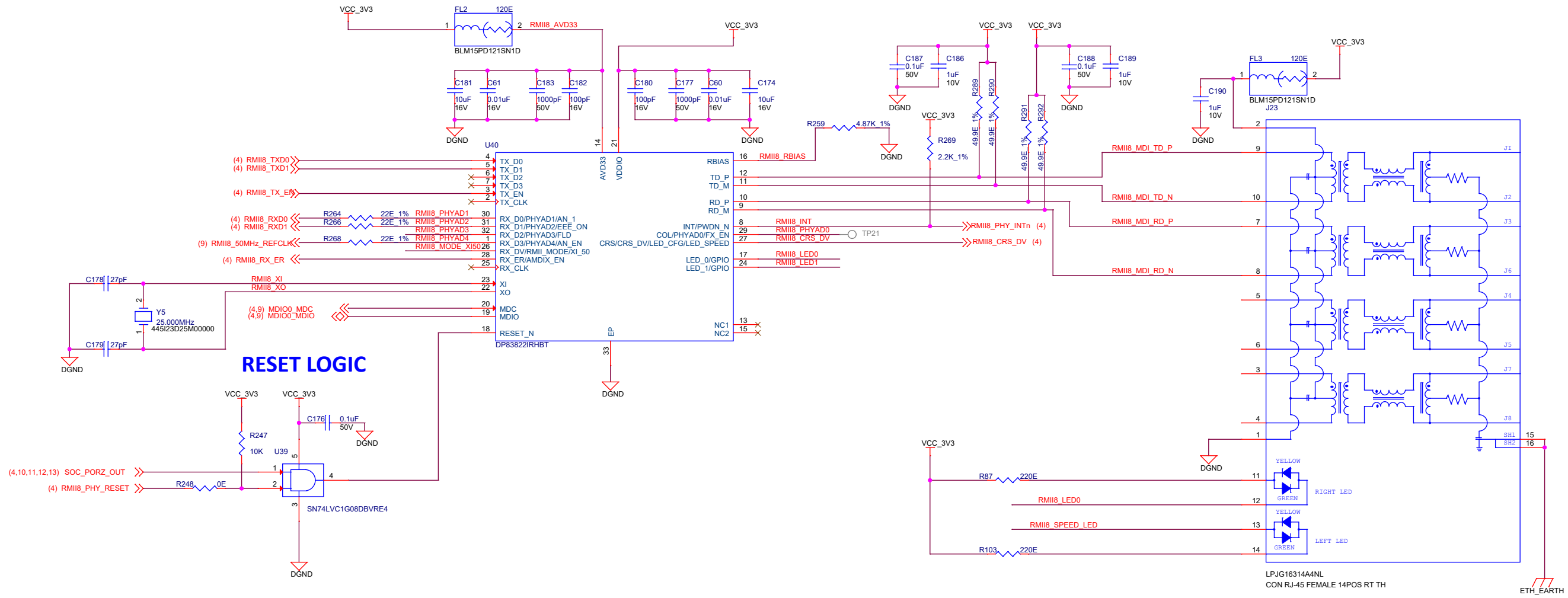


S.No	Supported Booster Packs	Part to be mounted	Part not be mounted
1	BOOSTXL-ULN2003	Ra	Rb
2	BOOST-DRV8711	Rb	Ra
3	BOOSTXL-DRV8301	Rc	Rd
4	CC3100BOOST	Rd	Rc
5	BOOST-CC2564MODA	Rd Rf Rh Rj Rl	Rc Re Rg Ri Rk

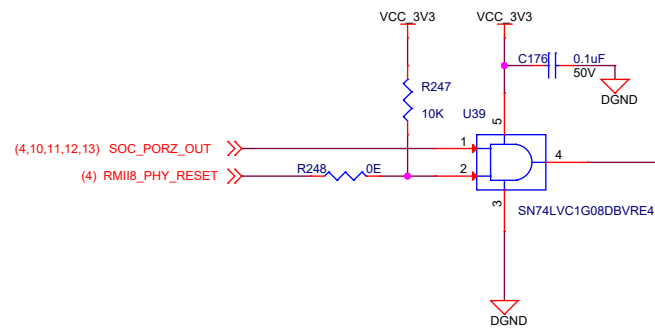
ADC IN



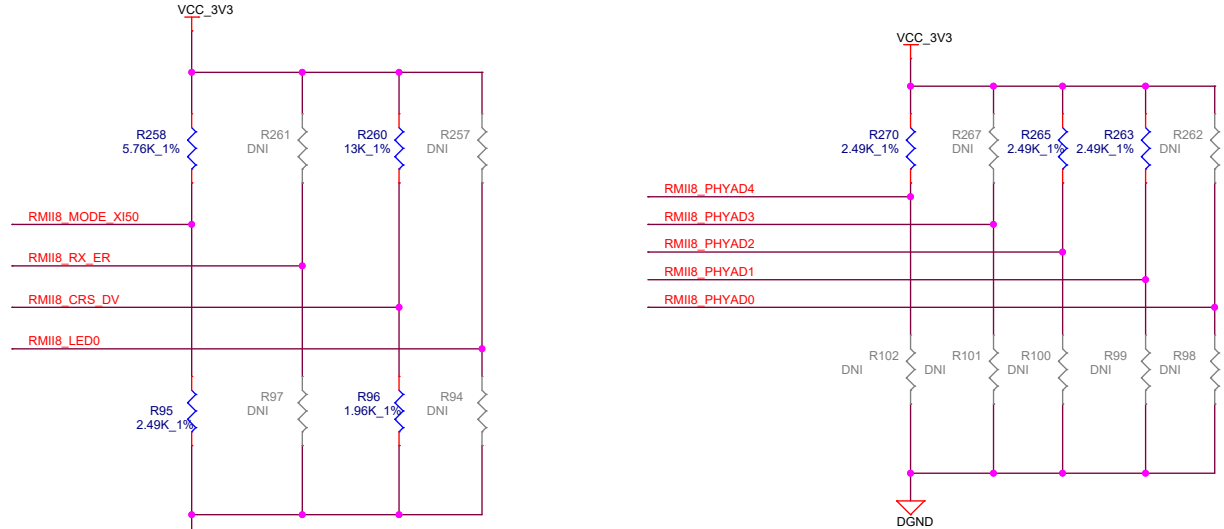
RMII8 INTERFACE



RESET LOGIC

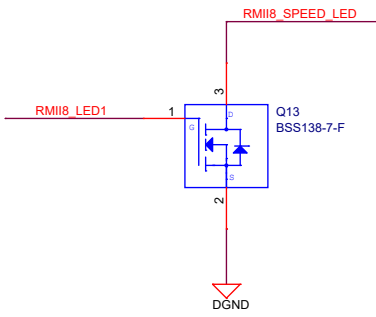


RESISTOR STRAPPING



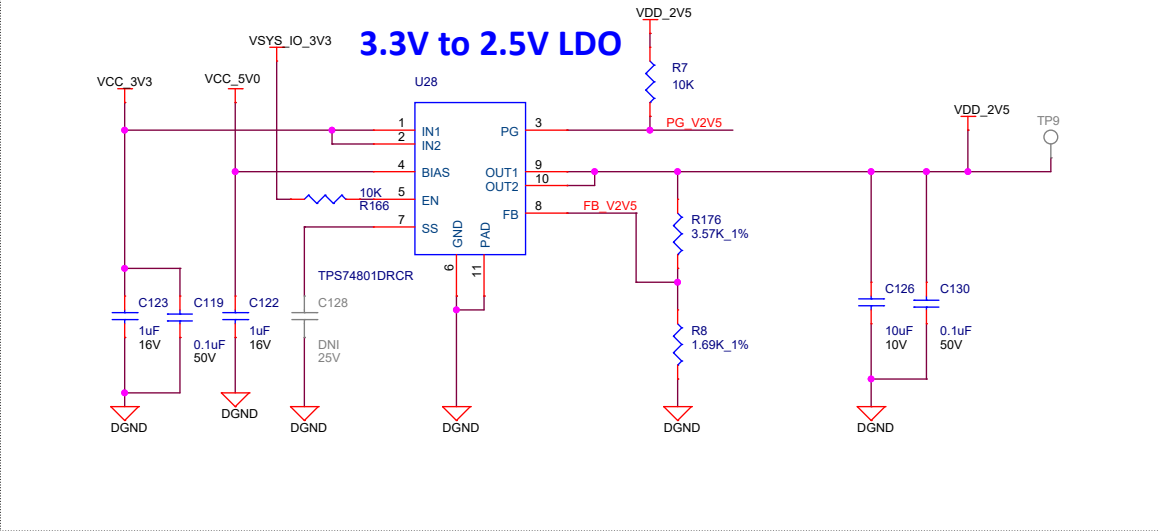
PHY ADD : 10111

PHY	Address	
QSGMII_PHY0	10000	0x10
QSGMII_PHY1	10001	0x11
QSGMII_PHY2	10010	0x12
QSGMII_PHY3	10011	0x13
PRG0_RGMII1	00000	0x00
PRG0_RGMII2	00011	0x03
PRG1_RGMII1	01100	0x0C
PRG1_RGMII2	01111	0x0F
RMII8	10111	0x17

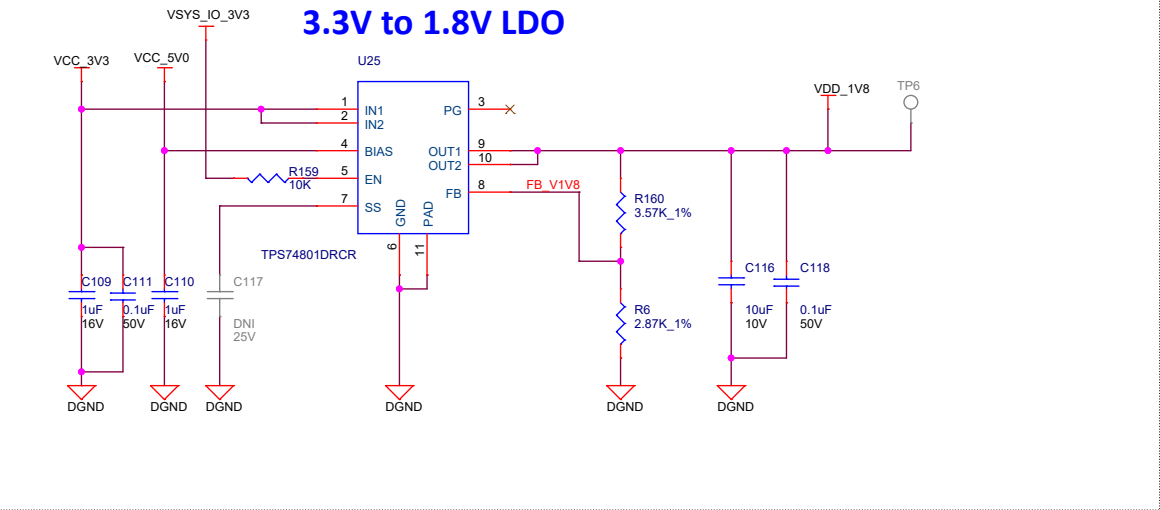


POWER SUPPLY

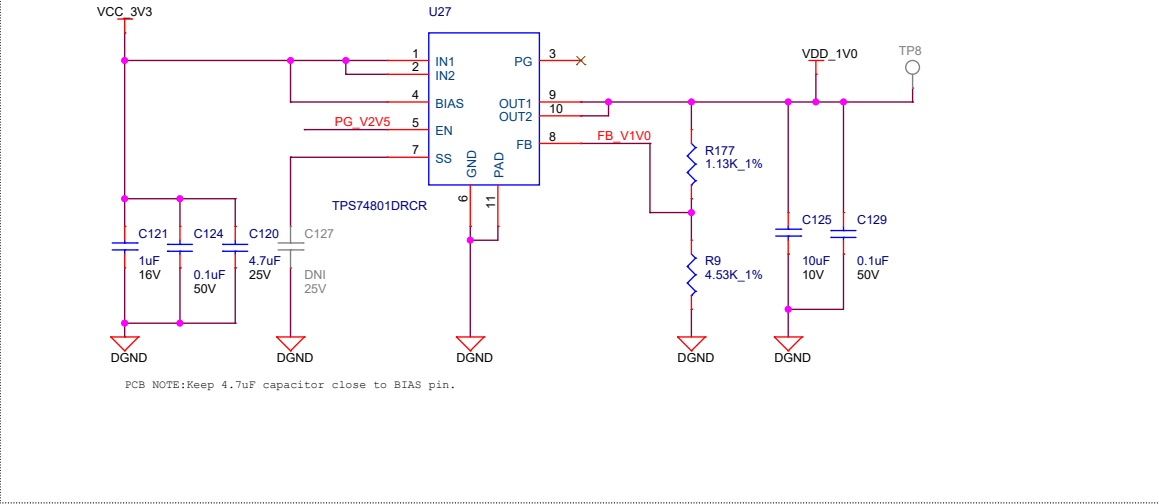
ETHERNET POWER



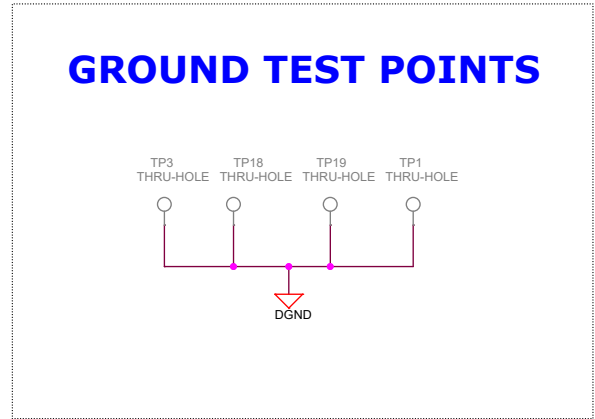
3.3V to 1.8V LDO



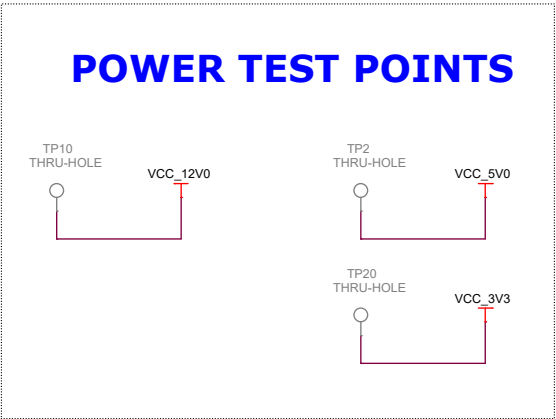
3.3V to 1.0V LDO



GROUND TEST POINTS



POWER TEST POINTS



HARDWARE SCHEMATICS

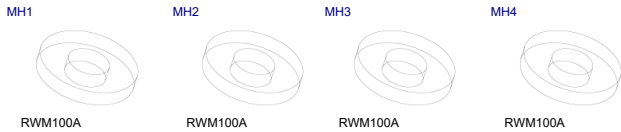
ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

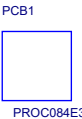
FIDUCIALS



WASHERS



BARE PCB



LABELS

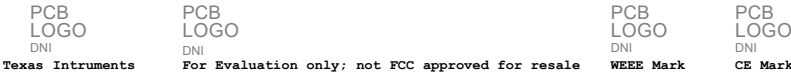
Board Serial No.



Assembly Revision.



LOGOs



Project :

J7 EVM



Title
HARDWARE SCHEMATICS

Size
C
PROC084 001 J7EXPC01EVM

Rev

E3A

Date: Thursday, December 05, 2019

Sheet 25 of 25