



**Customer :** Texas Instruments  
**Part Num :** DAC31X2EVM  
**Part Rev :** B

**Job Name :** TI\_DAC31X2EVM  
**Engineer :** David Gorden  
**Facility :** Toronto

Layer	Calc Thickness	Primary Stack	Description
Layer - 1	0.0005 0.0020		Taiyo 4000-MP 1/2oz Sig (Std Plt)
	0.0077		N4000-13
Layer - 2	0.0012		1oz P/G
	0.0050		N4000-13
Layer - 3	0.0012		1oz P/G
	0.0059		N4000-13
	0.0160		N4000-13
	0.0059		N4000-13
Layer - 4	0.0012		1oz P/G
	0.0050		N4000-13
Layer - 5	0.0012		1oz P/G
	0.0077		N4000-13
Layer - 6	0.0020 0.0005		1/2oz Sig (Std Plt) Taiyo 4000-MP

Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	0.0620	0.0062	0.0062	0.0630
Incl. Mask over Laminate	0.0580	0.0058	0.0058	0.0590
Incl. Plating	0.0610	0.0061	0.0061	0.0620
After Lamination	0.0582	0.0029	0.0029	0.0592
Over Laminate	0.0570	0.0057	0.0057	0.0580

Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol	Predict
1  Surface MS	L1	0.0150	0.0150	-	-	50	5.0	49.58
	-	-	-	-	L2			
2  EC Microstrip	L1	0.0070	0.0075	0.0130	-	100	10.0	99.37
	-	0.0070	0.0075	-	L2			
3  Surface MS	L6	0.0150	0.0150	-	L5	50	5.0	49.58
	-	-	-	-	-			
4  EC Microstrip	L6	0.0070	0.0075	0.0130	L5	100	10.0	99.37
	-	0.0070	0.0075	-	-			