Design Guide: TIDA-050088

Radiation-Tolerant Power Reference Design for the Versal™ AI Edge

Description

This is a radiation-tolerant power architecture reference design for the Versal™ AI Edge XQRVE2302 from AMD. The Versal Edge is an adoptive system-on-chip (SoC) for space applications which enables high levels of performance in a small form factor. Robust power delivery is critical to fully use this design in a space environment. This power design has multiple devices to power the various rails along with a sequencer to properly order and monitor the rails.

Resources

TIDA-050088	Design Folder
TPS7H5006-SEP, TPS7H6025-SEP	Product Folder
TPS7H1111-SEP, TPS7H4010-SEP	Product Folder
TPS73801-SEP, TPS7H3302-SEP	Product Folder
TPS7H3014-SP, TPS7H2221-SEP	Product Folder
SN54SC6T14-SEP	Product Folder

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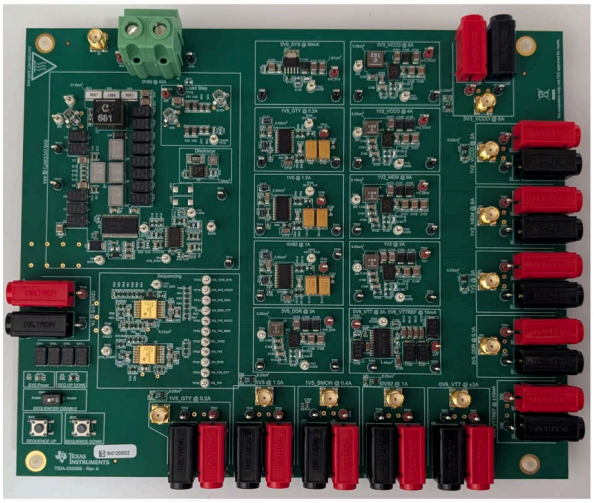
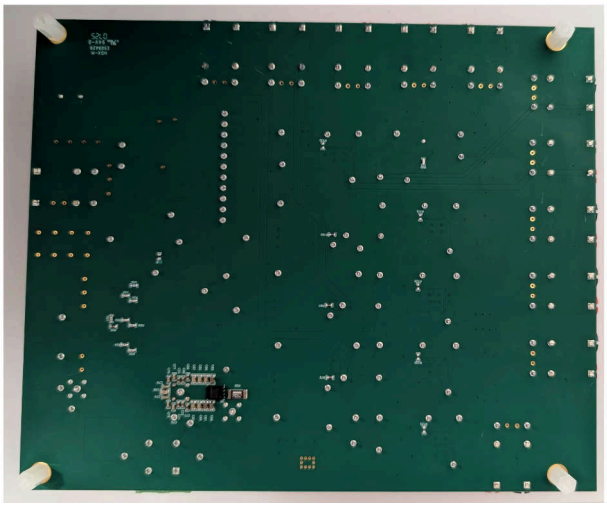
Features

- Radiation-tolerant power architecture by TI
- Designed to power the Versal AI Edge XQRVE2302 from AMD
- Power sequencing and discharge circuitry to sequence up and down all rails
- Core rail capable of 0.8V at 44A
- Regulators for all auxiliary rails along with DDR memory termination

Applications

- Satellite electric power system (EPS)
- Communications payload





1 System Description

A radiation-tolerant power architecture is described for the Versal™ AI Edge XQRVE2302 from AMD. The Versal Edge is an adoptive SoC for space applications which enables high levels of performance in a small form factor. Robust power delivery is critical to fully utilize this design in a space environment. This power design uses multiple devices to power the various rails along with a sequencer to properly order and monitor the rails.

1.1 Key System Specifications

The rails in the system, listed in Table 1-1, are all powered from a 12V input called the 12V0_SYS rail.

Table 1-1. Versal™ Edge and DDR4 Specifications

RAIL SEQUENCE	RAIL NAME(1)	VERSAL EDGE PINS, DDR POWERED	RAIL CURRENT	DC ACCURACY	AC ACCURACY	COMBINED ACCURACY(2)	LOAD STEP	PARTS
0(3)	5V0_SYS	–	–	–	–	–	–	TPS73801-SEP
1	3V3_VCCO	HDIO (bank 302) PSIO (bank 50x)	4A	±1%	–5%, +3%	-6%, +4%	4A at 10A/µs	TPS7H4010-SEP
	2V5_DDR_VPP	DDR_VPP	0.1A	–5%, +10%	–	N/A	–	TPS7H4010-SEP
	1V2_MEM	DDR_VDDQ	3A	±5%	–	N/A	–	TPS7H4010-SEP
	1V2_VCCO	XPIO (bank 7xx)	2A	±1%	±5%	±6%	2A at 10A/µs	TPS7H4010-SEP
	VTT (0V6)	DDR4_VTT	±3A	±5%	–	N/A	–	TPS7H3302-SEP
	VTTREF (0V6)	DDR4_VTTREF	±10mA	±1% to VTTSNS	±1%	N/A	–	
2	0V80	VCCINT VCC_IO VCC_SOC VCC_RAM VCC_PMC VCC_PSLP	44A	±1%	±17mV	±3.125%	11A at 200A/µs	TPS7H5006-SEP TPS7H6025-SEP 5xEPC7019G
3	1V5	VCCAUX_SMON VCCAUX_PMC	1.5A	±1%	±2%	±3%	900mA at 10A/µs	TPS7H1111-SEP
4	0V92	VGTYP_AVCC	1A	±2%	±10mV	±3.09%	195mA at 10A/µs	TPS7H1111-SEP
5	1V5_GTY	VGTY_AVCCAUX	0.1A	±2%	±10mV	±2.67%		TPS7H1111-SEP
6	1V2	VGTY_AVTT VGTY_AVTTRCAL	1.3A	±2%	±10mV	±2.83%	330mA at 10A/µs	TPS7H4010-SEP

(1) This is the maximum expected current for the FPGA or DDR. See the power tree in Table 2-1 for the designed current which can be greater than this rail current for margin and powering of other loads. As rail requirements can differ by application, consult the AMD Power Design Manager (PDM) and the DDR specifications for additional information.
(2) This is the combined AC and DC accuracy that is targeted for the Versal Edge rails.
(3) This is not part of the sequencing, the rail comes up as soon as 12V0_SYS is applied.

2 System Overview

2.1 Block Diagram

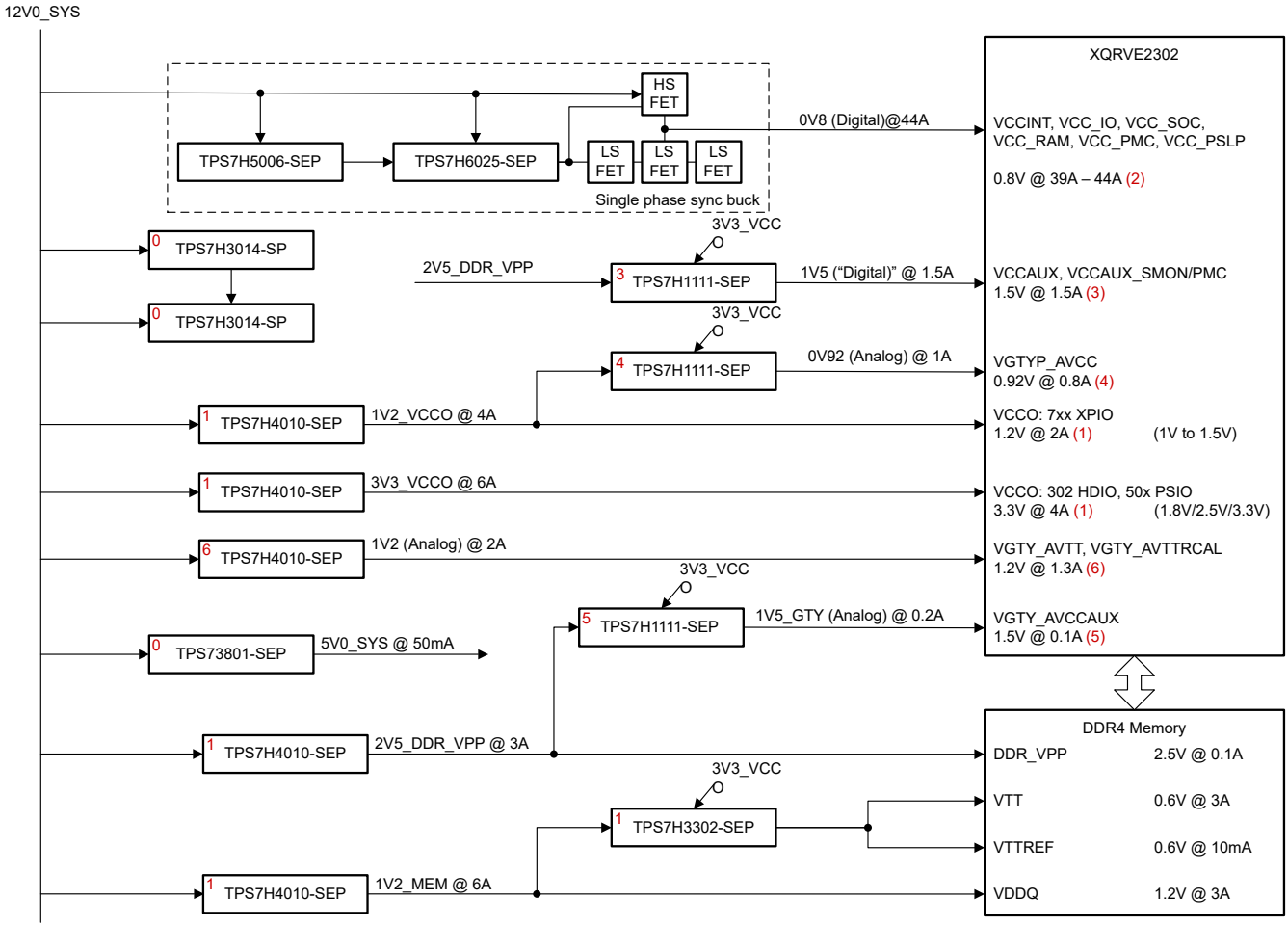


Figure 2-1. TIDA-050088 Block Diagram

2.2 Design Considerations

Using the sequencing and loads described in Table 1-1, a power tree is created as described in Table 2-1.

Table 2-1. Power Tree Specifications

RAIL SEQUENCE	RAIL NAME	PARTS	TOTAL RAIL DESIGN CURRENT(1)	LOADS	EXPECTED MAXIMUM LOAD CURRENTS
0(2)	5V0_SYS	TPS73801-SEP	50mA	Sequencers pullups	10mA
				TPS7H2221 input	0.2mA
				SN54SC6T14-SEP input	15mA
1	3V3_VCCO	TPS7H4010-SEP	6A	Versal HDIO and PSIO	4A
				TPS7H1111-SEP Bias rails	81mA
				TPS7H3302-SEP VDD	30mA
	2V5_DDR_VPP	TPS7H4010-SEP	3A	DDR_VPP	0.1A
				TPS7H1111-SEP input for 1V5	1.5A
				TPS7H1111-SEP input for 1V5_GTY	0.2A
	1V2_MEM	TPS7H4010-SEP	6A	DDR_VDDQ	3A
				TPS7H3302-SEP VLDOIN	3A
	1V2_VCCO	TPS7H4010-SEP	4A	Versal XPIO	2A
				TPS7H1111-SEP input for 0V92	1A
	VTT (0V6)	TPS7H3302-SEP	±3A	DDR4_VTT	±3A
	VTTREF (0V6)		±10mA	DDR4_VTTREF	±10mA
2	0V80	TPS7H5006-SEP TPS7H6025-SEP 5xEPC7019G	44A	Versal VCCINT and associated rails	44A
3	1V5	TPS7H1111-SEP	1.5A	Versal VCCAUX_SMON and VCCAUX_PMC	1.5A
4	0V92	TPS7H1111-SEP	1A	Versal VGTYP_AVCC	0.8A
5	1V5_GTY	TPS7H1111-SEP	0.2A	Versal VGTY_AVCCAUX	0.1A
6	1V2	TPS7H4010-SEP	2A	Versal VGTY_AVTT and VGTY_AVTTRCAL	1.3A

(1) This is the maximum design current which can be larger than the expected load currents due to adding design margin.
(2) This is not part of the sequencing, the rail comes up as soon as 12V0_SYS is applied.

This design uses radiation-tolerant parts rated to at least a total ionizing dose (TID) of 20krad(Si) and single-event effects (SEE) of at least 43MeV-cm^2/mg. These ratings provide an excellent choice for many satellite power systems in Low Earth Orbit (LEO). For higher radiation needs, many of the TI parts have radiation-hardened equivalents.

2.3 Highlighted Products

The following sections describe key features of the devices utilized for this power design.

2.3.1 TPS7H5006-SEP

The TPS7H5006-SEP is a radiation-tolerant PWM controller which is part of the TPS7H500x-SP and TPS7H500x-SEP family of high-speed controllers. The controllers provide a number of features that are beneficial for the design of DC-DC converter topologies intended for space applications. The controllers have a 0.613V +0.7%, –1% accurate internal reference and configurable switching frequency up to 2MHz. Each device offers programmable slope compensation and soft-start.

The TPS7H500x-SP series can be driven using an external clock through the SYNC pin or by using the internal oscillator at a frequency programmed by the user. The controller family offers the user various options for switching outputs, synchronous rectification capability, dead time (fixed or configurable), leading edge blank time (fixed or configurable), and duty cycle limit.

The TPS7H5006-SEP is used in this design as the buck controller for the high-current, VCCINT rail. The radiation-hardened TPS7H500x-SP is also available in both QMLV ceramic packages and QMLP plastic packages.

2.3.2 TPS7H6025-SEP

The TPS7H6025-SEP is a radiation-tolerant GaN FET gate driver which is designed for high-frequency, high-efficiency, and high-current applications. The TPS7H6025-SEP is part of the TPS7H60x5 series of gate drivers which consists of the TPS7H6005 (200V rating), the TPS7H6015 (60V rating), and the TPS7H6025 (22V rating). The drivers feature adjustable dead-time capability, small 30ns propagation delay, and 5.5ns high-side and low-side matching. These parts also include internal high-side and low-side LDOs, which provide a drive voltage of 5V regardless of supply voltage. The TPS7H60x5 drivers all have split-gate outputs, providing flexibility to adjust the turn-on and turn-off strength of the outputs independently.

The TPS7H60x5 drivers feature two control input modes: independent input mode (IIM) and PWM mode. In IIM each of the outputs is controlled by a dedicated input. In PWM mode, two complementary outputs signals are generated from a single input and the user can adjust the dead time for each edge. The drivers can also be utilized for both half-bridge and dual-low side converter applications.

The TPS7H6025-SEP is used in this design to drive the GaN FETs which are part of the buck regulator for the high-current, VCCINT rail. The radiation-hardened TPS7H60x5-SP is also available in QMLP plastic packages. Additionally, the radiation-hardened TPS7H60x3-SP is available in QMLV ceramic packages.

2.3.3 TPS7H1111-SEP

The TPS7H1111 is a radiation-tolerant ultra-low noise, high PSRR, low dropout linear regulator (LDO) optimized for powering radio-frequency (RF) devices. The device is capable of sourcing up to 1.5A over a 0.85V to 7V input range with a 2.2V to 14V bias supply.

The high performance of the device limits power-supply generated phase noise and clock jitter, making this device an excellent choice for powering high-performance ADCs, DACs, VCOs, PLLs, SerDes, and other RF components in satellites. For digital loads (such as FPGAs and DSPs) requiring low-voltage operation, the exceptional accuracy and excellent transient performance provide optimized system perform.

The radiation-tolerant TPS7H1111-SEP is utilized in this design whenever an LDO is required for one of the Versal rails. The radiation-hardened TPS7H1111-SP is also available in both a QMLV ceramic package and QMLP plastic package.

2.3.4 TPS7H4010-SEP

The TPS7H4010-SEP is a radiation-tolerant synchronous buck converter capable of outputting up to 6A of load current from a supply voltage ranging from 3.5V to 32V. The TPS7H4010-SEP provides exceptional efficiency and output accuracy in a very small size. Peak current-mode control is employed.

Additional features such as adjustable switching frequency, synchronization to an external clock, FPWM option, power-good flag, precision enable, adjustable soft start, and tracking provide both flexible and easy-to-use designs for a wide range of applications. Automatic frequency foldback at light load and optional external bias improve efficiency over the entire load range. The device requires few external components and has a pinout designed for simple PCB layout with optimized EMI and thermal performance. Protection features include thermal shutdown, input undervoltage lockout, cycle-by-cycle current limiting, and hiccup short-circuit protection.

2.3.5 TPS73801-SEP

The TPS73801-SEP is a radiation-tolerant low-dropout (LDO) linear regulator optimized for fast transient response. The device can supply 1A of output current with a dropout voltage of 300mV. Operating quiescent current is 1mA and drops to less than 1µA in shutdown.

The TPS73801-SEP regulator is available with an adjustable 1.21V reference voltage and an output voltage range from 1.21V to 20V. Internal protection circuitry includes current limiting, thermal limiting, and reverse-current protection.

The TPS73801-SEP is utilized in this design to create a low current, auxiliary 5V rail that is used for various housekeeping tasks.

2.3.6 TPS7H3302-SEP

The TPS7H3302 is a radiation-hardened double data rate (DDR) 3A termination regulator with built-in VTTREF buffer. The regulator is specifically designed to provide a compact, low-noise design for space-grade DDR termination applications such as single board computers, solid-state recorders, and payload processing.

The TPS7H3302 supports DDR VTT termination applications using DDR, DDR2, DDR3, DDR3L, and DDR4. The fast transient response of the TPS7H3302 VTT regulator allows for a stable supply during read and write conditions. The TPS7H3302 also includes a built-in VTTREF supply that tracks VTT to further reduce the design size. To enable simple power sequencing, both an enable input and a power-good output (PGOOD) have been integrated into the TPS7H3302.

The radiation-tolerant TPS7H3302-SEP is utilized in this design to power the DDR4 memory. The radiation-hardened TPS7H3302-SP is also available in a QMLP plastic package, and the TPS7H3301-SP is available in a QMLV plastic package.

2.3.7 TPS7H3014-SEP

The TPS7H3014 is an integrated, 3V to 14V, four-channel radiation-hardened power-supply sequencer. Channel count can be expanded by connecting multiple devices in a daisy-chain configuration. The device provides sequence up and down control signals for integrated circuits with active high (*on*) inputs. In addition SEQ_DONE and PWRGD flags are provided to monitor the sequence and power status of the monitored power tree.

An accurate 599mV ±1% threshold voltage and a 24µA ±3% hysteresis current provide programmable rise and fall monitoring voltages. The rise and fall delay time is globally programmed using a single resistor. Also, a time-to-regulation timer is provided to track the rising voltage on SENSEx. In addition to these features, a FAULT detection pin is incorporated to monitor internally generated faults and provide increased system level reliability for power sequencing space applications.

The radiation-hardened TPS7H3014-SP is utilized in this design to sequence the power rails. The radiation-tolerant TPS7H3014-SEP in a plastic package is also available (this part is not utilized in this TI design due to part availability during initial design).

2.3.8 TPS7H2221-SEP

The TPS7H2221-SEP device is a small, single channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1.6V to 5.5V and can support a maximum continuous current of 1.25A.

The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. When power is first applied, a Smart Pull Down is used to keep the ON pin from floating until system sequencing is complete. Once the pin is deliberately driven high ($V_{ON} > V_{IH}$), the Smart Pull Down is disconnected to prevent unnecessary power loss. The TPS7H2221-SEP load switch is also self-protected against short circuit events on the output of the device.

The TPS7H2221-SEP is used in this design as an output discharge for various voltage rails. This active discharge is needed to meet the sequence down timing specification for the Versal FPGA.

2.3.9 SN54SC6T14-SEP

The SN54SC6T14-SEP is a radiation-tolerant hex Schmitt-Trigger inverter. The device contains six independent inputs and the output voltage is referenced to the supply voltage. The device supports 1.2V, 1.8V, 2.5V, 3.3V, and 5V CMOS levels.

The input is designed with a lower threshold circuit to support up translation for lower voltage CMOS inputs. Additionally, the 5V tolerant input pins enable down translation.

The inverter is utilized in conjunction with the TPS7H3014-SP sequencer to drive the GaN FET which discharges the 0V8 (VCCINT) rail during shutdown.

3 System Design Theory

3.1 0V8 Discrete Buck Regulator (VCCINT)

The 0V8 rails is primarily used to power VCCCINT, sometimes called the core rail voltage. This high-current rail uses a discrete buck converter made of the TPS7H5006-SEP PWM controller, TPS7H6025-SEP GaN half-bridge driver, and EPC Space EPC7019GC GaN FETs.

These GaN FETs are selected due to the low on-resistance and availability as radiation-hardened devices. To support the low duty cycle of the 12V to 0.8V conversion ratio, three low-side FETs are used and one high-side FET. This asymmetric FET selection helps optimize the on-resistance and switching losses. The FETs are driven by the TPS7H6025-SEP gate driver. For the low-side FETs, 0Ω LOH and LOL gate resistors are determined to provide the fastest turn-on and turn-off times. For the high-side FET, a 0Ω HOL gate resistor is selected to provided the fastest turn-off time; however, a 3.3Ω HOH gate resistor is determined to be required to prevent excessive turn-on speed which can couple into the low-side gate.

The buck converter is operated in peak-current mode control using DCR current sensing. To provide a sufficient current signal, additional resistance is added in series with the inductor. Additionally, more slope compensation than traditionally required is added to provide additional noise mitigation and prevent excessive switch node jitter.

The buck regulator switches at 270kHz as a compromise between switching fast enough to result in a high enough crossover frequency and a reasonably small-sized inductor while not switching too fast which can cause minimum on-time issues and reduced efficiency. The output capacitor network is primarily sized based on the load step requirements of the Versal FPGA.

The output voltage is configured utilizing a resistor divider connected to the feedback pin. An R_{FB_TOP} of 10.05kΩ (10kΩ in series with a 50Ω) and R_{FB_BOT} of 33kΩ are selected which results in a nominal output voltage of 0.7997V. Utilizing the data sheet reference voltage parameter 0.607V minimum and 0.617V maximum along with 0.1% resistor tolerances (using a sum of squares to get ±0.14% error contribution), the overall DC accuracy can be approximated using Equation 1 and Equation 2. The accuracy is calculated to be –1.16% and +0.75%.

$$Error_{(\text{positive})} = \frac{V_{FB(max)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} + R_{(error)} \quad (1)$$

$$Error_{(negative)} = \frac{V_{FB(min)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} - R_{(error)} \quad (2)$$

Table 3-2 shows a summary of these calculations.

The layout of the GaN FETs and power loops is critical for optimized performance. The high-side FET is centered above the three low-side FETs for a balanced return path. The input capacitors are placed near the high-side FET and a ground return is provided on a second layer plane. This minimizes the return loop inductance and provides mutual inductance cancellation during FET turn-on.

Table 3-1. 0V8 Rail Design Values

PARAMETER	DESCRIPTION OR TYPICAL VALUE
V_{IN}	12V
V_{OUT}	0.8V
$I_{OUT(max)}$	44A
f_{SW}, switching frequency	270kHz
DC Accuracy	–1.16%, +0.75%
Output ripple	3.8mVpp
L_{SW}, output inductor	680nH XAL1010-681MEB
C_{OUT}, output capacitance	8x1.5mF (T520X) + 2x22µF ceramic + 2x1µF ceramic

Table 3-1. 0V8 Rail Design Values (continued)

PARAMETER	DESCRIPTION OR TYPICAL VALUE
C_{IN}, input capacitance	5x150µF (T521D) + 3x10µF ceramic + 8x100nF ceramic
t_{SS}, soft start time	12.7ms

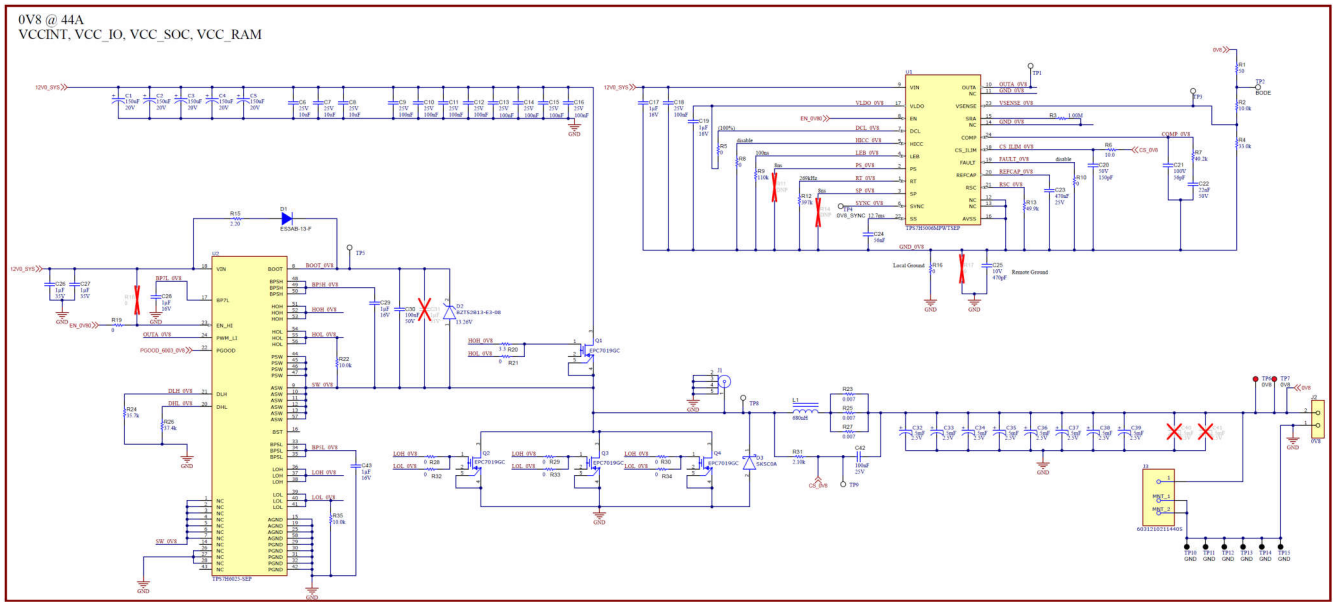


Figure 3-1. 0V8 (VCCINT) Schematic

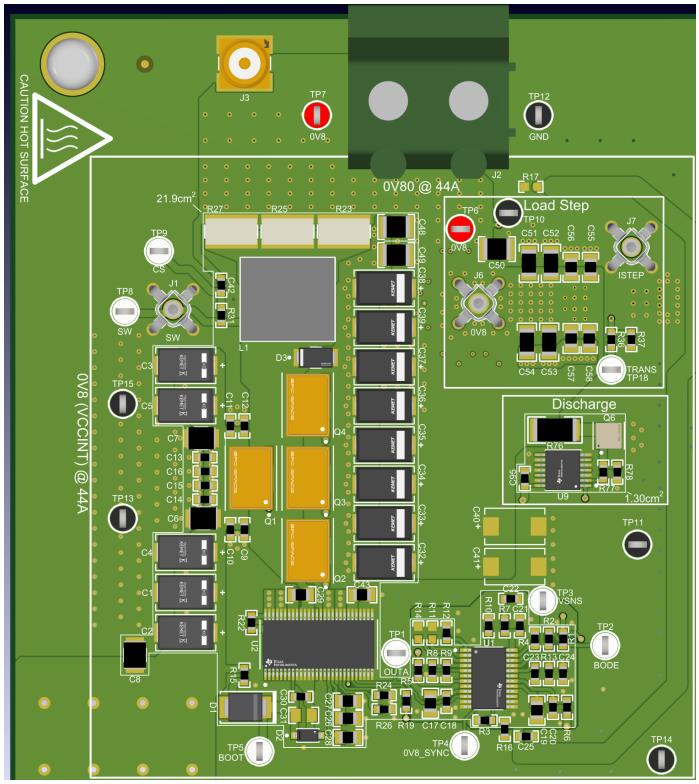


Figure 3-2. 0V8 (VCCINT) Layout – Top

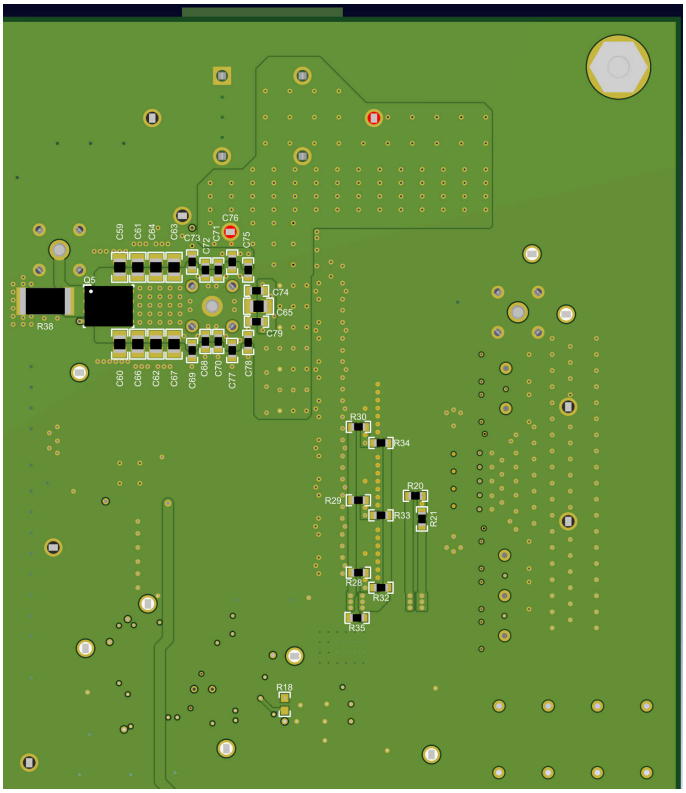


Figure 3-3. 0V8 (VCCINT) Layout – Bottom

3.1.1 VCCINT Load Step

A load step circuit is added to the design to be able to replicate the fast load steps from the Versal FPGA. This circuit is composed of a TI MOSFET that can be driven by a function generator and a load resistor. The MOSFET resistance and load resistor are sized to support an 11A load step. This load step and the resulting slew rate can be fine-tuned by adjusting the function generator applied voltage levels and slew rates.

In addition to the load step circuitry, decoupling capacitors are added. This additional capacitance is required to keep the impedance minimized at higher frequencies. In a final system design, place these capacitors near the FPGA. Additional optimization for the specific FPGA board layout can be required.

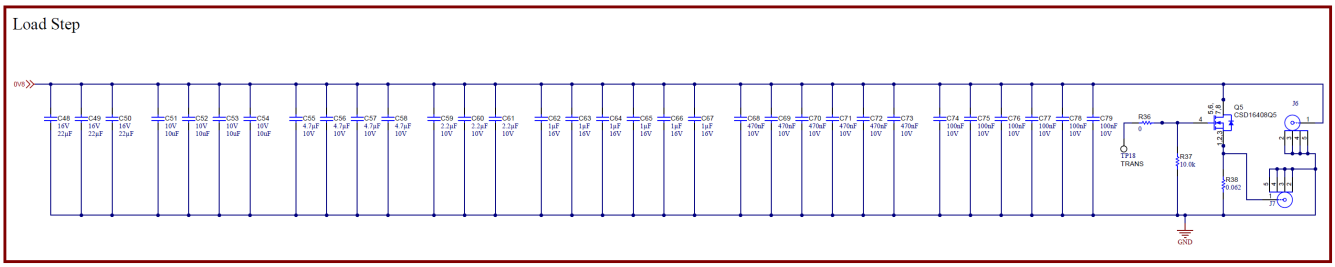


Figure 3-4. Load Step and Decoupling Capacitors Schematic

3.2 Buck Regulators (Integrated)

3.2.1 1V2

The TPS7H4010-SEP synchronous buck converter is selected to generate the required 1.2V directly from the 12V rail. While the TPS7H4010-SEP is capable of 6A, the Versal Edge VGTY_AVTT and VGTY_AVTTRCAL rails are estimated to only require 1.3A. Therefore, the buck converter is sized for 2A to provide reasonable margin.

A switching frequency of 1MHz and a 0.8µH XAL5030-801ME_ inductor are selected to provide a reasonable balance of design size and efficiency. Additionally, the *typical component selection* table in the *TPS7H4010-SEP Radiation Hardened 3.5V to 32V, 6A Synchronous Step-Down Voltage Converter in Space Enhanced Plastic* data sheet is consulted to make sure the values are close to the recommended selection. This is confirmed through a load step and Bode plot measurement as shown in Section 4.3.2. A 50Ω resistor is placed in series with the top feedback resistor and an option for a feed-forward capacitor is implemented to enable easier measuring and optimization of the control loop.

Next, output voltage ripple is determined. First the inductor ripple is calculated as shown in Equation 3. 1.35A of inductor ripple current is calculated.

$$I_{L(ripple)} = \frac{VIN - VOUT}{L} \times \frac{VOUT}{VIN \times f_{SW}} \quad (3)$$

where

- VIN is the input voltage, 12V
- VOUT is the configured output voltage, 1.2V
- L is the selected inductor, 0.8µH
- f_{SW} is the selected operating frequency, 1MHz

Next, two 100µF electrolytic capacitors and two 22µF ceramic capacitors are selected. Using the K-SIM tool from Kemet™, the output impedance of these parallel capacitors at 1MHz is determined to be approximately 2.5mΩ. Multiplying the impedance by the inductor ripple current gives the approximated output ripple of ±3.4mV.

Finally, the output voltage is configured using a resistor divider connected to the feedback pin. An R_{FB_TOP} of 50.55kΩ (50.5kΩ in series with a 50Ω) and R_{FB_BOT} of 261kΩ are selected which results in a nominal output voltage of 1.201V. Using the data sheet feedback voltage parameter, 0.987V minimum and 1.017V maximum along with 0.1% resistor tolerances (using a sum of squares to get ±0.14% error contribution), the overall DC accuracy can be approximated using Equation 4 and Equation 5. The accuracy is calculated to be –1.96% and +1.30%.

$$Error_{(\text{positive})} = \frac{V_{FB(max)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} + R_{(error)} \quad (4)$$

$$Error_{(negative)} = \frac{V_{FB(min)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} - R_{(error)} \quad (5)$$

One additional consideration for accuracy is if auto mode is enabled. Auto mode results in higher efficiency at light loads at the expense of worse load regulation. Consulting the TPS7H4010-SEP *load and line regulation* figure in the *TPS7H4010-SEP* data sheet and looking at the approximate 0.08V increase at light load for a 5V application, auto mode is approximated to add an additional error of +1.6%. Therefore, if auto mode is enabled, the accuracy is –1.96% and +2.90%. This is too much error for this rail and therefore auto mode is disabled.

Table 3-2 shows a summary of these calculations.

Table 3-2. 1V2 Rail Design Values

PARAMETER	DESCRIPTION OR TYPICAL VALUE
V_{IN}	12V
V_{OUT}	1.2V

Table 3-2. 1V2 Rail Design Values (continued)

PARAMETER	DESCRIPTION OR TYPICAL VALUE
$I_{OUT(max)}$	2A
f_{SW}, switching frequency	1MHz
DC Accuracy	–1.96%, +1.30%
Output ripple	3.4mVpp
L_{SW}, output inductor	0.8µH, XAL5030-801ME_
C_{OUT}, output capacitance	2x100µF T520B, 2x22µF ceramic
C_{IN}, input capacitance	3x10µF ceramic, 1x470nF ceramic
t_{SS}, soft start time	6.3ms (SS float)
Bias connection	Connected to external 3V3_VCCO
Mode	Forced PWM (auto disabled)

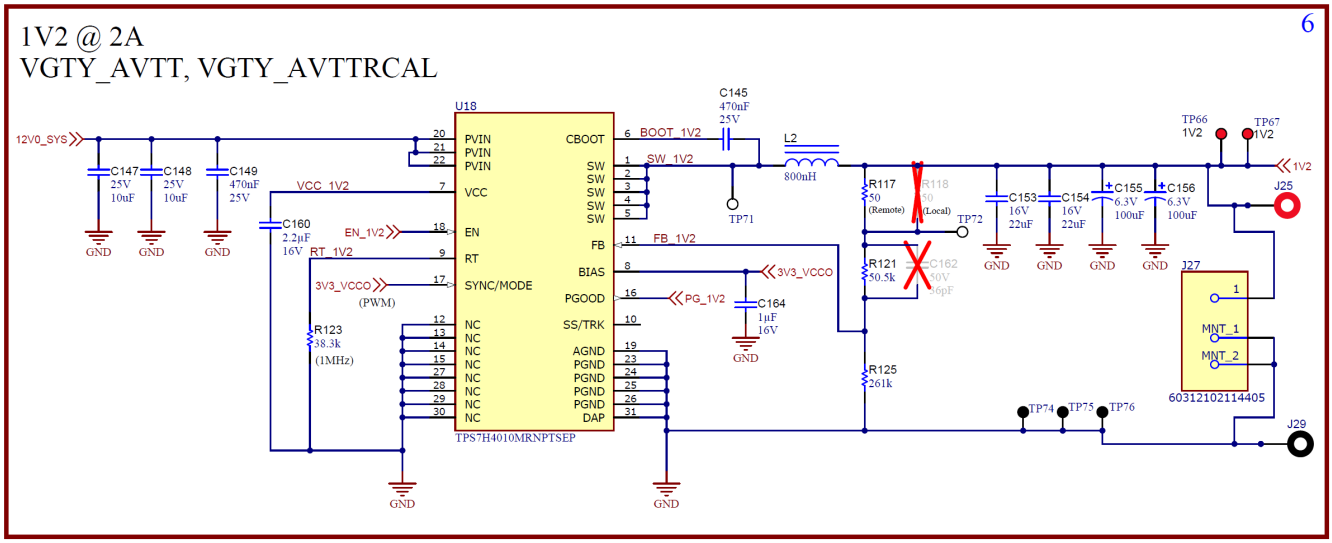


Figure 3-5. 1V2 Schematic

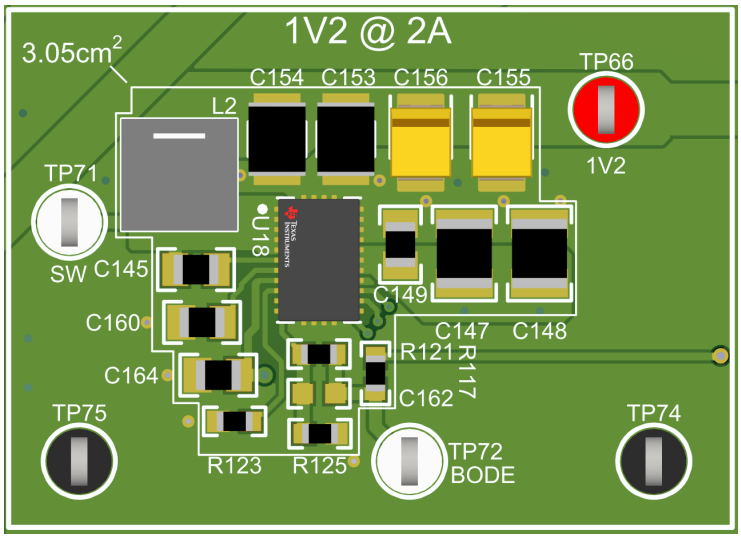


Figure 3-6. 1V2 Layout

3.2.2 1V2_VCCO

The TPS7H4010-SEP synchronous buck converter is selected to generate the required 1.2V directly from the 12V rail. While the TPS7H4010-SEP is capable of 6A, the Versal Edge XPIO (bank 7xx) rails only require 2A. Additionally, the 1V2_VCCO output feeds the input of the TPS7H1111-SEP for the 0V92 rail which is up to another 1A. Therefore, the design decision is to size this design for 4A to provide reasonable margin.

A switching frequency of 1MHz and a 0.8µH XAL5030-801ME_ inductor are selected to provide a reasonable balance of design size and efficiency. Additionally, the *typical component selection* table in the *TPS7H4010-SEP* data sheet is consulted to make sure the values are close to the recommended selection. This is confirmed through a load step and Bode plot measurement as shown in Section 4.3.2. A 50Ω resistor is placed in series with the top feedback resistor and an option for a feed-forward capacitor is implemented to enable easier measuring and optimization of the control loop.

Next output voltage ripple is determined. First the inductor ripple is calculated as shown in Equation 6. An inductor ripple current of 1.35A is calculated.

$$I_{L(ripple)} = \frac{VIN - VOUT}{L} \times \frac{VOUT}{VIN \times f_{SW}} \quad (6)$$

where

- VIN is the input voltage, 12V
- VOUT is the configured output voltage, 1.2V
- L is the selected inductor, 0.8µH
- f_{SW} is the selected operating frequency, 1MHz

Next, two 100µF electrolytic capacitors and one 22µF ceramic capacitor are selected. Using the K-SIM tool from Kemet, the output impedance of these parallel capacitors at 1MHz is determined to be approximately 4.2mΩ. Multiplying the impedance by the inductor ripple current gives the approximated output ripple of ±5.7mV.

Finally, the output voltage is configured using a resistor divider connected to the feedback pin. An R_{FB_TOP} of 50.55kΩ (50.5kΩ in series with a 50Ω) and R_{FB_BOT} of 261kΩ are selected which results in a nominal output voltage of 1.201V. Using the data sheet feedback voltage parameter 0.987V minimum and 1.017V maximum along with 0.1% resistor tolerances (using a sum of squares to get ±0.14% error contribution), the overall DC accuracy can be approximated using Equation 7 and Equation 8. The accuracy is calculated to be –1.96% and +1.30%.

$$Error_{(\text{positive})} = \frac{V_{FB(max)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} + R_{(error)} \quad (7)$$

$$Error_{(negative)} = \frac{V_{FB(min)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} - R_{(error)} \quad (8)$$

One additional consideration for accuracy is if auto mode is enabled. Auto mode results in higher efficiency at light loads at the expense of worse load regulation. Consulting the TPS7H4010-SEP *load and line regulation* figure in the *TPS7H4010-SEP* data sheet and looking at the approximate 0.08V increase at light load for a 5V application, auto mode is approximated to add an additional error of +1.6%. Therefore, if auto mode is enabled, the accuracy is –1.96% and +2.90%. This error is acceptable for this rail, and therefore auto mode is enabled.

Note that the output connector shows a current of 2A. This is because when all rails are fully loaded, 2A is outputted for the Versal Edge 1V2_VCCO rail while the other 2A is provided to other internal rails. The board connectors themselves are sized to support 4A.

Table 3-3 shows a summary of these calculations.

Table 3-3. 1V2_VCCO Rail Design Values

PARAMETER	DESCRIPTION OR TYPICAL VALUE
V_{IN}	12V
V_{OUT}	1.2V
$I_{OUT(max)}$	4A
f_{SW}, switching frequency	1MHz
DC Accuracy	–1.96%, +2.90%
Output ripple	5.7mVpp
L_{SW}, output inductor	0.8µH, XAL5030-801ME_
C_{OUT}, output capacitance	2x100µF T520B, 1x22µF ceramic
C_{IN}, input capacitance	3x10µF ceramic, 1x470nF ceramic
t_{SS}, soft start time	6.3ms (SS float)
Bias connection	Connected to external 3V3_VCCO
Mode	Auto enabled

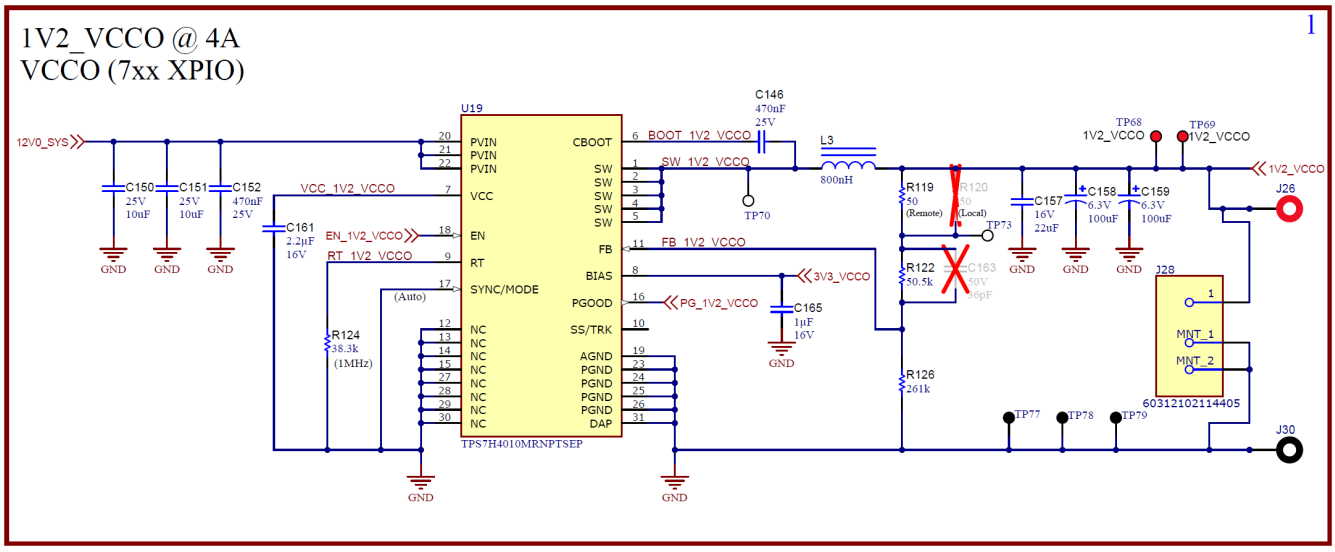


Figure 3-7. 1V2_VCCO Schematic

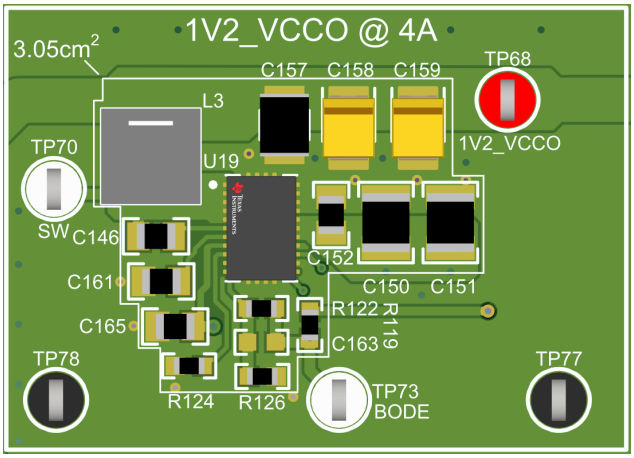


Figure 3-8. 1V2_VCCO Layout

3.2.3 1V2_MEM

The TPS7H4010-SEP synchronous buck converter is selected to generate the required 1.2V directly from the 12V rail. TI's estimate is that the DDR_VDDQ rail for DDR4 requires up to 3A and the VLDOIN of the downstream TPS7H3302-SEP requires up to 3A; therefore, the full 6A capability of the TPS7H4010-SEP is used.

A switching frequency of 1MHz and a 0.8µH XAL5030-801ME_ inductor are selected to provide a reasonable balance of design size and efficiency. Additionally, the *typical component selection* table in the *TPS7H4010-SEP* data sheet is consulted to make sure the values are close to the recommended selection. This is confirmed through a load step and Bode plot measurement as shown in Section 4.3.2. A 50Ω resistor is placed in series with the top feedback resistor and an option for a feed-forward capacitor is implemented to enable easier measuring and optimization of the control loop.

Next, the output voltage ripple is determined. First the inductor ripple is calculated as shown in Equation 9. An inductor ripple current of 1.35A is calculated.

$$I_{L(ripple)} = \frac{VIN - VOUT}{L} \times \frac{VOUT}{VIN \times f_{SW}} \quad (9)$$

where

- VIN is the input voltage, 12V
- VOUT is the configured output voltage, 1.2V
- L is the selected inductor, 0.8µH
- f_{SW} is the selected operating frequency, 1MHz

Next, two 100µF electrolytic capacitors and *one* 22µF ceramic capacitor is selected. Using the K-SIM tool from Kemet, the output impedance of these parallel capacitors at 1MHz is determined to be approximately 4.2mΩ. Multiplying the impedance by the inductor ripple current gives the approximated output ripple of ±5.7mV.

Finally, the output voltage is configured using a resistor divider connected to the feedback pin. An R_{FB_TOP} of 50.55kΩ (50.5kΩ in series with a 50Ω) and R_{FB_BOT} of 261kΩ are selected which results in a nominal output voltage of 1.201V. Using the data sheet feedback voltage parameter 0.987V minimum and 1.017V maximum along with 0.1% resistor tolerances (using a sum of squares to get ±0.14% error contribution), the overall DC accuracy can be approximated using Equation 10 and Equation 11. The accuracy is calculated to be –1.96% and +1.30%.

$$Error_{(\text{positive})} = \frac{V_{FB(max)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} + R_{(error)} \quad (10)$$

$$Error_{(negative)} = \frac{V_{FB(min)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} - R_{(error)} \quad (11)$$

One additional consideration for accuracy is if auto mode is enabled. Auto mode results in higher efficiency at light loads at the expense of worse load regulation. Consulting the TPS7H4010-SEP *load and line regulation* image in the *TPS7H4010-SEP* data sheet and looking at the approximate 0.08V increase at light load for a 5V application, auto mode is approximated to add an additional error of +1.6%. Therefore, if auto mode is enabled, the accuracy is –1.96% and +2.90%. This error is acceptable for this rail, and therefore auto mode is enabled.

Table 3-4 shows a summary of these calculations.

Table 3-4. 1V2 Rail Design Values

PARAMETER	DESCRIPTION OR TYPICAL VALUE
V_{IN}	12V
V_{OUT}	1.2V
$I_{OUT(max)}$	6A
f_{SW}, switching frequency	1MHz

Table 3-4. 1V2 Rail Design Values (continued)

PARAMETER	DESCRIPTION OR TYPICAL VALUE
DC Accuracy	–1.96%, +2.90%
Output ripple	5.7mVpp
L_{SW}, output inductor	0.8µH, XAL5030-801ME_
C_{OUT}, output capacitance	2x100µF T520B, 1x22µF ceramic
C_{IN}, input capacitance	3x10µF ceramic, 1x470nF ceramic
t_{SS}, soft start time	6.3ms (SS float)
Bias connection	Connected to external 3V3_VCCO
Mode	Auto enabled

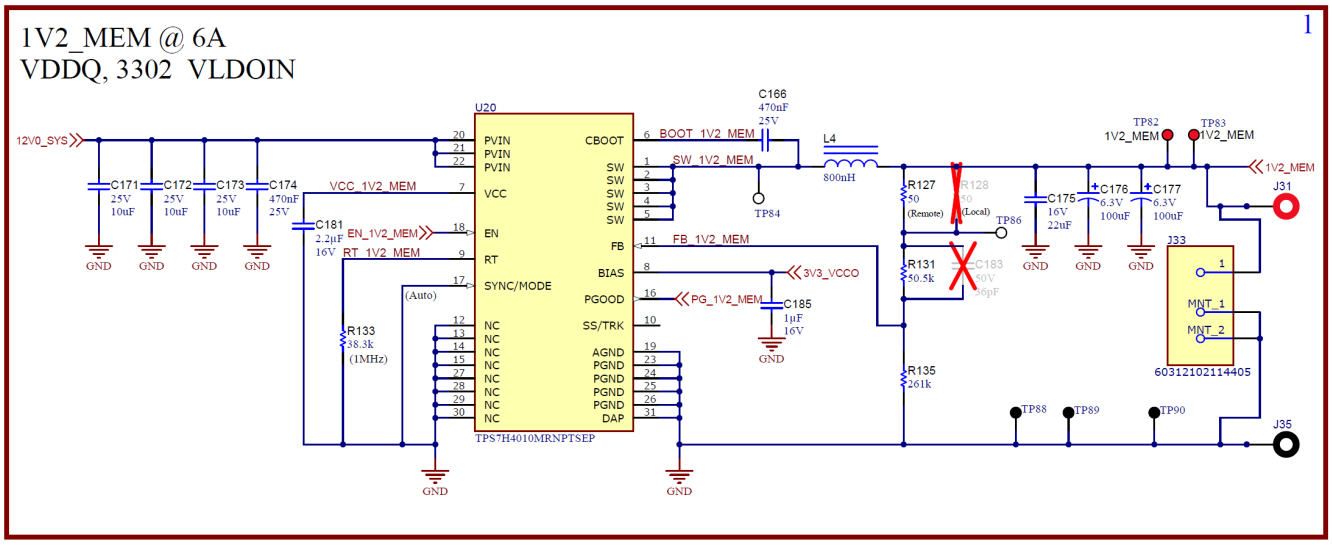


Figure 3-9. 1V2_MEM Schematic

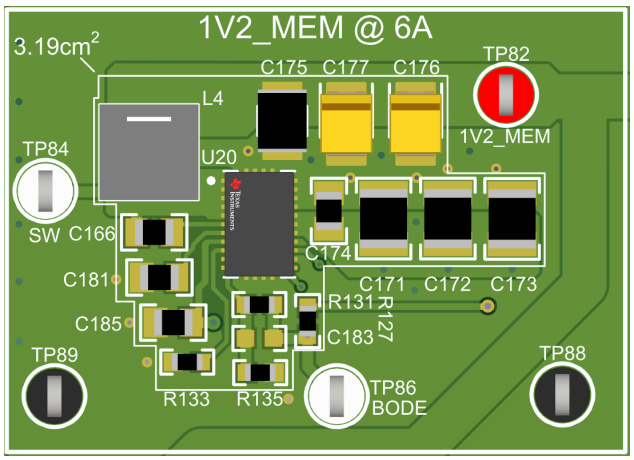


Figure 3-10. 1V2_MEM Layout

3.2.4 2V5_DDR_VPP

The TPS7H4010-SEP synchronous buck converter is selected to generate the required 2.5V directly from the 12V rail. The DDR_VPP rail for DDR4 is estimated to require up to 0.1A, the TPS7H1111-SEP input for the 1V5_GTY rail is estimated to require up to 0.2A, and the TPS7H1111-SEP input for the 1V5 rail is estimated to require up to 1.5A. Therefore, the design decision is for 3A to provide reasonable margin.

A switching frequency of 1MHz and a 1.2µH XAL5030-122ME_ inductor are selected to provide a reasonable balance of design size and efficiency. Additionally, the *typical component selection* table in the *TPS7H4010-SEP* data sheet is consulted to make sure the values are close to the recommended selection. This is confirmed through a load step and Bode plot measurement as shown in Section 4.3.2. A 50Ω resistor is placed in series with the top feedback resistor and an option for a feed-forward capacitor is implemented to enable easier measuring and optimization of the control loop.

Next, the output voltage ripple is determined. First the inductor ripple is calculated as shown in Equation 12. An inductor ripple current of 1.65A is calculated.

$$I_{L(ripple)} = \frac{VIN - VOUT}{L} \times \frac{VOUT}{VIN \times f_{SW}} \quad (12)$$

where

- VIN is the input voltage, 12V
- VOUT is the configured output voltage, 2.5V
- L is the selected inductor, 1.2µH
- f_{SW} is the selected operating frequency, 1MHz

Next, two 100µF electrolytic capacitors and one 22µF ceramic capacitor are selected. Using the K-SIM tool from Kemet, the output impedance of these parallel capacitors at 1MHz is determined to be approximately 4.2mΩ. Multiplying the impedance by the inductor ripple current gives the approximated output ripple of ±6.9mV.

Finally, the output voltage is configured using a resistor divider connected to the feedback pin. An R_{FB_TOP} of 50.55kΩ (50.5kΩ in series with a 50Ω) and R_{FB_BOT} of 34kΩ are selected which results in a nominal output voltage of 2.502V. Using the data sheet feedback voltage parameter 0.987V minimum and 1.017V maximum along with 0.1% resistor tolerances (using a sum of squares to get ±0.14% error contribution), the overall DC accuracy can be approximated using Equation 13 and Equation 14. The accuracy is calculated to be –1.96% and +1.30%.

$$Error_{(positive)} = \frac{V_{FB(max)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} + R_{(error)} \quad (13)$$

$$Error_{(negative)} = \frac{V_{FB(min)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} - R_{(error)} \quad (14)$$

One additional consideration for accuracy is if auto mode is enabled. Auto mode results in higher efficiency at light loads at the expense of worse load regulation. Consulting the TPS7H4010-SEP *load and line regulation* image in the *TPS7H4010-SEP* data sheet and looking at the approximate 0.08V increase at light load for a 5V application, auto mode is approximated to add an additional error of +1.6%. Therefore, if auto mode is enabled, the accuracy is –1.96% and +2.90%. This error is acceptable for this rail, and therefore auto mode is enabled.

Note that the output connector shows a current of 0.1A. This is because when all rails are fully loaded, 0.1A is outputted for the DDR_VPP rail, while the other 2.9A is provided to other internal rails. The board connectors themselves are sized to support 3A.

Table 3-5 shows a summary of these calculations.

Table 3-5. 2V5_DDR_VPP Rail Design Values

PARAMETER	DESCRIPTION OR TYPICAL VALUE
V_{IN}	12V
V_{OUT}	2.5V
$I_{OUT(max)}$	3A
f_{SW}, switching frequency	1MHz
DC Accuracy	–1.96%, +2.90%
Output ripple	6.9mVpp

Table 3-5. 2V5_DDR_VPP Rail Design Values (continued)

PARAMETER	DESCRIPTION OR TYPICAL VALUE
L_{SW}, output inductor	1.2µH, XAL5030-122ME_
C_{OUT}, output capacitance	2x100µF T520B, 1x22µF ceramic
C_{IN}, input capacitance	3x10µF ceramic, 1x470nF ceramic
t_{SS}, soft start time	6.3ms (SS float)
Bias connection	Connected to external 3V3_VCCO
Mode	Auto enabled

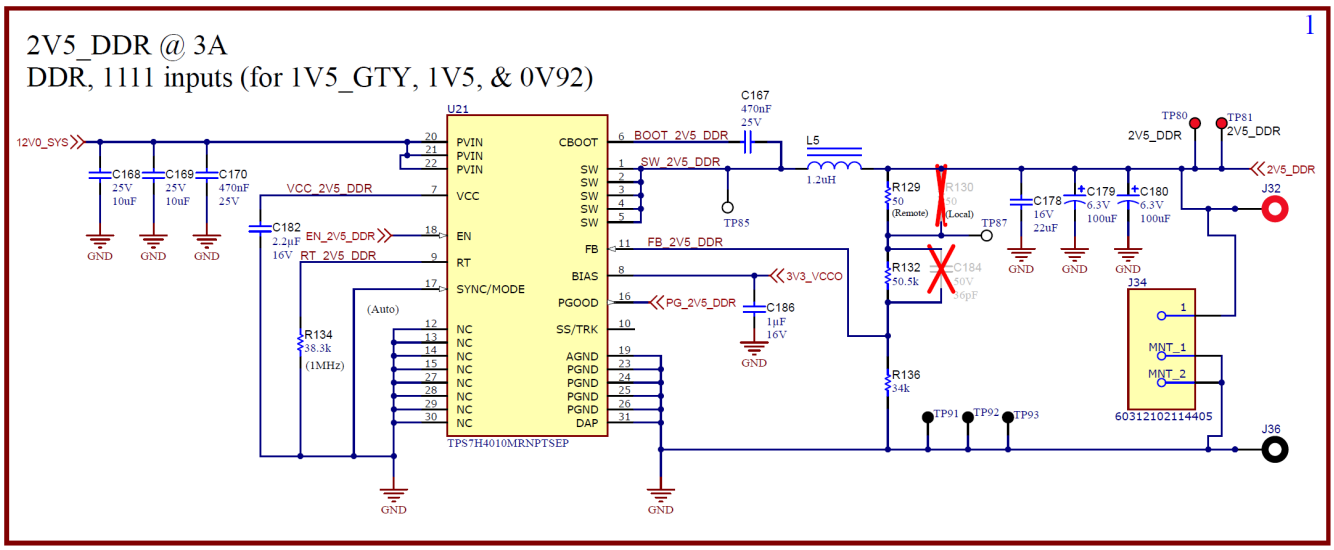


Figure 3-11. 2V5_DDR_VPP Schematic

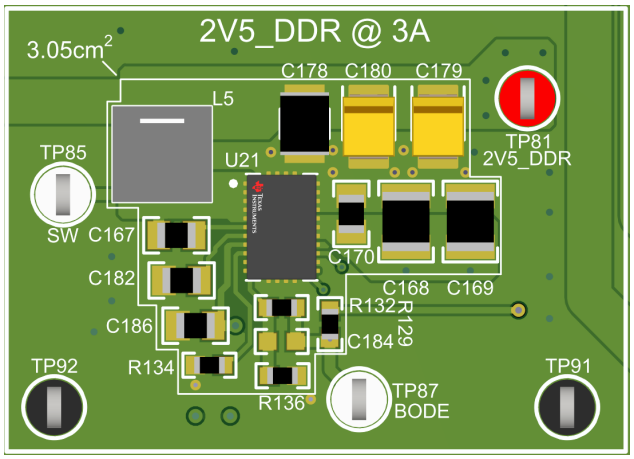


Figure 3-12. 2V5_DDR_VPP Layout

3.2.5 3V3_VCCO

The TPS7H4010-SEP synchronous buck converter is selected to generate the required 3.3V directly from the 12V rail. The Versal Edge VCCO_HDIO (bank 302) rails are estimated to require 2A, the VCCO_500, VCCO_501, and VCCO_503 (PSIO banks) and VCCO_502 (PSIO bank) are estimated to require 2A, the TPS7H3302-SEP VDD input is estimated to require 30mA, and the TPS7H1111-SEP bias rails are estimated to require 81mA. Therefore, TPS7H4010-SEP is sized for 6A to provide reasonable margin.

A switching frequency of 1MHz and a 1.8µH XAL6030-182ME_ inductor is selected to provide a reasonable balance of design size and efficiency. Additionally, the *typical component selection* table in the *TPS7H4010-SEP* data sheet is consulted to make sure the values are close to the recommended selection. This is confirmed through a load step and Bode plot measurement as shown in Section 4.3.2. A 50Ω resistor is placed in series with the top feedback resistor and an option for a feed-forward capacitor is implemented to enable easier measuring and optimization of the control loop.

Next, the output voltage ripple is determined. First the inductor ripple is calculated as shown in Equation 15. An inductor ripple current of 1.33A is calculated.

$$I_{L(ripple)} = \frac{VIN - VOUT}{L} \times \frac{VOUT}{VIN \times f_{SW}} \quad (15)$$

where

- VIN is the input voltage, 12V
- VOUT is the configured output voltage, 3.3V
- L is the selected inductor, 1.8µH
- f_{SW} is the selected operating frequency, 1MHz

Next, one 100µF electrolytic capacitor and two 22µF ceramic capacitors are selected. Using the K-SIM tool from Kemet, the output impedance of these parallel capacitors at 1MHz is determined to be approximately 12.2mΩ. Multiplying the impedance by the inductor ripple current gives the approximated output ripple of ±16.2mV.

Finally, the output voltage is configured using a resistor divider connected to the feedback pin. An R_{FB_TOP} of 50.55kΩ (50.5kΩ in series with a 50Ω) and R_{FB_BOT} of 22.1kΩ are selected which results in a nominal output voltage of 3.307V. Using the data sheet feedback voltage parameter 0.987V minimum and 1.017V maximum along with 0.1% resistor tolerances (using a sum of squares to get ±0.14% error contribution), the overall DC accuracy can be approximated using Equation 16 and Equation 17. The accuracy is calculated to be –1.82% and +1.45%.

$$Error_{(positive)} = \frac{V_{FB(max)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} + R_{(error)} \quad (16)$$

$$Error_{(negative)} = \frac{V_{FB(min)} \times \frac{R_{FB\_TOP} + R_{FB\_BOT}}{R_{FB\_BOT}} - V_{OUT(ideal)}}{V_{OUT(ideal)}} - R_{(error)} \quad (17)$$

One additional consideration for accuracy is if auto mode is enabled. Auto mode results in higher efficiency at light loads at the expense of worse load regulation. Consulting the TPS7H4010-SEP *load and line regulation* image in the *TPS7H4010-SEP* data sheet and looking at the approximate 0.08V increase at light load for a 5V application, auto mode is approximated to add an additional error of +1.6%. Therefore, if auto mode is enabled, the accuracy is –1.82% and +3.05%. This error is acceptable for this rail, and therefore auto mode is enabled.

Table 3-6 shows a summary of these calculations.

Table 3-6. 3V3_VCCO Rail Design Values

PARAMETER	DESCRIPTION OR TYPICAL VALUE
V_{IN}	12V
V_{OUT}	3.3V
$I_{OUT(max)}$	6A
f_{SW}, switching frequency	1MHz
DC Accuracy	–1.82%, +3.05%
Output ripple	16.2mVpp
L_{SW}, output inductor	1.8µH XAL6030-182ME_
C_{OUT}, output capacitance	1x100µF T520B, 2x22µF ceramic
C_{IN}, input capacitance	2x10µF ceramic, 1x470nF ceramic

Table 3-6. 3V3_VCCO Rail Design Values (continued)

PARAMETER	DESCRIPTION OR TYPICAL VALUE
t_{SS}, soft start time	6.3ms (SS float)
Bias connection	Connected to output 3V3_VCCO
Mode	Auto enabled

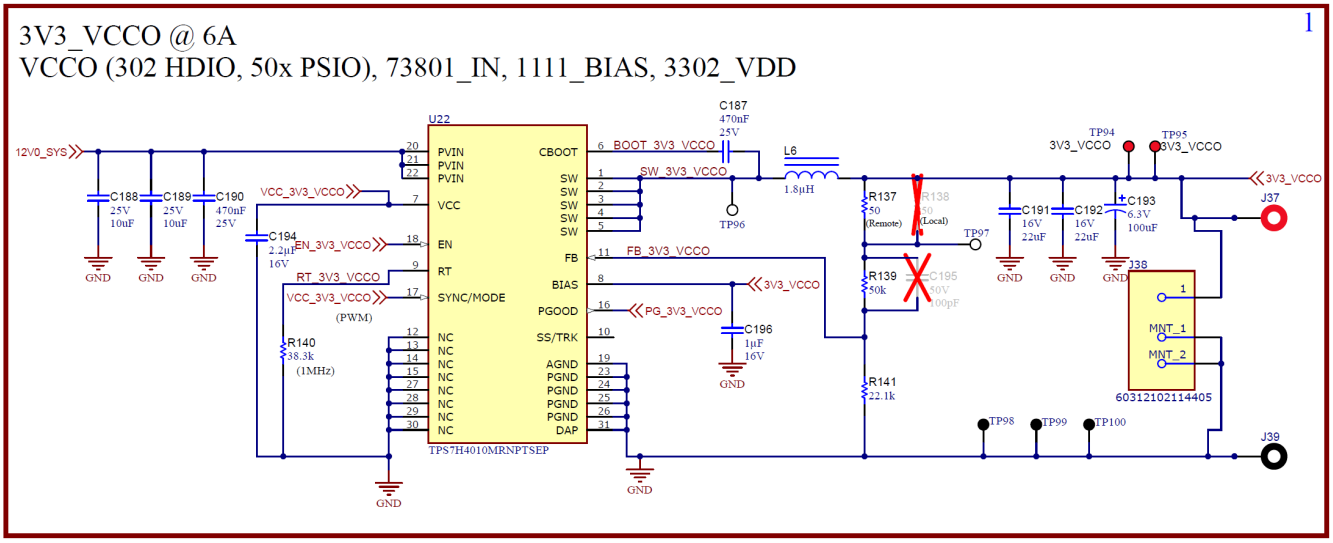


Figure 3-13. 3V3_VCCO Schematic

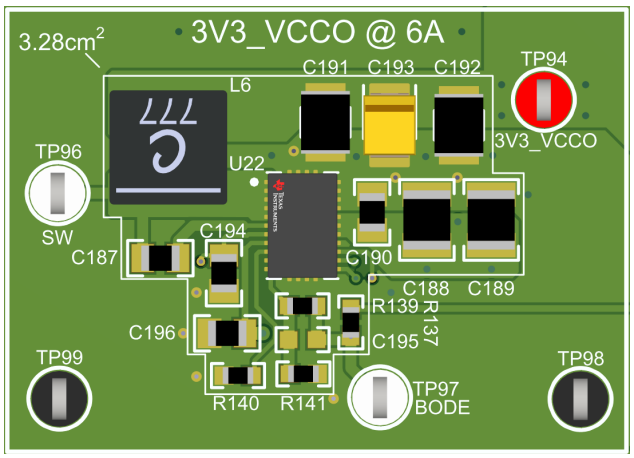


Figure 3-14. 3V3_VCCO Layout

3.3 Linear Regulators

3.3.1 DDR Termination

The TPS7H3302-SEP is selected for the termination of the DDR4 memory. This part generates the ±3A for VTT and ±10mA for VTTREF. The VLDOIN input comes from the 1V2_MEM rail and the VDD comes from the 3V3_VCCO rail. The output capacitors are selected to be 3x150µF + 4x4.7µF, which is the same as the EVM. From the TPS7H3302-SEP data sheet, the VTT accuracy is –2.5% and +5.0% (for ±1A).

Figure 3-15 shows the TPS7H3302-SEP schematic, and Figure 3-16 shows the layout.

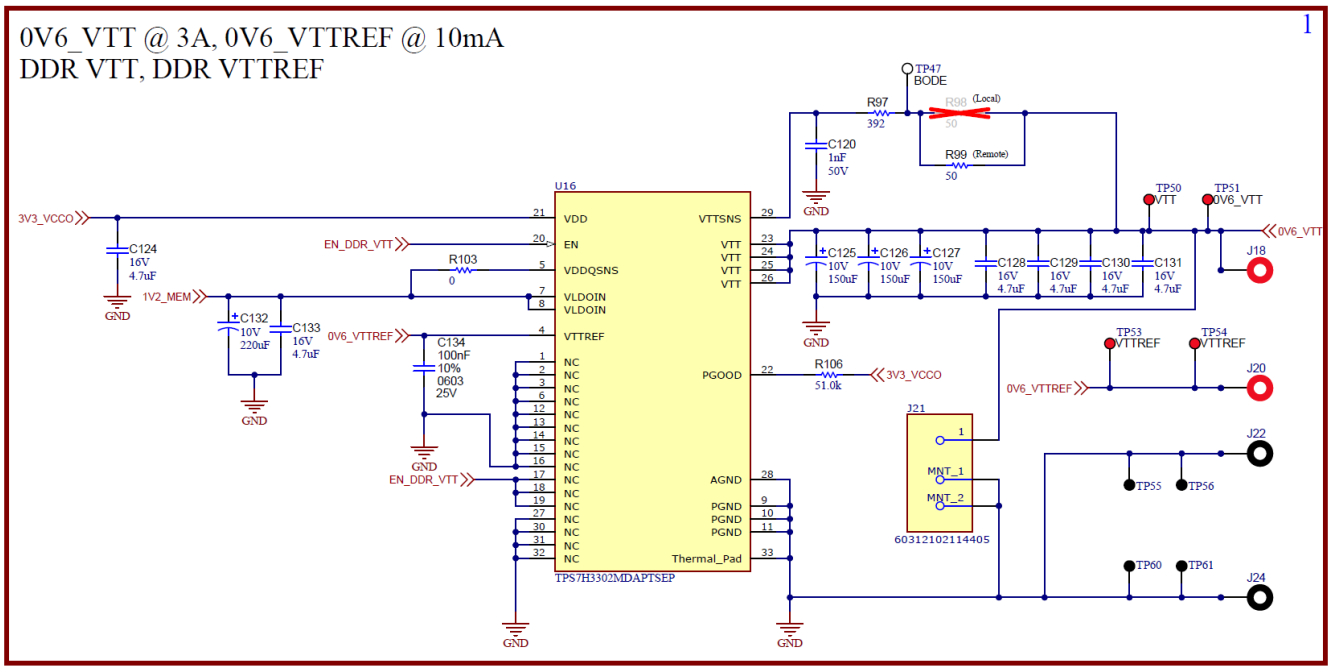


Figure 3-15. DDR Termination Schematic

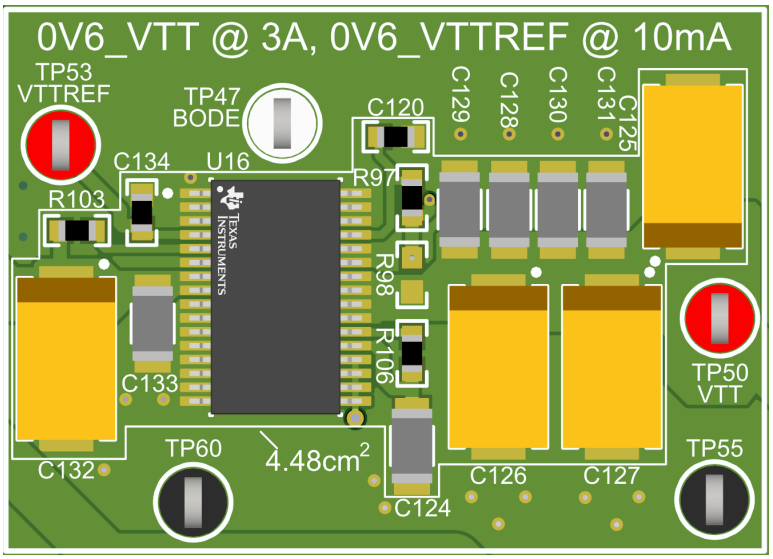


Figure 3-16. DDR Termination Layout

3.3.2 0V92

The TPS7H1111-SEP is selected to generate the 0.92V rail from the 1V2_VCCO rail (and 3V3_VCCO for the bias). While the TPS7H1111-SEP is capable of 1.5A, the Versal Edge VTYP_AVCC rail is estimated to only require 0.75A. Therefore, the LDO is designed for 1A maximum to provide reasonable margin.

The 2x100µF output capacitors used on the EVM are selected for this design. No additional ceramic decoupling capacitors are added as the TPS7H1111-SEP does not require them for good performance. However, if desired, a 100nF capacitor can be added near the FPGA load (a placeholder in the layout is provided for this purpose). The FB_PG resistors are sized so that the PG assert threshold occurs at 95.5% of VOUT. This threshold must be carefully selected to make sure that during start-up the TPS7H1111-SEP voltage ramps up within the maximum sequencing timing requirements of the Versal FPGA. Additionally, a 2.2µF C_{SS} capacitor is selected instead of the typical 4.7µF capacitor to provide additional timing margin during start-up. The lower noise that is provided by the 4.7µF capacitor is determined to not be critical for the Versal FPGA.

Figure 3-17 shows the 0V92 schematic, and Figure 3-18 shows the layout.

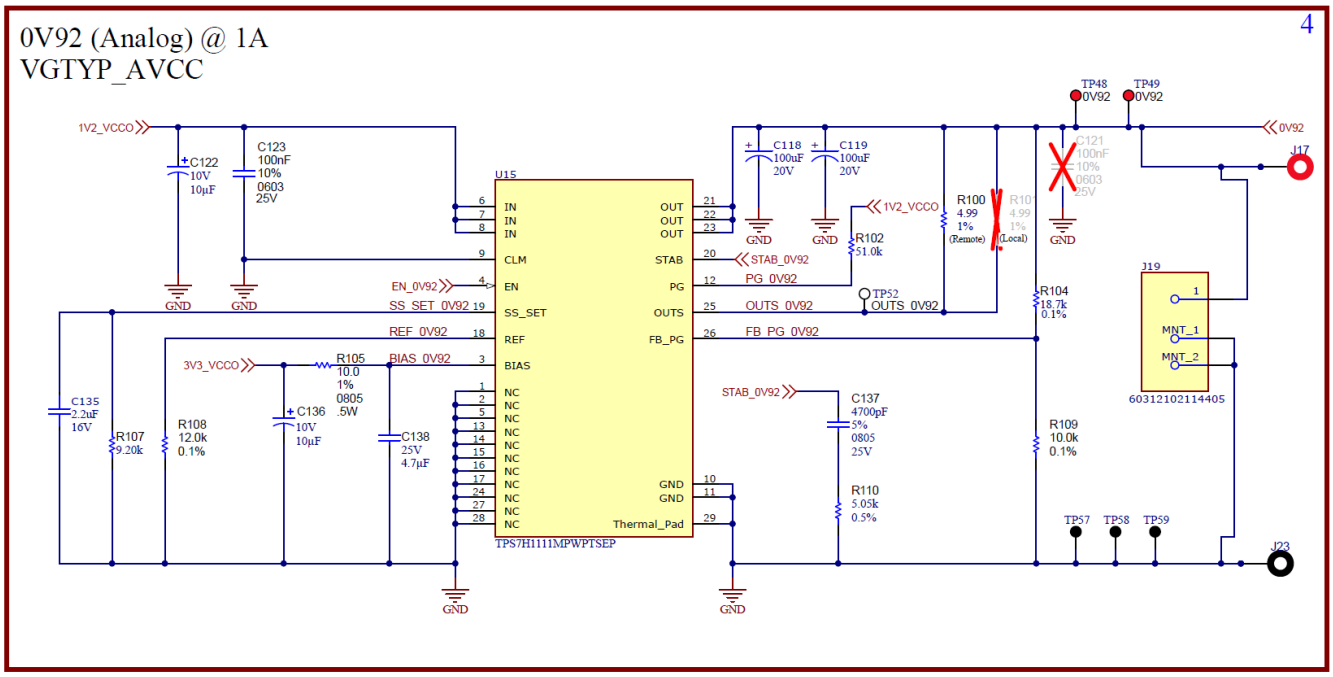


Figure 3-17. 0V92 Schematic

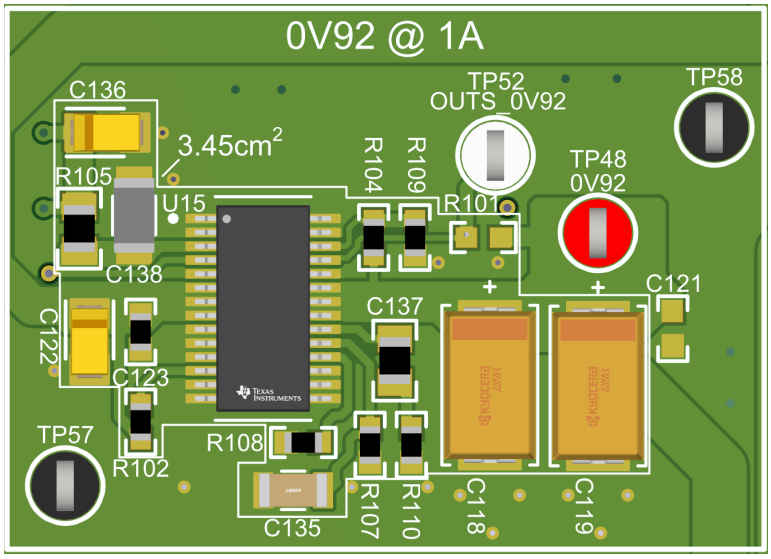


Figure 3-18. 0V92 Layout

3.3.3 1V5_GTY

The TPS7H1111-SEP is selected to generate the 1.5V rail from the 2V5_DDR rail (and 3V3_VCCO for the bias). While the TPS7H1111-SEP is capable of 1.5A, the Versal Edge VGTY_AVCCAUX rail is estimated to only require 0.05A. Therefore, the LDO is designed for 0.2A maximum to provide reasonable margin.

The 2x100µF output capacitors used on the EVM are selected for this design. No additional ceramic decoupling capacitors are added as the TPS7H1111-SEP does not require them for good performance. However, if desired, a 100nF capacitor can be added near the FPGA load (a placeholder in the layout is provided for this purpose). The FB_PG resistors are sized so that the PG assert threshold occurs at 94.9% of VOUT. This threshold must be carefully selected to make sure that during start-up the TPS7H1111-SEP voltage ramps up within the maximum sequencing timing requirements of the Versal FPGA. Additionally, a 2.2µF C_{SS} capacitor is selected instead of the typical 4.7µF capacitor to provide additional timing margin during start-up. The lower noise that is provided by the 4.7µF capacitor is determined to not be critical for the Versal FPGA.

Figure 3-19 shows the 1V5_GTY schematic and Figure 3-20 shows the layout.

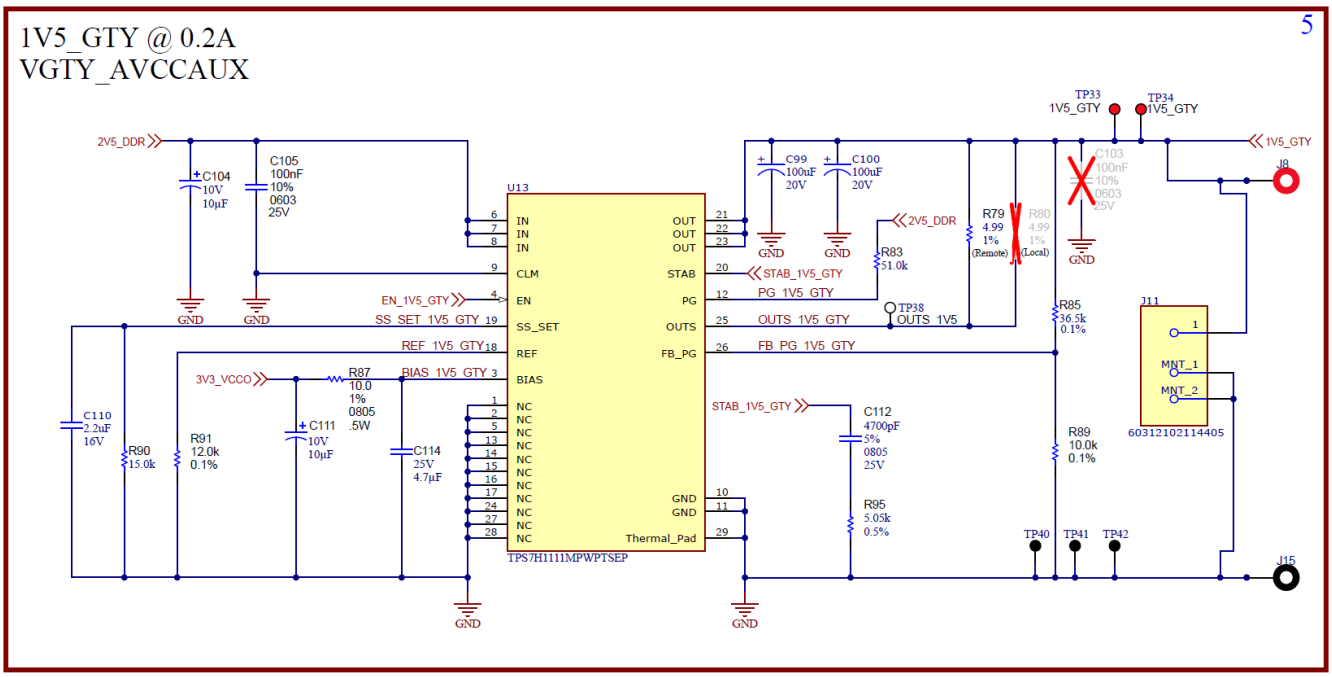


Figure 3-19. 1V5_GTY Schematic

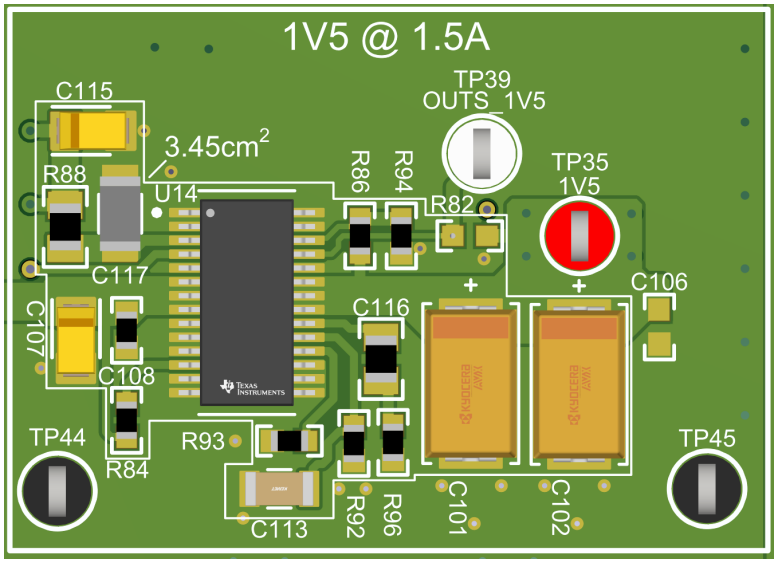


Figure 3-20. 1V5_GTY Layout

3.3.4 1V5

The TPS7H1111-SEP is selected to generate the 1.5V rail from the 2V5_DDR rail (and 3V3_VCCO for the bias). The Versal Edge VCCAUX requires 0.7A and the VCCAUX_SMON and VCCAUX_PMC requires 0.3A. To provide margin, the LDO is designed for the maximum current of 1.5A.

The 2x100µF output capacitors used on the EVM are selected for this design. No additional ceramic decoupling capacitors are added at the output of the TPS7H1111-SEP. The VCCAUX_SMON rail is recommended to have an additional ferrite bead filter. After the ferrite bead, a single 100nF capacitor is placed to stay well within the recommended output filter of the TPS7H1111-SEP. With this filter and the high PSRR of the TPS7H1111-SEP, a low-noise SMON rail is created. The FB_PG resistors are sized so that the PG assert threshold occurs at 94.9% of VOUT. This threshold must be carefully selected to make sure that during start-up the TPS7H1111-SEP voltage ramps up within the maximum sequencing timing requirements of the Versal FPGA. Additionally, a 2.2µF C_{SS} capacitor is selected instead of the typical 4.7µF capacitor to provide additional timing margin during

start-up. The lower noise that is provided by the 4.7µF capacitor is determined to not be critical for the Versal FPGA.

Note that the output connector for 1V5 shows a maximum current of 1.5A and the 1V5_SMON connector shows a maximum current of 0.4A . If these connectors are loaded at the same time, it is important to make sure the connectors are not loaded at more than 1.5A combined.

Figure 3-21 shows the 1V5 schematic and Figure 3-22 shows the layout.

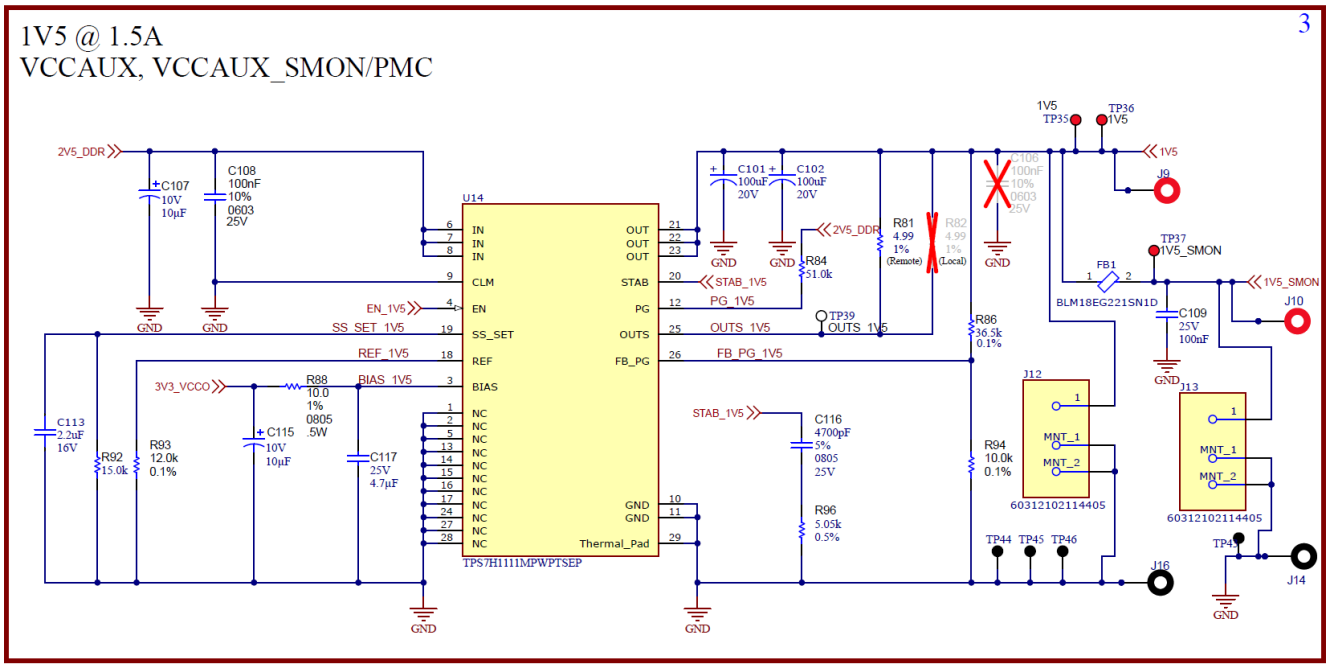


Figure 3-21. 1V5 Schematic

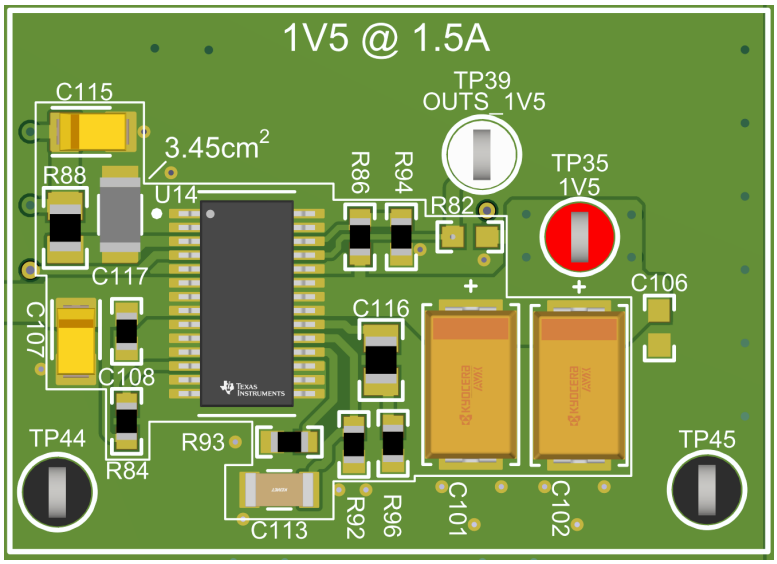


Figure 3-22. 1V5 Layout

3.3.5 5V0_SYS

The TPS73801-SEP is selected to generate the 5.0V rail from the 12V0_SYS rail. This rail is used to power the TPS7H3014-SP pullup inputs and power for the TPS7H2221-SEP devices. These are all relatively low power. The TPS73801 is sized for 50mA for plenty of margin.

Output capacitors of 1x100µF + 2x22µF are selected for the output. EN is tied high to start-up right away so that this rail is usable for the TPS7H2221 and TPS7H3014 as soon as possible.

Figure 3-23 shows the 5V0_SYS schematic and Figure 3-24 shows the layout.

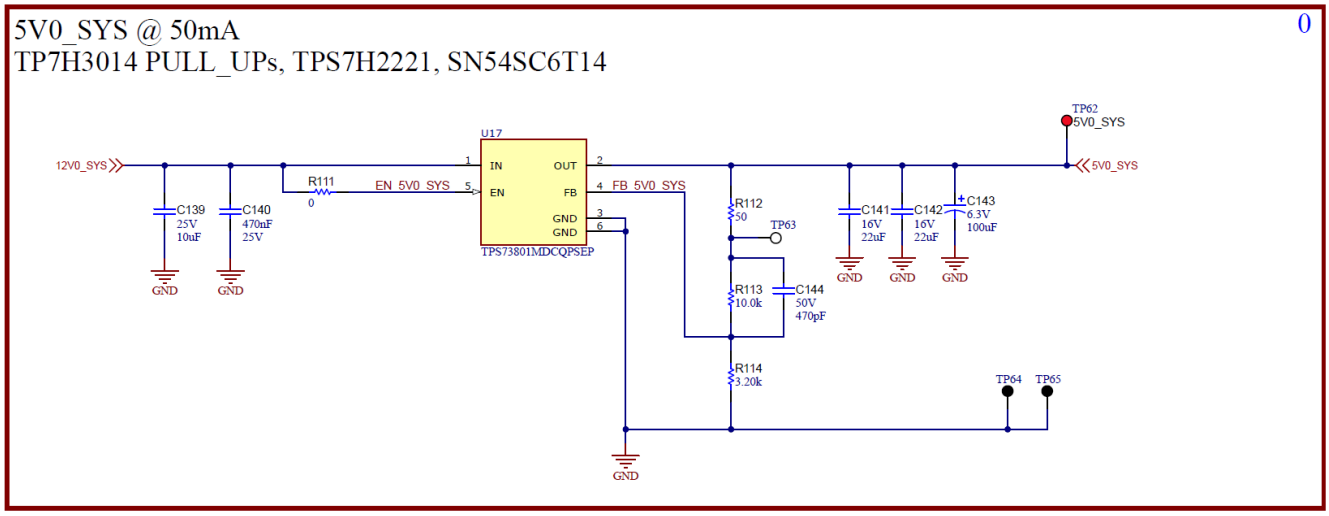


Figure 3-23. 5V0_SYS Schematic

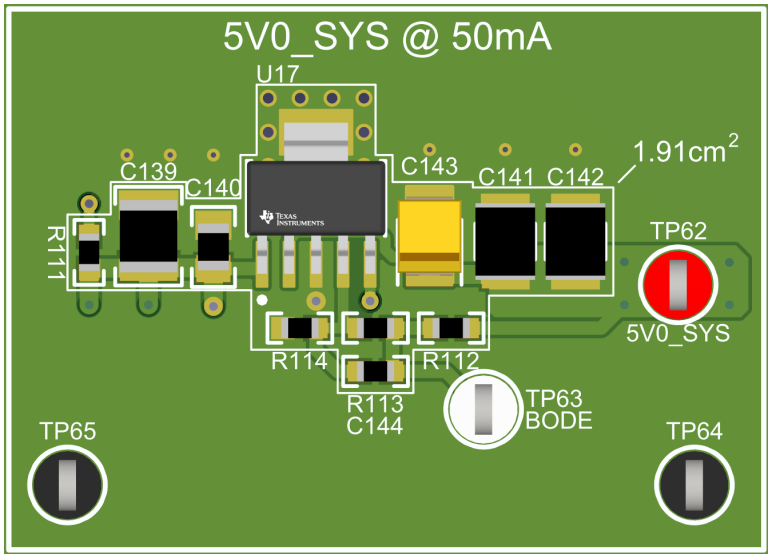


Figure 3-24. 5V0_SYS Layout

3.4 Sequencing

3.4.1 TPS7H3014-SP Sequencer

The Versal Edge has specific sequence up and sequence down requirements. Two TPS7H3014-SP devices are utilized in a daisy chain configuration to sequence the six Versal rails up in order and sequence down in reverse order. Table 3-7 shows the sequencer number of each rail. Since the TPS7H3014-SP devices monitor the rail voltage, the actual voltage thresholds for on and off can be programmed with a resistor divider as also shown in the table.

Table 3-7. Sequencing Order

SEQUENCE NUMBER	RAIL MONITORED AND SEQUENCED	OTHER RAILS SEQUENCED	R_{TOP}	R_{BOTTOM}	$V_{ON\text{-}NOMINAL}$ (V)	$V_{ON\text{-}NOMINAL}$ (%)	$V_{OFF\text{-}NOMINAL}$ (V)	$V_{OFF\text{-}NOMINAL}$ (%)
1	3V3_VCCO	1V2_VCCO, 2V5_DDR_VPP, 1V2_MEM, VTT(DDR)	118kΩ	28.7kΩ	3.064V	92.84% ± 0.93%	0.226V	6.85% ± 2.74%
2	VCCINT (0V80)	None	29.4kΩ	111kΩ	0.758V	94.76% ± 0.95%	0.051V	6.39% ± 2.82%
3	1V5	None	54.2kΩ	40.2kΩ	1.407V	93.83% ± 0.94%	0.104V	6.93% ± 2.77%
4	0V92	None	34kΩ	75kΩ	0.871V	94.68% ± 0.95%	0.053V	5.81% ± 2.83%
5	1V5_GTY	None	54.2kΩ	40.2kΩ	1.407V	93.83% ± 0.94%	0.104V	6.93% ± 2.77%
6	1V2	None	44.2kΩ	49.3kΩ	1.137V	94.72% ± 0.95%	0.074V	6.15% ± 2.82%
7(1)	12V0_SYS	None	56.9kΩ	3.61kΩ	10.046V	83.72% ± 0.84%	8.678V	72.32% ± 0.90%

(1) This rail is used to supervise the 12V0_SYS rail and the TPS7H2221-SEP is used to hold down the SENSE1 during start-up.

The TPS7H3014-SP begins a sequence up when a rising voltage on 12V0_SYS is detected (after a small delay). Similarly, when the 12V0_SYS is falling, a sequence down is started. This sequence down helps protect the supplies in a brownout event. Table 3-8 shows these details.

Table 3-8. Up and Down Sequencing

SEQUENCE	R_{TOP}	R_{BOTTOM}	VIN, min	VIN, typ	VIN, max	COMMENT
UP	20kΩ	1.3kΩ	9.50V	9.80V	10.08V	Sequence up begins before VIN > approximately 10V. 1.5µF capacitor for delay (1.9ms time constant)
DOWN	20kΩ	1.1kΩ	9.26V	9.55V	9.82V	Sequence down when VIN falls < approximately 9.6V. If not completed before VIN < approximately 8.678V, shutdown to protect core and other supplies

Figure 3-25 shows the sequencer schematic and Figure 3-26 shows the layout.

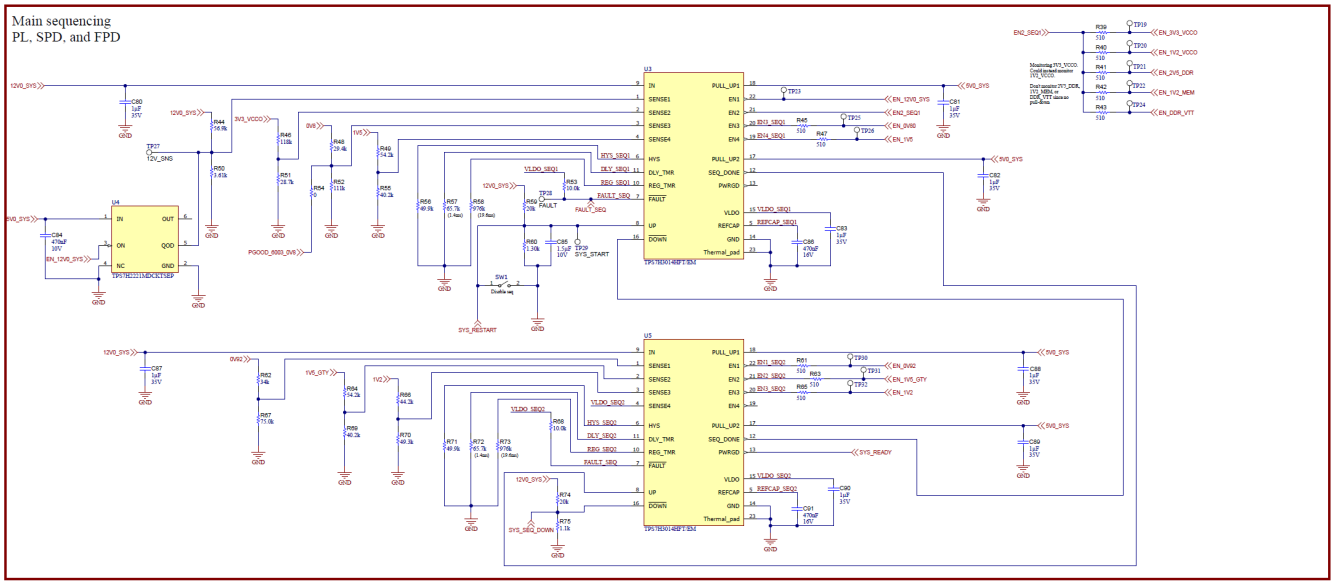


Figure 3-25. Sequencing Schematic

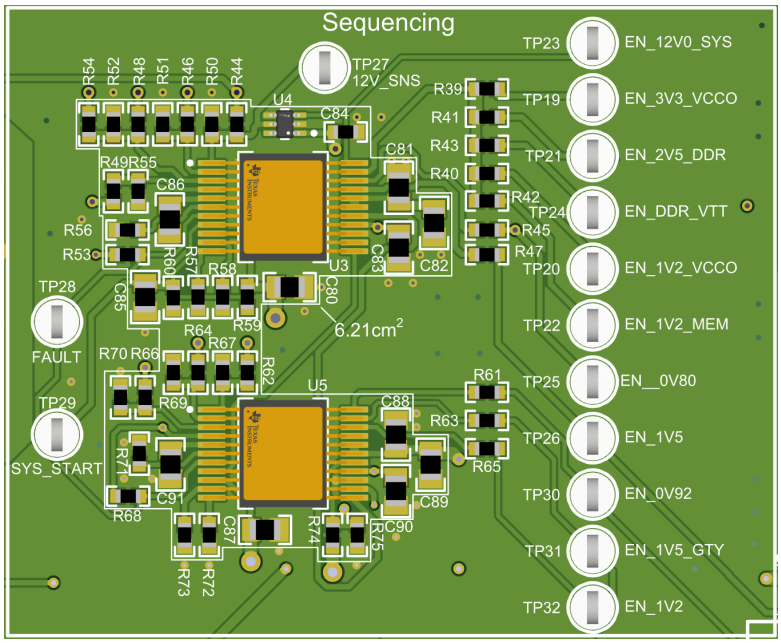


Figure 3-26. Sequencing Layout

3.4.2 TPS7H2221-SEP Discharge Circuit

The Versal FPGA requires rails to sequence up within a specific amount of time. This is easily attainable with typical soft start times used for the voltage regulators. However, when sequencing down these rails, without an active discharge, the rails can take too long to sequence off.

To implement an active discharge, typically an additional MOSFET can be used. However, depending on the specific implementation, additional support circuitry can be required and radiation-tolerant MOSFETs can be fairly large. Instead, the TPS7H2221-SEP load switch with a quick output discharge (QOD) is used to accomplish the active discharge. This small design only makes use of the QOD pin and a small decoupling capacitor to power the device. This design is used for all auxiliary power rails that have discharge requirements.

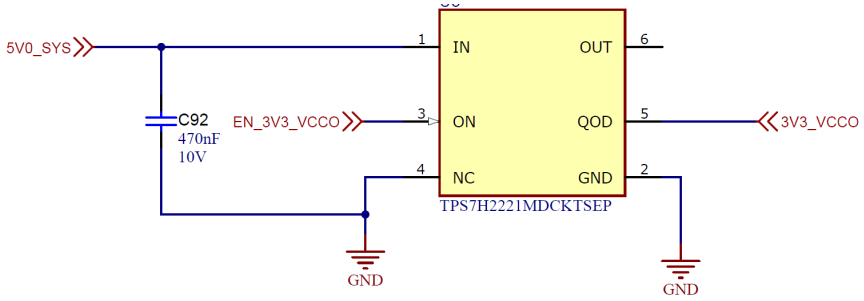


Figure 3-27. Discharge Schematic

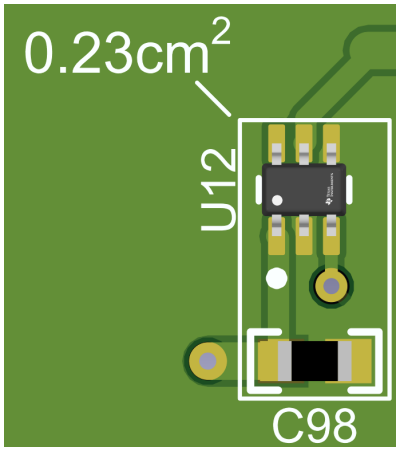


Figure 3-28. Discharge Layout

3.4.3 VCCINT Discharge Circuit

Similar to many of the auxiliary rails, the 0V8 (VCCINT) core rail also requires an active discharge to shutdown within the required time. However, due to the large capacitance on this rail, the TPS7H2221-SEP design does not discharge the rail in a sufficient time.

Instead, an inverter and a GaN FET is used to discharge this rail. A resistor is used to prevent large current peaks during this discharge. Figure 3-29 shows the schematic and Figure 3-30 shows the layout.

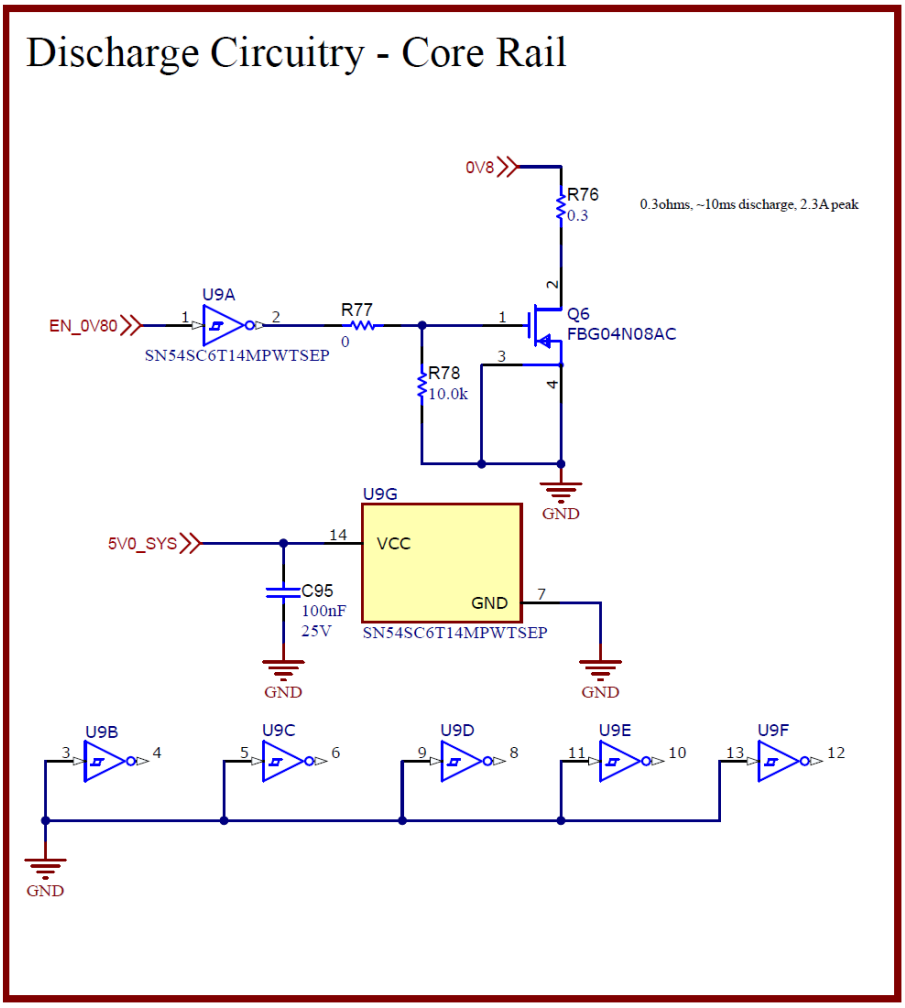


Figure 3-29. VCCINT Discharge Schematic

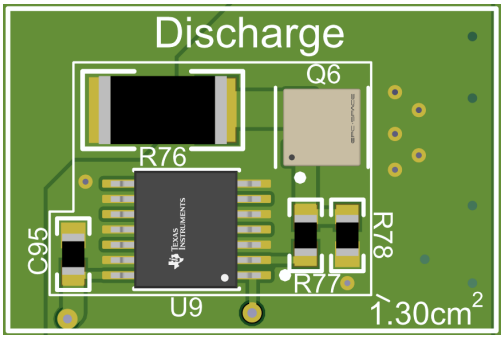


Figure 3-30. VCCINT Discharge Layout

4 Hardware, Testing Requirements, and Test Results

4.1 Hardware Requirements

- TIDA-050088 Reference Design Board
- DC Power Supply capable of 12V and 7A (4A sufficient if not fully loading the TIDA)
- Electronic Load (44A)
- Multimeter
- Oscilloscope
- Function generator (for VCCINT load steps)

4.2 Test Setup

Connect the power supply to the input terminals (labeled 12V0_SYS) and make sure the 12V is connected to the red connector and GND is connected to the black connector. To automatically start-up when the power is applied, make sure the sequencer is enabled with SW1 set to Enable. After the power supplies are all sequenced up, the supplies can then be sequenced down with the sequence down button, SW3. The supplies can again be sequenced up with the sequence up button (SW2).

To test individual power supplies, connect the electronic load to the desired output terminals. Multiple loads can be applied simultaneously if desired. The loads are not intended to go above the rated output listed on the board.

CAUTION

Caution Hot surface. Contact can cause burns. Do not touch!

Some components can reach high temperatures > 55°C when the board is powered on. Do not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

4.3 Test Results

4.3.1 Discrete Buck Regulator (VCCINT)

4.3.1.1 0V8

Unless otherwise noted, VIN = 12V in Figure 4-1 to Figure 4-27.

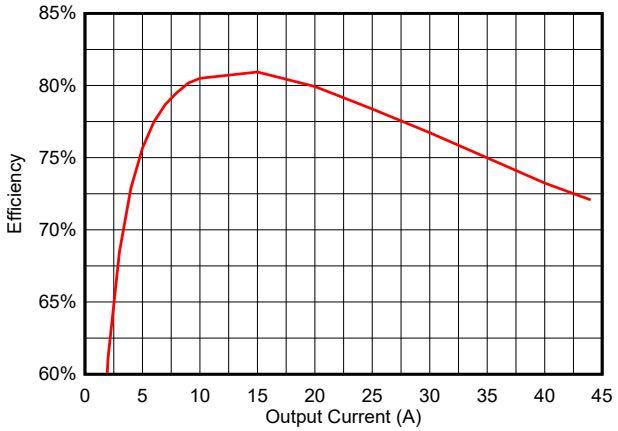
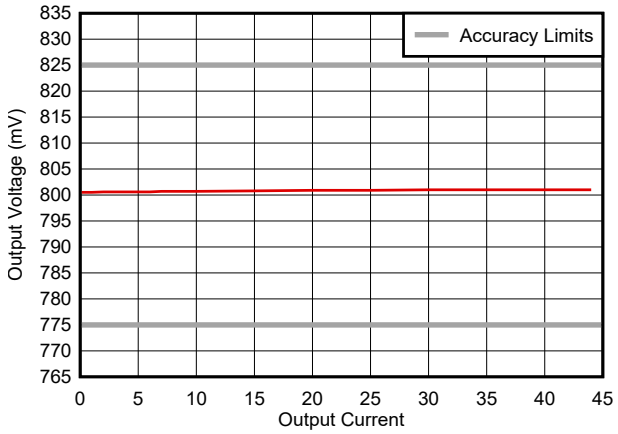
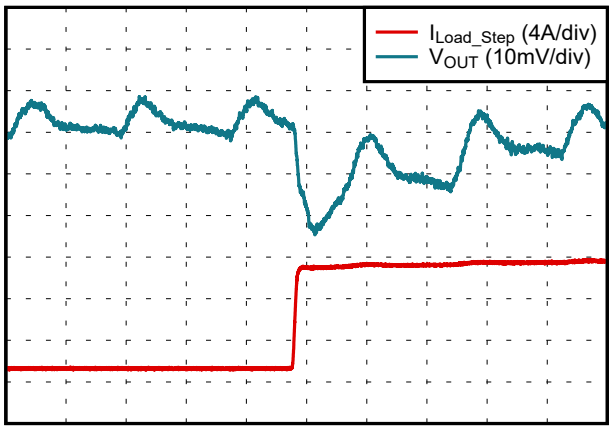


Figure 4-1. Efficiency



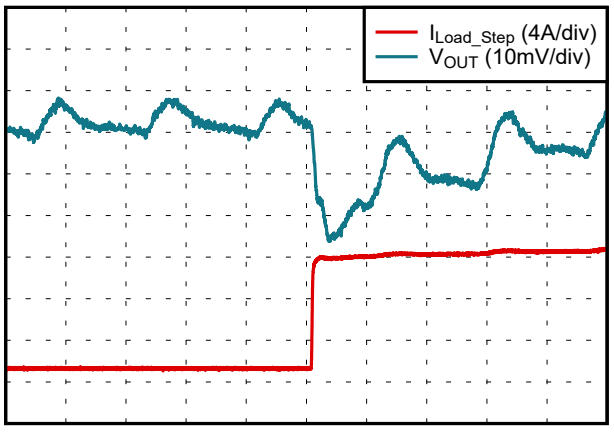
Local ground

Figure 4-2. Load Regulation



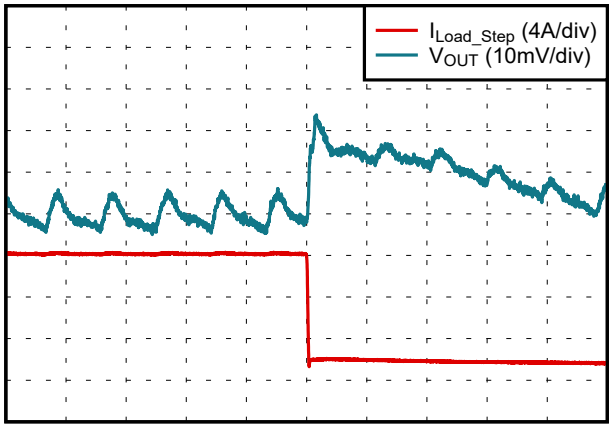
$V_{OUT(drop)}$ = 24.8mV, I_{LOAD_STEP} is measured using the voltage across the R38 load step resistor, the measurement does not include the 20A DC current

Figure 4-3. Load Step: 20A to 31A at 56A/µs



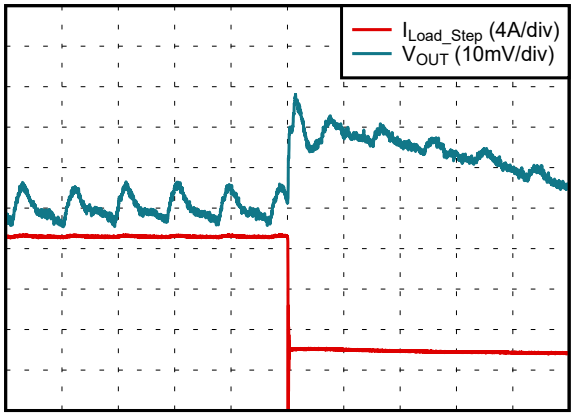
$V_{OUT(drop)}$ = 26.4mV, I_{LOAD_STEP} is measured using the voltage across the R38 load step resistor, the measurement does not include the 20A DC current

Figure 4-4. Load Step: 20A to 31A at 200A/µs



$V_{OUT(rise)}$ = 24.0mV, I_{LOAD_STEP} is measured using the voltage across the R38 load step resistor, the measurement does not include the 20A DC current

Figure 4-5. Load Step: 31A to 20A at 83A/µs



$V_{OUT(rise)}$ = 28.4mV, I_{LOAD_STEP} is measured using the voltage across the R38 load step resistor, the measurement does not include the 20A DC current

Figure 4-6. Load Step: 31A to 20A at 200A/µs

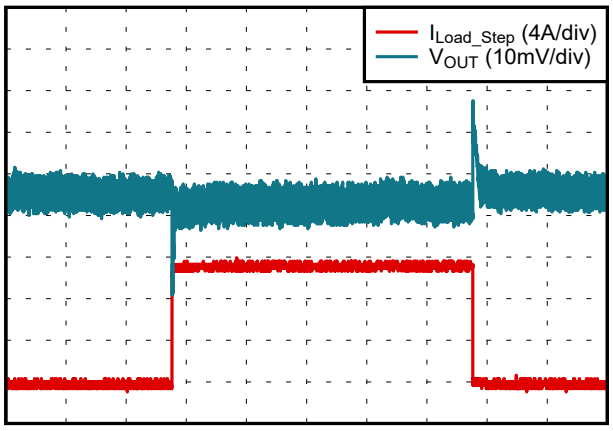
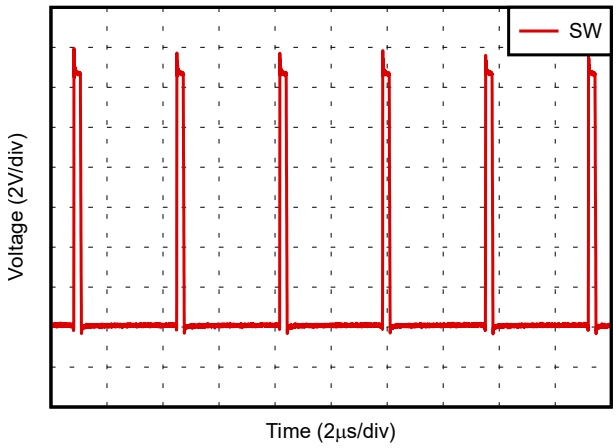


Figure 4-7. Load Step: 20A to 31A to 20A Load Step



f_{SW} = 272kHz, I_{OUT} = 2A

Figure 4-8. Switch Node and Switching Frequency

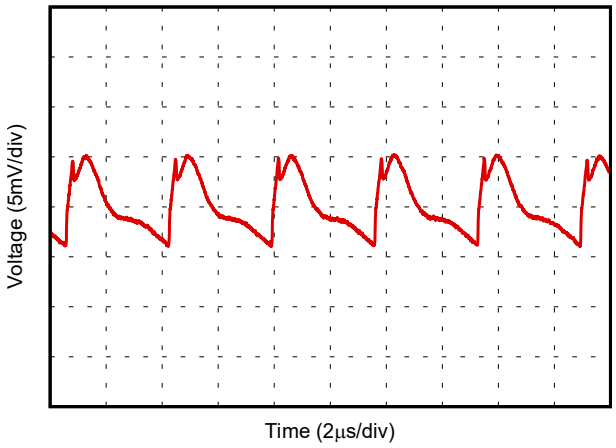


Figure 4-9. Output Voltage Ripple at 0A

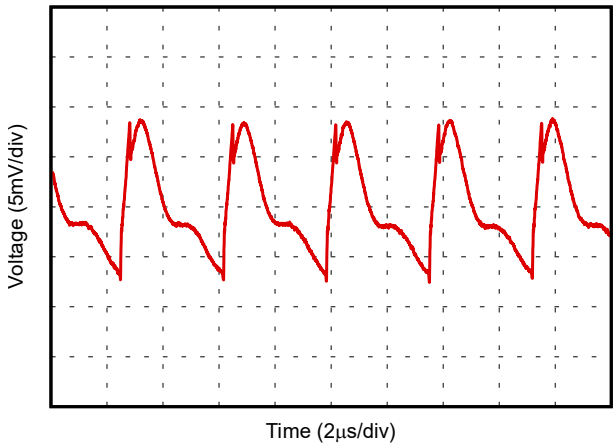
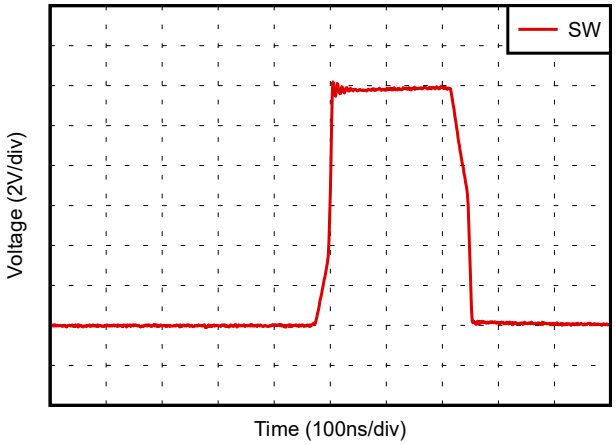
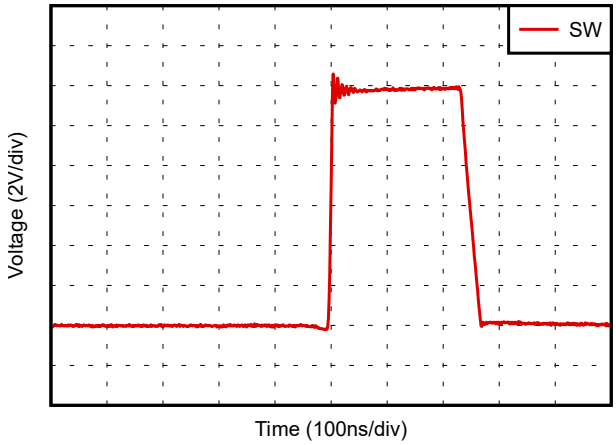


Figure 4-10. Output Voltage Ripple at 44A



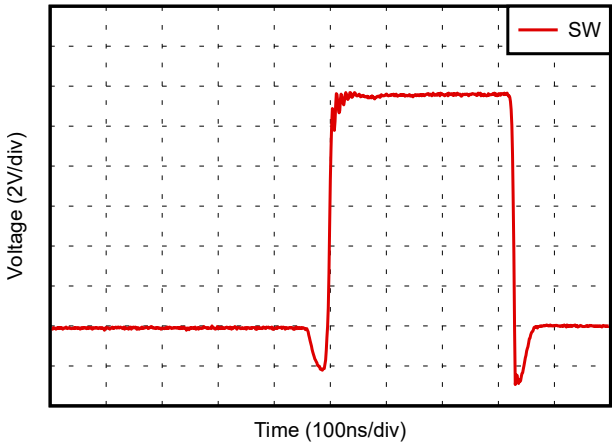
$V_{SW(max)}$ = 12.2V

Figure 4-11. Switch Node at 0A



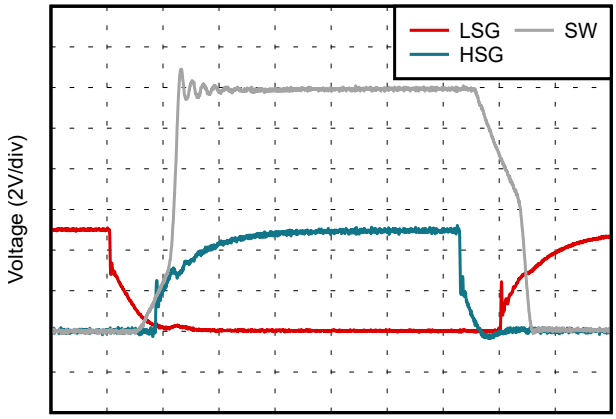
$V_{SW(max)}$ = 12.6V

Figure 4-12. Switch Node at 2A



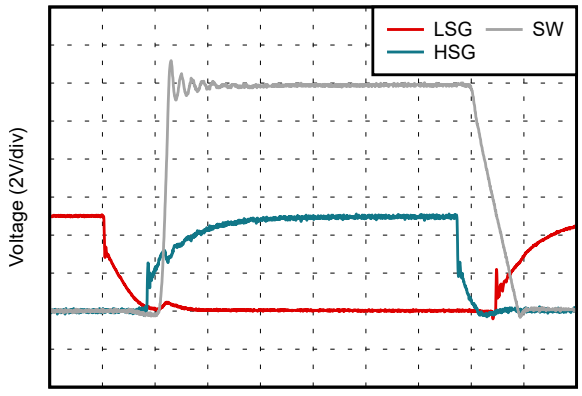
$V_{SW(max)}$ = 11.8V

Figure 4-13. Switch Node at 44A



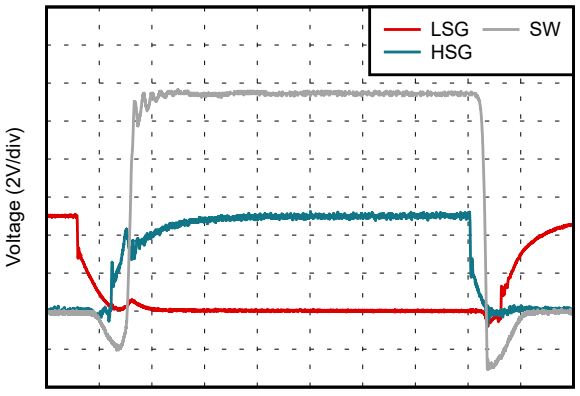
HSG is with respect to SW and is calculated with the oscilloscope using GND referenced measurements: $V_{HSG} – V_{SW}$

Figure 4-14. Gate Signals at 0A



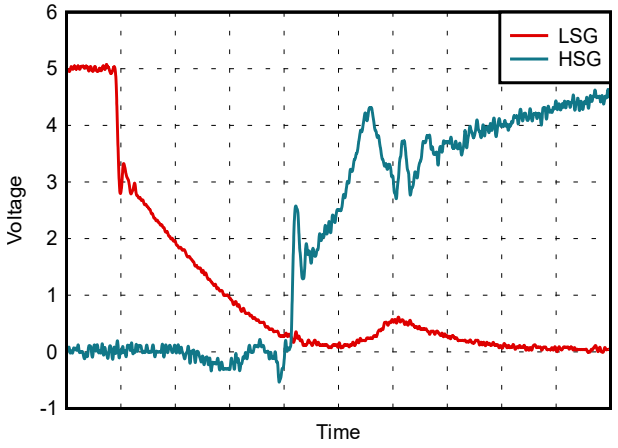
HSG is with respect to SW and is calculated with the oscilloscope using GND referenced measurements: $V_{HSG} – V_{SW}$

Figure 4-15. Gate Signals at 2A



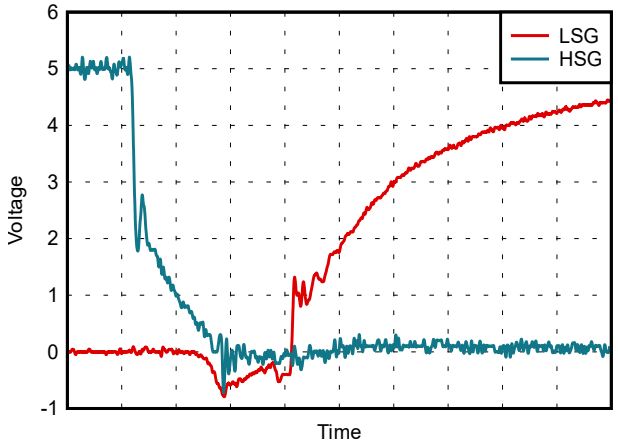
HSG is with respect to SW and is calculated with the oscilloscope using GND referenced measurements: $V_{HSG} – V_{SW}$

Figure 4-16. Gate Signals at 44A



I_{OUT} = 44A

Figure 4-17. Dead time: Low to High



I_{OUT} = 44A

Figure 4-18. Dead time: High to Low

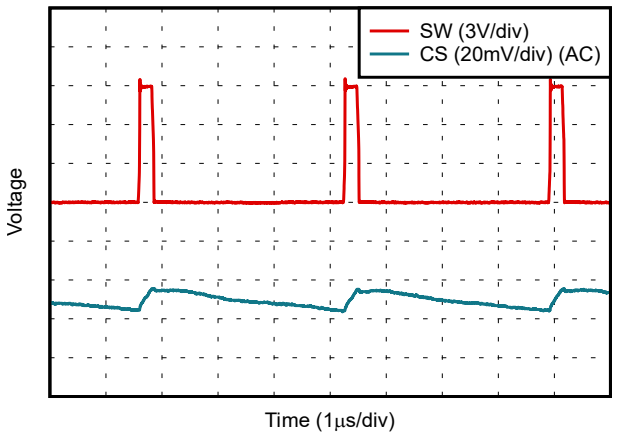


Figure 4-19. Current Sense Signal at 0A

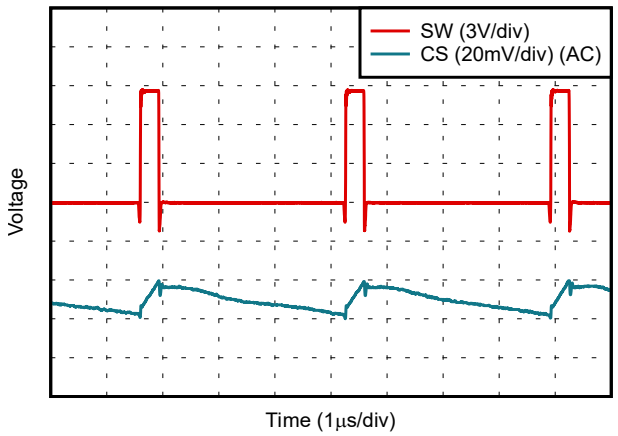
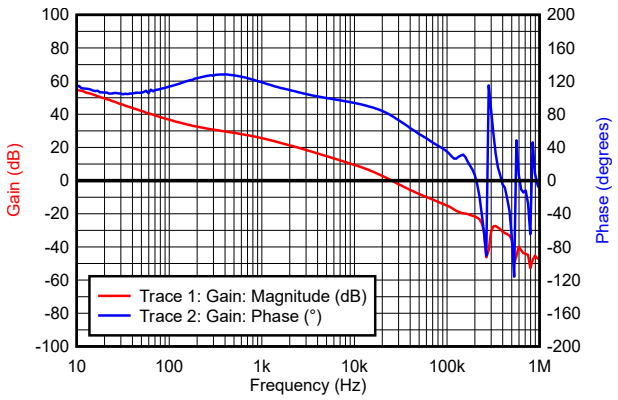
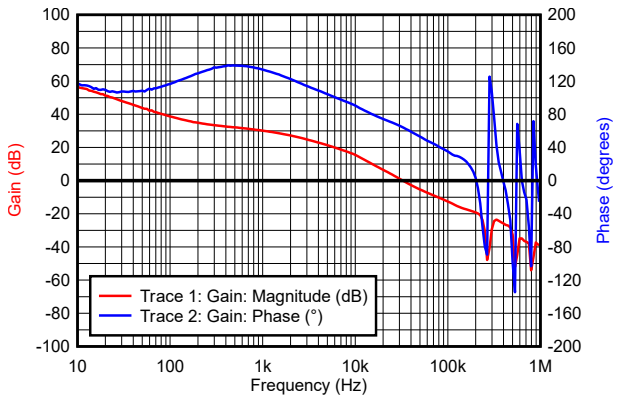


Figure 4-20. Current Sense Signal at 44A



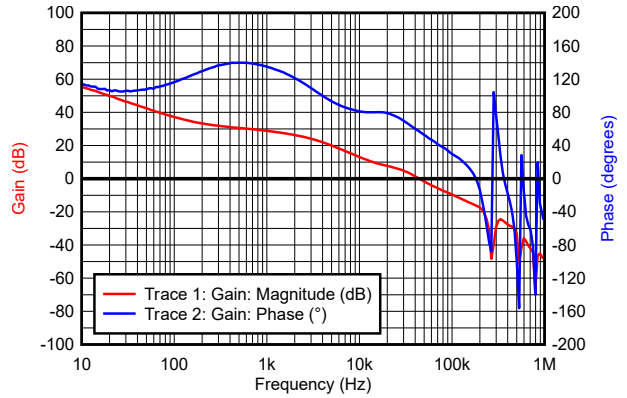
Phase Margin = 78°, Gain Margin = 22dB

Figure 4-21. Bode Plot at 100mA



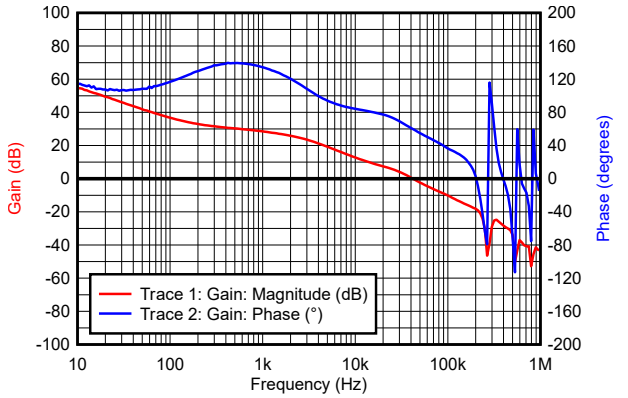
Phase Margin = 64°, Gain Margin = 19dB

Figure 4-22. Bode Plot at 10A



Phase Margin = 57°, Gain Margin = 16dB

Figure 4-23. Bode Plot at 40A



Phase Margin = 60°, Gain Margin = 18dB

Figure 4-24. Bode Plot at 44A

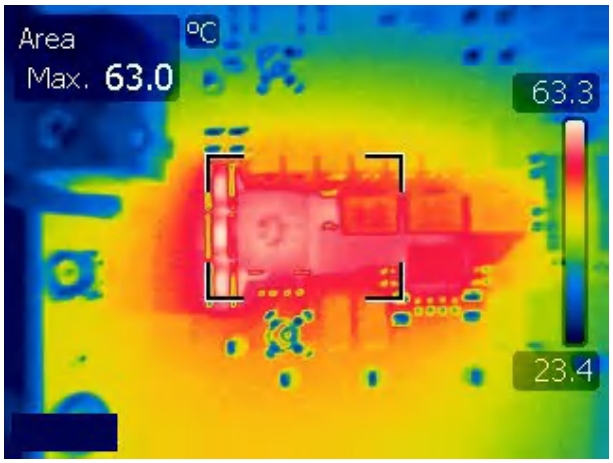


Figure 4-25. Thermals at 30A

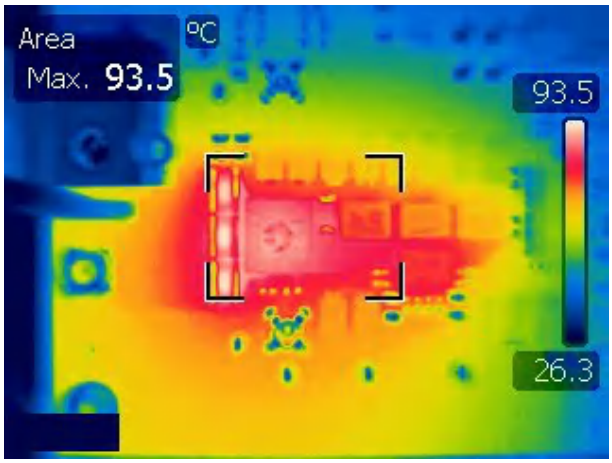


Figure 4-26. Thermals at 40A

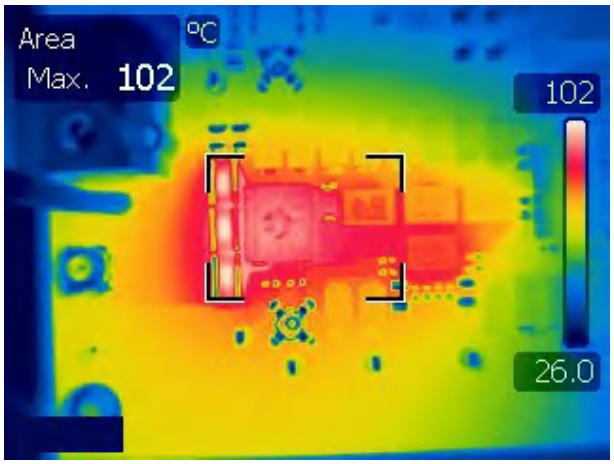


Figure 4-27. Thermals at 44A

4.3.2 Buck Regulators (Integrated)

4.3.2.1 1V2

Unless otherwise noted, VIN = 12V in Figure 4-28 to Figure 4-34.

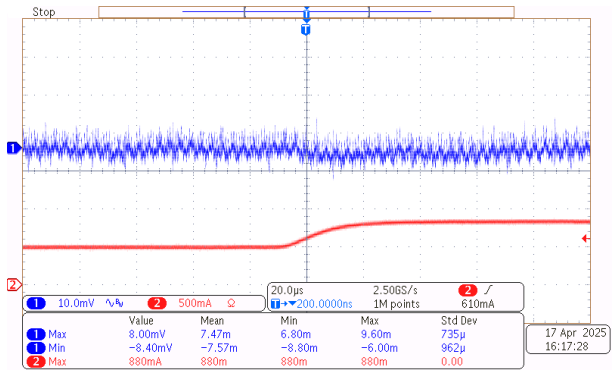


Figure 4-28. Load Step: 0.5A to 0.83A

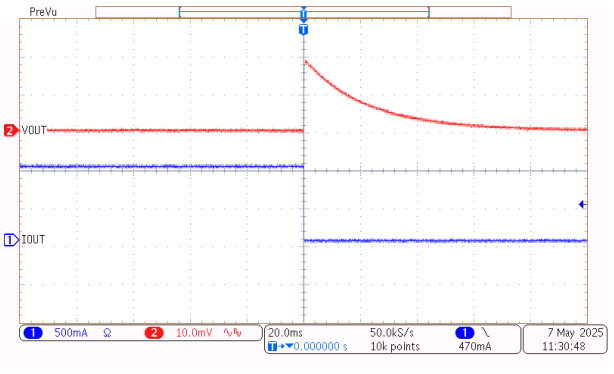
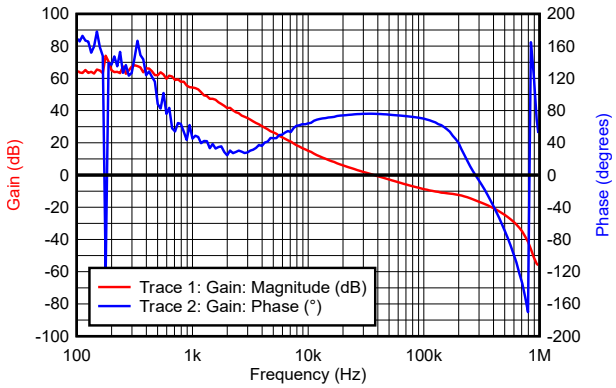
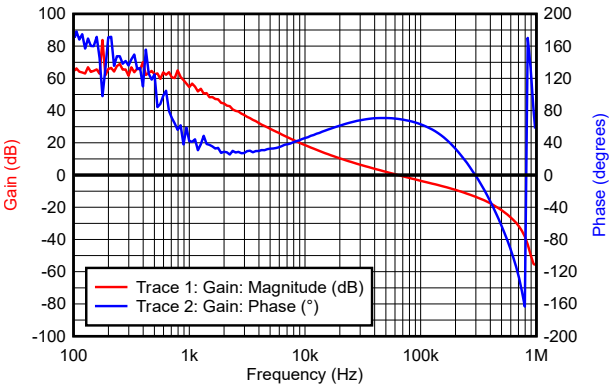


Figure 4-29. Load Step: 0.83A to 0.5A



Phase Margin = 76°, Gain Margin = 16dB

Figure 4-30. Bode Plot at 10mA



Phase Margin = 70°, Gain Margin = 13dB

Figure 4-31. Bode Plot at 2A

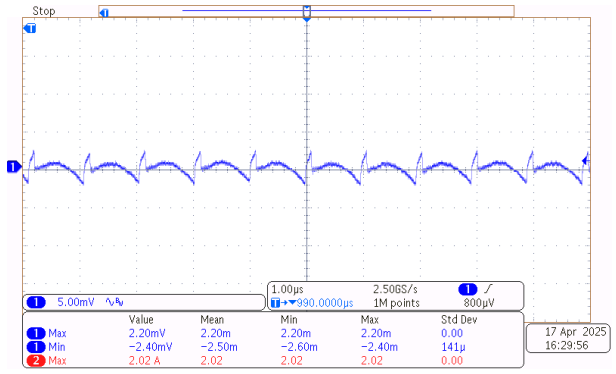


Figure 4-32. Output Voltage Ripple at 2A

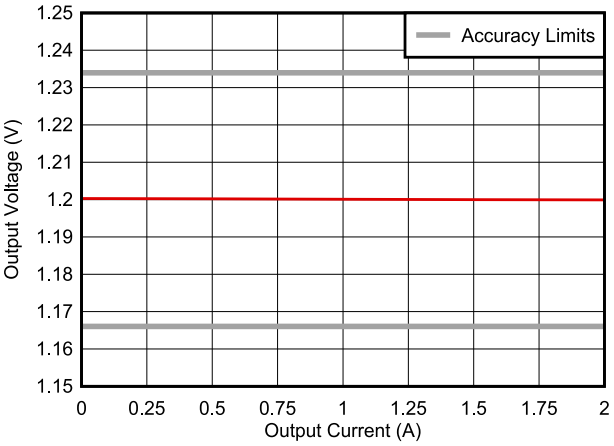


Figure 4-33. Load Regulation from 0A to 2A

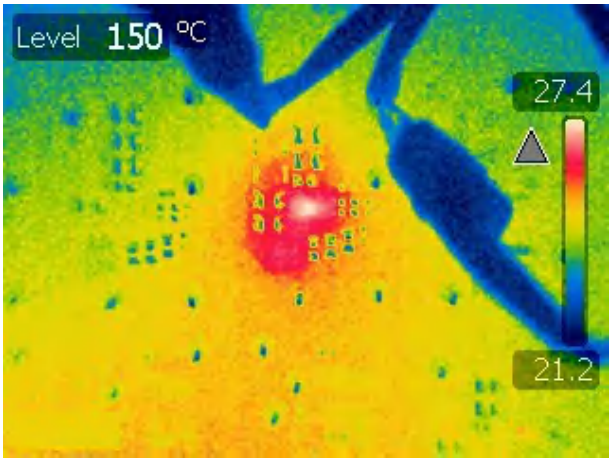


Figure 4-34. Thermals at 2A

4.3.2.2 1V2_VCCO

Unless otherwise noted, VIN = 12V in Figure 4-35 to Figure 4-41.

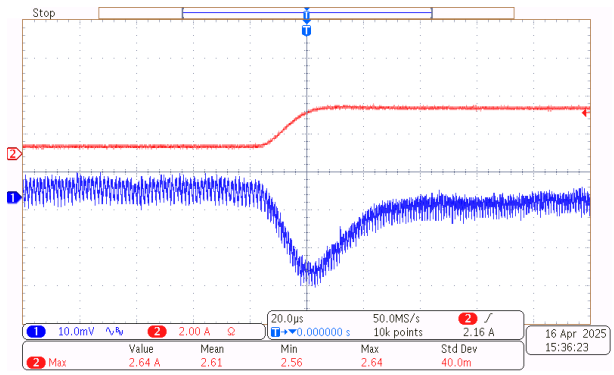


Figure 4-35. Load Step: 0.5A to 2.5A

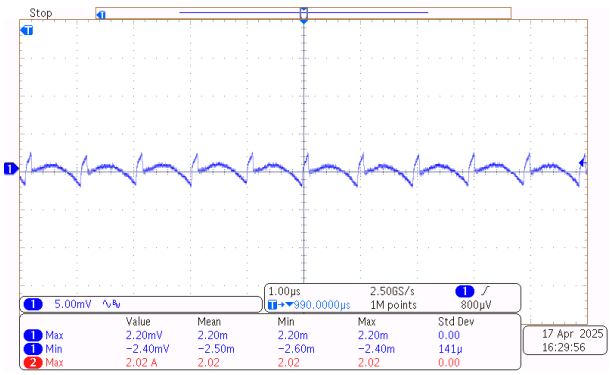
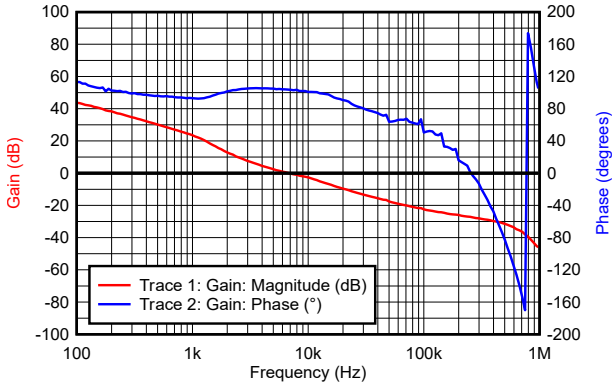
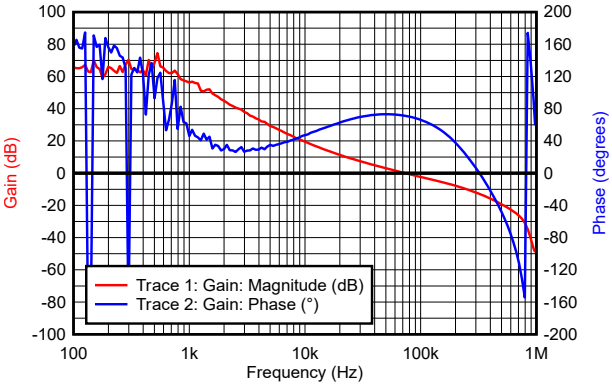


Figure 4-36. Load Step: 2.5A to 0.5A



Phase Margin = 104°, Gain Margin = 27dB

Figure 4-37. Bode Plot at 10mA



Phase Margin = 71°, Gain Margin = 13dB

Figure 4-38. Bode Plot at 4A

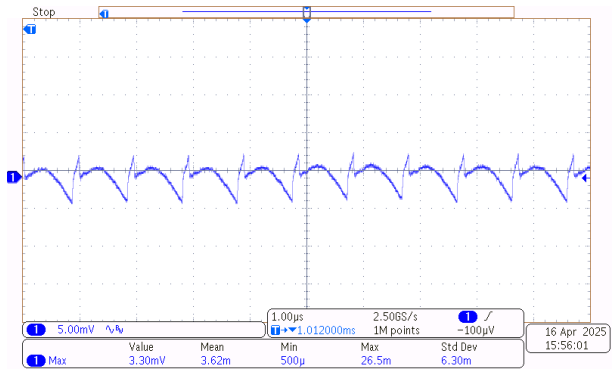


Figure 4-39. Output Voltage Ripple at 4A

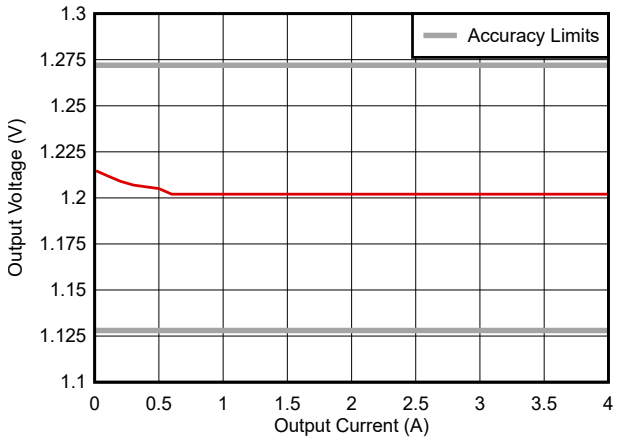


Figure 4-40. Load Regulation from 0A to 4A

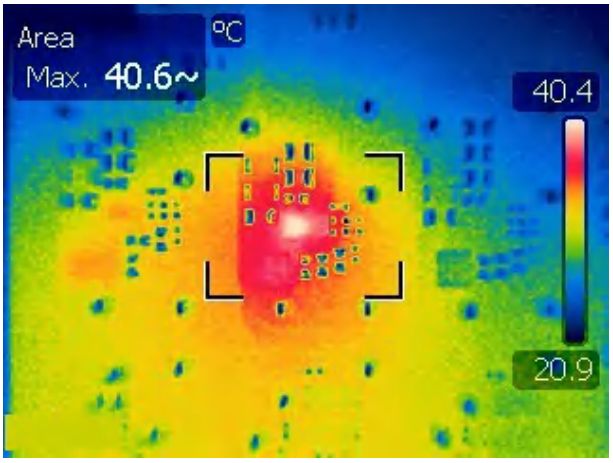


Figure 4-41. Thermals at 4A

4.3.2.3 1V2_MEM

Unless otherwise noted, VIN = 12V in Figure 4-42 to Figure 4-48.

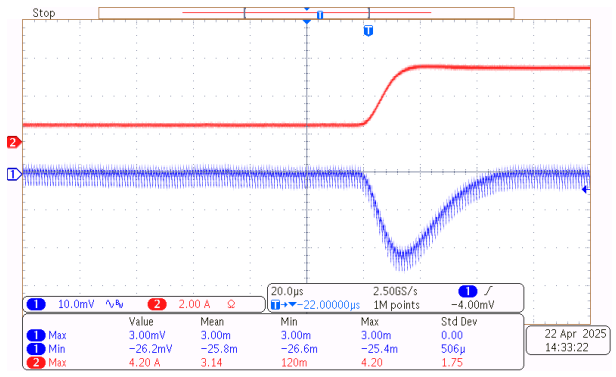


Figure 4-42. Load Step: 1A to 4A

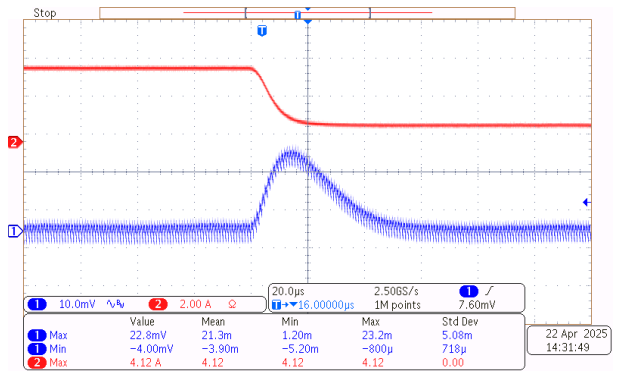
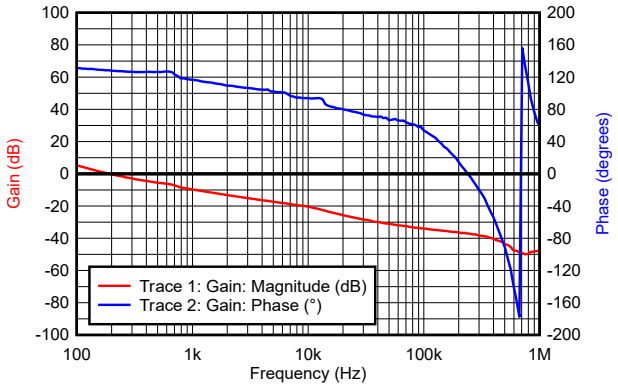
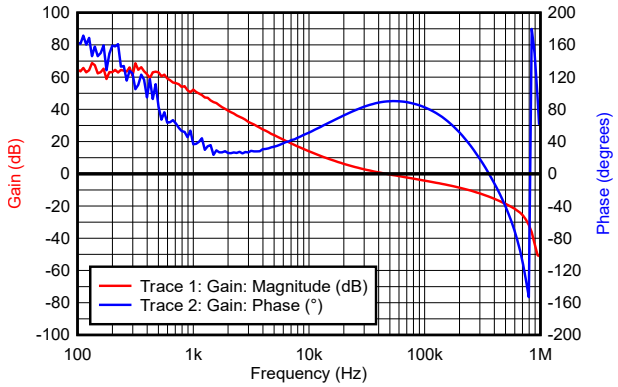


Figure 4-43. Load Step: 4A to 1A



Phase Margin = 128°, Gain Margin = 37dB

Figure 4-44. Bode Plot at 10mA



Phase Margin = 90°, Gain Margin = 14dB

Figure 4-45. Bode Plot at 6A

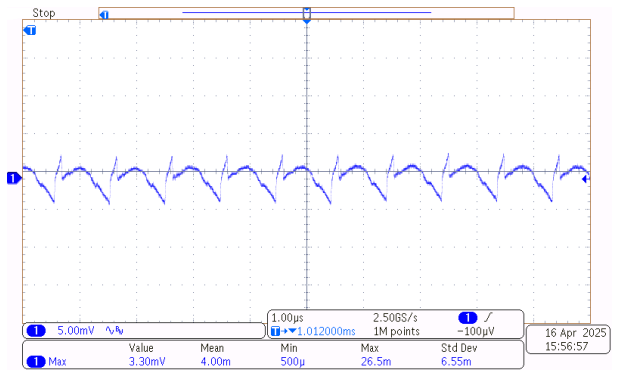


Figure 4-46. Output Voltage Ripple at 6A

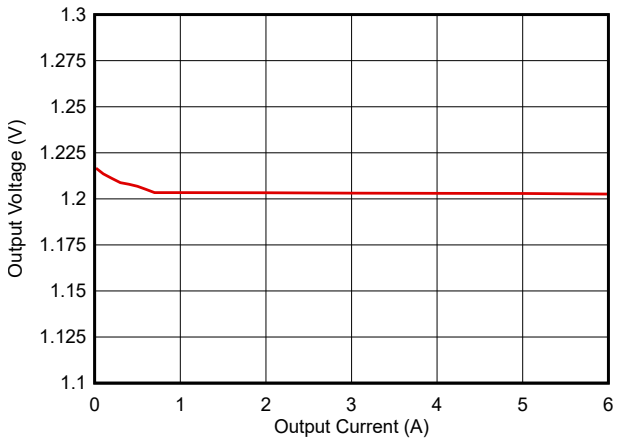


Figure 4-47. Load Regulation from 0A to 6A

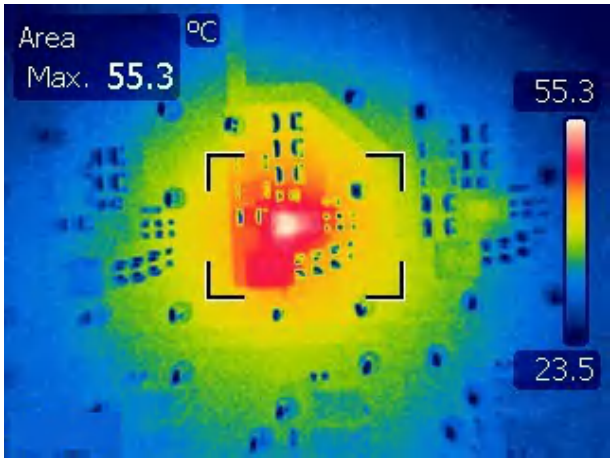


Figure 4-48. Thermals at 6A

4.3.2.4 2V5_DDR_VPP

Unless otherwise noted, VIN = 12V in Figure 4-49 to Figure 4-55.

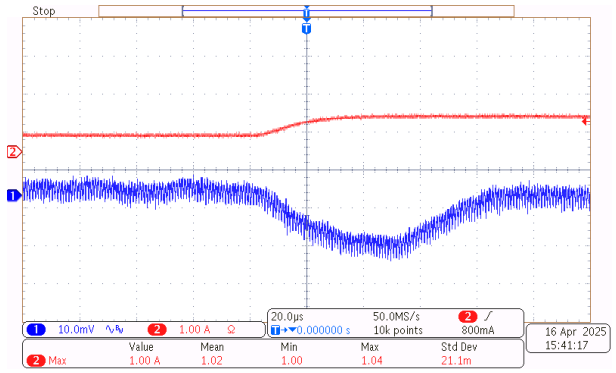


Figure 4-49. Load Step: 0.5A to 1A

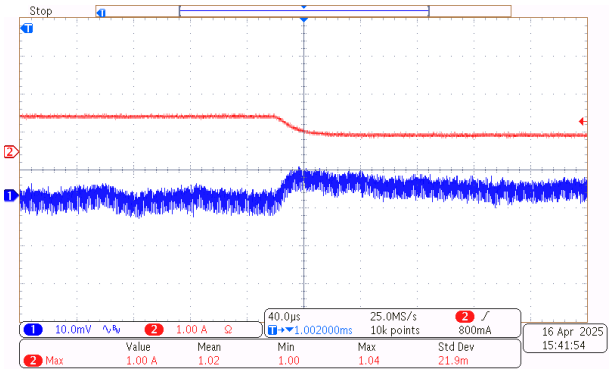
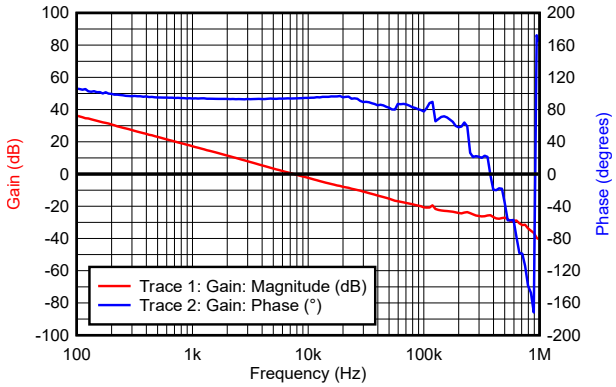
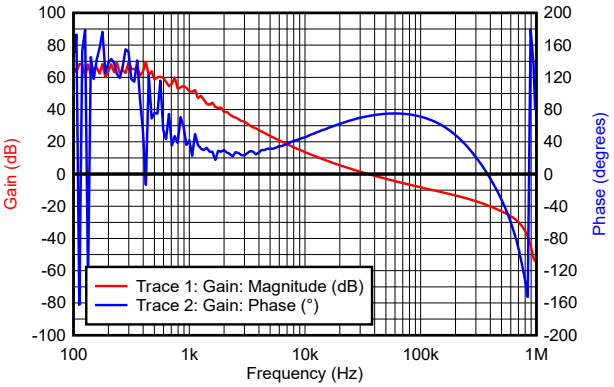


Figure 4-50. Load Step: 1A to 0.5A



Phase Margin = 94°, Gain Margin = 26dB

Figure 4-51. Bode Plot at 10mA



Phase Margin = 72°, Gain Margin = 19dB

Figure 4-52. Bode Plot at 3A

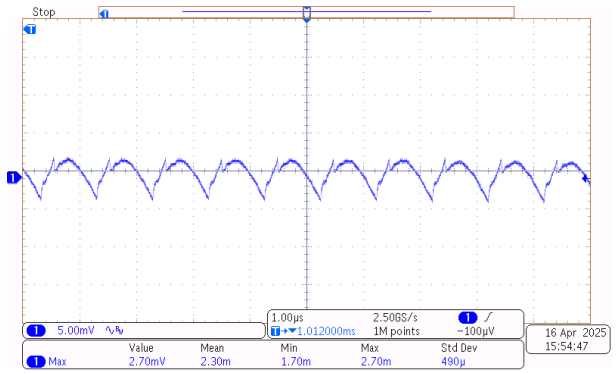


Figure 4-53. Output Voltage Ripple at 3A

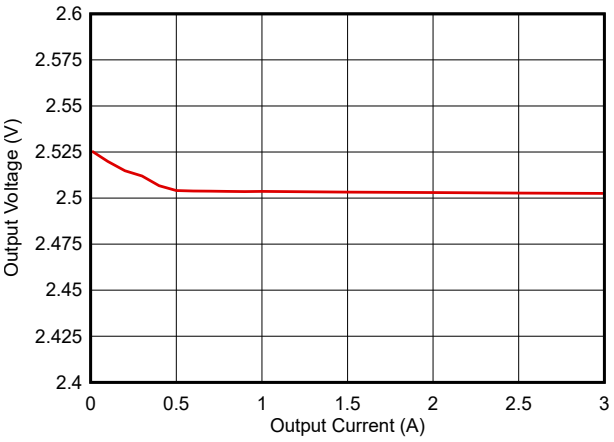


Figure 4-54. Load Regulation from 0A to 3A

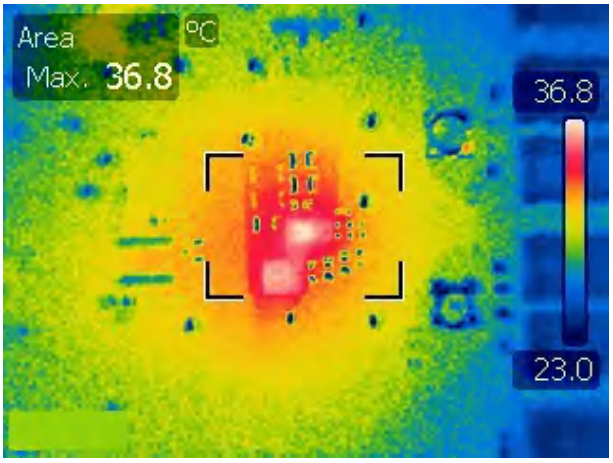


Figure 4-55. Thermals at 3A

4.3.2.5 3V3_VCCO

Unless otherwise noted, VIN = 12V in Figure 4-56 to Figure 4-62.

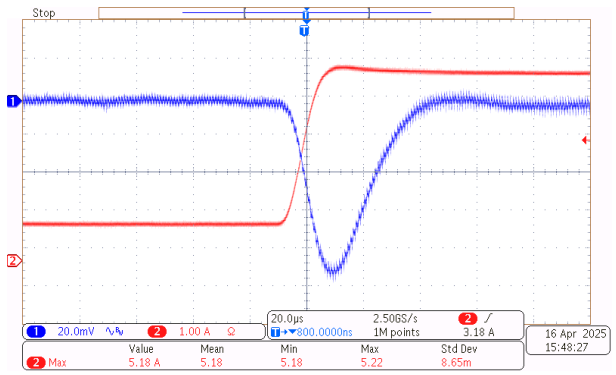


Figure 4-56. Load Step: 1A to 5A

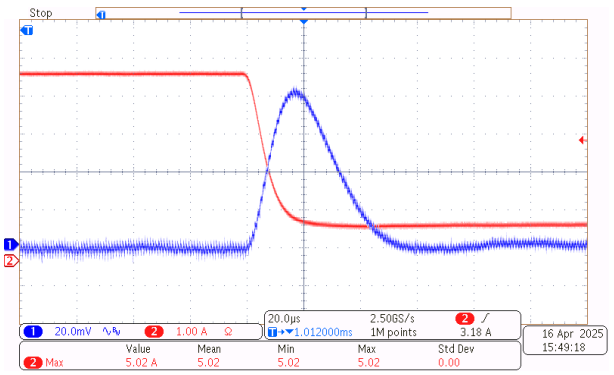
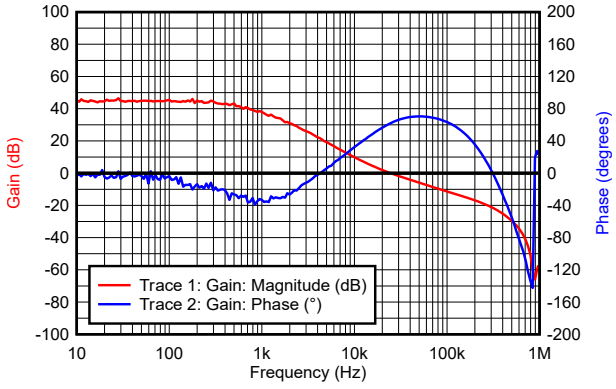
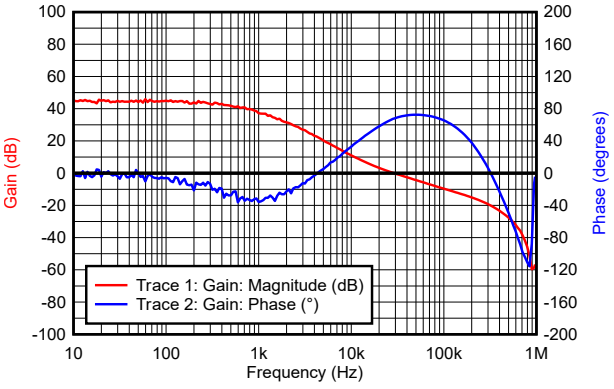


Figure 4-57. Load Step: 5A to 1A



Phase Margin = TBD°, Gain Margin = TBD dB

Figure 4-58. Bode Plot at 10mA



Phase Margin = 68°, Gain Margin = 22dB

Figure 4-59. Bode Plot at 6A

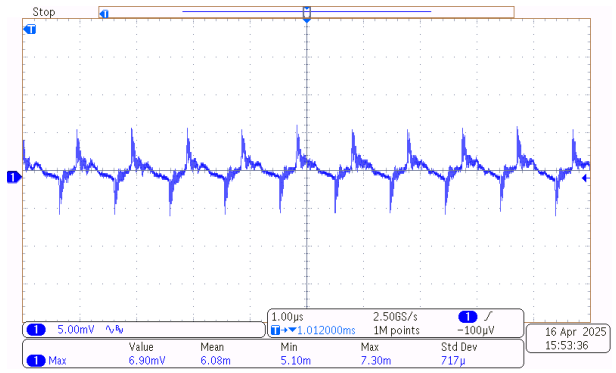


Figure 4-60. Output Voltage Ripple at 6A

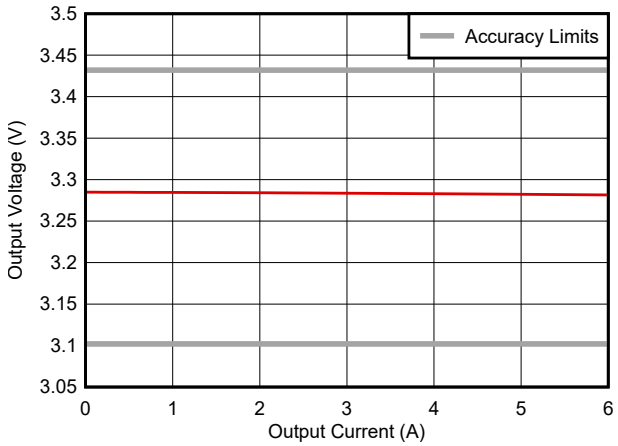


Figure 4-61. Load Regulation from 0A to 6A

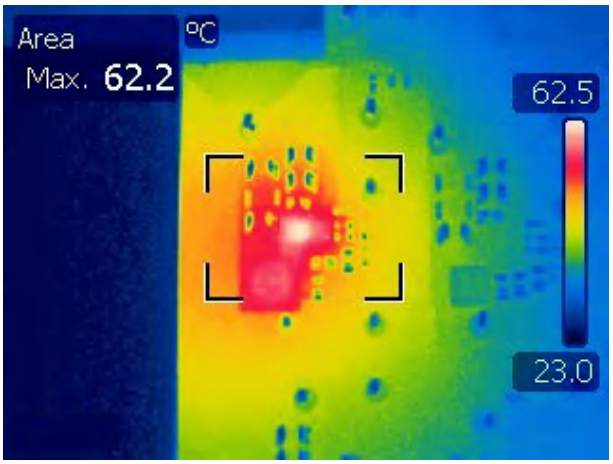


Figure 4-62. Thermals at 6A

4.3.3 Linear Regulators

4.3.3.1 0V6_VTT

Unless otherwise noted, VIN = 12V in Figure 4-63 to Figure 4-70.

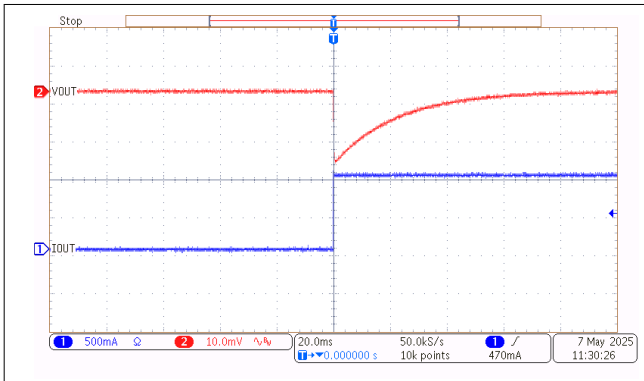


Figure 4-63. Load Step: 0A to 1A

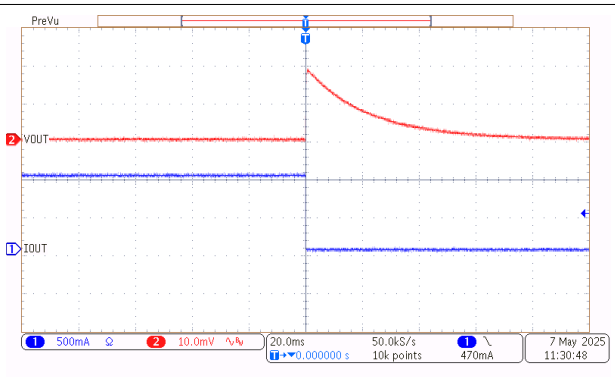
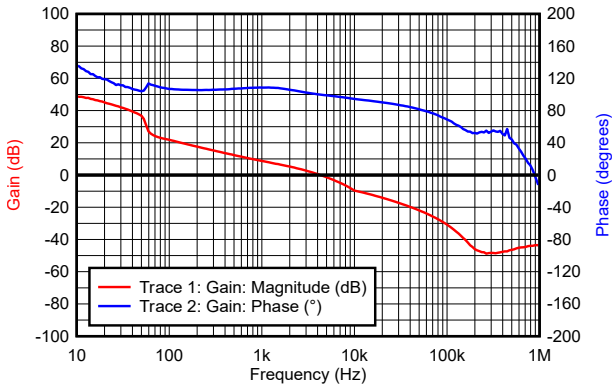
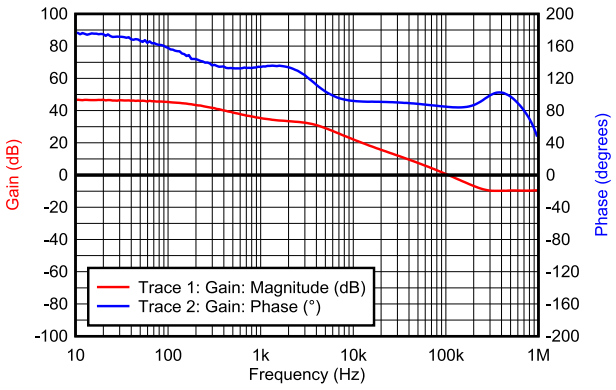


Figure 4-64. Load Step: 1A to 0A



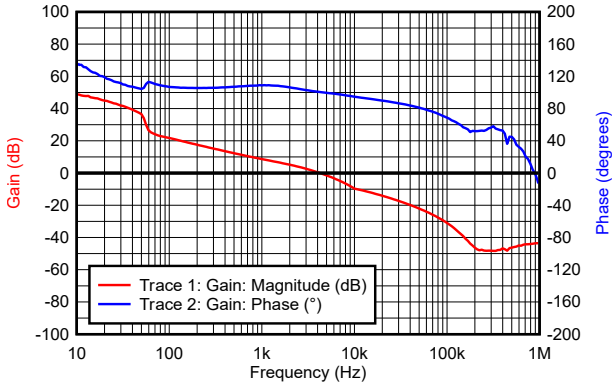
Phase Margin = 100°, Gain Margin = 44dB

Figure 4-65. Bode Plot at 10mA



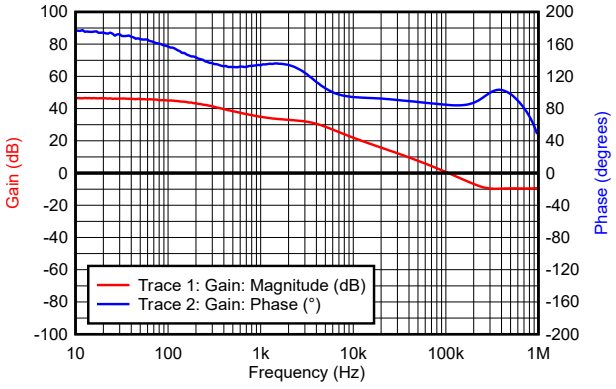
Phase Margin = 85°, Gain Margin = 9dB

Figure 4-66. Bode Plot at 3A



Phase Margin = 100°, Gain Margin = 44dB

Figure 4-67. Bode Plot at –10mA



Phase Margin = 84°, Gain Margin = 9dB

Figure 4-68. Bode Plot at –3A

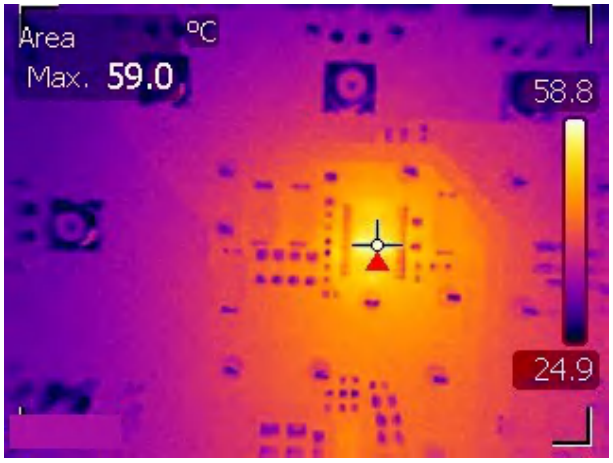


Figure 4-69. Thermals at I_{VTT} = 3A, I_{VTTREF} = 10mA

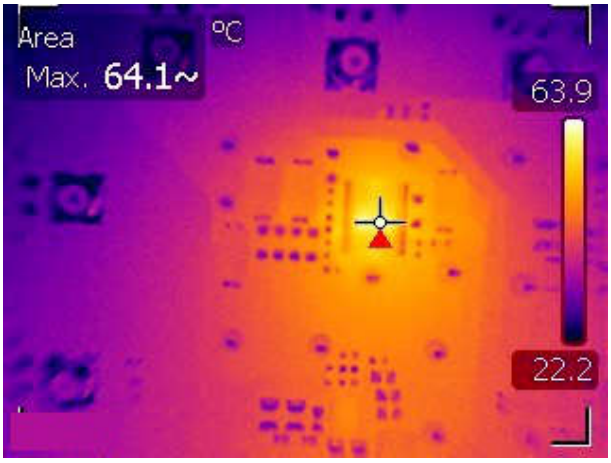


Figure 4-70. Thermals at I_{VTT} = –3A, I_{VTTREF} = –10mA

4.3.3.2 0V92

Unless otherwise noted, VIN = 12V in Figure 4-71 to Figure 4-76.

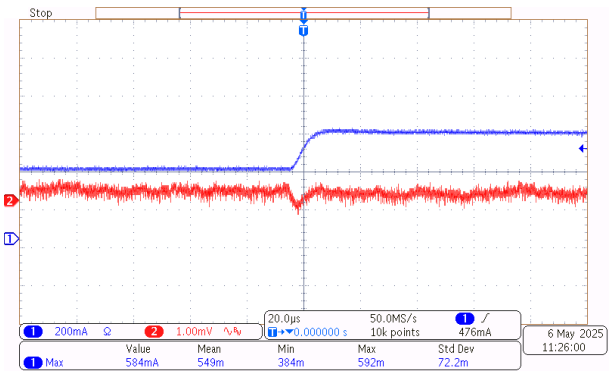


Figure 4-71. Load Step: 0.2A to 0.395A

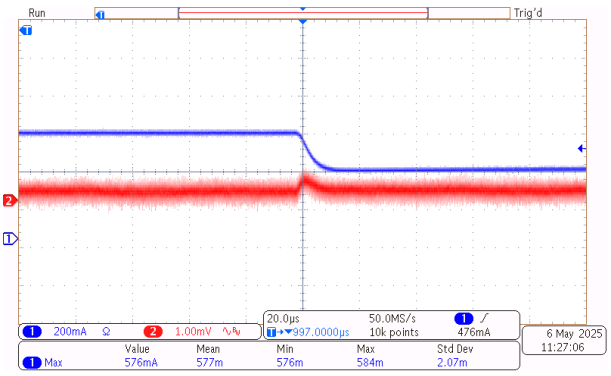
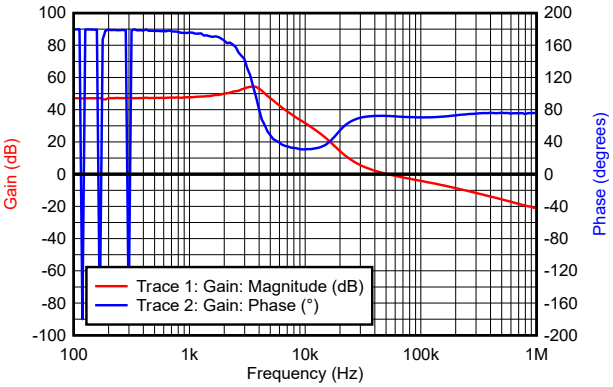
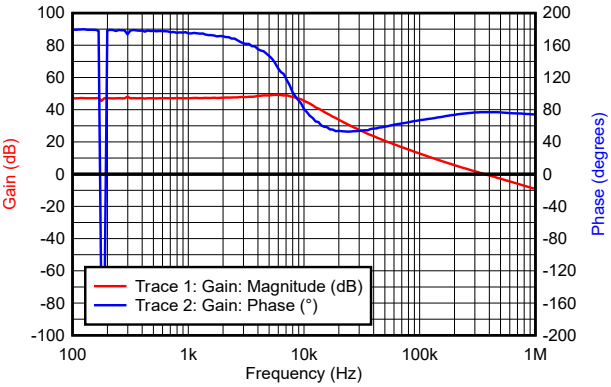


Figure 4-72. Load Step: 0.395A to 0.2A



Phase Margin = 72°

Figure 4-73. Bode Plot at 10mA



Phase Margin = 77°

Figure 4-74. Bode Plot at 1A

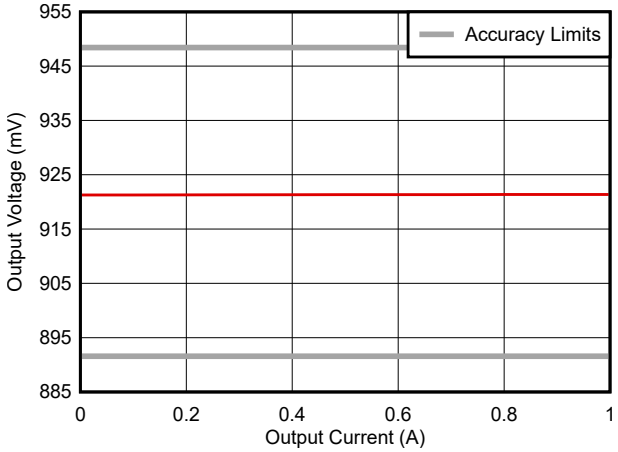


Figure 4-75. Load Regulation from 0A to 1A

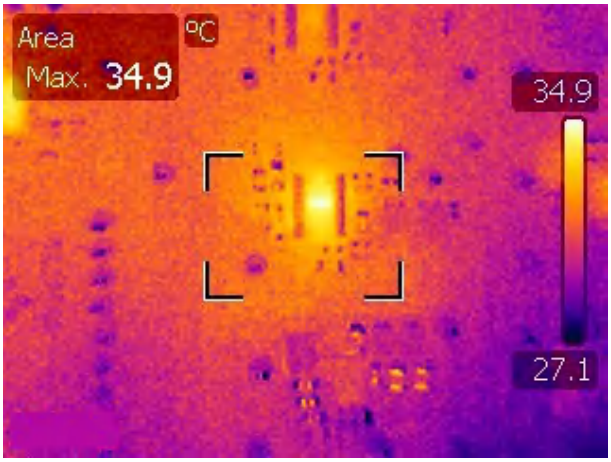


Figure 4-76. Thermals at 1A

4.3.3.3 1V5_GTY

Unless otherwise noted, VIN = 12V in Figure 4-77 to Figure 4-82.

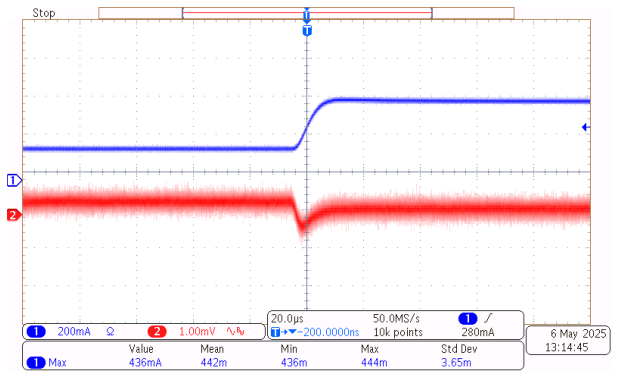


Figure 4-77. Load Step: 10mA to 35mA

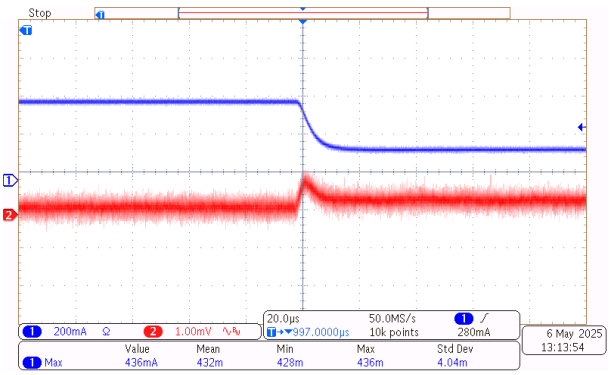
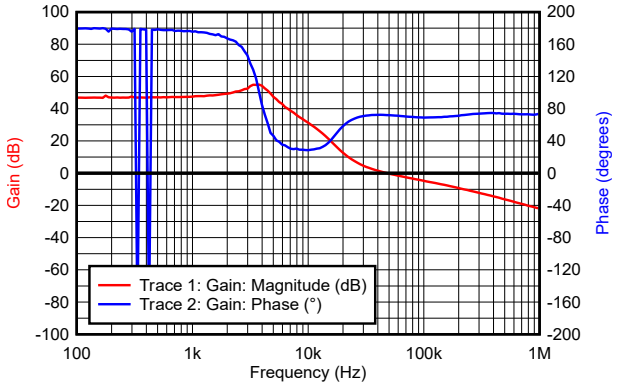
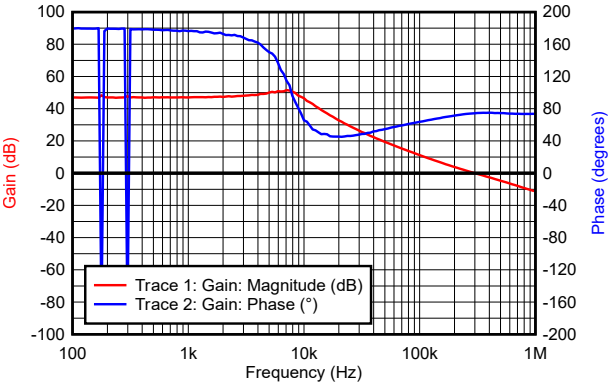


Figure 4-78. Load Step: 35mA to 10mA



Phase Margin = 72°

Figure 4-79. Bode Plot at 10mA



Phase Margin = 75°

Figure 4-80. Bode Plot at 200mA

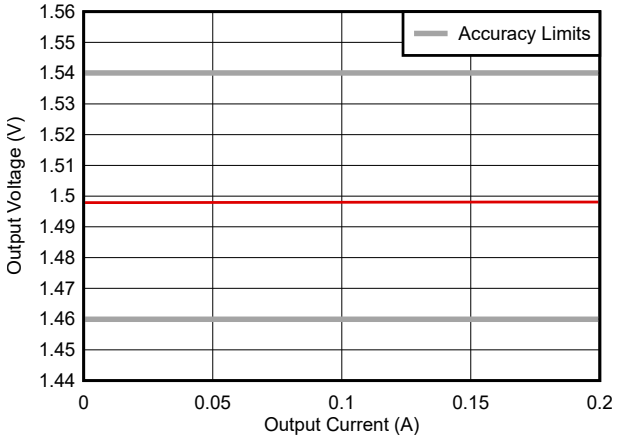


Figure 4-81. Load Regulation from 0A to 1A

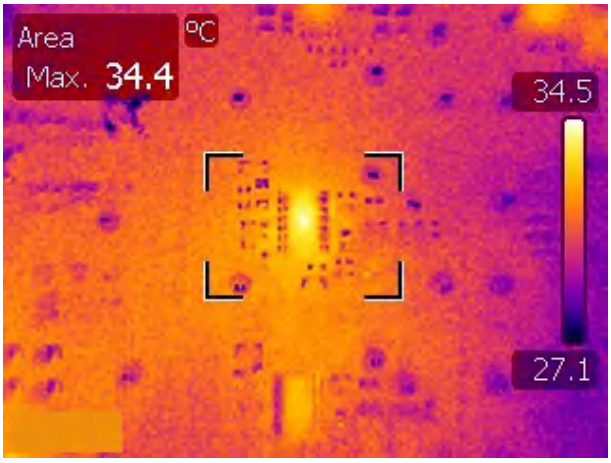


Figure 4-82. Thermals at 200mA

4.3.3.4 1V5

Unless otherwise noted, VIN = 12V in Figure 4-83 to Figure 4-91.

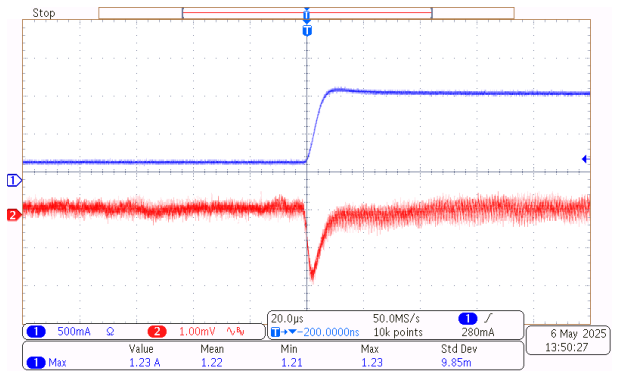


Figure 4-83. Load Step: 0.2A to 1.1A

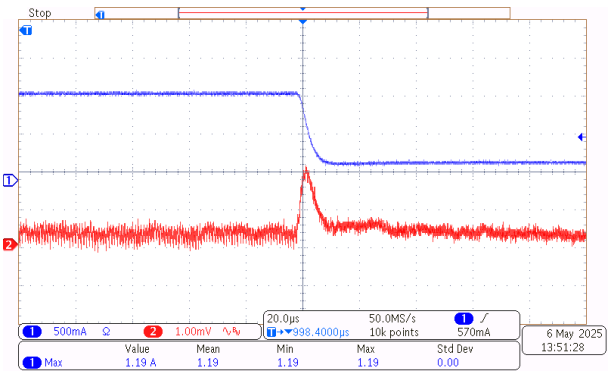


Figure 4-84. Load Step: 1.1A to 0.2A

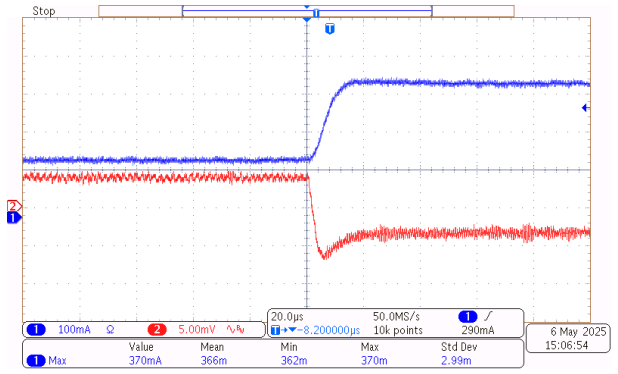


Figure 4-85. Load Step of VCCAUX_SMON: 0.2A to 1.1A

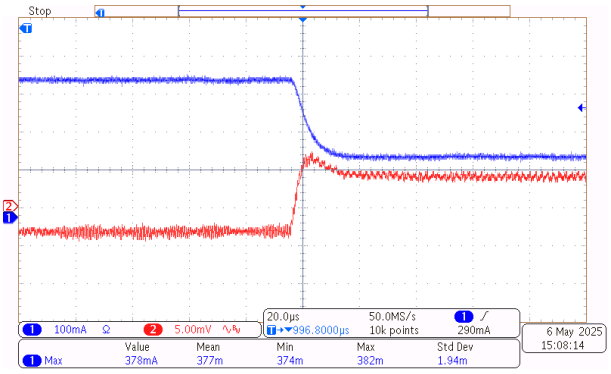
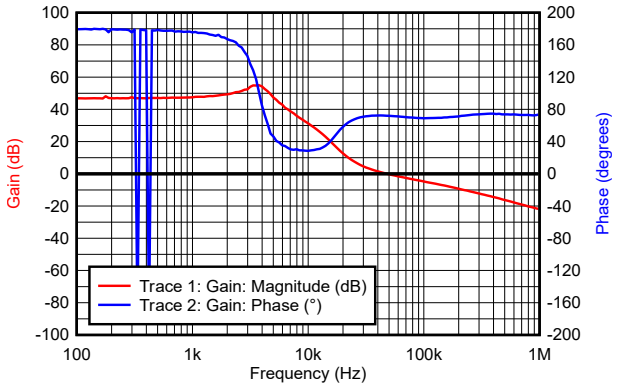
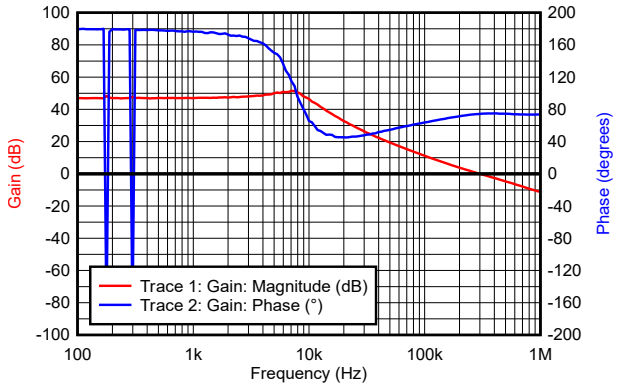


Figure 4-86. Load Step of VCCAUX_SMON: 1.1A to 0.2A



Phase Margin = 71°

Figure 4-87. Bode Plot at 10mA



Phase Margin = 77°

Figure 4-88. Bode Plot at 1.5A

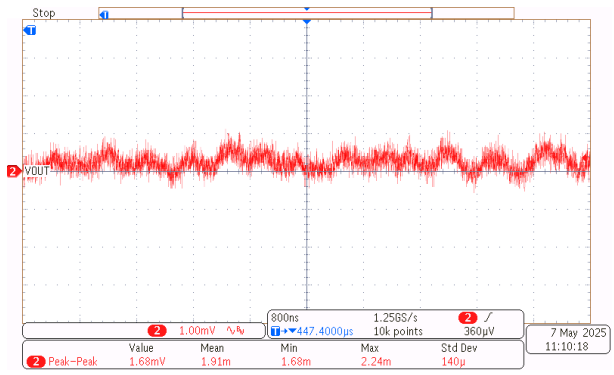


Figure 4-89. 1V5 Output Ripple

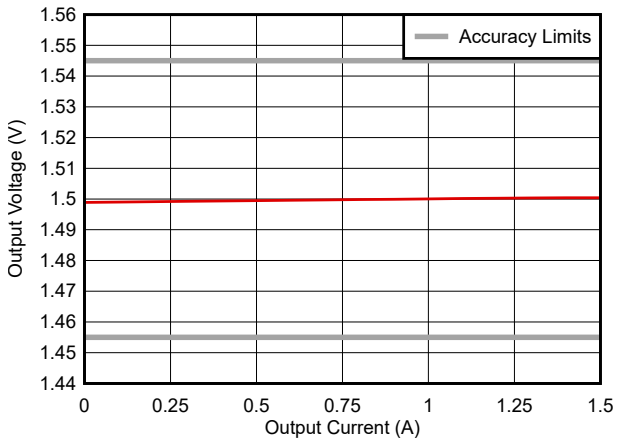


Figure 4-90. Load Regulation from 0A to 1.5A

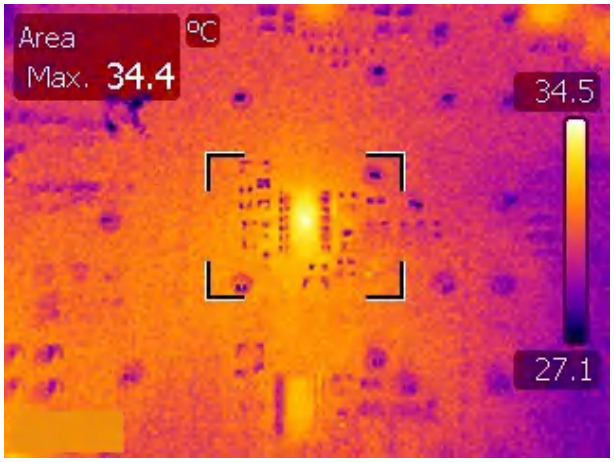


Figure 4-91. Thermals at 1.5A

4.3.3.5 5V0_SYS

Unless otherwise noted, VIN = 12V in Figure 4-92 to Figure 4-96.

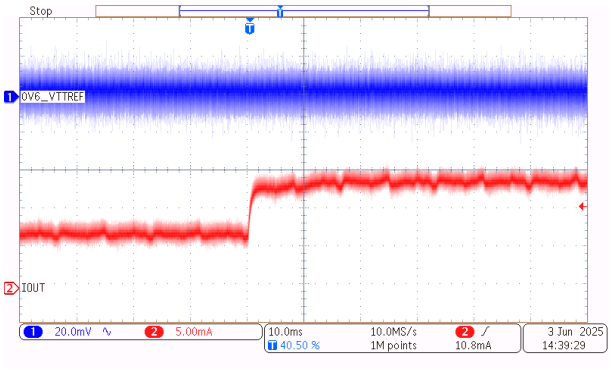


Figure 4-92. Load Step: 1mA to 10mA

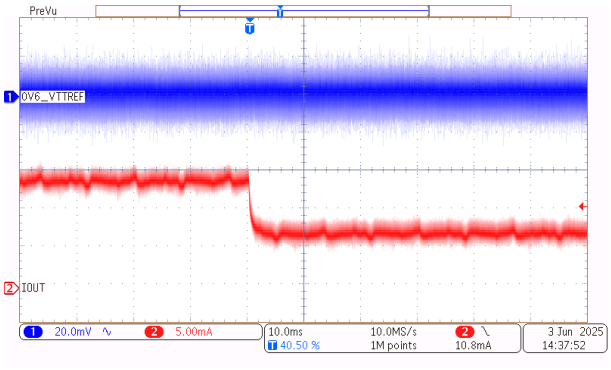
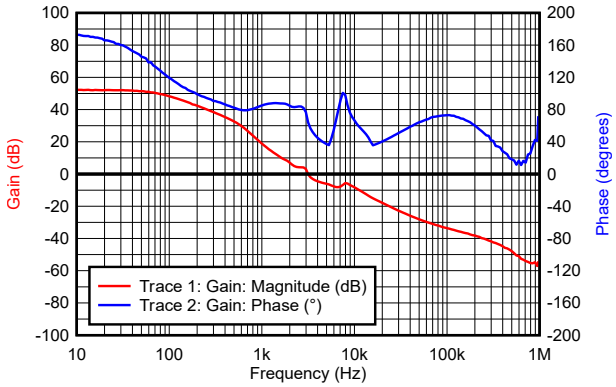
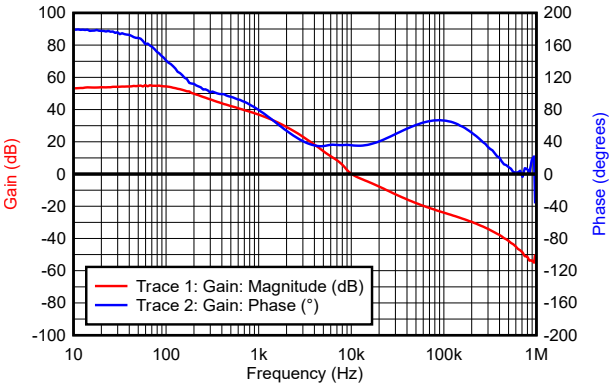


Figure 4-93. Load Step: 10mA to 1mA



Phase Margin = 63°

Figure 4-94. Bode Plot at 10mA



Phase Margin = 36°

Figure 4-95. Bode Plot at 50mA

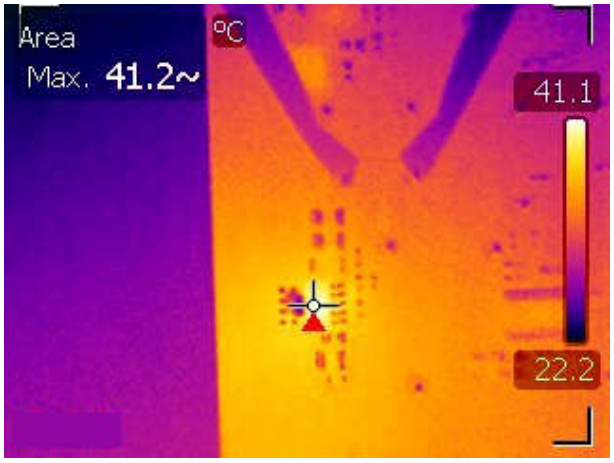


Figure 4-96. Thermals at 50mA

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-050088.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050088.

5.1.3 Layout Prints

To download the layer plots, see the design files at TIDEP-01036.

5.2 Documentation Support

1. Texas Instruments, *TPS7H500x-SEP Radiation-Tolerant 2MHz Current Mode PWM Controllers in Space Enhanced Plastic Data Sheet*
2. Texas Instruments, *TPS7H60x5-SP and TPS7H60x5-SEP Radiation-Hardness-Assured Half Bridge GaN FET Gate Drivers Data Sheet*
3. Texas Instruments, *TPS7H1111-SP and TPS7H1111-SEP 1.5-A, Ultra-Low Noise, High PSRR Radiation Hardened Low Dropout (LDO) Linear Regulator Data Sheet*
4. Texas Instruments, *TPS7H4010-SEP Radiation Hardened 3.5-V to 32-V, 6-A Synchronous Step-Down Voltage Converter in Space Enhanced Plastic Data Sheet*
5. Texas Instruments, *TPS73801-SEP 1-A Low-Noise Fast-Transient-Response Low-Dropout Regulator in Space Enhanced Plastic Data Sheet*
6. Texas Instruments, *TPS7H3302-SP and TPS7H3302-SEP 3-A DDR Radiation Hardened Termination Regulator Data Sheet*
7. Texas Instruments, *TPS7H3014-SP and TPS7H3014-SEP Radiation-Hardened, 14V, 4-Channel Sequencer Data Sheet*
8. Texas Instruments, *TPS7H2221-SEP Radiation Tolerant 5.5-V, 1.25-A, 115-mΩ Load Switch Data Sheet*
9. Texas Instruments, *SN54SC6T14-SEP Radiation Tolerant, Hex Schmitt-Trigger Inverters With Integrated Translation Data Sheet*

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

KYLE RAKOS is the Systems Manager for the Space Power Product Line at Texas Instruments where he is responsible for the road map of radiation-hardened and radiation-tolerant power parts. He earned his Bachelors of Science degree in Computer Engineering from Purdue University in 2017. Kyle thanks Daniel Hartung, Bhavika Kagathi, and Elizabeth Ann Won for the assistance on this design and paper.

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