Design Guide: TIDA-010210

11-kW, Bidirectional, Three-Phase ANPC Based on GaN Reference Design

Description

This reference design provides a design template for implementing a three-level, three-phase, gallium nitride (GaN) based ANPC inverter power stage. The use of fast switching power devices makes it possible to switch at a higher frequency of 100 kHz, reducing the size of magnetics for the filter and increasing the power density of the power stage. The multilevel topology allows the use of 600-V rated power devices at higher DC bus voltages of up to 1000 V. The lower switching voltage stress reduces switching losses, resulting in a peak efficiency of 98.5%.

Resources

TIDA-010210	Design Folder
LMG3422R030	Product Folder
UCC21541	Product Folder
TMDSCNCD280049C	Tool Folder
TMS320F280049C	Product Folder
AMC3302, OPA4376	Product Folder
ISO7741, SN6501	Product Folder
TPS563200, LP5907	Product Folder
TLV9004, LMT87	Product Folder

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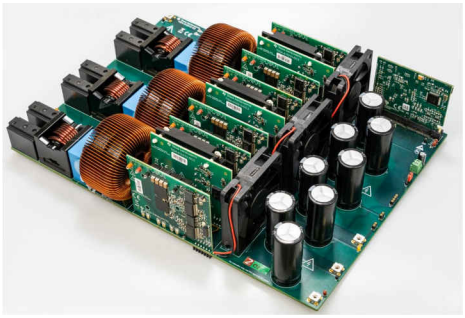
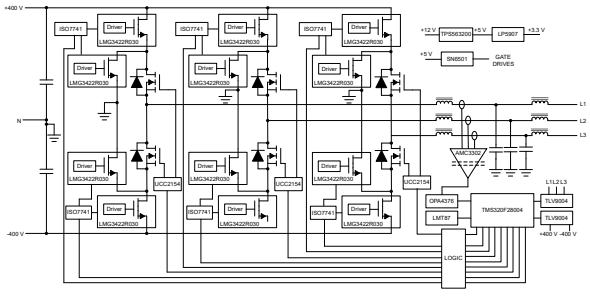
Features

- Power stage for three-phase inverters and PFCs using GaN switch
- 600-V rated switches in 800-V system (due to three levels)
- Novel onboard protection implemented using CLB of C2000
- Iso-quad channel driver supports high-frequency operation (100 kHz)
- Shunt-based current sense (high accuracy and linearity over temperature)
- Power module with up to 16-A current (on AC side)
- High power density due to high switching frequency (100 kHz) and high efficiency (> 98% at full load)
- Bidirectional operation with < 1-ms direction changeover
- Low component stress helps improve system reliability
- Optimized control scheme needs only 6 PWMs versus 9 PWMs for standard implementation
- Reduced cost - four high frequency switches (versus six) per arm
- Real-time safety operation with no extra cost

Applications

- String inverter
- DC wallbox charger
- Power conversion system (PCS)





1 System Description

Modern commercial scale solar inverters are seeing innovation on multiple fronts, which lead to smaller, higher efficiency products in the market:

- The move to higher voltage solar arrays
- Reducing the size of onboard magnetics
- Inclusion of localized power storage requiring bidirectional power stages

By increasing the voltage to 1000-V or 1500-V DC from the array, the current can be reduced to maintain the same power levels. The reduction in current reduces conduction losses and hence results in higher efficiency. The reduction in di/dt also reduces the stress on electrical components. However, high DC bus voltages can limit the choice of power components that can be used as devices with higher voltage withstand capability is needed.

To compensate for the voltage stresses generated by high-voltage solar arrays, new topologies of solar inverters have been designed. Traditional half bridges block the full input voltage on each switching device. By adding additional power components, the overall stress on the device can be significantly reduced. This reference design shows how to implement a three-level ANPC converter that limits the voltage stress on all the power components to only half the DC bus voltage, allowing use of more abundant and faster power components. This design also demonstrates the use GaN devices in solar inverters which was not possible with other topologies due to their limitation of voltage withstand capability.

Additional power density is also being enabled by moving to higher switching speeds in power converters. As this design shows, a higher switching speed reduces the overall size requirement of the output filter stage—a primary contributor to the design size.

Though multilevel topologies enable the use of lower voltage switching devices, they come with certain limitations – the need to drive more switches and need to avoid overvoltage even during abnormal operation. This design tries to demonstrate how to address all 18 power devices in the power stage with the limited number of PWMs available from a common MCU and also how to implement hardware based interlocking protections needed to avoid device overvoltage under all operating conditions without the use of additional components.

Another requirement that is becoming more prevalent for inverter power stages is the need for bidirectional power transfer. This is important in storage ready inverters where there can be a need for the power from the grid to be stored in local power storage like a battery. The power conversion stage in an electronic energy storage system also has the same requirement. The ANPC power stage demonstrated in this design is inherently capable of bidirectional operation – only software is required for it to operate either as inverter or power factor controller (PFC). Currently the design is tested in inverter mode operation and the testing in PFC mode is in progress.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Output power	11 kW	At 400-V AC
Nominal AC voltage	Three-phase 400-V AC	
Output frequency	50 or 60 Hz	
Output current	16 A	
Nominal DC voltage	800-V DC	600-V to 800-V DC
Inverter switching frequency	100 kHz	
Efficiency	98.5%	At 400-V AC, 60% load
Power density	2.57 kW/L	

2 System Overview

2.1 Block Diagram

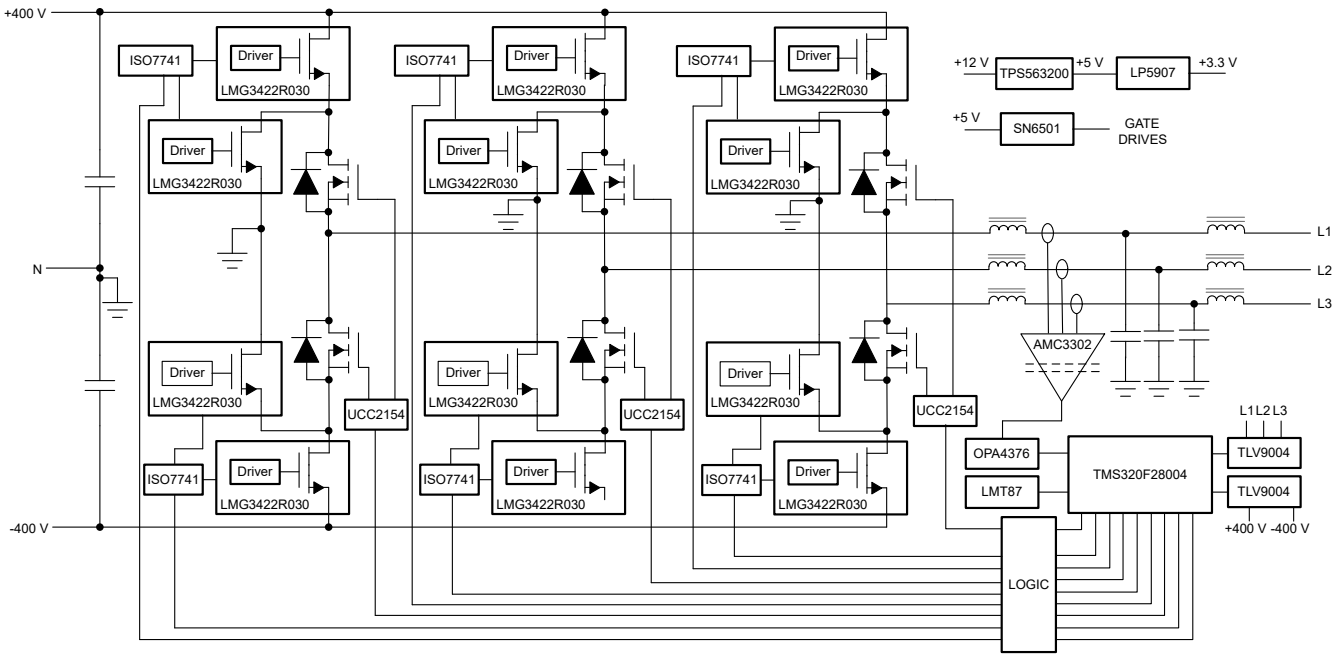


Figure 2-1. Block Diagram

This reference design is built in a modular construction to allow easy replacement of power switching devices to allow easy comparison between them. The following boards combine to form this three-phase inverter reference design:

- A motherboard, comprising of the LCL filter, sensing electronics, bias power, switching relays and cooling fans.
- A TMDSCNCD280049C Control Card to support the DSP.
- Six power cards switching at 100 kHz containing GaN power switching devices and isolated bias power supplies.
- Three power cards switching at 100 Hz and 120 Hz containing Si power switching devices, gate drivers and isolated bias power supplies.

Though the board can accept 12-V bias power from an external power supply, it has provision to add an auxiliary power supply that can run from the high voltage DC bus.

2.2 Design Considerations

2.2.1 Three-Phase ANPC Inverter Architecture Overview

The basic architecture of the ANPC topology is shown in Figure 2-2.

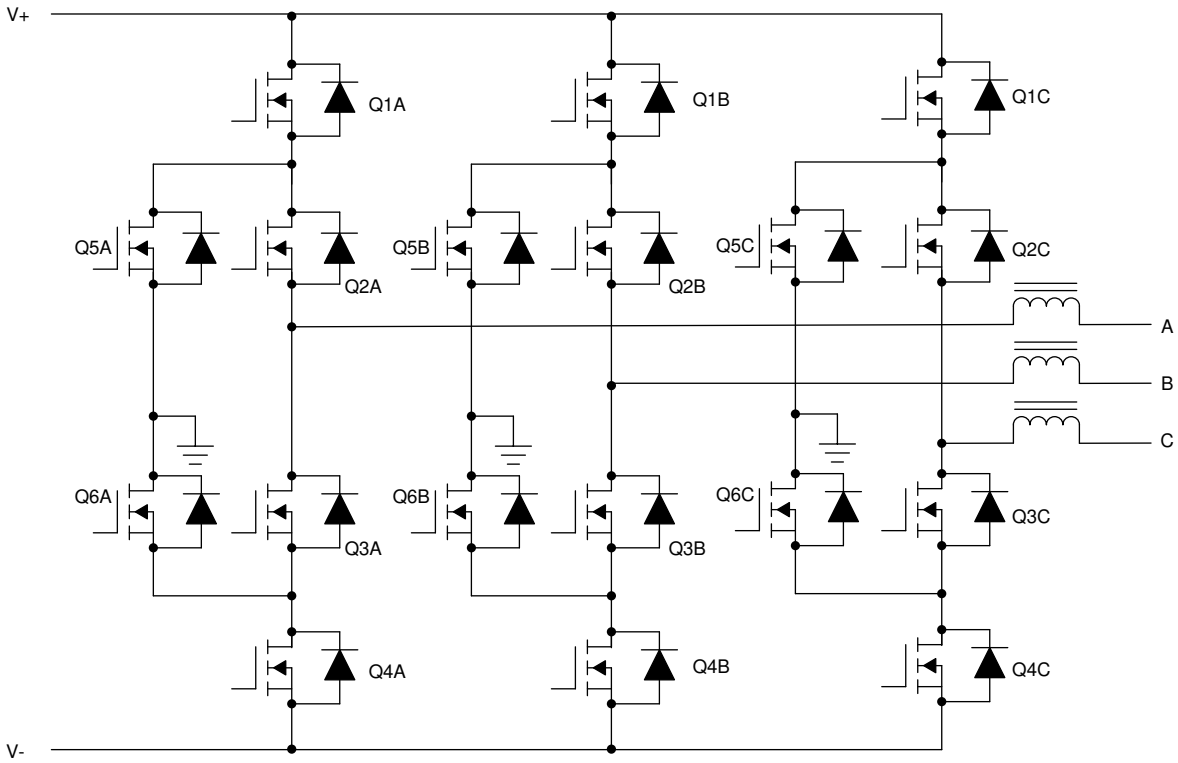


Figure 2-2. ANPC Three-Phase Inverter Architecture

To simplify the analysis, a single leg can be separated out as shown in Figure 2-3.

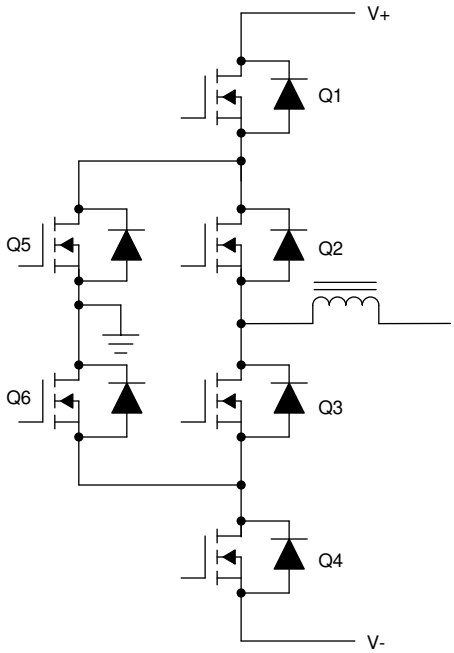


Figure 2-3. ANPC Single-Phase Inverter Leg

As can be seen, there are six switches in each phase. Though there can be various switching schemes to control this power stage, we selected a relatively simpler scheme to reduce complexity. The upper half of the circuit consisting of Q1, Q5 and Q2 is active during the positive half cycle and the lower half consisting of Q4, Q6 and Q3 is active during the negative half cycle. Q2 and Q3 are slow switches that connect the inductor to either the upper high frequency switching pair of Q1 & Q5 or Q4 & Q6 during positive and negative half cycles respectively. Each of the high frequency switching pairs is operated as a synchronous buck converter during their corresponding half cycles. The switching scheme is explained in detail in Figure 2-4 and Figure 2-5.

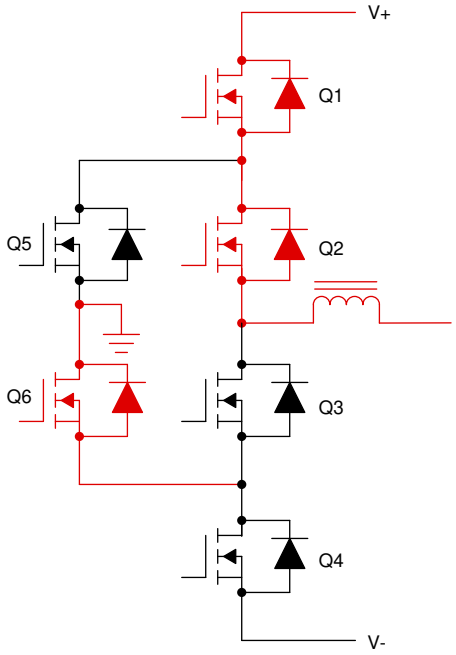


Figure 2-4. Inductor connected to V+

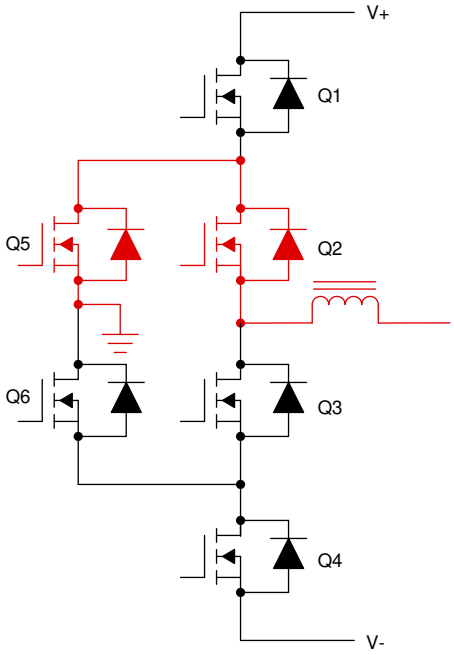


Figure 2-5. Inductor connected to N (+ve)

Figure 2-4 and Figure 2-5 show the operation of the circuit during the positive half cycle of this phase. The components in red are the ones that are conducting and those in black are the ones that are off. As can be seen Q2 remains on for the entire half cycle. When Q1 is on, the circuit is in active mode, establishing current flow from V+ to the inductor as in Figure 2-4. Since both Q1 and Q2 are on, the switching node of the inductor is connected to V+. Now, the switches Q3 and Q4 together have to withstand the full bus voltage. To avoid unequal distribution of the bus voltage among these devices (due to unequal device parasitics), Q6 also is kept on so that the central node gets connected to neutral, dividing the voltage equally between Q3 and Q4. When Q1 and Q6 are turned off together during the dead-time between the states shown in Figure 2-4 and Figure 2-5, the inductor current can only flow through the body diode of Q5 and Q2 (which stays on). During the freewheeling mode shown in Figure 2-5, Q5 acts as a synchronous diode, connecting the switching node of the inductor to neutral. Since the switches Q3 and Q4 have only half the bus voltage across them, it is not necessary to keep Q6 on for voltage balancing.

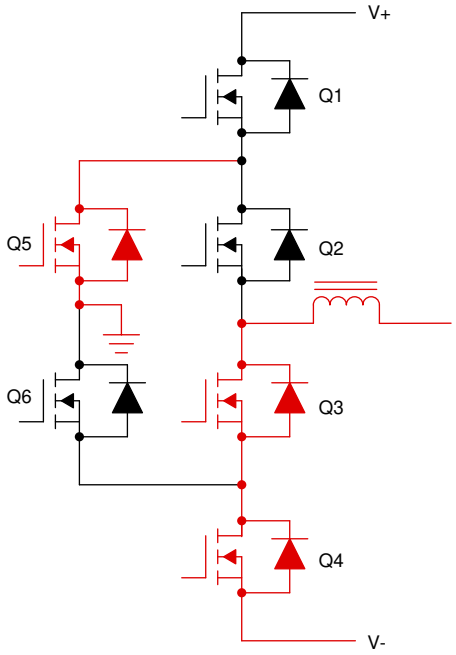


Figure 2-6. Inductor connected to V-

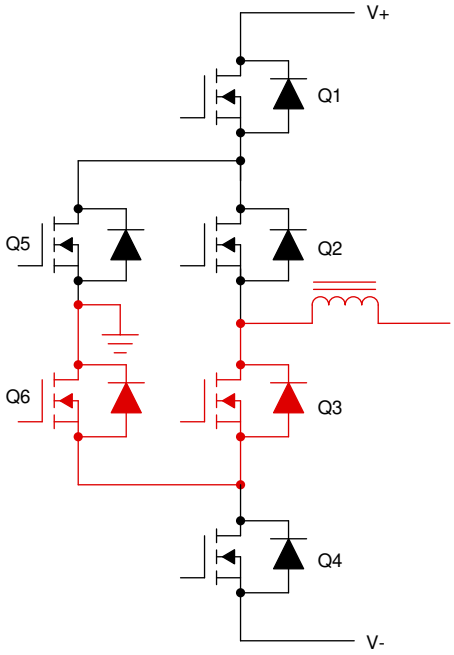


Figure 2-7. Inductor connected to N (-ve)

Similar to the operation during the positive half cycle, Figure 2-6 and Figure 2-7 illustrate the operation of the ANPC power stage during the negative half cycle. Q3 remains on for the entire duration of the negative half cycle.

Figure 2-6 shows the active mode operation in which the inductor gets connected to V- through Q4 and Q3. Similar to the operation during positive half cycle, Q5 also is kept on in this active mode operation to balance the voltage stress between Q1 and Q2. In freewheeling mode shown in Figure 2-7, the inductor current is maintained through Q6 and Q3, connecting the inductor switch node to neutral.

2.2.2 LCL Filter Design

Any system of power transfer with the grid is required to meet certain output specifications for harmonic content. In many rectifiers, a high-order LCL filter typically provides sufficient harmonic attenuation, along with reducing the overall design size versus a simpler filter design. However, due to the higher order nature, take some care in its design to control resonance. Figure 2-8 shows a typical LCL filter.

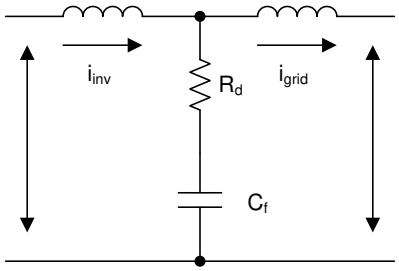


Figure 2-8. LCL Filter Architecture

One of the key benefits of using GaN switching device (as this reference design does) is the ability to increase the switching frequency of the power stage significantly versus traditional Si-based switching devices. This increased switching frequency has a direct impact on the filter resonant design of the converter, which needs to be accounted for. To ensure that the filter is designed correctly around this switching frequency, the known mathematical model of this type of filter is used in this design.

The primary component is the switch side inductor, or L_{inv}, which can be derived using Equation 1:

$$L_{inv} = \frac{V_{DC}}{8 \times f_{SW} \times I_{grid\_rated} \times \%ripple} \quad (1)$$

Using the system specifications, the primary inductor value can be calculated:

$$L_{inv} = \frac{1000\ V}{8 \times 100\ kHz \times 10\ A \times 30\%} = 417\ \mu H \quad (2)$$

An inductor from Wurth Elektronik (750344413) with rated current of 15 A having zero bias inductance of 480 mH is used. With the high current bias during the operation, the inductance can reduce by 25% as per the data sheet. This results in an effective inductance of 360 mH at 15 A, which is sufficient to ensure ripple current below 40%.

The sizing of the primary filter capacitor is handled in a similar fashion using Equation 3:

$$C_f = \frac{\%\chi \times Q_{rated}}{2 \times \pi \times F_{grid} \times V_{grid}^2} \quad (3)$$

Make some design assumptions to finalize the value of C_f , limiting the total reactive power absorbed by the capacitor to 3.5%. Scaling the total system power by the per phase power results in a primary capacitor value of:

$$C_f = \frac{3.5\% \times \frac{6.6\ kW}{3}}{2 \times \pi \times 50\ Hz \times \left(\frac{400\ V}{\sqrt{3}}\right)^2} = 4.59\ \mu F \quad (4)$$

A standard value capacitor of 4.7 µF was selected.

For the remainder of the filter design, determine the values by defining the attenuation factor between the allowable ripple in grid inductor and the inverter inductor. This factor needs to be minimized while still maintaining a stable and cost effective total filter. By assuming an attenuation factor, an r value, which defines the ratio between the two inductors, is determined using Equation 5:

$$I_{att} = \frac{1}{\left|1 + r \times \left[1 - L_{inv} \times C_b \times \left(2 \times \pi \times f_{SW}\right)^2 \times \chi\right]\right|} \times 100 \quad (5)$$

Where C_b is given by:

$$C_b = \frac{C_f}{\chi\%} = \frac{4.7\ \mu F}{3.5\%} = 134\ \mu F \quad (6)$$

To obtain an attenuation factor of 5%, and using the earlier derived values, the value of r can be evaluated by rewriting Equation 5 to be:

$$r = \left| \frac{\frac{1}{5\%} - 1}{1 - 360\ \mu H \times 134\ \mu F \times \left(2 \times \pi \times 100\ kHz\right)^2 \times 3.5\%} \right| = 2.85\% \quad (7)$$

The resultant value for L_{grid} is then:

$$L_{grid} = r \times L_{inv} = 2.85\% \times 360\ \mu H = 10.3\ \mu H \quad (8)$$

A higher standard value of 15 µH was selected to ensure good attenuation.

The filter design can be validated by determining its resonant frequency (F_{res}). A good criteria for ensuring a stable F_{res} is that it is an order of magnitude above the line frequency and less than half the switching frequency. This criteria avoids issues in the upper and lower harmonic spectrums. The resonant frequency of the filter is given by Equation 9:

$$F_{res} = \frac{1}{\frac{\sqrt{\frac{L_{grid} \times L_{inv}}{L_{grid} + L_{inv}} \times C_f}}{2 \times \pi}} \quad (9)$$

Using the derived filter values, the resonant frequency is:

$$F_{res} = \frac{1}{\frac{\sqrt{\frac{15\ \mu H \times 360\ \mu H}{15\ \mu H + 360\ \mu H} \times 4.7\ \mu F}}{2 \times \pi}} = 19.35\ kHz \quad (10)$$

This value for F_{res} meets the criteria listed earlier and validates the filter design.

The remaining value to determine is the passive damping that must be added to avoid oscillation. Generally, a damping resistor at the same relative order of magnitude as the C_f impedance at resonance is suitable. This impedance can be derived using Equation 11:

$$R_d = \frac{1}{6 \times \pi \times F_{res} \times C_f} \quad (11)$$

$$R_d = \frac{1}{6 \times \pi \times 19.35\ kHz \times 4.7 \mu F} = 0.58\ \Omega \quad (12)$$

For the final implementation in hardware, use real values for all of these components based on product availability and must be chosen to be appropriately close (±10% typically). When final values are determined, recalculate the resonant frequency to ensure the filter is still stable.

2.2.3 Power Switching Devices Selection

As shown in the architecture overview, the main switching device needs to support only half the full switching voltage. To support the 800-V DC link voltage of this design, use 600-V rated devices. The switches Q1, Q5, Q4, and Q6 are high-frequency switching and hence must be GaN devices. However, the switches Q2 and Q3 are only switching at 100 Hz and 120 Hz and can use Si MOSFETs.

Conduction loss is mainly determined by the $R_{DS(on)}$ of the GaN MOSFET and the $R_{DS(on)}$ of the Si MOSFET. At any instance, there are two devices conducting at the same time (one each of the GaN device and the Si device). So the $R_{DS(on)}$ of these should be selected based on the conduction loss that can be allowed on them.

Switching loss is a function of the switching frequency and switching energy of each switching element; the switching energy being related to the device current and voltage at the switching transient. Using the switching energy curve in the data sheet, the total switching loss can be estimated. Note that in inverter configuration, only Q1 or Q4 experience switching loss, as Q5 and Q6 work as synchronous switches only and hence experience zero voltage switching. However, since Q5 and Q6 body diodes conduct during dead-time, they can have forward drop loss and reverse recovery loss. However, TI's GaN devices do not have reverse recovery loss at

all and SiC devices have only negligible reverse recovery. Q2 and Q3 switch only at a very low frequency and hence their switching loss can be neglected.

The conduction loss and switching loss can be estimated for all the devices and efficiency can be estimated as explained. With the thermal impedance information of the thermal system design, the proper device rating can be selected. 600-V, 30-mΩ GaN and 650-V, 40-mΩ Si MOSFET are good tradeoffs among thermal, efficiency and cost.

2.2.4 GaN Power Stage

Unlike the Si power boards which are driven by isolated gate drivers as explained in Section 2.2.8, the TI GaN device LMG3422R030 has built-in gate drive. So the power stage needs signal isolation to interface with the MCU. Figure 2-9 shows the GaN power stage. The ISO7741 isolator used to isolate the PWM input has another channel in the reverse direction that can transmit the fault signal back to the MCU side. As this is a negative logic one, an AND gate is used to combine these signals to give a negative logic fault signal back to the MCU if either of these GaN devices generate a fault.

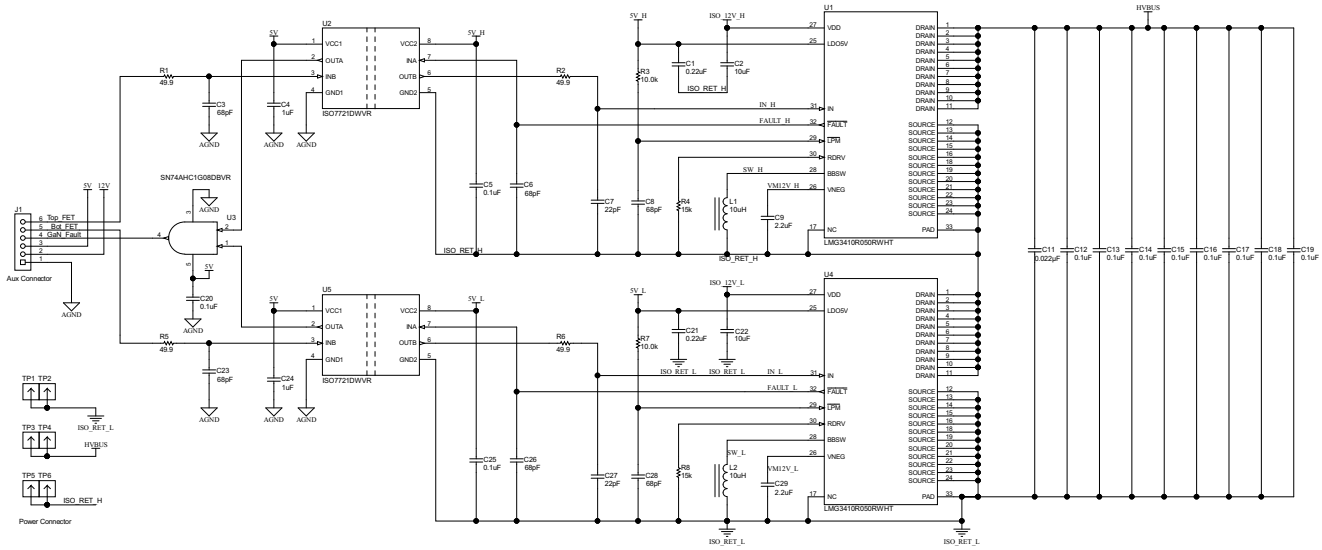


Figure 2-9. GaN Power Stage

2.2.5 Voltage Sensing

Voltage sensing happens at three points in the inverter signal path to aid in control: before and after the primary output relay and at the positive and negative bus voltages. By enabling measurement on both sides of the relay, the control system can lock into the grid voltage and frequency before connecting, thus preventing any mismatch issues. Similarly, sensing of the positive and negative bus voltages help in fine adjusting the duty cycle separately during the positive and negative half cycle to prevent any bus voltage mismatch.

All three sensing topologies are similar. First, PGND is used as a virtual neutral using a resistor network. The high voltage signal is attenuated using a series of large value resistances. An offset of 1.65 V is added to the attenuated neutral point to center the voltage signal in the middle of the input range of the TLV9004, and the attenuated value from the phase voltage is measured using the ADC within the C2000™ MCU. Figure 2-10 shows this sensing arrangement.

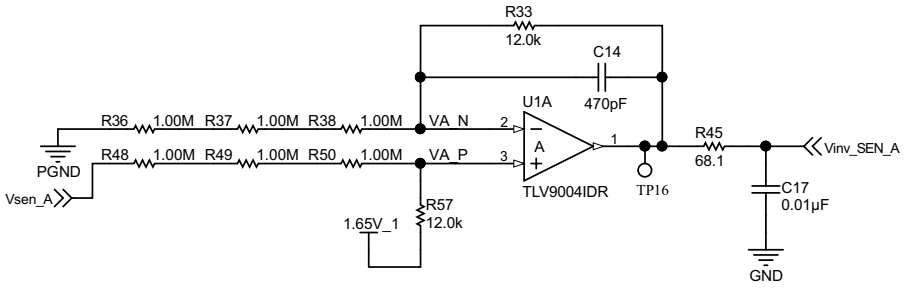


Figure 2-10. High-Voltage Sensing Signal Path

2.2.6 Current Sensing

Critical to getting a closed loop control system is accurate current measurement of the inverter. In this design, current measurement is done to sense the current through the inductor. Because the output is high voltage and the controller needs to remain isolated, the AMC3302 reinforced isolated current sensor is used to measure the resistor voltage drop. To keep system losses low, the AMC3302 has a ±50-mV input range. When compared to other devices with a typical input range of ±250 mV, the total power loss across the shunt is significantly reduced.

Sizing the shunt resistor for this design is a trade-off between sensing accuracy and power dissipation. A 2-mΩ shunt provides a ±50-mV output signal at the inverters approximate ±25-A output but also only generates 0.5 W of heat at full load. When choosing an actual device, select a high accuracy one to eliminate the need to calibrate each sensor path.

The voltage across the shunt resistor is fed into the AMC3302 isolated current sensor with integrated isolated bias power supply, which generates a differential output. This differential output is converted to a single ended output with a 1.65-V offset using an OPA4376 amplifier for measurement using the ADC present on the C2000™ MCU. Figure 2-11 shows the current sensing circuit.

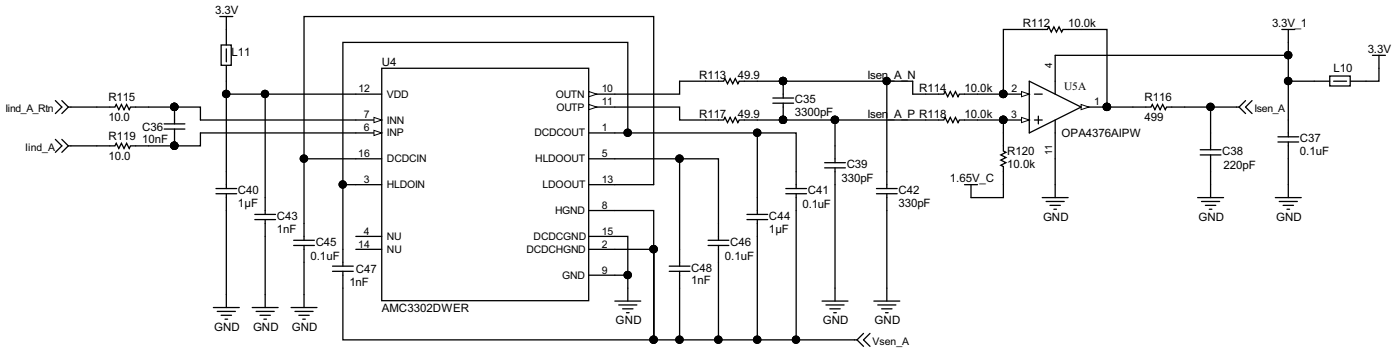


Figure 2-11. Isolated Current Sensing With AMC3302

2.2.7 System Power Supplies

This reference design uses multiple voltage domains across the system:

- A primary bias power input to power the entire design (regulated 12 V). This is used to directly power relays and fans used on the board. There is a connector provision on the main board to generate this 12-V supply directly from the high-voltage DC bus.
- A TPS563200 synchronous buck converter generates 5 V to power the control card and power cards from the 12 V main power. Each of the power cards generate its own isolated power supply for gate driving from this 5-V power supply.
- The 3.3-V supply for analog sensing and logic is generated by an LDO LP5907 from the 5 V.

Figure 2-12 shows the power tree for all of these domains.

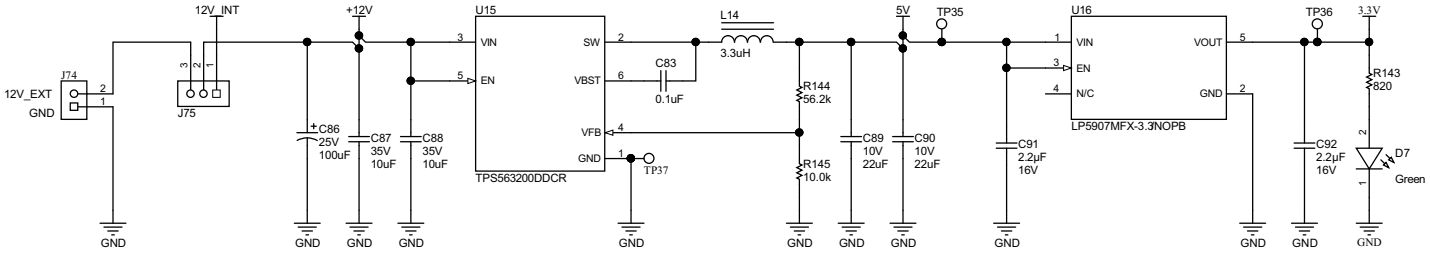


Figure 2-12. Power Tree

2.2.7.1 Isolated Bias Supplies

To generate the isolated bias supplies for each of the power cards, the SN6501 transformer driver is used to drive transformers suited for the power rails required to drive the specific power switching devices used in each type of board As each of the boards have two switching devices, there are two isolated bias power supplies per board.

For the TI GaN device LMG3410R050, a 12-V output is needed. This is generated using the SN6501 transformer driver along with Würth Elektronik 750313638 transformer in a voltage doubler configuration as shown in Figure 2-13.

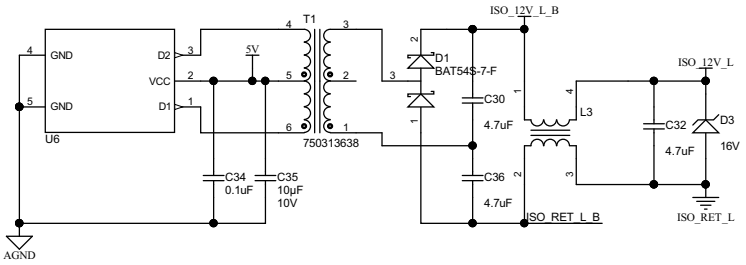


Figure 2-13. SN6501 Bias Voltage Supply for GaN Power Board

For the slow switching Si power board, a +12-V, –5-V drive is used to drive the FCH040N65S3 Si MOSFET. The SN6501 transformer driver along with Würth Elektronik 750342879 transformer in a push-pull configuration is used to generate a 17-V supply. A TL431-based level-shifting circuit converts this to +12-V, –5-V supply. The circuit is shown in Figure 2-14.

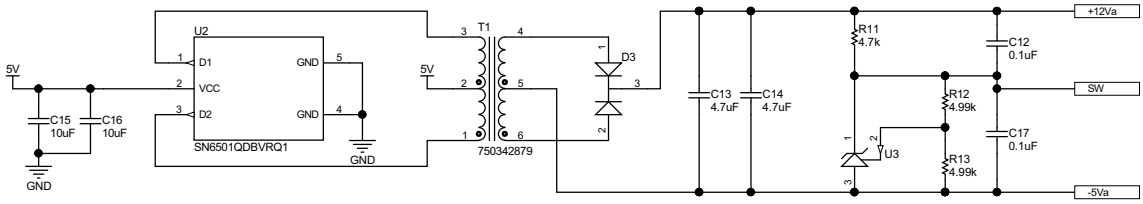


Figure 2-14. SN6501 Bias Voltage Supply for Si Power Board

2.2.8 Si Gate Driver Circuit

Figure 2-15 shows the schematic of the isolated Si MOSFET gate driver. As the UCC21541 gate driver used has two isolated gate drive outputs, it can drive both the devices in the half-bridge power stage of the power board. The drive current is controlled separately for turn-on and turn-off with diode controlled separate drive paths. A ferrite bead is used in the gate drive path to suppress ringing.

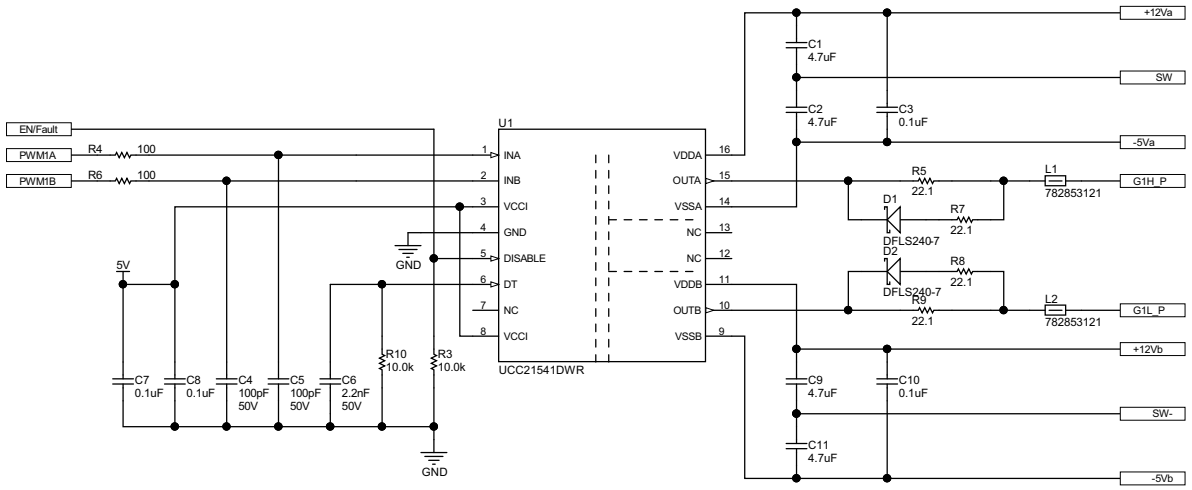


Figure 2-15. UCC21541 Gate Drive Circuit

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware and Software Requirements

3.1.1 Hardware

The DUT in this design is set up and operated in several pieces:

- One TIDA-010210 mother board (TIDA-010210-MB-E2)
  - J75 Header : Jumper between pin 1 and pin 2
  - Change 750344413 with 750343810 (L2, L4, L6)
- Six TIDA-010210 power cards based on GaN (TIDA-010210-GaN-E3)
- Three TIDA-010210 power cards based on Si (TIDA-010210-Si-E2)
- TMDSCNCD280049C Control Card:
  - S2 Switch : Change from the DOWN to the UP position
  - S3 Switch : Changed from the UP to the DOWN position
- Mini USB cable
- Laptop or other computer

The test equipment required to power and evaluate the design is as follows:

- >12-V, 2-A bench style supply for primary board power
- >11-kW AC source
- >11 kW, 800-V DC load
- > 1000-V, 10-A power supply for DC link input
- > 6.6-kW resistive AC load
- Four-channel power quality analyzer

3.1.2 Software

- Code Composer Studio™ 9.3 or later versions with TI C2000 powerSUITE

3.2 Testing TIDA-010210 With AC Resistive Load

In this test condition, the system is configured to operate in an open loop and close-loop control mode, generating a static 50-Hz output. The power demand is then modulated by the resistive bank, together with the MCU, to test the system at multiple load points. This operation allows the user to do preliminary testing before going at high voltage and high power operation.

3.2.1 Test Setup

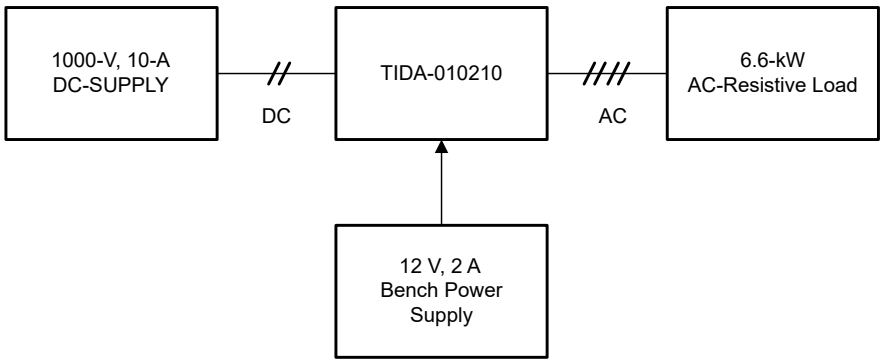


Figure 3-1. Test Setup for Resistive AC Load

To test the functionality of this reference design, use the following equipment:

- One Magna-Power 1000-V, 10-A power supply to provide CV/CC adjustable input to the DUT
- A 6.6-kW KWE load bank is used as a configurable load to test the design at various set points.
- An oscilloscope
- An external bench power supply is used to provide a 12-V input to power the DUT

3.2.2 Experimental Results

The open loop test output waveforms in Figure 3-2 show clean sinusoidal waveforms with the new PWM scheme, when DC bus is operating at 800 V. There is very little distortion even at zero crossing with CLB based protection active.

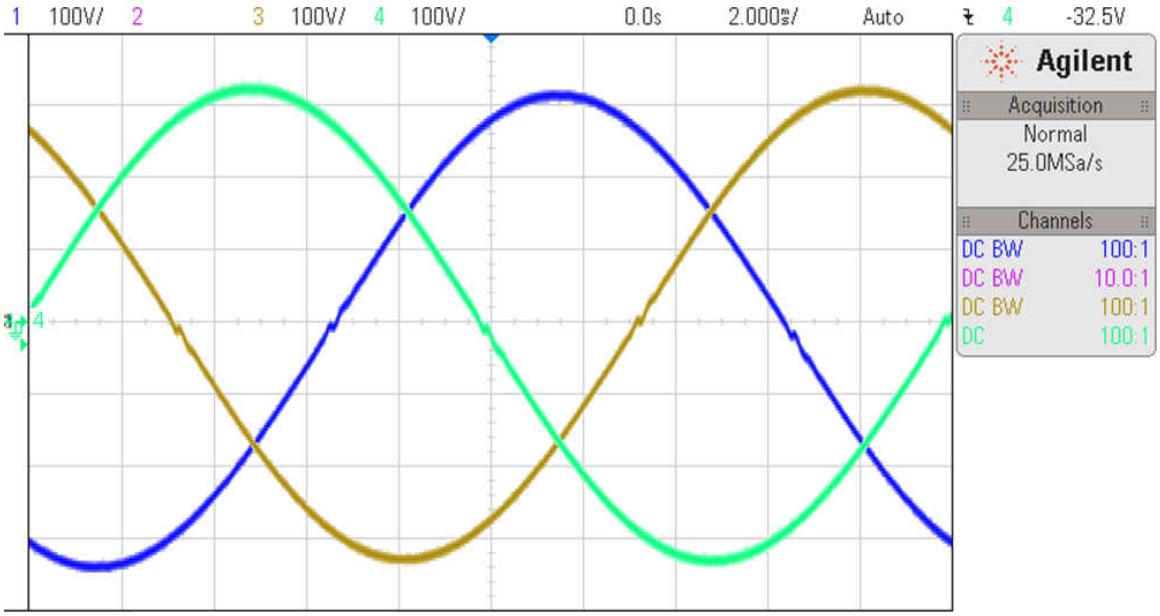


Figure 3-2. Open Loop Output Waveforms (AC Load Voltage Waveforms)

The current loop stability of the circuit is demonstrated by the smooth transition in the current transient response. Figure 3-3 shows the response when current is changed from 1 A to 6 A and Figure 3-4 shows the response when current is changed from 6 A to 1 A.

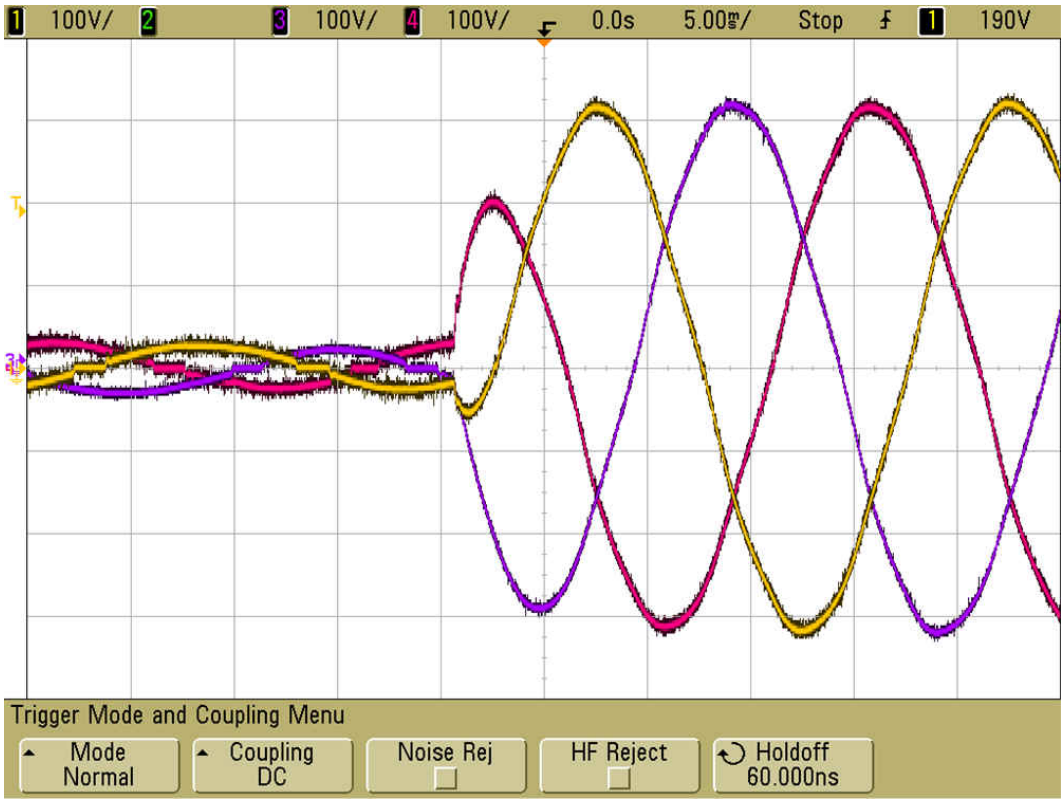


Figure 3-3. Positive-Going Transient Response (AC Load Voltage Waveforms)

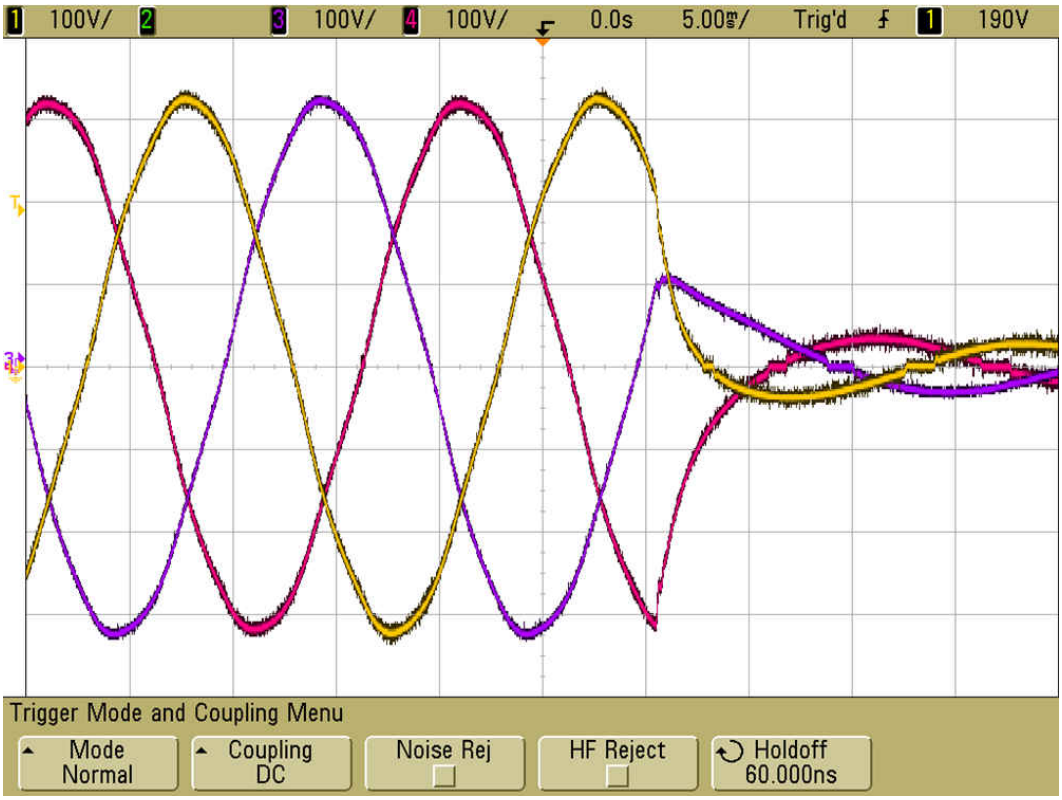


Figure 3-4. Negative-Going Transient Response (AC Load Voltage Waveforms)

3.3 Testing TIDA-010210 in PFC Operation

In this test condition, the system is configured to operate in an close-loop control mode. The TIDA-10210 design is implementing a current control loop able to synchronize with the emulated grid voltages of the AC source. On the DC link, the DC load is controlling directly the voltage, thus allowing the user to control the converter power by changing the reference current of the d sequence. In this operating condition, efficiency versus power has been measured.

3.3.1 Test Setup

To test the efficiency of this reference design, use the following equipment:

- A 12-kW DC load able to regulate the load voltage from 50 V to 850 V
- A 12-kVA AC supply able to regulate the voltage from 25 to 250 V
- An AC power analyzer is connected to the DUT input and output to perform efficiency measurements
- An external bench power supply is used to provide a 12-V input to power the DUT

Figure 3-5 shows the test setup for PFC operation.

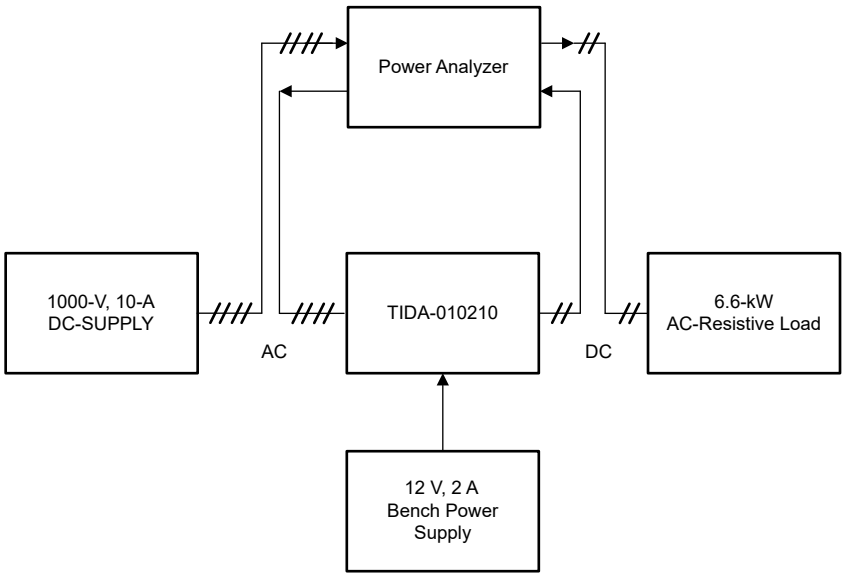


Figure 3-5. Test Setup for PFC Operation

3.3.2 Experimental Results

Close loop test output waveforms in Figure 3-6 show clean sinusoidal waveforms at the nominal load. During the experiments, no important zero crossing distortion was observed in the currents. Total harmonic distortion less than 4% was measured.

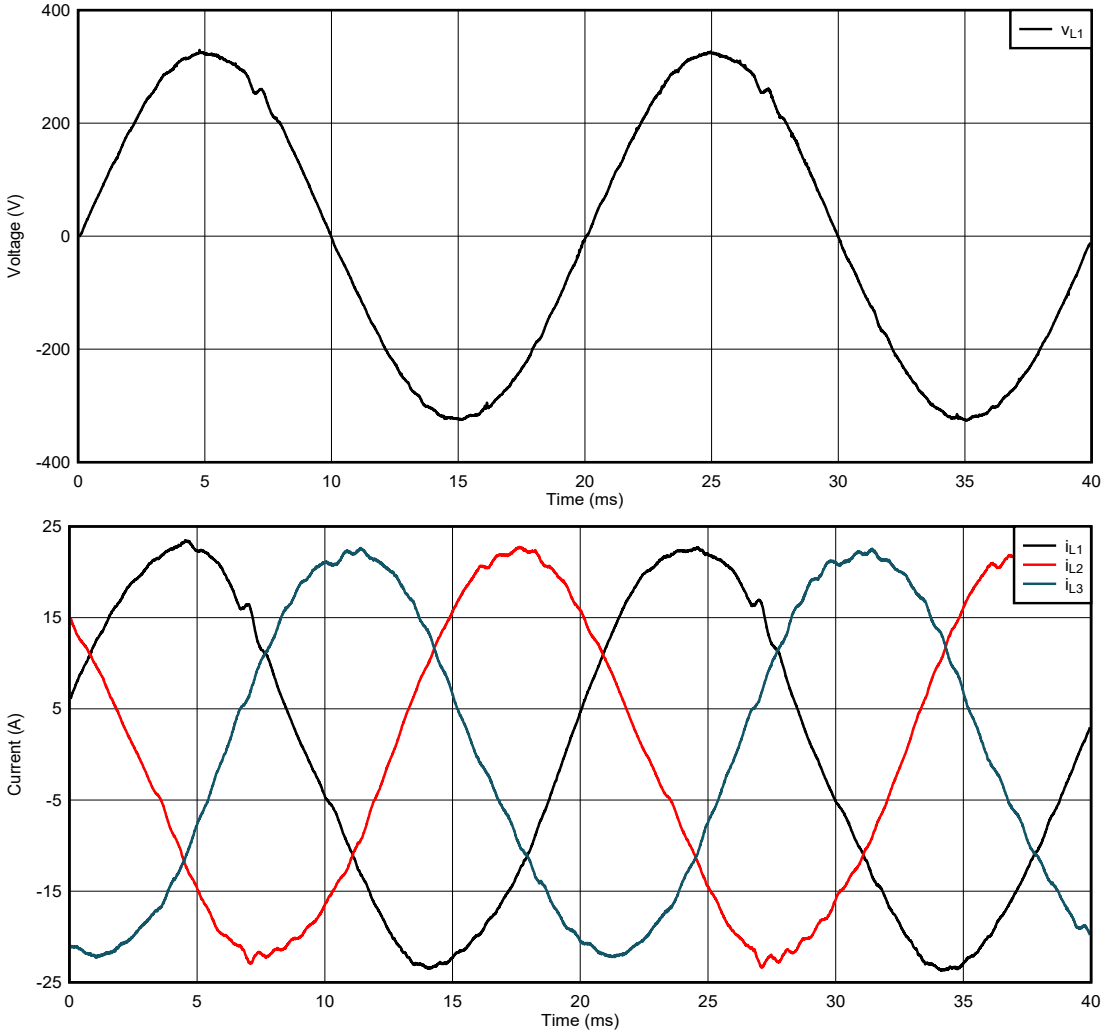


Figure 3-6. Currents and Voltage Working at 11-kVA PFC full

Table 3-1 and Table 3-2 collect the efficiencies of the PFC at 230 V_{RMS}, respectively for two different DC bus voltages: 600 V and 800 V. The results obtained from the power analyzer are taken from 2 kW to 11 kW. In most of all the operating points, the power efficiency is higher than 98% by reaching a maximum of 98.62%.

Table 3-1. System Efficiency With GaN LMG3422R030 at 600-V DC

DC BUS VOLTAGE (V)	AC GRID CURRENT (A)	INPUT POWER (W)	OUTPUT POWER (W)	EFFICIENCY
605.3	3	2045.7	1980.2	96.8
605.34	5.22	3559.5	3506.1	98.5
605.38	7	4773.3	4707.4	98.62
605.2	8.9	6068.9	5978.5	98.51
605.28	10.9	7432.7	7309.3	98.34
605.34	13.05	8898.8	8731.5	98.12
605.5	15.2	10364.9	10148.3	97.91
605.8	16.5	11251.4	11006.1	97.82

Table 3-2. System Efficiency With GaN LMG3422R030 at 800-V DC

DC BUS VOLTAGE (V)	AC GRID CURRENT (A)	INPUT POWER (W)	OUTPUT POWER (W)	EFFICIENCY
803.4	3.02	2070	1976.8	95.5
801.4	5.24	3601.8	3511.8	97.5
802.4	7.01	4830	4747.9	98.3
803.4	8.95	6141	6042.7	98.4
803.5	10.93	7521	7408.2	98.5
802.8	12.98	8970	8826.5	98.4
803.8	15.21	10488	10304.5	98.25
803.1	16.52	11385	11180.1	98.2

All the data summarized in the tables have been collected and plotted as shown in Figure 3-7. At low power it is better to keep the PFC to work at lower DC bus voltage. Conversely, at a higher current keeping higher DC bus voltage leads an important efficiency improvement of 0.4%.

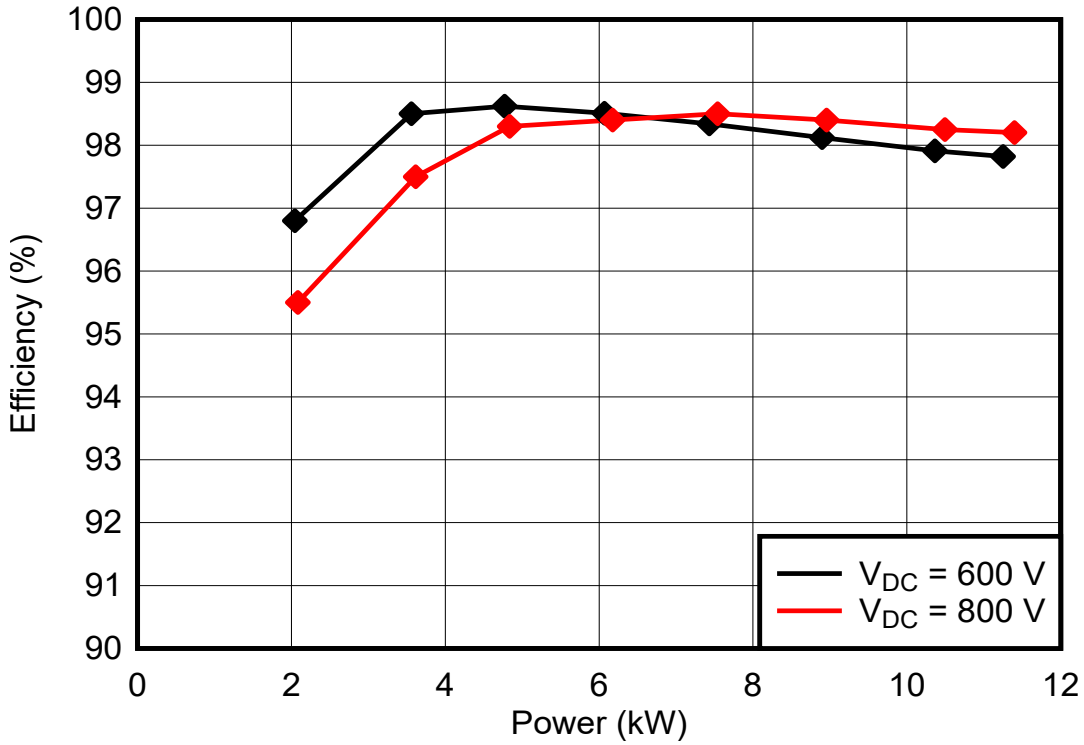


Figure 3-7. PFC Efficiency vs Input Power

The final design dimensions are outlined in Table 3-3 and show a total volume of 4.3 L. With a power rating of 11 kW, this results in a power density of 2.57 kW/L.

Table 3-3. TIDA-010210 Dimensions

AXIS	DIMENSION
X	300 mm
Y	220 mm
Z	65 mm
Volume	4.29 liters

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010210.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010210.

4.1.3 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010210.

4.1.4 Gerber Files

To download the Gerber files, see the design files at TIDA-010210.

4.1.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010210.

4.2 Tools and Software

Tools

Concise Description	TMDSCNCD280049C is an HSEC180 controlCARD based evaluation and development tool for the C2000™ *F28004x series* of microcontroller products. controlCARDs are ideal to use for initial evaluation and system prototyping. controlCARDs are complete board-level modules that utilize one of two standard form factors (100-pin DIMM or 180-pin HSEC) to provide a low-profile single-board controller solution. For first evaluation controlCARDs are typically purchased bundled with the *TMDSHSECDOCK* baseboard or bundled in an application kit.

Software

Concise Description	To download the software, see the software files at TIDA-010210.

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2021) to Revision A (March 2022)	Page
• The TIDA-010210 is upgraded to run at 11 kW. Changes in revision A of this design guide support this upgrade	1

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