Design Guide: TIDEP-01022

Automotive and IoT Gateway Reference Design Based on the Jacinto DRA821 Processor

Description

This reference design is an optimized system design for automotive gateways in newly emerging architectures—including domain, central and zonal gateway architectures—and is based on the Jacinto™ DRA821 processor family. DRA821 processors are tailor-made for gateway systems with cloud connectivity.

Created as an 8-layer PCB design with optimized power architecture and a variety of connectivity options, including Ethernet switch, CAN-FD, and PCIe, the design accommodates a wide range of automotive and industrial applications.

Resources

TIDEP-01022	Design Folder
DRA821	Product Folder
DP83TG720S-Q1, TCAN1046-Q1	Product Folder
TLIN1022-Q1, TPS6594-Q1	Product Folder
LM5141, TPS22965	Product Folder
TPS61088, TPS62810-Q1	Product Folder

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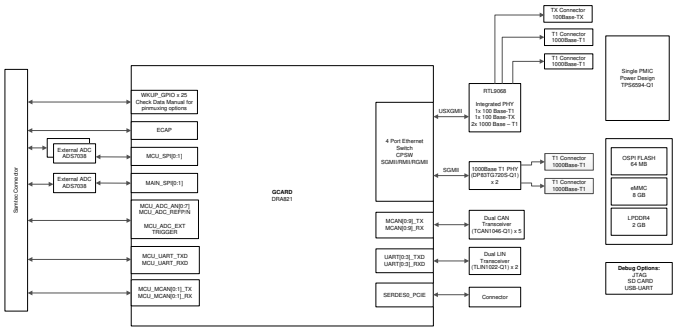
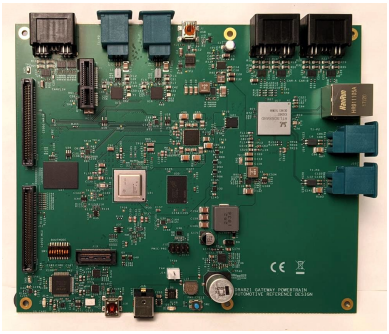
Features

- Integrated Ethernet switch and external Ethernet switch with automotive connectors
- Multi CAN/LIN array with wakeup functionality
- PCIe Connector
- Optimized power management via TPS6594x solution
- Early CAN response and fast system boot
- Standby IO domain support
- 2666 MT/s LPDDR4
- OPSI and eMMC flash memory support
- Gateway application stack (AutoSAR)

Applications

- Automotive Gateway
- ADAS Domain Controller





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1 System Description

Automotive architectures are evolving to meet the demands of the future requiring an ever-increasing amount of data. There are 3 types of gateways in the new vehicle architectures: centralized, domain, and zone. The centralized gateway safely and securely moves data between numerous domains of the vehicle including powertrain, chassis, body, ADAS, and so on. The domain controller consolidates ECUs in the functional domain, safely and securely facilitates data movement between the remaining ECUs within a functional domain and to the centralized gateway. Zonal gateways are similar to domain gateways but are physically located to aggregate IO in a specific area of the vehicle.

This reference design is an easy-to-use, detailed DRA821-based reference design for use as a centralized gateway, domain controller, or zonal controller. The DRA821 is a high performance heterogeneous SoC that integrates legacy automotive connectivity (LIN and CAN) with high speed interfaces such as PCIe, USB, a 4-port Gigabit Ethernet switch, safety and security features. The DRA821's high integration lowers overall system BOM and enables its use in a wide variety of gateway use cases. More information on peripherals, safety, and security features can be found in the Jacinto™ DRA821 Automotive Processors data sheet.

This reference design is based on a single PMIC (TPS6594x) power architecture with on board OSPI, eMMC, and LPDDR4 memory, as well as debug functionality. The board has hardware connectors that showcase and support a diverse set of communication protocols including five Ethernet ports, 10 CAN-FD ports, four LIN ports, and a PCIE connector. Headers have also been included for easy access to serial protocols such as SPI, UART, GPIOS, and I^2C.

This reference design serves as a starting point for OEMs and Tier1 to easily and quickly create a fully functional DRA821 solution in the automotive space. Leveraging this design can substantially decrease development costs and time to market.

2 Key System Specifications

Table 2-1. Key System Specifications

PARAMETER	SPECIFICATIONS
SoC	DRA821 SoC
Power	• 12 V • Single PMIC Solution
Auto Connectivity	• CAN • LIN
High-Speed Connectivity	• Integrated 4-port Gigabig Ethernet Switch • External Realtek Ethernet Switch • PCIe Connector
Serial Protocols	• SPI • I2C • GPIO • ADC • UART
Memory	• 2 GB of LPDDR4 at 2666 MT/s • 8 GB eMMC • 64 MB OSPI
Wakeup	GPIO Retention Mode through CAN, LIN,< GPIO Events
Debug	• JTAG • USB over UART • SD CARD

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3 System Overview

3.1 Block Diagram

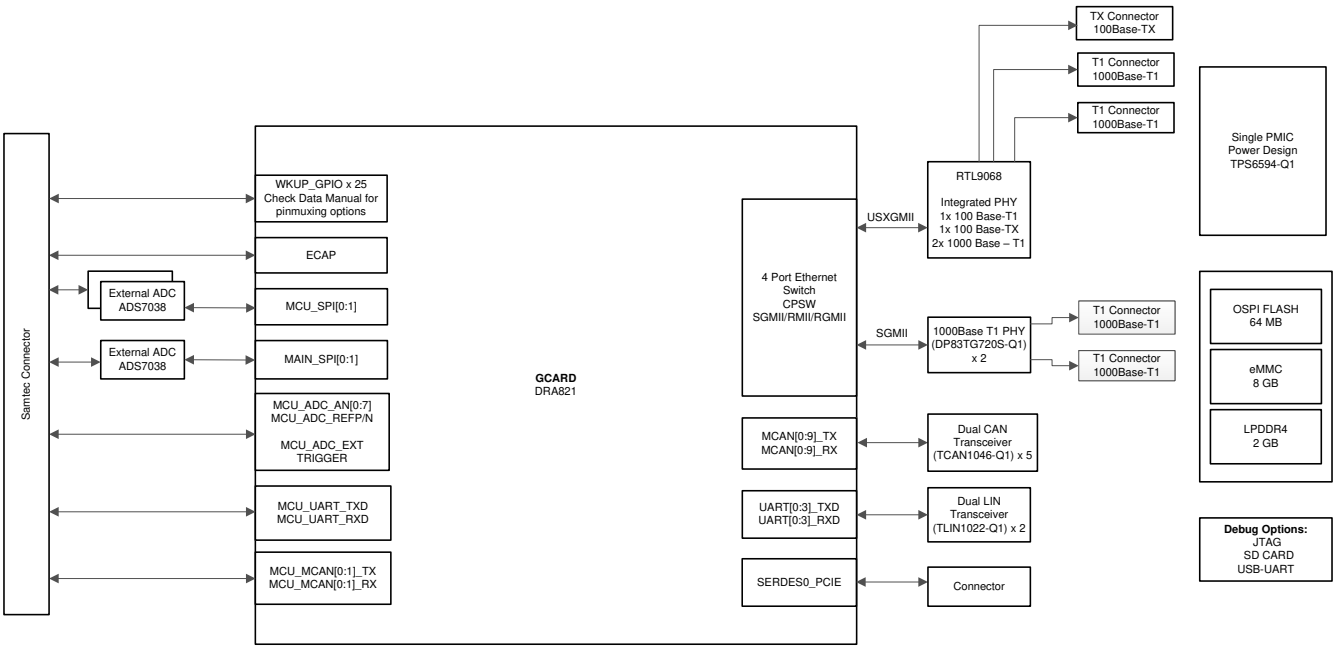

Figure 3-1. TIDEP-01022 Block Diagram

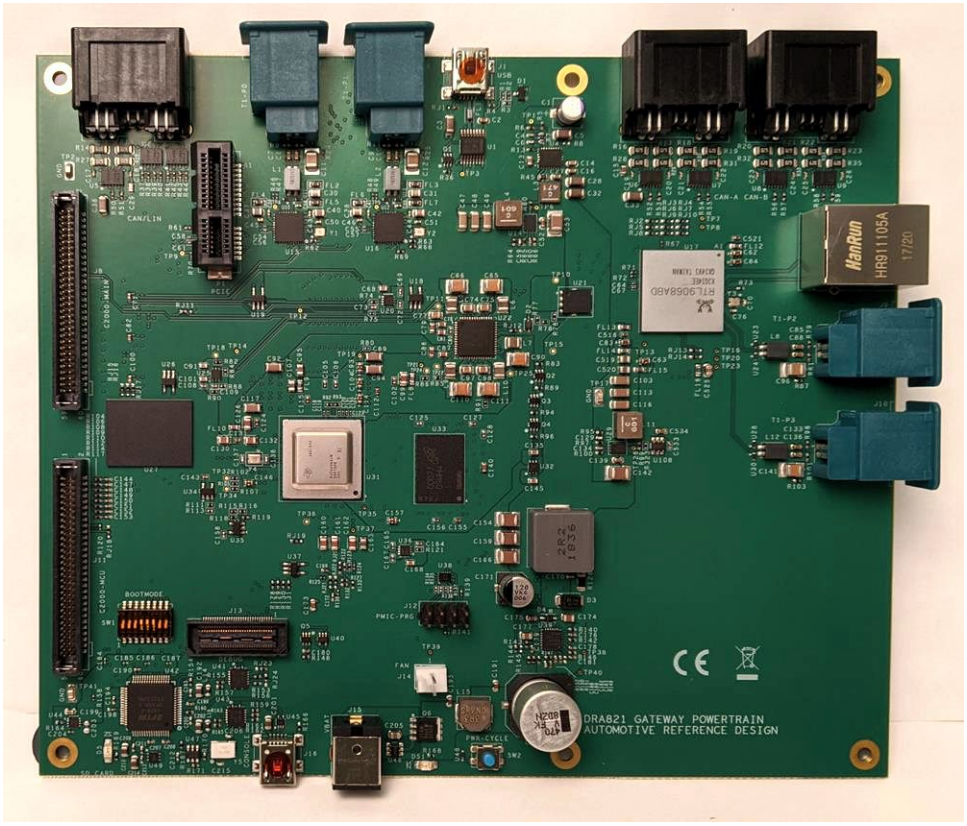

Figure 3-2. TIDEP-01022 Board

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3.2 Design Considerations

- Showcase DRA821 SoC features targeted at gateway applications
- Demonstrate optimized system reference design
- – 8-layer PCB design
  – Optimized power architecture
  – Integrated Ethernet switch and multi-CAN support
  – IO standby support
- Minimize total system BOM

Power Considerations

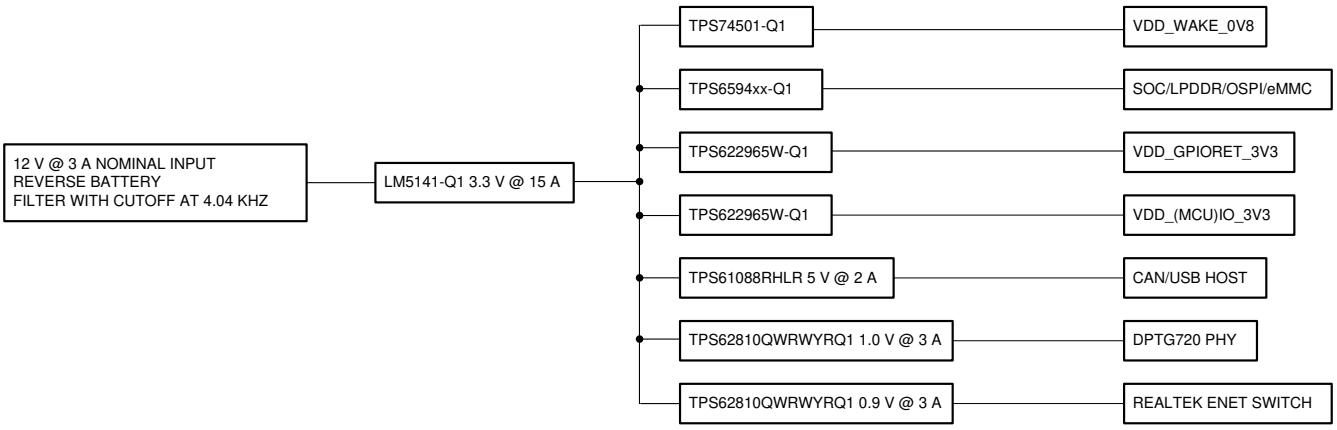

Figure 3-3. Power Tree Design

3.3 Highlighted Products

Processor

The reference design is based on the DRA821 SoC which is heterogeneous automotive processor with dual ARM Cortex-A72 cores and four ARM R5Fs to support a variety of processing and real-time applications. The DRA821 also has an integrated 4-port Ethernet switch, 20 CAN-FD interfaces, PCIe, an integrated HSM, and up to ASIL-D systematic capability to ensure safe and secure data communication of high bandwidth data in gateway applications.

Power Supply

The reference design is based off of a single TPS6594x PMIC. The power topology is based off a 12V input to the PMIC in conjunction with several discrete bucks. The TPS6594x-Q1 is a PMIC that integrates optimized power management, ASIL-D features, and wakeup functionality into a chip.

Ethernet

[Integrated Switch]

Two 1000Base automotive connectors are connected to the DRA821 integrated 4-port gigabit Ethernet switch ports via SGMII. The integrated switch supports a diverse set of interfaces including one 2.5 GB XFI or SGMII, up to four 1 Gb SGMII, up to four RMII (10/100) or RGMII (10/100/1000), and one 5GB QSGMII. Time synchronization functions to support IEEE 1588 (annex D,E,F) are also integrated for TSN/AVB support.

[External Switch]

The RealTek RTL9068 switch is connected to the DRA821 integrated gigabyte Ethernet switch through USXGMII (up to 5Gbps). An RJ45 100Base connector, and two 1000Base automotive connectors are sourced from the RTL9068.

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CAN

There are five TCAN1046 devices on the board to support a total of 10 CAN connections. The TCAN1046 is a dual-CAN transceiver that supports both classical CAN and CAN-FD bus networks up to 8 Mbps.

LIN

There are two TLIN1022 devices on the board to support a total of four LIN connections. The TLIN1022-Q1 is a Dual Local Interconnect Network (LIN) physical layer transceiver with integrated wake-up and protection features (up to 12V), complaint up to LIN 2.2A standards.

Wakeup Functionality

Wakeup functionality can be achieved via any of the CAN, LIN, of GPIO inputs – which are on their own I/O standby domain enabling power savings and wakeup synergy.

Memory

The reference design uses a single MT53D512M32D2DS Micron memory banks for a total of 2 GB of onboard LPDDR4 memory running at 2666 MT/s. Micron's MTFC8GAMALNA provides 8 GB of on-board NAND flash, connected to DRA821's eMMC interface. To support fast booting over OSPI, the board uses Cypress's S28HS512T for 64 MB of NOR Flash.

Connector

The board contains several extra headers enabling access to GPIO, SPI, I2C, ADC and ECAP. There are also dedicated CAN transceivers, LIN transceivers, and automotive Ethernet connectors on board. A standard PCIe connector supports high bandwidth communication. Due to pin muxing limitations, if SGMII and QSGMII are used the PCIe connector will operate via 1–Lane at Gen 2 speeds. If the SGMII or QSGMII ports are not used, then 2-Lane at Gen 3 speed entitlement can be obtained. More information can be obtained by looking at SERDES pin muxing documentation. Refer to 4-L Serializer/Deserializer (SERDES) section of the technical reference manual

Debug

JTAG, SD Card, and USB-UART over mini USB A/B connectors are available for debug ports.

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4 Hardware, Software, Testing Requirements, and Test Results

Software is developed for demo and reference purposes and is not currently integrated into the support SDK. Resources are provided below on basic hardware setup and software references.

4.1 Hardware Requirements

The board requires a 12V DC power supply to power up via the standard 2.5mm EVM power connector.

4.2 Software Requirements

Gateway POC

- Connected Apps (Cloud demonstration via Ethernet)
- Multi-CAN, Ethernet
- Boot KPIs, safety
  - Support fast CAN response
    - <50ms HS
    - <70ms HS+BIST
  - Fast Linux boot to prompt: < 1 s
- Optimized gateway function on MAIN R5Fs

4.3 Test Setup

Diagnostic tests were run on board after power up (12 V DC power brick) with no external components attached to connectors.

4.4 Test Results

Preliminary toggle on and off tests were conducted successfully on several peripherals during initial board bring up.

PERIPHERAL	TEST RESULTS
Main R5	PASS
A72	PASS
Linux Boot	PASS
CCS JTAG	PASS
MCU UART Console	PASS
Main UART Console	PASS
DDR @ 2666MT/s	PASS
EMMC	PASS
SD Card	PASS
LIN	PASS
SPI	PASS
MCAN	PASS
GPIO	PASS
Oscillators	PASS
Essential Power Supplies	PASS
USB2.0 Enumerate	PASS

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5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at .

5.1.2 BOM

To download the bill of materials (BOM), see the design files at .

5.1.3 PCB Layout Prints

To download the layer plots, see the design files at .

5.1.4 Gerber Files

To download the gerber files, see the design files at .

5.1.5 Assembly Drawings

To download the assembly drawings, see the design files at .

5.2 Documentation Support

1. Texas Instruments, *Jacinto™ DRA821 Processors Technical Reference Manual*
2. Texas Instruments, *Jacinto™ DRA821 Automotive Processors Data Sheet*

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.4 Trademarks

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2020) to Revision A (December 2020)	Page
• Updated *3200 MT/s LPDDR4* to *2666 MT/s LPDDR4*	1

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