Design Guide: TIDA-050043
Integrated Power Supply Reference Design for NXP i.MX 6ULL

Description

This reference design is a fully functional development board powering an NXP™ i.MX 6ULL application processor from a TPS6521815 PMIC. The hardware design consists of DDR3L SDRAM (512 MB), 32-MB Serial NOR Flash, 8-GB eMMC 5.0 iNAND, SD Card interface v3.0, dual-channel 100Base-T Ethernet, 5-channel USB hub with Type-A ports, micro-AB USB OTG, mountable LCD screen, and expansion connector for additional inputs and outputs. This design is intended to be used as a reference for data concentrator projects in grid communications or for any project using the i.MX 6ULL, i.MX 6ULZ, or i.MX 6UltraLite processor that requires evaluation of alternative power solutions.

Resources

TIDA-050043	Design Folder
TPS6521815	Product Folder
TPS22964C	Product Folder
TPS2054B	Product Folder
INA3221	Product Folder
DP83849I	Product Folder

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Features

- Full system-on-board for rapid development of NXP i.MX 6ULL, i.MX6 ULZ, and i.MX 6UltraLite systems
- Low-power modes and DVFS supported
- Ethernet, USB wired connectivity
- LCD display included for real-time current monitoring
- Selectable boot options (SD, eMMC, QSPI)

Applications

- Data Concentrators
- Electricity Meter
- HVAC Gateway
- ARM-based SoM-CoM
- Panel PLC (HMI)

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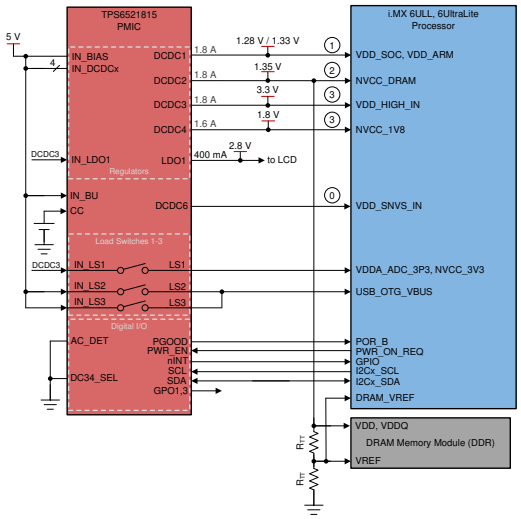
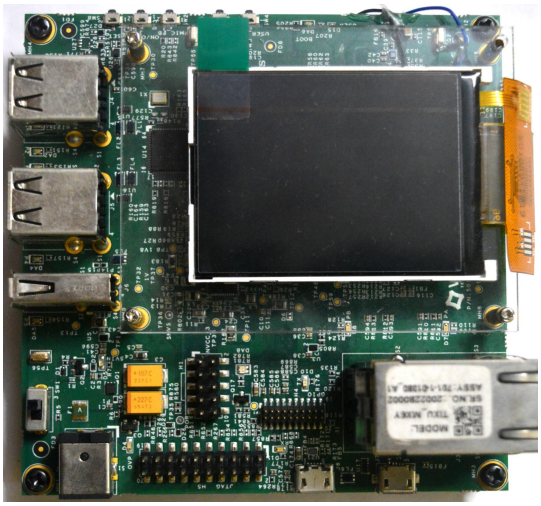




1 System Description

TIDA-050043 is first-and-foremost a reference design for powering the NXP i.MX 6ULL processor from the TPS6521815 PMIC. To show that the PMIC can power the processor, it made the most sense to build a data concentrator design that can also be used as a full evaluation kit (EVK) board with a variety of peripheral devices to assist with development of various end equipments. As a result, there are a variety of wired connections available, as well as multiple BOOT options. The end result of adding all the peripherals, especially a 5-port USB hub, is that some external load switches have been added to provide more voltage rails to deliver 5-V USB from the input to the USB hub. Finally, to ensure the entire board is operational, we developed and tested software using the open-source embedded Linux Yocto SDK to get started working with this design.

1.1 Key System Specifications

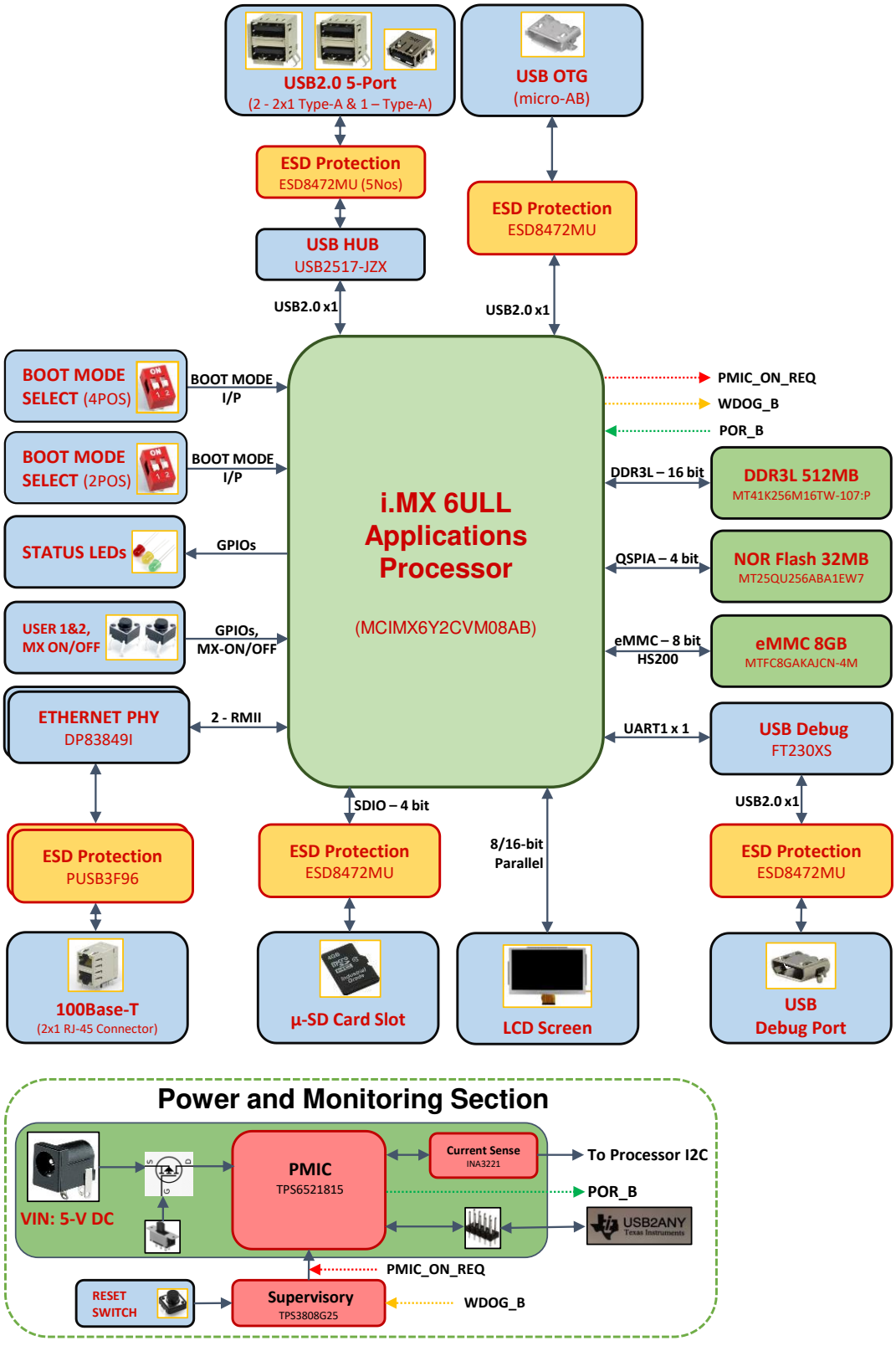
Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Processor	i.MX 6ULL, ARM Cortex-A7 Applications Processor, MCIMX6Y2CVM08AB	Section 2.2.1
PMIC	TPS6521815 user-programmable PMIC with automatic sequencing and DVFS	Section 2.3.1
Memory	4-Gb DDR3L (512 MB), 256-Mb QSPI NOR-Flash (32 MB), 8GB eMMC 5.0, SD v3.0 interface	Section 2.2.2
Ethernet	Dual-port ethernet interface - TI DP83849I PHY and 0845-2R1T-E4 RJ45 jack from Bel Fuse	Section 2.3.2
Debug method (USB-to-UART)	FTDI FT230X is required to implement USB to serial UART conversion	Section 2.2.3
USB ports	5x USB Type-A ports (USB2517I-JZX hub IC) and 1x micro-AB port for USB OTG (Amphenol 10104111-0001LF)	Section 2.2.4
LCD display	RGB TFT 40-pin connector (Molex 54132-4062) for LCD display (Newhaven Display NHD-2.4-240320CF-CTXI#-F), compatible with touch-screen controller (TI TSC2046IPWR)	Section 2.2.5
JTAG header	JTAG connection to i.MX 6ULL processor with 50-mil pitch, 10-pin header	Section 2.2.6
USB2ANY header	Debug method for PMIC separate from processor I^2C bus. Provided by USB2ANY (standard 100-mil pitch, 10-pin header)	Section 2.2.7
Current monitoring	2x TI INA3221 devices are used to monitor current through 6 rails in the system	Section 2.3.3
Operation with Coin Cell	Coin cell for i.MX 6ULL SNVS input. Using DCDC6 of TPS6521815 PMIC, system always powers SNVS before full power-up sequence begins.	Section 2.3.4
Tactile inputs, visual feedback	Push-buttons and status LEDs connected to GPIOs of the processor to assist with debugging software	Section 2.2.8

2 System Overview

2.1 Block Diagram

Figure 1. TIDA-050043 Block Diagram



2.2 Design Considerations

This design is intended to show the ability of the TPS6521815 PMIC to provide power to the i.MX 6ULL processor and all of the peripheral ICs in a variety of designs. To verify this, we had to populate all of these other ICs on the design, starting with the processor. All other devices necessary to build an operational data concentrator or general-purpose evaluation kit are included in this section. The PMIC and other TI devices used in this design are described in Section 2.3.

2.2.1 Processor – i.MX 6ULL Applications Processor

The main component of this design is the NXP i.MX 6ULL processor. It is a single-core Arm® Cortex®-A7 16-bit processor. Dynamic voltage and frequency scaling (DVFS) is a highlight of the processor, wherein the processor can change the core voltage with respect to the processing power required. The multimedia performance of the processor is enhanced by a multilevel cache system, an ARM NEON media processor engine (MPE) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, an electrophoretic display (EPD) controller, and a pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending and rotation. DDR3L, eMMC, SD, QSPI, UART, and I^2C are the processor interfaces we are using in this design.

DESCRIPTION	MFG.	PART NUMBER
iMX6ULL, ARM Cortex-A7 Application Processor, 792MHz, MAPBGA-289	NXP	MCIMX6Y2CVM08AB

2.2.2 i.MX 6ULL Memory Interfaces

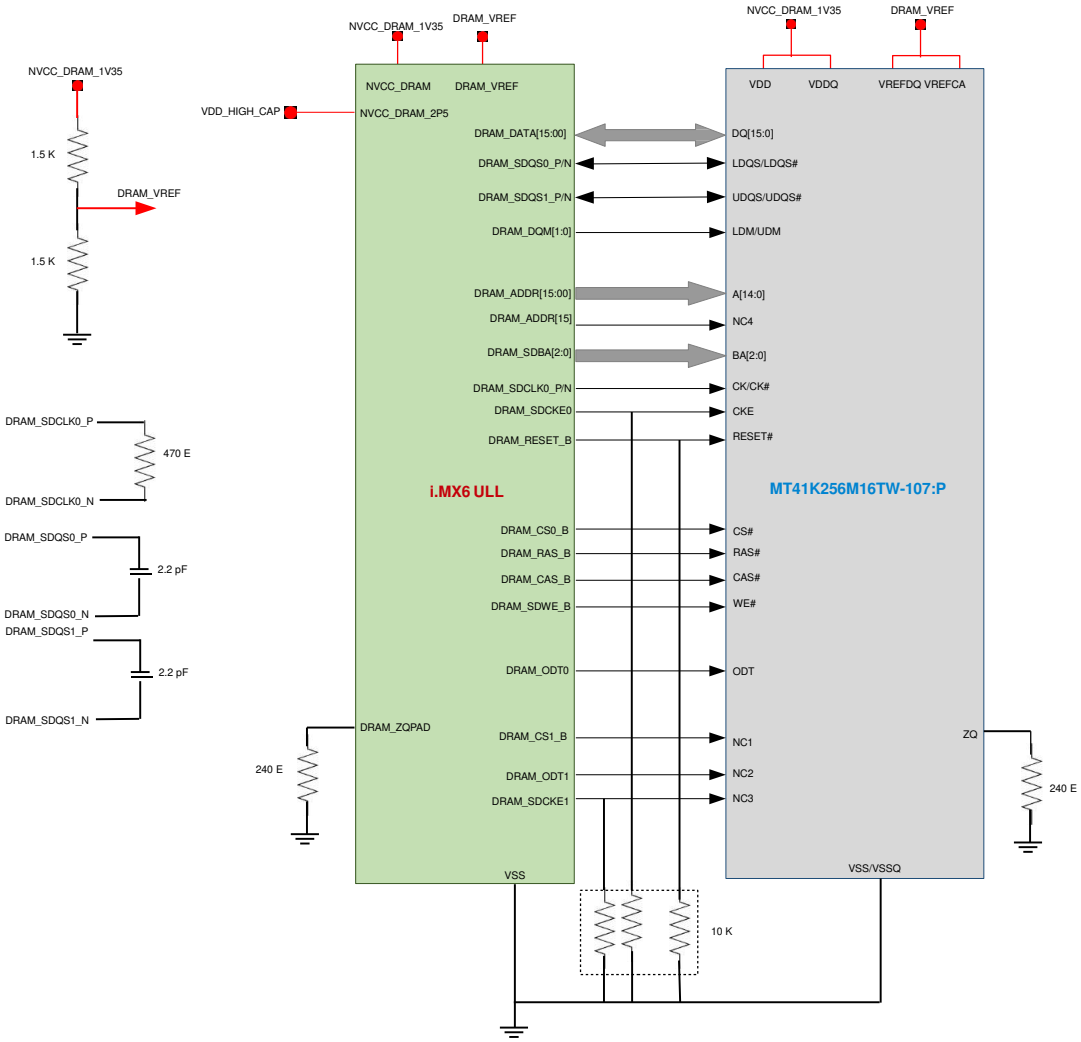
This project makes use of i.MX 6ULL processor's four different external memory interfaces using 4-Gb DDR3L (512 MB), 256-Mb QSPI NOR-Flash (32 MB), 8-GB eMMC 5.0, and SD v3.0.

2.2.2.1 DDR3L

i.MX 6ULL has a dedicated DDR memory controller which supports 16-bit LP-DDR2-800, DDR3-800, and DDR3L-800, all of which can operate up to 800 MT/s data rate. This design is provided with single 4-Gb x16 (512 MB) DDR3L memory. Micron's MT41K256M16TW-107:P is a 4-Gb DDR3L SDRAM used in this design. The memory interface comprises of single channel of 16-bit data signals, along with command and address signals. The DDR interface is shown in Figure 2.

DESCRIPTION	MFG.	PART NUMBER
IC, DDR3L SDRAM, 512MB, x16bit, 1866 MT/s, FBGA-96	Micron	MT41K256M16TW-107:P

Figure 2. DDR3L Interface

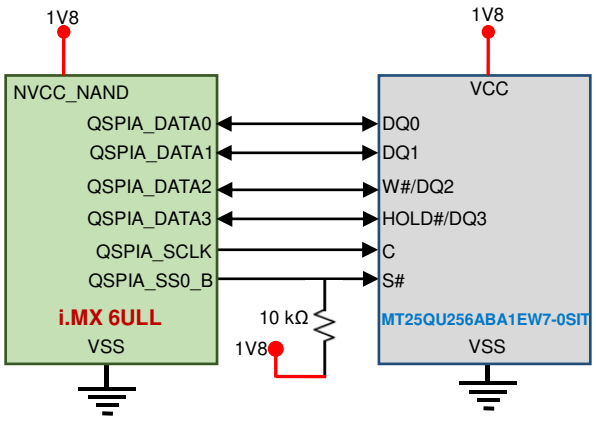


2.2.2.2 Quad SPI NOR Flash

The i.MX 6ULL processor has a Serial NOR Flash interface (QSPI). This design uses Micron's MT25QU256ABA1EW7-0SIT Serial NOR Flash memory with a density of 256 Mb (32 MB) supports a clock frequency of 166 MHz for data through-put up to 90 MBps at DTR with an operating voltage of 1.7 V to 2.0 V, and the interface diagram of this Flash IC with the processor is shown in Figure 3.

DESCRIPTION	MFG.	PART NUMBER
IC, NOR Flash, 32MB, 133MHz, SPI, 1.7-2V, W-PDFN-8	Micron	MT25QU256ABA1EW7-0SIT

Figure 3. QSPI NOR Flash Interface

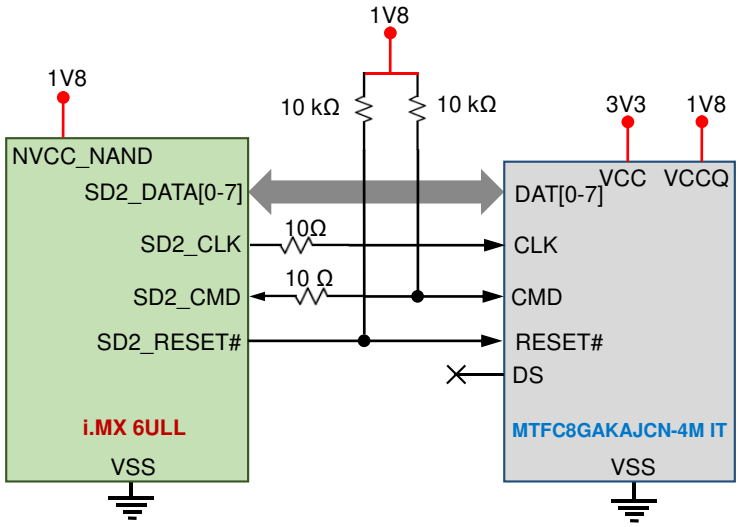


2.2.2.3 eMMC iNAND

The i.MX 6ULL processor supports eMMC versions 4.4, 4.41, and 4.5. This design uses Micron's 8-GB MTFC8GAKAJCN-4M IT, an eMMC version 5.0 memory device. The eMMC version 5.0 specification indicates is backwards compatibility, allowing it to work correctly with the processor. The data transfer speed used is HS200 mode with 1.8-V I/O voltage. The interface diagram of eMMC with the processor is shown in Figure 4.

DESCRIPTION	MFG.	PART NUMBER
IC, eMMC 5.0, 8GB, x8bit, 52MHz, VFBGA-153	Micron	MTFC8GAKAJCN-4M IT

Figure 4. eMMC Interface



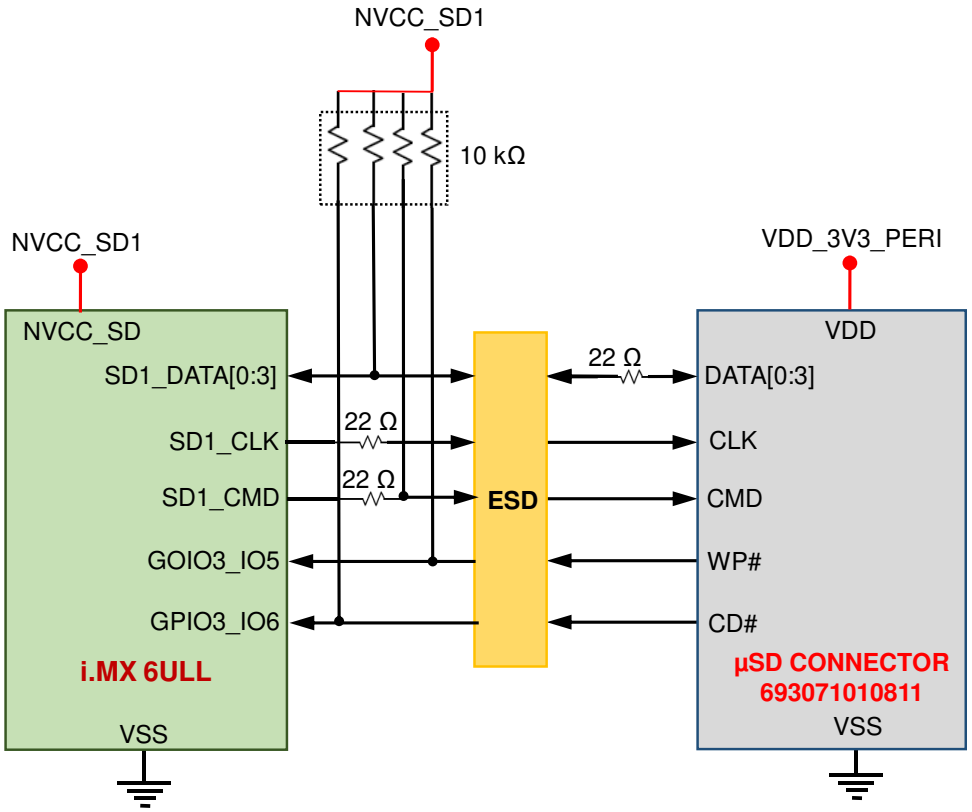
Note: NVCC_NAND and VCCQ needs to be 1V8 for HS200 Mode. CLK/CMD/DATA lines impedance need to be 50 Ω

2.2.2.4 SD Card Connector

i.MX 6ULL supports SD3.0 so in this design there is a micro-SD card connector provided. The power supply to the SD card is 3.3 V and the wiring for the SD Card interface is shown in Figure 5.

DESCRIPTION	MFG.	PART NUMBER
Conn, uSD card socket, 1x1, Push-Push, RA, SMD	Wurth Elektronik, Inc	693071010811
Diode, ESD-Bidir, 5.5V, SOD-882D	NXP	PESD5V0F1BL

Figure 5. SD Card Power and Connector

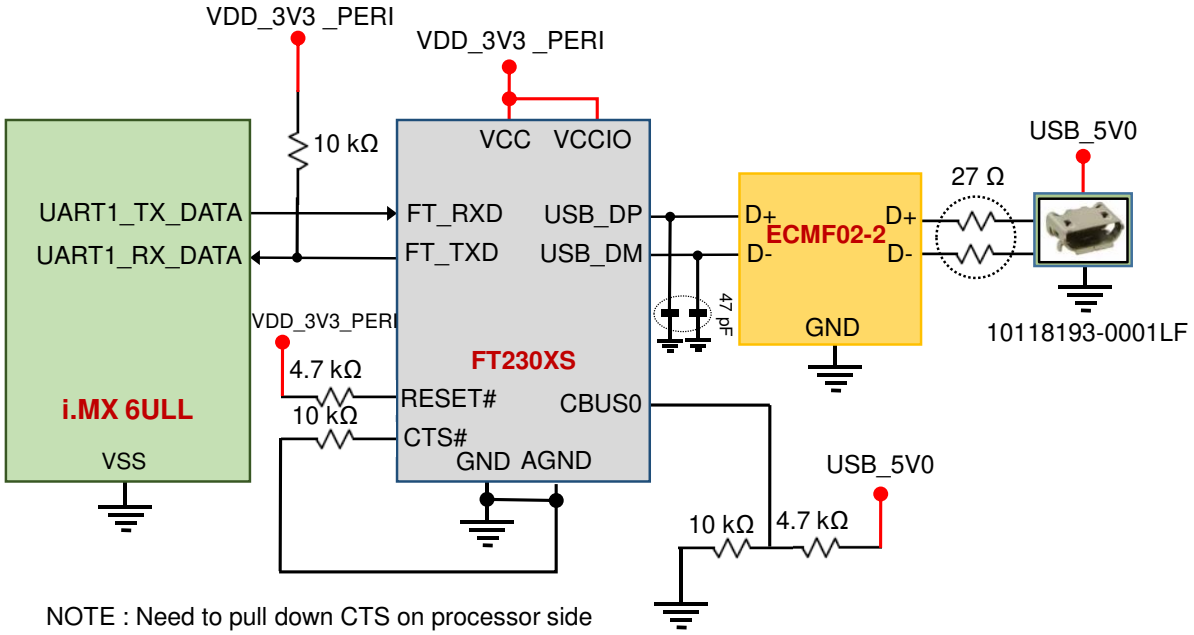


2.2.3 USB to UART Converter

There is a USB to Serial (UART) interface in the design. To implement this feature, the FT230X chip from FTDI is used which is a USB to dual port RS232 converter. The detailed diagram of interconnection is shown in Figure 6.

DESCRIPTION	MFG.	PART NUMBER
IC, FT230X, USB to UART Converter, SSOP-16	FTDI Chip	FT230XS
IC, ECMF02-2, Dual-line CM Filter with ESD Protection, 5GHz, WLCSP-5P	ST Microelectronics	ECMF02-2BF3
Conn, USB Micro-B Receptacle, 1x1, RA, SMD	FCI - Amphenol ICC	10118193-0001LF

Figure 6. USB to Serial UART Interface With FT230X

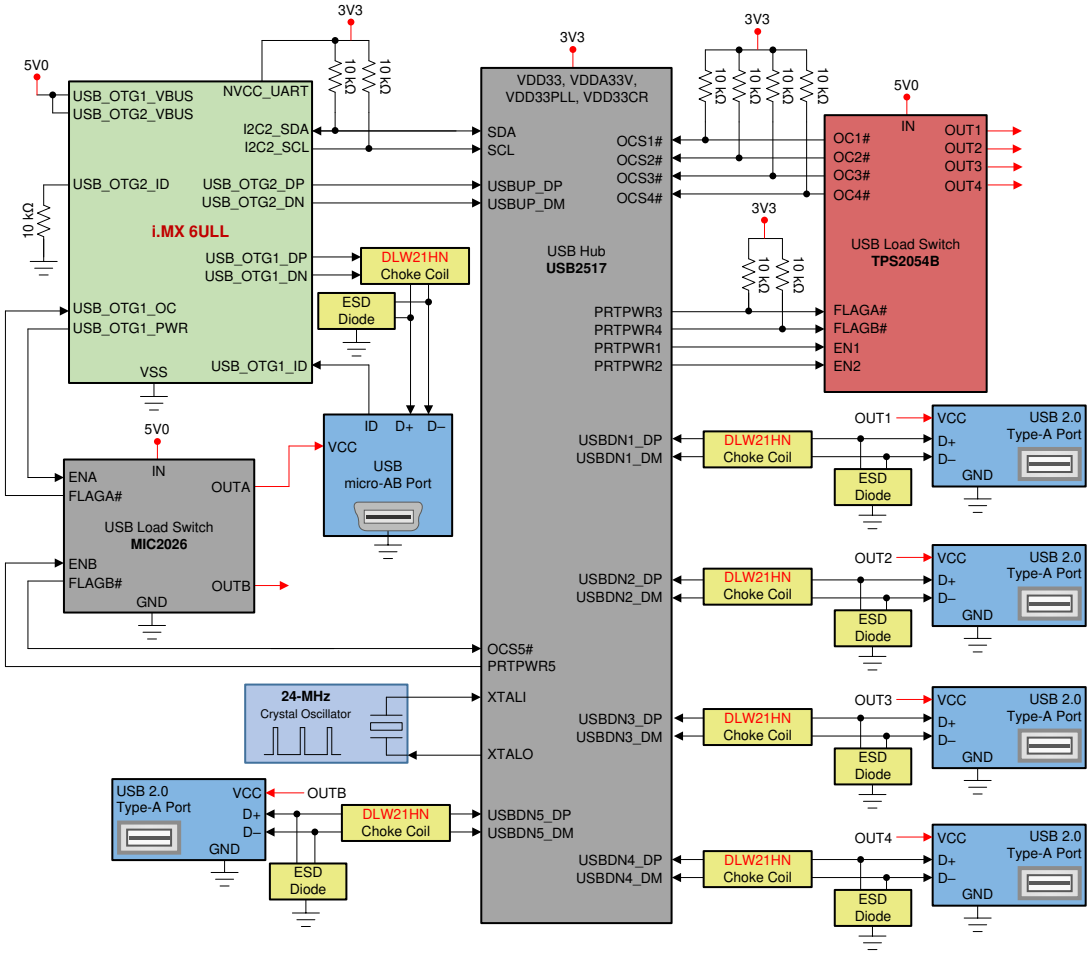


2.2.4 USB Ports

This design uses the processor's two USB interfaces, where the primary USB OTG1 interface connects directly to the micro-AB port and USB OTG2 acts as a host only, connecting to a USB Hub. The USB2517I is a 7-port USB hub that multiplexes the USB data from OTG2 and distributes the data to 5 Type-A receptacles. The block diagram shows both USB HUB and OTG interfacing with the processor. The wiring of the USB interfaces is shown in Figure 7.

DESCRIPTION	MFG.	PART NUMBER
USB Hub Section		
Conn, USB 2.0, Type-A, Receptacle, 1x1, Shielded, RA, TH	TE Connectivity	1-1734775-1
Conn, USB Type-A Receptacle, 2x1, Shielded, Stacked, RA, TH	TE Connectivity	ZX62D-AB- 5P8(30)
Filter, Choke coil, CM, 90E, 330mA, Signal Line, SMD	Murata	DLW21HN900SQ2L
IC, TPS2054B, Quad Current-Limited Power-Distribution Switch, SOIC-16	Texas Instruments	TPS2054BDR
IC, USB2517I, USB HUB, 7-Ports, QFN-64	Microchip	USB2517I-JZX
USB OTG Section		
Conn, USB 2.0 Micro AB Receptacle, 1x1, Shielded, RA, SMD	FCI - Amphenol ICC	10104111-0001LF
Filter, Choke coil, CM, 90E, 330mA, Signal Line, SMD	Murata	DLW21HN900SQ2L
IC, MIC2026, Dual Channel Power Distribution Switch, SOIC-8	Microchip	MIC2026-1YM

Figure 7. USB Interface



2.2.5 LCD Screen Connector

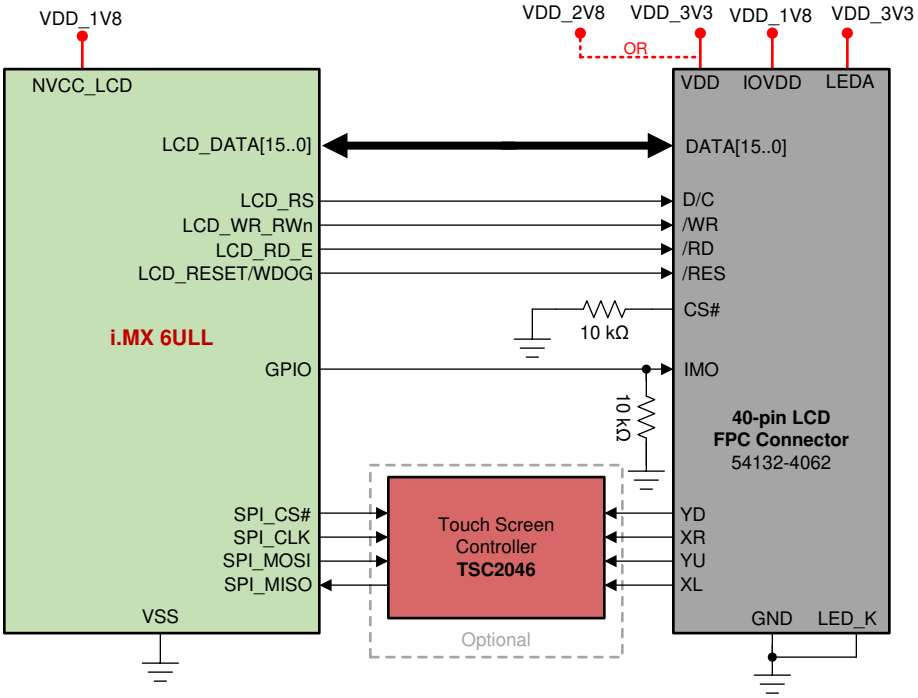
This design has a mountable LCD screen. The i.MX 6ULL processor's LCD interface can be used to control a wide range of display devices varying in size and capability. Many of these displays have an asynchronous parallel MPU interface for command and data transfer to an integrated frame buffer. There are other popular displays that support moving pictures and require the RGB interface mode (called DOTCLK interface in this document) or the VSYNC mode for high-speed data transfers. In addition to these displays, it is also common to provide support for digital video encoders that accept ITU-R BT.656 format. The goal is to select an LCD screen that is suitable for the application and compatible with the processor.

The Newhaven Display NHD-2.4-240320CF-CTXI#-F backlight and LCD screen selected for this design can make use of the already available 3.3 V and 1.8 V supply voltages so we can eliminate the need for additional voltage regulators. Additionally, this display is compatible with the processor and exceeds the simple requirements of a data concentrator application. The LCD interface is connected through 40-pin FPC connector. The connection diagram of the LCD interface is shown in Figure 8.

DESCRIPTION	MFG.	PART NUMBER
Display, TFT LCD, 240x320, 8/16-bit Parallel MPU Interface	Newhaven Display	NHD-2.4-240320CF-CTXI#-F
Conn, FPC, Receptacle, 1x40, 0.5mm, 0.5A, Bottom Contact, RA, SMD	Hirose Electric Co Ltd	FH40-50S-0.5SV
IC, TSC2046, Touch Screen Controller, TSSOP-16	*Texas Instruments*	*TSC2046IPWR*(1)

(1) The touch-screen controller is optional and can be added to take advantage of the touch-screen capability of the display, but TSC2046 is not mounted in this design.

Figure 8. LCD Interface From i.MX 6ULL Processor to Connector



2.2.6 JTAG Header

The JTAG connections match the requirements of the i.MX 6ULL for direct access to the processor for programming and debugging.

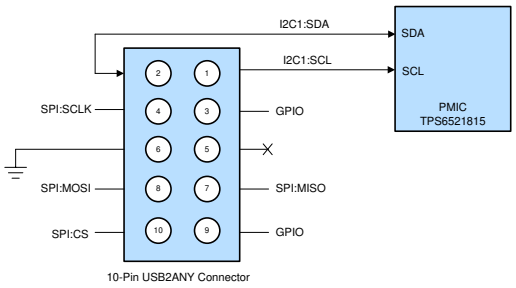
DESCRIPTION	MFG.	PART NUMBER
Connector, Berg strip, 2x5, 1.27mm, 1A, ST, SMD	FCI	20021121-00010*4LF

2.2.7 USB2ANY Header

USB2ANY is TI MCU-based adapter intended to allow a computer to control an electronic evaluation module (EVM) via a USB connection. In this design, the I^2C interface of USB2ANY is used to externally monitor, control, and or re-program the internal registers of PMIC. The wiring of the USB2ANY header is shown in Figure 9.

DESCRIPTION	MFG.	PART NUMBER
Connector, Berg strip, 2x5, 2.54mm, ST, SMD	Samtec	TSM-105-01-T-DV

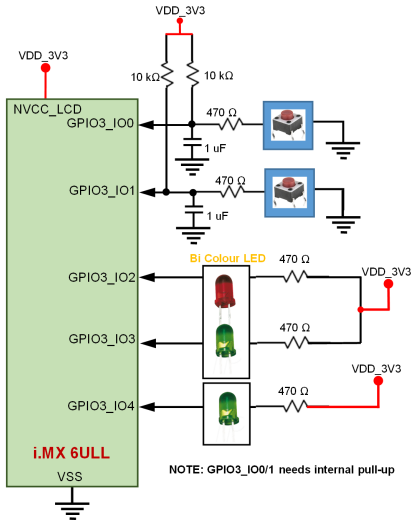
Figure 9. USB2ANY Header Connections to PMIC I^2C Pins



2.2.8 Functional Switches and Status LEDs

There are two functional multi-purpose push buttons connected to GPIOs configured as inputs on the processor that can be used for software developers to test applications developed using this board. Three LED are connected to three GPIOs of the processor to indicate the status of processes that are running, completed, or may have failed. Both the push-buttons and status LEDs can be used for debugging or to provide tactile inputs and visual feedback to the user. These connections are shown in Figure 10.

Figure 10. GPIO Connections to Push-buttons and LEDs



2.2.9 GPIO Expansion Connector

All un-used GPIO pins on the i.MX 6ULL processor are routed out to an expansion header, which is also capable of providing 1.8 V, 3.3 V, and 5 V to a daughter card PCB.

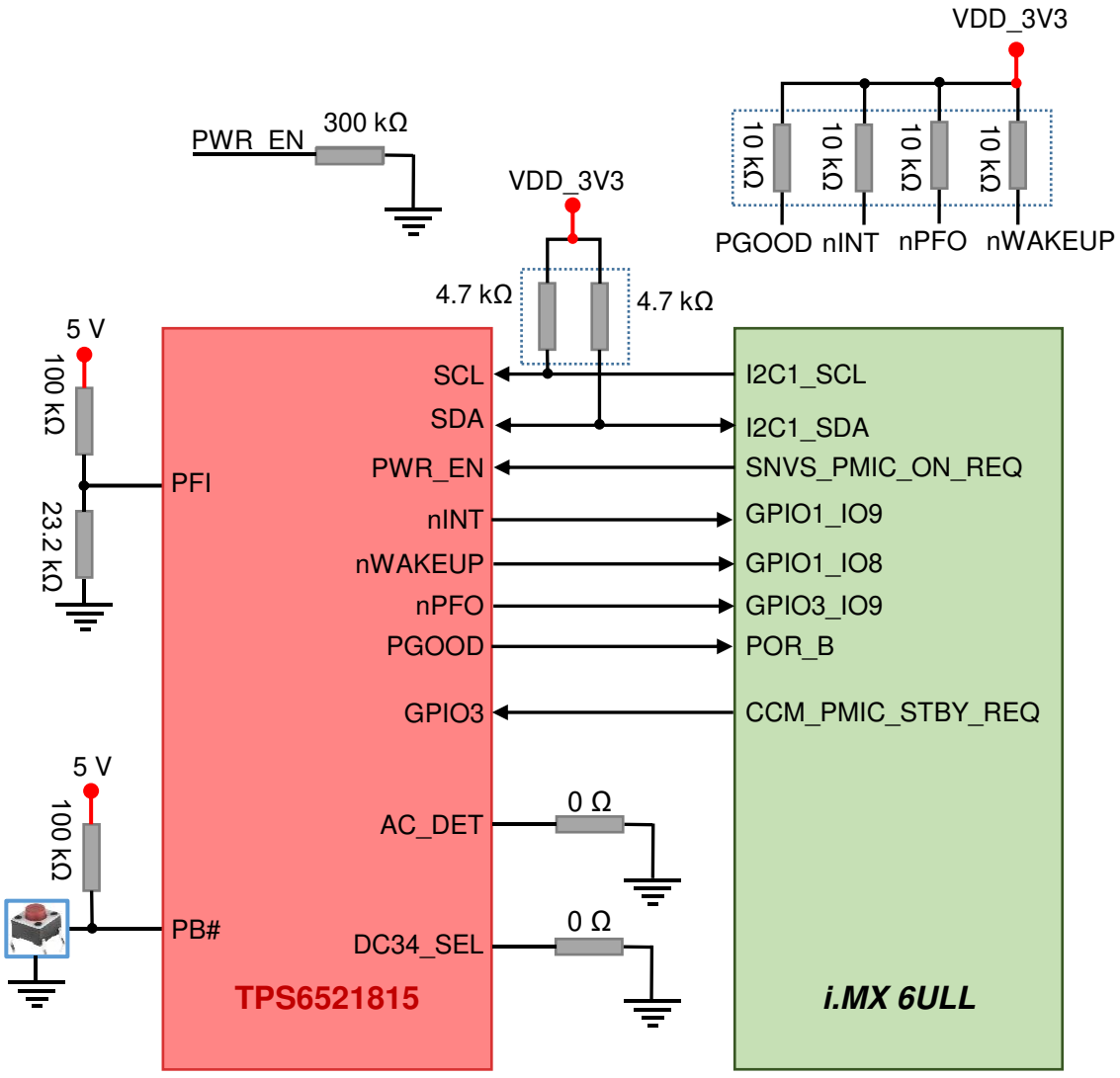
2.3 Highlighted Products

2.3.1 TPS6521815 - Power Management IC

The TPS6521815 device is a Power Management IC (PMIC) specifically designed to support Arm Cortex processors like the i.MX 6ULL from NXP. The PMIC is a good fit for applications powered from a 5-V supply or a Li-Ion battery. The IC consists of three adjustable step-down (buck) converters, one buck-boost converter, one adjustable LDO regulator and three load switches with two selectable current limit. The PMIC supports undervoltage lockout (UVLO), over-temperature warning and shutdown, separate power-good output for all regulators, programmable power sequencing for all regulators, and an I^2C interface for register reading and writing to the device. The full power architecture of this design is shown in Figure 15.

The I/O connections between the processor and the TPS6521815 PMIC are shown in Figure 11, as well as analog and digital input pins on the PMIC.

Figure 11. TPS6521815 PMIC I/O Wiring to i.MX 6ULL Processor



2.3.2 DP83849I - Dual Ethernet PHY

i.MX 6ULL supports two 10/100Mbps (MII/RMII) Ethernet interfaces. This design requires two 100 Base-T Ethernet ports so the DP83849I-Dual Ethernet PHY is used in this design. This Ethernet PHY supports two RMII interface and able to work from a single 3.3V supply. The PHY needs an external 50MHz oscillator to function properly. To connect MDI to the Cat5e cable, we used a dual RJ45 connector with internal magnetics from Wurth Elektronik. The addresses for the two separate PHYs are listed in Table 2.

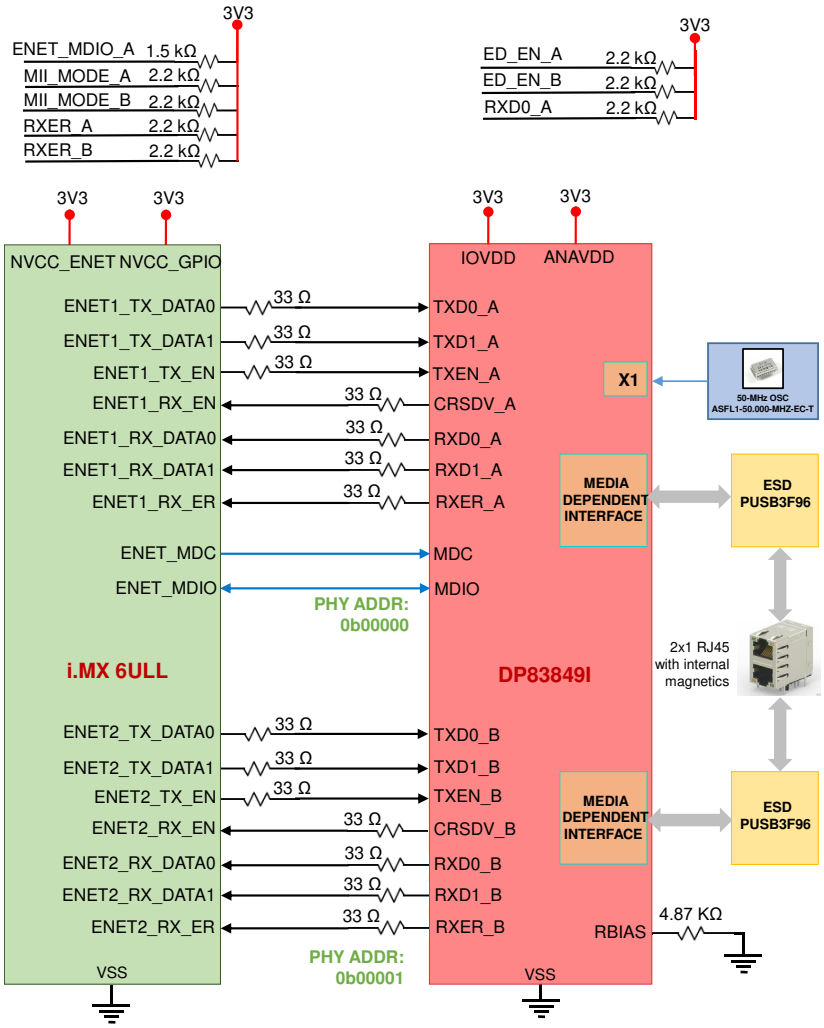
Table 2. PHY Addresses

PHY Number	PHY Address
PHY1	0b00000
PHY2	0b00001

The Ethernet interface connections are shown in Figure 12.

DESCRIPTION	MFG.	PART NUMBER
IC, DP83849I, Dual Port, 10/100 Ethernet PHY Transceiver, TQFP-80	Texas Instruments	DP83849IVSX/NOPB
Connector, RJ45 Jack with Magnetics, Shielded, LED(G/Y, G/Y), RA, TH	Wurth Elektronik	7499111446

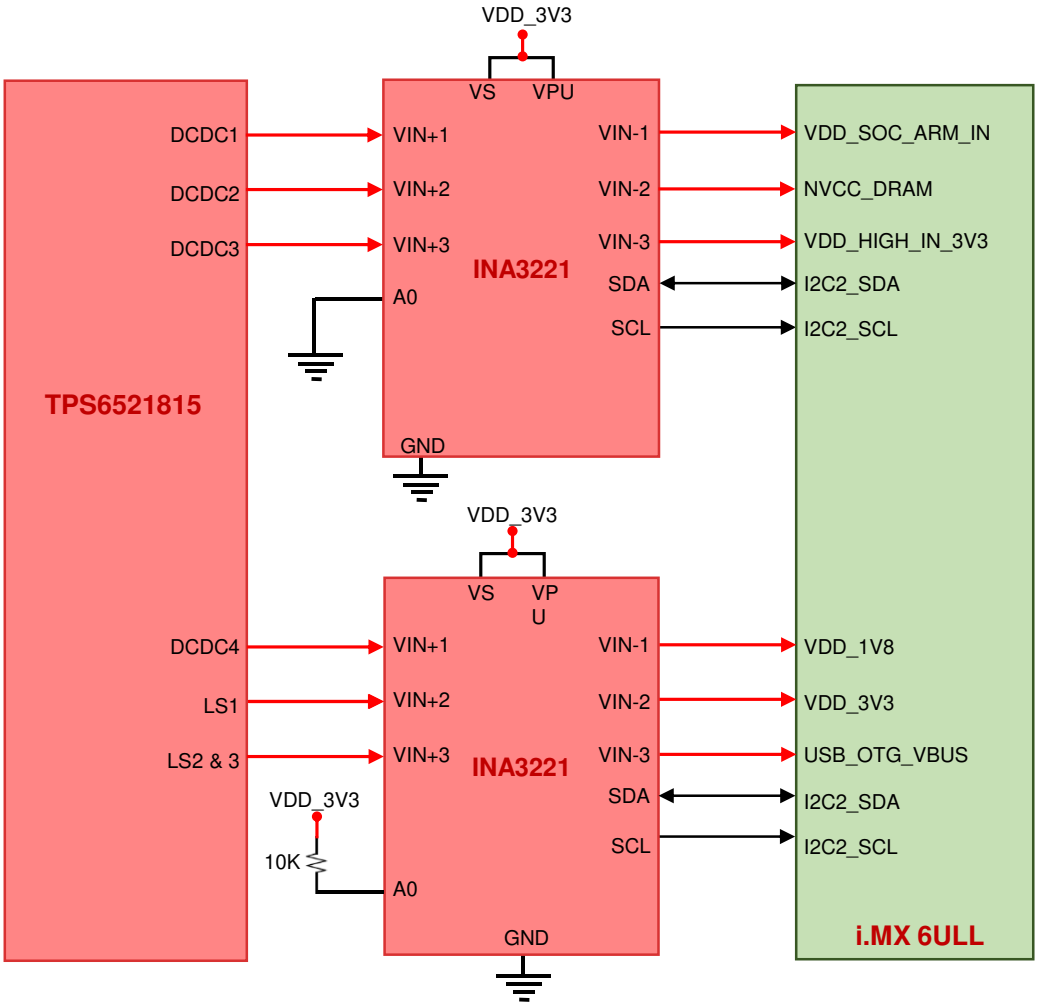
Figure 12. Ethernet Interface With DP83849I PHY



2.3.3 INA3221 - Current Monitor

To measure the live current information, a current sense circuit is inserted in series with the power nets from the PMIC to the processor. The current sensing is done with the INA3221 device. There are two devices used to monitor all the TPS6521815 PMIC power rails. The wiring is shown in Figure 13. The address pin A0 of the INA3221 device needs to be terminated according to Table 3.

Figure 13. INA3221 Current Sensor Wiring From PMIC to Processor



(1) Both of the I²C lines, SDA and SCL, require a pull-up resistor. A resistance of 2.2-kΩ is used to pull-up these open-drain signals to 3.3V

Table 3. INA3221 I²C Slave Address Options

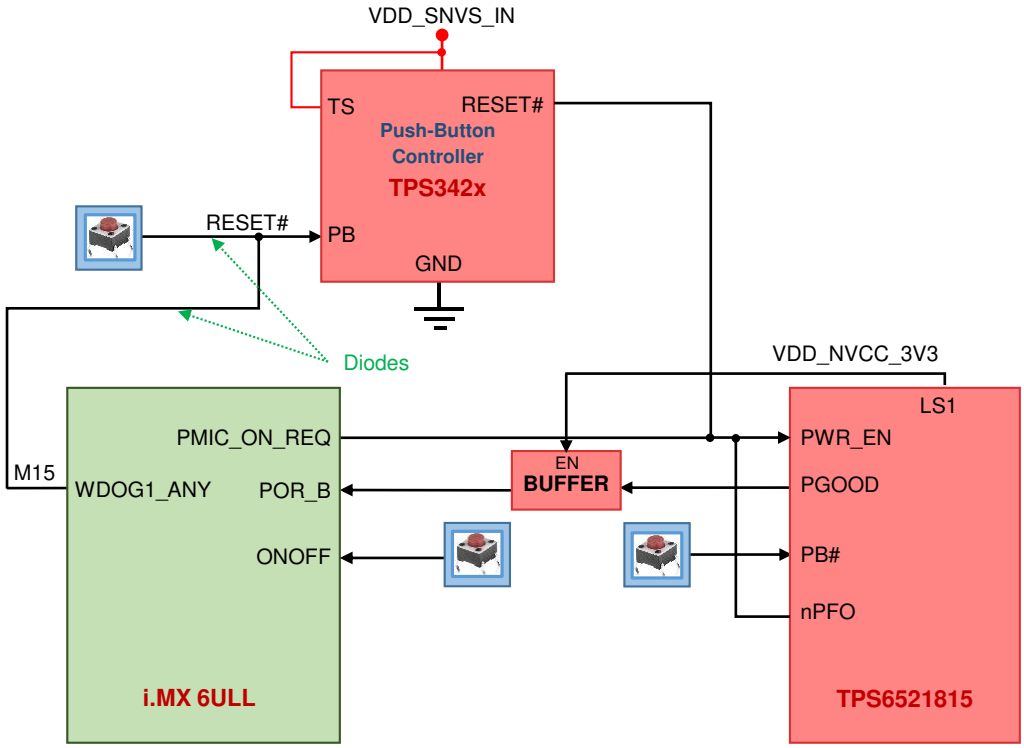
7-BIT BINARY ADDRESS	7-BIT HEX ADDRESS	ADDR PIN TERMINATION
1000000b	0x40	GND
1000001b	0x41	V_S
1000010b	0x42	SDA
1000011b	0x43	SCL

2.3.4 Reset Scheme

The reset scheme for this project is shown in Figure 14. The DCDC6 low-power buck regulator from TPS6521815 provides the VSNVS voltage from the coin-cell. If the coin-cell is not inserted, the PMIC will still provide VSNVS supply first through SYS_BU input. This is critical to ensure the power-up sequence is correct. When VSNVS is stable along with all the power outputs, the PGOOD pin will de-assert the Power-ON Reset (POR_B).

A reset push-button is connected to the watchdog output of the i.MX 6ULL processor in a wire-OR configuration, which goes into the PB input of a TPS342x push-button controller. The push-button controller can override the enable signal (PWR_EN) to the PMIC and the POR_B input on the processor simultaneously, forcing the system to reset. To shut the system down completely, a separate push-button connected to the ONOFF pin of the processor is used.

Figure 14. Reset Scheme

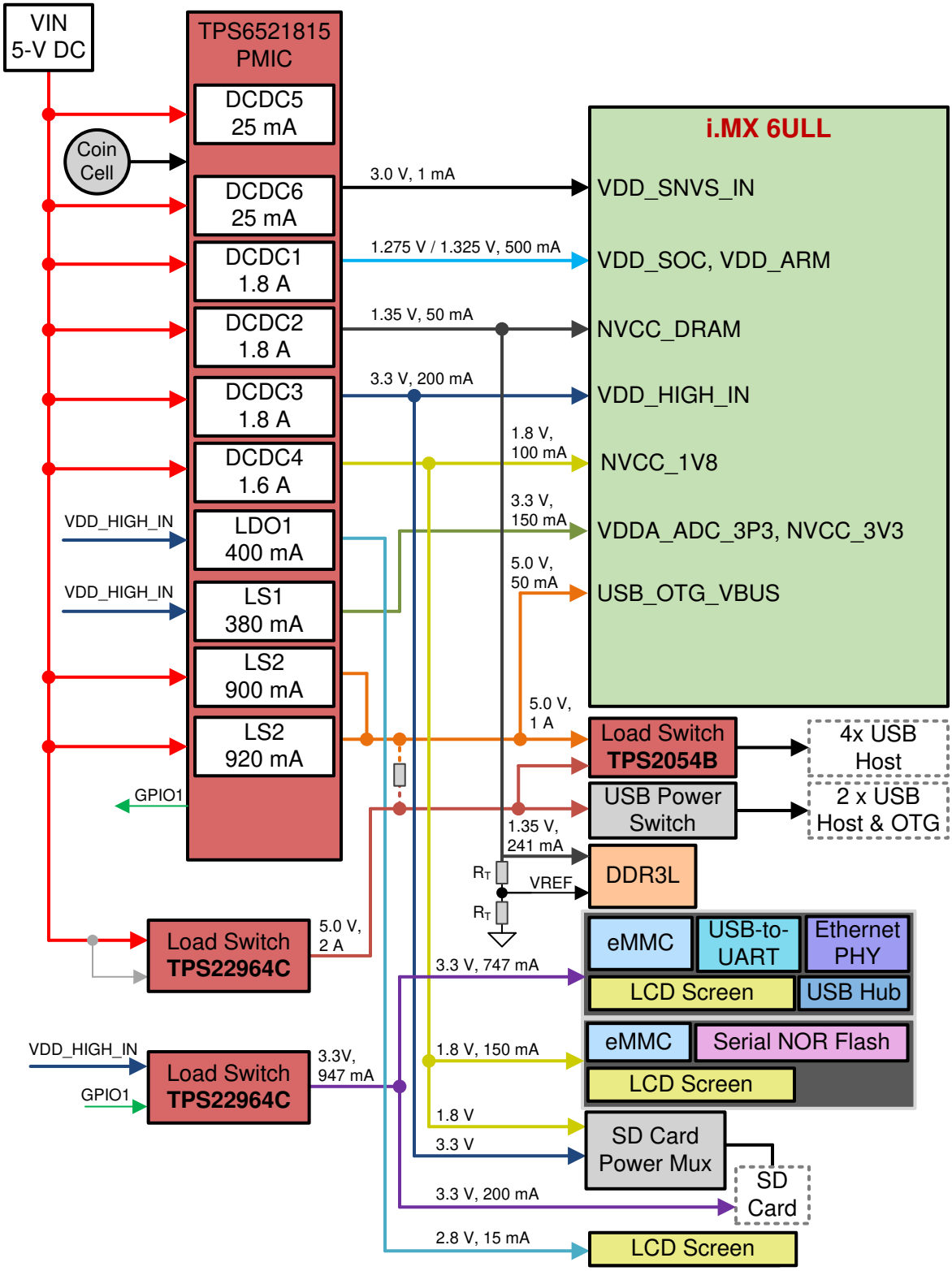


2.3.5 TPS2054B, TPS22964C - Auxiliary Load Switches

Figure 15 shows the full power architecture. Each peripheral device added to a design may require additional power in addition to what is required by the processor. For this design, we had to add load switches (TPS22964C, TPS2054B) for powering the multiple USB ports and an additional load switch (TPS22964C) for 3.3 V peripherals for the MIPI CSI. Both of these voltages are already available in the design: 5 V is the main input power supply voltage and 3.3 V is generated by DCDC3 of the TPS6521815. As a result, only load switches were added to enable and disable these supply rails, as opposed to adding additional DC-DC or LDO voltage regulators.

Finally, it is sometimes necessary to terminate DDR memory. DDR termination provides a supply (0.675 V) that is half the voltage of the main supply (1.35 V) with the ability to sink or source current. If only one channel of DDR is used, the current consumption is low, or the routing is point-to-point, then tapping off the center of an evenly matched voltage divider may be sufficient. In other cases, a DDR terminator power IC is needed. For this design, we used the matched resistor divider option to terminate the single DDR3L memory IC in the system.

Figure 15. TIDA-050043 Full Power Architecture



2.4 System Design Theory

The full power architecture is the result of carefully estimating the power consumed by ICs on the board and peripherals that can be connected to the board. The ideal power sequencing of the i.MX 6ULL processor must be known to ensure the power sequencing of the TPS6521815 is correct. The I^2C chain must be drawn in its entirety to ensure there are no I^2C address conflicts. The BOOT Mode settings must be mapped to boot the processor using the intended memory storage IC. And finally, PCB floor planning must be completed to make sure the layout of the board is reasonable. All of this system design theory is taken into consideration in this section.

2.4.1 Power Estimation

This design is powered from a 5-V adapter. This 5 V is the main power supply to the TPS6521815 device. The PMIC will generate 6 different voltages: 1.275 V/1.325 V with dynamic voltage scaling (DVS), 1.35 V, 3.3 V, 1.8 V, 2.8 V, and a 2.4 V to 3.0V always-on supply for SNVS. The load switches LS2 and LS3 are used to power USB slave devices with 5.0 V. The estimated current consumption for each rail is listed in Table 4.

Table 4. System Power Estimation

VOLTAGE (V)	SUPPLY IC, RAIL NAME	SUPPLY CURRENT (mA)	LOAD IC, RAIL NAME	CURRENT (mA)	POWER (mW)
1.275/1.325	TPS6521815, DCDC1	1800	iMX6 VDD_SOC_IN	500	663
1.35	TPS6521815, DCDC2	1800	iMX6 NVCC_DRAM	50	67.5
			DDR3L VDD/VDDQ	290	392
3.3	TPS6521815, DCDC3	1800	iMX6 VDD_HIGH_IN	200	660
			iMX6 NVCC_3V3	150	495
			DP83849I IOVDD, ANA33VDD	50	165
			IOVDD_LCD, VDD_LCD_BCKLIGHT	200	660
			eMMC	40	132
			SD Card	200	660
			FT230X	10	33
			USB Hub (USB2517)	460	1518
1.8	TPS6521815, DCDC4	1600	i.MX7 NVCC_1V8	100	489
			eMMC	100	180
			NOR Flash	35	63
2.8	TPS6521815, LDO1	400	VDD_LCD	200	560
5	TPS6521815, LS2/3 & TPS22964C into TPS2054B & MIC2026	1820 & 2000 into 4x500 & 2x500	6x USB2 Ports	3000	15000
			USB_OTG_VBUS	50	350
2.4 - 3.0	TPS6521815, DCDC6	25	iMX6 VDD_SNVS_IN	1	3
				Total Estimated Power	**22.1 W**

2.4.2 Power Sequencing

The processor power-up sequencing is shown in Figure 16. First the VDD_SNVS needs to turn on before any other power supply. For our design, VDD_SNVS is powered through a coin cell connected to the CC pin of the TPS6521815 PMIC, and the DCDC6 supply will always be the first PMIC supply rail to turn on. Once SNVS voltage is stabilized, then VDD_HIGH_IN should turn on because VDD_HIGH_IN should be enabled before VDD_SOC_IN for the i.MX 6ULL processor. After VDD_SOC_IN, NVCC_DRAM is turned on for the DDR3L memory followed by 3.3 V for I/O and analog along with 2.8 V for the LCD screen. The final supply to turn on is the 1.8-V I/O rail. Once all these voltages are enabled and within regulation, there is a delay before PGOOD is set high. PGOOD is the PMIC output that control the power-on reset (POR_B) input of the processor.

The processor power-down sequencing is shown in Figure 17, which is the reverse of the power-up sequence.

Figure 16. Required Power-Up Sequence for i.MX 6ULL Processor

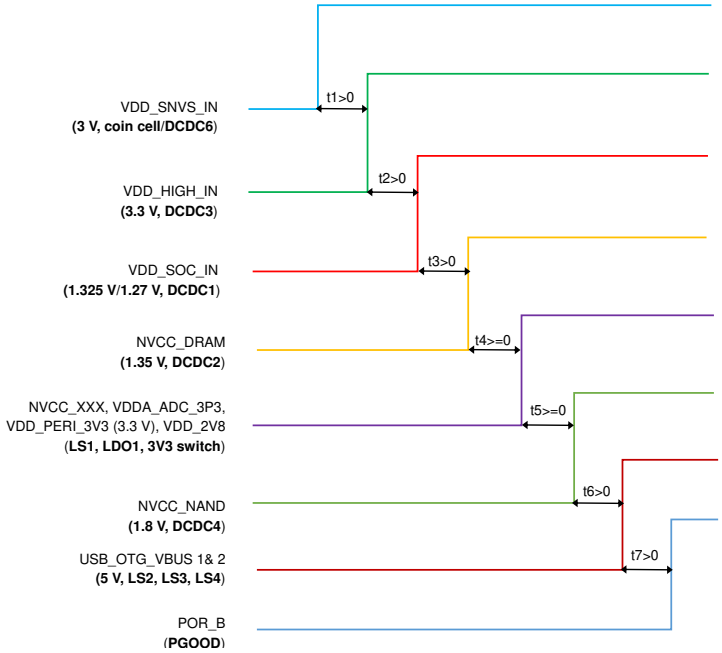
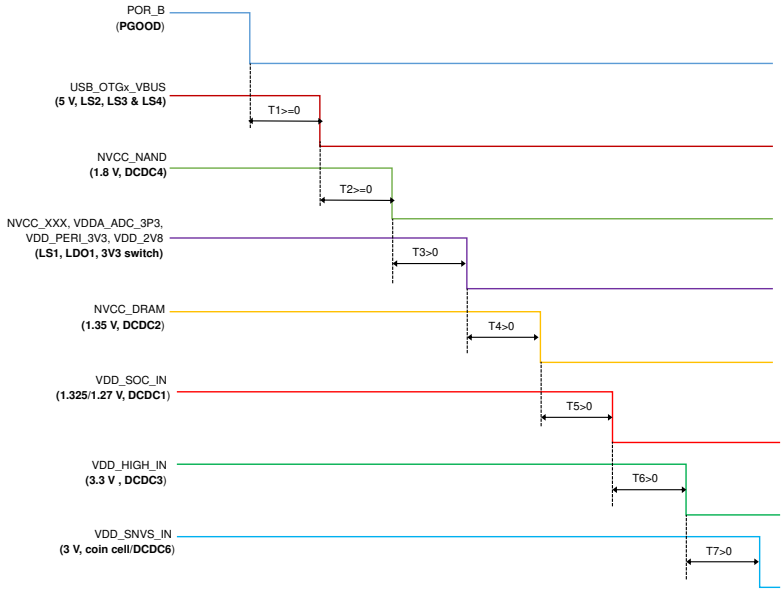


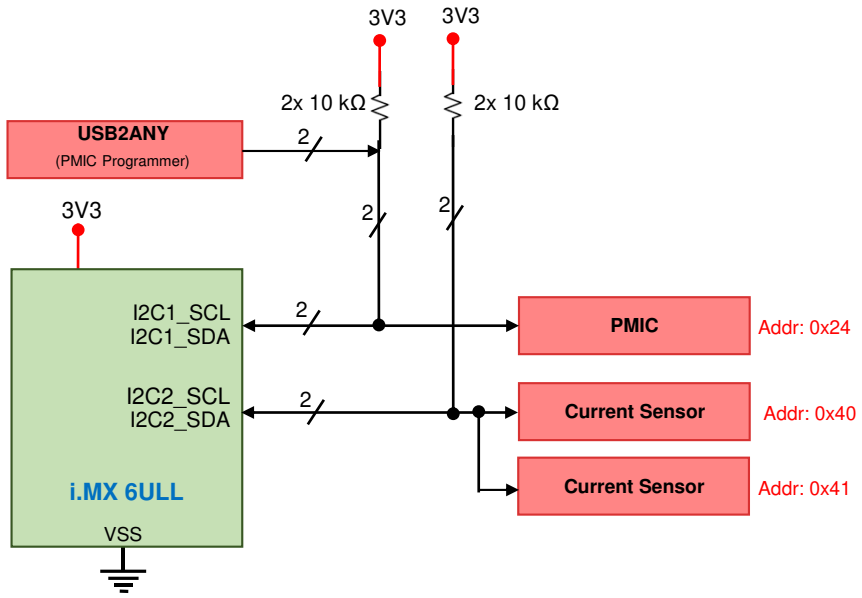
Figure 17. Required Power-Down Sequence for i.MX 6ULL Processor



2.4.3 I²C Device Chain

Figure 18 shows the I²C channel mapping from the processor to each slave device.

Figure 18. I²C Device Chain

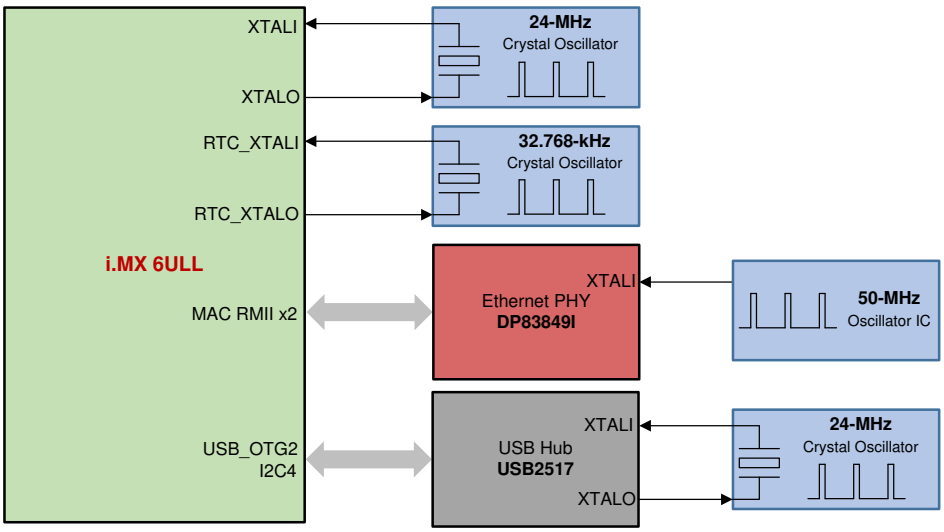


2.4.4 Clock Scheme

The following is a list matching the required clock frequency to each IC that needs clocking. Figure 19 shows the clocks that interface with the i.MX 6ULL processor.

- i.MX 6ULL – 24 MHz and 32.768 kHz
- DP83849I (Ethernet PHY) – 50 MHz
- USB2517I (USB Hub) – 24 MHz

Figure 19. Clock Structure



2.4.5 BOOT Configuration

This design uses two sets of BOOT configuration switches. BOOT Mode pins are controlled by SW7 DIP switches that are connected to dedicated BOOT_MODE0 and BOOT_MODE1 input pins of i.MX 6ULL Processor. Along with these, there are 24 different pins for setting Boot Config which shares pins with LCD Data. Of these 24 pins, 4 of them are controlled by the 4 DIP Switches of SW6. All of the possible BOOT options for this design are given in Table 5 (SW7) and Table 6 (SW6). The connections of the DIP switches to the processor are shown in Figure 20

Figure 20. BOOT Mode and Configuration DIP Switches

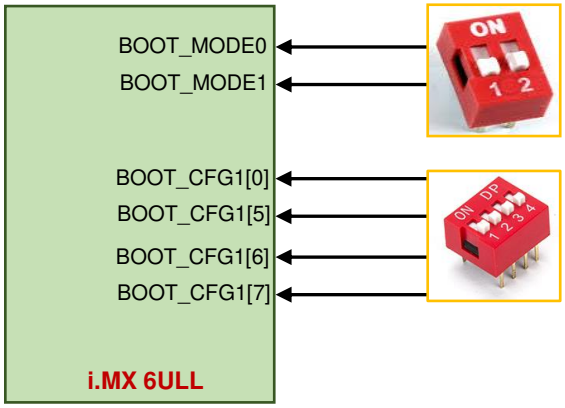


Table 5. SW7 BOOT Mode Settings

	SW7, PIN 1	SW7, PIN 2
BOOT Type	**BOOT_MODE[1]**	**BOOT_MODE[0]**
Boot from Fuses	0	0
Serial Download	0	1
Internal BOOT	1	0
Reserved	1	1

Table 6. SW6 BOOT Config Settings

	SW6, PIN 4	SW6, PIN 3	SW6, PIN 2	SW2, PIN 1
BOOT Device	**BOOT_CFG1[7]**	**BOOT_CFG1[6]**	**BOOT_CFG1[5]**	**BOOT_CFG1[0]**(1)
QSPI	0	0	0	x
SD, eSD, SDXC	0	1	0	x
eMMC(2)	0	1	1	x

(1) BT_CFG1[0] is used for SD loopback clock selection.
(2) To select boot device as eMMC, an assembly change must also be performed. See schematic for details.

2.4.6 PCB Floor Planning

Figure 21 shows the floor planning for the top side of the PCB and Figure 22 shows the floor planning for the bottom side of the PCB.

Figure 21. PCB Floor Planning (top)

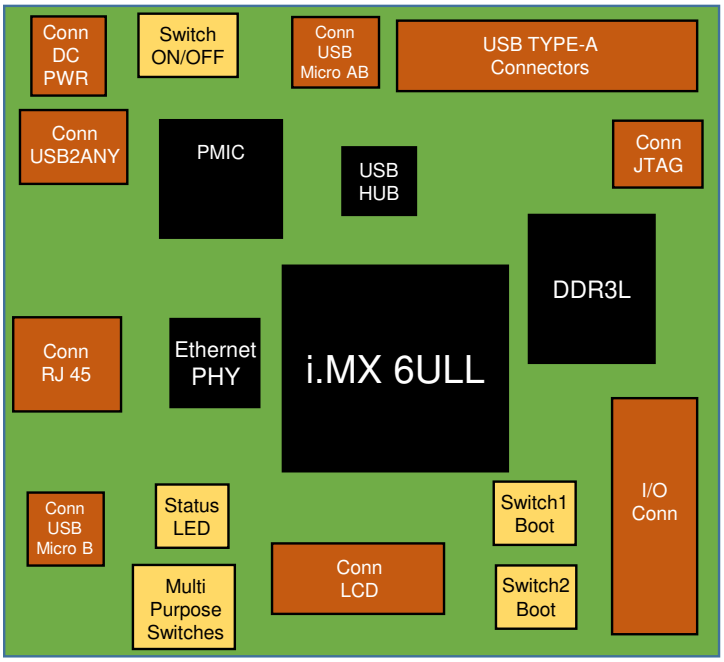
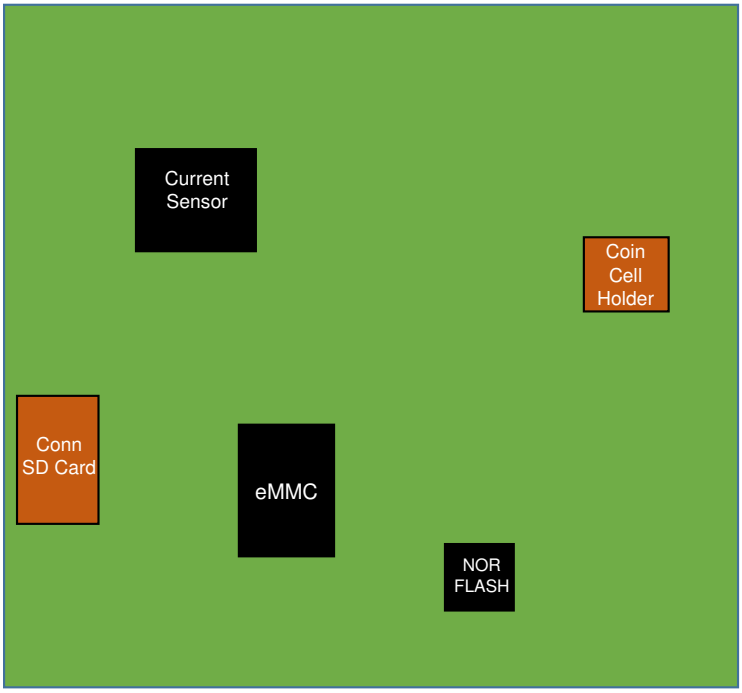


Figure 22. PCB Floor Planning (bottom, flipped)



3 Getting Started, Testing Setup, and Test Results

3.1 Getting Started with Hardware and Software

3.1.1 Hardware

This section contains information about the initial set-up of the TIDA-050043 board, power-up options and user interfaces. Figure 23 shows the top side of the fully assembled PCB with labels to help locate connectors or switches on the boards.

Figure 23. Top of TIDA-050043 PCB With Labels

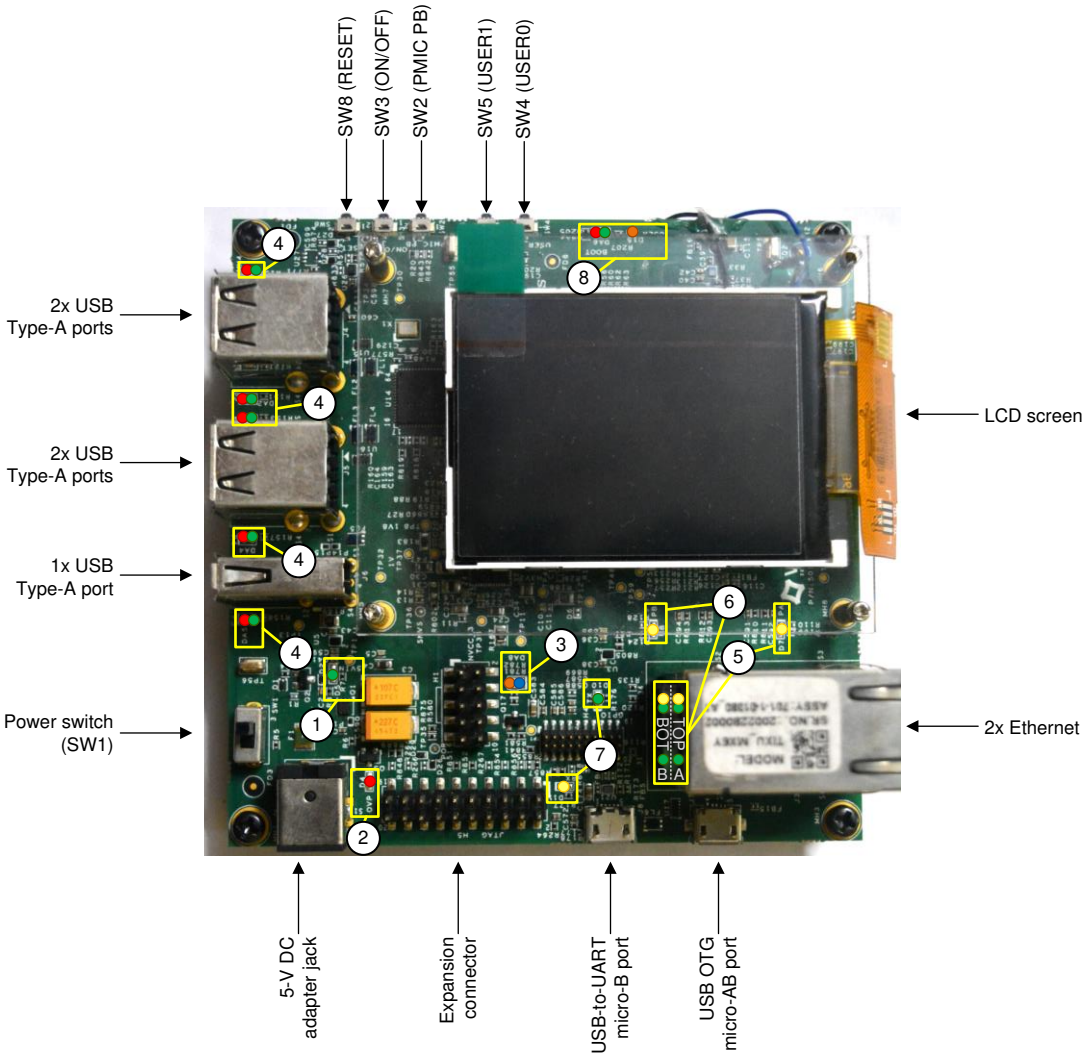
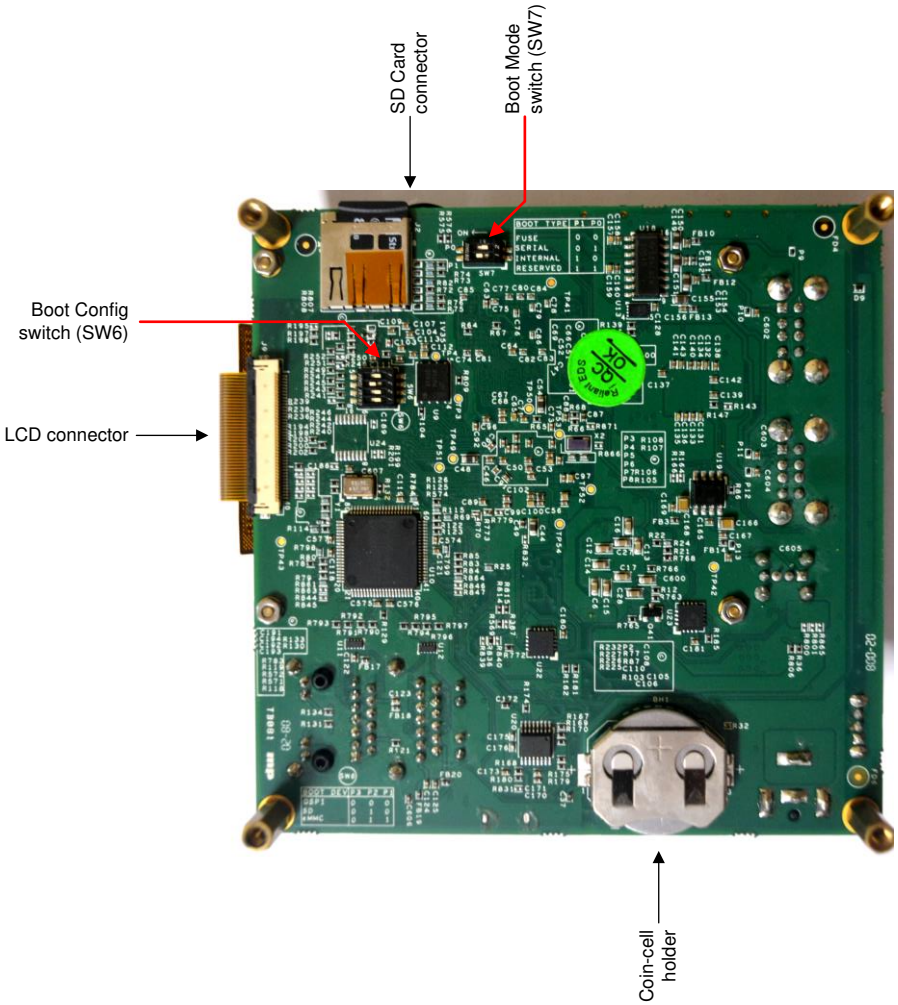


Figure 24 shows the bottom side of the fully assembled PCB with labels.

Figure 24. Bottom of TIDA-050043 PCB With Labels



The following is a list of steps that must be followed to set up the hardware of the system.

1. Attach stand-offs to the board with screws inserted in the four holes at the edge of the PCB.
2. Set the BOOT option using SW7/SW6 DIP switches (Figure 25 and Figure 26).
3. Insert CR2032 coin-cell battery in the holder BH1 (Figure 27).
4. Insert the SD card in J2 connector, if SD Card is used for BOOT (Figure 28).
5. Insert the USB micro-B cable into J8 connector for UART debug in Terminal window (Figure 29). Type-A plug connects to computer USB port
6. Insert the 5-V DC adapter barrel jack into J1 connector to supply power (Figure 30). SMI24-5-V-P6 from CUI Inc is the recommended power supply.
7. Set SW1 to the *ON* position.
8. After BOOT is complete, connect the desired peripherals. For example: RJ-45 Ethernet (J3), LCD screen (J9), USB device (J4, J5, J6, J7).

Figure 25. Setting DIP Switch (SW7) for BOOT Mode from Internal Memory

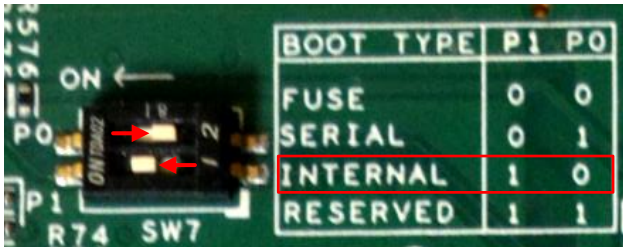


Figure 26. Setting DIP Switch (SW6) for BOOT Config from SD Card

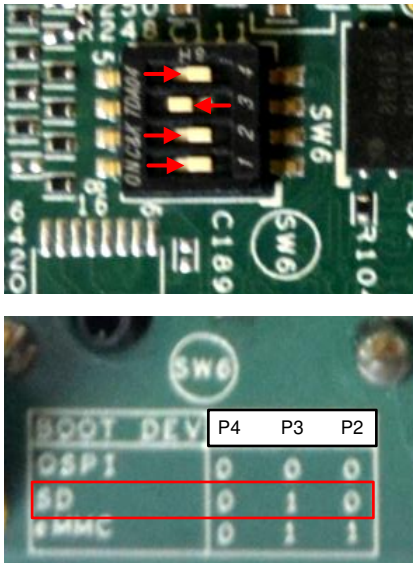
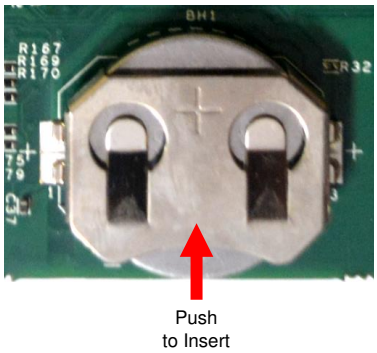


Figure 27. Inserting Coin Cell Battery Into BH1



NOTE: The voltage of the coin-cell battery (3.0 V nominal) must be above 2.4 V for the supervisor to allow system power-on. If the coin-cell battery voltage is too low, it must be replaced with a fresh battery to continue testing.

Figure 28. Inserting SD Card Into J2

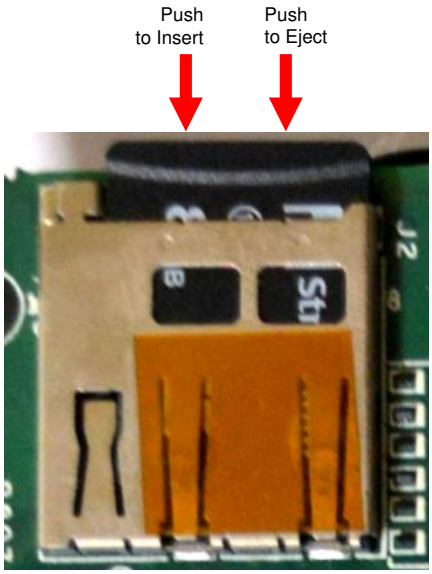
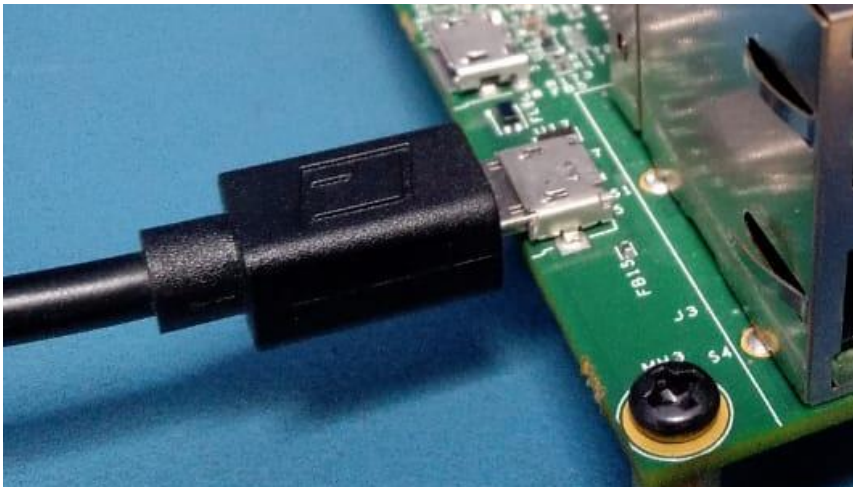


Figure 29. Inserting micro-B Cable Into J8



NOTE: Refer to Section 3.1.2 for the procedure to debug TIDA-050043 through Terminal window

Figure 30. Inserting 5-V DC Adapter Into J1

NOTE: Power supplies other than the SMI24-5-V-P6 may be substituted if the DC output voltage, current rating, polarity, and barrel jack size (inside diameter and outside diameter) are equivalent. Power supplies with DC voltage greater than 5.25V are not acceptable because of the over voltage protection circuit on the board which is intended to prevent damage to the ICs.

NOTE: It is always recommended to power-down the system by switching SW1 to the *OFF* position before unplugging the DC adapter power supply.

3.1.1.1 On-board LED Information

Table 7 lists the indicator LEDs installed on the PCB and provides a short description of their meaning to improve the user experience getting started with the TIDA-050043 reference design.

Table 7. Indicator LEDs

NUMBER[1]	DESIGNATOR	DESCRIPTION	MEANING
1	D5	Power-On LED	ON: Power-On
			OFF: Power-Off
2	D4	Over-voltage LED	ON: Input over-voltage (>5.25 V)
			OFF: Input voltage within recommended range
3	DA8	Coin-Cell LED	Blue: PMIC BU domain powered from main supply
			Orange: PMIC BU domain powered from coin cell
4	DA1-DA5	USB Link LEDs	Green ON: LS device attached
			Red LED: FS device attached
			Orange ON: HS device attached
			OFF: No devices are attached, or the hub is in suspend
5	D7[2]	Ethernet Link LED (Port A)	ON: Ethernet link established
			OFF: Ethernet link down
6	D8[2]	Ethernet Link LED (Port B)	ON: Ethernet link established
			OFF: Ethernet link down
7	D10, D11 (COM)	Debug UART TX/RX	D10 blinking: Transmitting data
			D11 blinking: Receiving data
8	DA6 (Red/Green), D15	User LEDs (processor status)	RED ON: U-boot running
			RED Blinking: Kernel running
			GREEN ON: File system running

(1) Number shown in Figure 23

(2) D7 is assigned to Port A along with J3A (top port) indicator LEDs, and D8 is assigned to Port B along with J3B (bottom port indicator LEDs)

3.1.2 Software

The primary boot source used for testing TIDA-050043 was the SD card. The primary method for testing was using a pre-built binary image to prepare SD card. The purpose of this section is getting started using the software and assumes the software used is already written onto an SD Card that is inserted into the correct slot on the PCB and the BOOT switches are set properly.

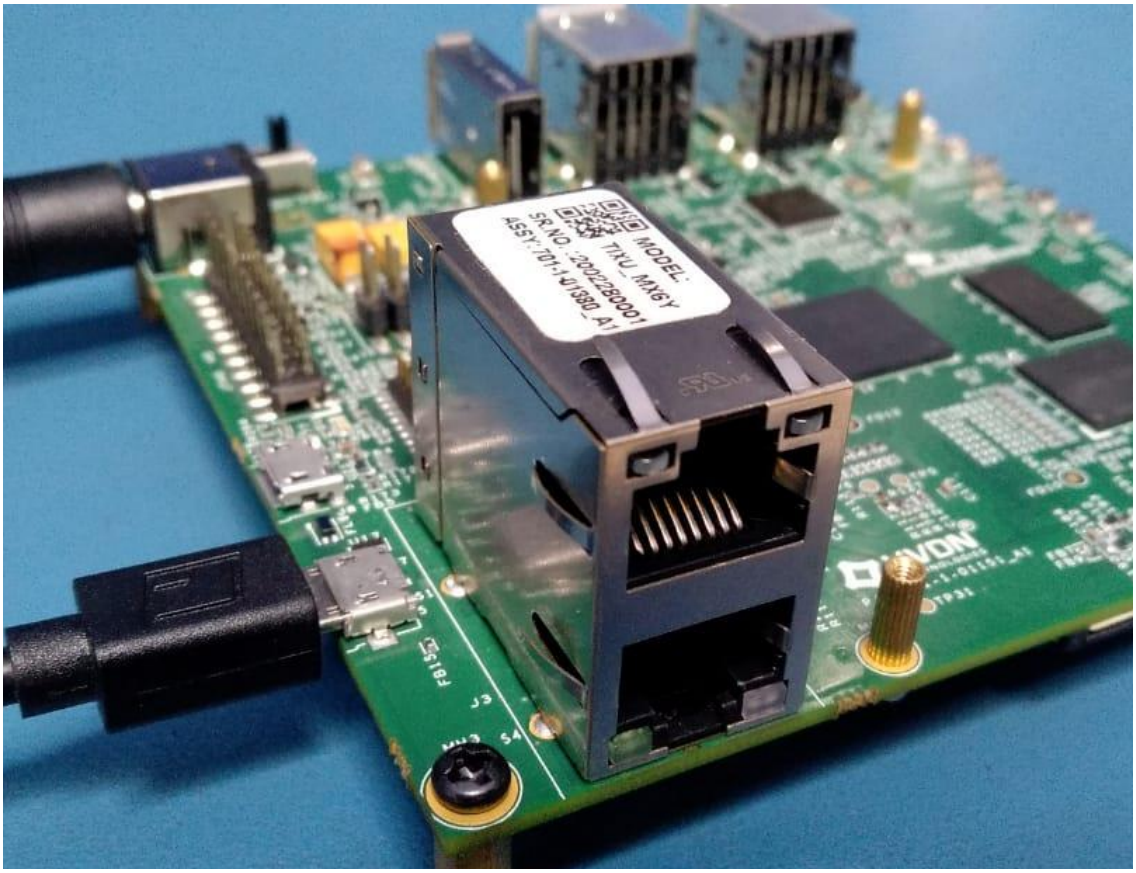
The software used for testing is an embedded Linux Yocto build with drivers written for all of the TI ICs and patches to modify the original SDK written for the NXP i.MX 6ULL processor. Building and installing the image requires a laptop running Ubuntu 16.04 (or later), 120 GB HDD, a fully-assembled TIDA-050043 board, micro-SD card, micro-SD to SD Card adaptor, a micro-USB cable, and a 5-V DC power supply. The procedure for building and installing the software image is outside the scope of this document.

3.1.2.1 Booting of TIDA-050043

Insert the SD card into the SD card slot provided in the board and set the boot switches to boot from SD card. If executables are not found in the configured boot source, then the software is automatically fetched from the SD card.

Connect micro-B side of a USB cable to debug port of the board and Type-A side to a host PC. The connections on the board at this step will look like Figure 31.

Figure 31. Board Connections for BOOT from SD Card With Debug Over USB (LCD screen removed)



Use TeraTerm or Putty to open a Terminal and get the debug log from the device node if the host PC is running Windows. Change port number according to the COMxx port found in Device Manager for the FTDI chip.

For example, when I am testing this board I can select the **COM7** port with a baud rate of **115200** and leave the other **Putty** settings as the default option.

If the debug prints are coming when the board is powered on, then that interface is working. When prompted to logon, enter *'root'* and press the **Enter** key.

```
timx6y login: root
root@timx6y:~#
```

At the time of writing, the latest software/firmware version for TIDA-050043 is 3.0.1_3, which can be verified using a simple Linux command.

```
root@timx6y:~# fw-version
firmware version : 3.0.1_3
```

There are many other Linux functions and commands that are useful for testing the power supplies and consumption of TIDA-050043, and the next section provides some examples.

3.1.2.2 Example Linux Commands for Testing TIDA-050043

To figure out which I²C devices are on the bus, where "0" means I am looking for I²C devices on channel 0 (because the TPS6521815 should be here at 0x24):

```
root@timx6y:~# i2cdetect -y -r 0
     0   1   2  3   4   5   6   7   8   9   a   b   c   d  e   f
00:             --  --  --  --  --  --  --  --  --  --  --  --  --
10: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
20: --  --  --  --  UU  --  --  --  --  --  --  --  --  --  --  --
30: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
40: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
50: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
60: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
70: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
```

To verify dynamic voltage scaling is working for the PMIC with respect to the CPU frequency of the processor, where 792 MHz corresponds to DCDC1 = 1.275 V while 900 MHz corresponds to DCDC1 = 1.325 V:

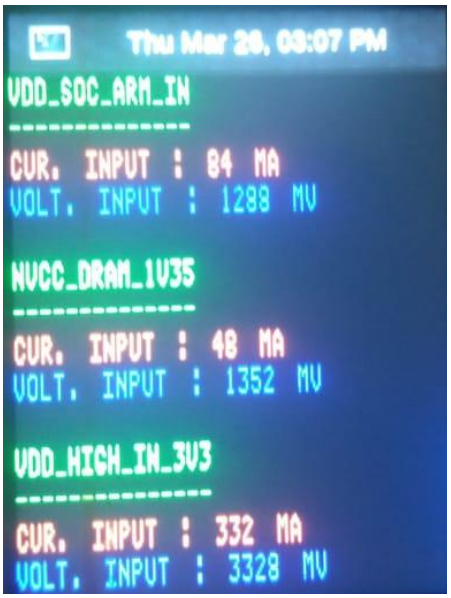
```
root@timx6y:~# echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
root@timx6y:~# echo 900000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
root@timx6y:~# echo 792000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
```

To run a current sensor application and measure the current on any rail coming out of the TPS6521815 PMIC, where "1" in the first prompt is current sensor IC #1, "1" in the second prompt is channel 1, and "*curr1_input*" returns a value of 248 mA that is being used by the VDD_ARM and VDD_SOC rails:

```
root@timx6y:~# test_currentsensor
Enter current sensor no[1-2]: 1
Enter voltage Level[1-3]: 1
/*************************************************************************/
/*                              CURRENT SENSOR2                          */
/*           Location of node:/sys/bus/i2c/devices/2-0040/hwmon/h1mon1/    */
/*************************************************************************/
/* ===================================================================== */
/*                             VDD_SOC_IN                                */
/* ===================================================================== */
      curr1_crit :  16380 mA
curr1_crit_alarm :  0
     curr1_input :  248 mA
       curr1_max :  16380 mA
 curr1_max_alarm :  0
       in1_input :  1104 mV
/*************************************************************************/
```

Alternatively, software has been written to set up the LCD screen and use it to display the real-time current monitoring information in addition to displaying the time configured in the real-time clock (RTC) supplied by the coin cell battery and the always-on power supply. Figure 32 shows the LCD screen during power-up, running color configurations tests, and displaying real-time current monitoring with labels and converted values.

Figure 32. Real-time Current Monitoring with LCD Screen



There are many other useful functions that are written specifically for testing TIDA-050043 in addition to the thousands of pre-defined Linux commands that can be included as part of the Yocto build for iMX. The most useful one for stress testing the processor and increase load current to test the PMIC is "stress-ng." More information on Linux commands can be found in the Ubuntu manual.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050043.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050043.

4.3 CAD Files

To download the CAD files, see the design files at TIDA-050043.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-050043.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050043.

5 Software Files

To download the software files, see the design files at TIDA-050043.

6 Related Documentation

1. Texas Instruments, *TPS6521815 User-Programmable Power Management IC (PMIC) With 6 DC/DC Converters, 1 LDO, and 3 Load Switches Data Sheet*
2. Texas Instruments, *Powering the NXP i.MX 6ULL, 6UltraLite with the TPS6521815 PMIC* Tech Note
3. *Evaluation Kit based on i.MX 6ULL* Quick Start Guide
4. *Ubuntu Manpage Repository*
5. *Yocto Project* home page

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