Test Report
For PMP15026

Inverting Buck-Boost Converter with variable output voltage using LM76003

2/16/2018

Table of Contents

Table of Figures

1. Design Specifications

V_{IN} Minimum	**3.5 VDC**
V_{IN} Maximum	**45 VDC**
V_{OUT}	**-5 to -15 VDC**
Switching Frequency	**500 kHz**

For the Buck-Boost converter, the relation between load current and average inductor current is as follows:

$$I_{OUT} = (1 - D) \times I_{L(avg)} \quad \text{(Equation 1)}$$

In Buck configuration, the average inductor current equals the average output current. For a Buck-Boost converter however, the inductor current is higher than the average inductor current.

The Duty cycle can be calculated by:

$$D = \frac{|Vout|}{Vin + |Vout|} \quad \text{(Equation 2)}$$

The design has a variable output voltage ranging from -5 V to -15 V. This is achieved by using the current injection method. The current injection method, changes the voltage drop occurring across the top feedback resistor (Rt), therefore varying the output voltage. The relation between the control voltage (Vctrl) and output voltage (Vo) can be expressed as below:

$$|Vo| = Vref - Rt * [\frac{Vctrl - Vbe}{Rctrl} - \frac{Vref}{Rb}] \quad \text{(Equation 3)}$$

Where Vbe is the drop across the base and emitter of the PNP transistor, Rctrl is the resistance at the emitter of the PNP transistor, Vref is the reference voltage of LM76003 (1V), Rb and Rt are the bottom and top resistances on the feedback loop respectively. As seen in equation 3, there exists a linear relation between the control voltage and output voltage. This is also shown in figure 1.

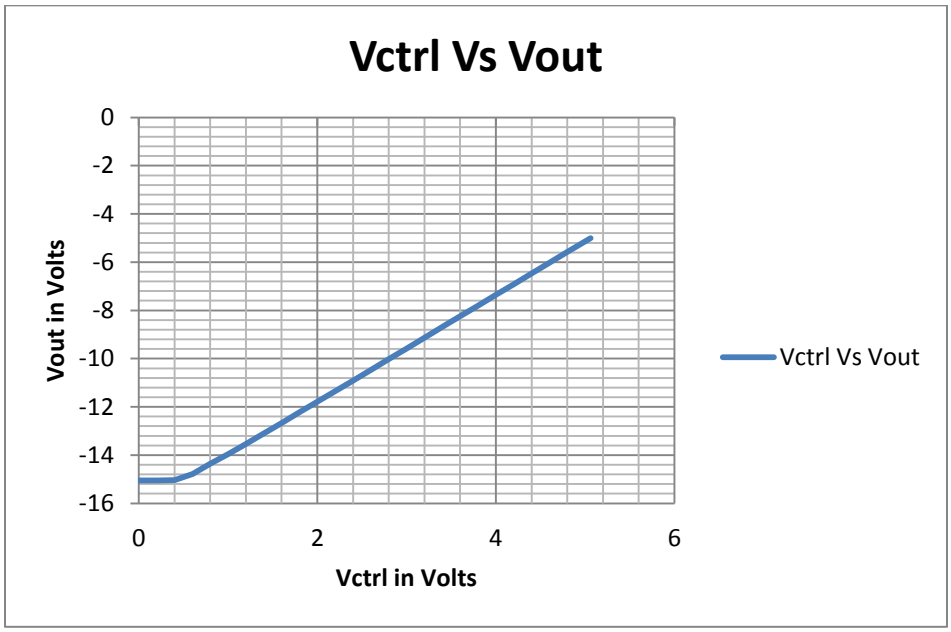

Figure 1 : Control voltage vs output voltage at input voltage of 24 V

As the reference level is negative due to the inverted buck-boost configuration, level shifters are used for the enable and sync functionalities. A jumper setting on the board helps to connect the enable to an external supply or connect them to the onboard rails. The enable pin can be connected to the input voltage and the sync to the ground reference of the design i.e. output in this case.

Keeping the input voltage constant and varying the output voltage, using equation 1, 2 and 3, the design is able to achieve different current limits at different output voltages. As for the boundary conditions, the design can achieve a max of 2 A at -15 V and 3 A at -5 V output voltage. The recommended output voltage levels should be maintained between -15 V and -5 V to achieve optimum efficiency from the design. However, the output voltage can be varied down to -1.5 V with a drop in the capability of the design to deliver output current up to 250 mA.

2. Circuit Descriptions

PMP15026 is designed in a Buck-Boost topology using the LM76003 which is a 3A, 60V synchronous buck regulator IC. The design accepts an input voltage in the range of 3.5 V to 45 V and provides a variable output voltage from -5 V to -15 V. The design is capable of supplying a maximum of 2 A load current with -15 V output voltage at 24 V input. This design was built on a 4-layer board (2 oz. Copper on Top and Bottom layers, 1 oz. Copper on two inner layers).

3. Schematic and PCB

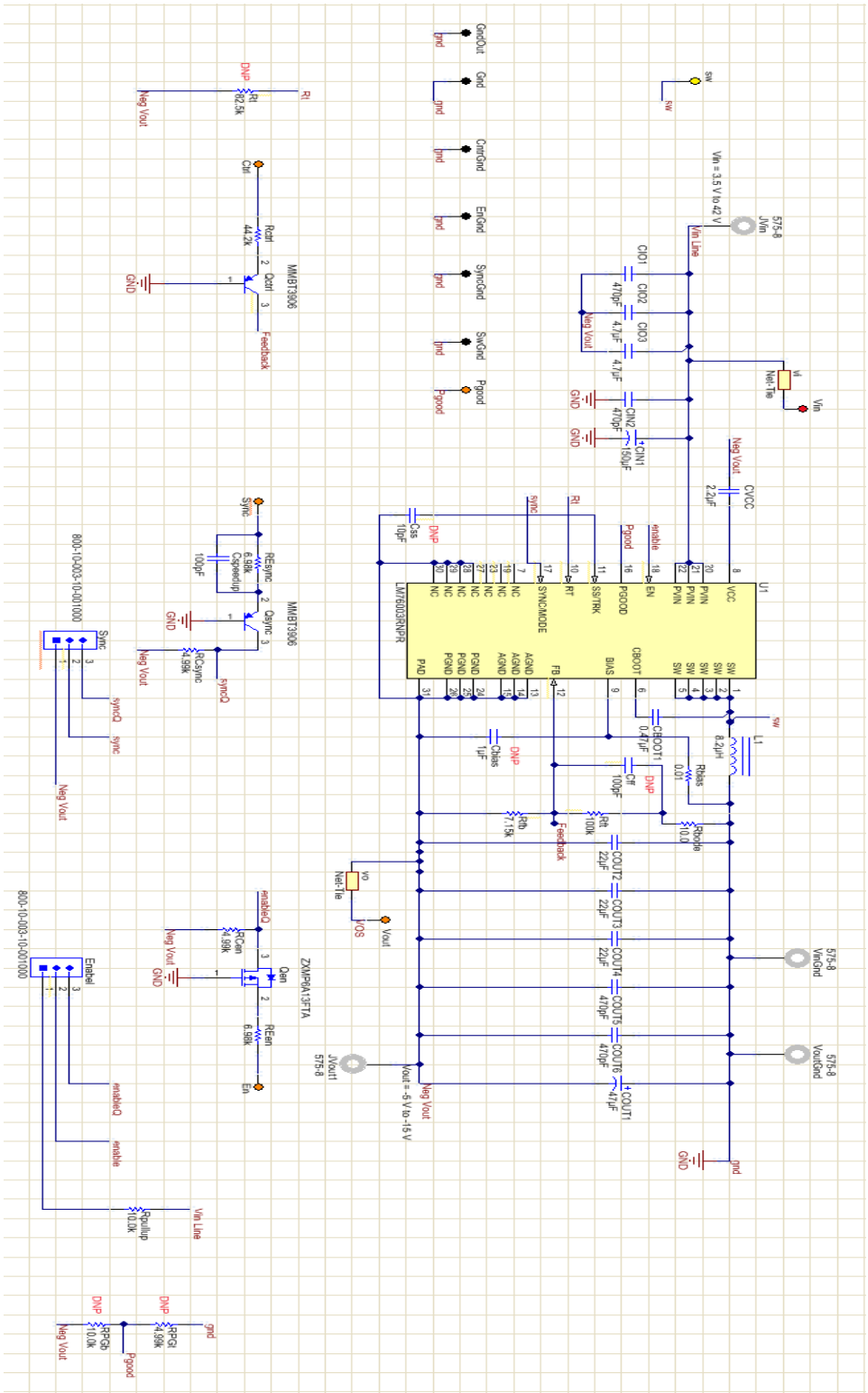

Figure 2: PMP15026 Schematic design

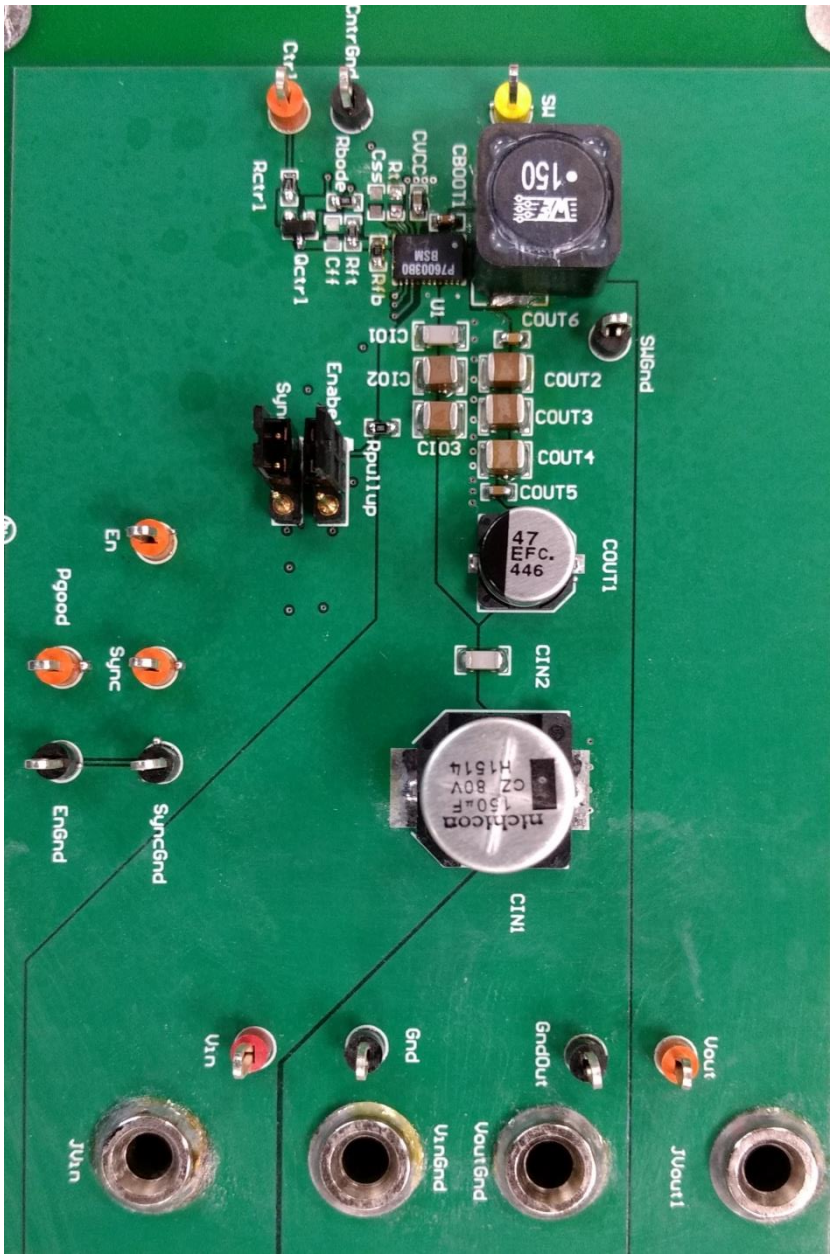

Figure 3 : PMP15026 PCB (Top)

Figure 4: PMP15026 PCB (Bottom)

4. Parametric Curves

4.1. Efficiency

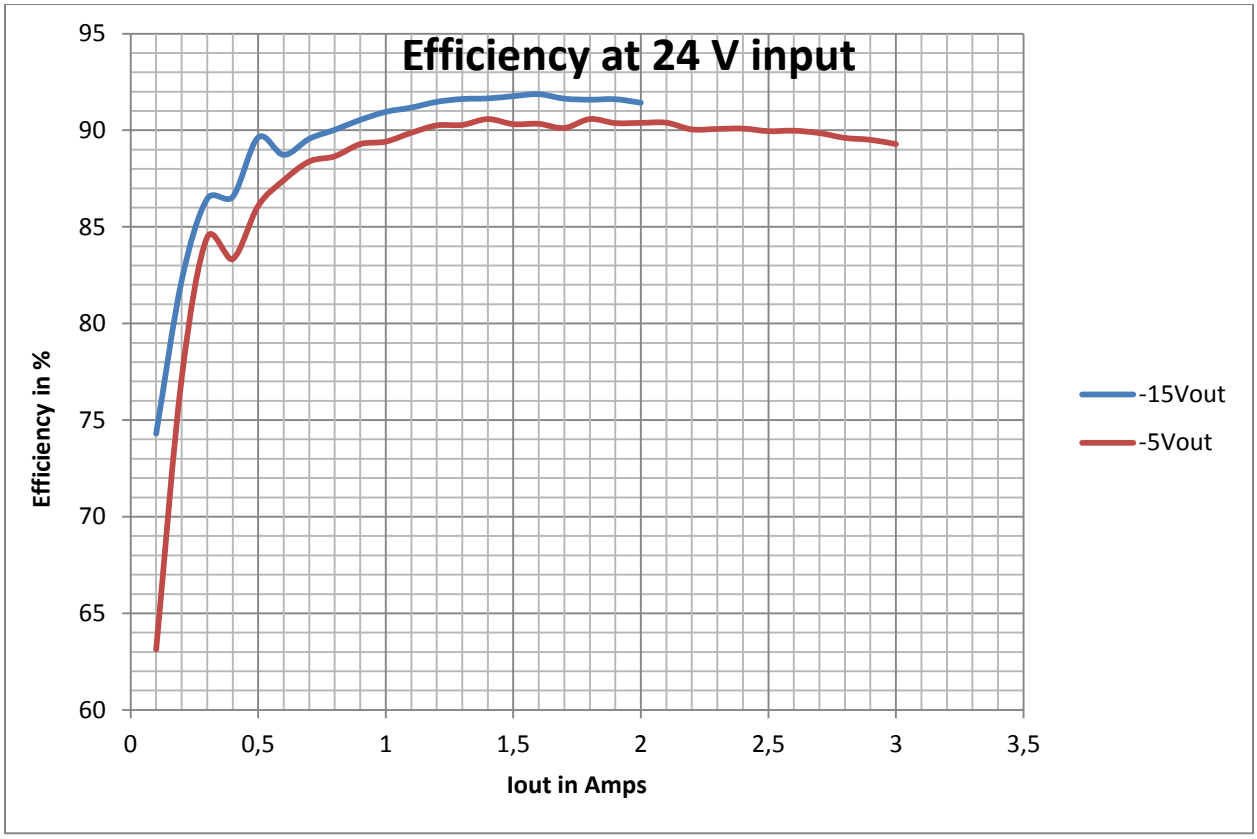

Figure 5: Efficiency Graph for PMP15026 at input voltage of 24 V (room temp)

Figure 5 shows the efficiency graph of the PMP15026 design. The design achieves a high efficiency of 92% when operated at 24 V input and -15 V output at 1.5A load current (room temp). The average efficiency of the design in CCM mode is 90%. Even at very light loads (200 mA), the design provides an efficiency of around 75%.

When operated with the same voltage operating conditions (24 V, room temperature) at a different output voltage i.e. -5 V output, the design achieves a maximum of 90% efficiency at 1.5 A load current. The average efficiency for the design in CCM with -5V output is around 88%.

4.2. Load Regulation

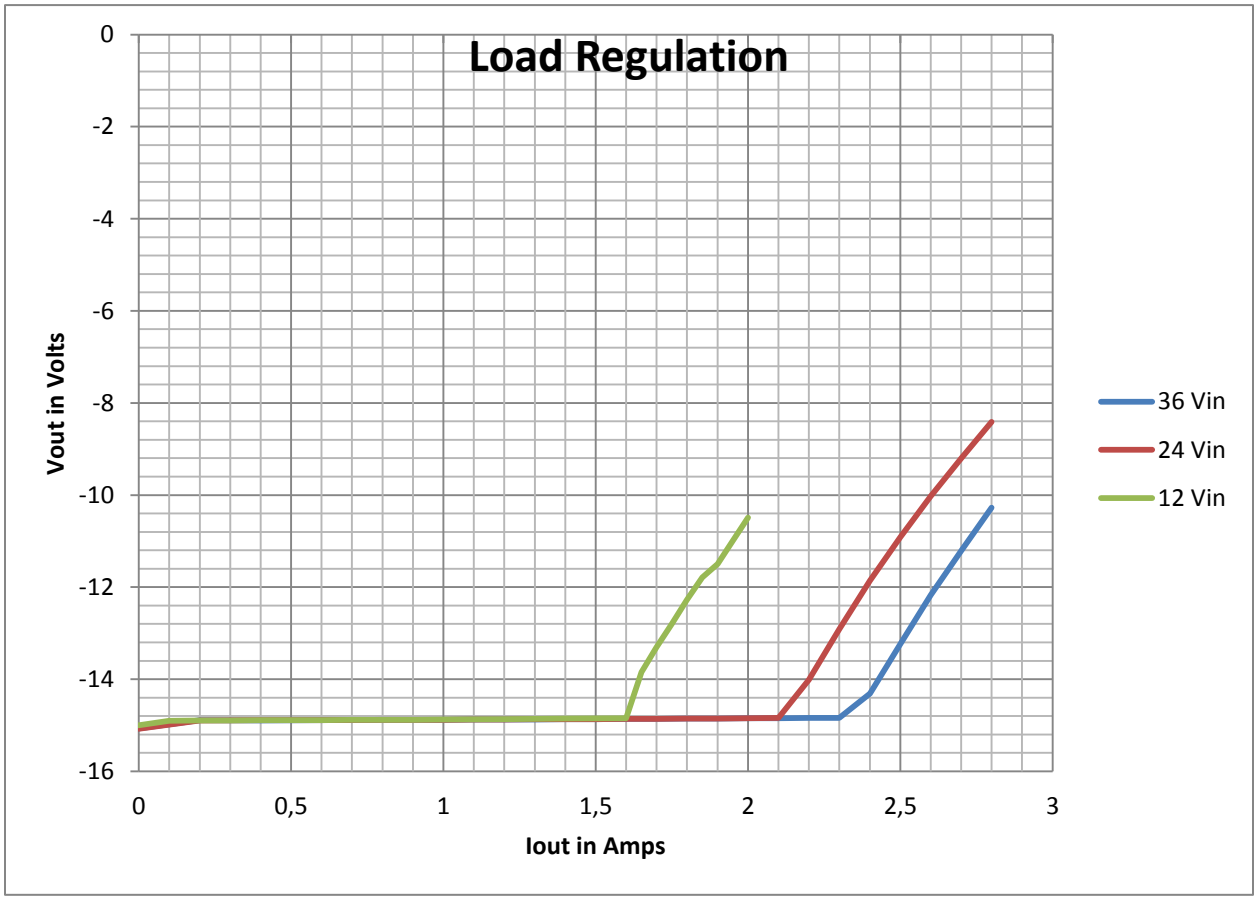

Figure 6: Load Regulation graph (room temp)

Load regulation can be defined as the capability of the device to maintain a constant output voltage when the load current is changed. As shown in figure 6, with higher input voltage, the range of the design to hold the output voltage increases. This happens because, at lower input voltages, the duty cycle is higher, thus reaching current limit condition earlier.

4.3. Line Regulation

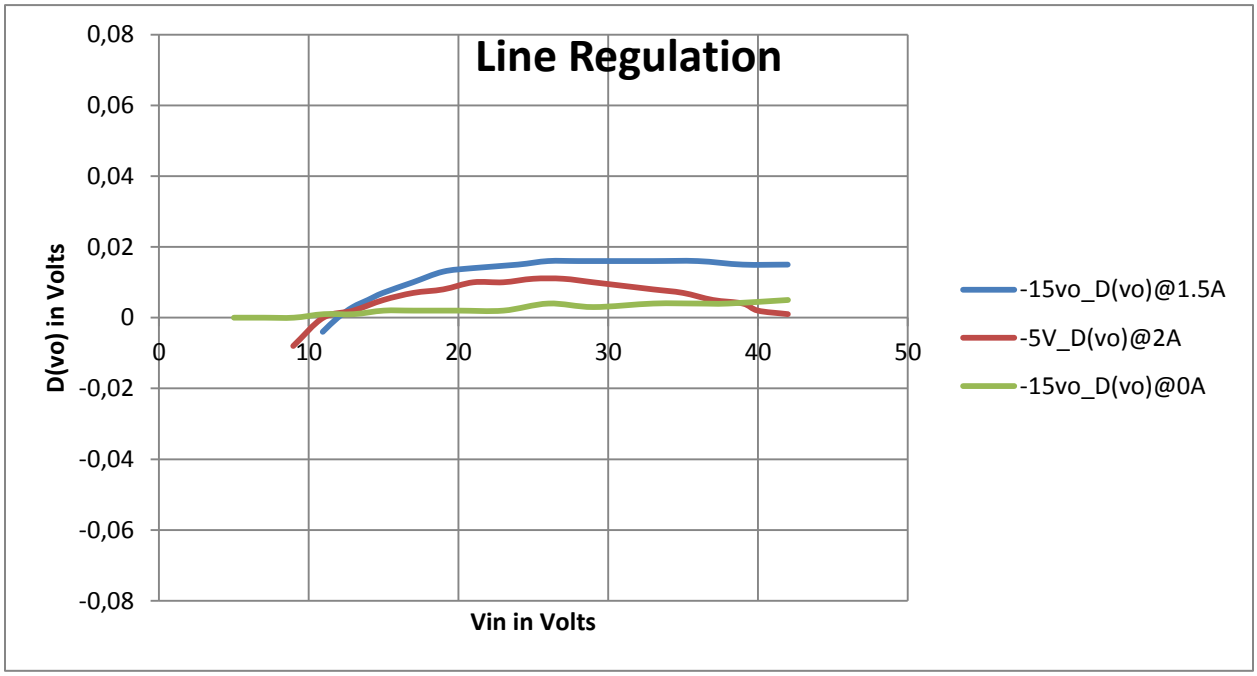

Figure 7: Line Regulation graph (room temp)

Line regulation can be defined as the ability of the device to maintain its output voltage with changes in input voltage. Figure 7 shows the line regulation performance of PMP15026 over its full operating range of input voltages. The Y axis is the deviation of output voltages with respect to its mean value. As it can be inferred from the graph, the line regulation of the device is less than 20mV over the voltage range of 25V to 45 V and the line regulation is very low for lower values of input voltages. When operating in no load condition, the deviation of the output voltage is less than 5mV.

4.4. Maximum Output Current

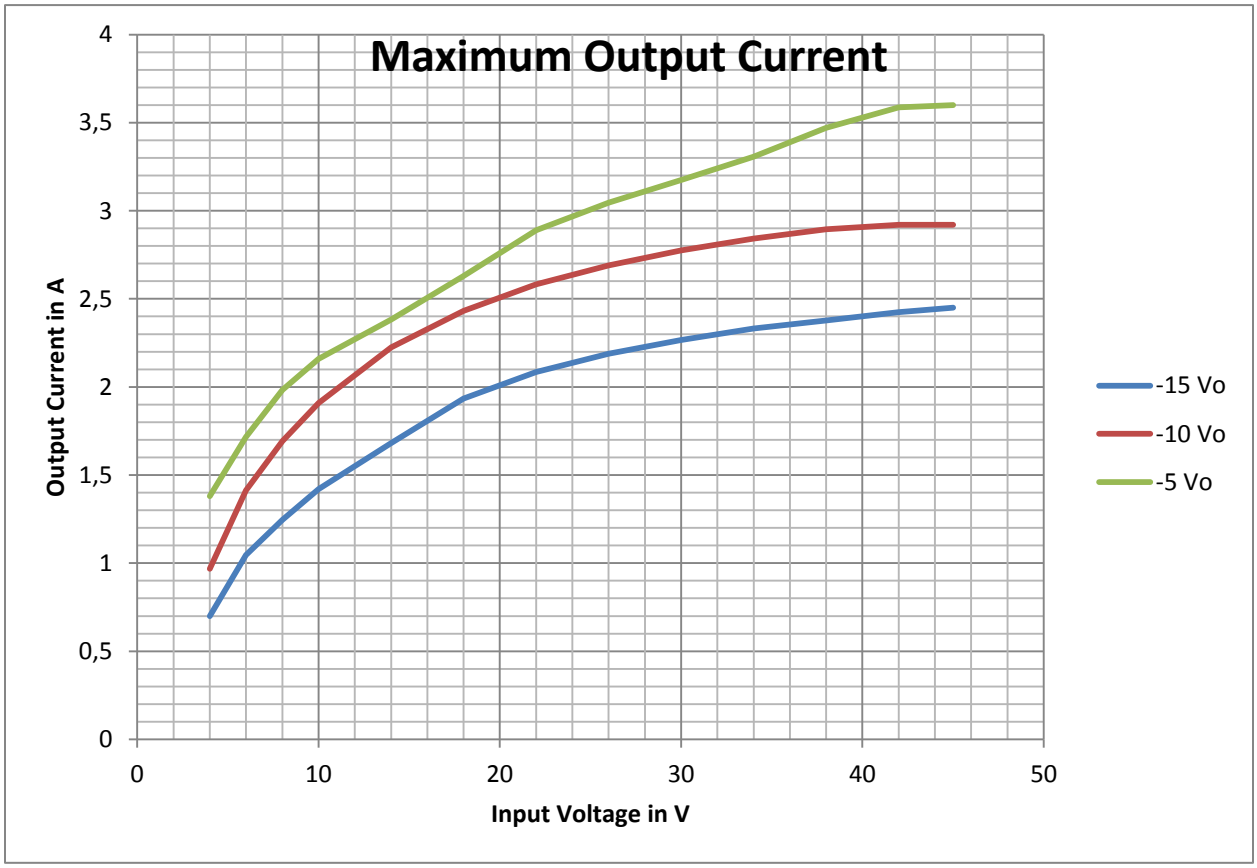

Figure 8: Maximum Output Current graph (room temp)

Figure 8 shows the range of the maximum load currents that the design can offer when operated with different output voltages. A maximum of 3 A can be reached with an output voltage of -5 volts. As the average inductor current is higher than the output current in a buck-boost topology, the ripple on the inductor current and the current limit on the inductor current define the limit on the average output current that can be delivered.

4.5. Thermal Data

Figure 9: IR thermal image taken at steady state with 24 VIN , -15 Vout and 0 A load (no airflow)

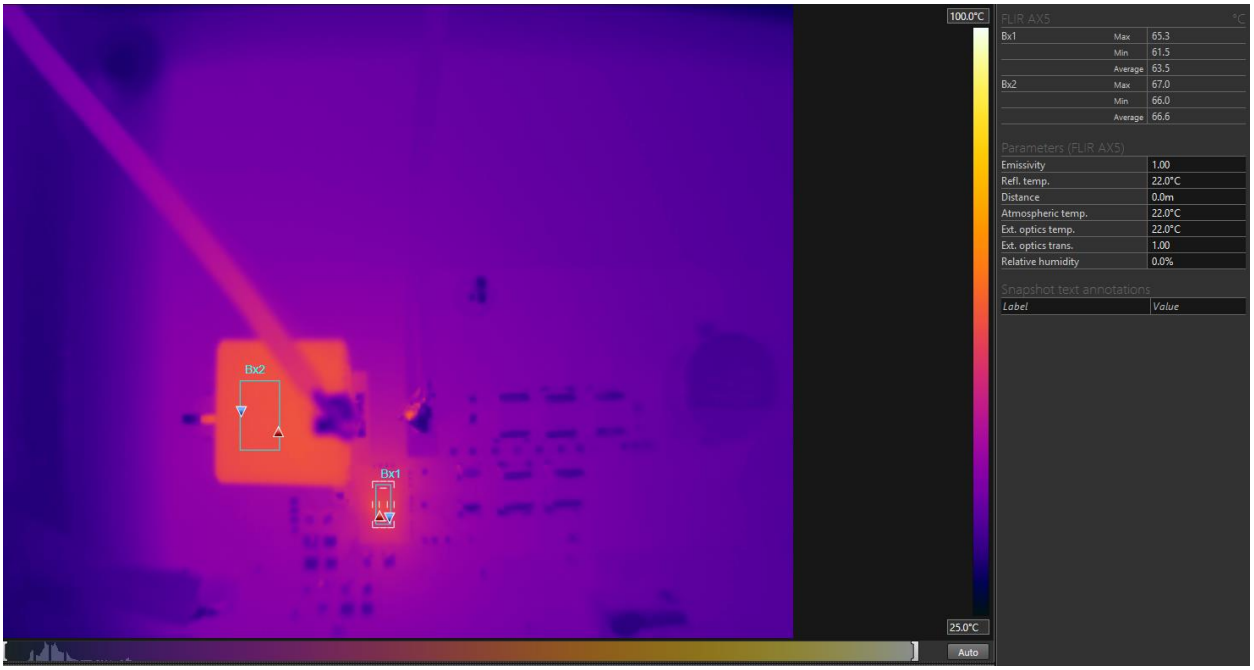

Figure 10: IR thermal image taken at steady state with 24 VIN , -15 Vout and 2 A load (no airflow)

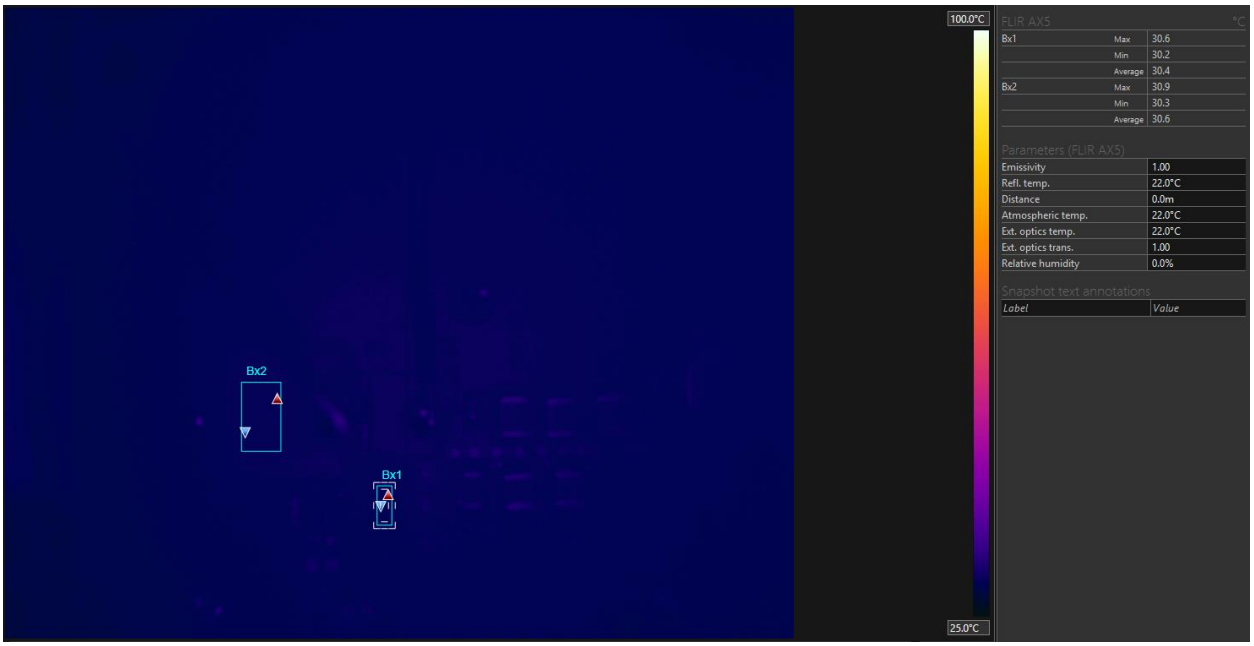

Figure 11: IR thermal image taken at steady state with 24 VIN, -5 Vout and 0 A load (no airflow)

Figure 12: IR thermal image taken at steady state with 24 VIN, -5 Vout and 3 A load (no airflow)

5. Waveforms

5.1. Steady State

Channel 2: Switch node voltage
Channel 3: Inductor Current
Channel 4: Output voltage ripple
Test Conditions: 24 V input, -15 V output, 500 KHz, no load condition

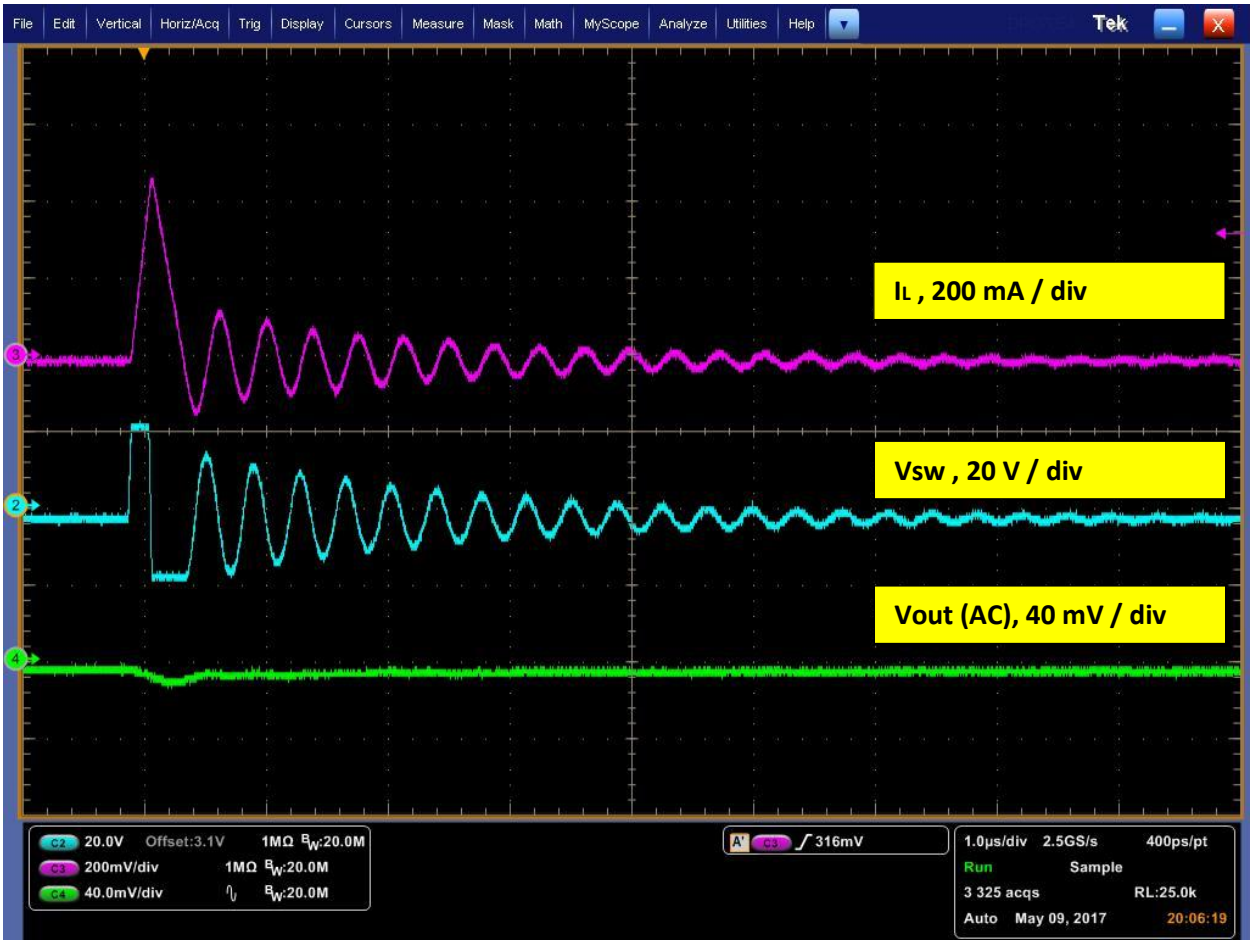

Figure 13: Steady State graph at -15V output and no load

Figure 13 shows minimal output voltage ripple at no load condition.

Channel 2: Switch node voltage
Channel 3: Inductor Current
Channel 4: Output voltage ripple
Test Conditions: 24 V input , -15 V output , 500 KHz, 1 A load

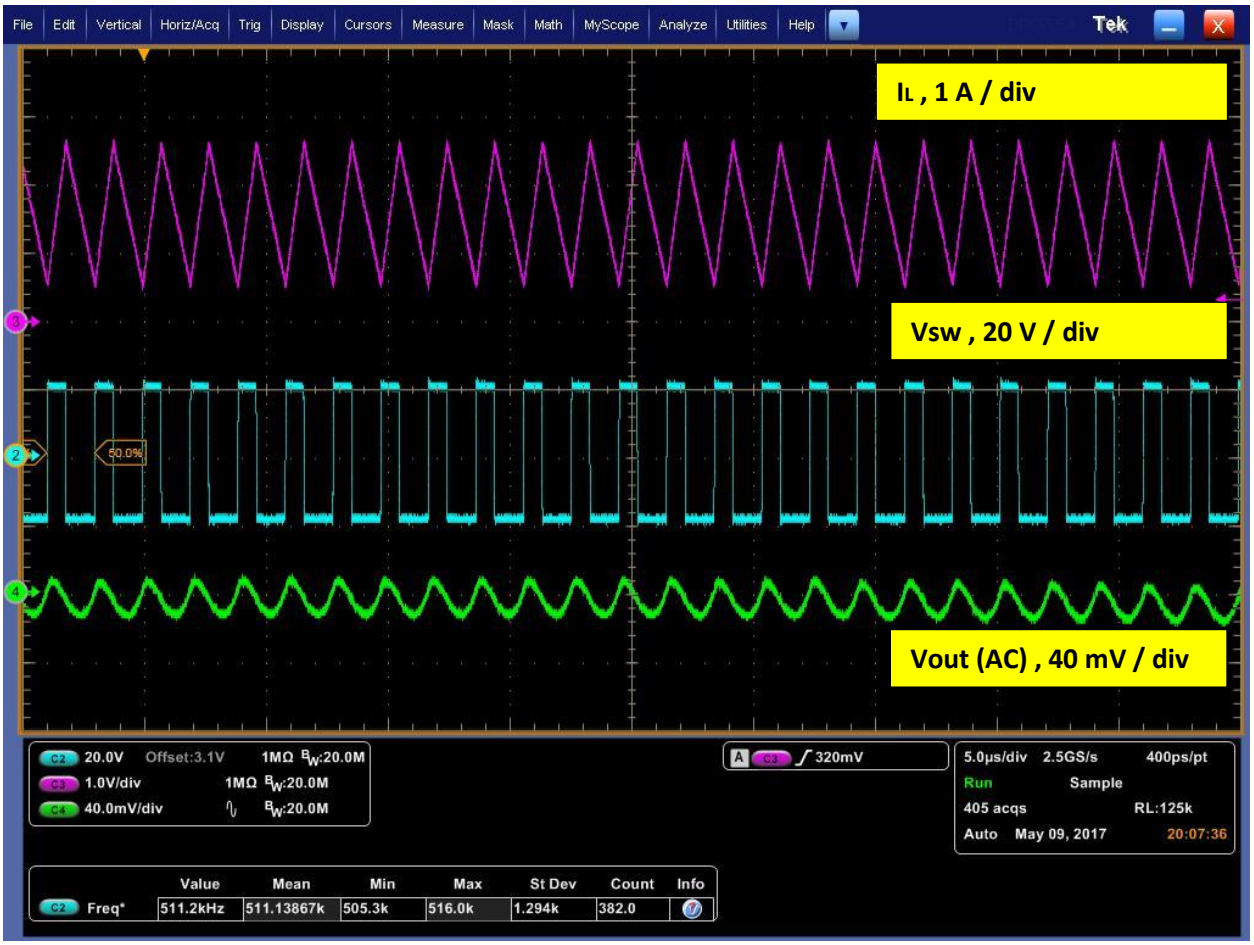

Figure 14: Steady State graph at -15V output and 1A load

In CCM mode, the output voltage ripple is less than 15 mV. The swing below the mean value in the switch node voltage seen in channel 2 is because of the inverting buck boost topology.

Channel 2: Switch node voltage
Channel 3: Inductor Current
Channel 4: Output voltage ripple
Test Conditions: 24 V input , -15 V output , 500 KHz, 2 A (full) load

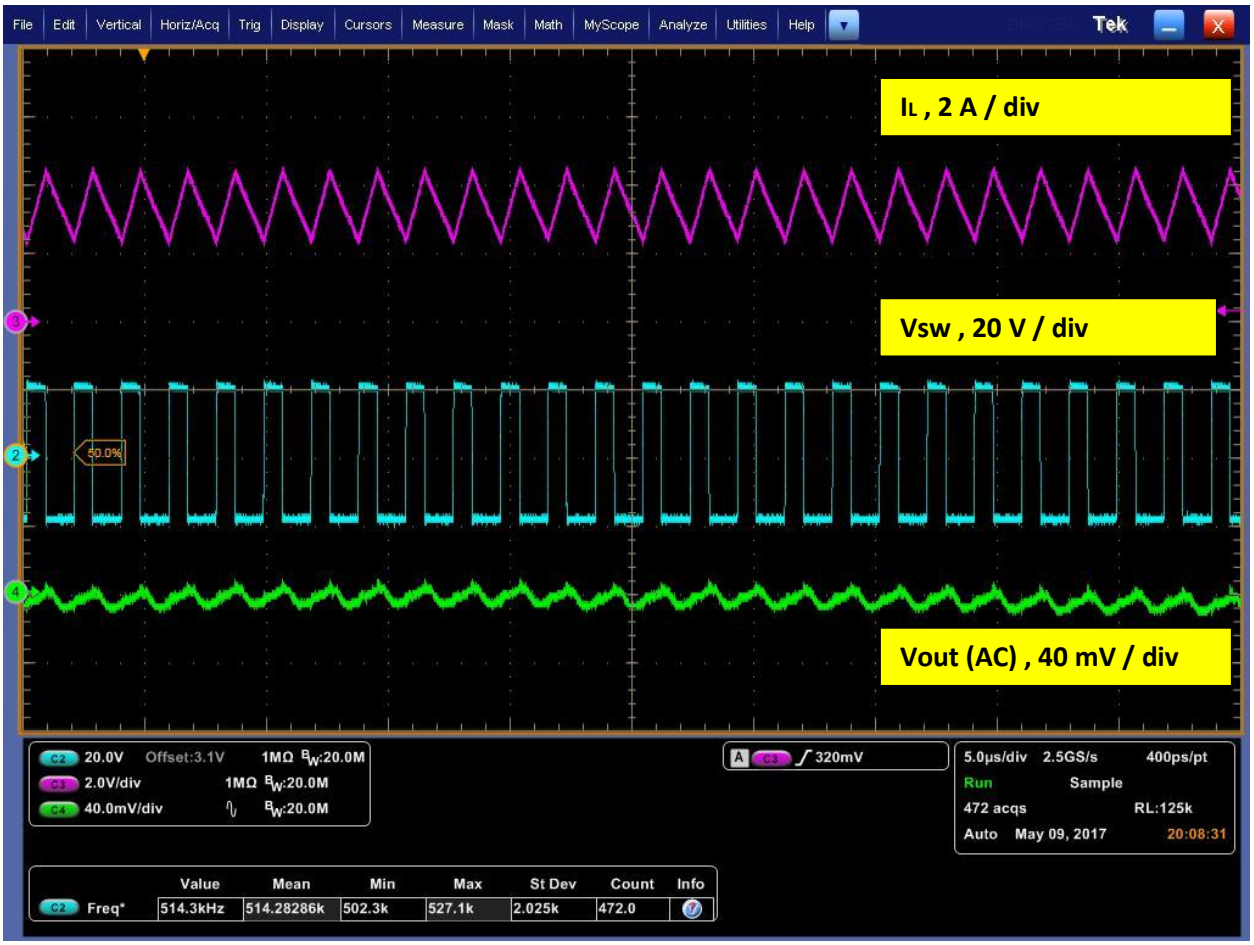

Figure 15: Steady State graph at -15V output and Full load

Channel 2: Switch node voltage
Channel 3: Inductor Current
Channel 4: Output voltage ripple
Test Conditions: 24 V input , -5 V output , 500 KHz, 0 A load

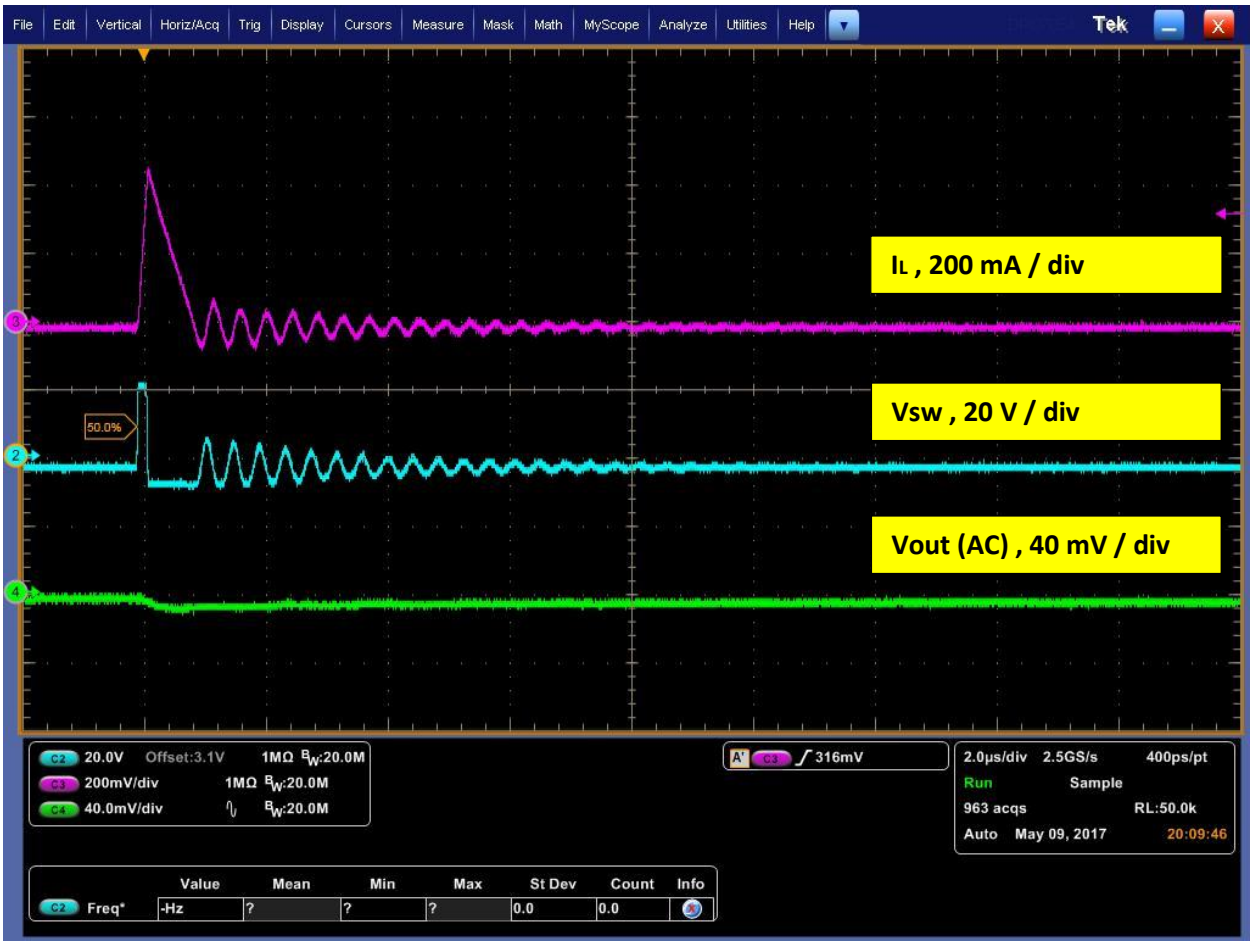

Figure 16: Steady State graph at -5V output and no load

Channel 2: Switch node voltage
Channel 3: Inductor Current
Channel 4: Output voltage ripple
Test Conditions: 24 V input , -5 V output , 500 KHz, 1 A load

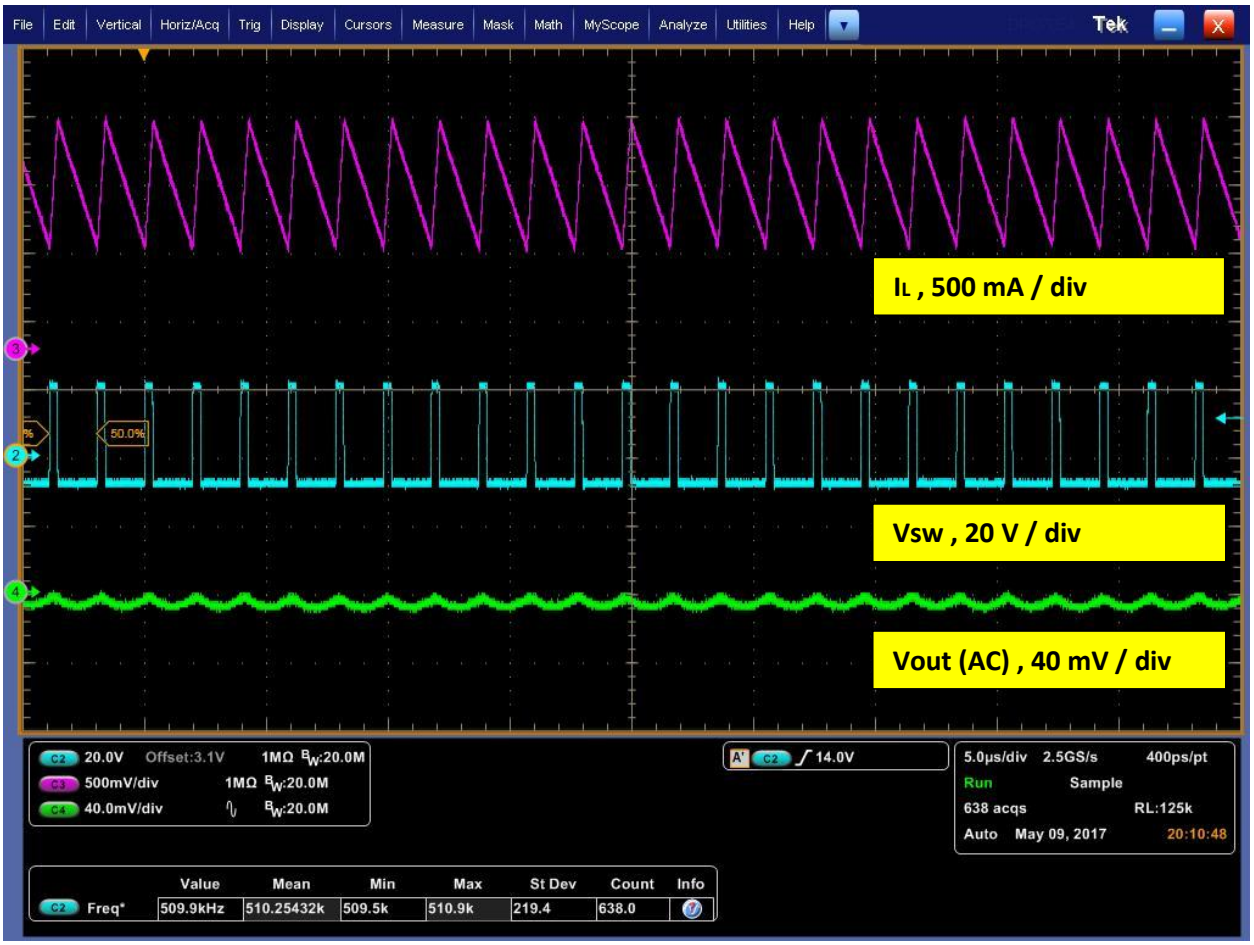

Figure 17: Steady State graph at -5V output and 1A load

Channel 2: Switch node voltage
Channel 3: Inductor Current
Channel 4: Output voltage ripple
Test Conditions: 24 V input , -5 V output , 500 KHz, 3 A (full) load

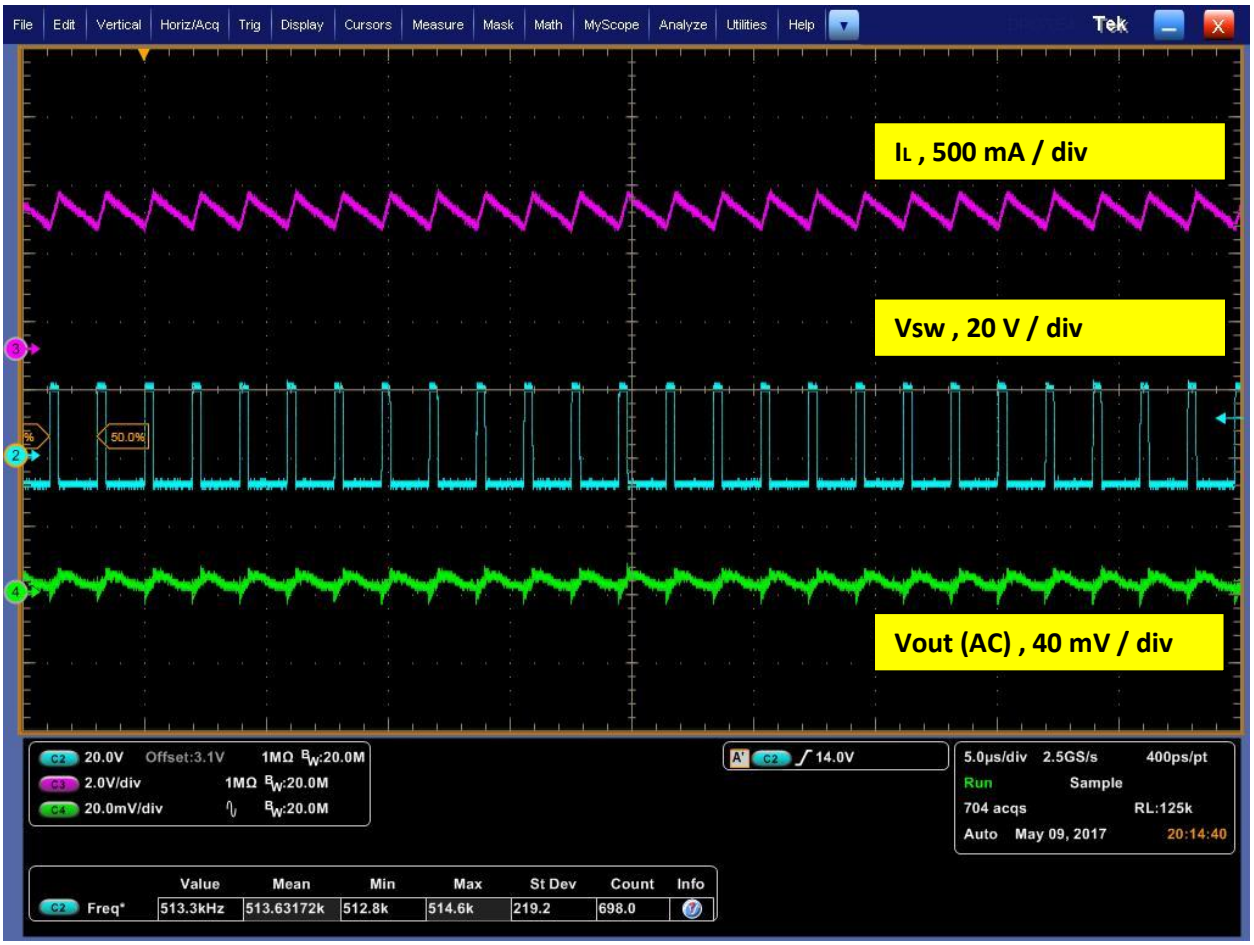

Figure 18: Steady State graph at -5V output and full load

5.2. Load Transient Response

Channel 2: Switch node voltage
Channel 3: Inductor Current
Channel 4: Output voltage transient
Test Conditions: 24 V input, -15 V output, 500 KHz, 0 A to 1 A load transient

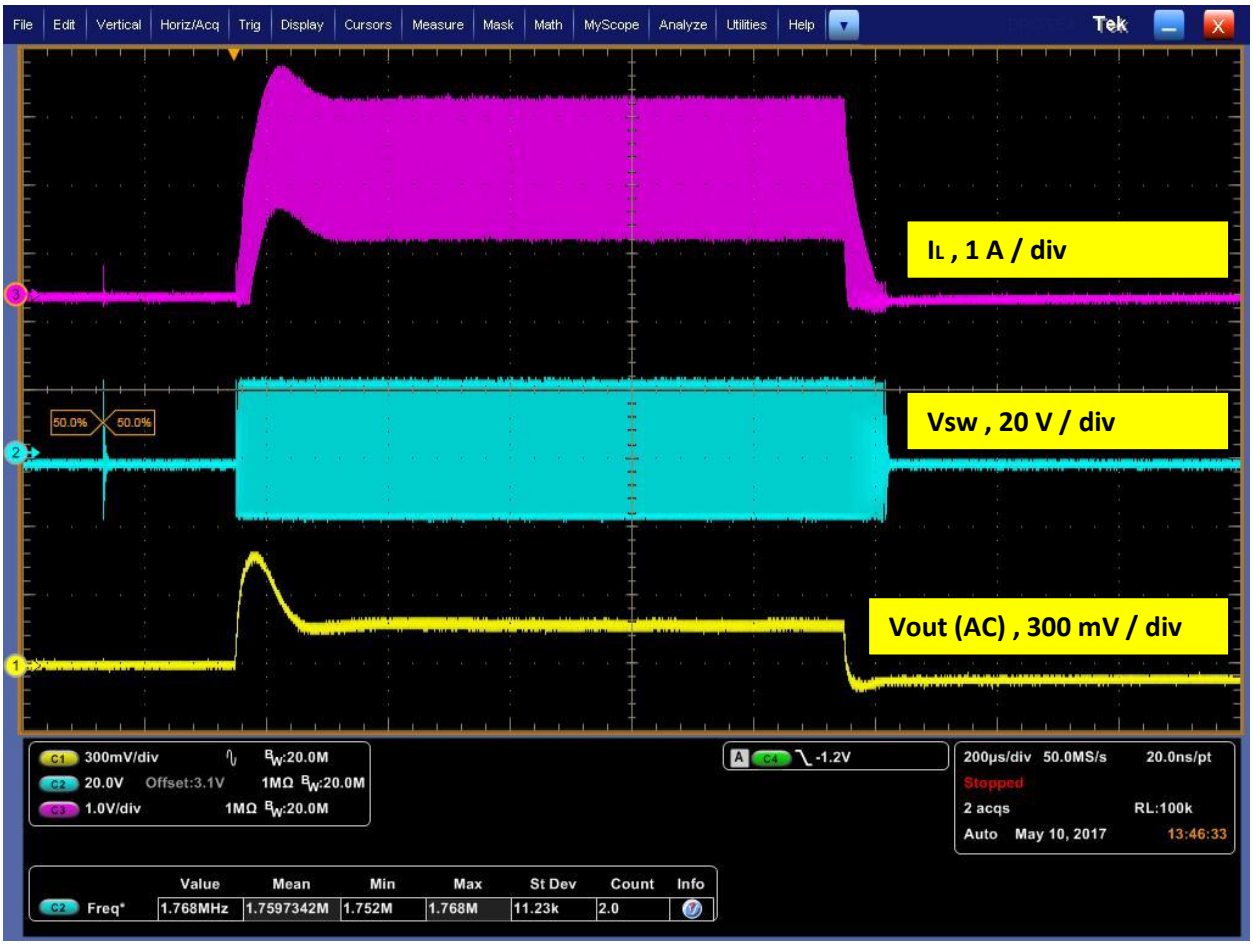

Figure 19: Load Transient response from no load to 1A load

The accepted voltage transient should be less than 5% of the output voltage. As seen in figure 19, the transient occurring when the load is changed from no load condition to full load condition is around 300 mV which is well within the accepted levels.

Channel 1: Output voltage transient
Channel 2: Switch node voltage
Channel 3: Inductor Current
Channel 4: Transient pulse
Test Conditions: 24 V input , -15 V output , 500 KHz, 0 A to 2 A load transient

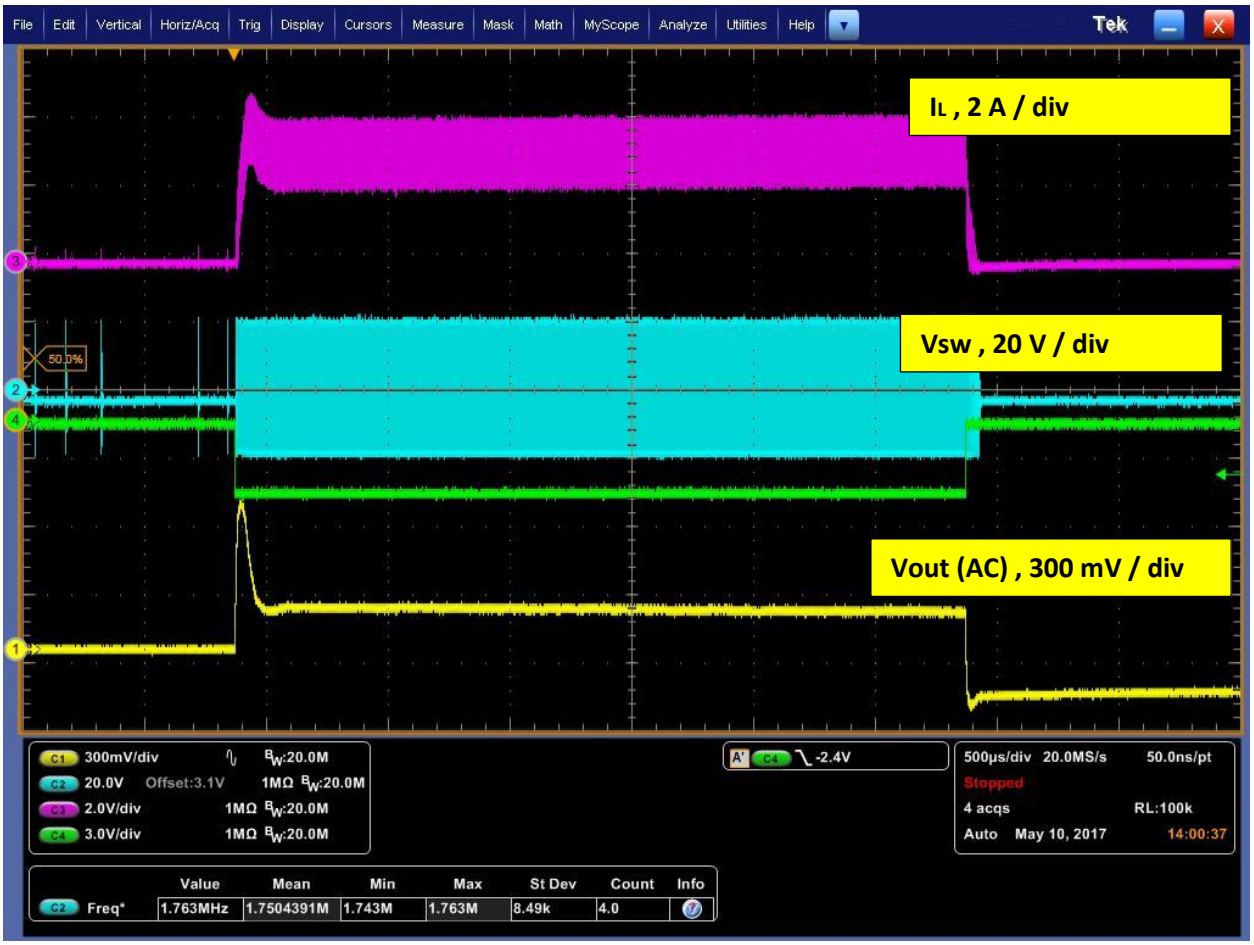

Figure 20: Load Transient response from no load to 2A load

Channel 2: Output voltage transient
Channel 3: Inductor Current
Test Conditions: 24 V input , -15 V output , 500 KHz, 0.2 A to 2 A load transient

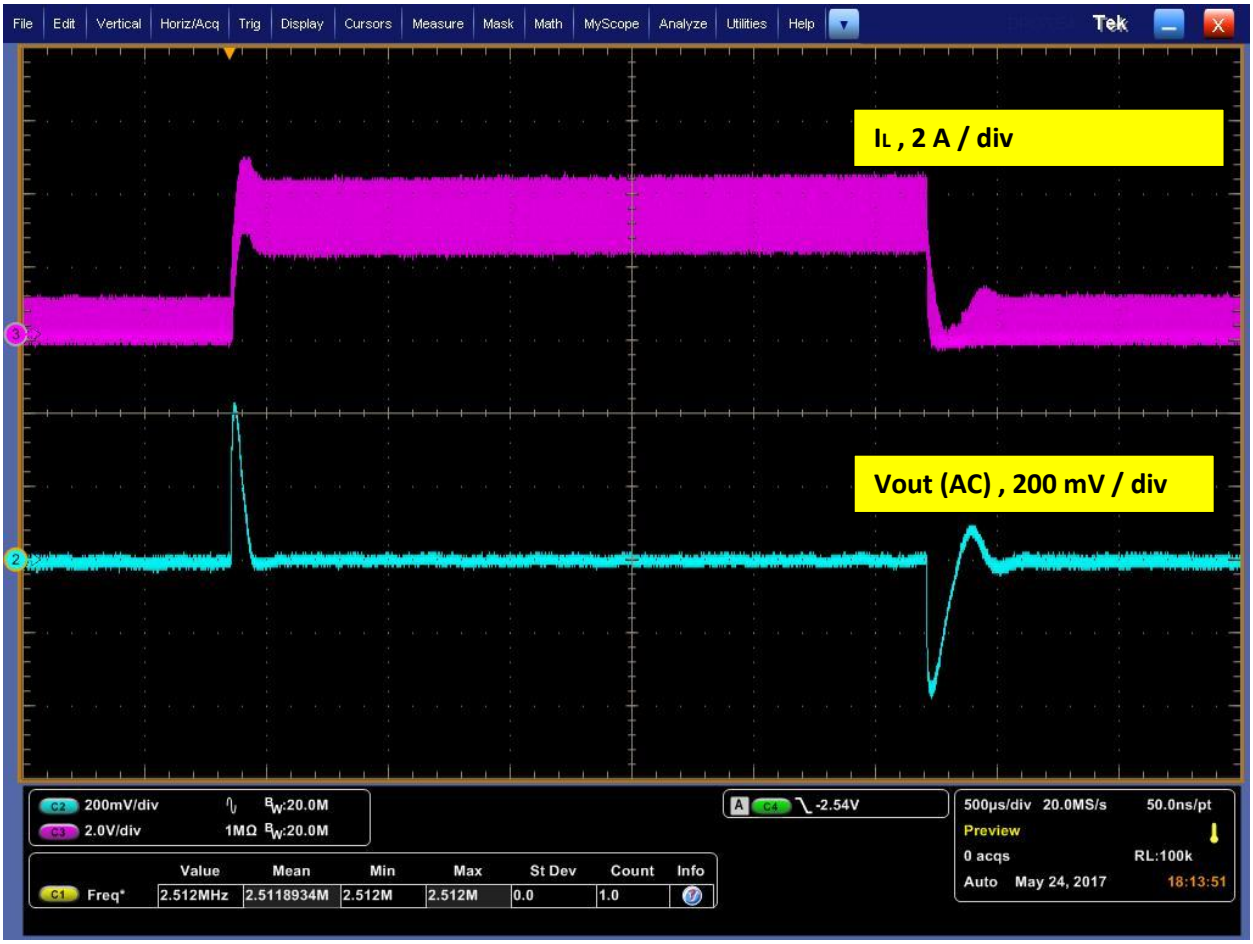

Figure 21: Load Transient response from light load to 2A load

5.3. Start up from Enable

Channel 1: Output voltage
Channel 3: Inductor Current
Channel 4 : Enable pulse
Test Conditions: 24 V input , -15 V output , 500 KHz, external enabled

Figure 22: Start up from Enable at -15V output

The startup test helps to understand the slow rising ramp at the output voltage. As can be seen in figure 22, channel 1 shows the increase in the output voltage from 0 to -15. The ramp helps the output capacitors to be charged slowly, thus not overdrawing charge from the input.

Channel 1: Output voltage
Channel 3: Inductor Current
Channel 4 : Enable pulse
Conditions: 24 V input , -5 V output , 500 KHz, external enabled

Figure 23: Start up from Enable at -5V output

5.4. Short Circuit and Recovery

Channel 3: Inductor Current
Channel 4: Output voltage
Conditions: 24 V input , -15 V output , 500 KHz

Figure 24: Short circuit response and recovery

The LM76003 uses a 'Hiccup' mode during short circuit condition. In this mode, the device switches for a certain number of cycles, trying to assess the presence or absence of a short circuit. If the short circuit condition is still present, the device switches off and tries to switch again after certain number of cycles. The device continues in this state while the short is present at the output. This behavior of the device can be seen in Figure 24.

5.5. Bode Plot

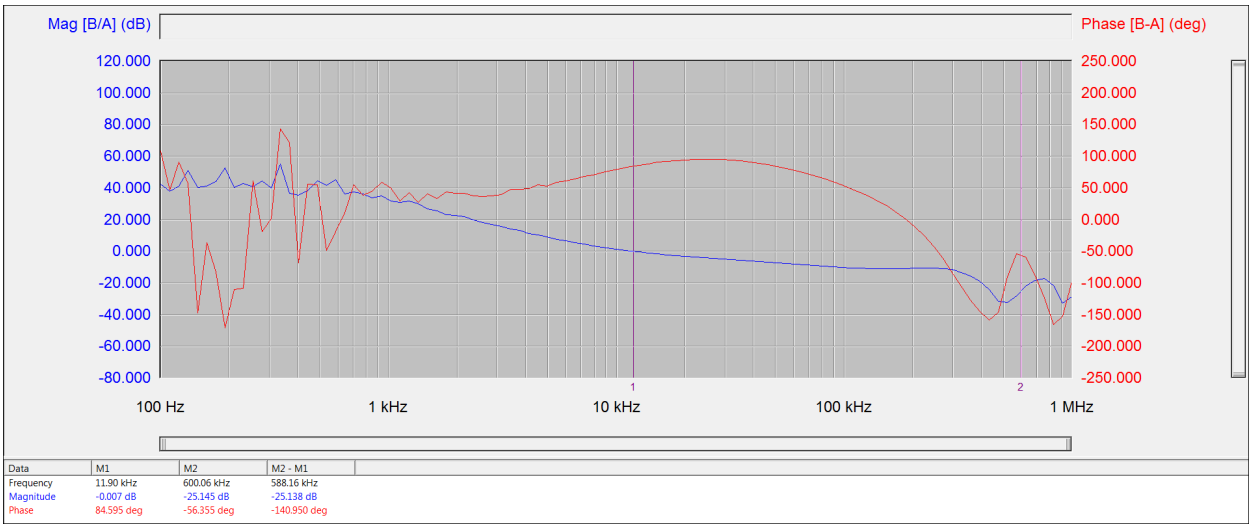

Figure 25: Loop response of PMP15026 with 45V input and -15V output @ 500KHz

The Bode plot of the device is illustrated in figure 25. The cross over frequency is 11.9 kHz and the phase margin is 84.6 degrees. The cross over frequency can be adjusted slightly by adjusting the values of the output capacitor, inductor and the feed forward cap (Cff). The measurements shown in figure 25 are made with a 15 uH inductor, 115 uF output capacitor (cumulative) and no feed forward capacitor.

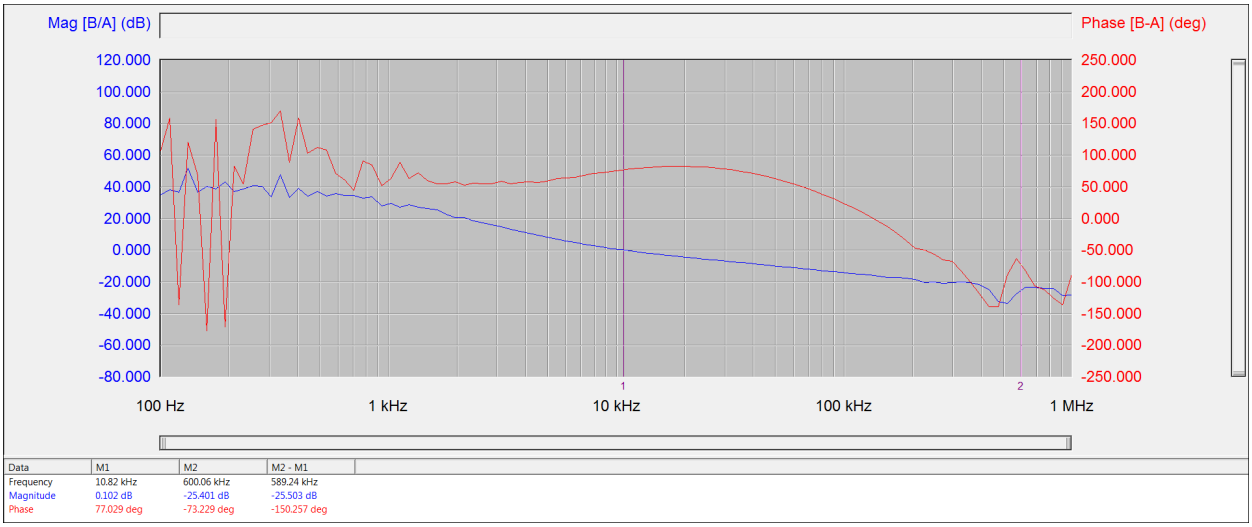

Figure 26: Loop response of PMP15026 with 45V input and -5V output @ 500KHz

6. Application

A negative output power regulator finds its applications in many fields. For example, it is used for power amplifiers used in the field of Audio. The power amplifiers require a dual rail input to amplify the input signal. A negative rail also finds applications in Line drivers, receivers and instrumentation amplifiers. Similar applications can be found in the field of Telecommunication and imaging devices etc.

7. Conclusion

PMP15026 demonstrates the ability of LM76003 to be configured as an inverting buck boost converter showcasing its high performance. The efficiency of the design is around 89%. The voltage transient and the output voltage ripple stay within the margins. The level shifters used for enable and sync signals work as per expectation.

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