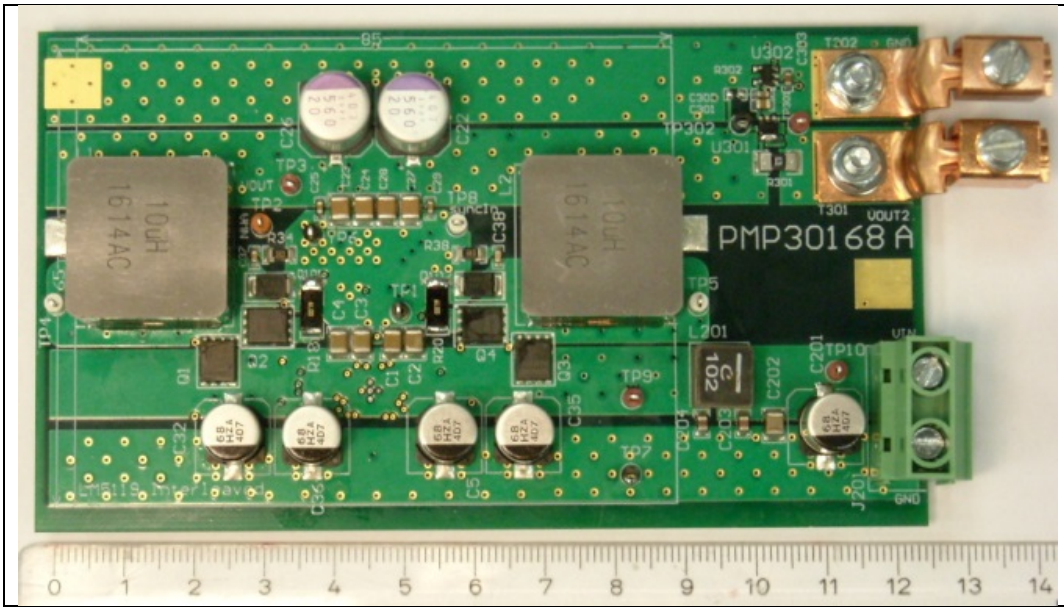
# PMP30168RevB Test Results



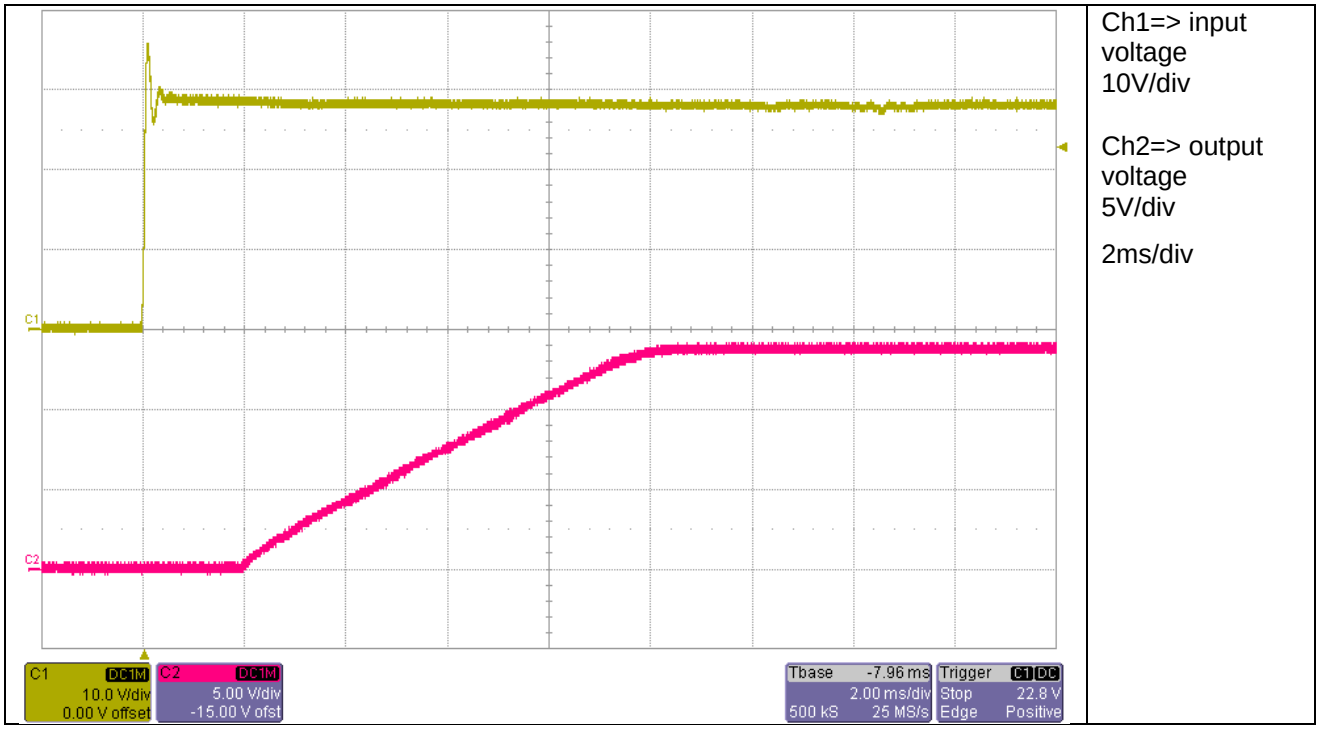
Topology: Synchronous Two Phase Interleaved Buck Converter
Device: LM5119
Unless otherwise mentioned the output current was set to 20A (with electronic load) at 14 volt output, and the input voltage set at 28V; measurements done w/ convectional cooling

Design has been tested here w/ inductors Vishay IHLP8787 for best efficiency,
so dimensions of power stage are 85mm x 65mm:



# 1 Startup

The startup waveform is shown in Figure 1, soft start 8ms. UVLO: ON at 21.9Vin / OFF at 17.1Vin




Ch1=> input voltage 10V/div

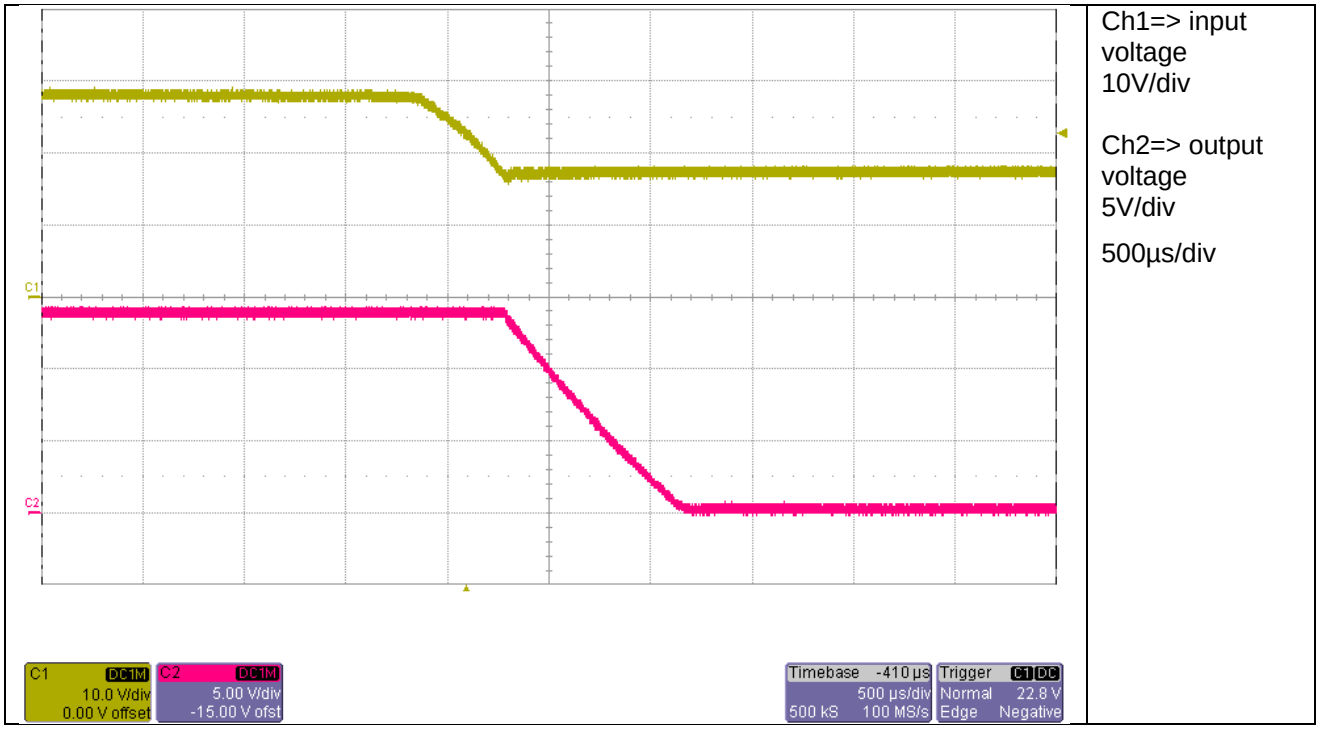
Ch2=> output voltage 5V/div

2ms/div

**Figure 1**

# 2 Shutdown

The shutdown waveform is shown in Figure 2.




Ch1=> input voltage 10V/div

Ch2=> output voltage 5V/div

500µs/div

**Figure 2**

# 3 Efficiency

The efficiency and the power losses are shown in the Figure 3 below, max. load 20Amps/280W

The measurements have been conducted for the pure power stage, without input filter and output current measurement shunt. Efficiency curve is flat, **in between 6A to 20A >97% efficiency**:

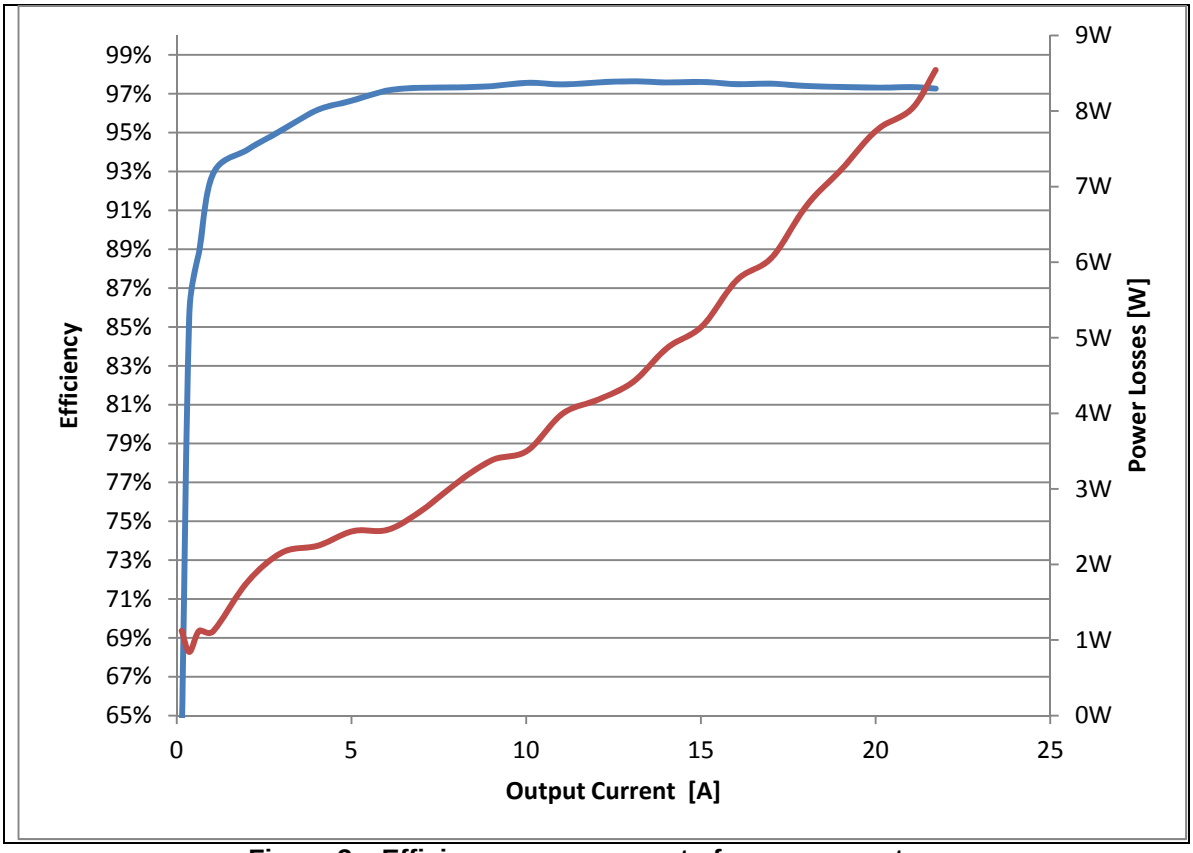



**Figure 3 – Efficiency measurement of pure power stage**

## 4 Load Regulation

The load regulation of the output is shown in Figure 4 below, **deviation 2mV**.

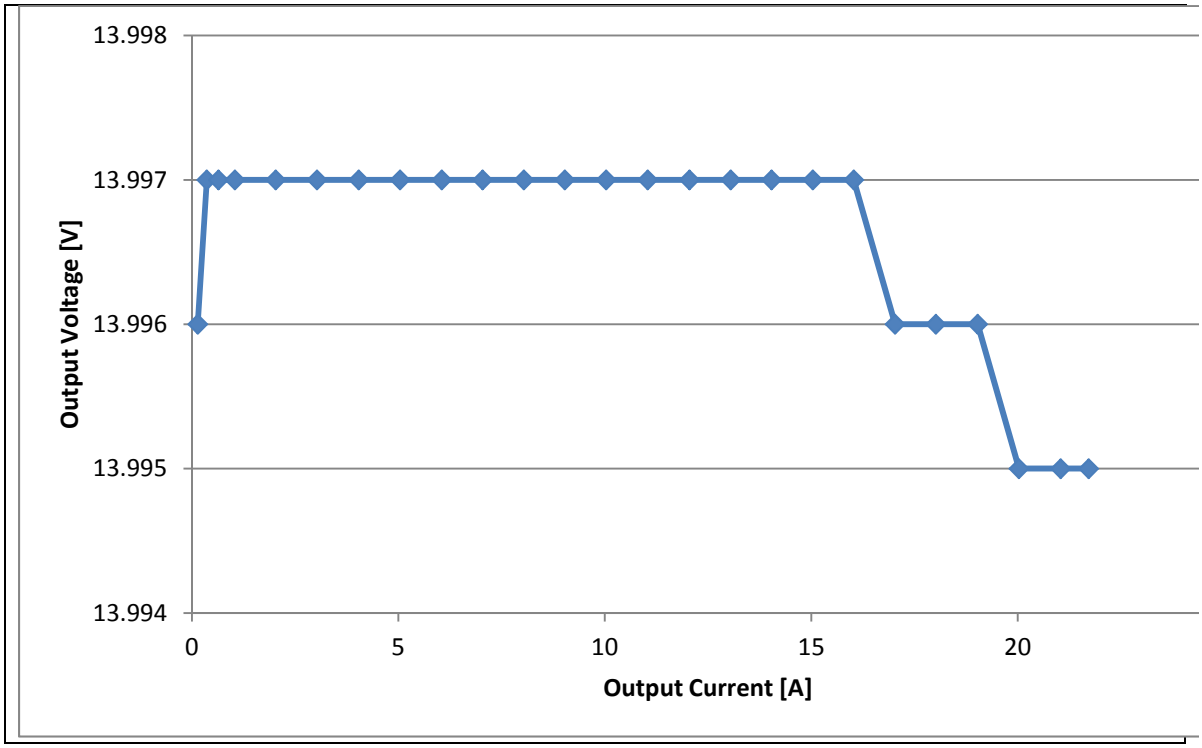
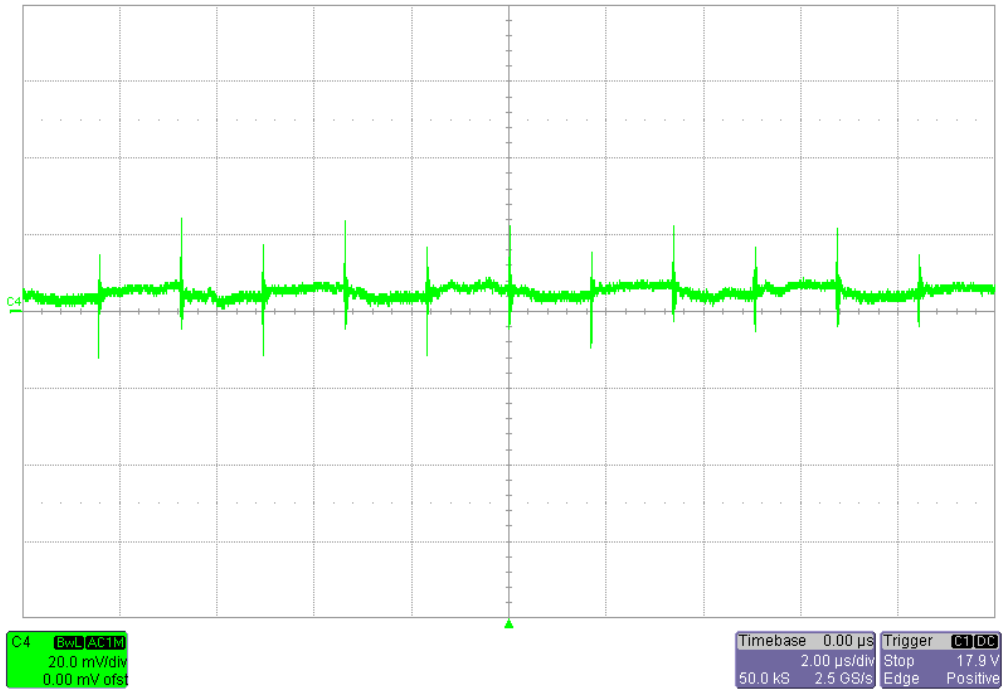



**Figure 4 – Efficiency**

## 5 Output Ripple Voltage

The output ripple voltage is shown in Figure 5, **ripple <10mVpp, noise around 20mVpp**.




Ch1 => output voltage 1 20mV/div

AC coupled

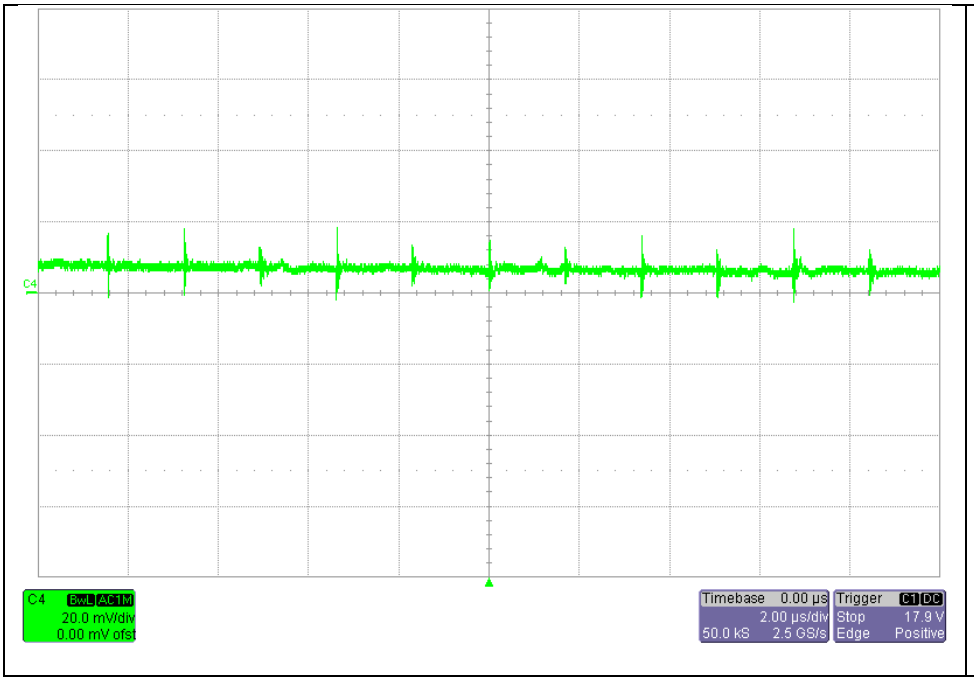
20MHz bw

2µs/div

**Figure 5**

## 6 Input Ripple Voltage

The filtered input ripple voltage is shown in Figure 6, and the unfiltered input ripple voltage is shown in Figure 7 – **input filter reduces reflected noise 600mVpp to 20mVpp**.



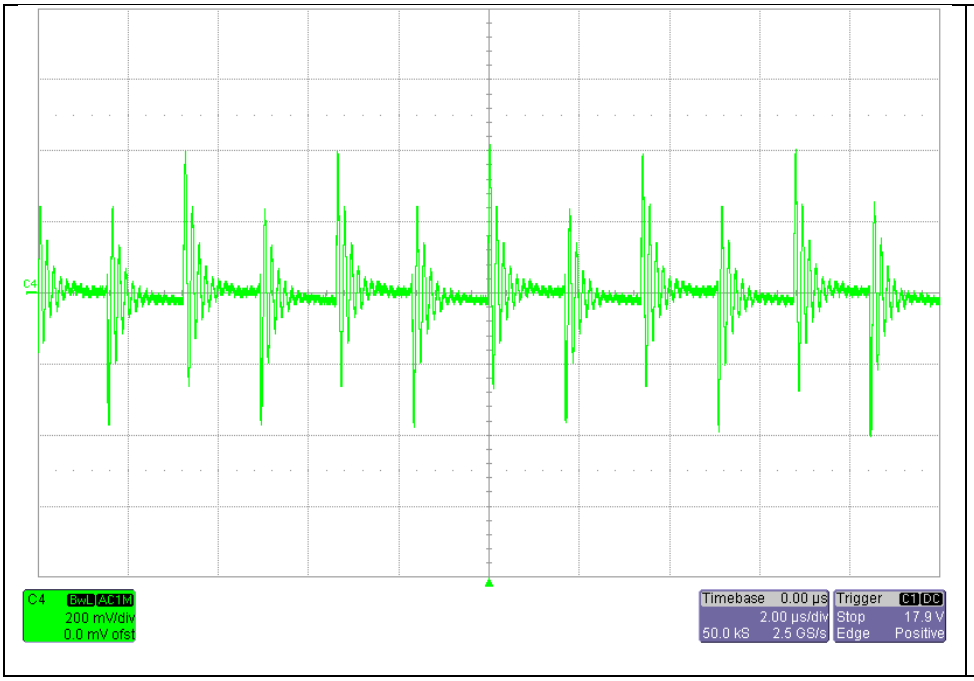

Ch1 => input voltage
20mV/div

AC coupled

20MHz bw

2µs/div

**Figure 6**




Ch1 => input voltage@8Vin
200mV/div

**w/o input filter**

AC coupled

20MHz bw

2µs/div

**Figure 7**

## 7 Control Loop Frequency Response

Figure 8 shows the loop response at full load current of 20A and nominal input voltage of 28V. Dynamic performance has been squeezed to max. capability of error amplifier:

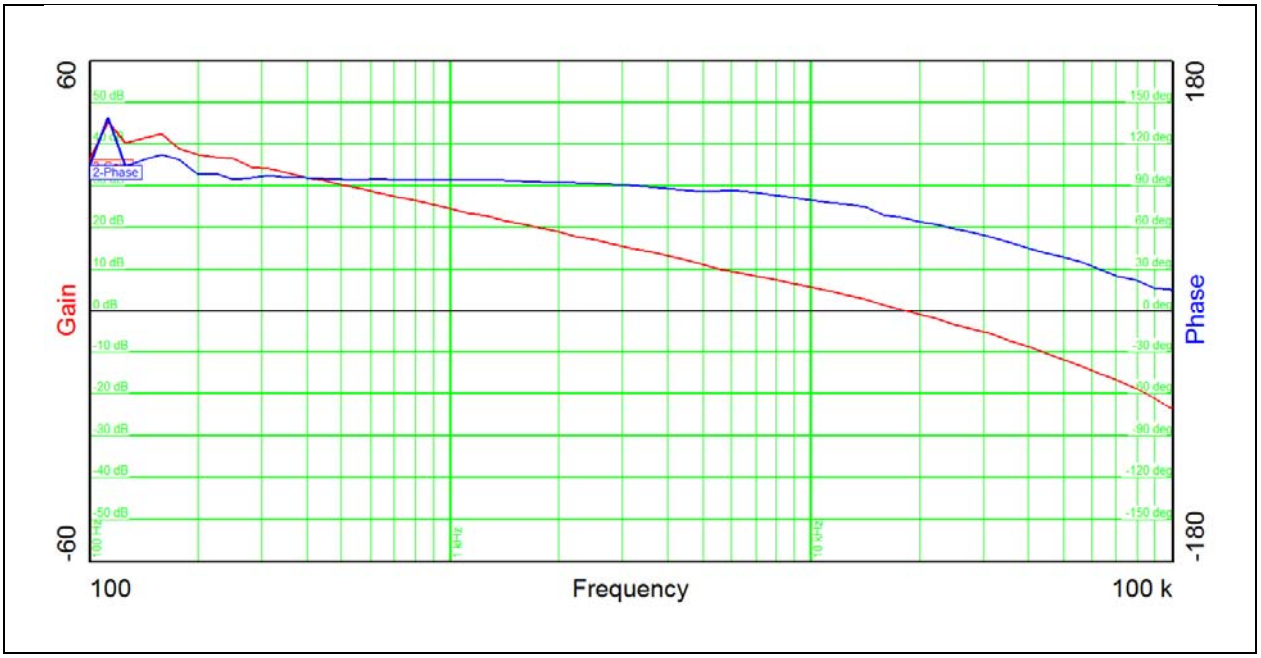


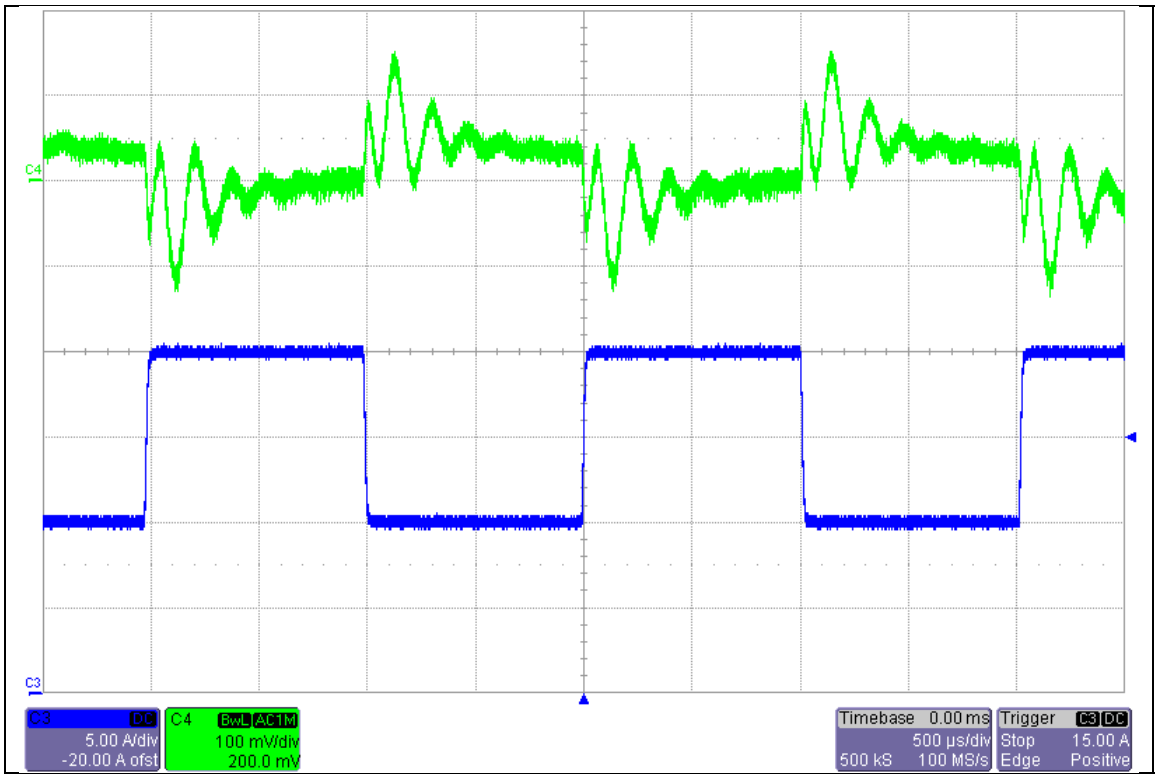

**Figure 8**

| | |
|---|---|
| **Bandwidth (kHz)** | 18.15 |
| **Phase margin** | 66.35° |
| **slope (20dB/decade)** | -1.15 |

**Table 1**

## 8 Load Transient Response

The load transient response from a load step from 10A to 20A is shown in Figure 9.




Ch4 => output voltage
100mV/div
AC coupled
20MHz bw

Ch3=> output current
5A/div

500us/div

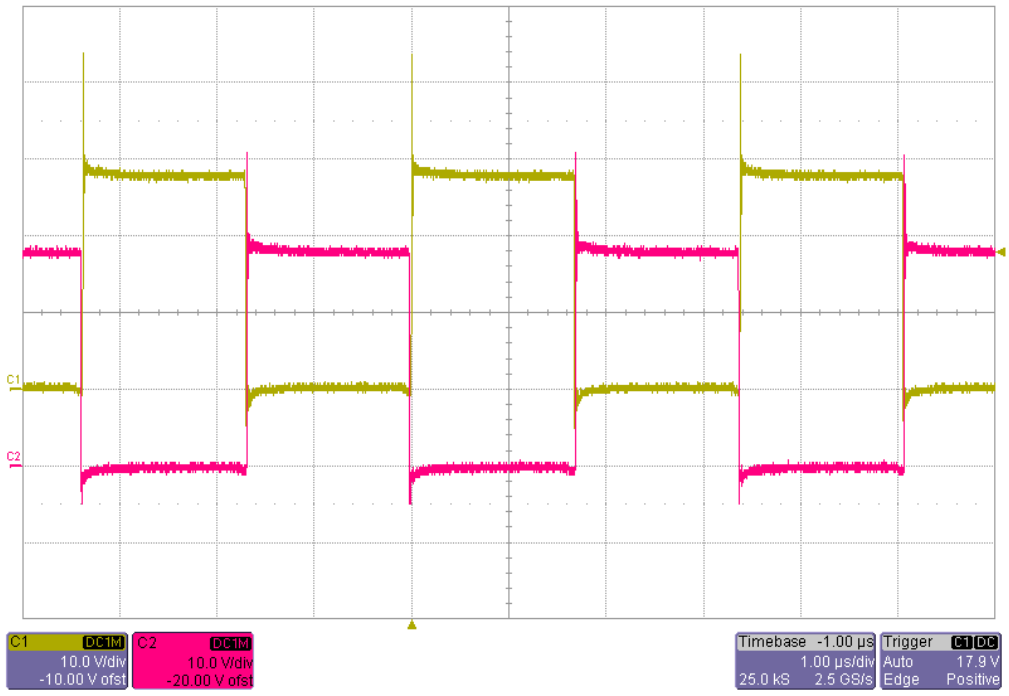
**Figure 9**

*The deviation for 50% load step is around 150mVpk, so voltage drop is slightly above 1%.*

# 9 Miscellaneous Waveforms

## *9.1 Interleaving*

Figure 10 shows the interleaving of the two power stages, measured with standard probes.




Ch1 => SW1
10V/div

Ch2 => SW2
10V/div

DC coupled

full bw

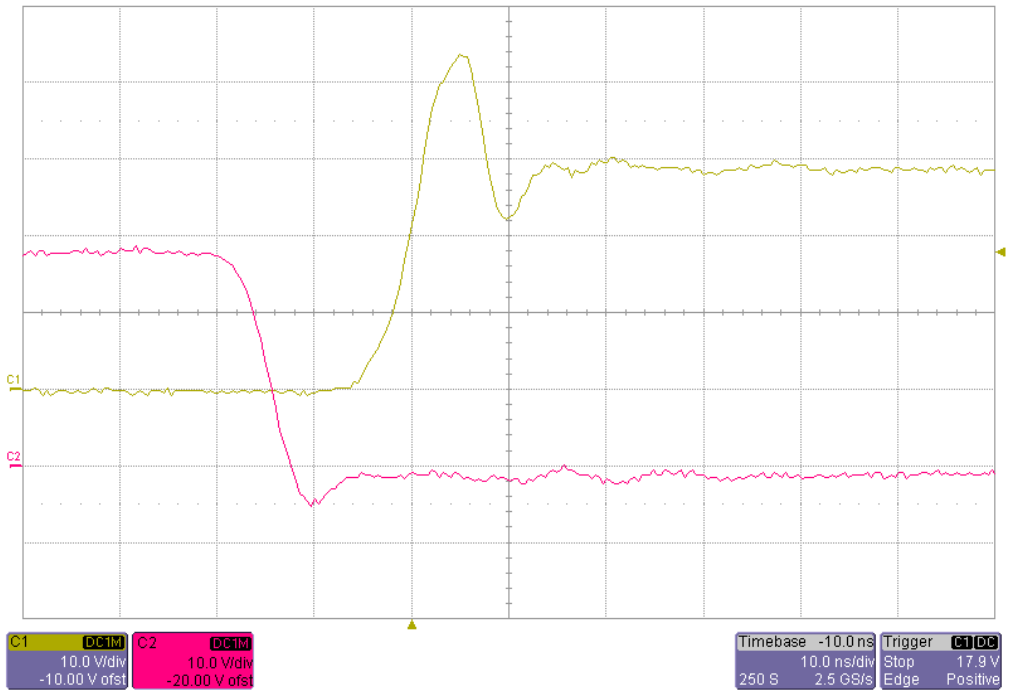
1µs/div

**Figure 10**

*180 degrees phase shift between phase A and phase B, Fsw 297kHz*

## *9.2 Switch Nodes*

Figure 11 shows the two switch nodes in the moment where Q1 is turning off and Q3 is turning on.




Ch1 => SW1
10V/div

Ch2 => SW2
10V/div

DC coupled

full bw

10ns/div

**Figure 11**

### 9.3 High Side FET Q1

The gate voltage waveform of high side FET Q1 (gate-source) is shown in Figure 12.

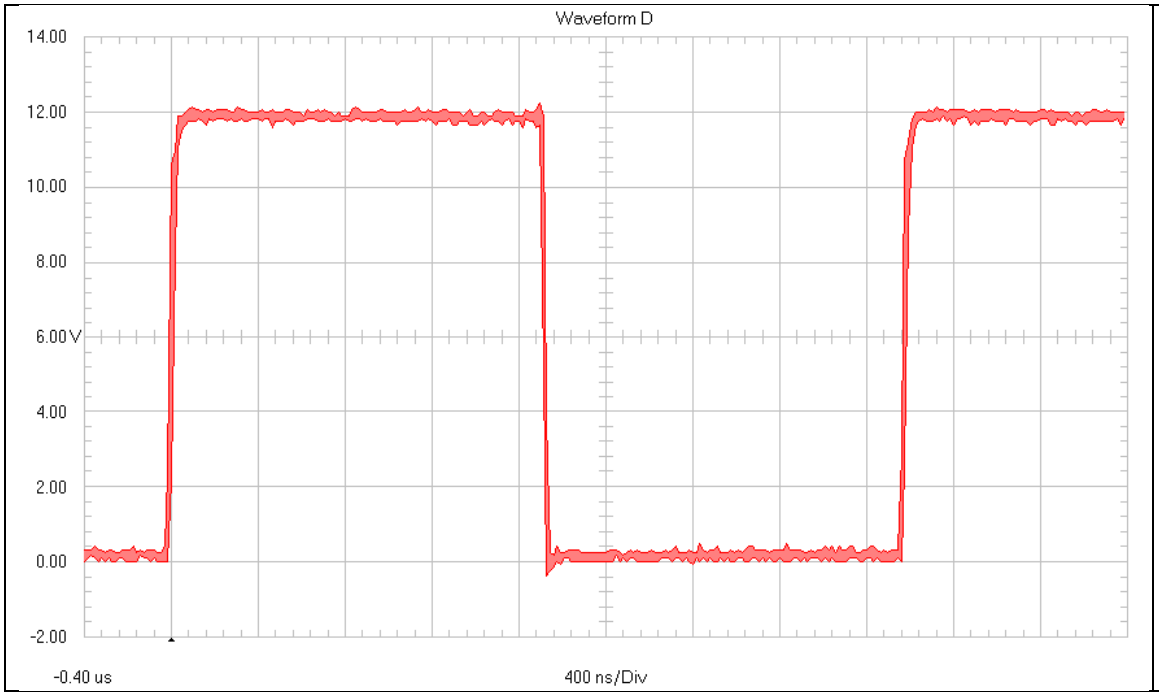



**Figure 12**

### 9.4 High Side FET Q3

The gate voltage waveform of high side FET Q3 (gate-source) is shown in Figure 13.

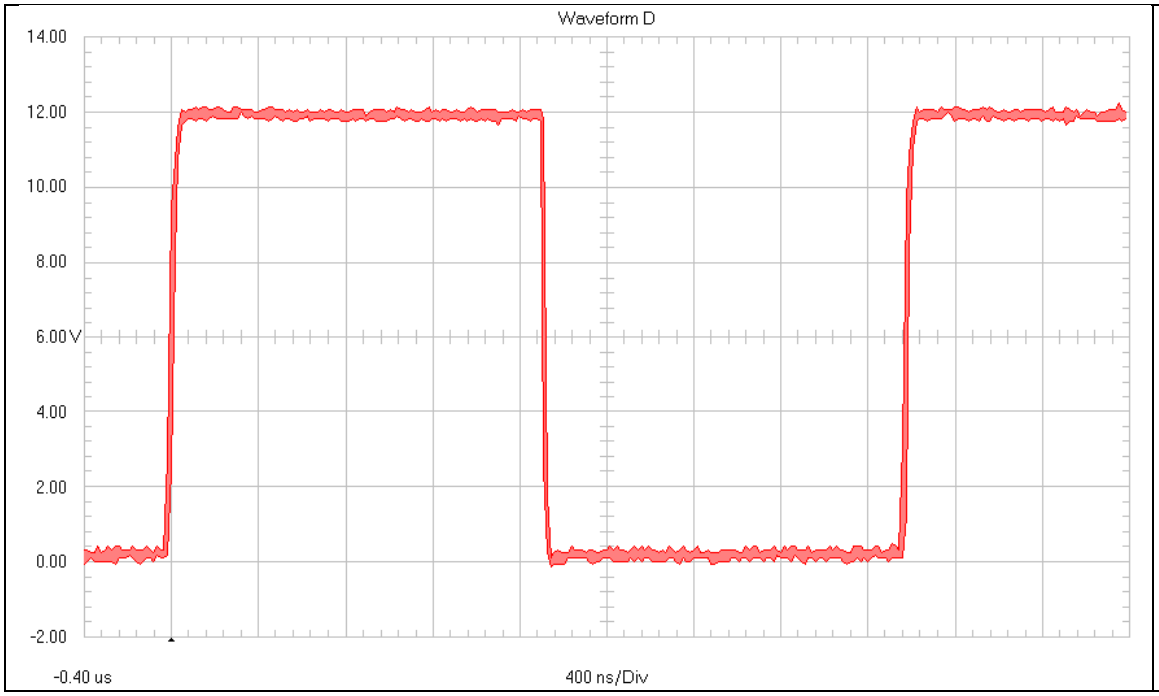



**Figure 13**

## 9.5 Low Side FET Q2

The gate voltage waveform of low side FET Q2 (gate-source) is shown in Figure 14.

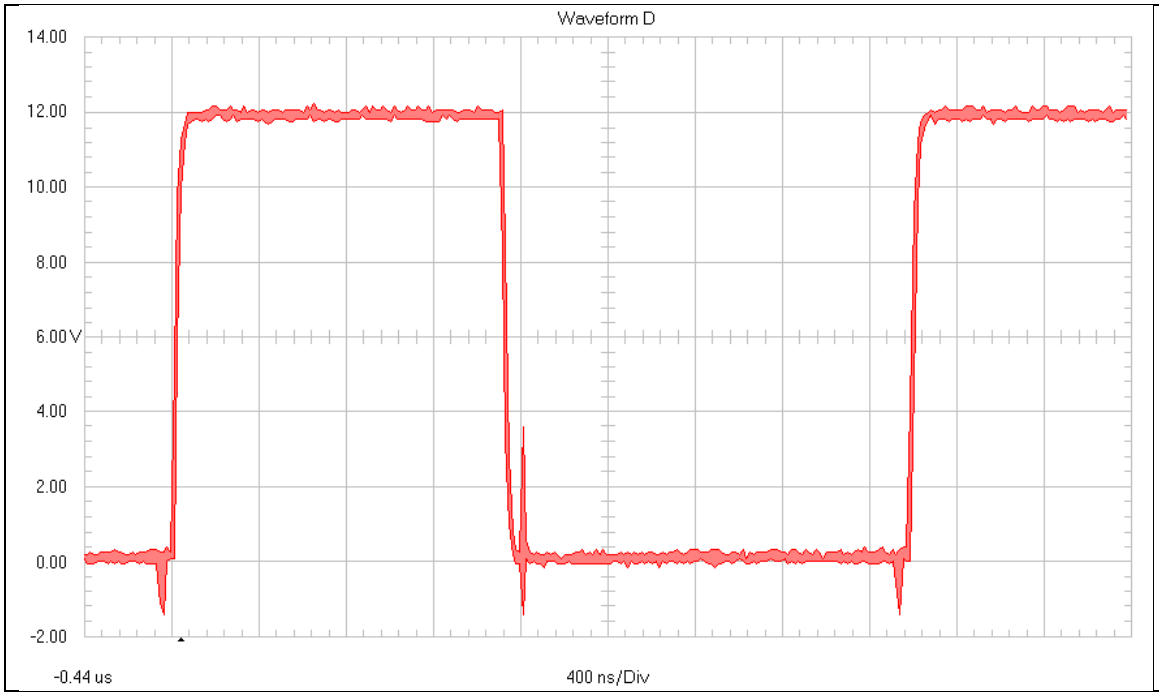



**Figure 14**

## 9.6 Low Side FET Q4

The gate voltage waveform of low side FET Q4 (gate-source) is shown in Figure 15.

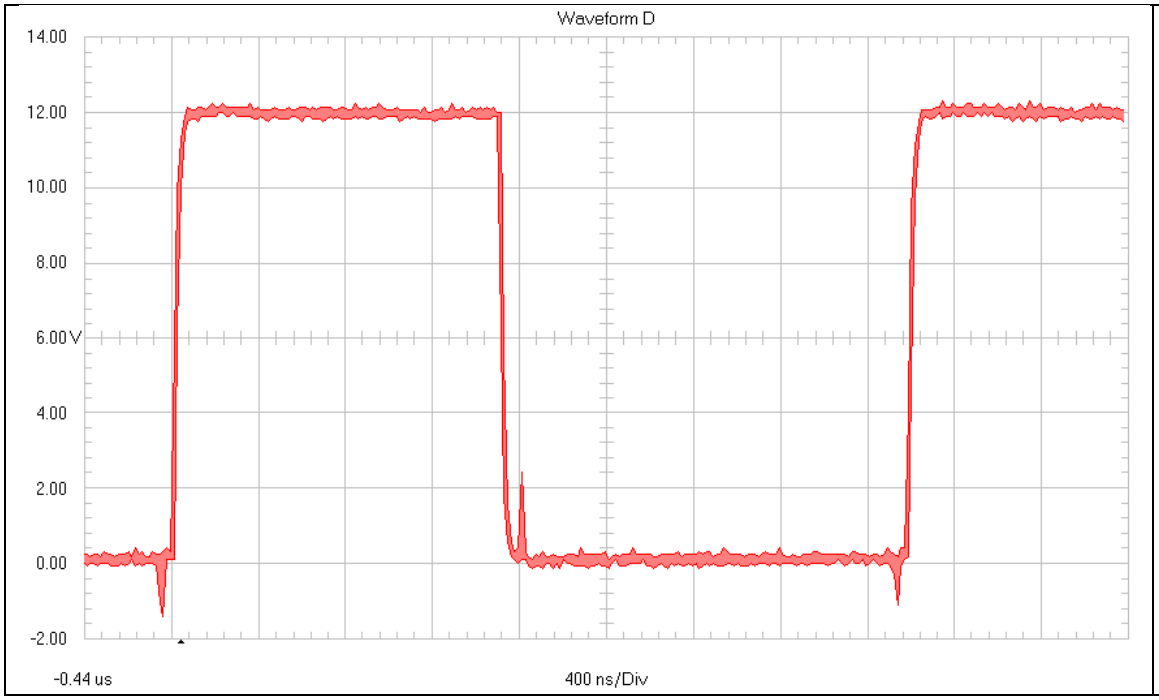



**Figure 15**

## 10 Thermal Image

Figure 16 shows the thermal image with 20A output current (NO forced cooling!);
Board under full load for >30mins before measurement:

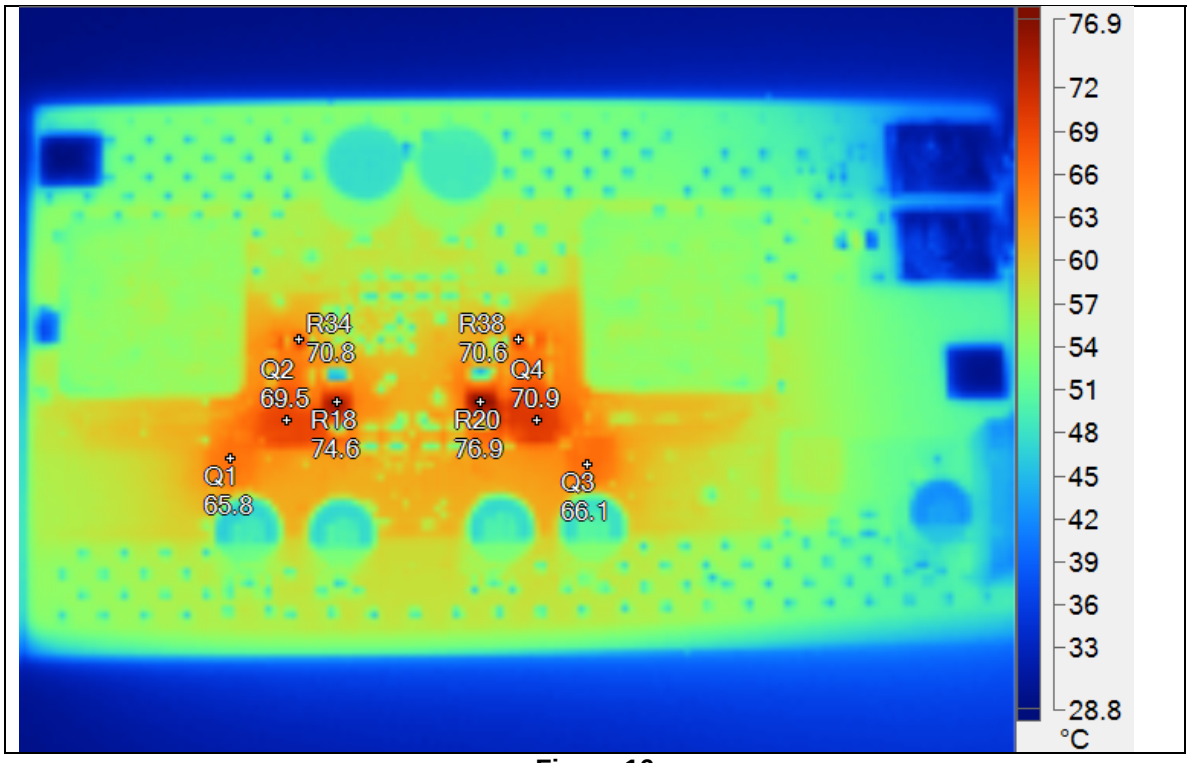



**Figure 16**

| Name | Temperature |
|---|---|
| R18 | 74.6°C |
| R20 | 76.9°C |
| Q3 | 66.1°C |
| Q1 | 65.8°C |
| Q2 | 69.5°C |
| Q4 | 70.9°C |
| R38 | 70.6°C |
| R34 | 70.8°C |

After the photo (Figure 16) the board was turned to bottom side up and a second photo was taken.

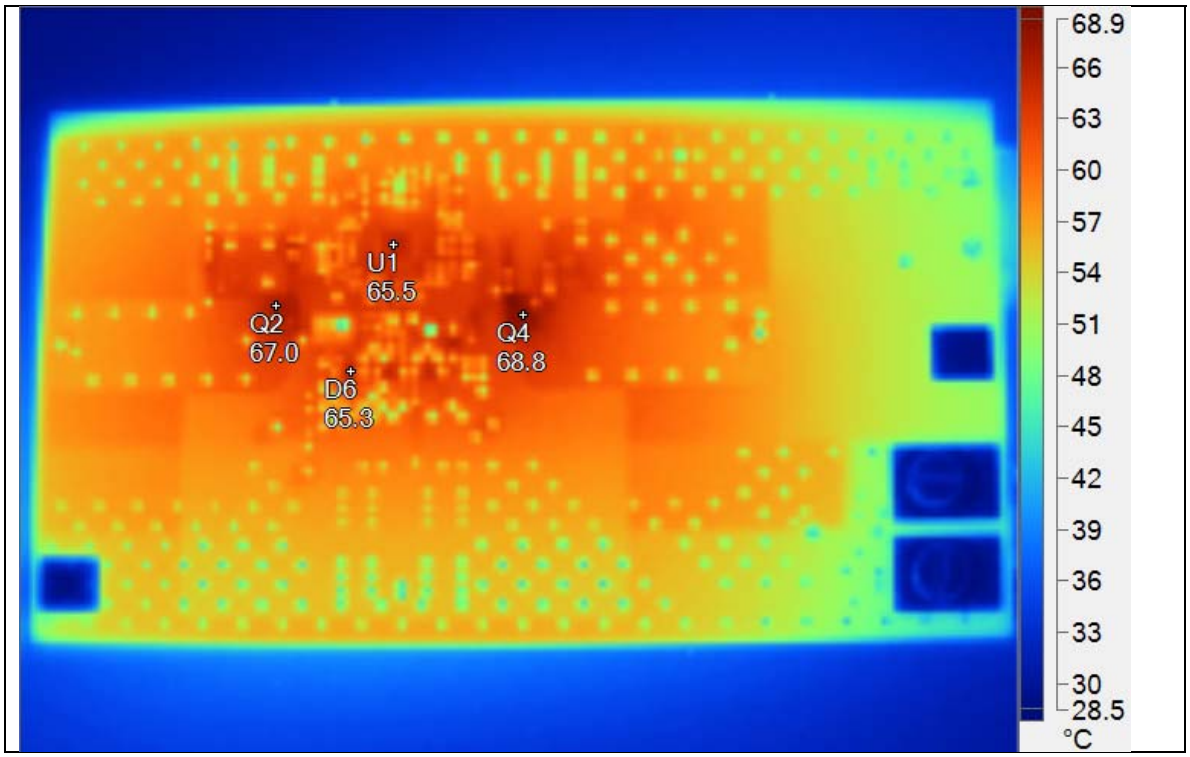



**Figure 17**

| Name | Temperature |
|---|---|
| U1 | 65.5°C |
| D6 | 65.3°C |
| Q4 (from below) | 68.8°C |
| Q2 (from below) | 67.0°C |

*Though full load efficiency is around 97%, power losses are more than 8W.*
*Output power is 280W on 85mm x 65mm !*

## 11 Output Current Measurement

To test the output current measurement feature, the current was increased in steps of 2A and the current sense voltage of the INA198 was measured. Figure 18 shows the measurement voltage in relationship to the output current. Table 2 lists the measured values.

Shunt resistor 1 milliOhm, gain INA198 is 100 – a certain DCDC offset could be measured; due to temperature DC offset is nonlinear at currents >10A (10A: 100mW...20A: 400mW):

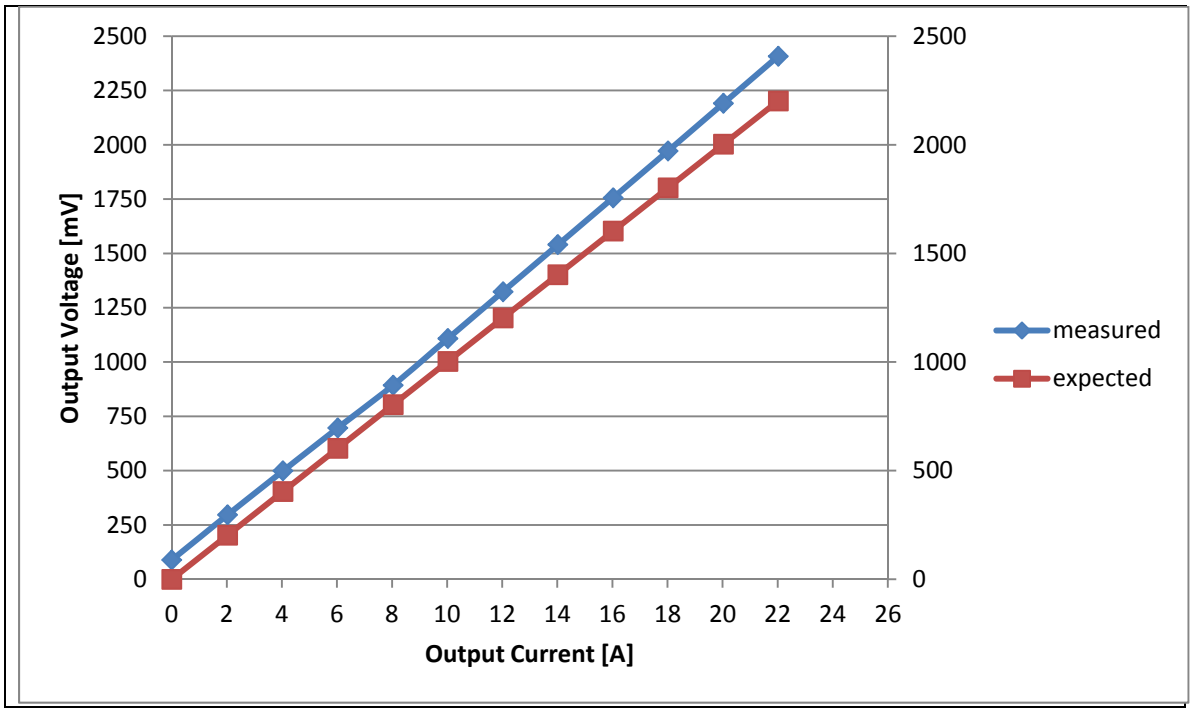
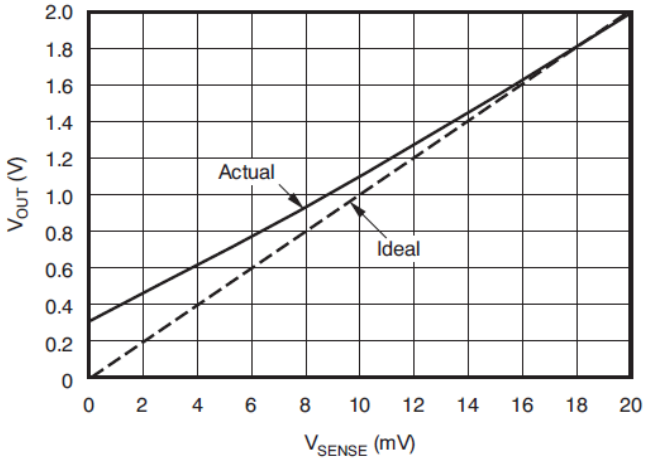



**Figure 18**

| Output Current [A] | INA198 Voltage [mV] |
|---|---|
| 0.00 | 88.5 |
| 2.03 | 296.3 |
| 4.04 | 498.8 |
| 6.03 | 696.6 |
| 8.04 | 893.3 |
| 10.03 | 1108.0 |
| 12.03 | 1323.4 |
| 14.02 | 1540.7 |
| 16.03 | 1756.0 |
| 18.02 | 1971.8 |
| 20.03 | 2190.7 |

**Table 2**




**INA198 offset, Datasheet pg. 19**

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