TI Designs

LDO Reference Design With Low Dropout, High Current, and No Bias Rail for Industrial Applications

Description

TI Design TIDA-01322 demonstrates a low-noise, low-dropout, high-current power stage with no voltage bias rail requirement utilizing the LP5922 low dropout (LDO) linear regulator. The power stage demonstrated is ideal for industrial applications. Within industrial applications, low-noise power is often achieved by introducing an LDO at the point-of-load to clean up voltage ripple from a previous switching regulator power stage. The LP5922 device makes this possible in an efficient manner by supporting very low dropout, which also eliminates any need for a voltage bias at its input.

Resources

TIDA-01322	Design Folder
LM26420	Product Folder
LP5922	Product Folder

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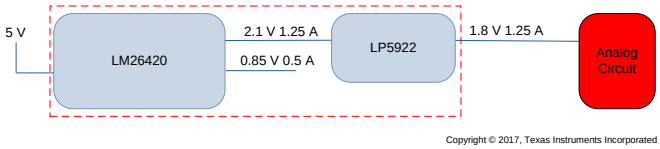
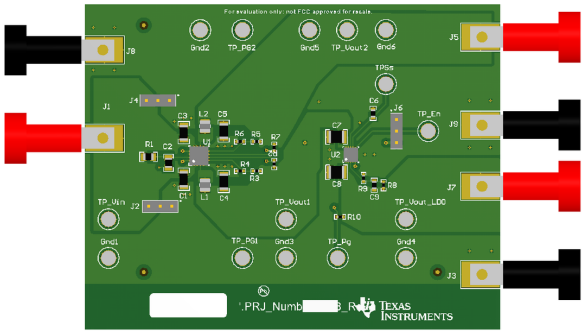
Features

- Power Management Solution for Industrial Applications
- Low Dropout of LDO Allows up to 80% High System Efficiency
- Two High-Current Outputs
- High 70-dB PSRR
- Low Noise (26 μV_{RMS}) Output for Sensitive Devices
- Small Solution Size 40 mm × 25 mm
- Low Quiescent Current 25 mA at No Load
- Extremely Good Line- and Load-Transient Performance

Applications

- Industrial Microprocessor Power
- Low Noise Sensor Power
- DAC and ADC Front-End Power and Microprocessor Data Processing
- IP Camera





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1 System Overview

1.1 System Description

This reference design implements an LDO capable of high current, low noise, and low drop-out voltage. This LDO does not require an input voltage bias rail. In many industrial applications, LDOs are used to clean up AC ripple from the output of a switching buck regulator. Because LDOs step down voltages via thermal dissipation, from an efficiency standpoint it is ideal if most of the power conversion from the input of a buck regulator to the output of the following LDO occurs within the buck regulator. In order to optimize this efficiency, an LDO that can operate with a very small voltage step down, without requiring a voltage bias on its input, is ideal for these applications. This reference design demonstrates such a configuration.

The LM26420 regulator is a monolithic, high-efficiency, dual-PWM, step-down DC-DC converter. The LM26420 device can drive two 2-A loads with an internal 75-mΩ PMOS top switch and an internal 50-mΩ NMOS bottom switch using state-of-the-art BICMOS technology, resulting in the best power density available. The world-class control circuitry allows on times as low as 30 ns, thus supporting exceptionally high-frequency conversion over the entire 3-V to 5.5-V input operating range down to the minimum output voltage of 0.8 V. Although the operating frequency is high, efficiencies up to 93% are easy to achieve. External shutdown is included, featuring an ultra-low standby current. The LM26420 utilizes current-mode control and internal compensation to provide high performance regulation over a wide range of operating conditions.

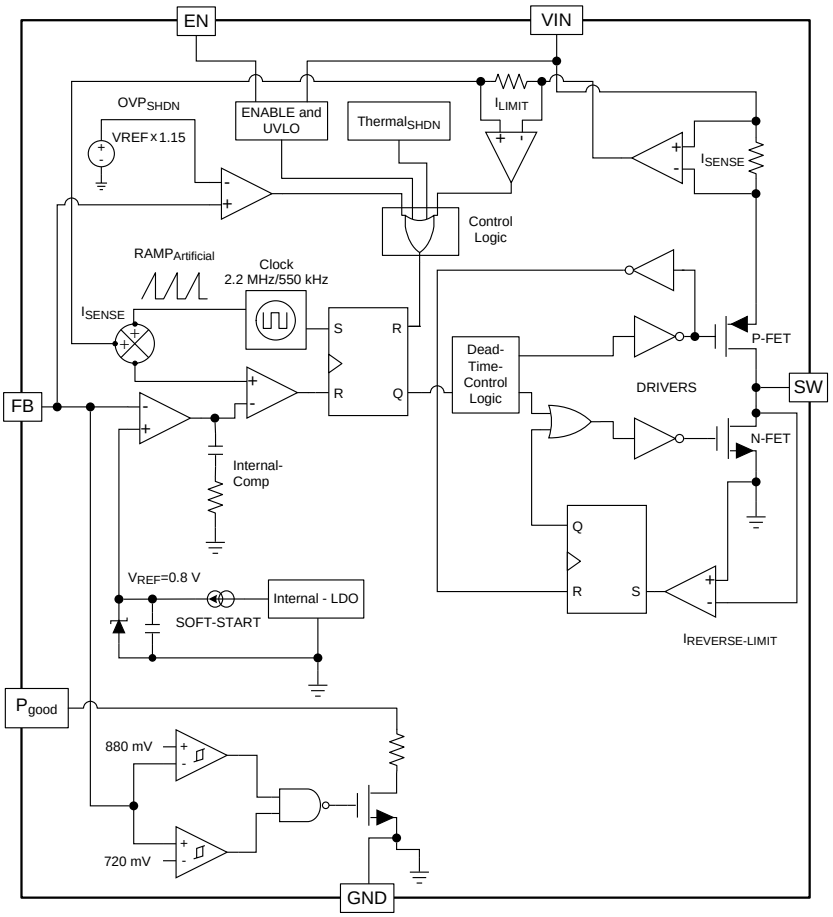


Figure 1. LM26420 Functional Block Diagram

The LP5922 device is a linear regulator capable of supplying 2-A output current. Designed to meet the requirements of RF and analog circuits, the LP5922 device provides high performance for output accuracy, noise, and power supply ripple rejection (PSRR) as well as line- and load-transient response. The LP5922 also offers ultra-low input voltage down to 1.3 V without additional bias rail. The soft-start time of the LP5922 device is programmable by an external capacitor on the CSS pin.

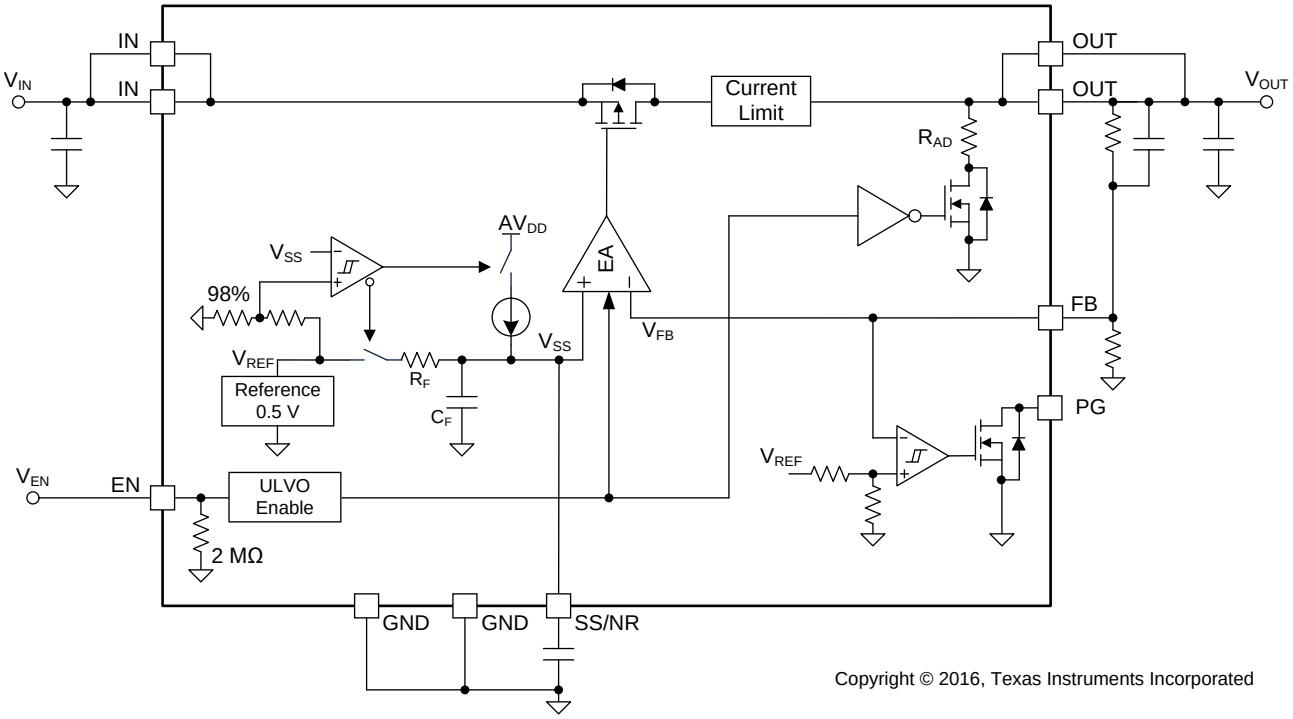


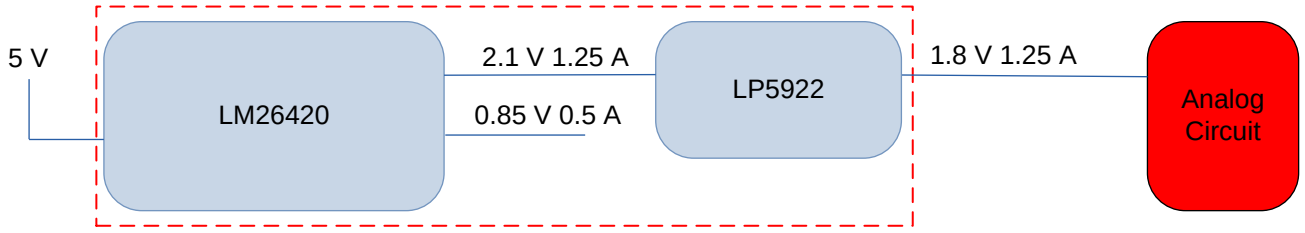
Figure 2. LP5922 Functional Block Diagram

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	COMMENTS	SPECIFICATION
SYSTEM OPERATION		
V_{IN}	Input voltage (J1 on board)	5 V
V_{OUT1}	Output voltage of LP5922 (J7 on board)	1.8 V
V_{OUT2}	Output voltage from LM26420 (J5 on board)	0.85 V
f_{SW}	Switching frequency	2.2 MHz
I_{OUT} J5	Output current of LP5922 (J7 on board)	1.25 A
I_{OUT} J7	Output current of LM26420 (J5 on board)	0.5 A

1.3 Block Diagram



1.4 Highlighted Products

1.4.1 LP5922 LDO

- Wide Input Voltage Range: 1.3 V to 6 V
- Low V_{IN} Voltage Without Extra Bias Voltage
- Output Voltage Range: 0.5 V to 5 V
- Output Current: 2 A
- Low Output Voltage Noise: 25 μV_{RMS}
- PSRR: 70 dB at 1 kHz
- Output Voltage Tolerance: ±1.5%
- Shutdown Supply Current : 0.1 μA
- Low Dropout: 200 mV at 2-A Load
- Thermal-Overload and Short-Circuit Protection
- Power Good Output
- Programmable Soft Start Limits Inrush Current
- –40˚C to +125°C Operating Junction Temperature
- 3-mm × 3-mm × 0.75-mm 10-Pin WSON Package

1.4.2 LM26420 2-Phase Switching Regulator

- Input Voltage Range: 3 V to 5.5 V
- Output Voltage Range: 0.8 V to 4.5 V
- 2-A Output Current per Regulator
- High Switching Frequency: 2.2 MHz (LM26420X); 0.55 MHz (LM26420Y)
- 0.8-V, 1.5% Internal Voltage Reference
- Internal Soft Start
- Independent Power Good and Precision Enable for Each Output
- Current Mode, PWM Operation
- Thermal Shutdown
- Overvoltage Protection
- Start-up into Pre-biased Output Loads
- Regulators are 180° Out of Phase

2 Getting Started Hardware

2.1 Reference Design Power Up and Power Down

This LDO reference design is very easy to set up to begin evaluating key functionalities. Figure 3 is marked with red circle the input 5-Vconnection (red) and the ground connection (black) banana plugs. Use a good-quality power supply and consider adding bypass capacitor at board end if using long wires from supply to the board.

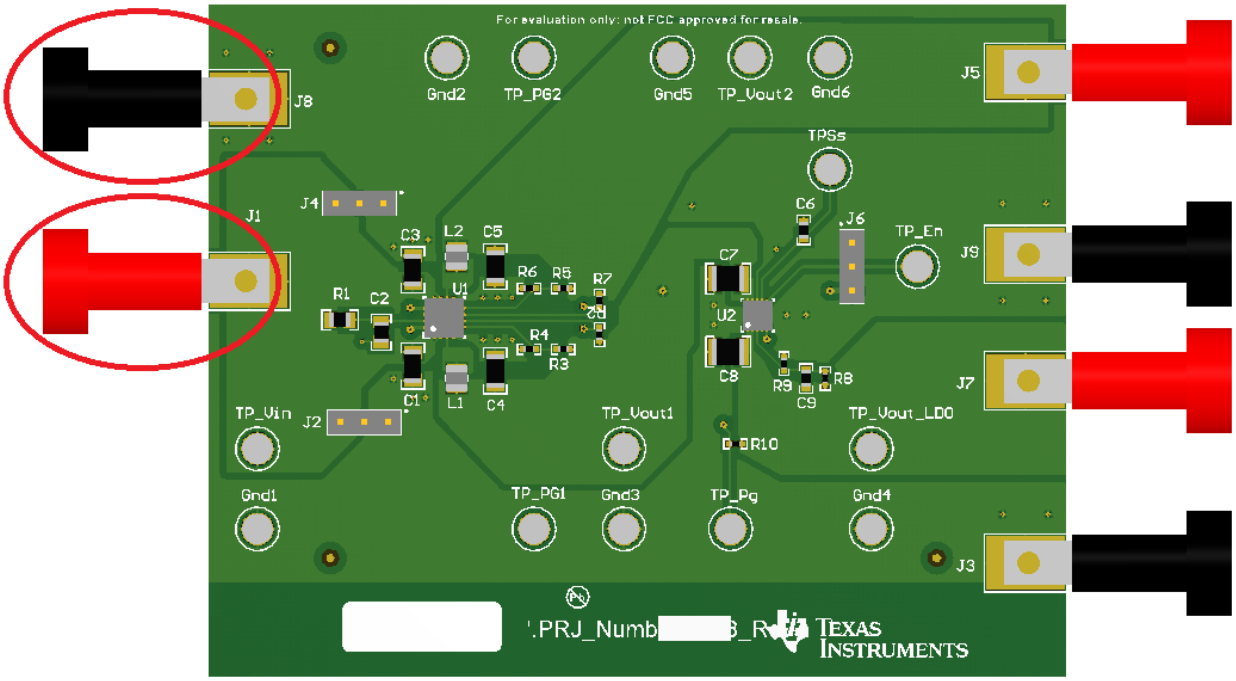


Figure 3. Reference Design Input-Power-Supply Connectors

Load devices can be connected to the reference design board by banana plugs as well. In Figure 4 blue-circled banana plugs are connected directly to the LM26420 device second output and initially provide 0.85-V output level for end equipment. Yellow-circled plugs provide the initial 1.8-V voltage from the LP5922 LDO. This voltage is meant to be fed to a sensitive analog component, which operation may be affected by the switching regulator noise and voltage ripple. The main purpose of the LP5922 device is to clean voltage rail as effectively as possible. On both output connections the red plug is the higher potential, and the black plug is the ground connection.

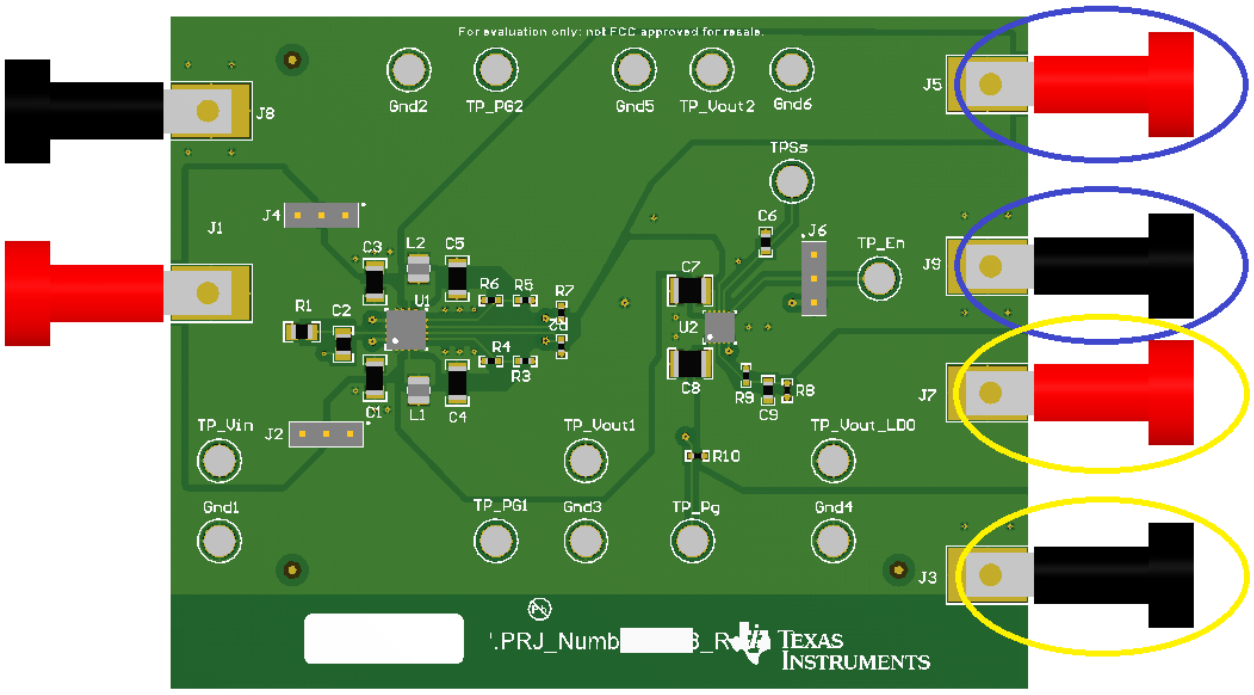


Figure 4. Reference Design Output Connectors

Power management devices LM26420 and LP5922 each have separated enable signals to turn switching regulator output voltages on and off and for LDO output voltage. This means user can enable them one by one by connecting jumper to the each pin header (see Figure 5). In the same way user can shut down devices by moving jumper to the adjacent position of pin header.

Jumpers can already be populated before devices have input voltage present, making usage even easier if end equipment is supporting start-up that is not sequenced. Many times power management systems are powered up sequentially, which means that some power rails are up and at the correct level before other rails; shutdown is also controlled. This reference design board supports this functionality, and user can control the enable signals with a signal generator from the outside of the board to emulate sequenced start-up and shutdown.

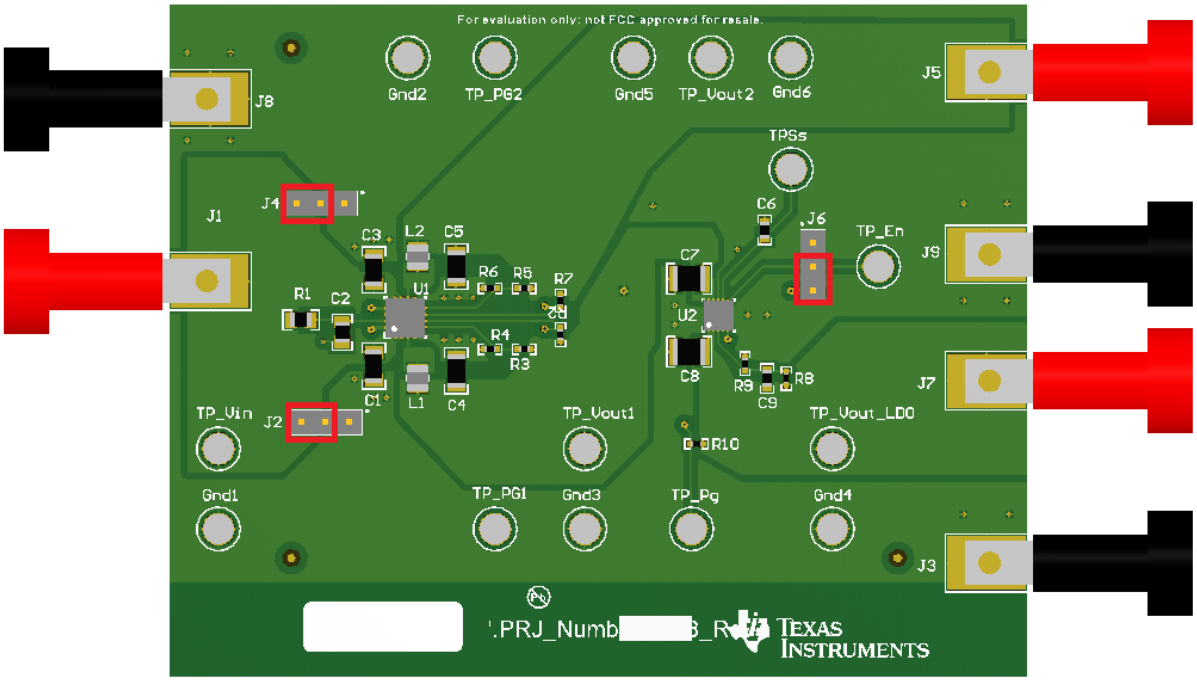


Figure 5. Power-Up Jumper Connections for Power Management Devices

2.2 Reference Design Component Selection

2.2.1 Component Selection for LP5922 Device

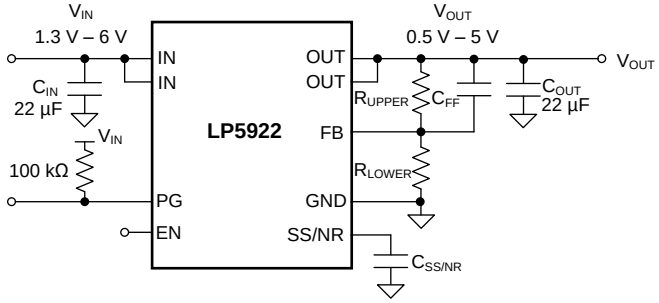


Figure 6. LP5922 Typical Configuration

2.2.1.1 Setting the Output Voltage of LP5922

Output voltage for the LP5922 device can be set to any value from 0.5 V to 5 V using two external resistors shown as R_{UPPER} and R_{LOWER} in Figure 6. The value for the R_{LOWER} must be less than, or equal to, 100 kΩ for good loop compensation. R_{UPPER} can be selected for a given V_{OUT} using Equation 1:

$$R_{UPPER} = \frac{(V_{OUT} - V_{FB}) \times R_{LOWER}}{V_{FB}} \quad (1)$$

where

- V_{FB} = 0.5 V

2.2.1.2 Input Capacitor Selection

An input capacitor is required for stability. The input capacitor must be at least equal to, or greater than, the output capacitor for good load-transient performance. A capacitor of at least 22 µF must be connected between the LP5922 IN pin and ground for stable operation over full load-current range. It is acceptable to have a higher value of output capacitance than input capacitance, as long as the input is at least 22 µF. The input capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5922 device, then TI recommends increasing the input capacitor. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be verified by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains 22 µF ±30% over the entire operating temperature range.

2.2.1.3 Output Capacitor Selection

The LP5922 device is designed to work specifically with a low-ESR ceramic (MLCC) output capacitor, typically 22 µF. A ceramic capacitor (dielectric types X5R or X7R) in the 22-µF to 100-µF range, with an ESR not exceeding 500 mΩ, is suitable in the LP5922 application circuit having an output voltage greater than 0.8 V. For output voltages of 0.8 V or less, the output capacitance must be increased to typically 47 µF. The output capacitor must be connected between the device OUT and GND pins. The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that does not exceed 500 mΩ to ensure stability.

It is possible to use tantalum capacitors at the device output, but these are not as attractive for reasons of size, cost, and performance.

A combination of multiple output capacitors in parallel boosts the high-frequency PSRR. The combination of one 0805-sized, 47-µF ceramic capacitor in parallel with two 0805-sized, 10-µF ceramic capacitors with a sufficient voltage rating optimizes PSRR response in the frequency range of 400 kHz to 700 kHz (which is a typical range for DC-DC supply switching frequency). This 47-µF || 10-µF || 10-µF combination also ensures that the minimum effective capacitance is met at high-input-voltage and high-output-voltage configurations. Many 0805-sized, 47-µF ceramic capacitors have a voltage derating of approximately 60% to 75% at 5 V, so the addition of the two 10-µF capacitors ensures that the capacitance is at or above 22 µF.

2.2.1.4 Capacitor Characteristics

The LP5922 device is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values of approximately 22 μF, ceramic capacitors are the smallest, least expensive, and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 22-μF ceramic capacitor is in the range of 10 mΩ to 20 mΩ, which easily meets the ESR requirement for stability for the LP5922 device. A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings of 22 μF. Another important consideration is that tantalum capacitors have higher ESR values than equivalently sized ceramics. While it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. Also, the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

2.2.2 Component Selection for LM26420 Device

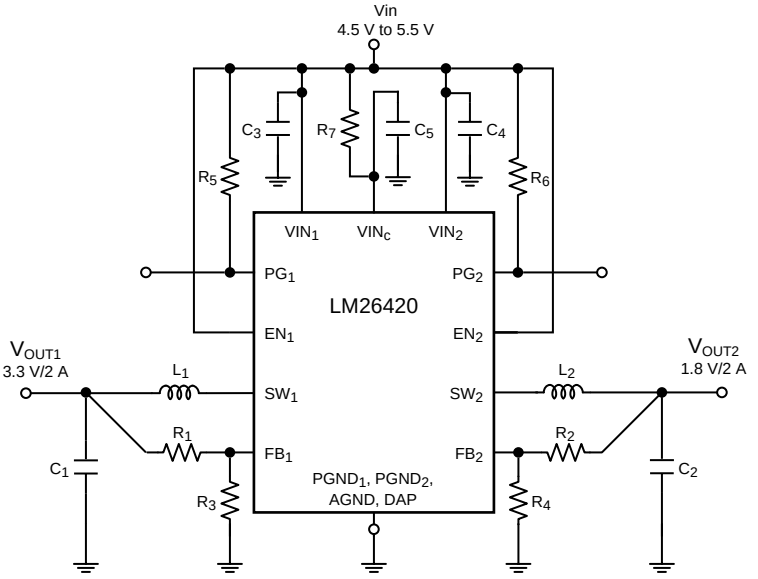


Figure 7. LM26420 Typical Configuration

2.2.2.1 Setting the Output Voltage

The output voltage is set using Equation 2 where R2 is connected between the FB pin and GND, and R1 is connected between V_{OUT} and the FB pin. A good value for R2 is 10 kΩ. When designing a unity gain converter (V_{OUT} = 0.8 V), R1 must be between 0 Ω and 100 Ω, and R2 must be on the order of 5 kΩ to 50 kΩ. 10 kΩ is the suggested value where R1 is the top feedback resistor and R2 is the bottom feedback resistor.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (2)$$

where

- V_{REF} = 0.8 V

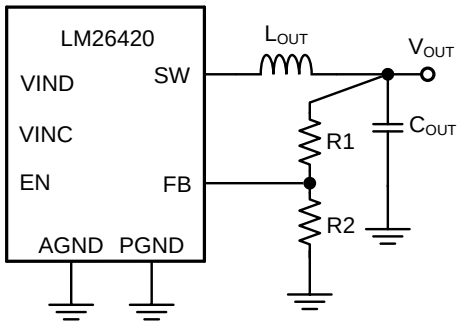


Figure 8. Programming V_{OUT}

To determine the maximum allowed resistor tolerance, use Equation 3:

$$\sigma = \left(\frac{1}{1 + 2x \frac{1 - \frac{V_{FB}}{V_{OUT}}}{TOL - \phi}} \right) \quad (3)$$

where

- TOL is the set point accuracy of the regulator, is the tolerance of V_{FB}

2.2.2.2 Input Capacitor Selection

The input capacitors provide the AC current needed by the nearby power switch so that current provided by the upstream power supply does not carry a lot of AC content, generating less EMI. To the buck regulator in question, the input capacitor also prevents the drain voltage of the FET switch from dipping when the FET is turned on, therefore providing a healthy line rail for the LM26420 to work with. Because most of the AC current is typically provided by the local input capacitors, the power loss in those capacitors can be a concern. In the case of the LM26420 regulator, because the two channels operate 180° out of phase, the AC stress in the input capacitors is less than if they operated in phase. The measure for the AC stress is called input ripple RMS current. TI strongly recommends that at least one 10-µF ceramic capacitor be placed next to each of the VIND pins. Bulk capacitors such as electrolytic capacitors or OSCON capacitors can be added to help stabilize the local line voltage, especially during large load transient events. As for the ceramic capacitors, use X7R or X5R types. They maintain most of their capacitance over a wide temperature range. Try to avoid sizes smaller than 0805. Otherwise significant drop in capacitance may be caused by the DC bias voltage. See *Section 2.2.2.3* for more information. The DC voltage rating of the ceramic capacitor must be higher than the highest input voltage.

Capacitor temperature is a major concern in board designs. While using a 10-µF or higher MLCC as the input capacitor is a good starting point, it is a good idea to check the temperature in the real thermal environment to make sure the capacitors are not over-heated. Capacitor vendors may provide curves of ripple RMS current vs temperature rise, based on a designated thermal impedance. In reality, the thermal impedance may be very different. It is always a good idea to check the capacitor temperature on the board.

Because the duty cycles of the two channels may overlap, calculation of the input ripple RMS current is a little tedious. Use the following equation:

$$I_{irrms} = \sqrt{(I_1 - I_{av})^2 d1 + (I_2 - I_{av})^2 d2 + (I_1 + I_2 - I_{av})^2 d3}$$

where

- I_1 is the maximum output current of channel 1
- I_2 is the maximum output current of channel 2
- d1 is the non-overlapping portion of the duty cycle (d1) of channel 1
- d2 is the non-overlapping portion of the duty cycle (d2) of channel 2
- d3 is the overlapping portion of the two duty cycles.
- I_{av} is the average input current (4)

$I_{av} = I_1 \times d2_1 + I_2 \times d2$. To determine the duty cycle of each channel, use $D = V_{OUT} / V_{IN}$ for a quick result or use Equation 5 for a more accurate result.

$$D = \frac{V_{OUT} + V_{SW\_BOT} + I_{OUT} \times R_{DC}}{V_{IN} + V_{SW\_BOT} - V_{SW\_TOP}}$$

where

- R_{DC} is the winding resistance of the inductor (5)

2.2.2.3 Output Capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is approximately:

$$\Delta V_{OUT} = \Delta I_L \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}} \right) \quad (6)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple is approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LM26420 device, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high-frequency noise. A certain amount of switching edge noise couples through parasitic capacitances in the inductor to the output. A ceramic capacitor bypasses this noise, while a tantalum capacitor does not. Because the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications require a minimum of 22 µF of output capacitance. Capacitance often, but not always, can be increased significantly with little detriment to the regulator stability. As it does for the input capacitor, TI recommends multilayer ceramic capacitors such as X7R or X5R types for the output capacitor.

2.2.2.4 Inductor Selection

The duty cycle (D) can be approximated as the ratio of output voltage (V_{OUT}) to input voltage (V_{IN}):

$$D = \frac{V_{OUT}}{V_{IN}} \quad (7)$$

The voltage drop across the internal NMOS (SW_BOT) and PMOS (SW_TOP) must be included to calculate a more accurate duty cycle. Calculate D by using the following formulas:

$$D = \frac{V_{OUT} + V_{SW\_BOT}}{V_{IN} + V_{SW\_BOT} - V_{SW\_TOP}} \quad (8)$$

V_{SW_TOP} and V_{SW_BOT} can be approximated by:

$$V_{SW\_TOP} = I_{OUT} \times R_{DSON\_TOP} \quad (9)$$

$$V_{SW\_BOT} = I_{OUT} \times R_{DSON\_BOT} \quad (10)$$

The inductor value determines the output ripple voltage. Smaller inductor values decrease the size of the inductor, but increase the output ripple voltage. An increase in the inductor value decreases the output ripple current.

User must ensure that the minimum current limit (2.4 A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$I_{LPK} = I_{OUT} + \Delta i_L \quad (11)$$

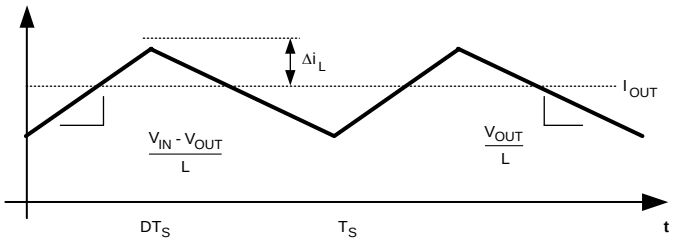


Figure 9. Inductor Current

$$\frac{V_{IN} - V_{OUT}}{L} = \frac{2\Delta i_L}{DT_S} \quad (12)$$

In general,

$$\Delta i_L = 0.1 \times (I_{OUT}) \rightarrow 0.2 \times (I_{OUT}) \quad (13)$$

If Δi_L = 20% of 2 A, the peak current in the inductor is 2.4 A. The minimum ensured current limit over all operating conditions is 2.4 A. User can either reduce Δi_L, or make the engineering judgment that zero margin is safe enough. The typical current limit is 3.3 A.

The LM26420 device operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple voltage. See *Section 2.2.2.3* for more details on calculating output voltage ripple. Now that the ripple current is determined, the inductance is calculated by:

$$L = \left(\frac{DT_S}{2\Delta i_L}\right) x\ (V_{IN} - V_{OUT}) \quad (14)$$

where

$$T_S = \frac{1}{f_S} \quad (15)$$

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation results in a sudden reduction in inductance and prevents the regulator from operating correctly. The peak current of the inductor is used to specify the maximum output current of the inductor, and saturation is not a concern due to the exceptionally small delay of the internal current limit signal. Ferrite-based inductors are preferred in order to minimize core losses when operating with the frequencies used by the LM26420 device. This presents little restriction because there are many varieties of ferrite-based inductors. Lastly, inductors with lower series resistance (R_{DCR}) provide better operating efficiency.

3 Testing and Results

To verify and prove the system functionality and highlight its excellent performance in this reference design, the most important parameters were measured in a real use case. This power management reference design makes a system-level, power-management design phase easier, thus saving time to enable user to focus on end-equipment functionality and integration because the power management device already has measurement-proven performance.

3.1 Test Plan

The following items were identified as important measurements, all done at room temperature (+25°C):

1. Line regulation
   - Input voltage sweep: 4.5 V to 5.5 V
   - Load current 5 mA on LDO and Buck 2
2. Load regulation
   - Nominal input voltage 5 V
   - Full load range for LDO: 1.8 V, 0 to 1.25 A
   - Full load range for Buck 2 output: 0.85 V, 0 to 0.5 A
3. Efficiency
   - Nominal input voltage 5 V
   - Full load range for LDO: 1.8 V, 0 – 1.25 A
   - Full load range for Buck 2 output: 0.85 V, 0 to 0.5 A
4. Line transient response
   - Line transient step from 4.5 V – 5.5 V – 4.5 V with 5-µs/V rise/fall time, full load on LDO and Buck 2
5. Load transient response
   - 100 µA – 1.25 A – 100 µA, 1 A/µs for LDO
   - Buck 2 load 0.5 A
6. Ripple comparison
   - LM26420 Buck 1 output vs LP5922 output
7. Noise comparison
   - LM26420 Buck 1 output vs LP5922 output, 10 Hz – 1 MHz
8. PSRR comparison
   - LM26420 Buck 1 output vs LP5922 output, 10 Hz – 1 MHz
9. Start-up and shutdown behavior
10. Current consumption
    - Shutdown and active mode

3.2 Test Results

3.2.1 Line Regulation

Line regulation measures how well circuits can maintain in regulation while input voltage changes. Measurement result is presented in Figure 10.

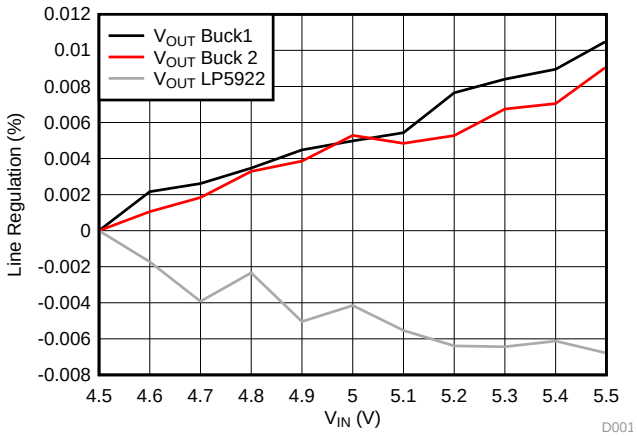


Figure 10. System Output Voltages Line Regulation

3.2.2 Load Regulation

Load regulation measures how well circuits maintain in regulation while load current changes. Measurement result is presented in Figure 11.

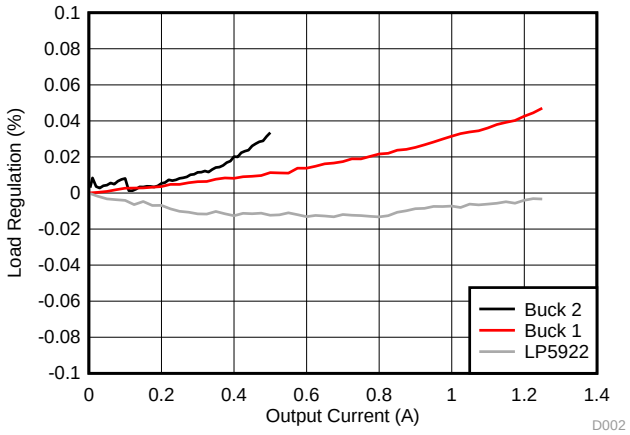


Figure 11. System Output Voltages Load Regulation

3.2.3 Efficiency

System efficiency is presented in Figure 12 . Efficiency is split in two data lines. The LM26420 efficiency shows that it is beneficial to pre-regulate voltage rails downward as much as possible and after that clean voltage rail with LDO. The highest system efficiency is achieved with that approach. This approach is also wise from thermal management point of view. Because the LDO “wastes” energy to heat while regulating desired voltage, it is beneficial to avoid extra voltage over a linear regulator.

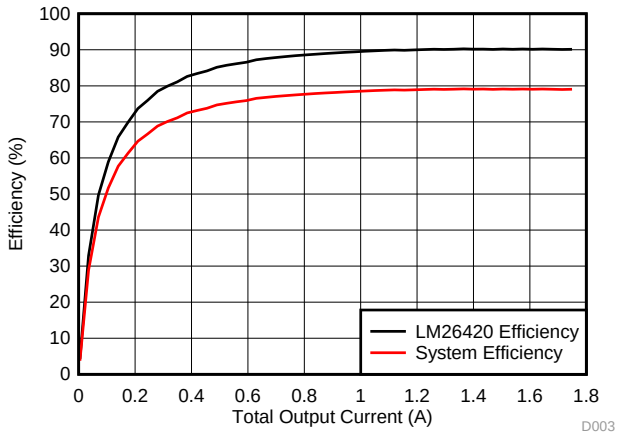


Figure 12. System Efficiency

3.2.4 Line Transient Response

Line transient response measures how well circuits tolerate input voltage disturbances and behave during those transients. Line transient response in shown in Figure 13

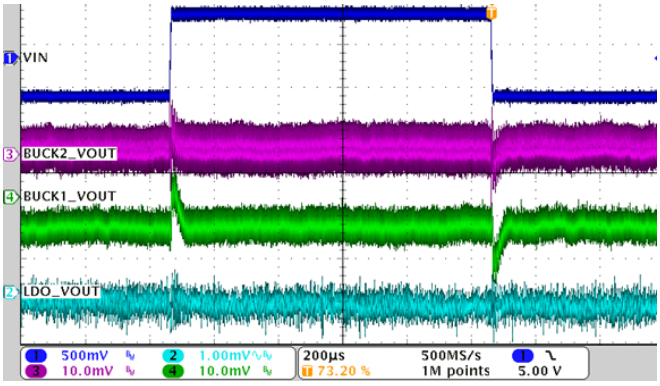


Figure 13. Line Transient Response

3.2.5 Load Transient Response

Load transient response measures how well circuits tolerate output load current changes. Behavior during those transients is also important. Load transient response in presented in Figure 14.

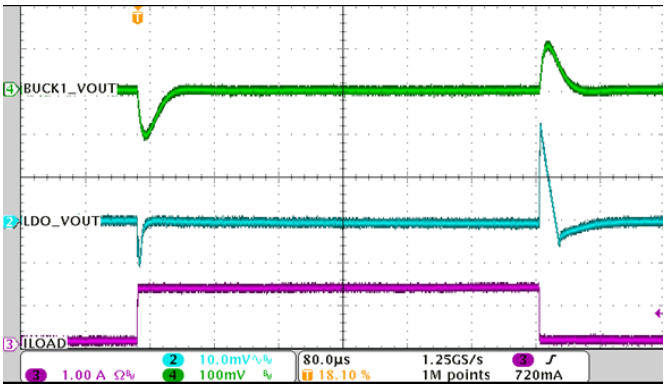


Figure 14. Load Transient Response

3.2.6 Ripple Comparison

In Figure 15 compares Buck 1 output and LDO output ripple. In Buck 1 ripple the buck type of switching regulator typical output voltage is clearly seen in the waveform, which has voltage steps synchronously in switching frequency. In contrast, in the LDO output there is no switching waveform present anymore because it is filtered out.

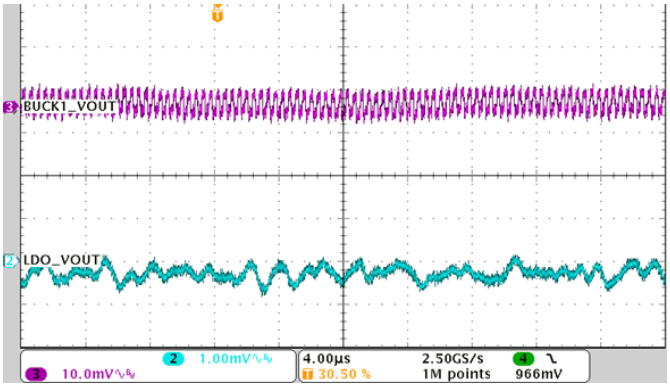


Figure 15. Buck 1 vs LDO Output Ripple

3.2.7 Noise Comparison

Noise is presented in Figure 16. The strength of the low-noise LDO is the ability to filter undesirable noise on a sensitive analog circuit input voltage. Total integrated noise 10-Hz to 100-kHz range in Buck 1 output is 150 μV_{RMS}. After LDO total noise in same range is 26 µVrms.

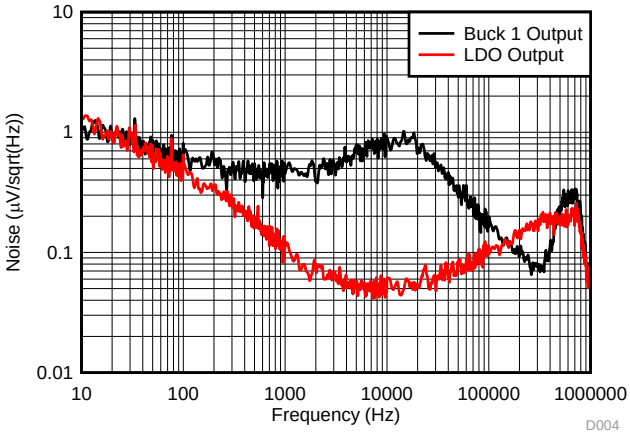


Figure 16. Noise Comparison

3.2.8 PSRR Comparison

PSRR is presented in Figure 17. The LDO is able to further reject input line disturbances after switching converter and produce extremely clean output voltage.

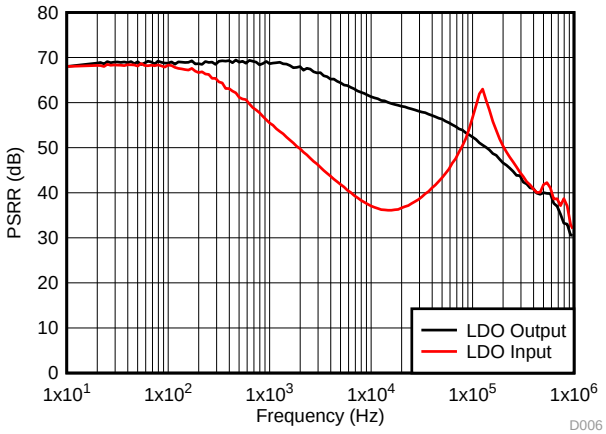


Figure 17. PSRR Comparison

3.2.9 Start-Up and Shutdown Behavior

Start-up and shutdown without load is presented in Figure 18 and Figure 19. The LDO has programmable soft-start functionality, and output voltage is ramped up linearly depending on the soft-start capacitor CSS value.

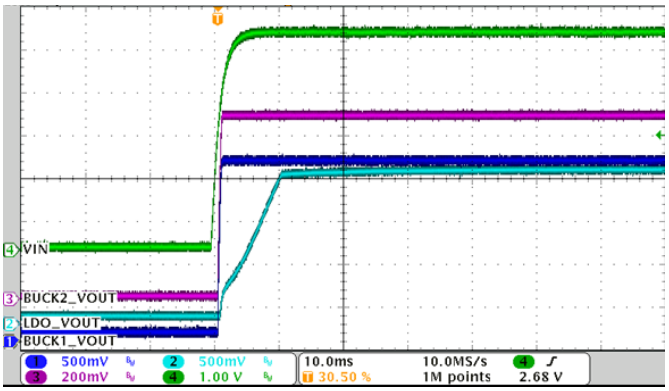


Figure 18. Start-Up Without Load

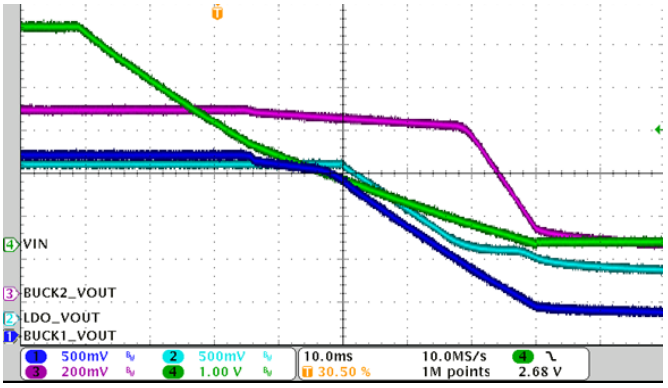


Figure 19. Shutdown Without Load

Start-up and shutdown behavior with full load is presented in Figure 20 and Figure 21. LDO output current is 1.25 A, and Buck 2 output current is 0.5 A.

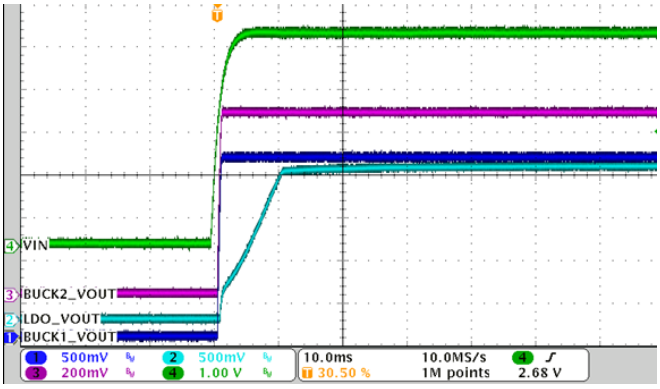


Figure 20. Start-Up With Full Load

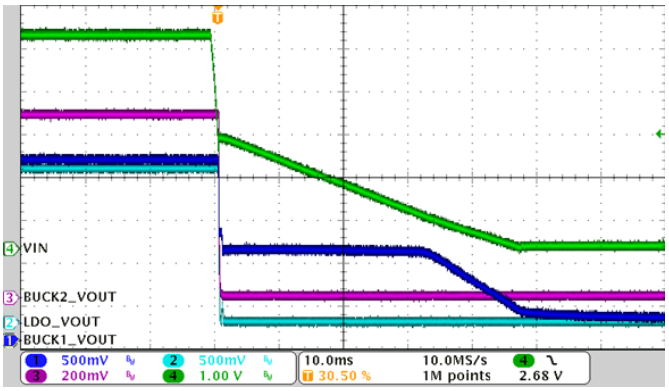


Figure 21. Shutdown With Full Load

3.2.10 Current Consumption

Current consumption in both active mode and shutdown mode is presented in Figure 22 and Figure 23. In active mode all input current other than load current is calculated as ground current. This means that from input power supply the portion not going to the loads is defined as a “waste” power and is given as a current taken from the input power supply (5 V in this design). In shutdown mode all current taken from the input power supply is defined as the shutdown current.

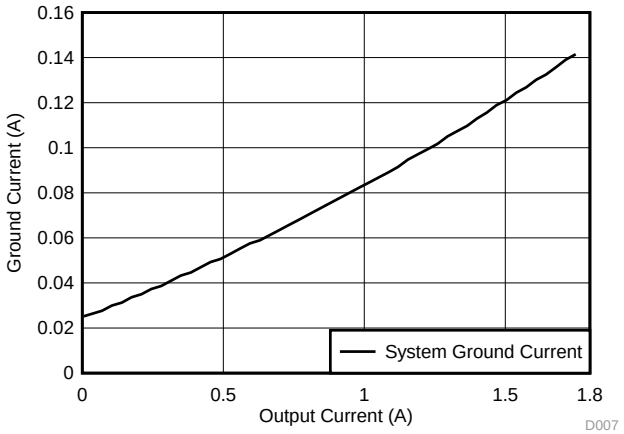


Figure 22. Active Mode Ground Current

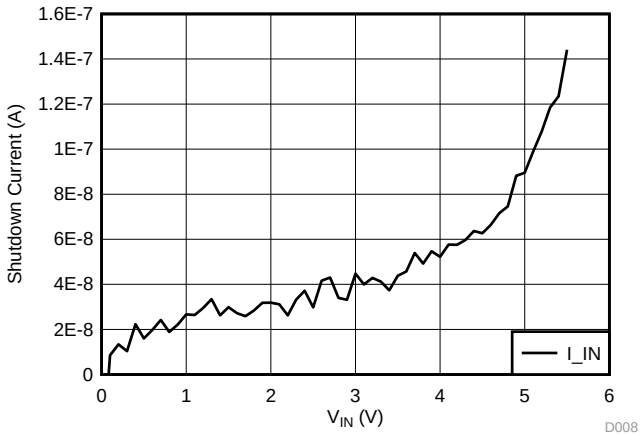


Figure 23. System Shutdown Current

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01322.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01322.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01322.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01322.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01322.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01322.

5 Related Documentation

1. Texas Instruments, *LDO Noise Demystified*, Application Report (SLAA412)
2. Texas Instruments, *Understanding the Terms and Definitions of LDO Voltage Regulators*, Application Report (SLVA079)
3. Texas Instruments, *Basic Calculation of a Buck Converter's Power Stage*, Application Report (SLVA477)

5.1 Trademarks

6 Terminology

LDO— Low Dropout Regulator

PSRR— Power Supply Ripple Rejection

PWM— Pulse Width Modulation

RF— Radio Frequency

MLCC— Multi-Layer Ceramic Capacitor

ESR— Equivalent Series Resistance

FB— Feedback

7 About the Author

JARI NIEMELÄ is an applications engineer at Texas Instruments, where he is responsible for developing reference design solutions, new product development, and customer support for the industrial segment. Jari brings to this role his extensive experience in applications engineering and validation as well as switched mode and linear regulator analog design expertise. Jari earned his Master of Science in Electrical Engineering (MSEE) from Oulu University in Oulu, Finland.

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