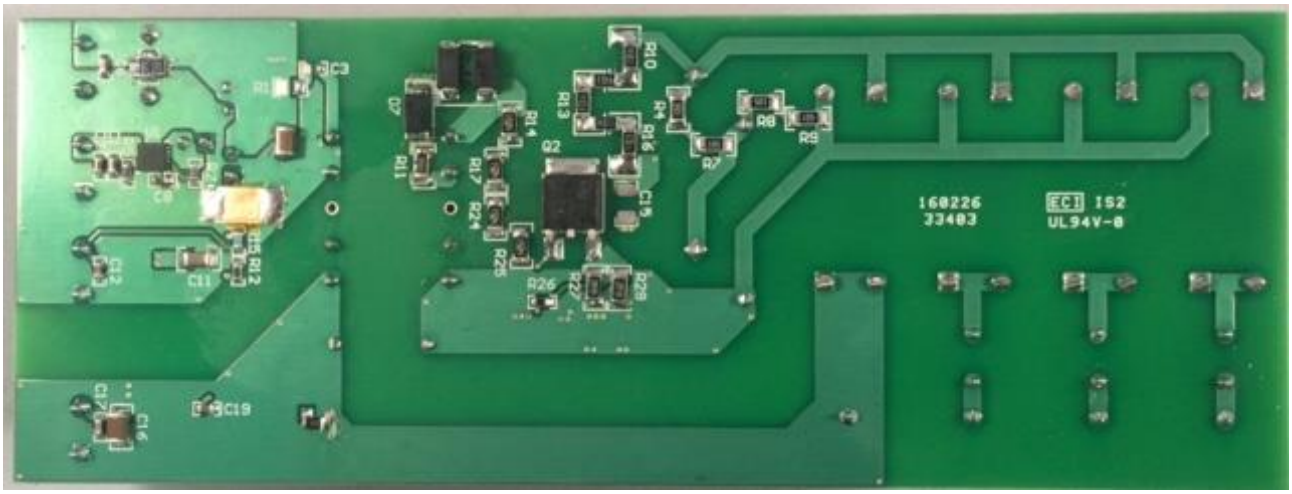
1 Photo

The photographs below show the PMP12082 Rev B assembly. This circuit was built on a PMP12082 Rev B PCB.

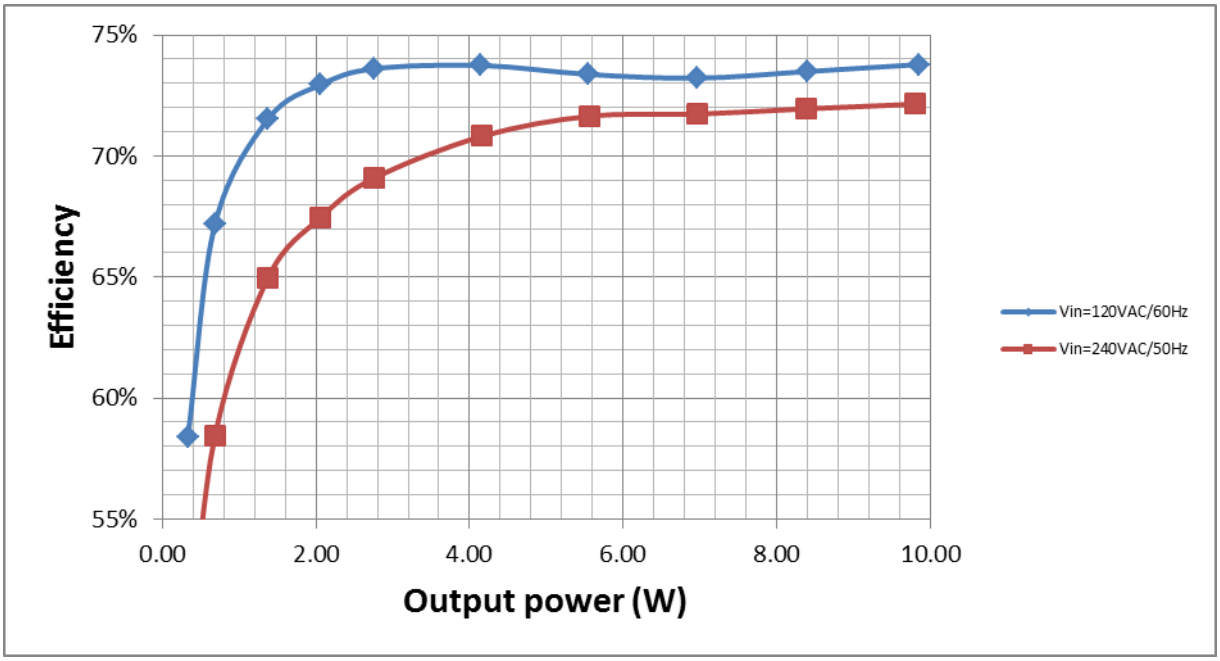
Top side

Bottom side



2 Flyback Efficiency

The efficiency data is shown in the tables below. J1 and J4 are opened during the test. Output current is drawn from J3.



V_{in}: 120V_{AC}/60Hz from Line1 to Line2

Vin(AC)	Iin(A)	Pin(W)	PF	Vout(V)	Iout(A)	Pout(W)	Eff (%)
120.08	0.2317	13.339	0.479	7.01	1.404	9.84	73.78%
120.11	0.2045	11.434	0.466	6.98	1.204	8.40	73.50%
120.15	0.1744	9.511	0.454	6.95	1.002	6.96	73.22%
120.19	0.1420	7.554	0.443	6.92	0.801	5.54	73.38%
120.21	0.1088	5.623	0.430	6.90	0.601	4.15	73.75%
120.23	0.0755	3.744	0.413	6.89	0.400	2.76	73.61%
120.24	0.0588	2.824	0.400	6.89	0.299	2.06	72.95%
120.26	0.0418	1.929	0.383	6.90	0.200	1.38	71.54%
120.28	0.0237	1.021	0.359	6.93	0.099	0.69	67.20%
120.30	0.0140	0.570	0.338	6.93	0.048	0.33	58.39%
120.31	0.0036	0.119	0.275	6.89	0.000	0.00	0.00%

V_{in}: 240V_{AC}/50Hz from Line1 to Line2

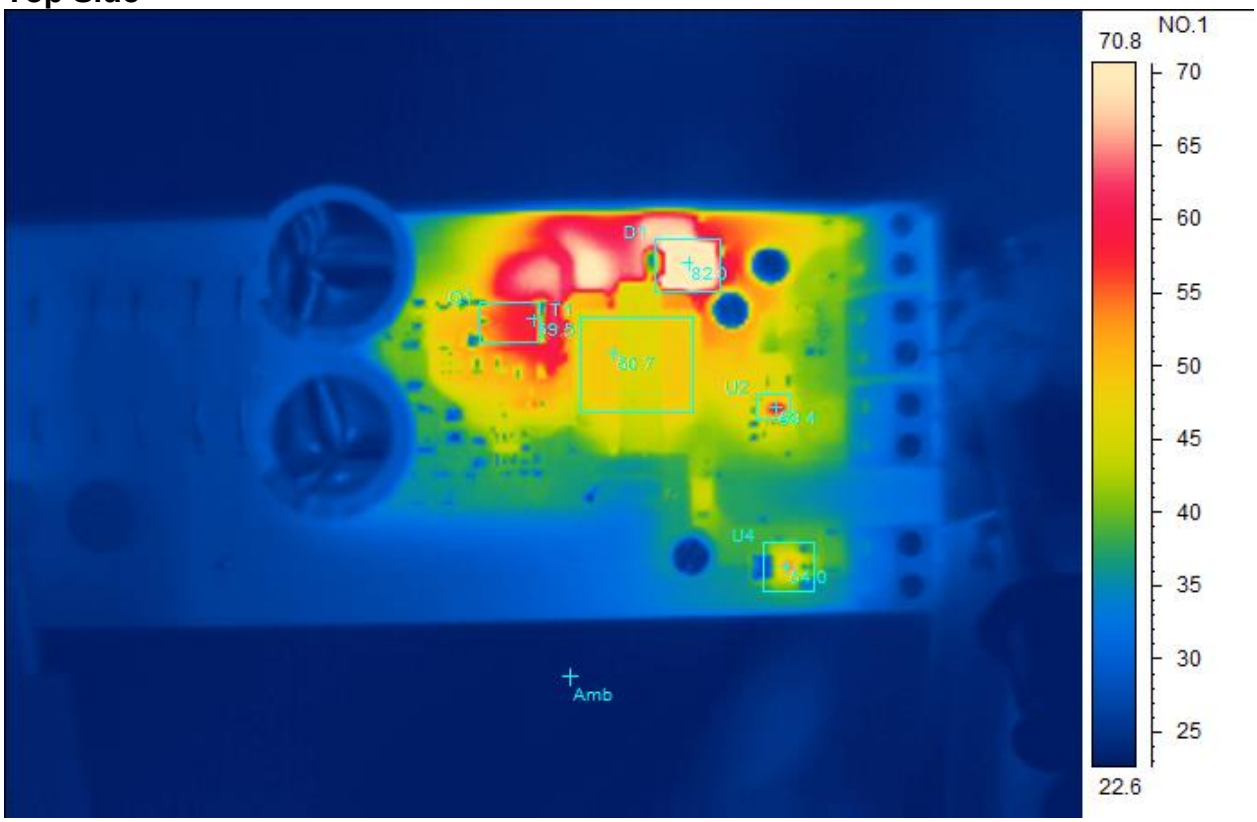
Vin(AC)	Iin(A)	Pin(W)	PF	Vout(V)	Iout(A)	Pout(W)	Eff (%)
240.00	0.1433	13.593	0.395	6.99	1.403	9.81	72.15%
240.00	0.1248	11.646	0.389	6.96	1.204	8.38	71.95%
239.90	0.1060	9.699	0.381	6.93	1.004	6.96	71.74%
240.00	0.0868	7.756	0.372	6.92	0.803	5.56	71.64%
240.00	0.0678	5.875	0.361	6.90	0.603	4.16	70.82%
240.00	0.0479	3.989	0.347	6.89	0.400	2.76	69.09%
240.00	0.0379	3.059	0.336	6.88	0.300	2.06	67.47%
240.00	0.0273	2.115	0.323	6.87	0.200	1.37	64.96%
240.00	0.0161	1.172	0.303	6.85	0.100	0.69	58.45%
239.90	0.0103	0.706	0.287	6.84	0.051	0.35	49.40%
239.90	0.0033	0.161	0.205	6.83	0.000	0.00	0.00%

3 Thermal Images

The thermal images below show a top view and bottom view of the board under 120V_{AC}/60Hz and 692V_{DC} input conditions. The ambient temperature was 20ºC with no forced air flow. The output was at full load (resistive): 7V/1A from J2, 3.3V/500mA from J5, 3.3V/300mA from J6

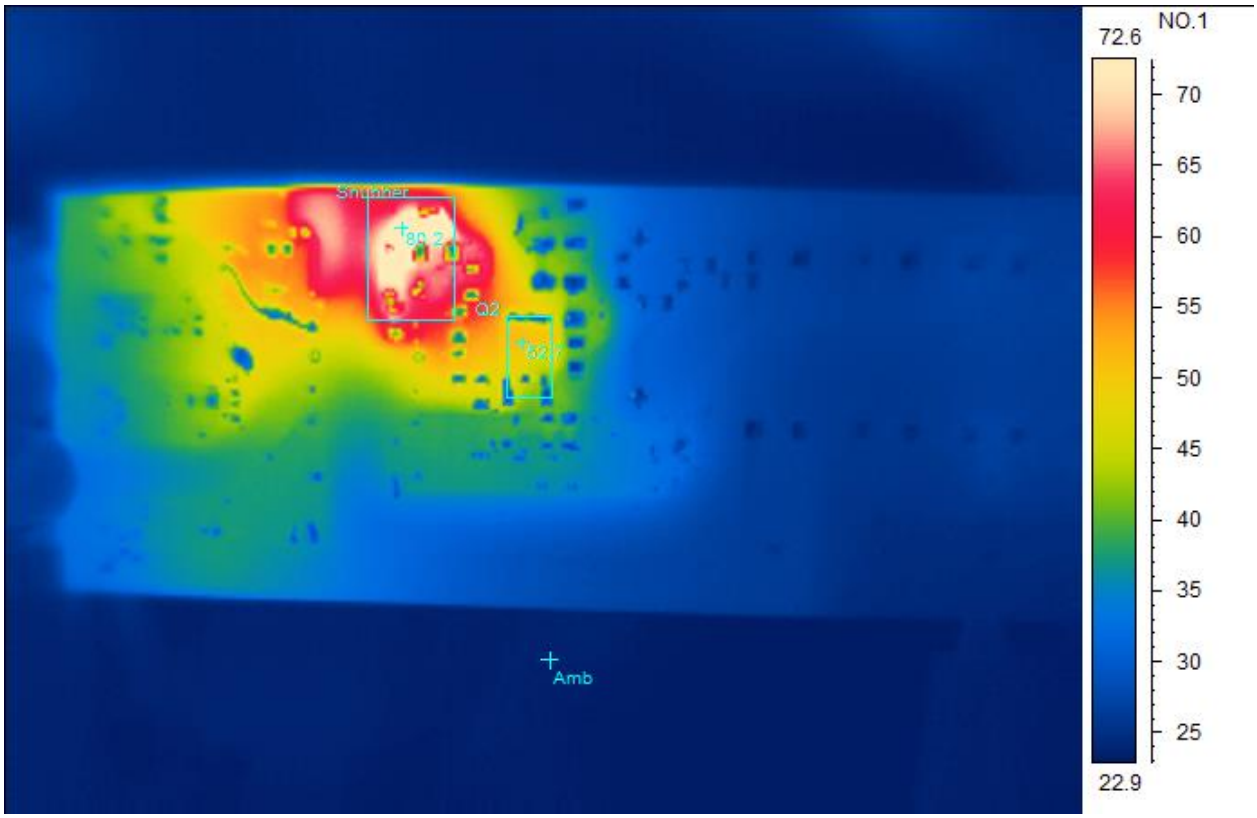
V_{in}: L-L 120V_{AC}/60Hz from Line1 to Line2

Top Side



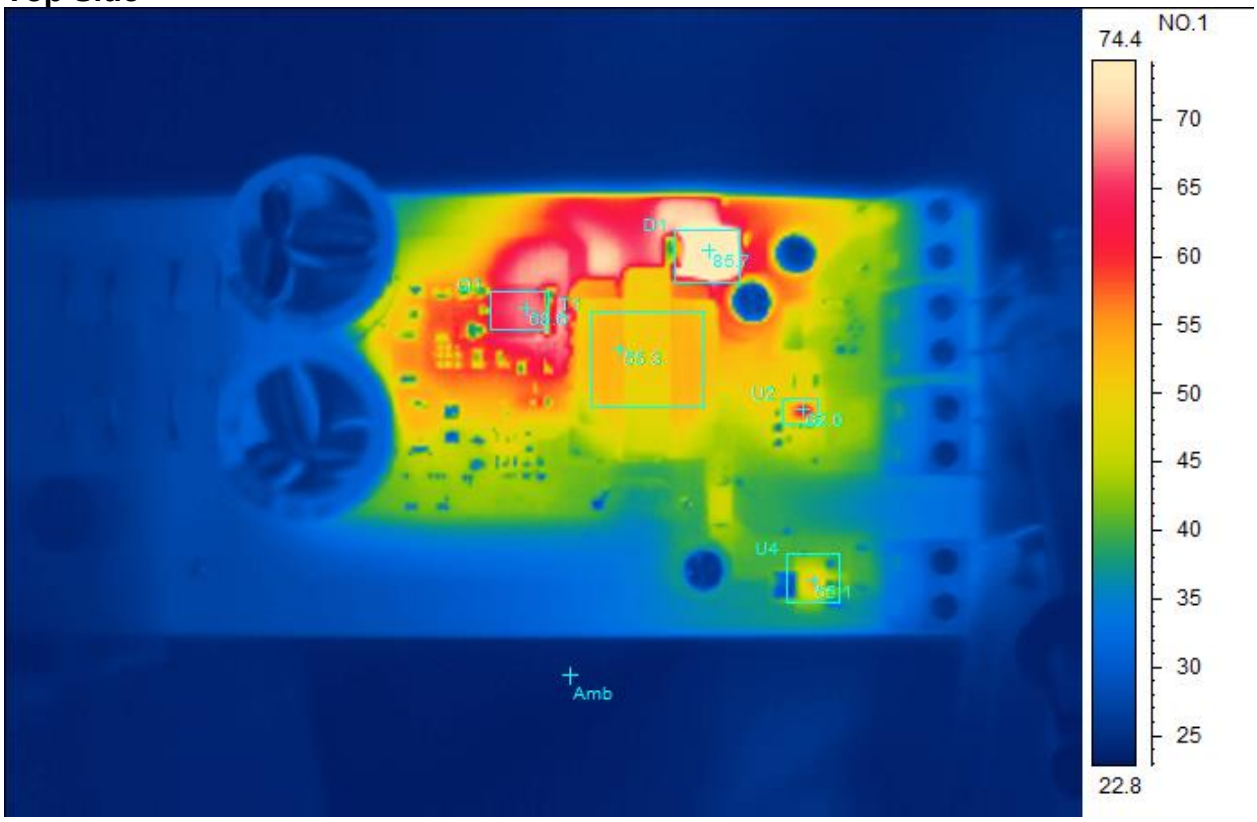
Spot analysis	Value
Amb Temperature	23.0°C
Area analysis	**Value**
D1Max	82.0°C
T1Max	50.7°C
Q1Max	59.5°C
U2Max	59.4°C
U4Max	54.0°C

V_{in}: L-L 120V_{AC}/60Hz from Line1 to Line2
Bottom Side



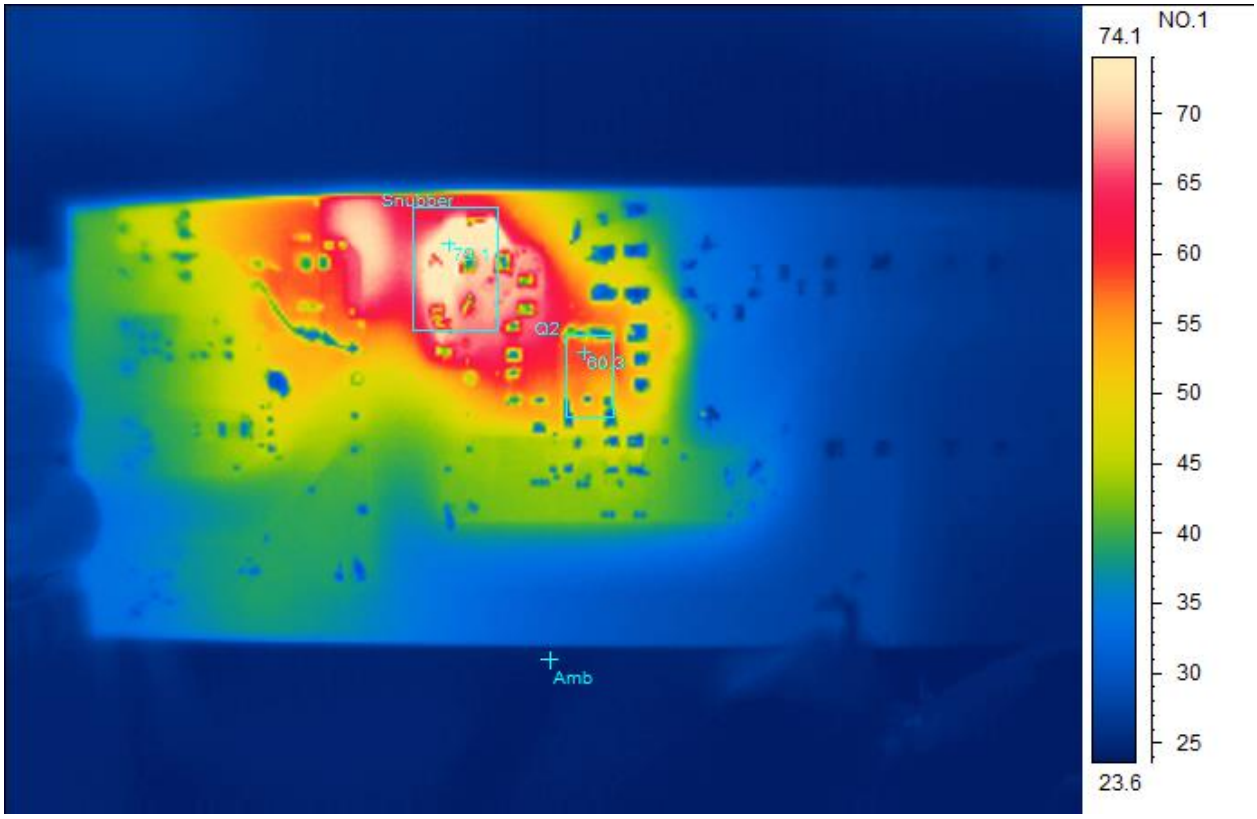
Spot analysis	Value
Amb Temperature	23.6°C
Area analysis	**Value**
SnubberMax	80.2°C
Q2Max	52.7°C

Vin=340VDC from Line1 to Line2 (340VDC is generated by an AC source with a voltage doubler circuit)
Top Side



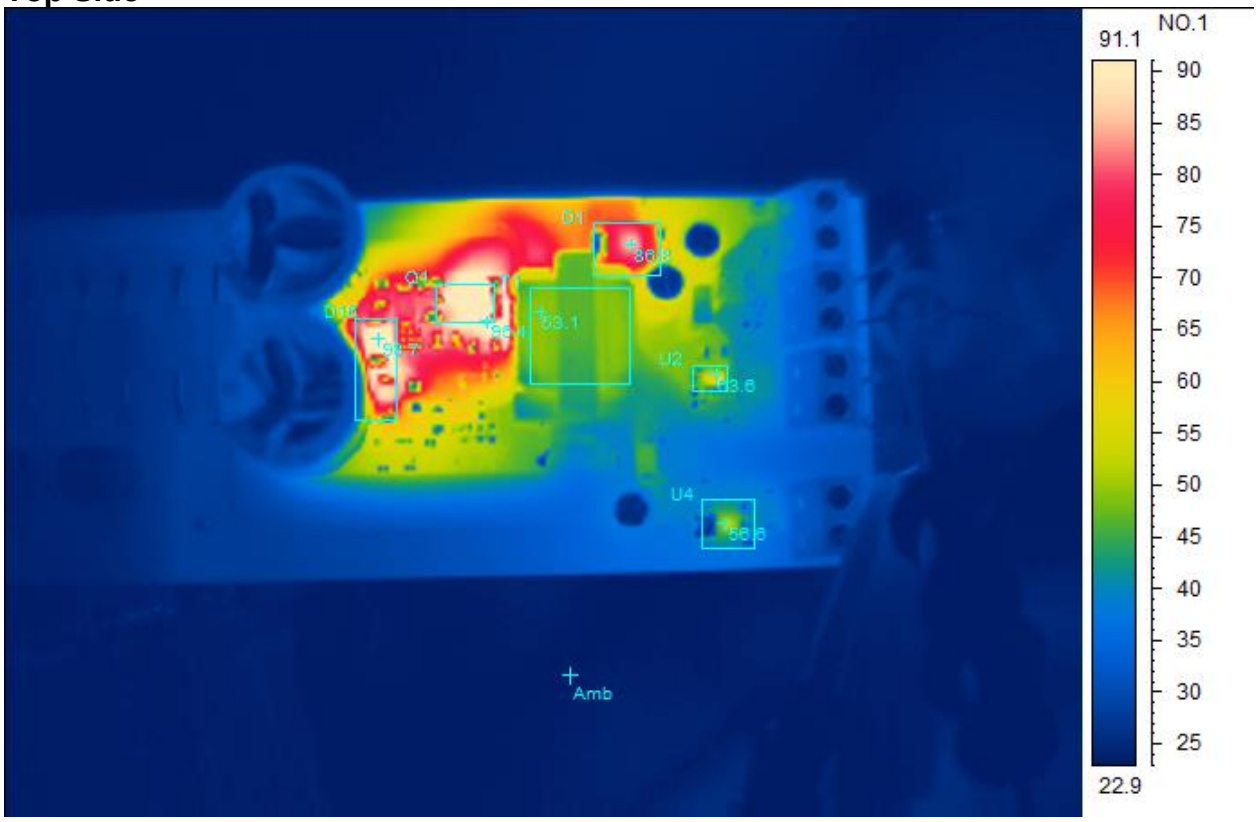
Spot analysis	Value
Amb Temperature	23.4°C
Area analysis	**Value**
D1Max	85.7°C
T1Max	55.3°C
Q1Max	68.6°C
U2Max	62.0°C
U4Max	55.1°C

Vin=340VDC from Line1 to Line2 (340VDC is generated by an AC source with a voltage doubler circuit)
Bottom Side



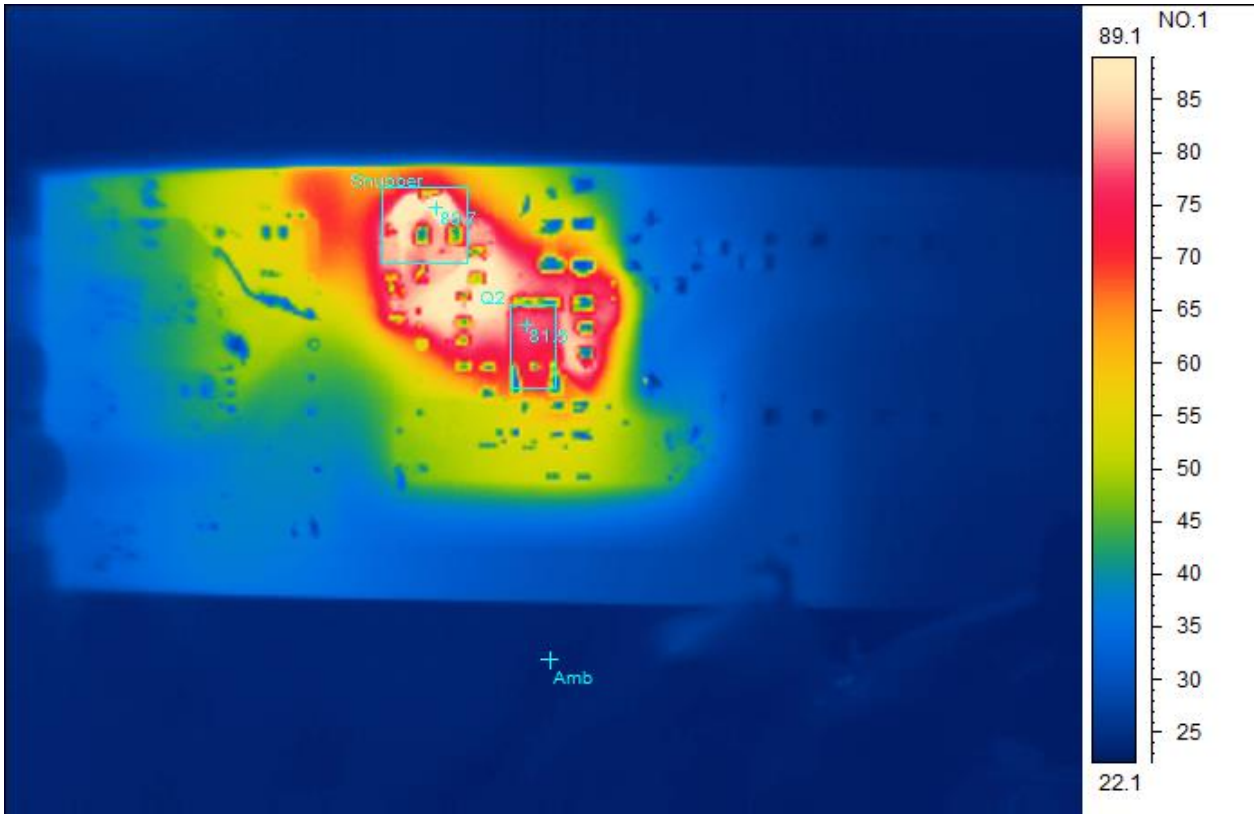
Spot analysis	Value
Amb Temperature	24.2°C
Area analysis	**Value**
SnubberMax	79.1°C
Q2Max	60.3°C

Vin=692VDC from Line1 to Line2 (692VDC is generated by an AC source with a voltage doubler circuit)
Top Side



Spot analysis	Value
Amb Temperature	23.4°C
Area analysis	**Value**
D1Max	86.8°C
T1Max	53.1°C
Q1Max	95.4°C
U2Max	63.6°C
U4Max	56.6°C
D16 Max	93.7°C

Vin=692VDC from Line1 to Line2 (692VDC is generated by an AC source with a voltage doubler circuit)
Bottom Side

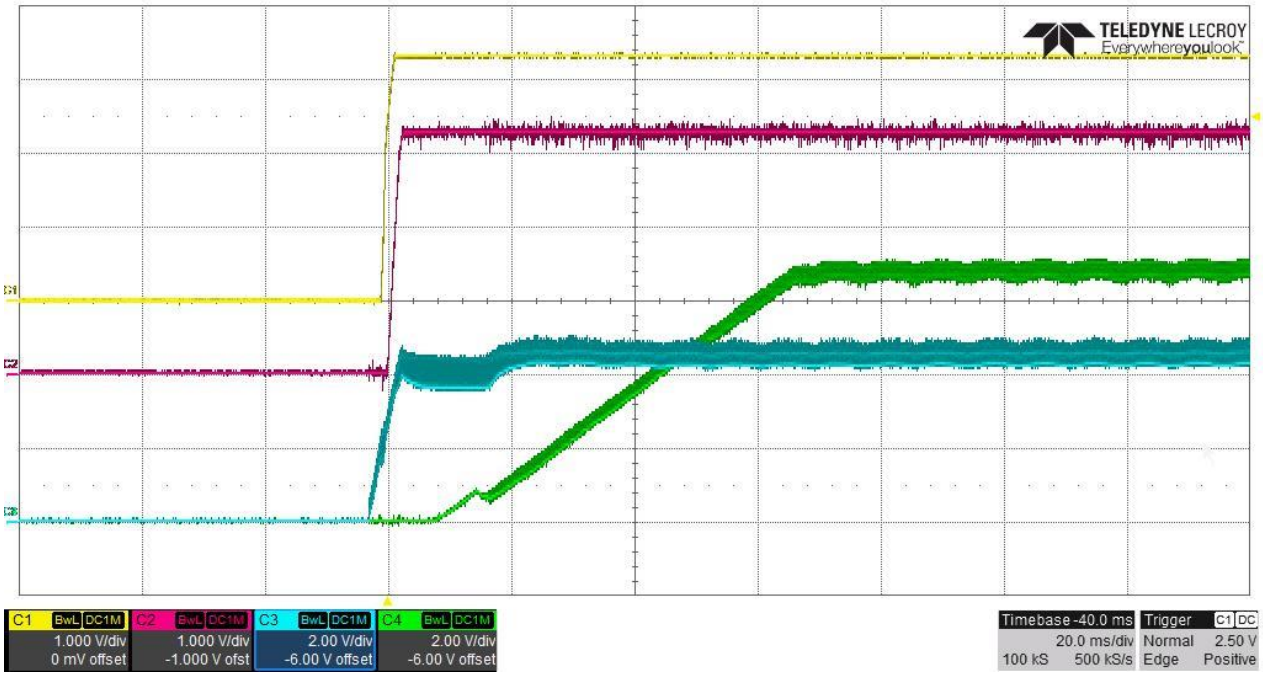


Spot analysis	Value
Amb Temperature	23.1°C
Area analysis	**Value**
SnubberMax	89.7°C
Q2Max	81.5°C

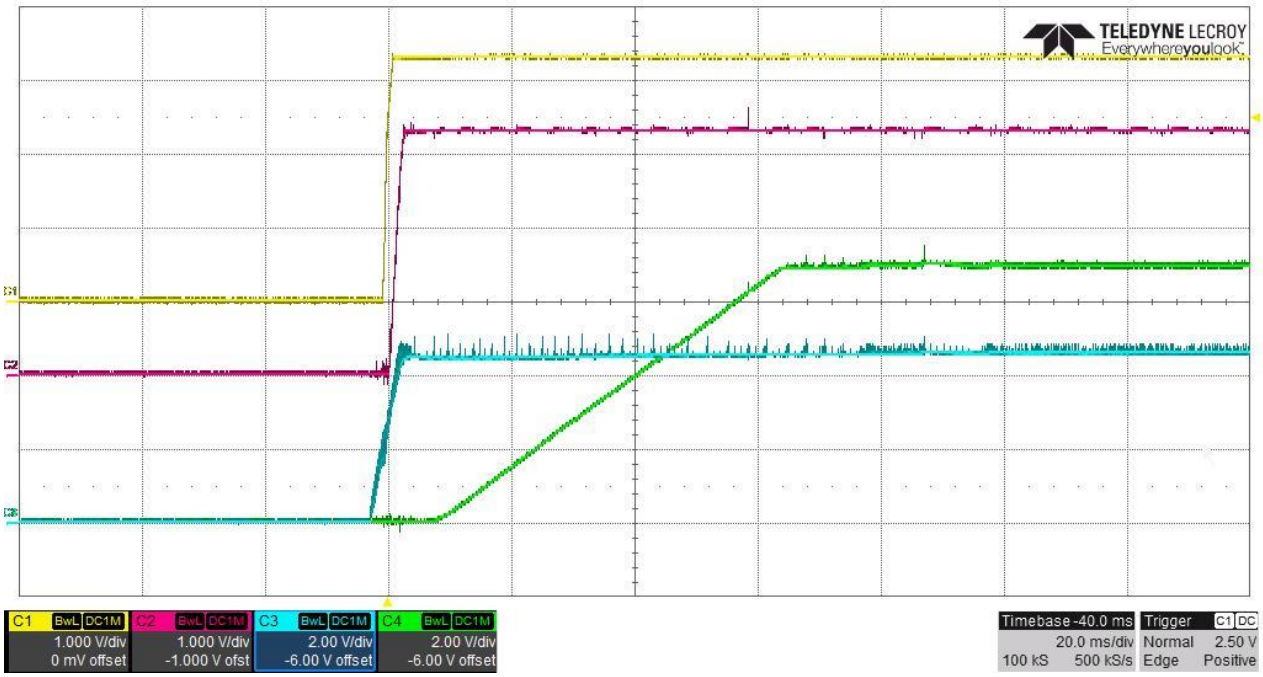
4 Startup Waveforms

The output voltages at startup are shown in the images below with resistive loads. CH1: Voltage after input rectifier, CH1: 3.3V(J6), CH2: 3.3V(J5), CH3: V(C18), CH4: 7V(J2)

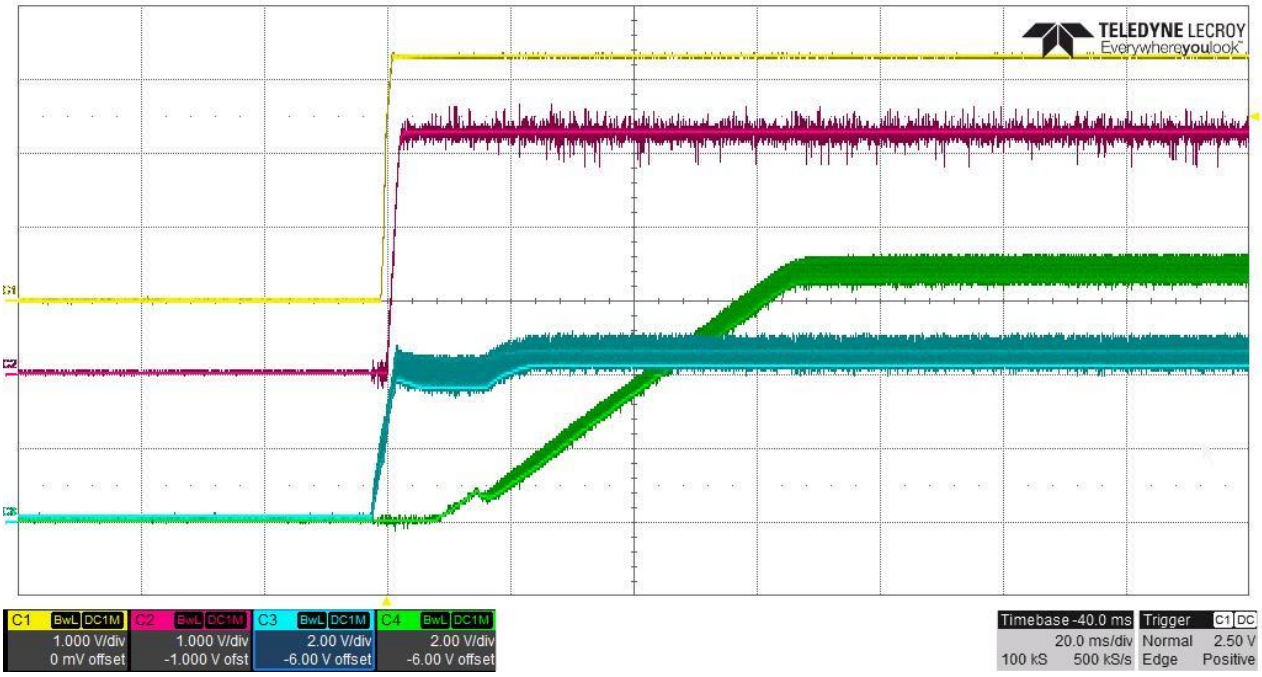
4.1 Start Up @ 80VDC input from Line1 to Line2, 7V/1A(J2), 3.3V/500mA(J5) and 3.3V/300mA(J6) outputs.



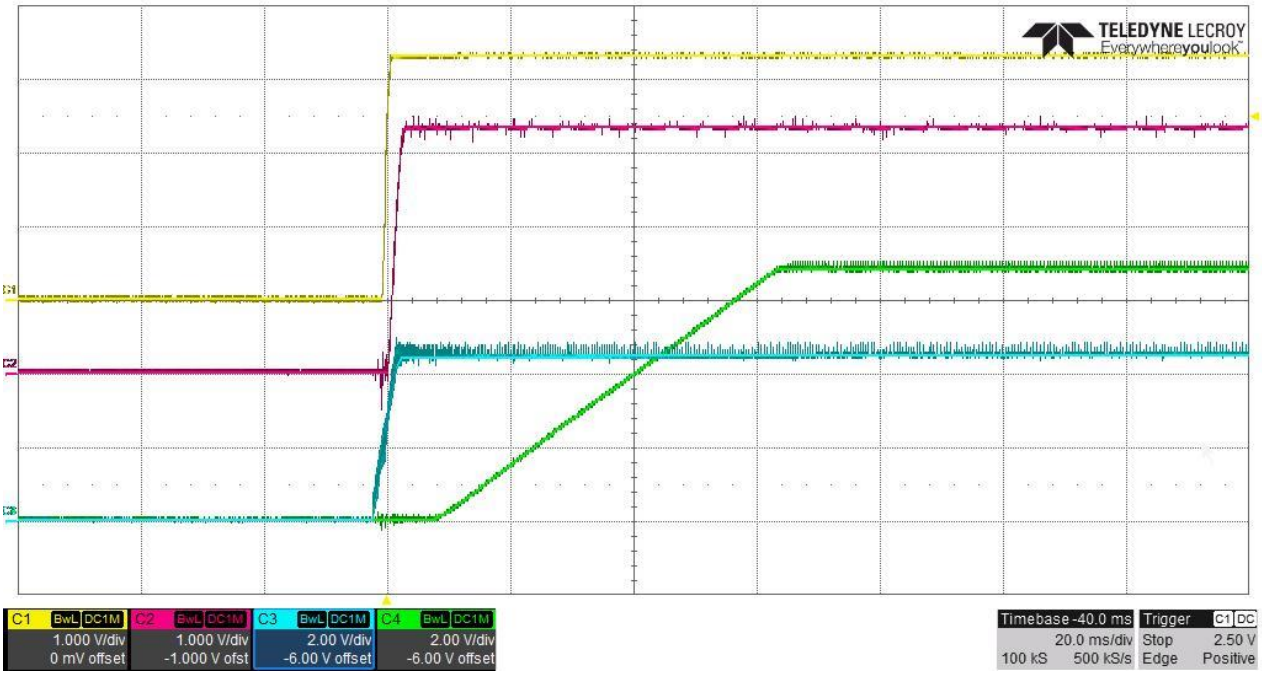
4.2 Start Up @ 80VDC input from Line1 to Line2 and no loads.



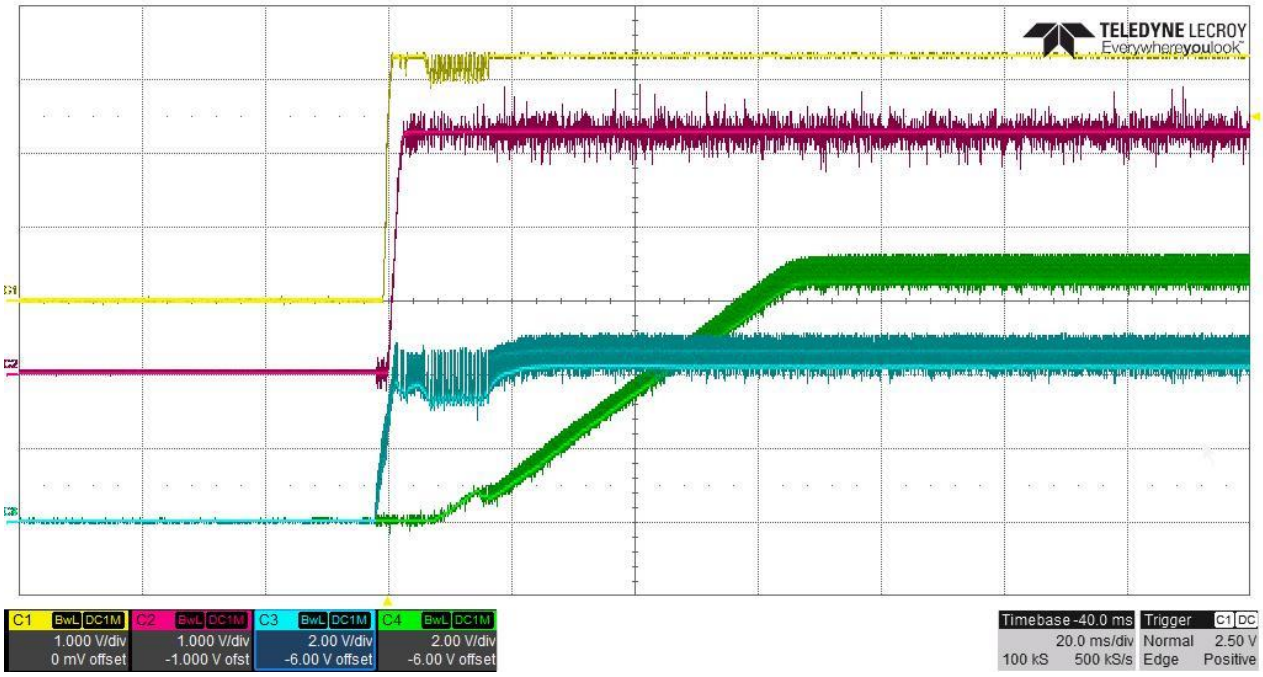
4.3 Start Up @ Vin=340VDC from Line1 to Line2 (340VDC is generated by an AC source with a voltage doubler circuit), 7V/1A(J2), 3.3V/500mA(J5) and 3.3V/300mA(J6) outputs.



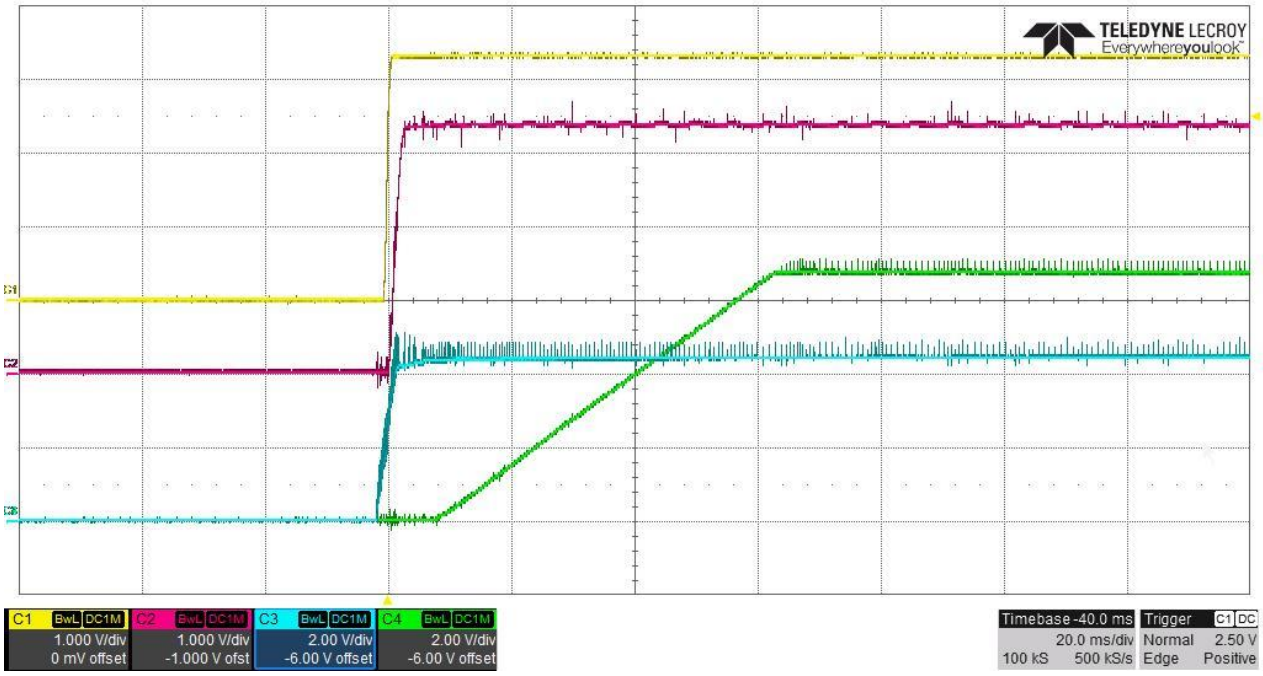
4.4 Start Up @ Vin=340VDC from Line1 to Line2 (340VDC is generated by an AC source with a voltage doubler circuit) input and no load.



4.5 Start Up @ Vin=692VDC from Line1 to Line2 (692VDC is generated by an AC source with a voltage doubler circuit), 7V/1A(J2), 3.3V/500mA(J5) and 3.3V/300mA(J6) outputs.



4.6 Start Up @ Vin=692VDC from Line1 to Line2 (692VDC is generated by an AC source with a voltage doubler circuit) input and no load.

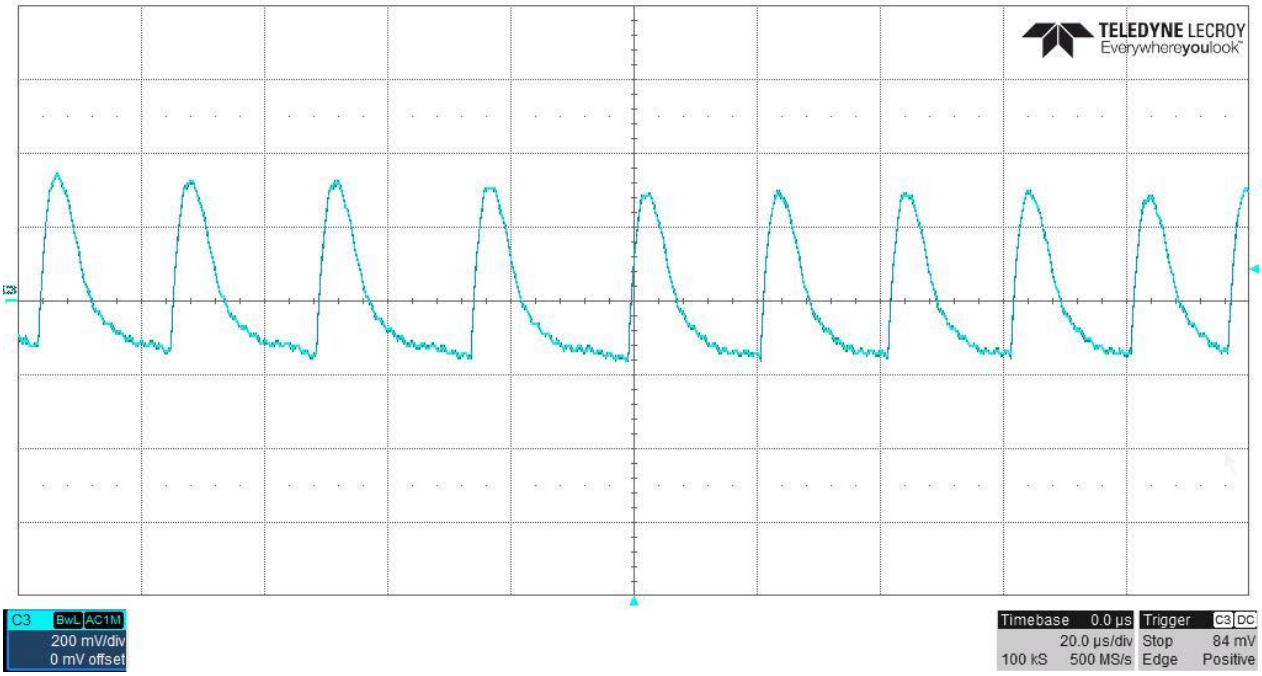


5 Output Ripple Voltages

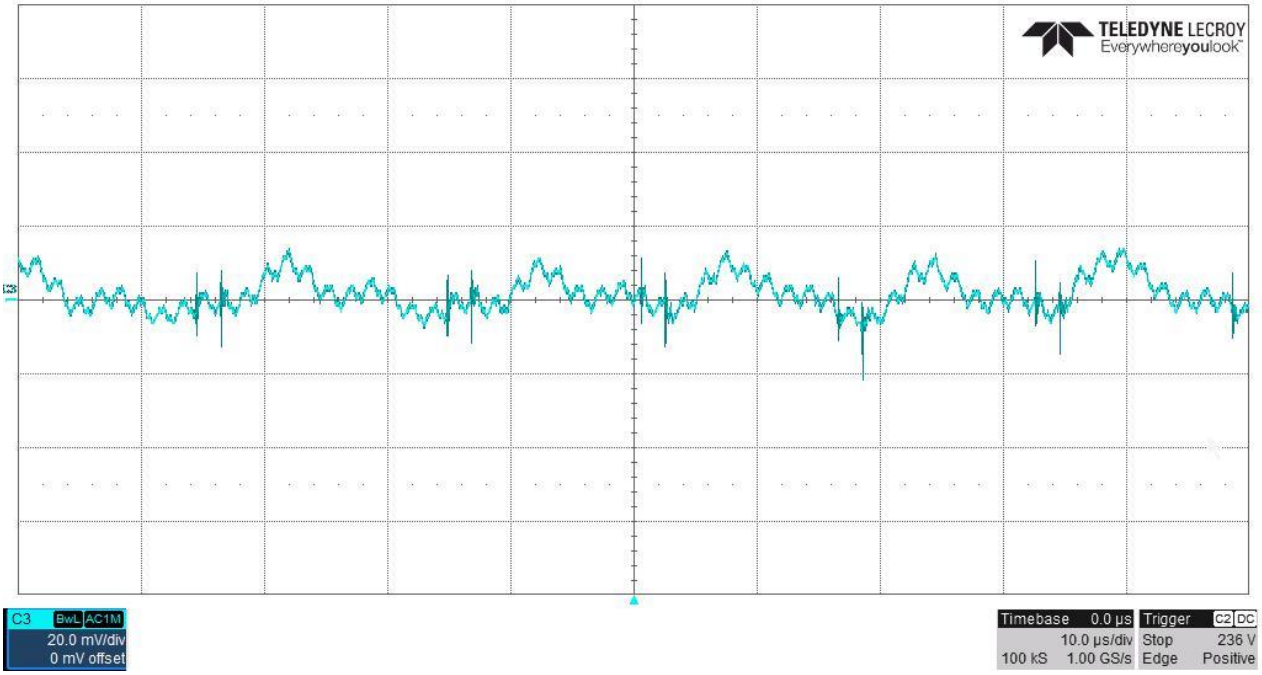
The output ripple voltages are shown in the plots below with resistive loads.

5.1 340VDC input from Line1 to Line2 with 7V/1A(J2), 3.3V/500mA(J5) and 3.3V/300mA(J6) outputs:

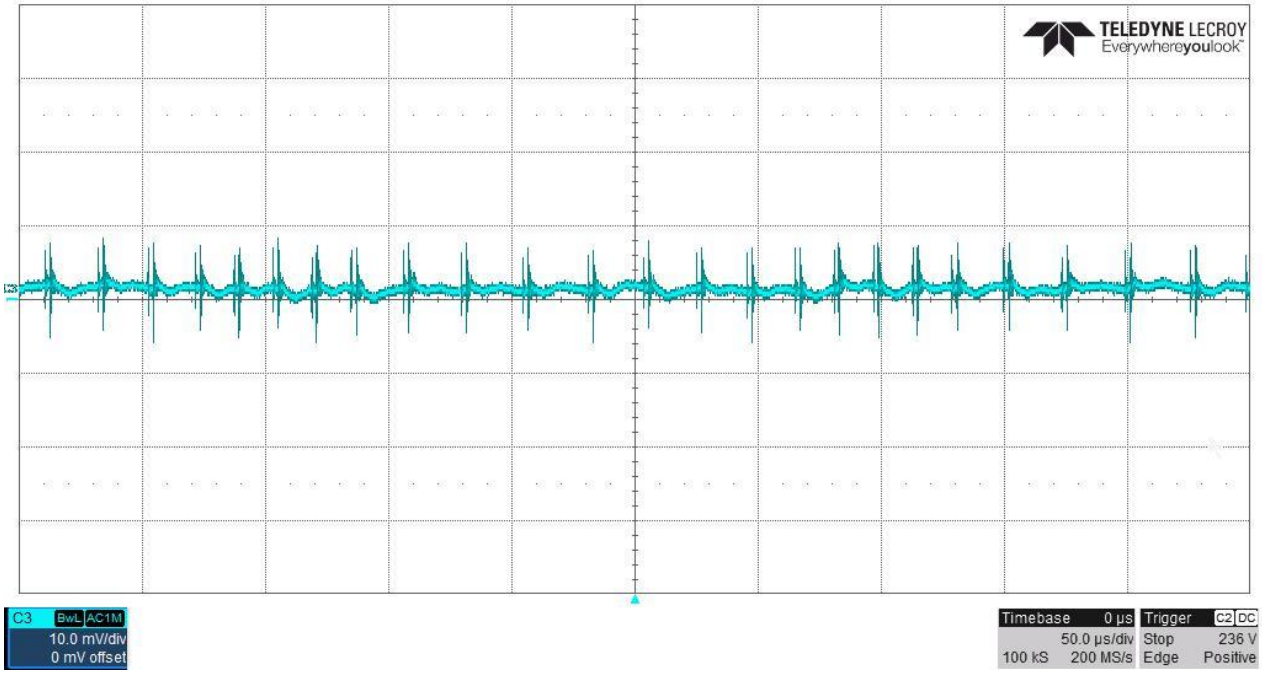
7V ripple:



3.3V(J5) ripple:

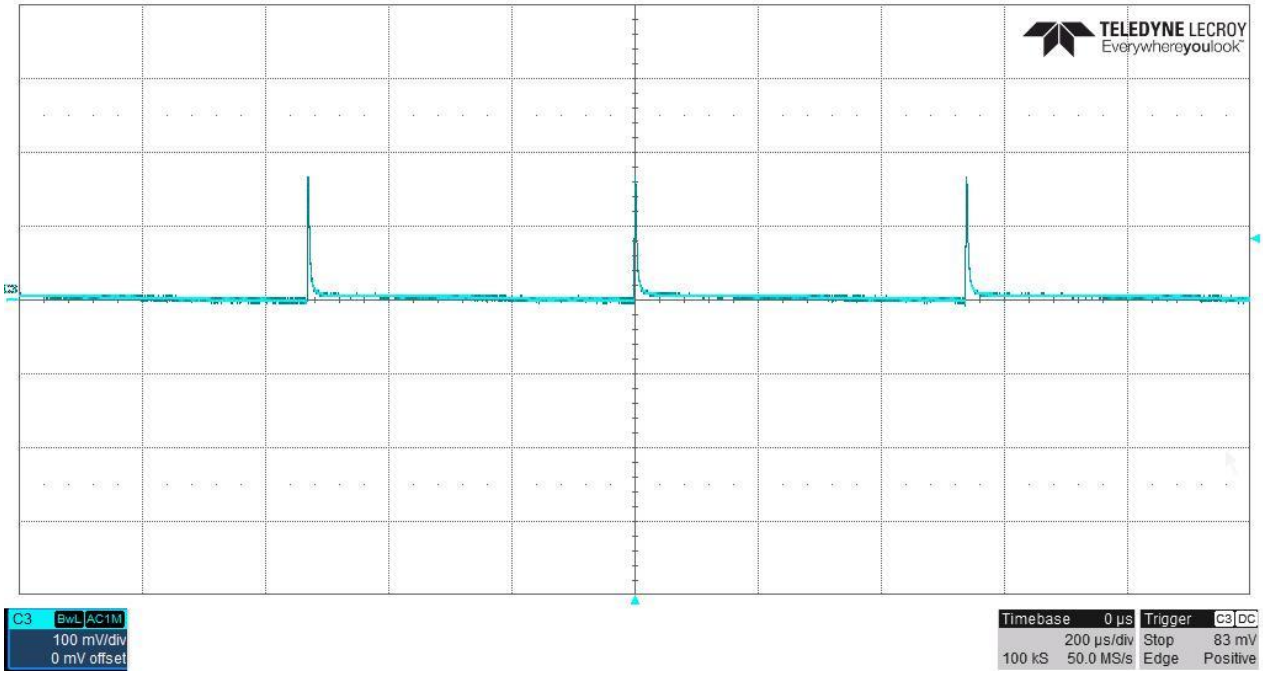


3.3V(J6) ripple:

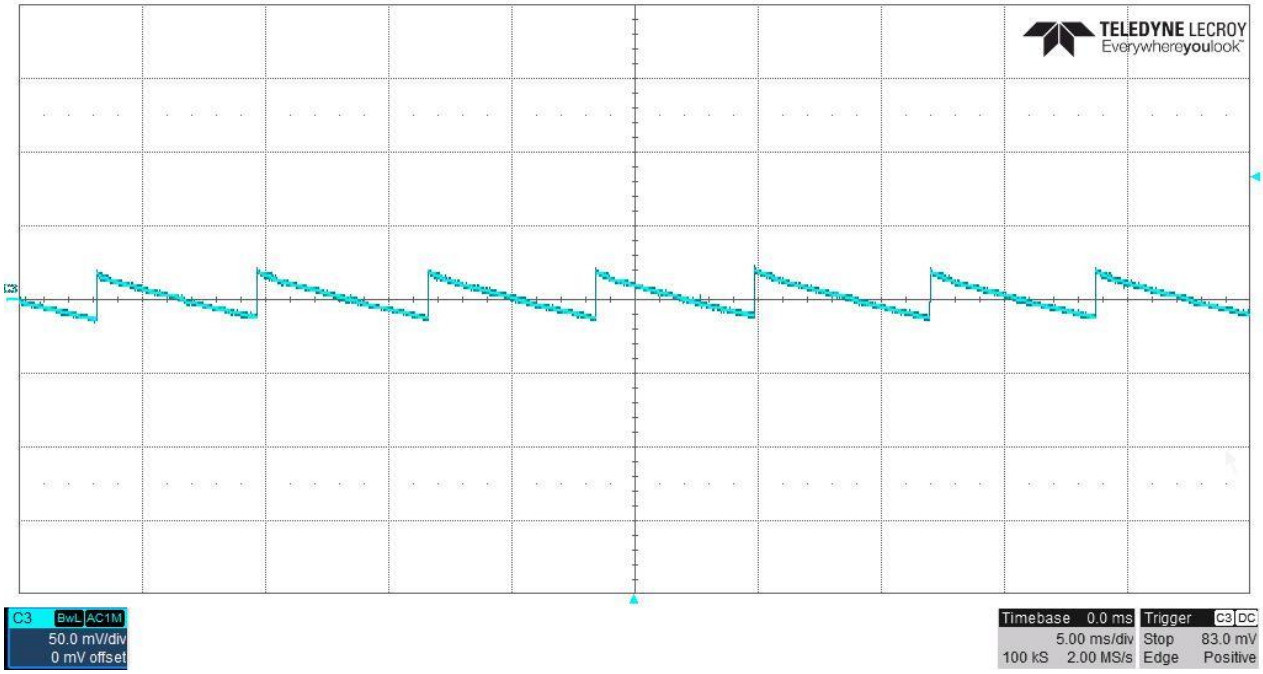


5.2 340VDC input from Line1 to Line2 with no loads:

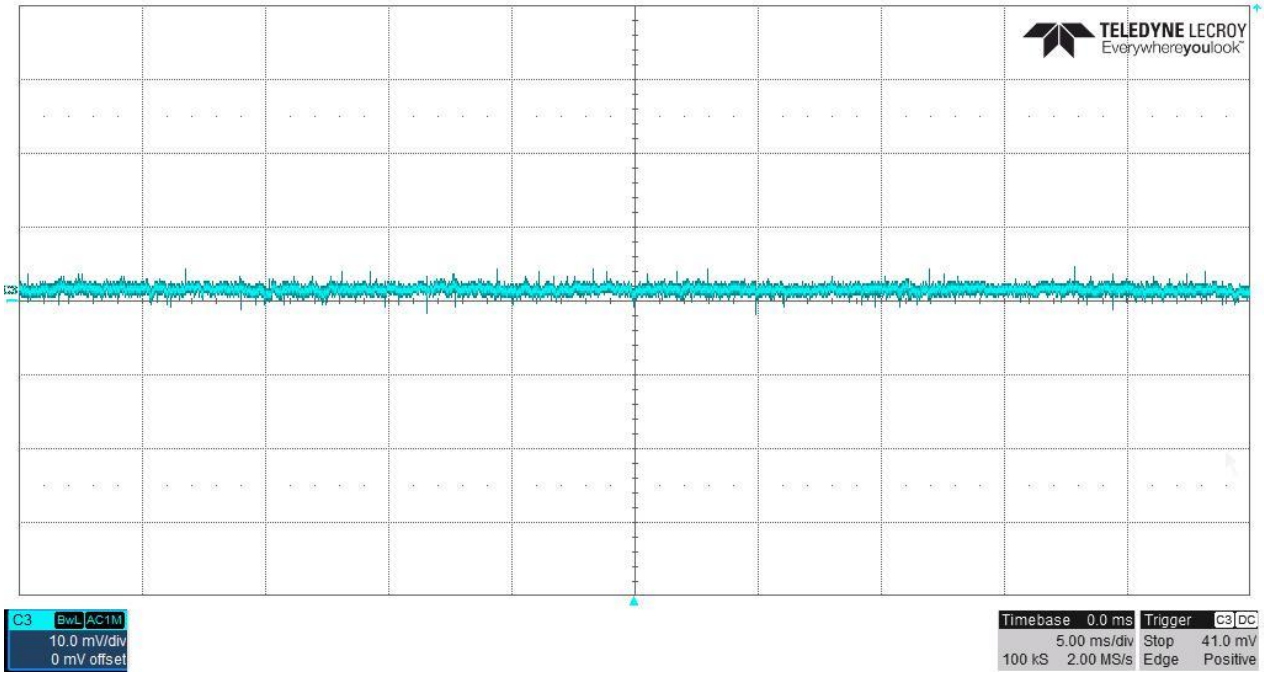
7V ripple:



3.3V(J5) ripple:

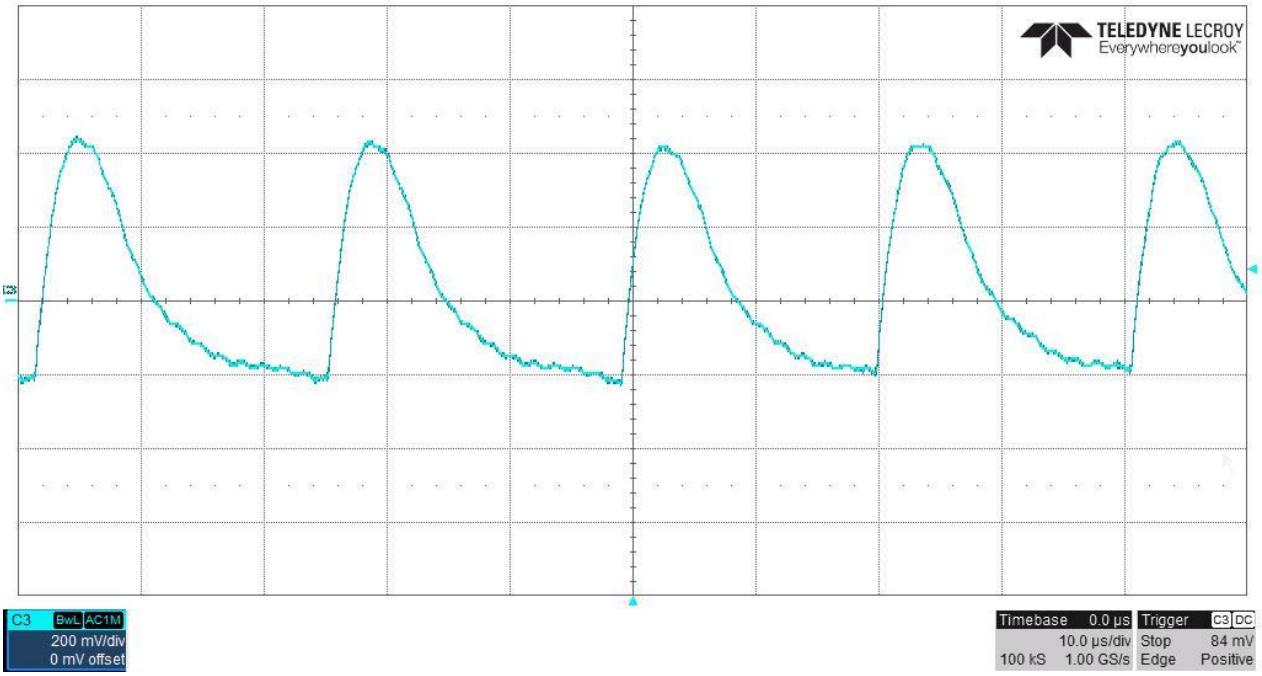


3.3V(J6) ripple:

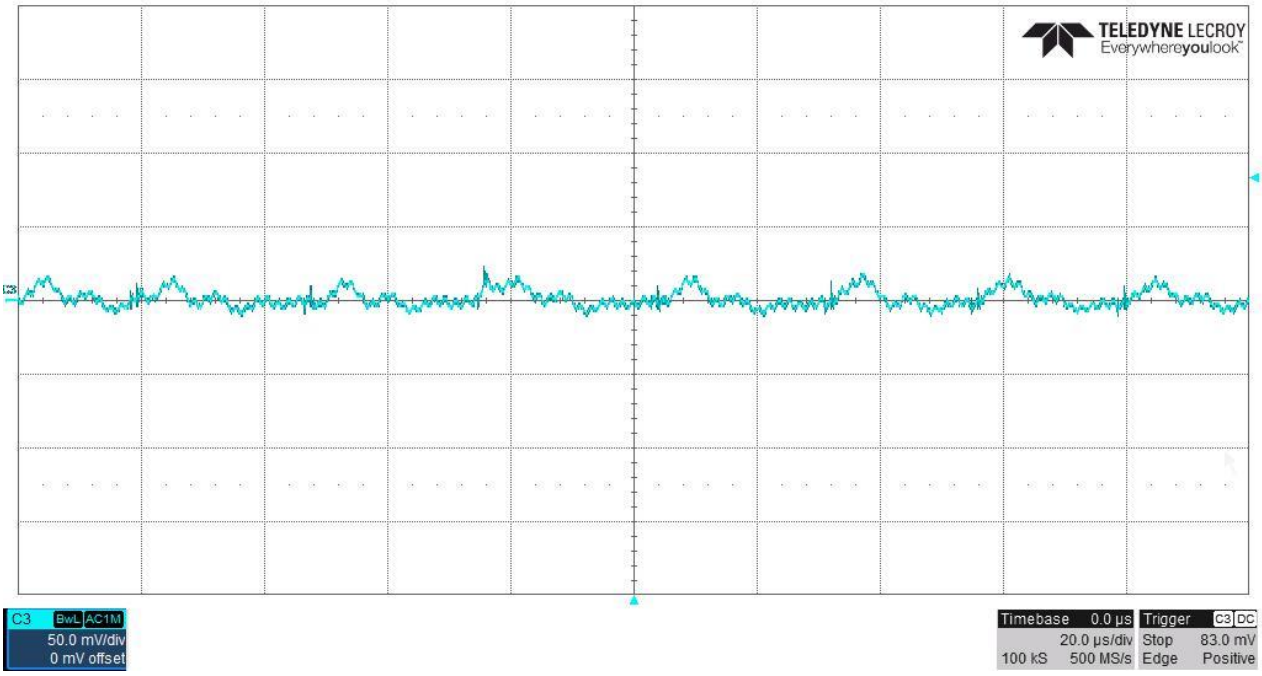


5.3 692VDC input from Line1 to Line2 with 7V/1A(J2), 3.3V/500mA(J5) and 3.3V/300mA(J6) outputs:

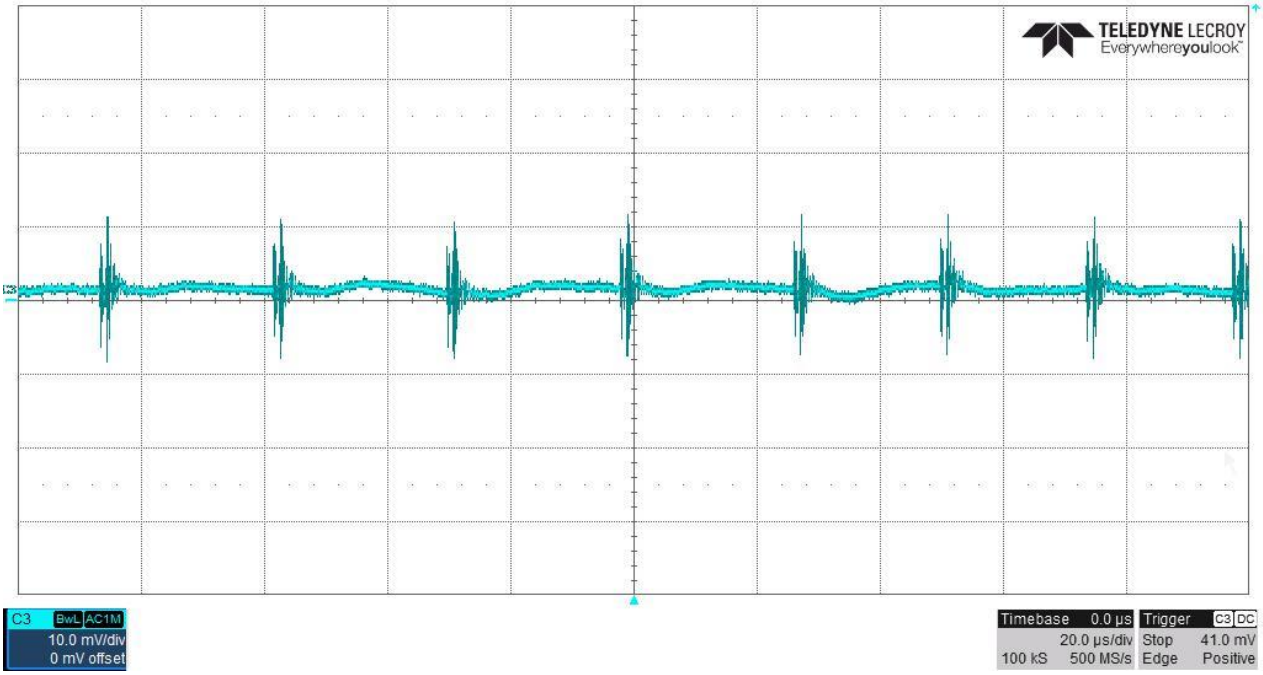
7V ripple:



3.3V(J5) ripple:

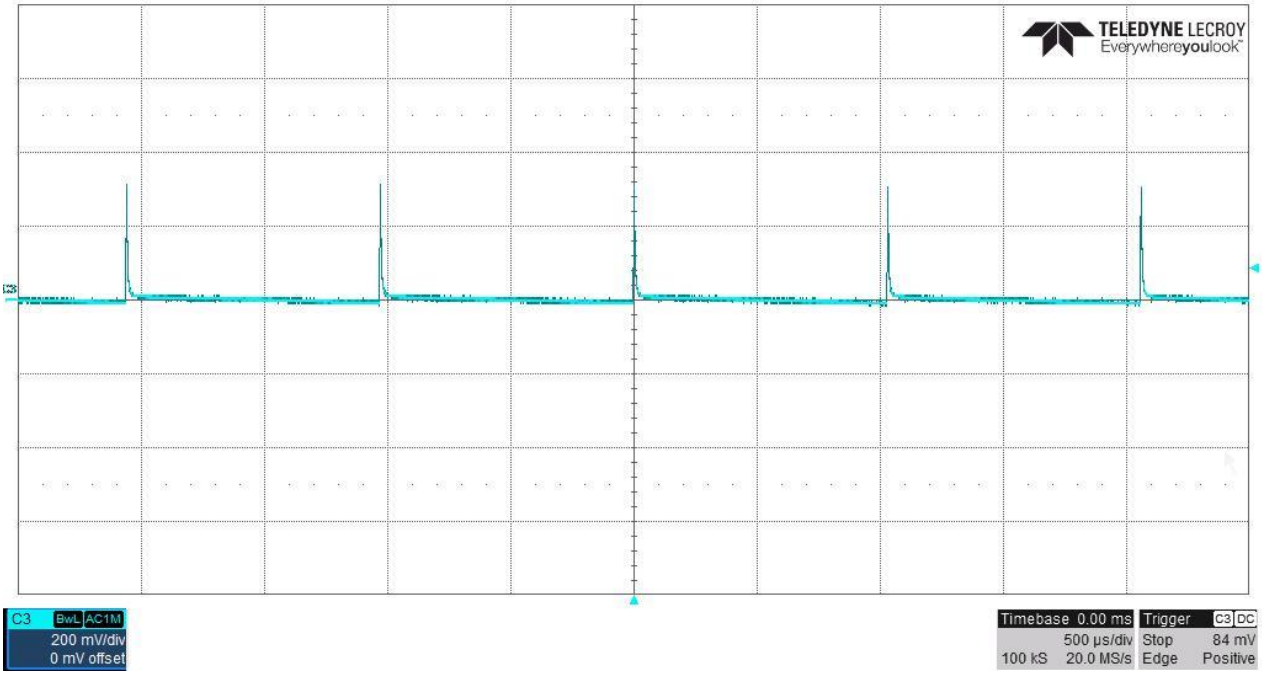


3.3V(J6) ripple:

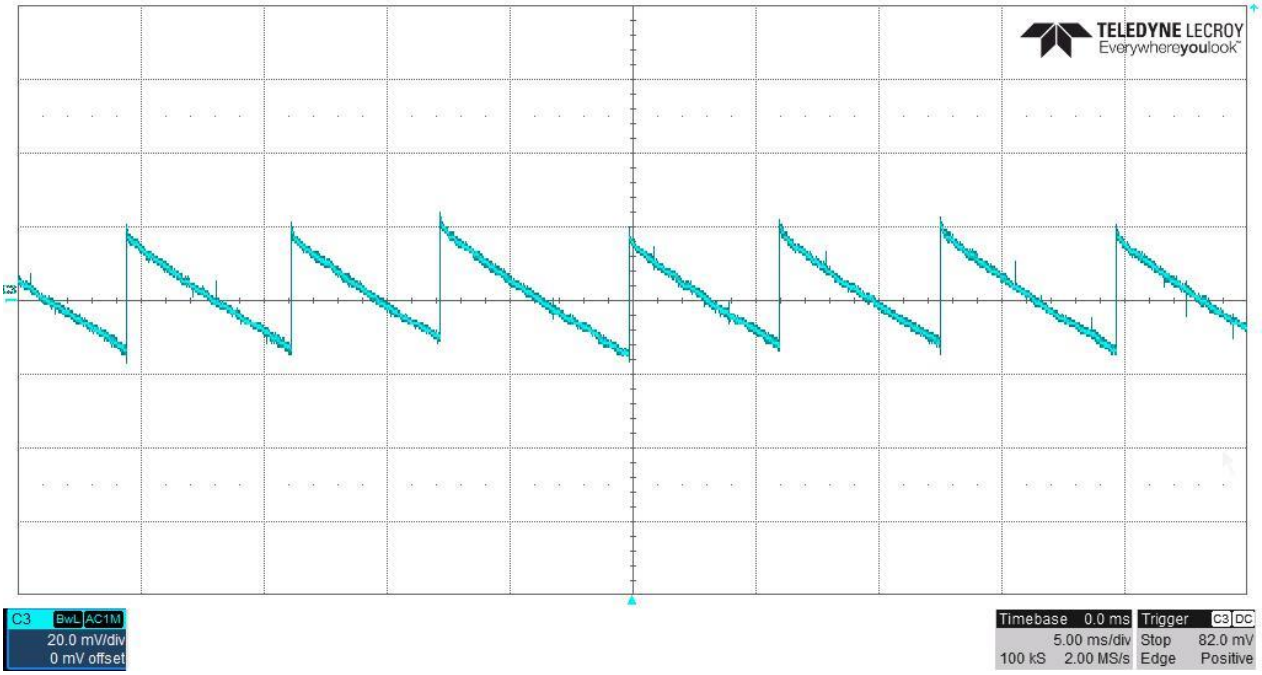


5.4 692VDC input from Line1 to Line2 with no loads:

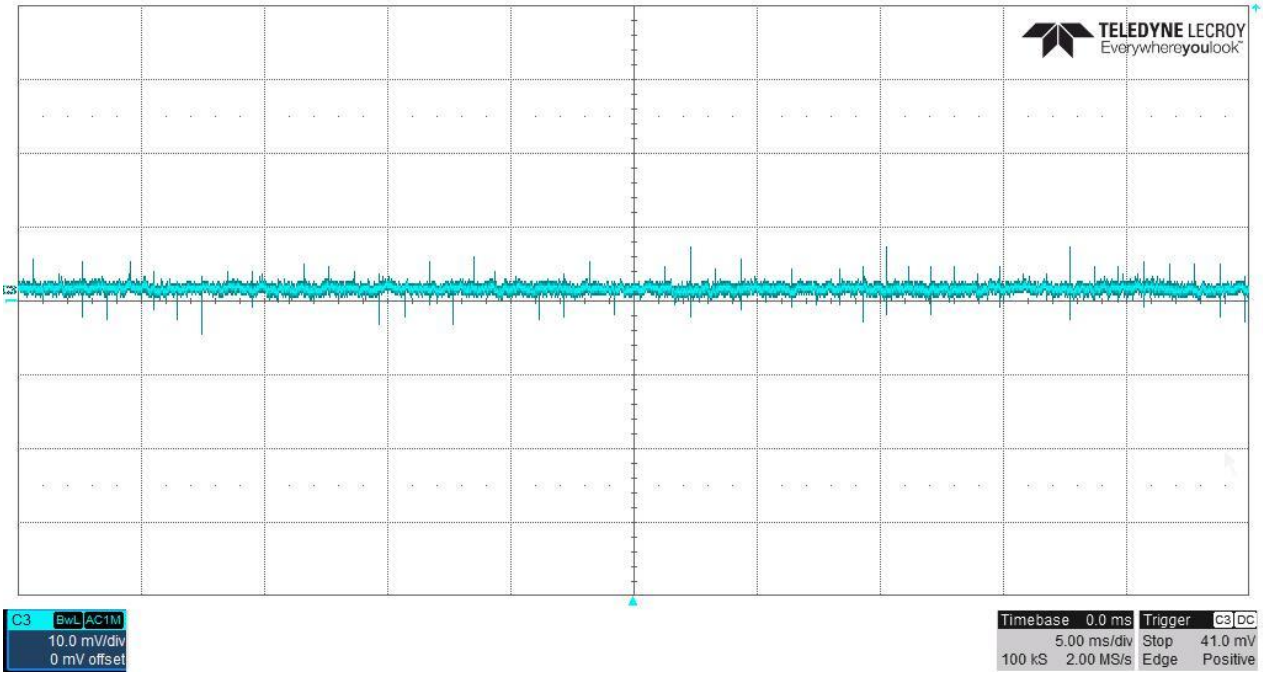
7V ripple:



3.3V(J5) ripple:



3.3V(J6) ripple:

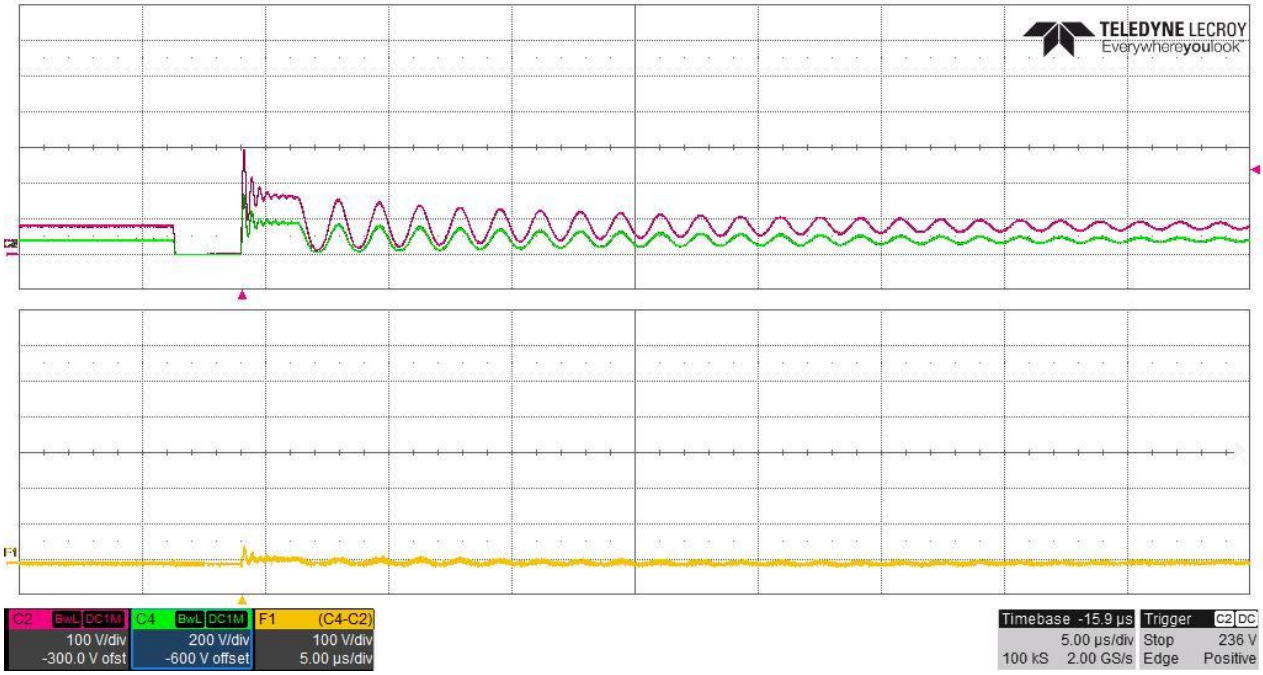


6 Switching Waveforms

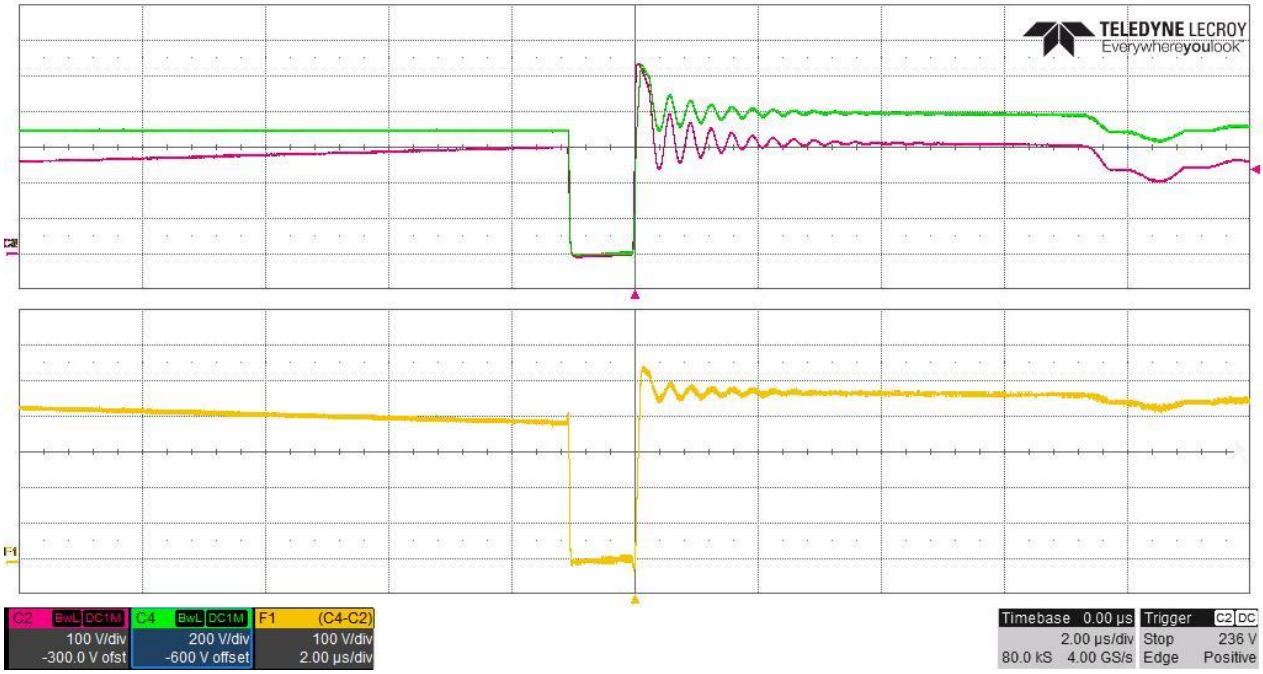
The images below show key switching waveforms of PMP12082RevB. The waveforms are measured with 7V/1.4A(J3) resistive load. Other outputs remain no load during the test. CH2: Q2 V_{DS}; CH4: T1 pin 2 to GND; F1: CH4 - CH2.

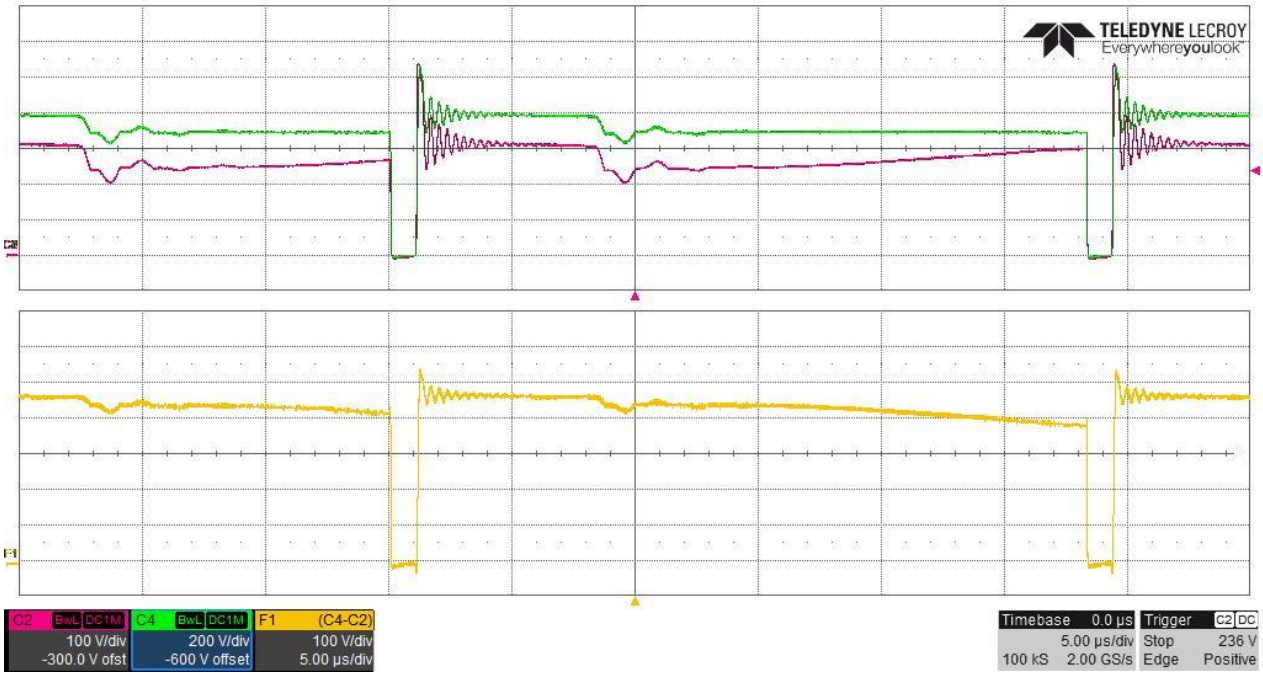
6.1 Vin: 80VDC from Line1 to Line2: 7V/1.4A(J3), other outputs remain not loaded.

6.2 Vin: 80VDC from Line1 to Line2: no load for all outputs.

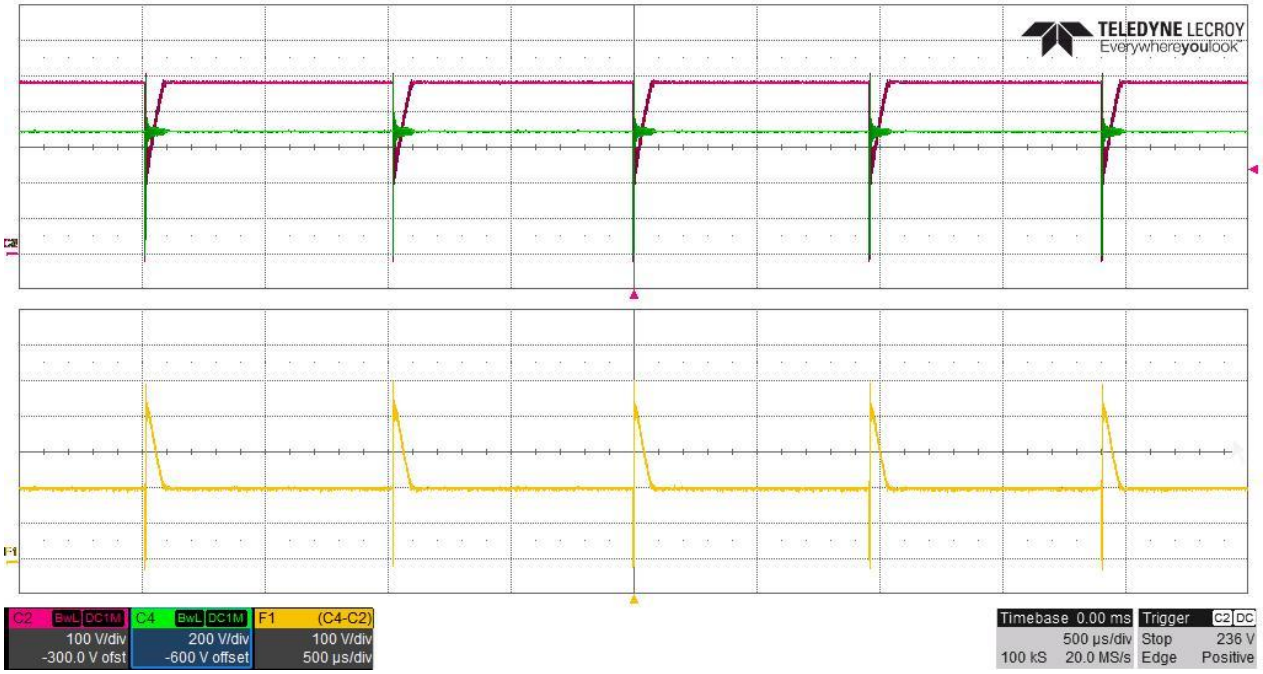


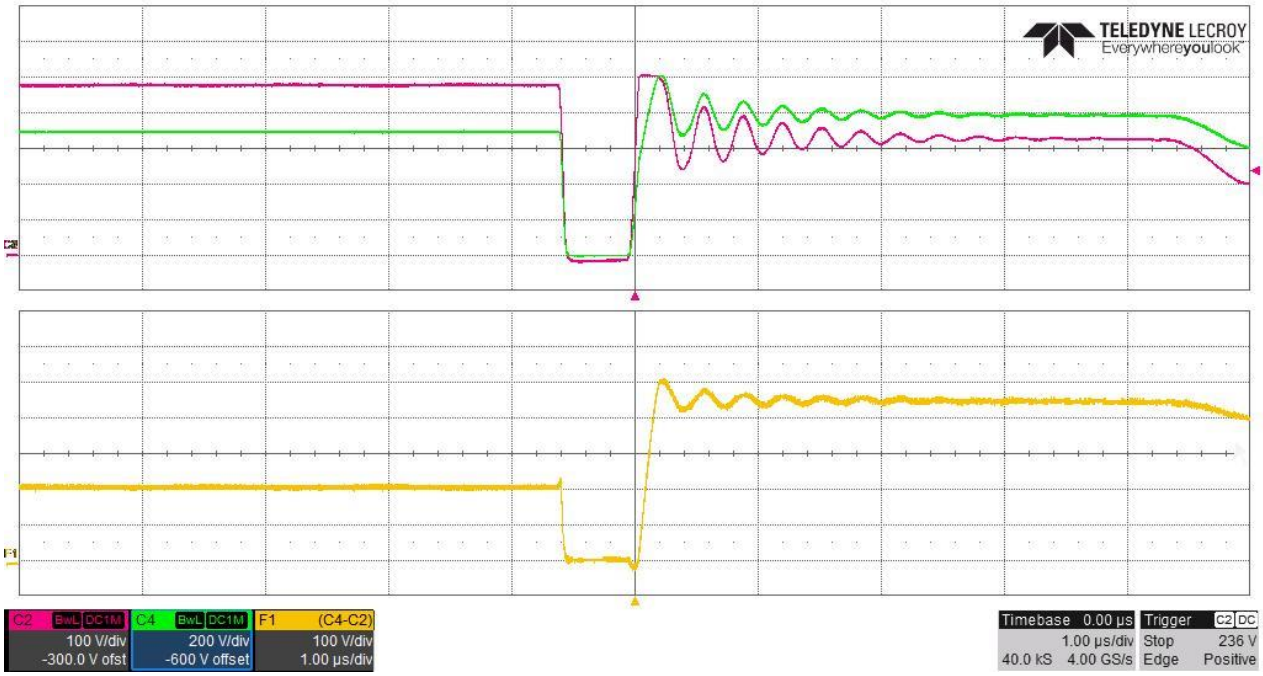
6.3 Vin=692VDC from Line1 to Line2 (692VDC is generated by an AC source with a voltage doubler circuit): 7V/1.4A(J3), other outputs remain not loaded.





6.4 Vin=692VDC from Line1 to Line2 (692VDC is generated by an AC source with a voltage doubler circuit): no load for all outputs.





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