TIDA-01162

Reference Design for Integrated Versus Discrete, Low-Voltage Motor Drive Comparison

Description

TIDA-01162 demonstrates the key differences between an integrated versus discrete low-voltage motor drive solution. The discrete solution is implemented using two large external MOSFETs while the integrated solution utilizes TI's DRV8850 brushed-DC motor driver. Both designs are implemented on a single printed-circuit board (PCB) for a quick comparison of the two solutions.

Resources

TIDA-01162	Design Folder
DRV8850	Product Folder
MSP430G2553	Product Folder
MSP-EXP430G2 LaunchPad™	Product Folder

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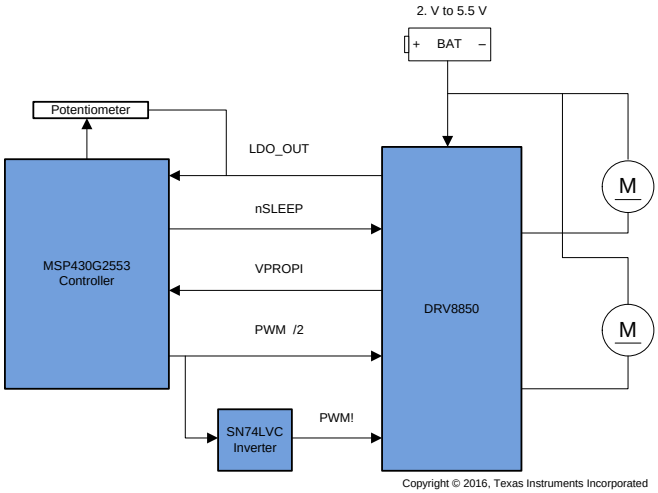
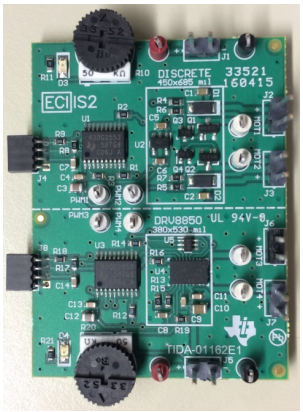
Features

- Lower Component Count
- Smaller Form Factor
- Solution More Economical
- Slew Rate Adjustment
- Protection
- Current Limiting

Applications

- RC Helicopters and Cars
- Personal Care Devices
- Robotics
- High-Current Battery-Powered Devices





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Overview

1.1 System Description

TIDA-01162 is a comparison design that addresses how to drive unidirectional motors used in low-cost consumer drone applications. Common designs use discrete parts to drive these motors, such as MOSFETs, regulators, diodes, and other simple passive devices. This TI design reduces the component count by implementing a single, integrated motor driver, the DRV8850. The logic signals used for this design are supplied by an ultra-low-power microcontroller (MCU), MSP430G2553.

The pulse width modulation (PWM) signals generated by the TI MSP430™ MCU are used to control the internal gates of the low-side drivers of the DRV8850 and spin the unidirectional motors connected to this device. Using a potentiometer connected to the MSP430 device, the speed of the motors can be changed by adjusting the duty cycle of the PWM signals supplied to the motor driver. As the duty cycle increases, the speed of the motors increases proportionally.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage	Input voltage from battery
Current sensing	Using VPROPI feature
Slew rate and time delay	From 70 ns to 70 µs
Protection	Overcurrent, overvoltage lockout (OVLO), and undervoltage lockout (UVLO)
Microcontroller	MSP430G2553 programmed in circuit using a four-wire serial peripheral interface (SPI)
Driver	DRV8850 brushed-DC motor driver

1.3 Block Diagram

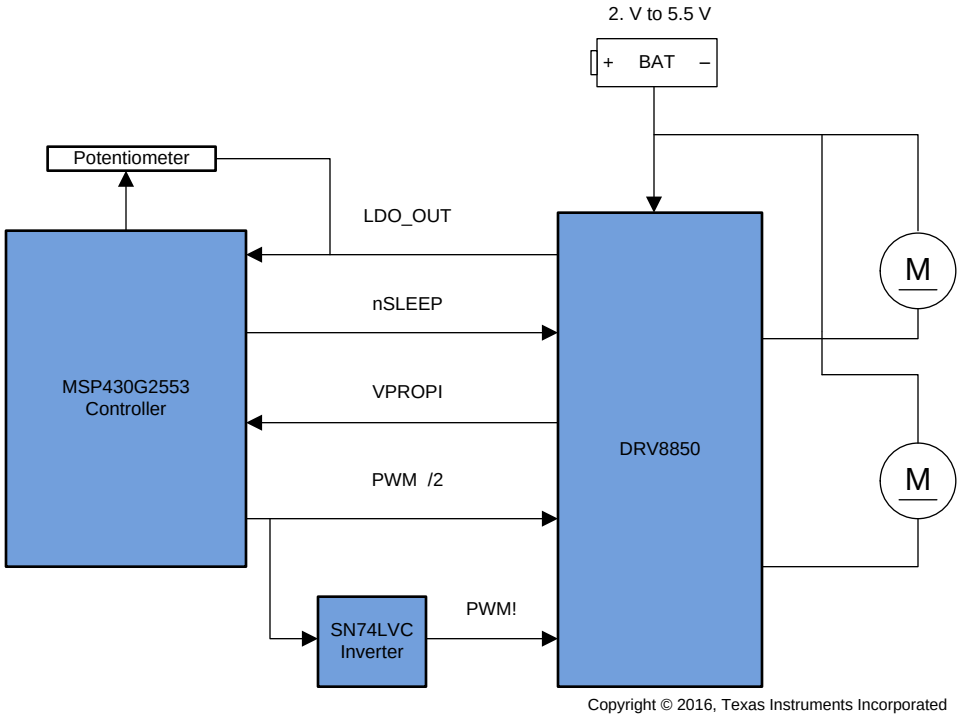


Figure 1. System Block Diagram

1.4 Highlighted Products

1.4.1 DRV8850 Device

The DRV8850 device provides a motor driver plus low-dropout (LDO) voltage regulator solution for consumer products, toys, and other low-voltage or battery-powered motion-control applications. The device has one H-bridge driver to drive a DC motor, a voice-coil actuator, a winding of a stepper motor, a solenoid, or other devices. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the load. An internal charge pump generates the required gate-drive voltages.

The DRV8850 device supplies up to 5 A of continuous output current (with proper PCB heat sinking) and up to 8-A peak current. The device operates on a supply voltage from 2 V to 5.5 V. Figure 2 shows the DRV8850 functional block diagram.

A LDO linear voltage regulator is integrated with the motor driver to supply power to MCUs or other circuits. The LDO voltage regulator can be active in device sleep mode so that the driver can be shut down without removing power to any devices powered by the LDO voltage regulator.

Internal shutdown functions provide overcurrent, short circuit, undervoltage, overvoltage, and overtemperature protection. In addition, the device also has built-in current sensing for accurate current measurement.

Features:

- H-bridge motor driver
  - Drives a DC motor, one winding of a stepper motor, or other loads
  - Low MOSFET ON-resistance: 65 mΩ HS + LS at 4.2 V, 25°C
- 5-A continuous 8-A peak-drive current
- Internal Current sensing with current sense output
- 2-V to 5.5-V operating supply voltage range
- Overvoltage lockout (OVLO) and undervoltage lockout (UVLO)
- Low-power sleep mode
- 100-mA isolated LDO voltage regulator
- 24-pin VQFN package

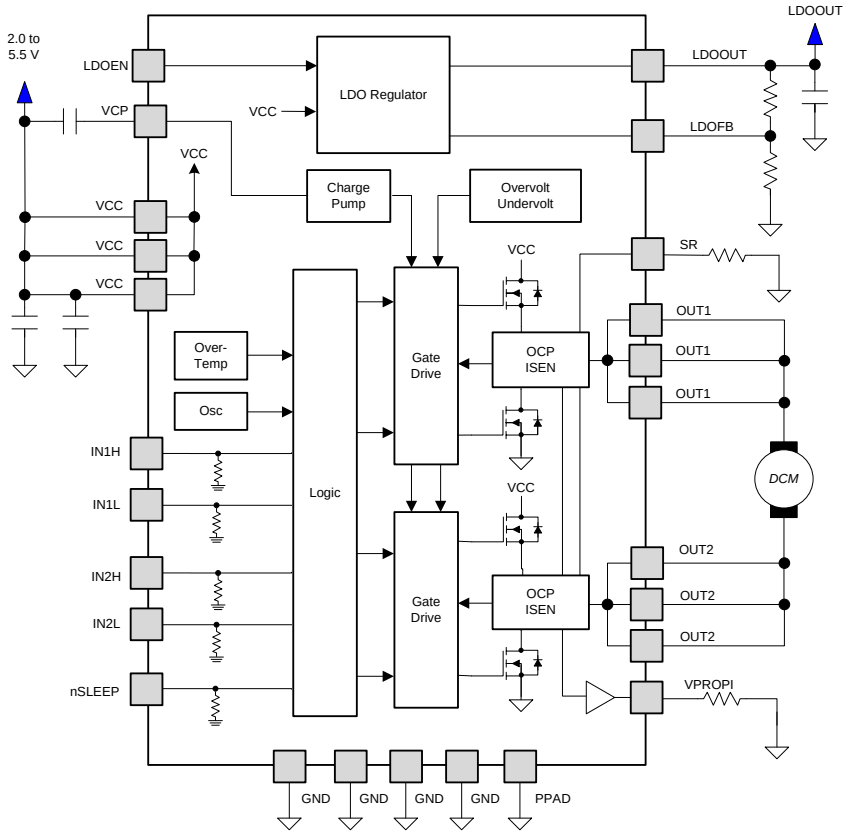


Figure 2. DRV8850 Functional Block Diagram

1.4.2 MSP430G2533

The TI MSP430 family of ultra-low-power MCUs consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful, 16-bit RISC central processing unit (CPU), 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally-controlled oscillator (DCO) allows wakeup from low-power modes to active mode in less than 1 µs.

The MSP430G2x13 and MSP430G2x53 series are ultra-low-power mixed-signal MCUs with built-in 16-bit timers, up to 24 input and output (I/O) capacitive-touch enabled pins, a versatile analog comparator, and built-in communication capability using the universal serial communication interface (USCI). In addition, the MSP430G2x53 family members have a 10-bit analog-to-digital converter (ADC). Figure 3 shows the MSP430G2x53 functional block diagram.

Features:

- Low supply-voltage range: 1.8 V to 3.6 V
- Ultra-low power consumption
  - Active mode: 230 µA at 1 MHz, 2.2 V
  - Standby mode: 0.5 µA
  - Off mode (RAM retention): 0.1 µA
- Five power-saving modes
- Ultra-fast wakeup from standby mode in less than 1 µs
- 16-bit RISC architecture, 62.5-ns instruction cycle time

- Basic clock module configurations
  - Internal frequencies up to 16 MHz with four calibrated frequency
  - Internal very-low-power low-frequency (LF) oscillator
  - 32-kHz crystal
  - External digital clock source
- Two 16-bit Timer_A with three capture and compare registers
- Up to 24 capacitive-touch enabled I/O pins
- Universal serial communication interface (USCI)
  - Enhanced universal asynchronous receiver and transmitter (UART) supporting auto baudrate detection (LIN)
  - IrDA encoder and decoder
  - Synchronous SPI
  - I^2C
- On-chip comparator for analog signal compare function or slope analog-to-digital conversion
- 10-bit, 200-ksps ADC with internal reference, sample-and-hold, and autoscan
- Brownout detector
- Serial onboard programming, no external programming voltage required, programmable code protection by security fuse
- On-chip emulation logic with spy-bi-wire interface

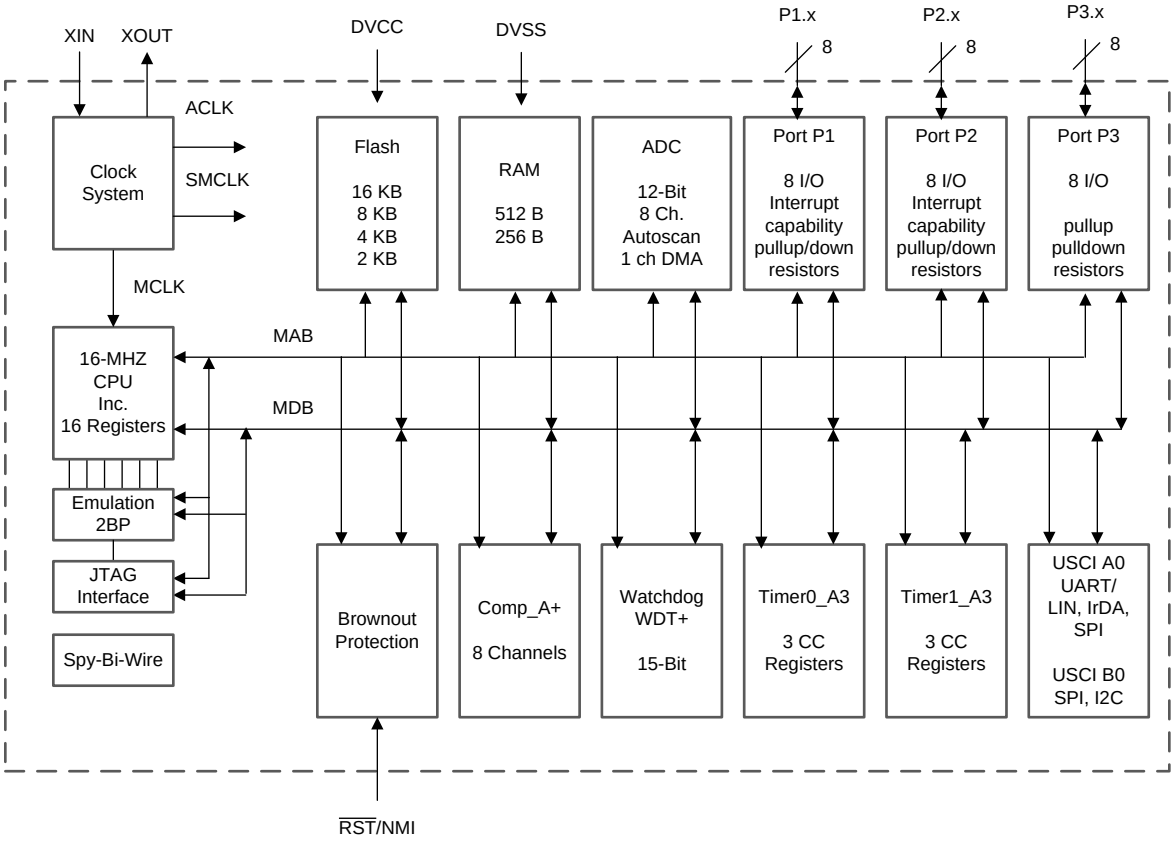


Figure 3. MSP430G2x53 Functional Block Diagram

1.4.3 SN74LVC2G14 Dual Schmitt-Trigger Inverter

This dual Schmitt-trigger inverter is designed for 1.65-V to 5.5-V VCC operation.

NanoFree™ package technology is a major breakthrough in integrated circuit (IC) packaging concepts, using the die as the package.

The SN74LVC2G14 device contains two inverters and performs the Boolean function Y = A. The device functions as two independent inverters, but because of Schmitt action, the device can have different input threshold levels for positive-going (VT+) and negative-going (VT–) signals.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it has been powered down.

Features:

- Available in the TI NanoFree package
- Supports 5-V VCC operation
- Inputs accept voltages to 5.5 V
- Max tpd of 5.4 ns at 3.3 V
- Low-power consumption, 10-μA maximum ICC
- ±24-mA output drive at 3.3 V
- Typical VOLP (output ground bounce) <0.8 V at VCC = 3.3 V, T_A = 25°C
- Typical VOHV (Output VOH Undershoot) >2 V at VCC = 3.3 V, T_A = 25°C
- Ioff supports live insertion, partial-power-down mode, and back-drive protection
- Support translation down (5 V to 3.3 V; 3.3 V to 1.8 V)
- Latch-up performance exceeds 100 mA per JESD 78, Class II

2 System Design Theory

The board created for this TI Design has two halves, as Figure 4 shows. The top part of the design is the discrete design, which includes 15 components.

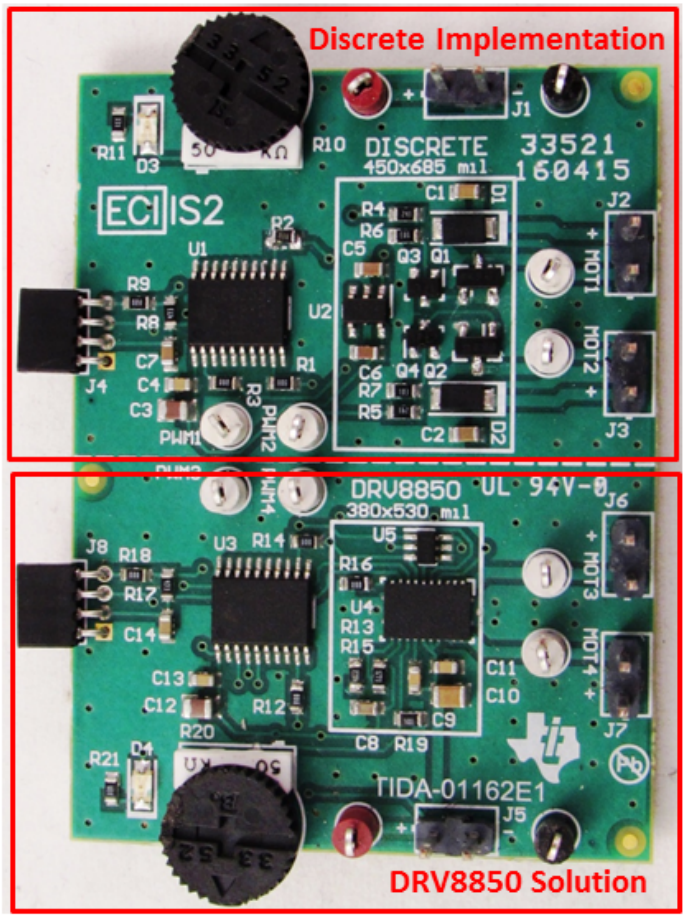


Figure 4. Board Layout

In the discrete implementation, one side of the motor is connected to the power source VBAT; the other side is connected to the drain of the MOSFETs, as Figure 5 shows.

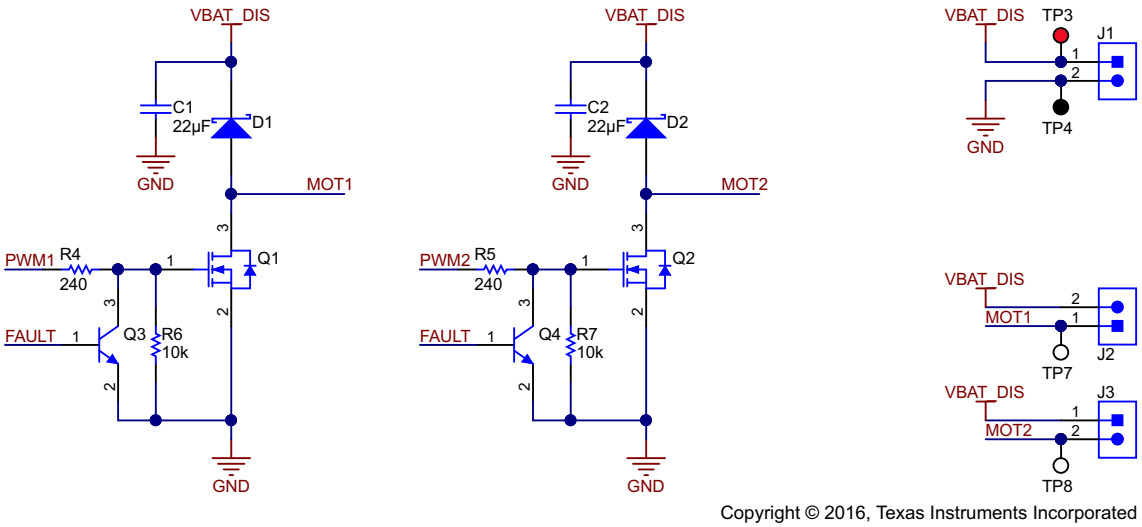


Figure 5. Discrete Implementation Motor Connection

The speed of the motor is controlled by the PWM1 and PWM2 signals connected to the gates of the MOSFETs. A typical bipolar junction transistor (BJT) is placed from the gate to the ground to prevent damaging the MOSFETs. Additional software implementation is required; for example, when a fault exists, the MCU can send a high signal and active the BJT. The flyback diodes are placed for protection as well.

In the second implementation, the DRV8850 drives the motor through the internal MOSFETs as Figure 6 shows. The MSP430G2253 device provides the input signals to the IN1H/IN1L and IN2H/IN2L pins. These pins enable the high side and low side of the MOSFETs when enabled. With one side of the motor connected directed to the battery, the low-side MOSFET opens and closes according to the PWM signal. The speed of the motor can be adjusted through a potentiometer which is connected to the MCU. The output of the dual-inverter device serves as an input for enabling and disabling the high side and low side of the MOSFETs.

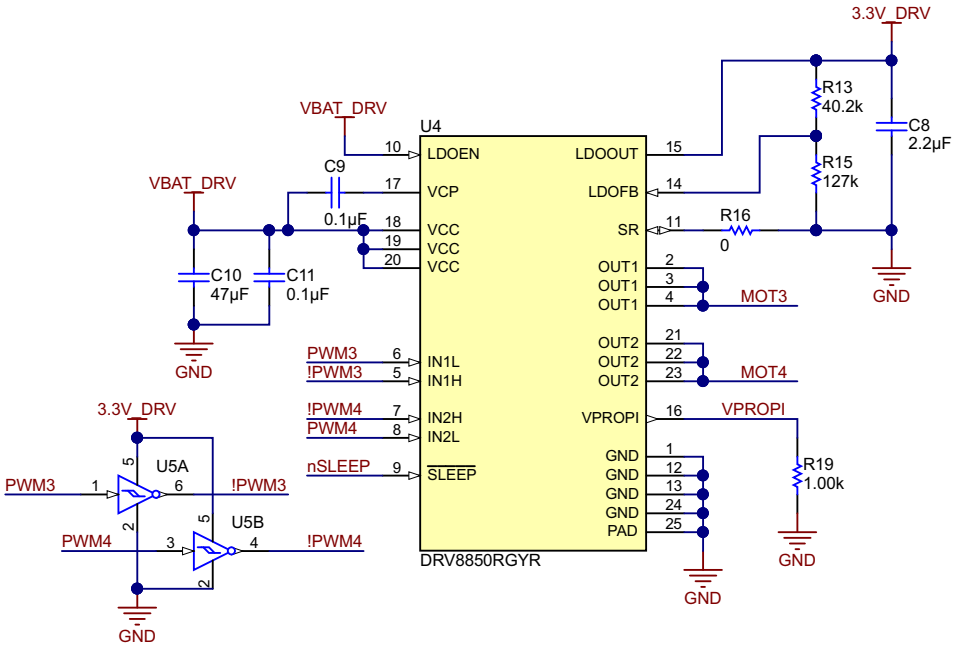


Figure 6. DRV8850 Implementation

3 Getting Started Hardware and Software

3.1 Hardware

The board in Figure 7 shows the inputs and outputs of this design. The board can be powered with a battery range of 2 V to 5.5 V JP1 is the input power for the discrete implementation, whereas JP5 is the input power for the DRV8850 side (see Figure 7). Note that each side requires its own voltage supply which, although not practical on a design, has been implemented for comparing purpose. This configuration is the case for the entire design. Each half operates independently of the other.

The unidirectional motor connections are JP2 and JP3 for the discrete half and JP6 and JP7 for the DRV8850 board. One pin of these headers is connected directly to the supply voltage and the other to the drain of the low-side MOSFET.

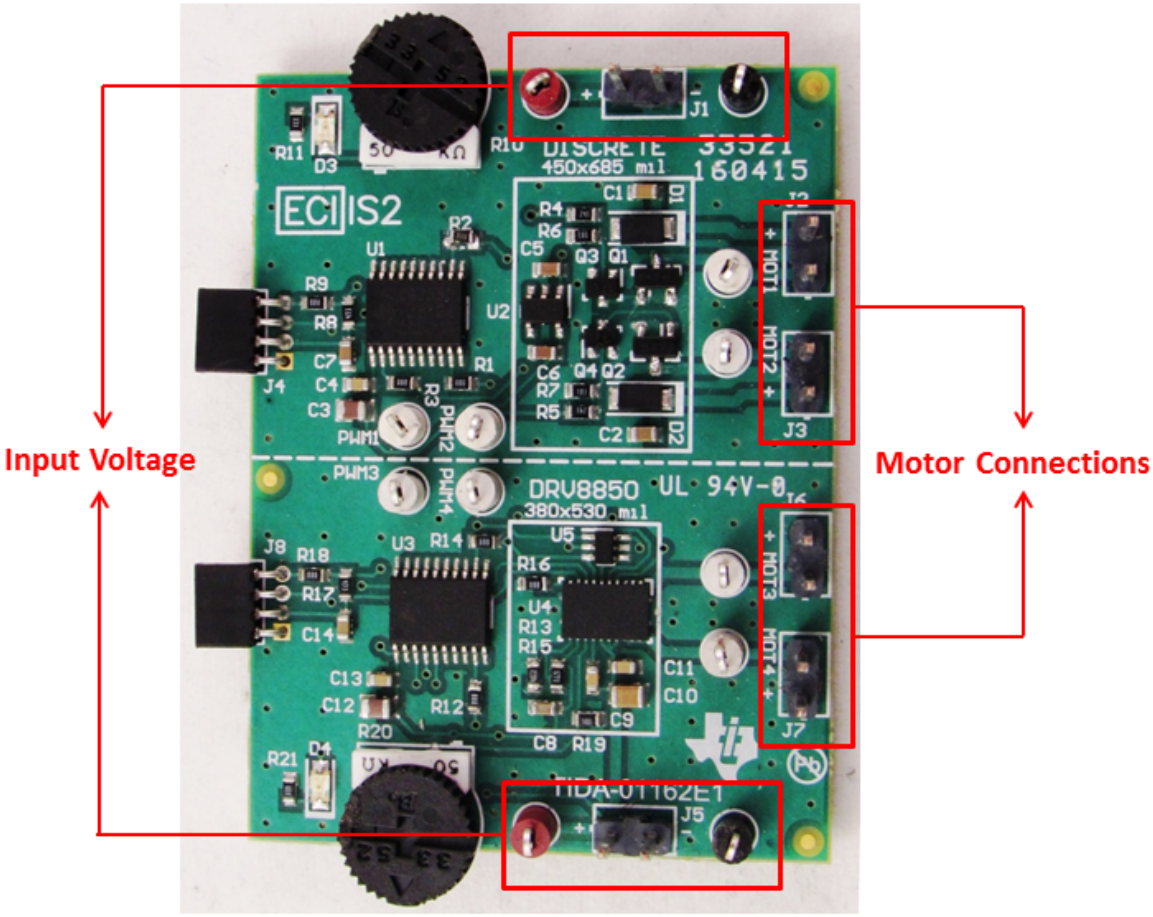


Figure 7. Input and Output Connections

3.2 Power On—Status LED and Speed Control

When the power source is connected correctly the DRV8850 is ON and the MSP430G2553 is also ON and generating the PWM signals and the green light-emitting diode (LED) starts toggling ON and OFF. To increase or decrease the speed of the motor, the potentiometer requires adjustment. The potentiometer is connected to a general-purpose input/output (GPIO) of the MSP430G2553 device, which is set as an input pin, and the potentiometer adjusts the duty cycle of the PWM signals. The MCU can be programmed through spy-bi-wire protocol. Figure 8 shows an image of the board highlighting the speed control, LED status, and spy-bi-wire connectors.

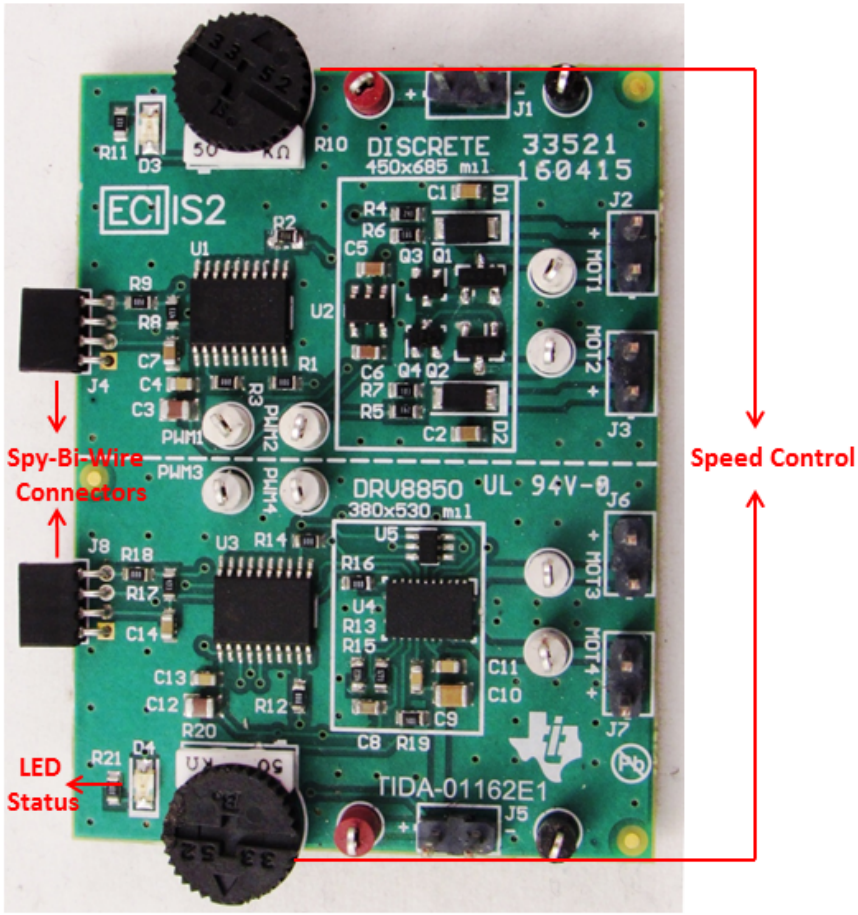


Figure 8. Speed Control and Status

3.3 Software

The firmware for this TI Design has been developed using TI Code Composer Studio™ (CCS) version 6.1.3. The code uploaded to the MSP430G2553 has been programmed through spy-bi-wire protocol (two-wire Joint Test Action Group (JTAG)). The code for both designs are essentially the same with the difference being that the DRV8850 design requires the nSLEEP pin to be enabled from the MCU to operate.

3.3.1 Code Description

This high-level description is implemented to drive both solutions. The code can be downloaded from the TIDA-01162 Design Folder.

1. The first step is to define the pins used in the MCU and then initialize global variables and function calls.
2. Next, enable the watchdog timer. This timer is set to about 30 ms and the clock (DCO) is set to run at 1 MHz.
3. Then configure all outputs from the MCU.
4. The last step is to configure the ADC to take the analog value from the potentiometer, which sets the duty cycle of the PWMs.

4 Testing and Results

This TI Design was tested under two conditions, no load and load, using a small propeller for load.

For the load case, the output voltage of the one of the motors was captured with a channel of the oscilloscope. Additionally, the current consumed for one motor was measured as well as the total current consumed for each system, discrete and DRV8850 implementation.

The board was also tested with two different input voltages 3.3 V and 5 V. Under these two voltages, the duty cycles were modified to acknowledge the current increase as the speed changes from 50% to about 95%.

4.1 Test Data

4.1.1 Propeller Load Start-Up Current

As Figure 9 and Figure 10 show, the start-up current for both designs are around 2.6 A at a 5-V supply and maximum duty cycle.

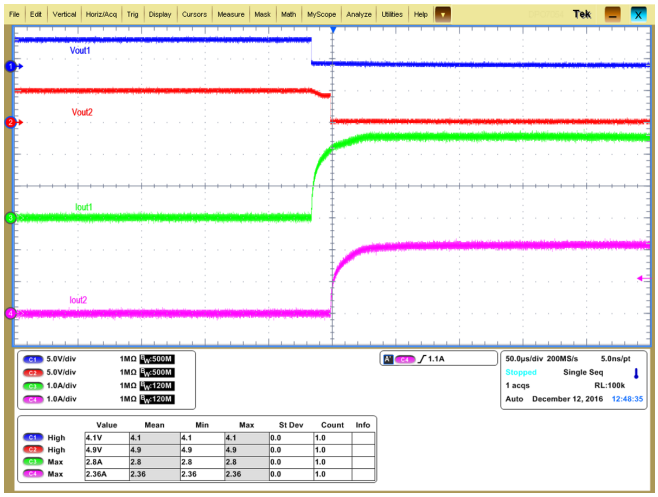


Figure 9. 5-V Discrete Board

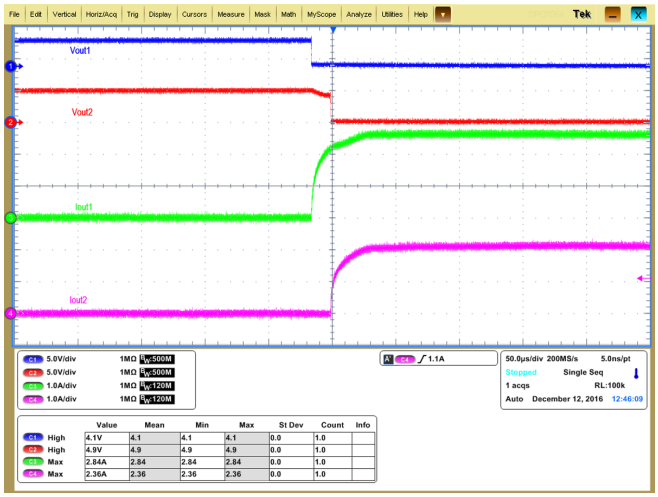


Figure 10. 5-V DRV8850 Board

4.1.2 Propeller Load

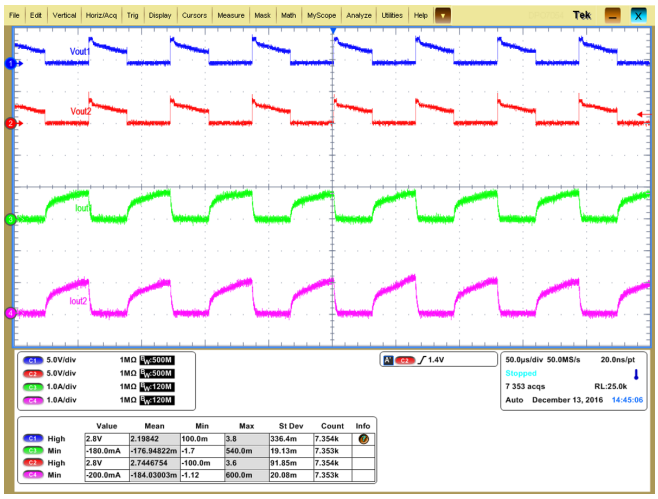


Figure 11. 3.3-V Discrete Board—50% Duty Cycle

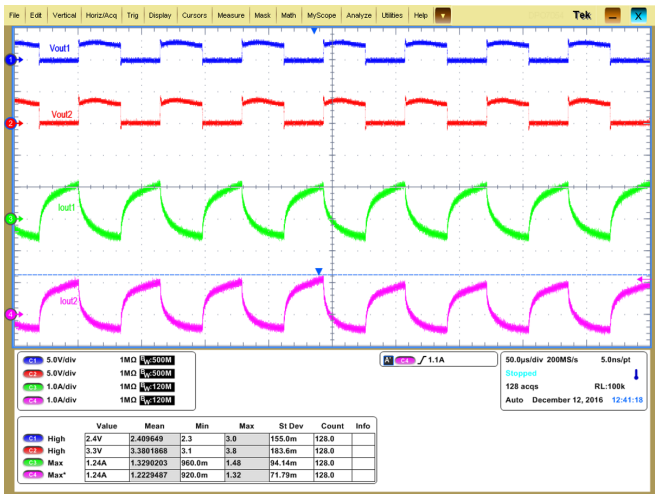


Figure 12. 3.3-V DRV8850 Board—50% Duty Cycle

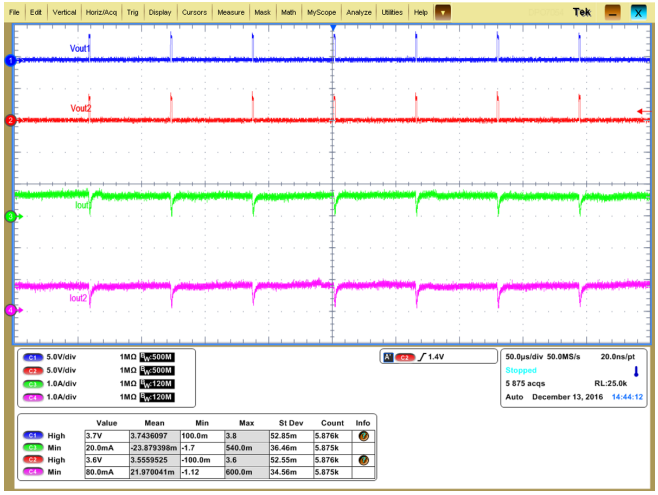


Figure 13. 3.3-V Discrete Board—95% Duty Cycle

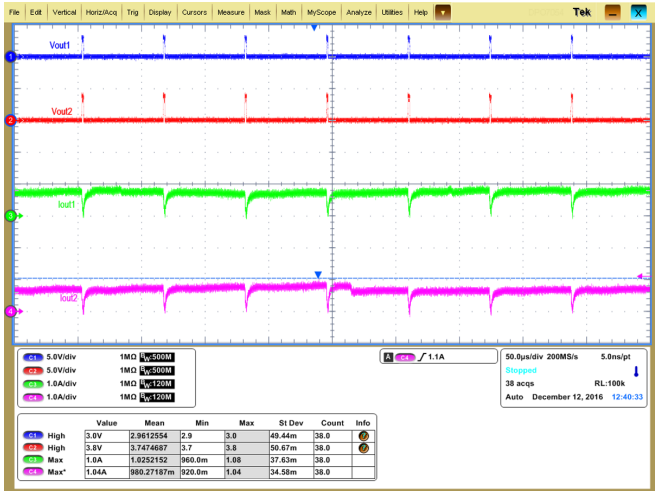


Figure 14. 3.3-V DRV8850 Board—95% Duty Cycle

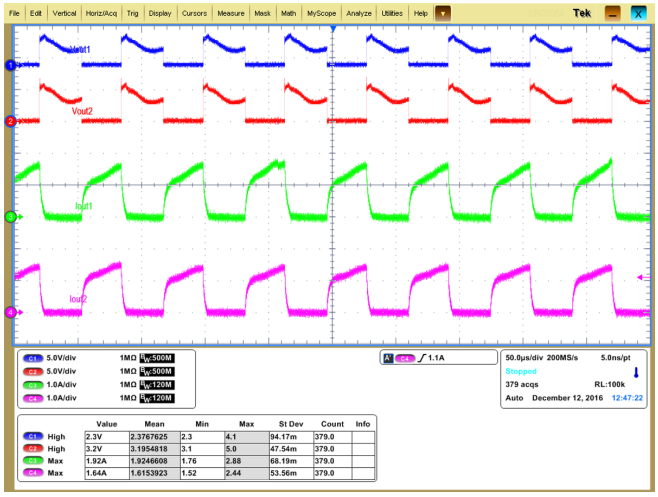


Figure 15. 5-V Discrete Board—50% Duty Cycle

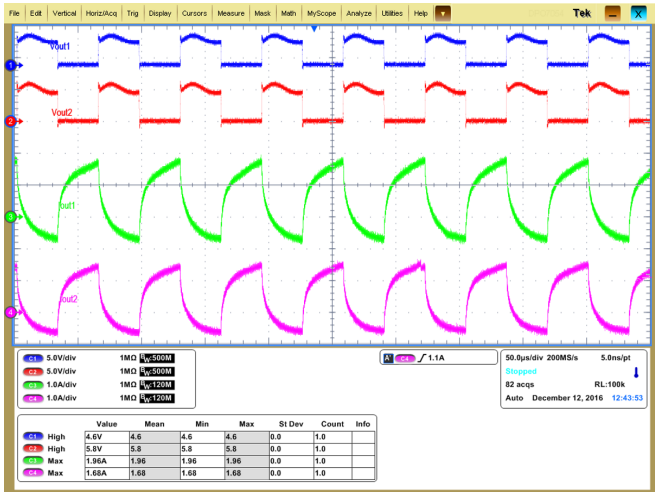


Figure 16. 5-V DRV8850 Board—50% Duty Cycle

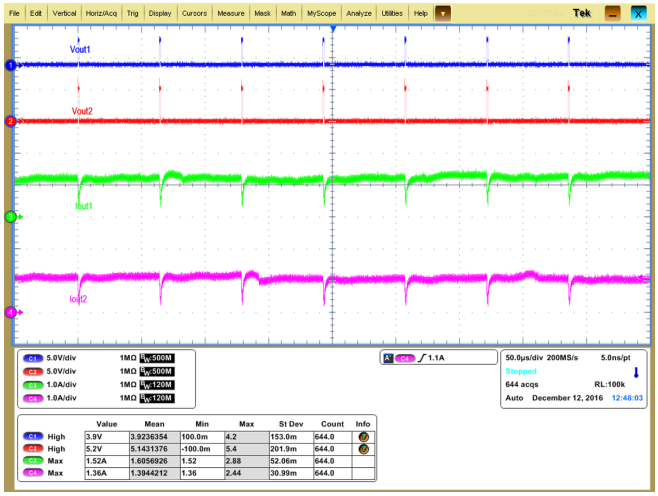


Figure 17. 5-V Discrete Board—95% Duty Cycle

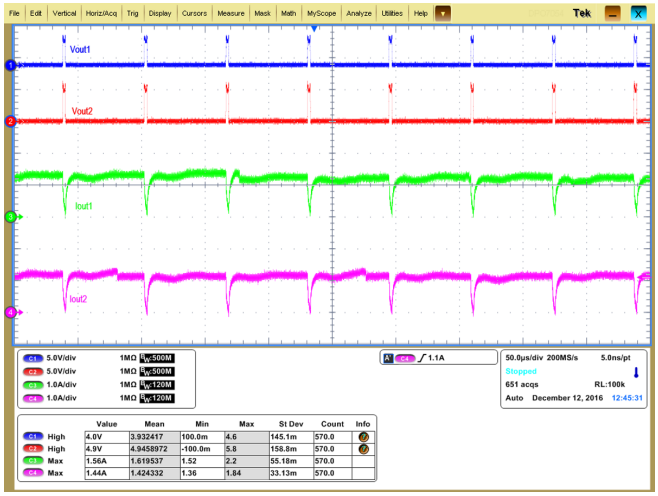


Figure 18. 5-V DRV8850 Board—95% Duty Cycle

As observed from the compiled test data, the results obtained from both designs (discrete and DRV8850 implemented) behave similarly under the same test conditions; therefore, the DRV8850 device serves as a worthy replacement for the discrete solution.

4.2 Thermal Images

Thermal images were captured at ambient temperature running the DC motors with the propeller as a load. The points on the captures show the low and max temperatures in °F.

The following thermal shots show the thermal difference between the two designs under the same conditions, which is 5 V at 95% of the duty cycle. Figure 19 shows that the thermal stress of the MOSFETs for the discrete solution is considerably noticeable. For the DRV8850 board, the heat is dissipated uniformly in the upper corner section 15º less from the discrete solution that Figure 20 shows.

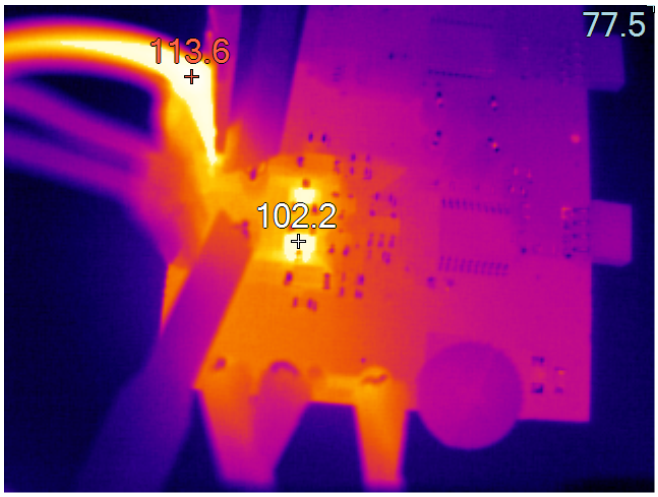


Figure 19. 5-V Discrete Board at 95% Duty Cycle

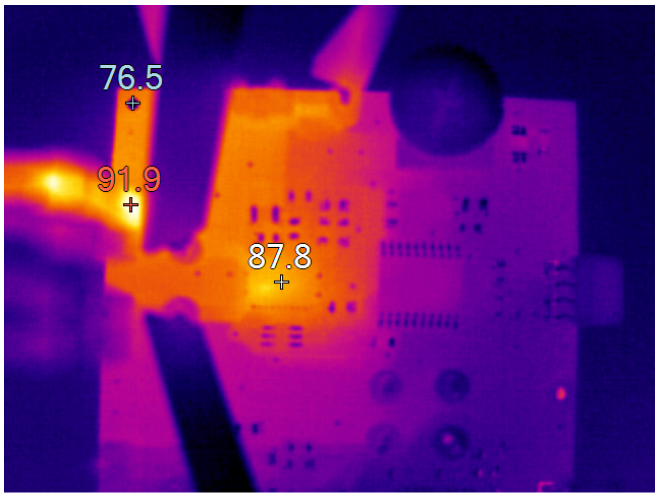


Figure 20. 5-V DRV8850 Board at 95% Duty Cycle

4.3 Physical Differences

Table 2 shows the main physical differences between the two options. It also shows the costs of components using a single-unit build. Note that it is worthwhile to have a lesser component count to provide an advantage to designers when reducing board size, which also translates in fabrication and assembly savings.

Table 2. Physical Differences

PARAMETER	COMPONENT COUNT	PCB FOOTPRINT AREA	COMPONENT COST
Discrete solution	15	198.89 mm^2	$1.56
DRV8850 implementation	10	129.89 mm^2	$1.42

4.4 Performance

4.4.1 Current Sensing

The DRV8850 features the VPROPI pin, which is an output proportional to the current flowing in high–side field-effect transistors (FETs) of the H-bridge. This feature is not used in this design because only the low-side FETs have been used to validate the same functionality as the discrete solution. Designers can definitely drive their design using the high-side MOSFETs of the H-bridge and take advantage of this useful feature. For information on how to use the current sensing feature, refer to the *Detailed Description* section of the DRV8850 datasheet [1].

4.4.2 Slew-Rate Control, Time Delay, and Dead Time

The rise and fall times of the outputs can be adjusted by setting the value of a single external resistor connected from the SR pin to ground, where the value of a resistor can range from 0 Ω (pin connected directly to ground) to 2.4 MΩ, setting the rise and fall time from 70 ns to 70 μs, respectively.

The dead time can be also modified by the values of the resistors. These values change the dead time between turning off one of the H-bridge FETs and turning on the other. The dead time can be adjusted anywhere from 400 ns to 110 μs.

Additionally, a propagation time delay is also set by placing a resistor at the SR pin. This time serves as an input deglitcher. The input deglitcher prevents noise on the input pins form affecting the output state. Figure 21 shows an example of a low-side slow decay showing the relationship of slew rate, time delay, and dead time.

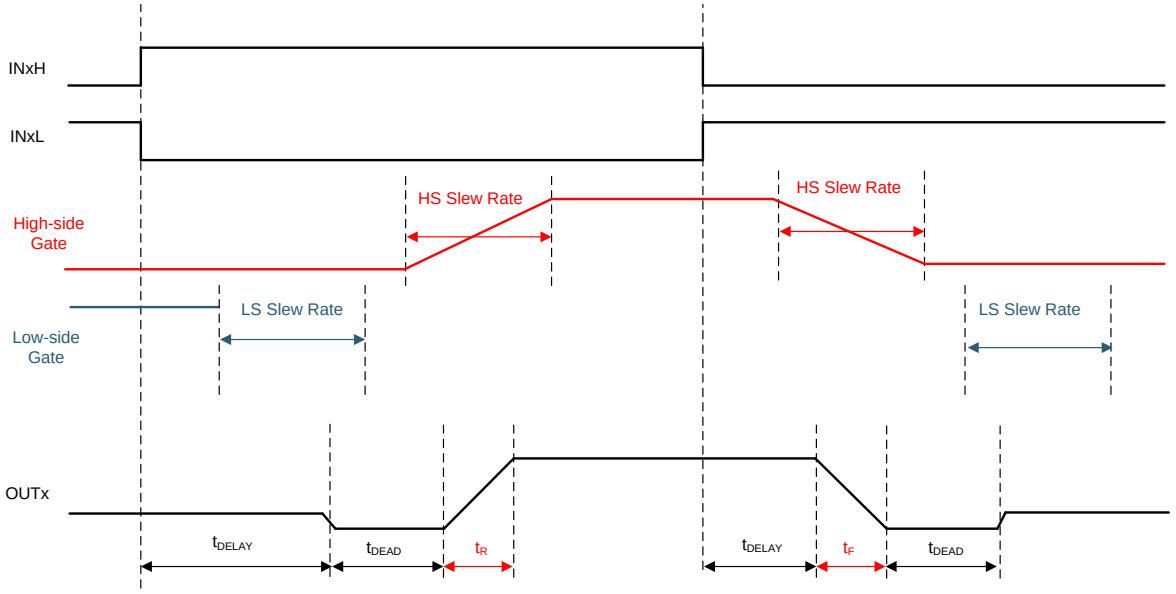


Figure 21. Example Graph—Low-Side Slow Decay

4.4.3 Thermal Shutdown

Another feature of the DRV8850 device is the thermal shutdown feature. If the die temperature exceeds the thermal shutdown temperature (t_{TSD}) of about 160ºC, then all the FETs in the H-bridge are disabled. These MOSFETs are automatically enabled when the temperature of the die has fallen below the thermal shutdown temperature minus the hysteresis temperature (approximately 110ºC).

4.4.4 Protection

The DRV8850 device is protected against overcurrent, undervoltage, overvoltage, and overtemperature events.

4.4.4.1 Overcurrent Protection

For the overcurrent protection, an analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than 1 μs (t_{OCP}), all MOSFETs in the H-bridge are disabled. After approximately 4 ms (t_{RETRY}), the bridge attempts to reenable automatically.

4.4.4.2 Undervoltage Protection

For undervoltage, if at any time the voltage on the VCC pins falls to less than 1.95 V (the UVLO threshold voltage), all circuitry in the device is disabled and internal logic resets. Operation resumes when V_{CC} rises to greater than the UVLO threshold. Under this condition, the device allows for a proper shutdown of devices powered by the internal 3.3-V LDO output of the DRV8850 device.

If at any time the voltage on the VCC pin resets to more than 5.6 V (the OVLO threshold), the output MOSFETs are disabled. The operation resumes when V_{CC} falls below the V_{OVLO}.

Another nice feature of the DRV8850 is the SLEEP mode. The device can be in SLEEP mode and the internal LDO regulator can still supply power to another device, such as an MCU, which saves power consumption when the DRV8850 is inactive.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01162.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01162.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01162.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01162.

5.5 Layout Guidelines

Figure 22 shows a few layout guidelines for this design. The complete layout can be downloaded from the design files at TIDA-01162.

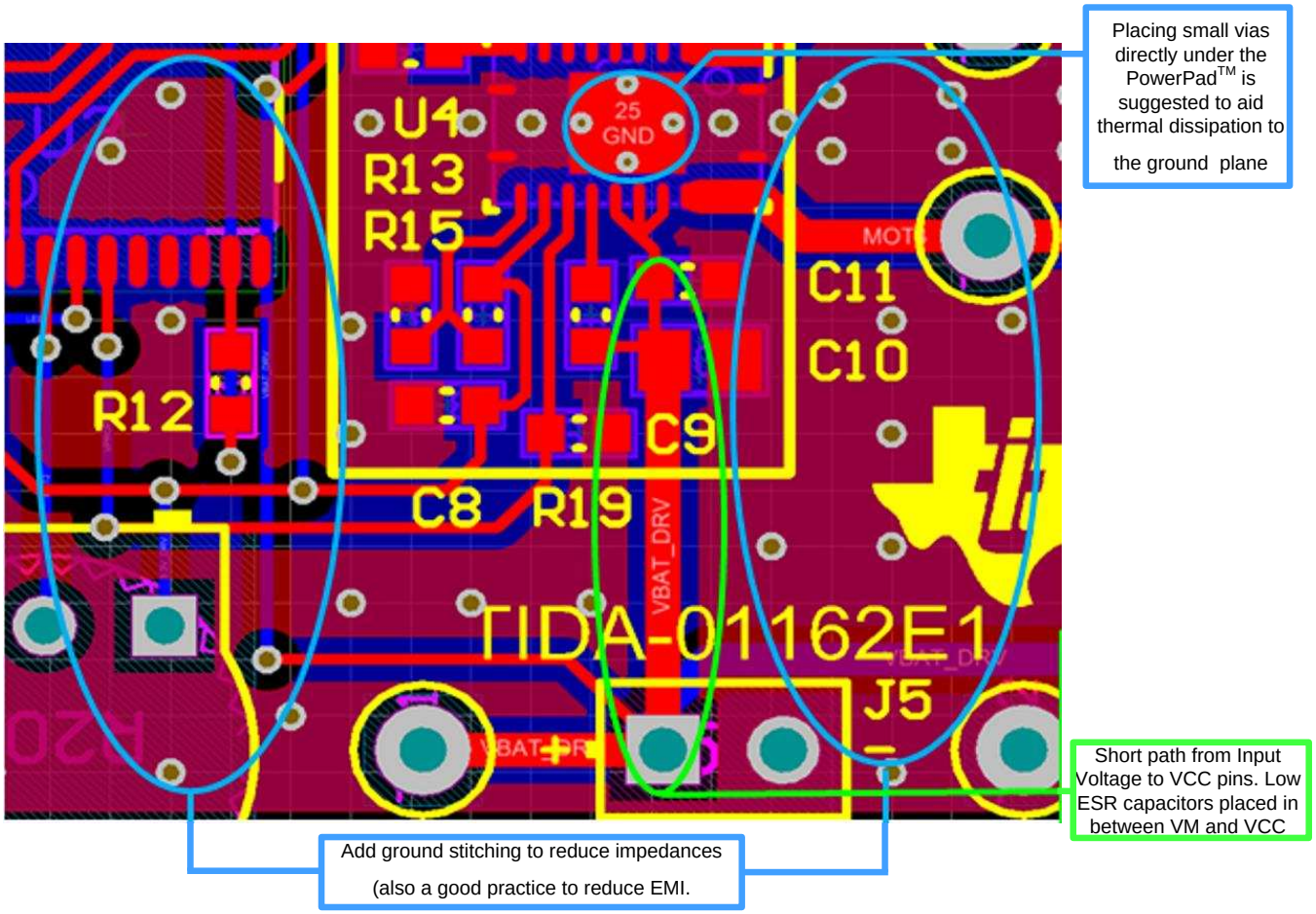


Figure 22. Layout Recommendations

5.6 Gerber Files

To download the Gerber files, see the design files at TIDA-01162.

5.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01162.

6 Software Files

To download the software files, see the design files at TIDA-01162.

7 Related Documentation

1. Texas Instruments, *DRV8850 Low-Voltage H-Bridge IC With LDO Voltage Regulator*, DRV8850 Datasheet (SLVSCC0)
2. Texas Instruments, *E2E Motor Drivers Forum*, TI E2E Community Forum

7.1 Trademarks

8 About the Author

NICHOLAS OBORNY is an Applications Engineer for Texas Instrument's motor drive business, where he is responsible for supporting TI's motor drive portfolio, developing evaluation tools, product demonstrations, motor drive training, and motor drive IC development. Nicholas has several years of experience with hardswitching power stages and brushless motor control system development. Nicholas graduated from Texas A&M University College Station with a Bachelor's of Science in Computer Engineering.

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