

## TI Designs

# bq7718: Stacked bq7718 Secondary Protection Reference Design for 60-V/15-S Industrial Battery Packs



### Description

This TI Design introduces the user to implementation of the existing TI bq7718, 3- to 5-S secondary protector in a stacked configuration for industrial packs up to 15-S system. This 60-V design details implementation using three of the bq7718XX without compromising high-accuracy over-voltage detection in 3- to 30-A load current environments mandating small form factor such as 2-cm x 2-cm of printed circuit board (PCB). This design also incorporates the latest technology, such as the Dexerial-SFK5030A, a surface mount, self-control protector and one-time current fuse. The advantage of a one-time fuse is that the circuit is permanently disabled and the pack will be inoperable until replaced. The reference design should allow the designer to easily and cost effectively add second level protection to the system.

### Resources

[TIDA-00108](#)

[Design Folder](#)



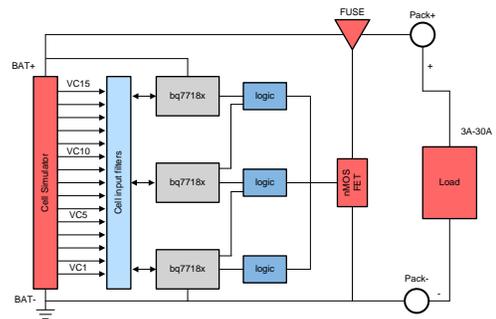
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### Features

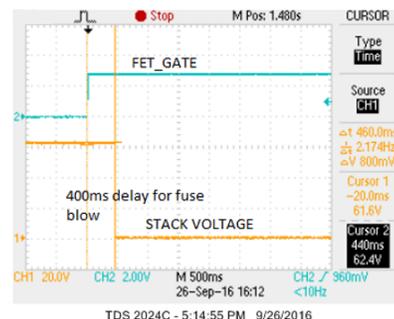
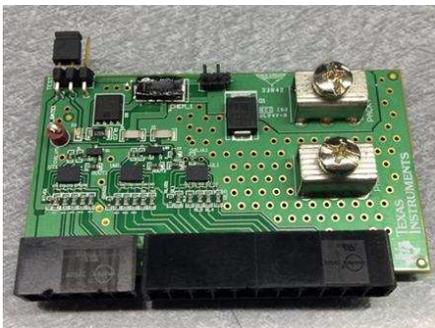
- Completely Independent of Existing Monitoring Analog Front-End (AFE) and Cell-Balancing Solutions
- Ability for Integration Into Pack With 5-, 10-, and 15-S Monitors and Protectors
- Electronically Control and Use Accurate Self Control Protector Inline Current Fuse
- Advantage of a One-Time Fuse Blow Where Circuit is Permanently Disabled, Pack is Isolated and Not Operable

### Applications

- Power Tools
- Storage Battery Protection
- Electronic Vehicle (EV) Bikes



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## 1 System Overview

### 1.1 System Description

In the secondary stack system reference design, there are three major functional blocks:

1. The cell input filters protection network as defined in the bq7718 device specification
2. The three bq771xx devices that are stacked and configured in a 3-S scheme with individual output signals forming a logic OR using an analog scheme. The serial configuration is allowed as the voltage translation from GND to 60 V.
3. Inline fuse blowing scheme is electronically commanded with a NMOS FET connected to the self-protector fuse.

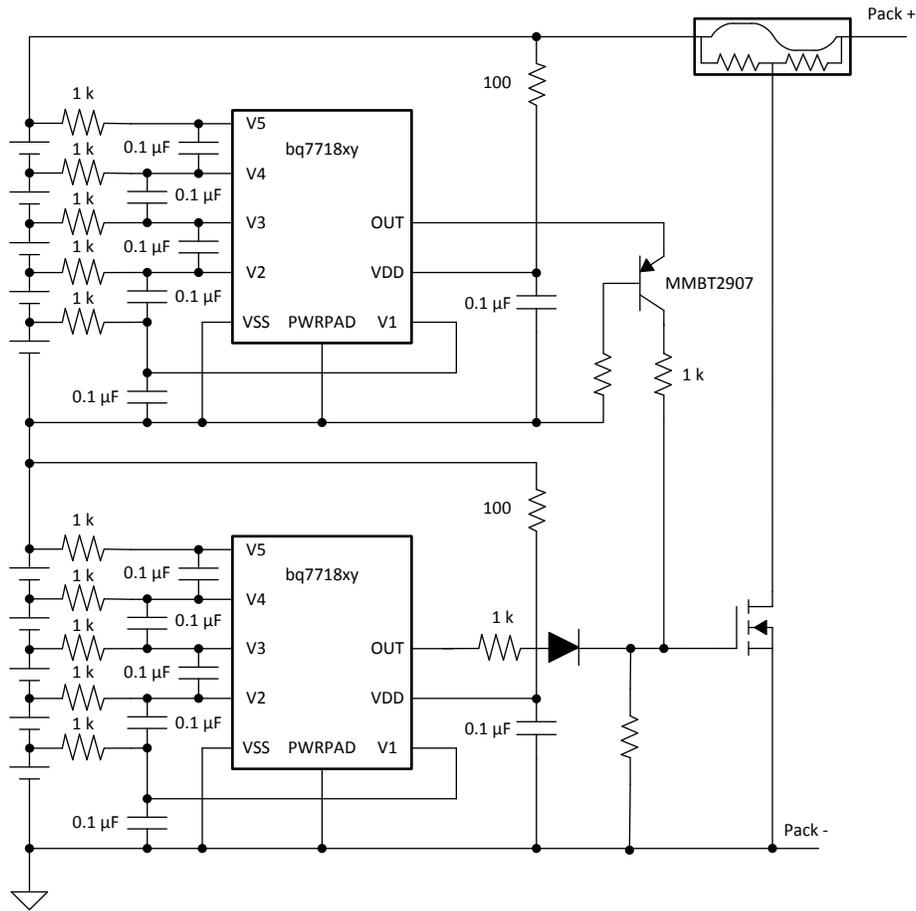
The cell banks are emulated in the lab by a cell bank simulator. The voltages of the cells are routed through a bank of low-pass filter network as per the device specification which also limit currents into the bq7718 in a differential fashion. In the bq7718 family, each cell is monitored independently with an embedded delay timer.

When the individual cell voltages of cell simulator is increased above the over-voltage protection (OVP) threshold of the device, the bq7718 Cout pin (active high output drive) is commanded from low to high.

The timer provides a constant time to prevent false trips of the of the OUT driver. When the OUT responds to an OVP event of any of the cells, the pin goes from low to high after about 4 s. Each of the OUT pins are logical ORed and will have the response when commanded to go high. The gate of the NMOS FET CDS is calculated to have 3 to 10 V. When the FET is ON, the FET commands to pull the fuse blow open through the heater resistance of the state-of-the-art, self control protector fuse.

The voltage sensing and active load unit is hooked across PACK+/PACK-. The unit is programmed to the desired loads from 3 to 30 A to test the PCB.

Figure 1 shows the conceptual 10-S stack protector systems circuit diagram.



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**Figure 1. Conceptual 10-S Stack Protector Systems Circuit Diagram**

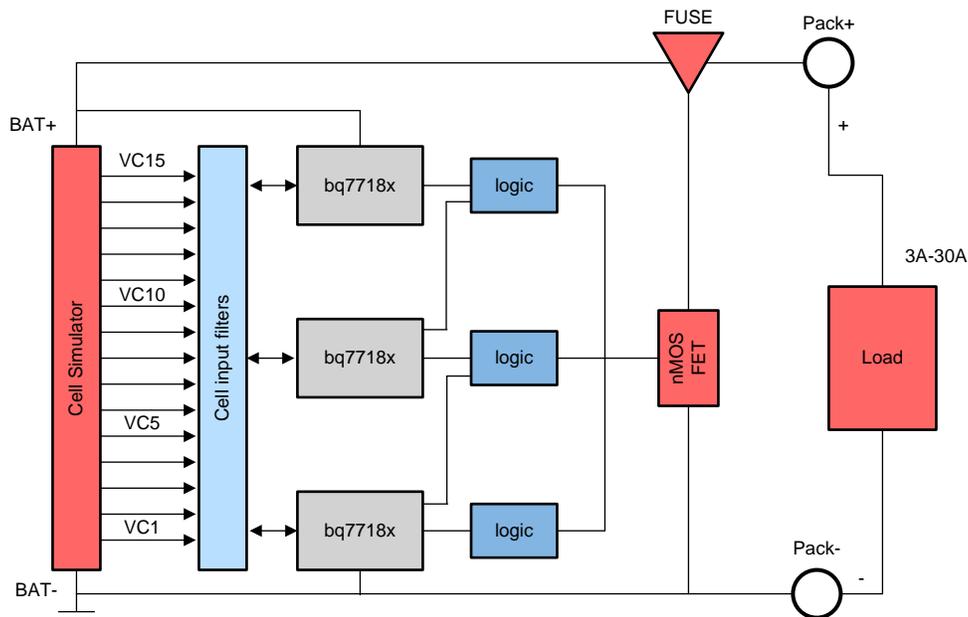
### 1.2 Key System Specifications

The key circuit parameters which is determined in the selection of the device specification is the normal operating current of the circuit under both charge and discharge; the maximum fault voltage and the secondary protection circuit response time to an over voltage condition. Based on the system requirement of cell over voltage threshold (OVP), output delay timer and the output drive, the secondary protection device bq7718xy can be selected for the design. The self-controlled protection fuse (SCP) must have a normal operating current above the charge and discharge current levels. During the charge cycle, the primary protection circuit in the battery pack is designed to allow charging until the maximum voltage is reached. The TVS diode at the input of the PACK+/PACK- leakage current characteristic is critical for the system design. The diode response time to transient and surges will depend on the type of loading across the PACK+/PACK- terminals.

**Table 1. Key System Specifications**

PARAMETER	SYSTEM PARAMETER	NOTES
Normal mode leakage	11.8 to 13.6 $\mu$ A	VC5/GND, VC10/VC5; VC15/VC10
Pin input current	< 0.12 $\mu$ A	All pins at 4 V
OVP threshold	4.300 V	Bq771800DP
Internal timer delay	4.0 s	No change in the stackable system
Voltage monitor filter resistance	1 K $\Omega$	No change in the stackable system
Voltage monitor filter capacitance	0.1 $\mu$ F	No change in the stackable system
Input transient diode protection	75 V	Protection at the PACK+ and PACK-
Vgs of FET	5 to 8 V	Set by the voltage divider at the gate of Q2
Dexerials SFK5030A self-controlled protection fuse	30 A or 62 V	Fuse resistance: 1 to 2.5 $\Omega$

### 1.3 Block Diagram



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**Figure 2. 15-S Stack Protector System Blocks**

## 1.4 Highlighted Products

### 1.4.1 bq7718xy

Each cell is monitored independently with an embedded delay timer provides to prevent false trips of the inline fuses. The bq7718xx family provides an over-voltage monitor and protector for Li-ion battery pack systems. The small QFN footprint of the bq7718xy and its wide range of OVP threshold and output drive (either high or low depending on the configuration) makes the bq7718xx a good stand-alone secondary protector that could be scalable from 5-, 10-, and up to 15-S.

### 1.4.2 n-MOS FET CDS 18534Q5A

A 60-V, N-channel NexFET with 17 nC and  $V_{gs}$  of about 2 V is robust for this design. The  $V_{gs}$  selection is based on the ability to turn on the FET gate at a relatively small logic voltage (about 2 V) and to avoid spurious false trips.

## 2 System Design Theory

Lithium-Ion and Lithium-Polymer battery technologies require secondary protection from improper charging and overheating. In the event that the primary monitoring and protection circuit has been damaged by ESD or thermal overstress, secondary protection will provide protection from both overcharge of cell and over-discharge of the battery before excessive temperatures can occur in the pack or external damage is caused.

When the individual cell voltages of cell simulator increases above the OVP threshold of the device, the OUT (active high output drive) pin goes from low to high. Because each of the devices OUT is implemented as a logic OR, an OVP event generated in any of the devices on the stacked configuration will be detected. Calculations must be made so there would be adequate drive voltage on the gate of the FET (Q2) to turn it on as commanded. The selected n-channel FET has a threshold of about 1.9 V.

### 2.1 System Calculation for Logic

During OVP conditions depending on the location of the cell (bottom, middle, top), typical cascaded gate voltages of the FET can be calculated. [Table 2](#) shows the different voltage measurements.

**Table 2. Gate Voltage of the NMOS FET Versus Stack Voltage**

15-S STACK VOLTAGE (V)	CELL VOLTAGE (V)	OVP	GATE VOLTAGE OF THE NMOS FET
20 V	1.333 V	Bottom device	$V_{gs} = 6.67V (15K/19.64K) = 5.1V$
20 V	1.333 V	Middle device	$V_{gs} = [13.35V - 1V] / [(10.2K + 15K)] * (15K) = 7.4V$
45 V	3.0 V	Top device	$V_{gs} = ([6.67 - 1V] / [21.5K + 15K]) * (15K) = 2.33V$

### 3 Getting Started Hardware

#### 3.1 Hardware

##### 3.1.1 Testing and Fuse Blow Emulation Fixture

For testing purposes only, the user can leverage fuse blow emulating function of the design without actually activating the self control protector (SCP) fuse blow by shorting the jumper (JL) and shorting the TEST header at pin one and two. In this specific setup instead of the actual fuse blow, the red LED will turn on when the OVP condition is met, and the fuse blow is bypassed. If the jumpers are not configured, the fuse will blow and break the high-current path through the load.

##### 3.1.2 TI's 24-Cell Simulator

TI's 24-cell simulator is programmed through the NI data-acquisition system to provide the needed cell voltages. The GUI enables the user to control any of the cell voltage to command an overvoltage condition. Initially, set all of the cell voltage to 4 V. If increasing the cell voltage from 4 V to beyond the OVP threshold of 4.300 V, the OUT pin would then be commanded to go from low to high (on this configuration).

##### 3.1.3 3- to 30-A Active Load

Depending on application demands, 3- to 30-A active load conditions at the PACK+/PACK- node is provided by the 6-KW PS PLW6K-800. The equipment can sense the voltage at the PACK+/PACK- bus and deliver the needed current.

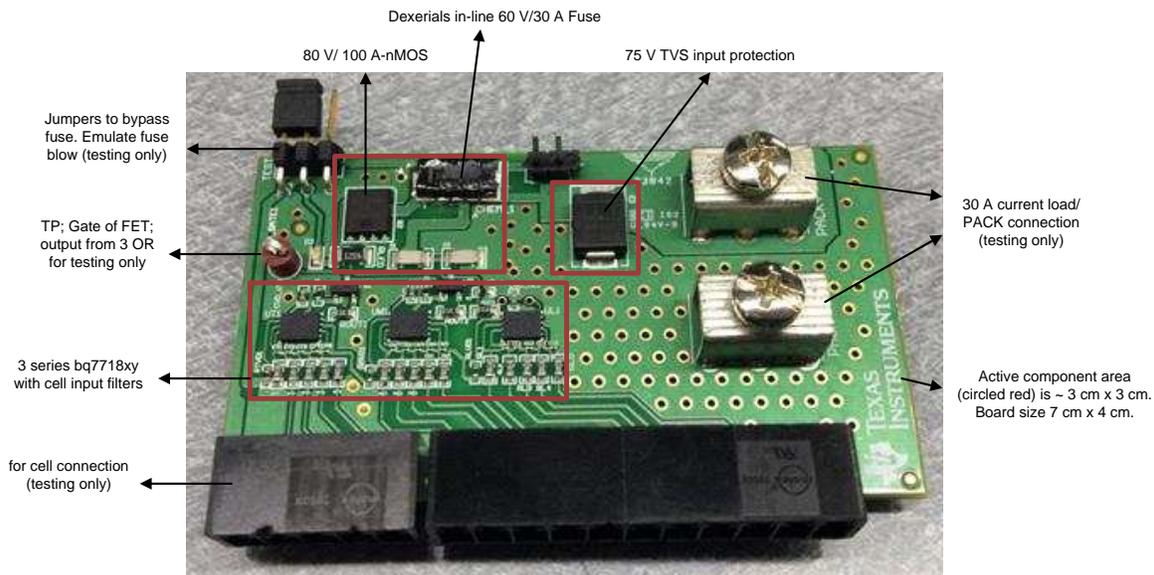
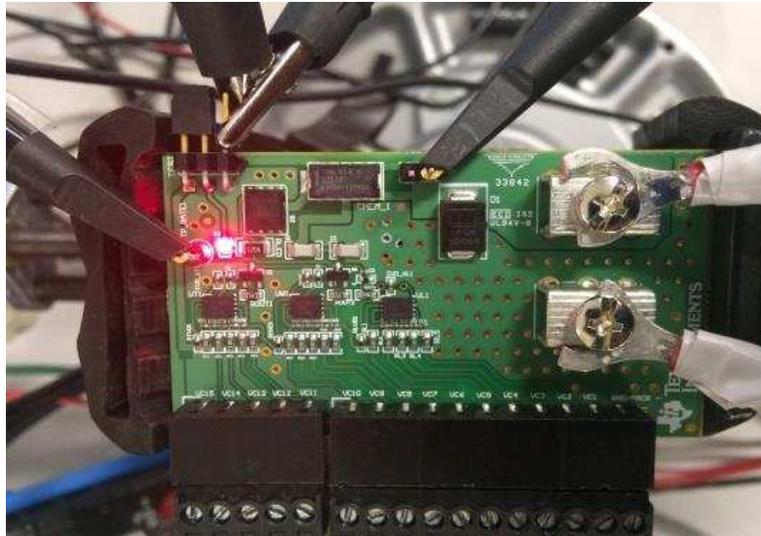


Figure 3. Active Components on 3-cm x 3-cm PCB With Connectors for Testing Setup

## 4 Testing and Results

### 4.1 Test Setup

Figure 4 shows the fuse bypass circuit emulating a fuse blow for testing purposes.

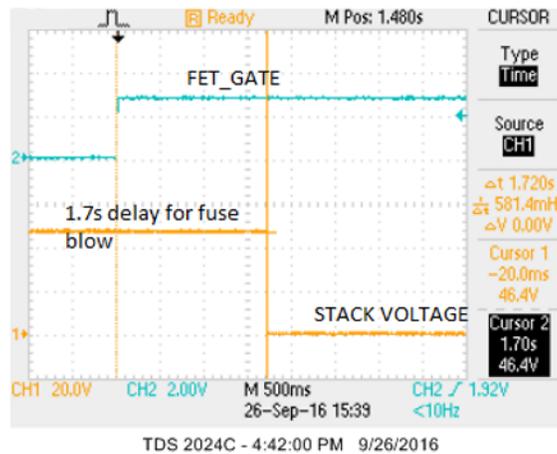


**Figure 4. Fuse Bypass Circuit LED ON for Testing Operation**

The fuse bypass circuit operation is recommended for testing without the fuse. In cases the fuse is installed may sure the inline JUMPER is shorted with a low-impedance wire. Also make certain the TEST HEADER pin 1 and 2 is shorted. The super LED current is scaled with inline resistance of about 4 K $\Omega$ . Therefore with a 45-V stack voltage, the current through the LED is about 10 mA when the CSD FET gate is commanded high, as shown in Figure 4.

## 4.2 Test Data

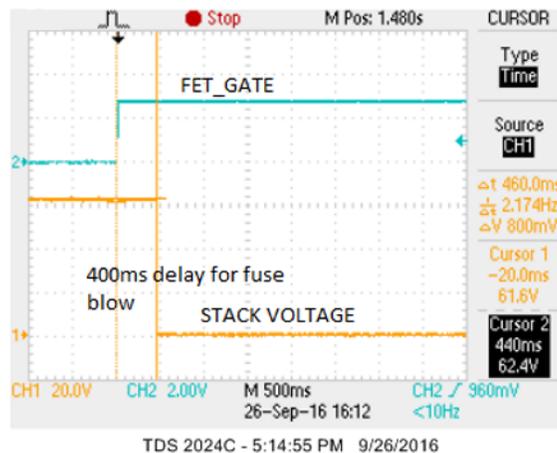
### 4.2.1 Dexerial SK5303A Fuse Blow Timing Characteristics



**Figure 5. 45-V STACK Voltage**

In the test setup with a 3-A load and a 45-V stack voltage, the time for the Dexerial fuse SK5303A to open is measured to be about 1.7 S, as seen in [Figure 5](#).

Timing is measured from the rising edge of NMOS FET gate (ORed) output of the bq7718 to the time it takes for the fuse to open.



**Figure 6. 60-V STACK Voltage**

In the test setup with a 3-A load and a 60-V stack voltage, the time for the Dexerial fuse SK5303A to open is measured to be about 400 ms.

Timing is measured from the rising edge of NMOS FET gate-Blue line (ORed) output of the bq7718 to the time it takes for the fuse to open, as depicted by the stack voltage monitored at the load (yellow line) in [Figure 6](#). When the fuse is commanded to open, the entire high current (load current of 3 to 30 A) path is an open circuit and, thus, isolates the battery. The collapsed stack voltage (after the fuse) is shown in yellow.

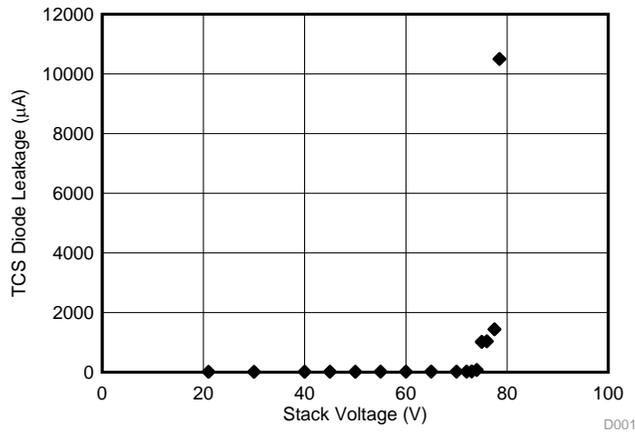


Table 3. TVS Diode Characteristics on 15 s

APPLYING VOLTAGE PACK+/PACK-	LEAKAGE CURRENT (µA)
21 V	14.5
30 V	15.5
40 V	16.7
45 V	17.8
50 V	18.7
55 V	19.29
60 V	20.44

The TVS diode at the input of the PACK+/PACK-current characteristic is critical for the system design. The diode response time to transient and surges should be characterized with the proper loading.

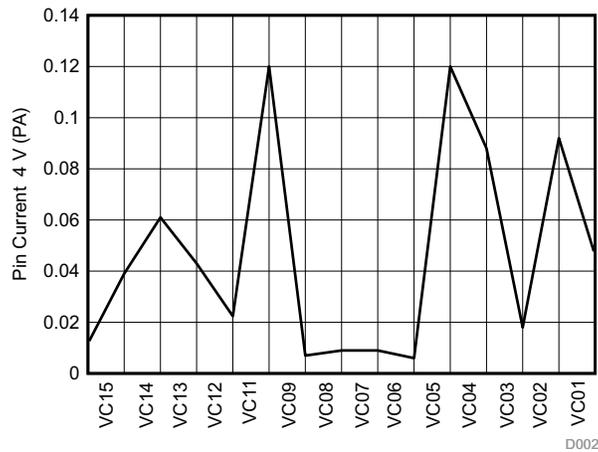


Figure 7. Pin Input Leakage Current at 4 V (µA)

The average current draw into the cell pin terminal before and after OVP events depicts a transitional current that can be characterized to be in sub-par as of the actual pin leakage currents. At the device-Vov threshold as the detection circuit is enabled, internal circuits switch several biasing circuits and the rise in the current to GND is detected. The device pin leakage for the stacked system, VC05 and VC10 demonstrate greater than 100 nA. This value is due to the extra components at the device boundary.

### 4.2.2 Temperature Gradient Across the PCB

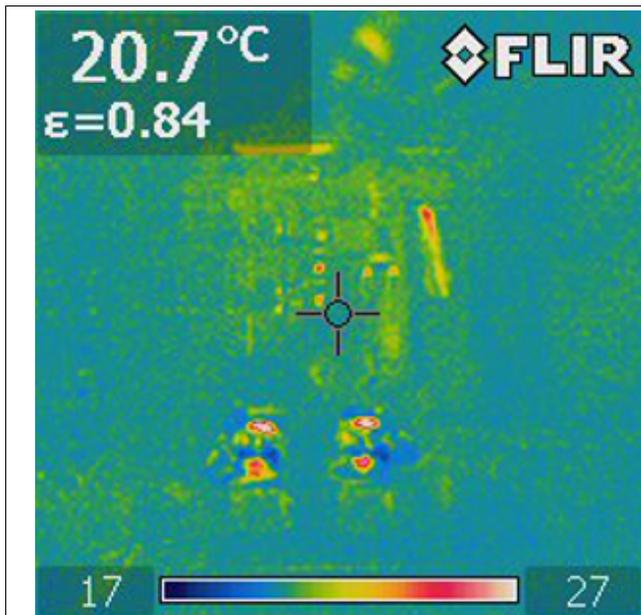


Figure 8. Temperature Gradients Before OVP Condition and Fuse Blow Activation

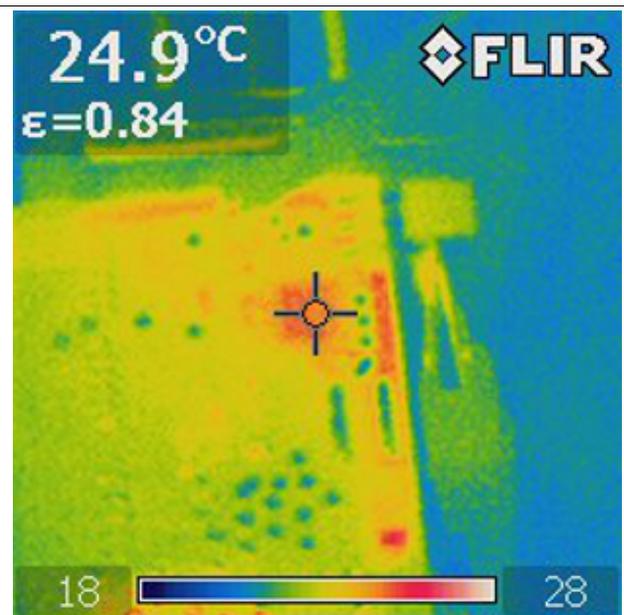


Figure 9. Temperature Gradients at OVP Condition and Fuse Blow

### 4.2.3 OVP Detection and Recovery Performance of Stacked Protector From 45 to 75 V

#### OVP Performance:

Figure 10 shows the effects of the cell voltage and OVP trip being set (device threshold 4.3 V with OV hysteresis of 300 mv).

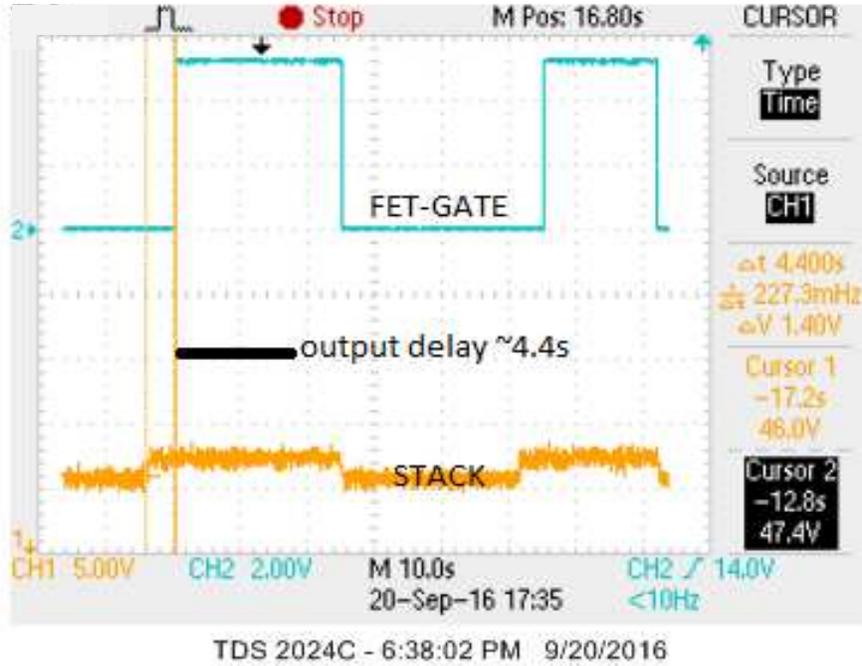
The stack also releases the OUT latch when the condition is not present.



Figure 10. Cumulative Stack Voltage Versus Gate Voltage Enabling Fuse

**Timer Delay:**

The time lag between the OVP event and the pull-down FET gate going active high is within the specification of the single device.



**Figure 11. Overall System Response Time to Cell OVP Event (Including Timer Delay)**

## 5 Design Files

### 5.1 Schematics

To download the schematics, see the design files at [TIDA-00108](#).

### 5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00108](#).

### 5.3 PCB Layout Recommendations

The 3-cm x 3-cm small form factor of the PCB demands the layout to take into consideration temperature rises and the high current paths.

1. This TI Design uses 2-oz Cu through the design and all of the high-currents paths. Route the high path around the BQ device.
2. Use of the solid ground planes on the top layer and bottom layer to avoid creation of small island on any of the GND planes.
3. Provide continuous ground planes using the polygons and ground copper areas on the top and bottom layers.
4. provide low inductance paths from the ground plane PACK-/BAT-. Avoid using thin ground traces to connect the components to the ground plane.
5. Use of the via stitches to reduce and minimize the impedance for the high return paths of the [unfinished sentence].

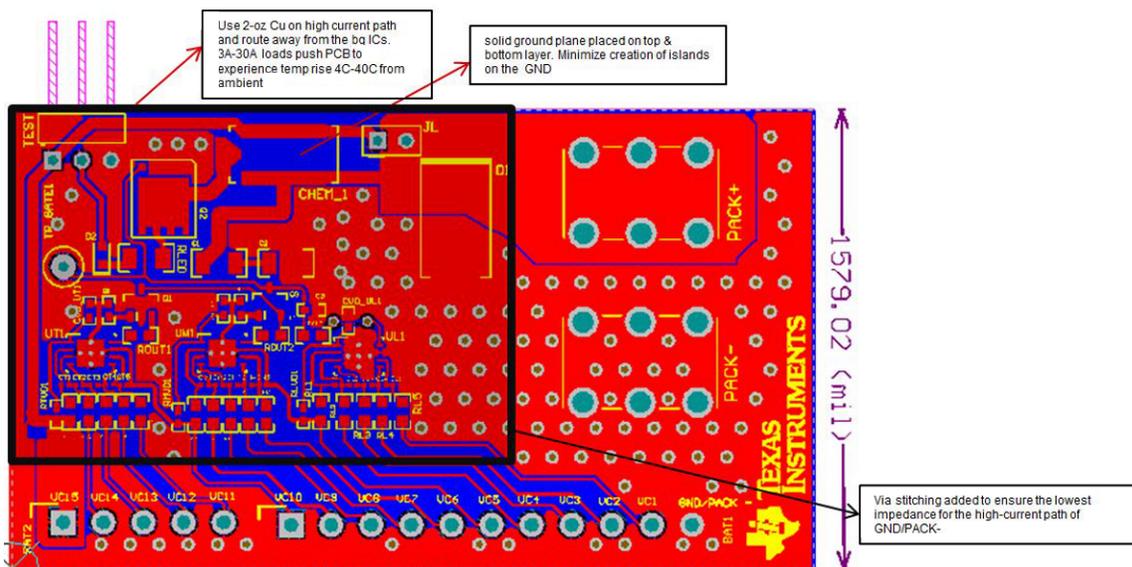


Figure 12. High current paths

#### 5.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-00108](#).

### 5.4 Altium Project

To download the Altium project files, see the design files at [TIDA-00108](#).

### 5.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-00108](#).

## 5.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-00108](#).

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