TI Designs

24-V_{AC} Power Stage With Wide V_{IN} Converter and Battery Backup Reference Design for Smart Thermostat

Description

This TI Design provides a low BOM cost, high-efficiency power stage solution for smart thermostats, and other gateway building automation end equipment. This power stage takes a 24-V_{AC} input and produces a 5-V and 3.3-V output rail, which can power additional point-of-load converters if added. The design provides LiPo battery charging and seamless switching to battery power during a 24-V_{AC} brownout. The power-path capability provides battery power assistance allowing system load transient to exceed the current limit of the 24-V_{AC} to DC system, allowing a lower cost wide V_{IN} buck to be used.

Resources

TIDA-01358	Design Folder
LM5166	Product Folder
bq24072	Product Folder
TLV62080	Product Folder
TPS27081A	Product Folder
LM2903	Product Folder
TPD2E2U06	Product Folder
TPD1E10B06	Product Folder

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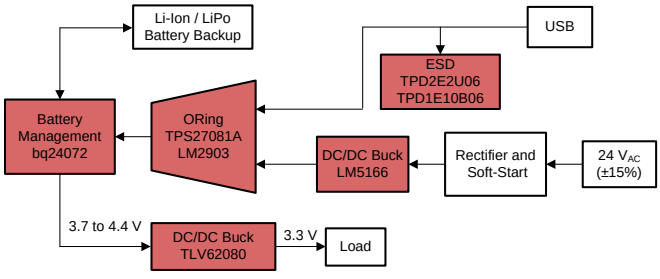
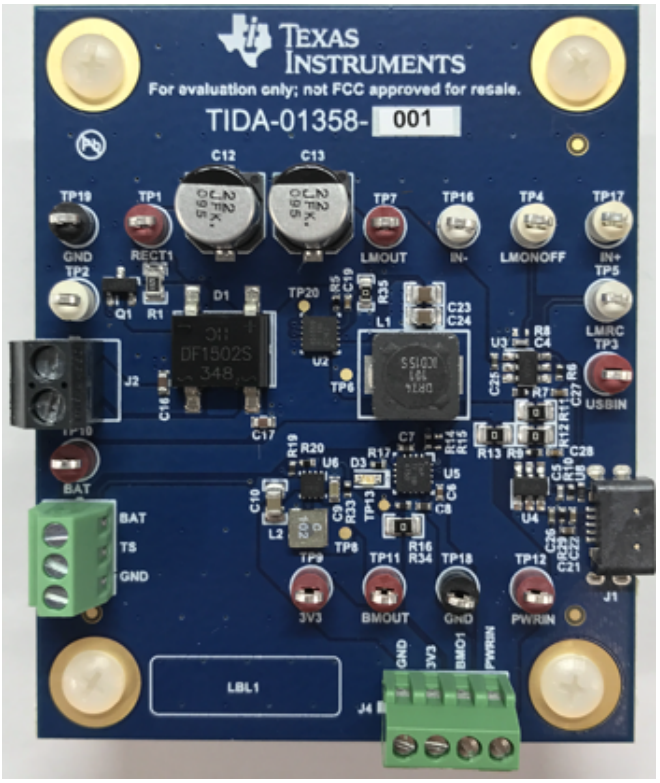


Features

- 24-V_{AC} or USB to 3.3-V Power Rail
- Battery Backup
- Independent Battery Charging and Load Path
- Dynamic Power Path and Battery Power Assist
- High Efficiency Over Entire Load Current Range
- USB Overcurrent Compliant
- Discrete Solution

Applications

- Thermostat
- Video Doorbell
- Wireless Video Surveillance
- Gateway



1 System Overview

1.1 System Description

A typical home uses a 24-V_{AC} system to power the HVAC system. Thermostats, as well as many other home automation equipment, use this 24-V_{AC} for power. Therefore, a power stage is needed to rectify the 24-V_{AC} and supply a DC voltage at the levels required by the thermostats internal components. Low cost is typically a priority for thermostat designs as board space is often plentiful enough to avoid small-footprint, high-cost parts. For thermostats implementing a chargeable battery backup system, high efficiency also becomes a priority to allow a smaller, and therefore lower cost, battery to be used. The TIDA-01358 focuses on these priorities and can be easily adjusted to meet specific needs.

In addition to the 24-V_{AC} and battery backup, this TI Design allows a USB power supply to be used for charging and powering the system. Having two supply options, 24 V_{AC} and USB, requires an ORing device. ORing and power mux devices can be high in cost and therefore are avoided by designers; this TI Design provides a discrete based ORing solution that cuts costs significantly over fully featured integrated solutions. If a USB is not desired, device can be removed with very minimal changes to the design.

The 24 V_{AC} is rectified and stepped down to a 5-V rail using an ultra-low I_Q, wide V_{IN}, 500-mA buck converter. The wide V_{IN} of the buck converter helps handle transients, thus eliminating the need for a TVS diode and other protection circuitry. Smaller capacitors may be used as the input voltage ripple can be higher when using a wide V_{IN} buck.

The TIDA-01358 uses a battery management device that allows independent current paths and monitoring for system power and battery charging. This device increases the cycle life of the battery. This TI Design features a seamless transition to battery power should the main supply fail, as well as battery power assist should the load requirement surpass the main supply's rating. A very efficient, low cost, and low BOM count buck converter is used to step down the battery management voltage to 3.3 V for use by the general system. Both DC-DC buck converters in this design feature low-load power saving feature to provide high efficiency even at light loads.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	NOTES
Target application	Thermostat, gateway building automation	—
Main Input power source	20 V_{AC}	—
Secondary input power source	USB	—
LM5166 (RectOut to LMOut) efficiency	87.0%	160-mA output
TLV62080 (Battery to 3.3 V) efficiency	96.6%	160-mA output
LM5166 load regulation	1.41%	160-mA nominal output current and 24-V_{AC} nominal input voltage
TLV62080 load regulation	0.12%	160-mA nominal output current and nominal 3.7-V battery input
LM5166 max output current	500 mA	5-V bus
TLV62080 max output current	1 A	3.3-V bus
Working environment	Indoor	—
Form factor	52.324×64.262-mm rectangular PCB	—

1.3 Block Diagram

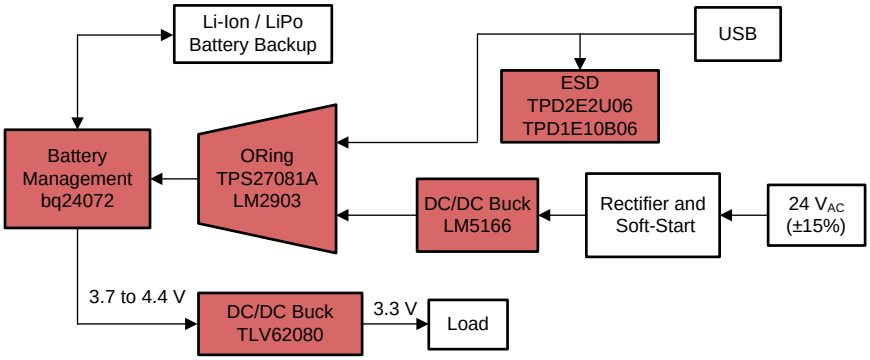


Figure 1. TIDA-01358 Block Diagram

1.4 Highlighted Products

Key features for selecting the devices for this reference design are highlighted in the following subsections. Find the complete details of the highlighted devices in their respective product datasheets.

1.4.1 LM5166

The LM5166 regulator is an easy-to-use synchronous buck DC/DC converter that operates from a 3.0- to 65-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated and fully-regulated supply rails. With integrated high-side and low-side power MOSFETs, the LM5166 delivers up to 500-mA DC load current with exceptional efficiency and ultra-low input quiescent current in a very small solution size.

Designed for simple implementation, a choice of operating modes offers flexibility to optimize its usage according to the target application. Fixed-frequency, constant on-time (COT) operation with discontinuous conduction mode (DCM) at light loads is ideal for low-noise, high current, fast transient load requirements. Alternatively, pulse frequency modulation (PFM) mode achieves ultra-high, light-load efficiency performance. Control loop compensation is not required with either operating mode, reducing design time and external component count.

The LM5166 incorporates other features for comprehensive system requirements, including an open-drain Power Good circuit for power-rail sequencing and fault reporting, internally-fixed or externally-adjustable soft-start, monotonic startup into pre-biased loads, precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO), and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple and optimized PCB layout, requiring only a few external components.

The high-side p-channel MOSFET buck switch operates at 100% duty cycle in low dropout voltage conditions and does not require a bootstrap capacitor for gate drive.

In the TIDA-01358, the LM5166 serves to step down the rectified voltage from the 24-V_{AC} system to 5 V_{DC} for use by battery management system.

1.4.2 bq24072

The bq2407x series of devices are integrated Li-Ion sources linear chargers and system power path management devices targeted at space-limited portable applications. The devices operate from either a USB port or an AC adapter and support charge currents up to 1.5 A. The input voltage range with input overvoltage protection supports unregulated adapters. The USB input current limit accuracy and start up sequence allow the bq2407x to meet USB-IF inrush current specifications. Additionally, the input dynamic power management (V_{IN-DPM}) prevents the charger from crashing incorrectly configured USB wall adapters sources.

The bq2407x features dynamic power path management (DPPM) that powers the system while simultaneously and independently charging the battery. The DPPM circuit reduces the charge current when the input current limit causes the system output to fall to the DPPM threshold; thus, supplying the system load at all times while monitoring the charge current separately. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack.

1.4.3 TLV62080

The TLV6208x device focuses on high-efficiency step-down conversion over a wide output current range. At medium to heavy loads, the TLV6208x converter operates in PWM mode and automatically enters power save mode operation at light-load currents to maintain high efficiency over the entire load current range.

The TLV62080 synchronous switched-mode converters are based on DCS-Control™. DCS-Control is an advanced regulation topology that combines the advantages of hysteresis and voltage mode control.

Features:

- 2.5- to 5.5-V input voltage range
- 100% duty cycle for lowest dropout
- Power good output
- Power save mode for light load efficiency
- DCS-Control architecture for fast transient regulation

1.4.4 TPS27081A

The TPS27081A device is a high-side load switch that integrates a Power PFET and a Control NFET in a small package. The TPS27081A device is capable fo handing up to 8 V and 3 A. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance P-channel MOSFET, which reduces the dropout voltage through the device.

In the TIDA-01358, the TPS27081A device is used in conjunction with the LM2903 in a low-cost power ORing circuit to switch between the USB source and the LM5166 source.

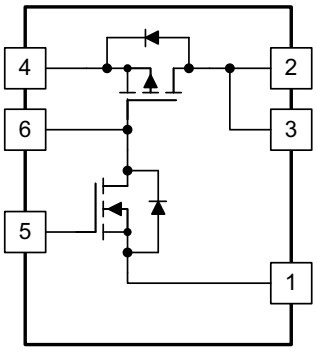


Figure 2. TPS27081A Basic Schematic

1.4.5 LM2903

The LM2903 consists of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range (2 to 36 V), low I_Q and fast response of the devices.

The open-drain output allows the user to configure the output's logic low voltage (VOL) and can be used to enable the comparator to be used in AND functionality.

Features:

- Low output saturation voltage
- Maximum rating: 2 to 36 V
- Low input bias current: 25 nA (typical)
- Common-mode input voltage range includes ground

The LM2903 is used as the logic for the power ORing circuit in the TIDA-01358.

1.4.6 TPD2E2U06

The TPD2E2U06 is a dual-channel low capacitance TVS diode electrostatic discharge (ESD) protection device. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I^2C.

Features:

- 5.5-A peak pulse current (8/29-µs pulse)
- Ultra-low leakage current 10 nA (max)
- Low ESD clamping voltage
- DC breakdown voltage 6.5 V (min)

The TPD2E2U06 is used on the USB communicated lines in the TIDA-01358.

1.4.7 TPD1E10B06

The TPD1E10B06 device is a single-channel 1 ESD transient voltage suppression (TVS) diode in a small 0402 package. This TVS protection product offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support. The 12-pF line capacitance of this ESD protection diode is suitable for a wide range of applications supporting data rates up to 400 Mbps. The 0402 package is an industry standard and is convenient for component placement in space-saving applications.

Typical applications of this ESD protection product are circuit protection for audio lines (microphone, earphone, and speakerphone), SD interfacing, keypad or other buttons, VBUS pin and ID pin of USB ports, and general-purpose I/O ports. This ESD clamp is good for the protection of the end equipment like ebooks, tablets, remote controllers, wearables, set-top boxes, and electronic point of sale equipment.

The TPD1E10B06 is used to protect the USB VBUS pin on the TIDA-01358.

2 System Design Theory

The TIDA-01358 provides the main power stages needed for building automation electronics that are primarily powered from the 24-V_{AC} system used in typical homes. This TI Design presents a system solution that is modular in design, allowing system designers to easily modify the design if necessary to more closely match their product's specifications.

Cost reduction is a priority in this TI Design. Efficiency, particularly when using the battery backup, and heat loss are taken into consideration as well. To keep costs low, avoiding an over engineered system is required. The discrete nature of the TIDA-01358 allows designers to easily remove features they do not need, or easily add features and power rails that are required for their specific application.

This section outlines the theory and design considerations used to develop and design the TIDA-01358.

2.1 24-V_{AC} to DC Rectification

A full-bridge rectifier is used for DC rectification. To prevent a significantly large inrush current during initial connection of 24 V_{AC}, a soft-start circuit is implemented.

The schematic shown in Figure 3 shows the rectification and soft-start process. C1, C2, and C3 function as high frequency bypass capacitors. R1, R2, C4, and C5 provide the soft-start time constant for the gate of the N-channel MOSFET (T1). Q1 has a gate threshold voltage range of 1.0 to 2.5 V and a 92-mΩ $R_{DS(on)max}$ at V_{GS} = 10 V. The values of R_2 and R_3 are chosen to voltage divide a maximum of 42 V (the peak of the 24 V_{AC} at the high end of its tolerance) down to approximately 10 V once steady state has been reached. Calculating R_2 and R_3 is shown in Equation 1:

$$42\ V\left(\frac{R_2}{R_2 + R_3}\right) = 42\ V\left(\frac{150\ k\Omega}{150\ k\Omega + 453\ k\Omega}\right) = 10.4\ V \quad (1)$$

Z1 is used as a protective device for the MOSFET gate. R4 is used to provide an initial current path while T1 is still open. The use of R4 prevents significantly differing soft-start times due to variances in the 24-V_{AC} transformer and Q1's gate threshold voltage. The resulting circuit provides a relatively consistent soft-start time regardless of the 24-V_{AC} source variances.

C6 and C7 function as the rectifier's smoothing capacitors. The TIDA-01358 has a maximum power output of 3.3 W. The output ripple will be a function of the load current. TINA-TI™ simulation shows a maximum worst case ripple of 11.7 V. This maximum assumes 4.3 W is required at the input to produce 3.3 W at the output and occurs when the 24-V_{AC} transformer is at the low-voltage edge of its tolerance and the output power of the 3.3-V rail is outputting its maximum current of 1 A. That worst case condition is typically unlikely to occur depending on application; a more reasonable use case of a 100-mA output from the 3.3-V rail and a nominal 24-V_{AC} transformer provides a rectification ripple of approximately 1.4 V. These ripple voltages must be checked in each application it is used. Even at the worse case scenario as previously outlined, the LM5166 buck converter is capable of handling those ripple voltages and voltage ranges.

Figure 4 shows a simulation example of the schematic detailed in Figure 3 under an input power of approximately 750 mW. The time from applied input power to the rectifier's output reaching steady-state is approximately 300 ms.

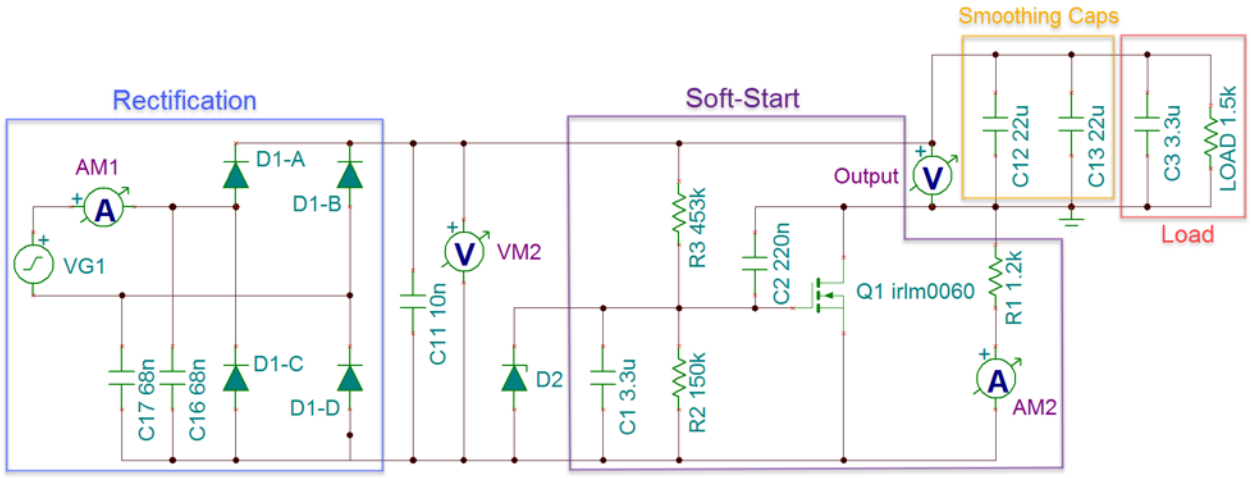


Figure 3. Soft-Start Schematic

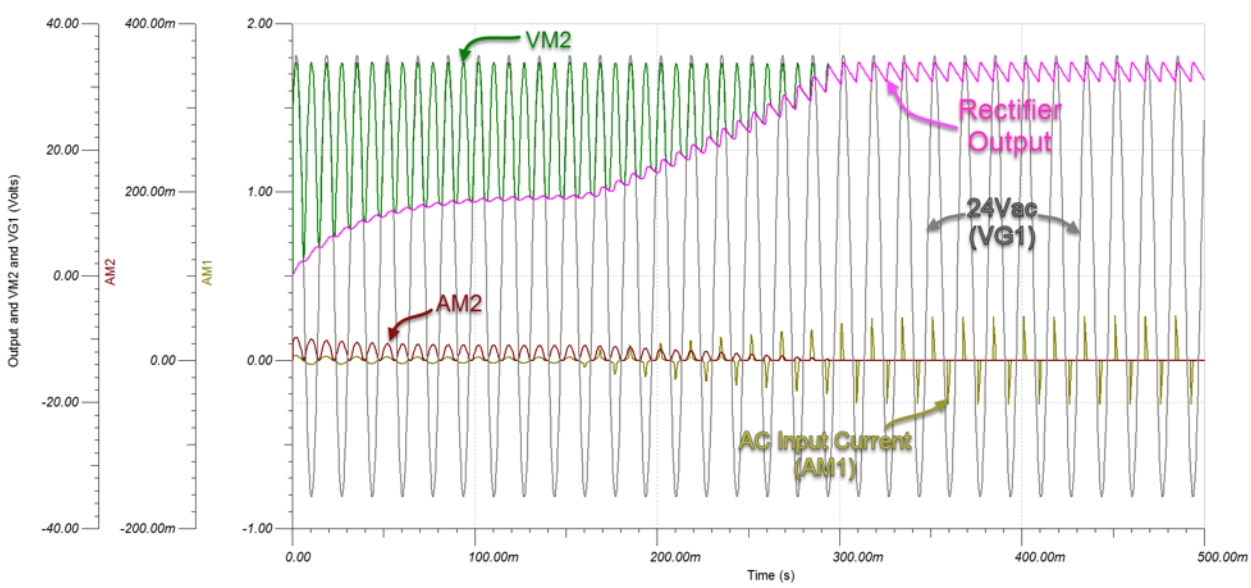


Figure 4. Soft-Start TINA-TI Simulation Example

2.2 5-V Rails

This section provides detail on both the LM5166 wide V_{IN} buck that converts the rectified 24 V_{AC} to 5 V as well as the USB 5-V rail.

2.2.1 LM5166 Voltage Rail

The LM5166 is the optimal choice of device for this design. The device has a very wide input voltage range (3 to 65 V), yet it allows 500-mA loads and does so in a small package. It has an extremely low no-load quiescent current and high efficiency at light loads.

The LM5166 is used to convert the rectified 24-V_{AC} source to 5 V_{DC} and is used as the primary source of power in the TIDA-01358.

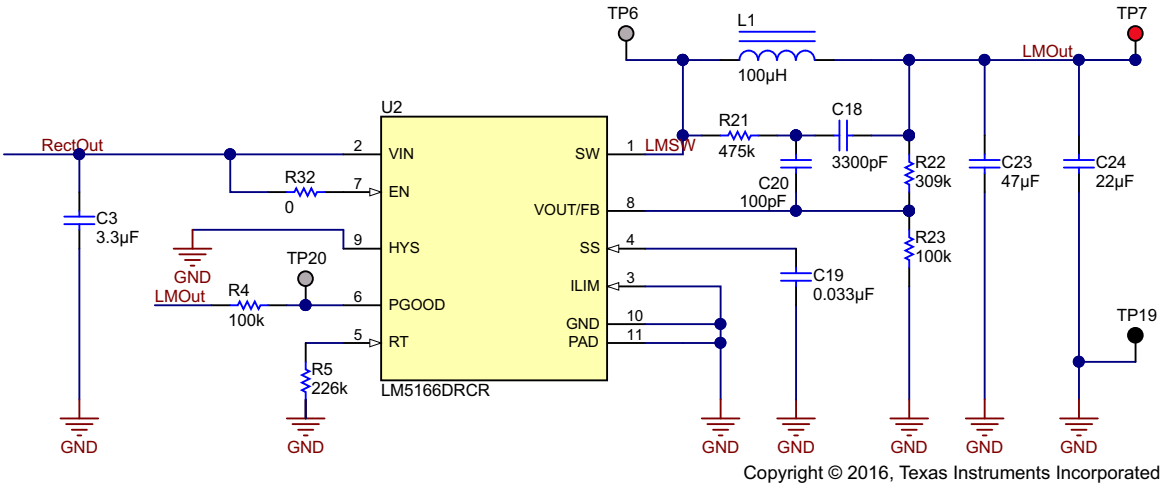


Figure 5. LM5166 Implementation

The TIDA-01358 uses the COT type III (COT III) method of the LM5166 to reduce the amount of output noise and ripple. Depending on the application, COT I, COT II, or PFM can be used to further reduce costs or quiescent current. However, a lower ripple will be more ideal for devices uses wireless technologies and systems needing reduced switching noise. To program the LM5166 to operate in COT mode, a resister, R5, is connected between the RT and GND pins. The value of R5 determines the switching frequency of the device per Equation 2. A low switching frequency of approximately 130 kHz will provide a higher efficiency.

$$R_5 = R_{RT}(k\Omega) = \frac{V_{OUT}(V)}{f_{sw}(kHz)} \times \frac{10^4}{1.75} = \frac{5.0\ V}{130\ \ kHz} \times \frac{10^4}{1.75} = 226\ k\Omega \quad (2)$$

The COT III ripple method uses a ripple injection circuit with R_{21}, C_{18}, and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is then AC-coupled into the feedback node (FB) with the capacitor C_{20}. Because this circuit does not use the output voltage ripple, it is suited for applications where low output voltage ripple is critical. Application note AN-1481[4] provides additional details on this strategy.

Datasheet recommendation for R_{23} is 10 to 100 kΩ for most applications. Higher resistance values are more susceptible to noise and therefore require a more careful PCB layout. In the TIDA-01358, R_{23} is chosen to be 100 kΩ and R_{22} is calculated using Equation 3. A value of 309 kΩ is conservatively chosen for R_{22}. Equation 4, Equation 5, and Equation 6 provide the value boundaries of C_{18}, C_{20}, and R_{21}. To stay within the calculated boundaries, 3300 pF is chosen for C_{18}, 475 kΩ for R_{21}, and 100 pF for C_{20}.

$$R_{22} = \frac{1.223\ V}{V_{OUT} - 1.223\ V} \times R_{23} = \frac{1.223\ V}{5 - 1.223\ V} \times 100\ k\Omega = 333\ k\Omega \quad (3)$$

$$C_{18} \geq \frac{5}{f_{sw} \times (R_{22} \,||\, R_{23})} \Rightarrow C_{18} \geq \frac{5}{138\ kHz \times \left(\frac{309\ k\Omega \times 100\ k\Omega}{309\ k\Omega + 100\ k\Omega}\right)} \Rightarrow C_{18} \geq 480\ pF \quad (4)$$

$$C_{20} \geq \frac{1}{2\pi \times f_{SW} \times \left(R_{22} \| R_{23}\right)} \Rightarrow C_{20} \geq \frac{1}{2\pi \times 138000 \times \left(\frac{309\ k\Omega \times 100\ k\Omega}{309\ k\Omega + 100\ k\Omega}\right)} \Rightarrow C_{20} \geq 15.3\ pF \quad (5)$$

$$R_{21}C_{18} \geq \frac{\left(V_{IN} - V_{OUT}\right) \times t_{on(@V_{IN})}}{20\ mV} \Rightarrow R_{21}C_{18} \geq \frac{\left(35\ V - 5\ V\right) \times \left(\frac{1}{138\ kHz} \times \frac{5\ V}{35\ V}\right)}{20\ mV} \Rightarrow R_{21}C_{18} \geq 1.553 \times 10^{-3} \quad (6)$$

The LM5166 prevents overcurrent conditions by cycle-by-cycle current limiting of the peak inductor current. The current sensed in the high-side MOSFET is compared every switching cycle to the current limit threshold set by the ILIM pin. When operating in COT mode, connecting the ILIM pin to GND will set a typical high-side FET current limit of 750 mA and low-side FET limit of 400 mA providing a maximum average DC current output of 500 mA.

The Enable pin is tied to V_{IN} and hysteresis is not used and thus tied to GND. Power good (PGOOD) is an open-drain output and is pulled up with a datasheet recommended 100-kΩ resistor R_4. The soft-start (SS) time can be programmable with an external capacitor C_{19} or left open for a default 900-µs soft-start time. An external capacitor was chosen for the TIDA-01358 to allow adjustability depending on application. Using Equation 7 and a desired soft-start time of approximately 4 ms provides a capacitance value of 0.033 µF for C_{19}.

$$C_{19} = C_{SS}\left(nF\right) = 8.1 \times t_{SS}\left(ms\right) = 8.1 \times 4 \cong 33\ nF \quad (7)$$

To calculate the value needed for L1, a desired inductor ripple current is needed. Knowing that the average DC output current is 500 mA while the peak inductor current cannot exceed 750 mA, the maximum ripple current allowed is 100% (inductor current swing from 250 to 750 mA providing a 500-mA total ripple). A more appropriate value for most applications is around 50%, 250-mA, inductor current ripple. A nominal inductance based on a 50% inductor current ripple is shown in Equation 8.

$$L1 = \frac{V_{LMOut}}{f_{SW} \times \Delta I_{L(nom)}} \times \left(1 - \frac{V_{LMOut}}{Rect_{Out}}\right) = \frac{5\ V}{138\ kHz \times 250\ mA} \times \left(1 - \frac{5\ V}{35\ V}\right) = 124\ \mu H \quad (8)$$

A lower value of 100 µH is chosen to improve efficiency and lower BOM size at the cost of additional inductor current ripple. The current ripple in this case is calculated in Equation 9 and the inductor current peak is subsequently calculated in Equation 10 and shows the peak stays within the 750-mA limit.

$$\Delta I_{L(nom)} = \frac{V_{LMOut}}{f_{SW} \times L1} \times \left(1 - \frac{V_{LMOut}}{V_{IN}}\right) = \frac{5\ V}{138\ kHz \times 100\ \mu H} \times \left(1 - \frac{5\ V}{35\ V}\right) = 311\ mA \quad (9)$$

$$I_{L1(peak)} = I_{OUT(max)} + \frac{\Delta I_{L(nom)}}{2} = 500\ mA + \frac{311\ mA}{2} = 656\ mA \quad (10)$$

Choose output capacitors C_{23} and C_{24} to satisfy Equation 11. Additionally, take into account the DC de-rating of the capacitors.

$$C_{Out} = C_{23} + C_{24} \geq \frac{\Delta I_{L(nom)}}{8 \times f_{SW} \times \Delta V_{LMOut}} \Rightarrow C_{23} + C_{24} \geq \frac{311\ mA}{8 \times 138\ kHz \times 20mV} \Rightarrow C_{23} + C_{24} \geq 14\ \mu F \quad (11)$$

A total capacitance of 69 µF is chosen to account for tolerances and de-rating at 5 V.

2.2.2 USB Power Input

Like the LM5166, the USB power input is capable of powering the entire system. The USB can serve as a backup power source, be used for debugging other aspects of the product's systems, or be used to charge the battery should the main 24 V_{AC} not be available. The TIDA-01358 does not supply power to USB; it only sinks power from a USB host. ESD and overvoltage protection are included as shown in Figure 6.

This TI Design uses USB 2.0, and therefore assumes the max current that can pulled from a USB host is 500 mA. USB 2.0 specification allows a tolerance of 5% from the nominal 5 V, thereby giving a host voltage range of 4.75 5.25 V. Furthermore, USB 2.0 specification also allows the worst case voltage drop across all cables and connectors to bring the total voltage at load to 4.35 V. The TIDA-01358 is designed to accommodate USB 2.0 at its worst case specification.

$R_{29}$and C_{21} provide a snubber circuit to the USB Vbus, reducing the overshoot and ringing caused the cable inductance and capacitive load resonance. The snubber circuit must be tuned for each system design; therefore, the snubber component values used in the TIDA-01358 must be tested when designed into a new system and the values must be changed appropriately. The ORing circuit used in this TI Design has a maximum input voltage rating of 8 V, so the USB voltage must remain below that threshold and within USB specifications.

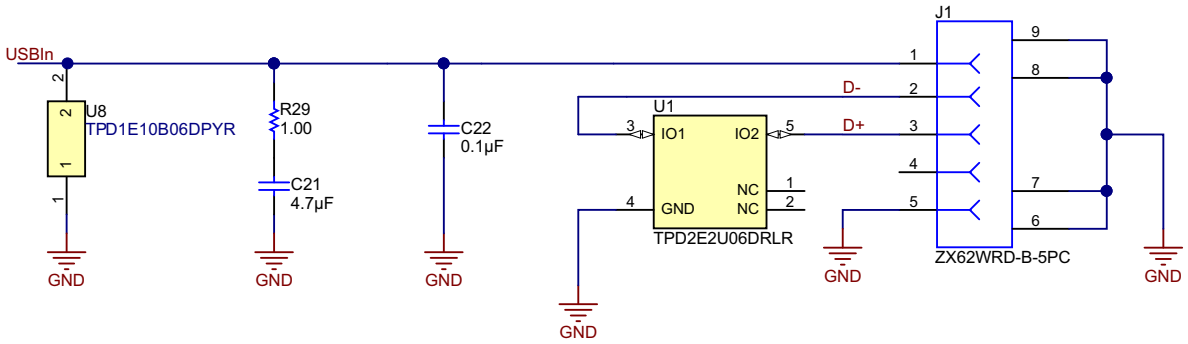


Figure 6. USB Implementation

2.3 Power Source ORing

The ORing section of the TIDA-01358 is designed to reduce costs while still allowing full system functionality from a USB power rail providing as little as 4.35 V.

A simple two-diode ORing configuration is not possible due to the voltage drop of forward biased diodes. The bq24072 battery management system used in this TI Design recommends a minimum of 4.35 V. USB 2.0 specifications allow the USB power bus to drop to 4.35 V at load. Therefore, there is virtually no margin available and thus basic diode oring cannot be used. A fully integrated power muxing chip is an option, though the costs are significantly higher and is thus avoided in this design. The ORing solution used in the TIDA-01358 uses two integrated N-FET/P-FET pairs and a basic comparator to accomplish power muxing capability at a significantly lower cost than a fully integrated solution.

As shown in Figure 7, U3 and U4 are TPS27081A chips, each containing an N-channel and P-channel MOSFET. U7, the LM2903, provides the basic logic necessary to accomplish the ORing. This ORing solution prioritizes one source over another should both sources be available simultaneously. Net "LMOut" Is connected to the 5-V output rail of the LM5166 while "USBIn" is connected to the USB power bus.

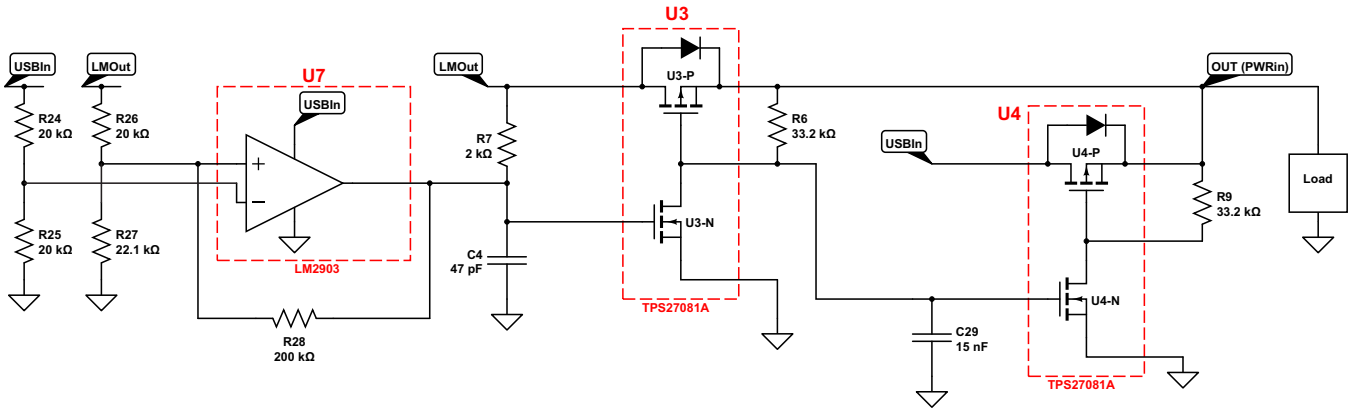


Figure 7. Power ORing Schematic

2.3.1 LMOut (LM5166) Priority

The 24-V_{AC} power, and consequently the LM5166 5-V rail, is considered the main power source for this system and should be prioritized above USB power or battery backup power. The ORing solution in this TI Design is designed to prioritize one source over another—in this case, the LM5166 over USB.

Figure 8 provides a visual overview of the functionality when the LM5166 is providing 5 V. The gate of the U3-N is pulled up through R7 to LMOut, thereby turning U3-N on and forcing the drain of the U3-N to GND. The drain of the U3-N is shorted to the gate of the U4-N. As a result, anytime U3-N is on, U4-N is off. U3-P is then turned on due to its gate being pulled to GND, and U4-P is turned off due to its gate being pulled up through R9. LMOut is then passed to the load.

The comparator's surrounding resistor values are chosen to ensure the non-inverting terminal will be higher than the inverting terminal if LMOut is suppling 5 V, resulting in the comparator's output being Hi-Z and thus having virtually no effect on the circuit. This setup allows the LM5166 to dominate the ORing circuit over USB should the USB be plugged in when the LM5166 is already supplying power.

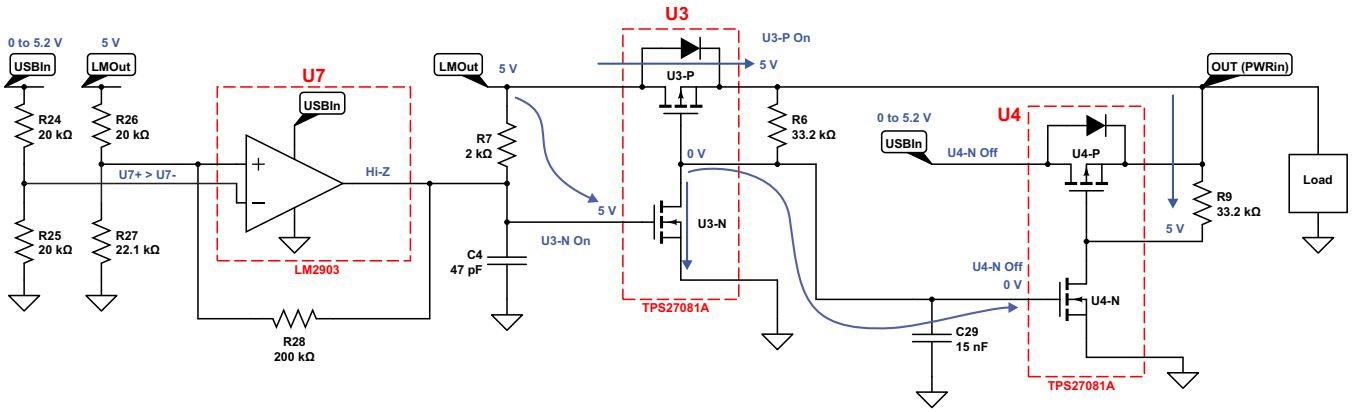


Figure 8. LM5166 Supplied Power ORing

2.3.2 USB While 24 V_{AC} is Absent

Figure 9 provides the visual overview of the ORing process when the USB is present and the 24-V_{AC} power line is absent. In this scenario, the comparator is most needed.

When Net "LMOut" is absent and "USBIn" is 4.35 to 5.25 V, the inverting input to the comparator becomes greater than the non-inverting input and the comparator drives the output terminal low, thereby turning off U3-N. With U3-N turned off, "USBIn" drives the gate of U4-N and the gate of U3-P high, turning off U3-P and turning on U4-N. U4-P will turn on as a result, and the USB voltage will be passed to the load.

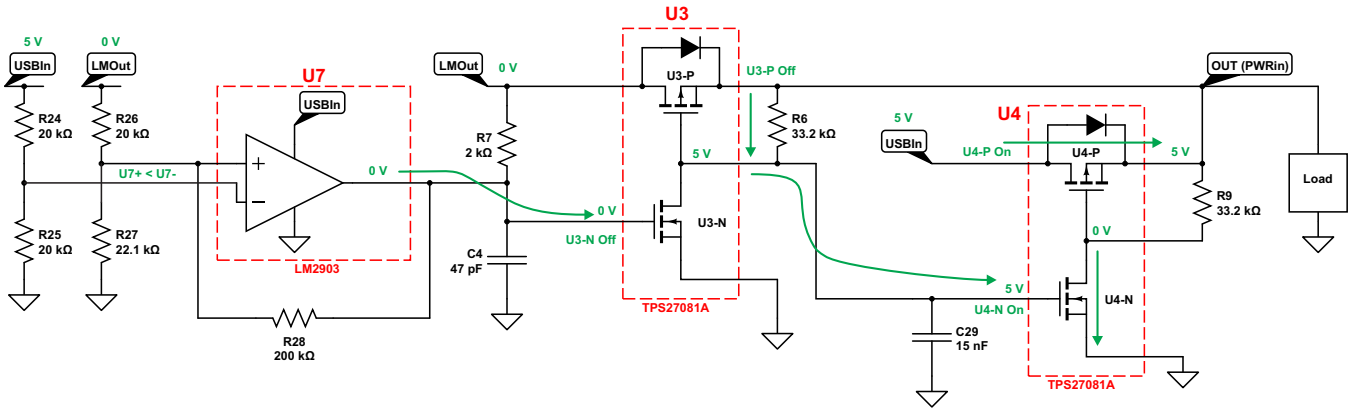


Figure 9. USB Supplied Power ORing

2.3.3 Comparator Design and Calculations

The comparator's primary function is to provide the system an active method to drive the U3 fets off. When both sources are available, the comparator ensures that the U3 fets will not latch should LMOut become unexpectedly unavailable (that is, 24-V_{AC} power is unplugged). The comparator also prevents a voltage spike due to the drain-to-source capacitance from latching the U3 fets on when USB is initially plugged in. Hysteretics is used on the comparator to ensure the device does not oscillate about the threshold voltage and ensures the U3 fets are turned fully off when switching to USB power.

The resistors chosen must ensure that when LMOut is present (for example, 5 V in the TIDA-01358), the USBIn required to drive the comparator low exceeds the maximum possible USB voltage use case. USB 2.0 specifications allow the power bus to reach a maximum of 5.25 V; therefore, the USBIn required to drive the comparator low must be larger than 5.25 V to ensure the condition never becomes true during operation. When the comparator output is High-Z, R_{28} is virtually in parallel with R_{26} thus raising the non-inverting terminal of comparator, requiring a higher USB voltage to drive the comparator's output low. The equivalent resistance of R_{26} in parallel with R_{28} is:

$$R_{eqH} = \frac{20\,k\Omega \times 200\,k\Omega}{20\,k\Omega + 200\,k\Omega} = 18.18\,k\Omega \tag{12}$$

Given LMOut is 5 V, the non-inverting input is calculated with a basic voltage divider:

$$IN + LR = LMOut \times \left(\frac{R_{27}}{R_{27} + R_{eqH}} \right) = 5\ V \times \left(\frac{22.1\,k\Omega}{22.1\,k\Omega + 18.18\,k\Omega} \right) = 2.74\ V \tag{13}$$

Therefore, the inverting terminal, must exceed 2.74 V. Because R_{24} and R_{25} are of equal resistance, 20 kΩ, the required USBIn to drive the comparator low is twice the required inverting terminal.

$$USBIn_{LR} = 2 \times IN + LR = 2 \times 2.74\ V = 5.48\ V \tag{14}$$

Because 5.48 V is higher than the maximum USB specification, the comparator cannot be driven low by a USB plugin if the LM5166 is already supplying power.

To account for the opposite scenario, USB was initially present and 24 V_{AC} was subsequently provided, the same threshold calculations must be performed for when the comparator's output was initially low. This scenario is unlikely to occur in the specific end products this TI Design targets; however, such a scenario is planned for regardless.

When the USB is present with LMOut absent, the comparator output is low (see Section 2.3.2). Therefore, R_{28} is virtually in parallel with R_{27} providing an equivalent resistance:

$$R_{eqL} = \frac{22.1\,k\Omega \times 200\,k\Omega}{22.1\,k\Omega + 200\,k\Omega} = 19.9\,k\Omega \tag{15}$$

Given USBIn is at nominal 5 V, and thus the inverting terminal is 2.5 V through the voltage divider of R_{24} and R_{25}, the required LMOut needed to produce a non-inverting terminal voltage greater than 2.5 V is calculated in Equation 16.

$$LMOut_{HZR} = IN - \times \left(\frac{R_{eqL}\ R_{26}}{R_{eqL}} \right) = 2.5\ V \times \left(\frac{19.9\,k\Omega + 20\,k\Omega}{19.9\,k\Omega} \right) = 5.01\ V \tag{16}$$

The voltage drop across a USB cable during current draw is significant enough to assume that USBIn will not sit at the nominal 5 V, nor the maximum 5.25 V, at the ORing input. Therefore, the 5 V of the LM5166 will dominate the ORing circuit should the USB be 5 V or less.

2.4 Battery Management

Battery charging and power path management are performed by the bq24072 in the TIDA-01358. The bq24072 provides a low-cost solution that features independent battery charging and load paths through its power path capability without the need for any external FETs. The device can monitor battery temperature through a dedicated pin, ensures USB compliant inrush current and current limits, and provides PGOOD and charge signals.

The bq24072 is a single-power input device and was specifically chosen over dual-input devices due to cost. The bq24072 and ORing detailed in Section 2.3 provide the same functionality as a fully integrated dual-input device but at a lower cost. The TIDA-01358 is designed with an understanding that end products may have different requirements and that ease of design changes to fit individual systems is necessary. If the end product does not use USB (or a secondary power source in general), the ORing solution and the USB related components detailed in Section 2.2.2 can be eliminated and the single input of the bq24072 can be used for an even lower cost solution. In such a scenario, a dual-input battery management IC would be over-engineered for the application and would incur unnecessary costs or significant design changes. For those reasons, the bq24072 was chosen as the ideal low-cost solution.

The bq24072 features power path capability, allowing the battery to supplement the main power source to meet high load demands. This feature allows the use of a smaller main power source, thus reducing costs further.

Figure 10 displays the setup and components chosen for the TIDA-01358. The bq24072 has a minimum recommended input voltage of 4.35 V, V_{OVP} of 6.6 V, and a maximum absolute input voltage of 28 V. The device charges the battery up to 4.2 V ($V_{BAT(REG)}$). The output is regulated to 200 mV above $V_{BAT(REG)}$.

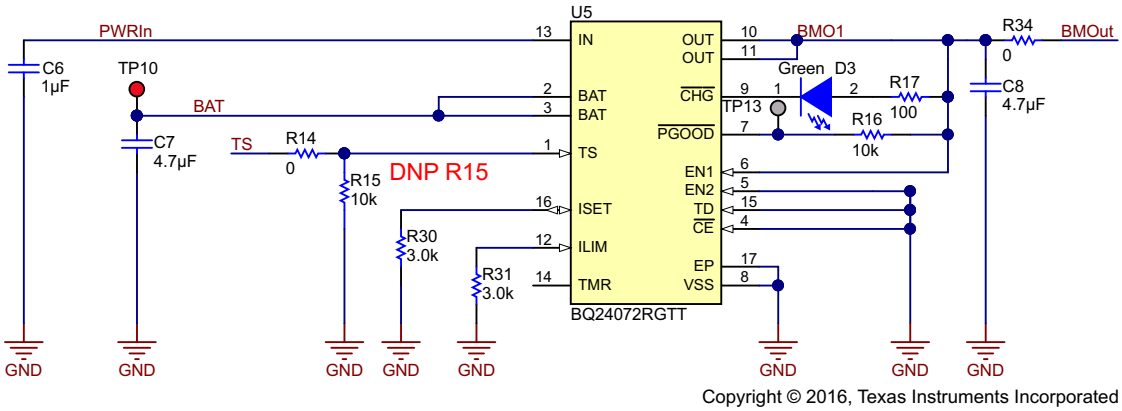


Figure 10. Battery Management Implementation

A small input cap (C6) is chosen as USB 2.0 specifications requires less than 10 µF to be hard started. The bq24072 datasheet recommends between 1 and 10 µF of the input capacitance. A 4.7-µF battery input capacitor (C7) was chosen per datasheet recommendation. The output capacitor (C8) of 4.7 µF is the minimum recommended value per the datasheet.

To comply with USB 2.0 specifications, the input current must be limited to 500 mA. The EN1, EN2, and ILIM pins of the bq24072 allow a programmable current limit. As per datasheet, EN1 is set HIGH and EN2 is set LOW to program a 500-mA current limit. ILIM must not be left floating, as doing so would disable charging, so the ILIM is set to provide a higher current limit (536 mA) than the EN1/EN2 pins, which allows the EN1/EN2 current limit to be the dominant, more conservative limit. Equation 17 shows the calculation used in the TIDA-01358 for R_{31}.

NOTE: K_{ILIM} is a datasheet provided value for current limits above 500 mA.

$$R_{31} = R_{ILIM} = \frac{K_{ILIM}}{I_{IN-MAX}} = \frac{1610\ A\Omega}{536\ mA} = 3\ k\Omega \quad (17)$$

R_{30} is connected to the ISET pin and determines the battery's fast charge current level ($I_{O(CHG)}$ shown in Figure 11. The calculation for R30 in this TI Design is shown in Equation 18. However, the fast charge current must be chosen depending on the battery specifications used in the end product.

$$R_{30} = R_{ISET} = \frac{K_{ISET}}{I_{O(CHG)}} = \frac{890\ A\Omega}{300\ mA} \cong 3\ k\Omega \quad (18)$$

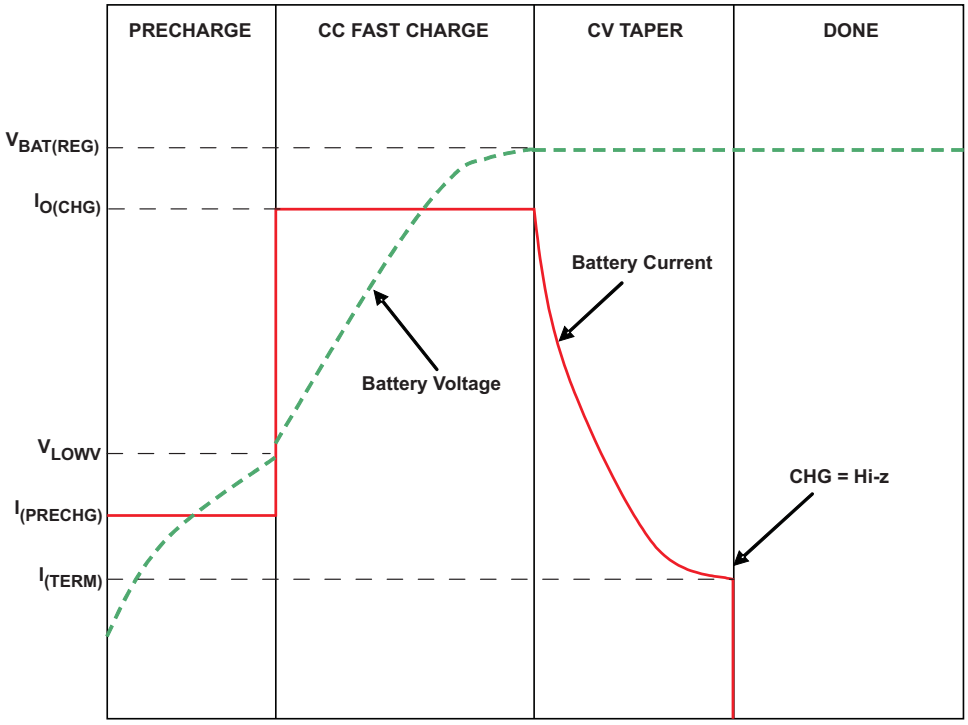


Figure 11. Typical Battery Charge Cycle

Net "TS" is used to monitor the battery temperature on battery packs that have a built-in thermistor. If using TS, R15 must be not populated. Use R15 if leaving TS floating and not using temp sensing. The value of 10k is per datasheet recommendation.

The "TMR" pin is left unconnected to set the pre-charge and fasts-charge safety timers to their default values. The pre-charge safety timer will be set to a typical value of 1800 seconds. The charge safety timer will be set to a typical value of 18000 seconds. Pin "TD" is tied to GND to enable charger termination. Pin "CE" is tied to DNG to enable the battery charger. PGOOD is pulled to VSS when a valid input source is detected and is high impedance when the input power is not within specified limits. PGOOD can sink a maximum of 15 mA so R16 must be chosen appropriately to ensure PGOOD does not sink more than 15 mA.

Pin CHG is pulled to VSS when the battery is charging and is high impedance when the charging is complete or when the charger is disabled. R17 must be chosen to ensure CHG does not sink more than 15 mA. The TIDA-01358 uses an indication LED (D3) on the charge pin. D3 exhibits a typical forward bias voltage of 3.2 V. The appropriate R17 is thus calculated in Equation 19. 100 Ω was chosen to allow less than 15 mA.

$$R_{17} = \frac{V_{OUT(MAX)} - V_{D3(Forward-Bias)}}{15\ mA} = \frac{4.4\ V - 3.2\ V}{15\ mA} = 80\ \Omega \quad (19)$$

2.5 3.3-V Rail—TLV62080

The 3.3-V rail serves as the main power output that directly supplies power to the various system components in the end product. The input of the TLV62080 is connected to the output of the bq24072. The 3.3-V rail ultimately receives its power from either the 24-V_{AC} line, USB, or the battery, depending on which source is available. Devices powered from this rail are battery backup protected and benefit from the power assistance features of the bq24072.

The TLV62080 is a very lost cost, low BOM count, high efficient step-down converter. It has a 100% duty cycle capability, which is particularly useful in battery powered applications such as the TIDA-01358 to achieve the longest operation time by taking full advantage of the whole battery voltage range. The converter features DCS-Control (direct control with seamless transition into power save mode) architecture to achieve excellent load transient performance and output voltage regulation accuracy. The TLV62080 as an output current max of 1.2 A. Should more than a 1.2-A output be required, the TLV62084 offers pin-to-pin compatibility (though the input and output capacitors as well as inductor may need to be changed appropriately) with the TLV62080 but features a 2-A output current. Figure 12 shows the specific system implementation in the TIDA-01358 and highlights the simplicity of the part and the low external BOM count.

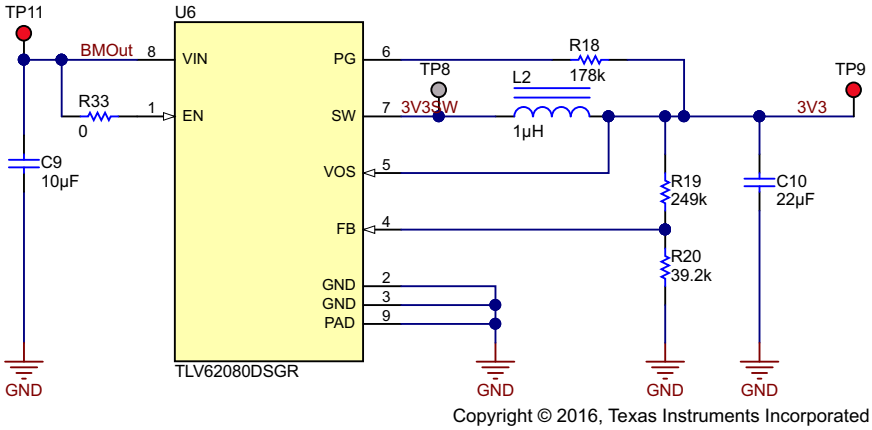


Figure 12. TLV62080 Implementation

Proper inductor selection is critical for buck converters, particularly the inductor value and the saturation current of the inductor. To calculate the maximum inductor current under static load conditions Equation 20 and Equation 21 are used. $I_{OUT,MAX}$ is 1 A per the TIDA-01358 specifications. A desired ΔI_L of approximately 40% of $I_{OUT,MAX}$ is used to set ΔI_L to 0.4 A. During medium to heavy load conditions, the TLV62080 operates in PWM mode at a nominal switching frequency (f_{SW}) of 2 MHz. A maximum input voltage of 4.4 V is used as specified in Section 2.4.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} = 1A + \frac{0.4\ A}{2} = 1.2\ A \tag{20}$$

$$L = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{F_{SW} \times \Delta I_L} \right) = 3.3\ V \times \left(\frac{1 - \frac{3.3\ V}{4.4\ V}}{2\ MHz \times 0.4} \right) = 1.03\ \mu H \cong 1\ \mu H \tag{21}$$

As calculated in Equation 20 and Equation 21, a 1-µH inductor must be chosen. Standard practice is to choose an inductor with a saturation current at least 20% to 30% percent higher than $I_{L,MAX}$. The XFL3012-102ME Inductor by manufacturer Coilcraft is a 1-µH inductor with a 2500-mA current rating, a low DC resistance of 35 mΩ, is recommended by the TLV62080 datasheet, and was chosen for L2 in the TIDA-01358.

The output capacitor (C10) value of 22 µF was chosen based on the TLV62080 datasheet recommended output capacitor and inductor combinations. The recommended capacitance anticipates capacitance tolerance and bias voltage de-rating. The effective capacitance can vary by 20% and –50%. An input capacitance (C9) of 10 µF was chosen per datasheet recommendation and will be sufficient for most applications, a larger value reduces input current ripple.

For best accuracy, R_{20} must be kept smaller than 40 kΩ to ensure that the current flowing through R_{20} is at least 100 times larger than I_{FB}. Using Equation 22, a desired output voltage of 3.3 V, a datasheet specified feedback regulation voltage of 0.45 V, and a chosen R_{20} value of 39.2 kΩ, R_{19} is calculated to be 249 kΩ. As with most applications, tight tolerance resistors (less than or equal to 1%) should be used for the feedback network.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{19}}{R_{20}}\right) = 0.45\ V \times \left(1 + \frac{249\ k\Omega}{39.2\ k\Omega}\right) = 3.3\ V \quad (22)$$

VOS serves as the output voltage sense terminal for the internal control loop and must be connected to the output.

3 Getting Started Hardware

3.1 Hardware

Several test points are made available for the each process on the PCB. However, when performing ripple, transient, and efficiency tests, the break out test points should not be used due to parasitic noise. Instead, the output, input, or other point of interest should be measured as close to the IC pins as possible.

Examples of transient test setups are shown in Figure 13, Figure 14, and Figure 15 that uses a barrel wire to GND technique and the current carrying wires soldered directly onto the output capacitor of the DC-DC being tested. These current carrying wires are connected directly to a programmable electronic load and the current is measured through a current probe. When performing efficiency plots, separate wires from the current carrying wires must be used, as shown in Figure 16 to avoid inaccurate measurements due to line voltage drops.

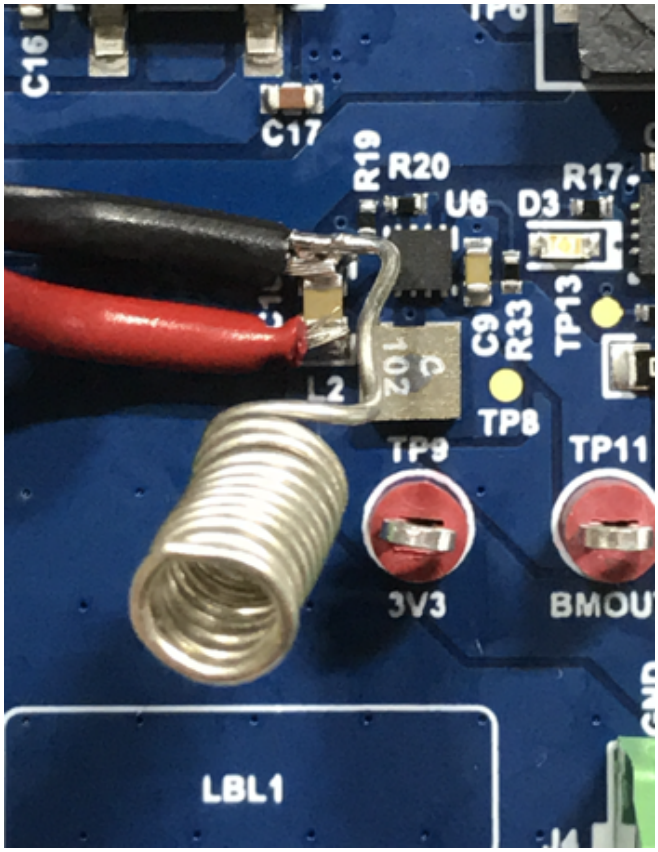


Figure 13. Soldered Output Wires Test Setup

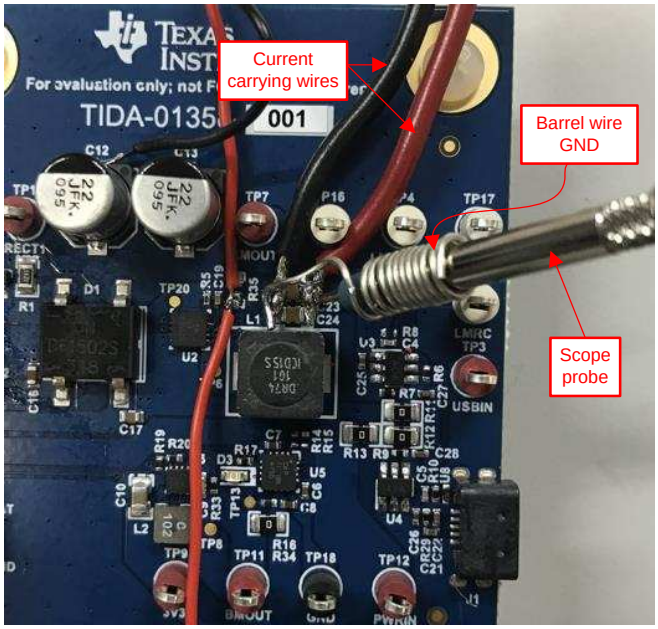


Figure 14. Scope Probe and Barrel Test Setup

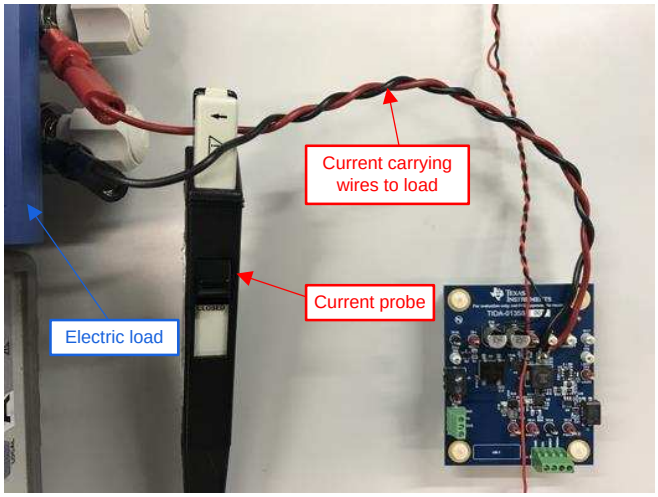


Figure 15. Current Probe and Electronic Load Test Setup

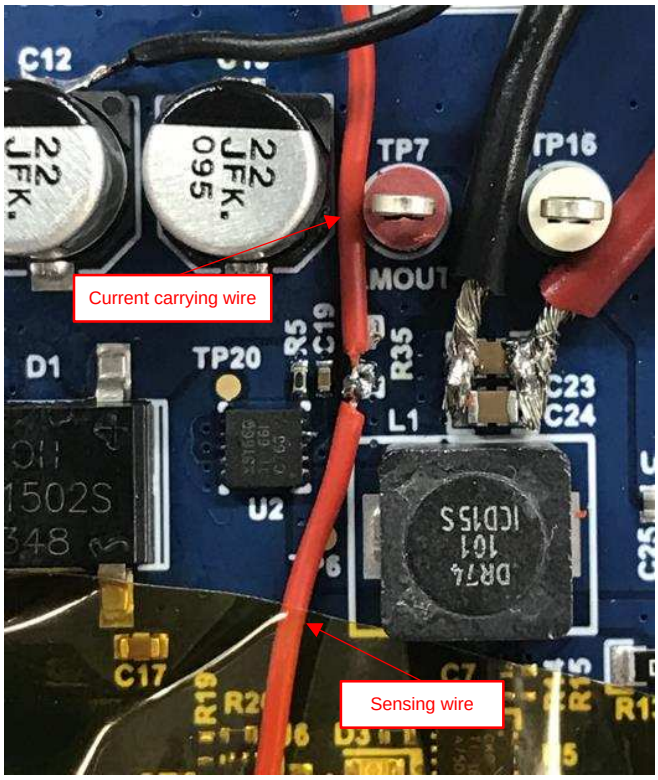


Figure 16. Separate Sensing and Current Carrying Wires Test Setup

4 Testing and Results

Several tests were performed on the TIDA-01358 and are detailed in this section. When testing ripple, transients, and efficiency, the point of measurement is crucial to get accurate measurements. See Section 3 for more testing details.

4.1 Startup, Shutdown, and ORing

This section analyzes the 24-V_{AC} system startup, its soft-start functionality, and provides data showing the consecutive power up of each power stage. USB power is also tested covering the USB specifications voltage range. ORing between the 24-V_{AC} and USB systems are also tested and detailed.

4.1.1 24-V_{AC} Startup and Shutdown

Figure 17 shows the sequence of power up when a 24-V_{AC} system is plugged in. The battery was already connected and powering the 3V3 rail before 24 V_{AC} was plugged in. Upon the 24-V_{AC} plugin, the system begins charging the battery and takes over powering the system load. RectOut reaches steady state in approximately 300 ms from the initial 24-V_{AC} plugin. Variances in the 24-V_{AC} transformer will cause variances in the steady-state rise time as can be seen by comparing Figure 17, Figure 21 and Figure 23. The LM5166 rail (PWRIn) will however power up before steady state is reach as the LM5166 only requires greater than 5 V to be present. Note that the LM5166 rail is tested at node PWRIn, which is directly on the output of the ORing solution. The 3V3 rail exhibits no distinguishable transient response during the transition from battery power to 24-V_{AC} power. Figure 21 and Figure 23 provide startup tests to account for tolerances present in 24-V_{AC} transformers and show comparable results to Figure 17.

Immediate loss of 24-V_{AC} power is tested in Figure 18, Figure 22, and Figure 24. As is evident by the smooth nature of RectOut in these tests, the battery was fully charged and no significant load current was being supplied. Upon a 24-V_{AC} power loss, RectOut discharges most of the rectification caps energy in 1 second for a nominal 24 V_{AC}.

Figure 19 and Figure 20 show a 24-V_{AC} loss while a load on the 3V3 bus is demanding current. The rectification caps discharge considerably faster than no load conditions. The BMOut rail drops in voltage as the BM24072 parts transitions to battery power. The 3V3 rail exhibits no significant transient response to the loss of 24 V_{AC} and remains regulated and supplying to output load.

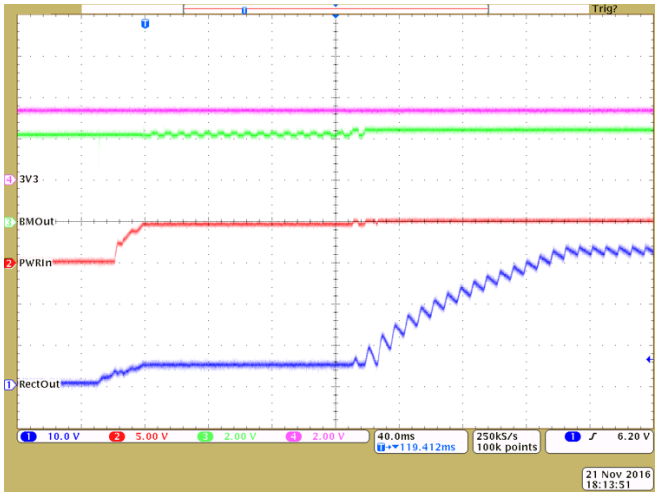


Figure 17. 24-V_{AC} Startup

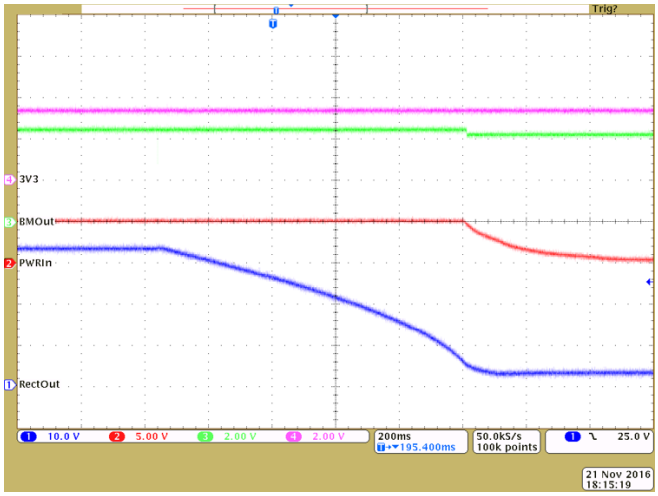


Figure 18. 24-V_{AC} Shutdown

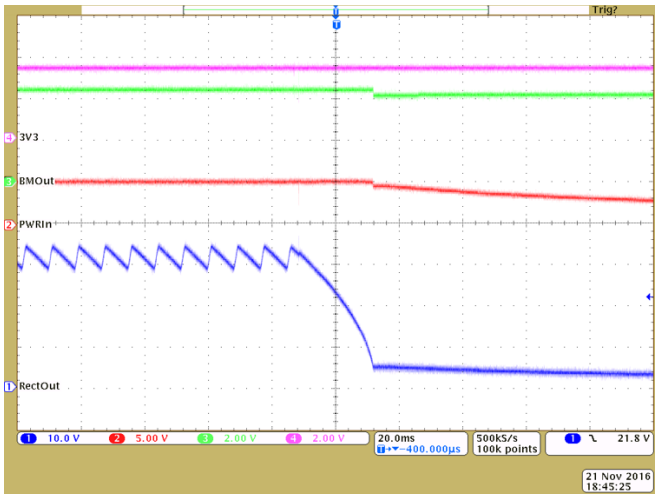


Figure 19. 24-V_{AC} Shutdown (3V3 Load = 200 mA)

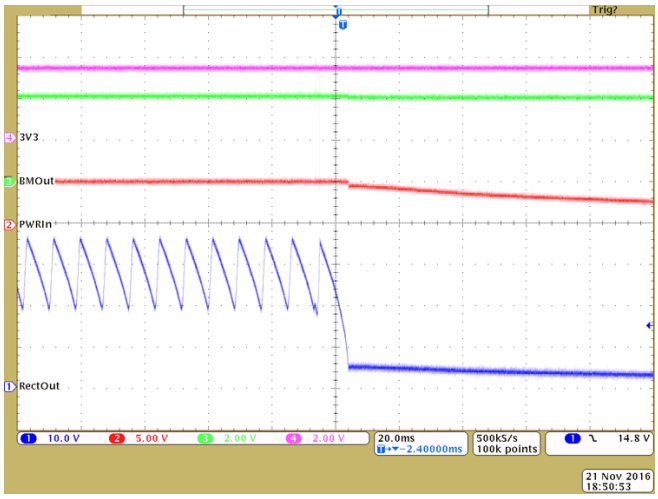


Figure 20. 24-V_{AC} Shutdown (3V3 Load = 750 mA)

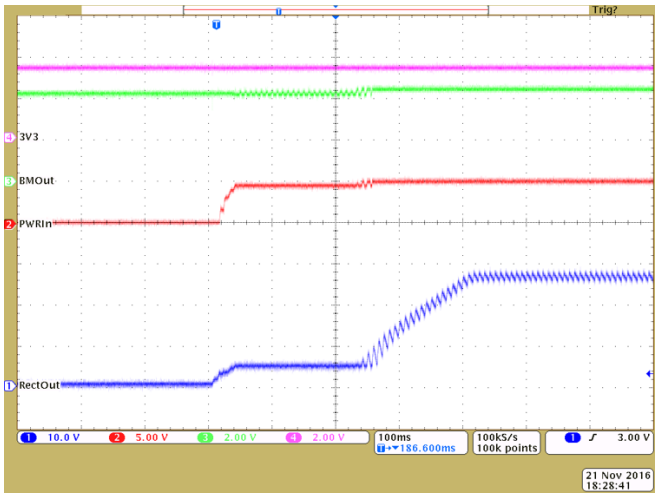


Figure 21. 20-V_{AC} Startup

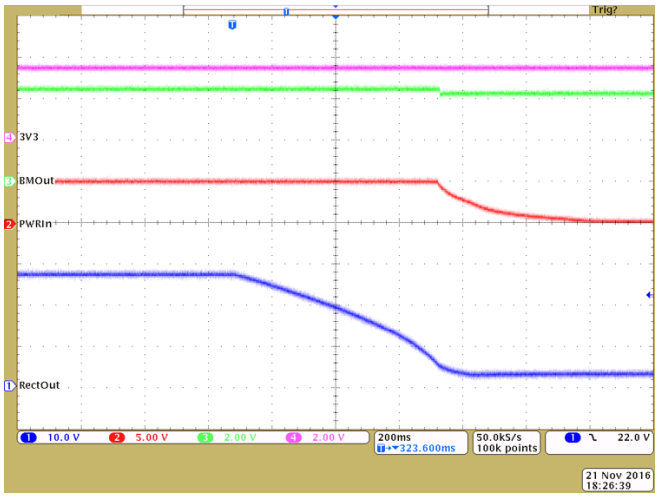


Figure 22. 20-V_{AC} Shutdown

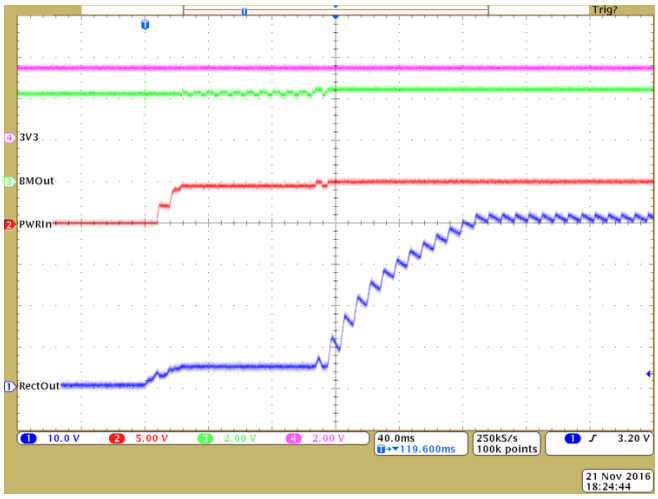


Figure 23. 30-V_{AC} Startup

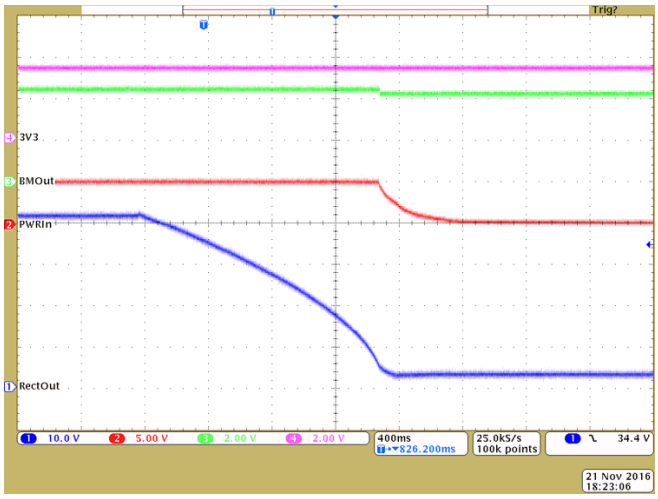


Figure 24. 30-V_{AC} Shutdown

4.1.2 USB Startup and Shutdown

Figure 25 shows a 5.1-V USB cable being plugged into the system (Note: A 3-ft USB A to USB micro-B cable was used for Figure 25 and Figure 26). The node USBin exhibits no overshoot, which is due, in part, to the snubber circuit detailed in Section 2.2.2. The PWRIn, which is the output of the ORing circuit, matches the response of the USBin. This test shows 1.85 ms passes before the battery management system regulates the output, BMOut, to 200 mV plus V_{BATT}. As with the 24-V_{AC} startup, the battery was previously supplying the load when the USB was plugged in. Upon USB plugin, the battery management will begin charging the battery with up to 300 mA. The 3V3 rail show no significant transient response to the change in power sources.

Figure 26 shows power transition back to the battery as the USB is unplugged. Approximately 100 ms passes before the USBIn rail diminishes towards zero. A slight drop at BMOut can bee seen as the system switches to battery power and thus V_{BATT}. The 3V3 rail remains very steady with no significant transient response during the transition.

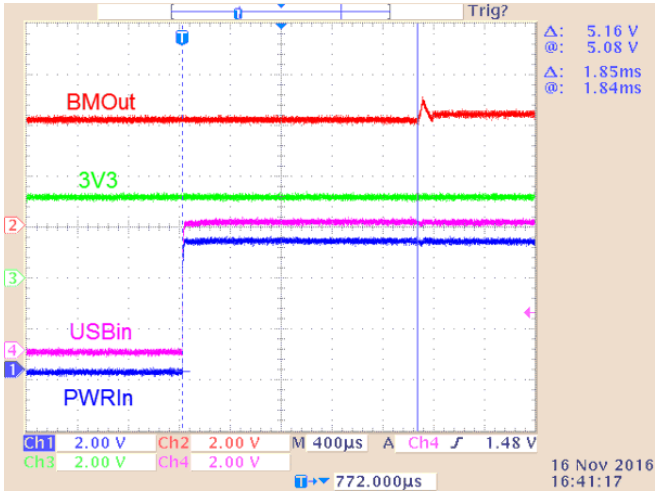


Figure 25. USB 5.1-V Startup

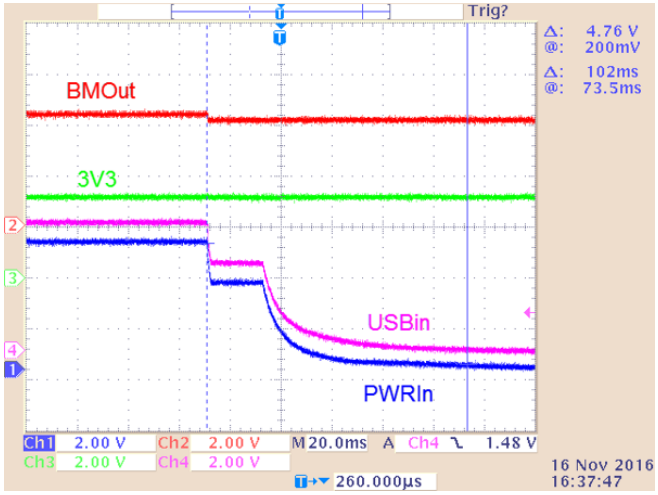


Figure 26. USB 5.1-V Shutdown

Figure 27 shows a startup variation with USBin at 4.35 V, the minimum allowed per USB 2.0 specifications. The actual tests for Figure 27 through Figure 28 were performed with banana to grabber cables. These cables are not isolated and exhibit significantly more parasitic inductance than a typical USB cable. Even so, a very minimal overshoot of 160 mV is observed. The high level voltage of the USB rail is reached approximately 2 µs after initial plugin. As observed in Figure 27, the delay time for the ORing circuit to pass the USBin to the PWRIn rail is approximately 1 µs. Figure 29 and Figure 30 show similar results.

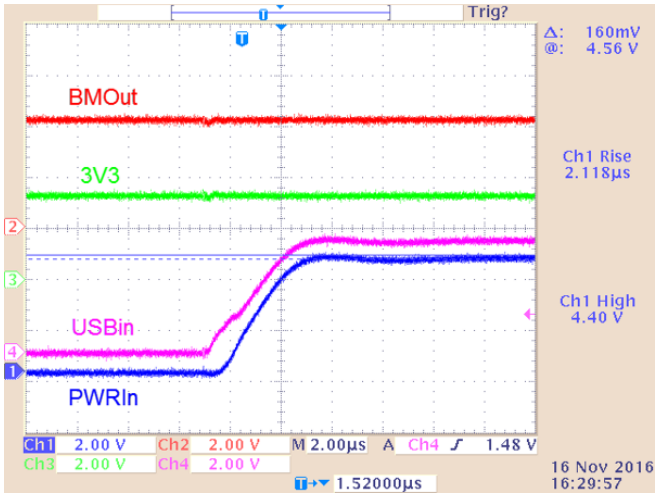


Figure 27. USB 4.35-V Startup

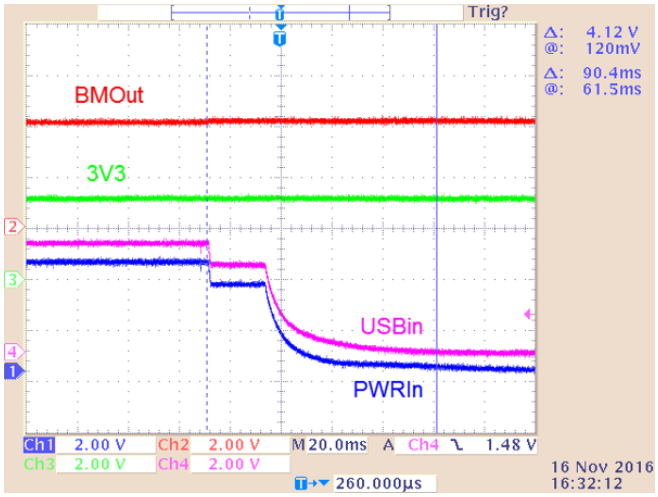


Figure 28. USB 4.35-V Shutdown

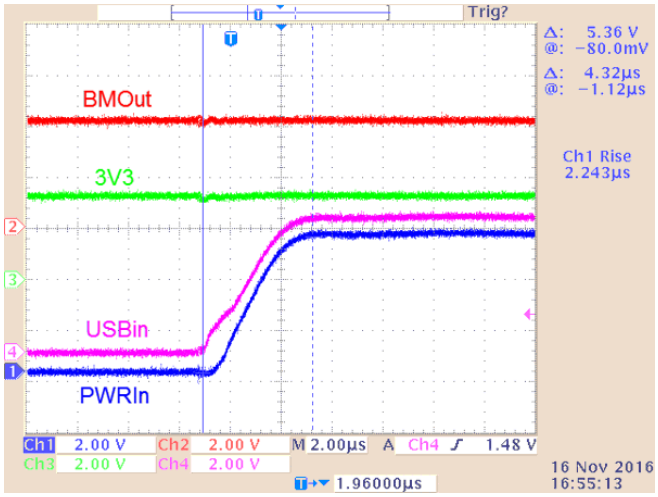


Figure 29. USB 5.25-V Startup

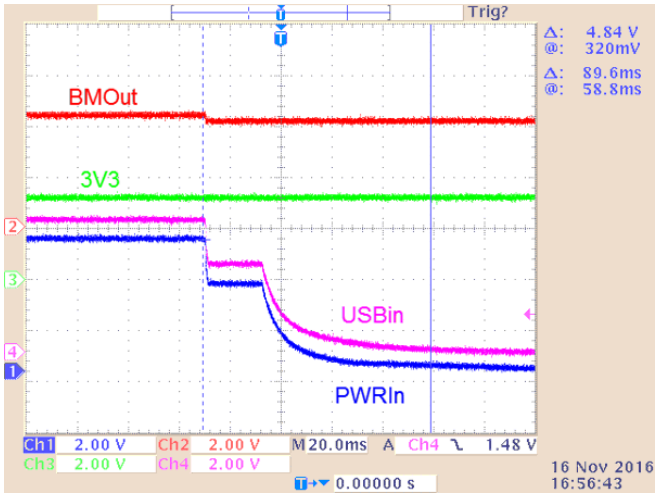


Figure 30. USB 5.25-V Shutdown

4.1.3 ORing

The ORing circuit as described in Section 2.3 is tested in this section. Figure 31 shows LMOut dominating USB upon plugin. Prior to LMOut powering up, USB is shown high and LMRC is high, forcing the USBin associated fets on and LMOut fets off. Once LMOut is powered up, the LMOnOff node begins to be pulled up, thus driving LMRC low, thereby turning the LM associated FETs on, and the USB associated FETs off. Figure 32 shows the opposite activity when LMOut shifts low. When the USB power is not present, the LM still passes through to output by pulling LMOnOff high as shown in Figure 33 and Figure 34.

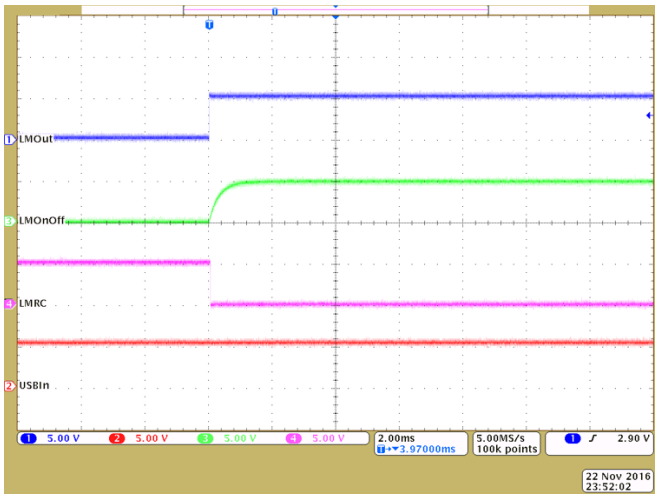


Figure 31. ORing Startup (LMOut Power Up; USB Source Present)

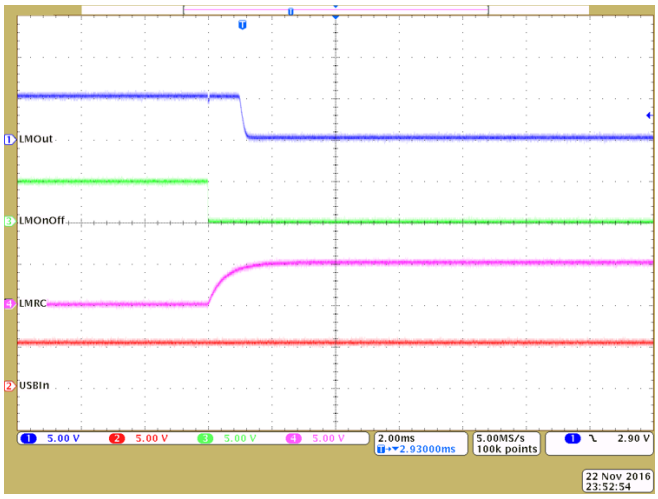


Figure 32. ORing Shutdown (LMOut Power Loss; USB Source Present)

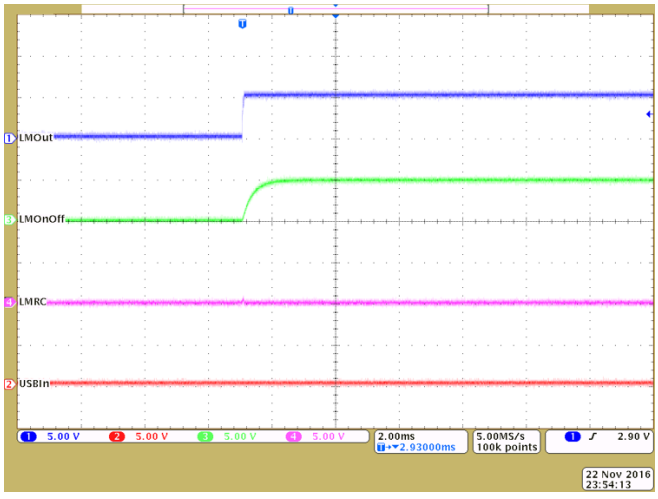


Figure 33. ORing Startup (LMOut Power Up; USB Source Absent)

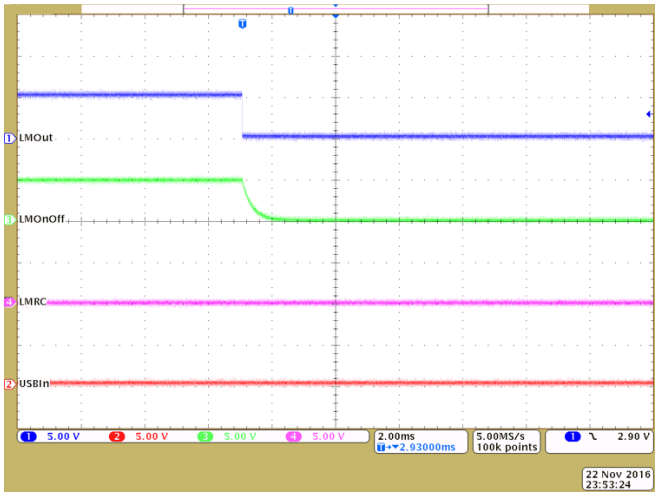


Figure 34. ORing Shutdown (LMOut Power Loss; USB Source Absent)

The ORing crossover test results summarized in Table 2 show the USB will never dominate the LMOut assuming the LMOut was available prior to USB plugin. If USB is available prior to LMOut startup, LMOut will dominate USB once the thresholds stated in Table 2 are met.

Table 2. ORing Transition Summary

PREVIOUS STATE	THRESHOLD REQUIREMENT FOR STATE CHANGE	NEW STATE	NOTES
LMOut = 5 V; LMOnOff high; LMRC low; PWRIn = 5 V (LMOut)	USBin exceeds 5.43 V or LMOut drops below 4.6 V	LMOut = 5 V; LMOnOff low; LMRC high; PWRIn = 5.43 V (USB)	This shows the transition from LMOut dominance to USB dominance. The USB requirement exceeds USB 2.0 specification and LMOut is regulated to 5.0 V through the LM5166; use case will not exist in system implementation.
USB = 5 V; LMOnOff low; LMRC high; PWRIn = 5 V (USB)	LMOut exceeds 5.03 V or USBin drops below 4.97 V	LMOut = 5.03 V; LMOnOff high; LMRC low; PWRIn = 5.03 V (LMOut)	When USB is present prior to LMOut power up, LMOut will dominate once it exceeds 5.03 V or USB drops below 4.97 V.

4.2 Load Transients

This section provides load transient data for each of the main DC power stages (LM5166, bq24072, and TLV62080). A summary of transient measurements for switching regulators are provide in Table 3.

Table 3. Load Transient Test Data Summary

DEVICE	NODE NAME	LOAD STEP (mA)	TRANSIENT AMPLITUDE (mV)	TRANSIENT PERCENTAGE	TEST DATA FIGURE
LM5166	LMOut	0 to 480	236.0	4.72%	Figure 35
		200 to 480	104.0	2.08%	Figure 36
TLV62080	3V3	250 to 750	34.5	1.05%	Figure 38
		0 to 1000	61.1	1.85%	Figure 39

4.2.1 LM5166

Figure 35 shows the transition of the LM5166 from DCM to CCM operating modes as is evident by the differing ripple frequencies during no load and 480 mA. A transition from DCM to CCM will cause the worst case transient response. The transient response while operating only in CCM is significantly smaller as seen in Figure 36. Figure 37 provides the load current rise and associated transient response on a small time scale to allow closer analysis.

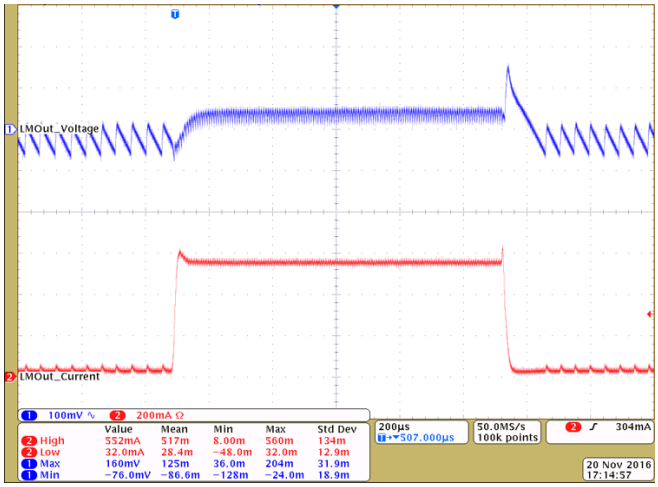


Figure 35. LM5166 Transient Response (0 to 480 mA)

Figure 36. LM5166 Transient Response (200 to 480 mA)

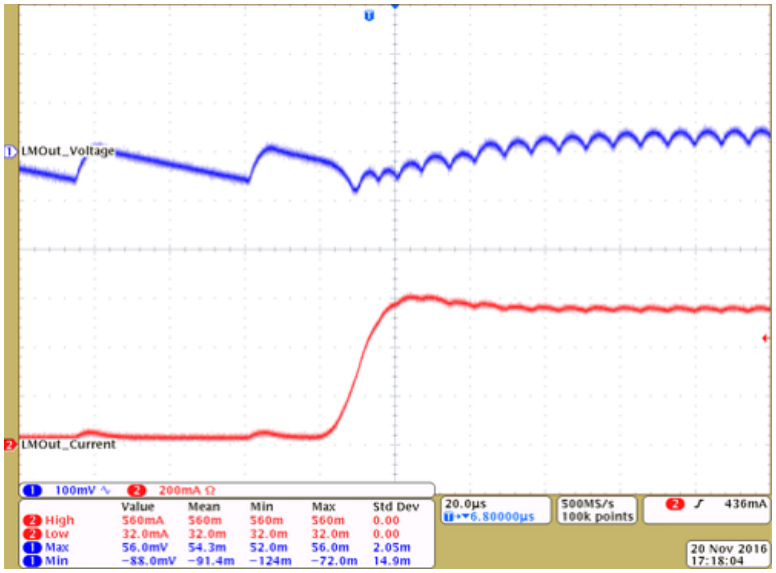


Figure 37. LM5166 Transient Response Slew

4.2.2 TLV62080 Transient Response

The 3V3 rail will be the primary power bus powering a system load and thus ripple and transient response on this rail must remain small. In this TI Design, the TLV62080 operates very well, with a transient response of less than 2% for a 0- to 1-A load step.

Figure 38. TLV61080 Transient Response (250 to 750 mA)

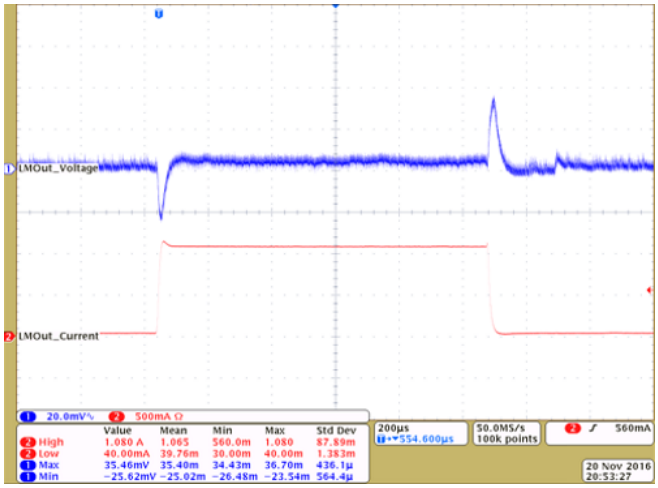


Figure 39. TLV62080 Transient Response (0 to 1 A)

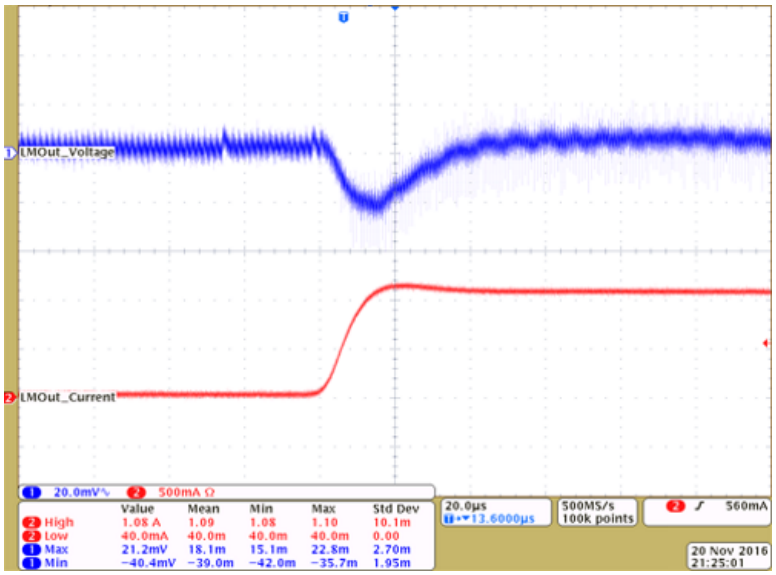


Figure 40. TLV62080 Transient Response Slew

4.2.3 BM24072 Transient Response

The battery management system transient response is more complicated than the LM5266 and TLV62080 as the BM24072 must pull current from two sources, the battery and the PWRin node, when load currents exceed 500 mA. Figure 41 shows a 250- to 750-mA load step on the BM24072 output. As the load current becomes too high for the PWRin node to supply, the battery management system drops in voltage as it uses the battery as power assistance. BMOut returns to the initial voltage once the output current steps back down and the battery is no longer required to provide additional current. Figure 42 shows the battery management power assist beginning when the load current crosses above 610 mA and ceasing when crossing below 480 mA. However, the BMOut voltage, which is dependant on the battery voltage, will change those crossover points. A lower BMOut voltage will raise the current crossover point at which battery power assistance is needed.

When the battery is the only source present, the transient response of the BM24072 exhibits only the voltage drop across the battery's power line as current is pulled as shown in Figure 43.

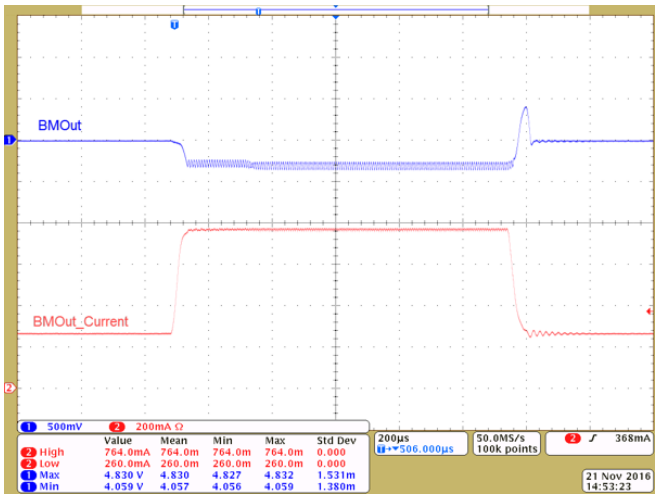


Figure 41. BM24072 Transient Response (250- to 750-mA; Battery and PWRin Source)

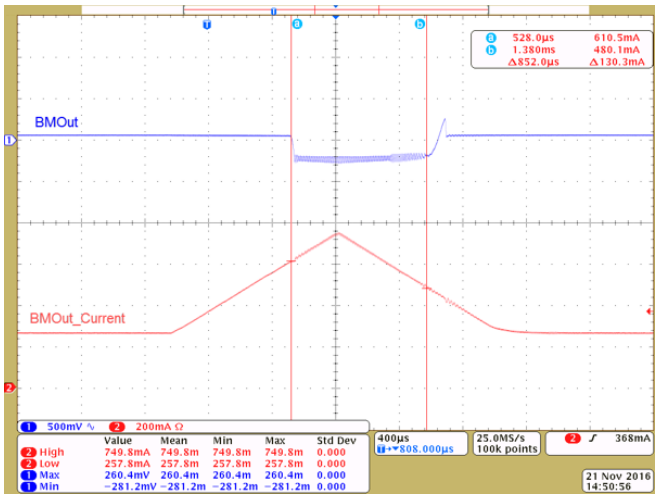


Figure 42. BMOut Transient Response (250- to 750-mA Slow Ramp; Battery and PWRin Source)

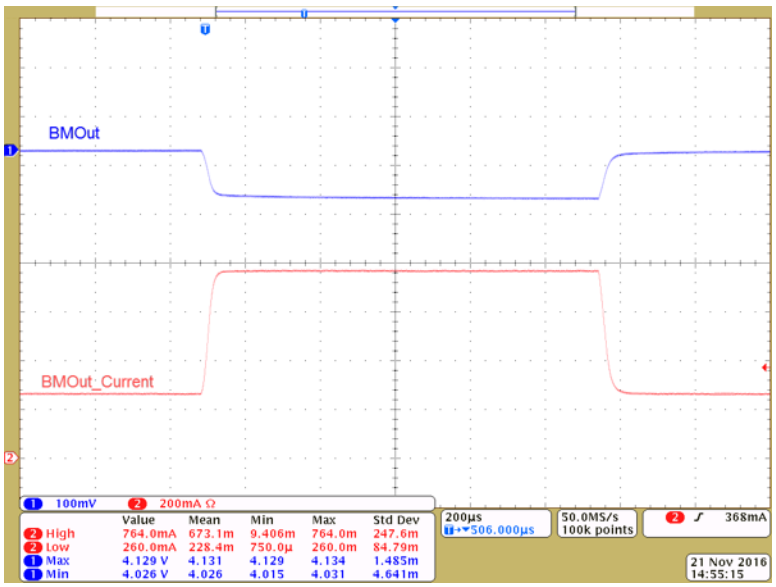


Figure 43. BM24702 Transient Response (250 to 750 mA; Battery Only)

4.3 Output Ripple

The output ripple is measured at full load and light load for all three DC stages (LM5166, bq24072, TLV62080). For the LM5166 and the TLV62080, additional measurements are taken to observe the difference in ripple during DCM and CCM operation.

Table 4. Output Ripple Test Summary

DEVICE	NODE NAME	LOAD	RIPPLE AMPLITUDE (mV)	RIPPLE PERCENTAGE	TEST DATA FIGURE
TLV62080	3V3	0 (DCM operation)	14.0	0.42%	Figure 44
	3V3	90 mA (DCM operation)	13.2	0.40%	Figure 45
	3V3	125 mA (CCM operation)	11.9	0.36%	Figure 46
	3V3	1 A (CCM operation)	23.9	0.72%	Figure 48
LM5166	LMOut	0 (DCM operation)	98.0	1.96%	Figure 51
	LMOut	130 mA (DCM operation)	100.0	2.00%	Figure 52
	LMOut	180 mA (CCM operation)	47.0	0.94%	Figure 53
	LMOut	490 mA (CCM operation)	45.4	0.91%	Figure 55
BM24072	BMOut	0 A	5.5	0.14% (V_{BMOut}=4.0V)	Figure 56
	BMOut	500 mA (Battery and USB source)	88.4	2.2% (V_{BMOut}=4.0V)	Figure 60
	BMOut	1 A (Battery Source)	6.1	0.15% (V_{BMOut}=4.0V)	Figure 57
	BMOut	1 A (Battery and USB source)	35.5	0.89% (V_{BMOut}=4.0V)	Figure 59

4.3.1 TLV62080 (3V3 Power Rail)

Perhaps the most important power rail to monitor the ripple and noise on is the TLV62080 3V3 as it will be powering the system load. In this TI Design, the TLV62080 exhibits very low amplitude ripple. At a 125-mA load test, shown in Figure 46, the 3V3 rail's ripple is equal or less than the noise floor of the oscilloscope used for testing. Figure 47 shows low jitter on the switch node when using only one source. When using two sources during high current loads as shown in Figure 49, the battery in addition to the PWRin source, the SW node will exhibit more jitter as the input voltage is constantly changing to balance battery and PWRin sources. Even while using dual sources and full load current the ripple of the 3V3 rail stays beneath 0.75%.

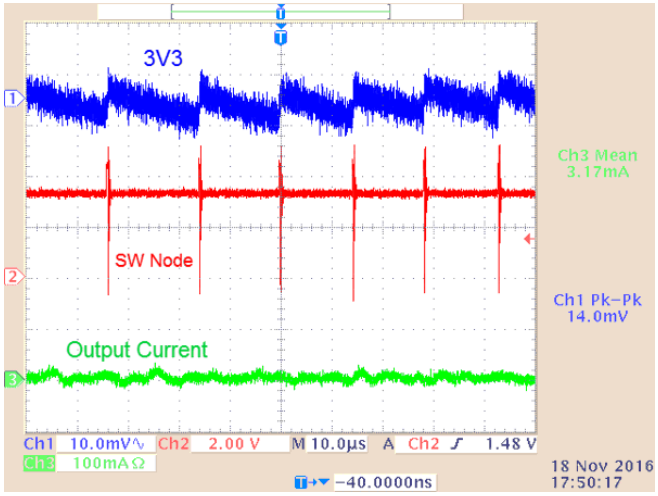


Figure 44. "3V3" Ripple (No Load; 24-V_{AC} Source)

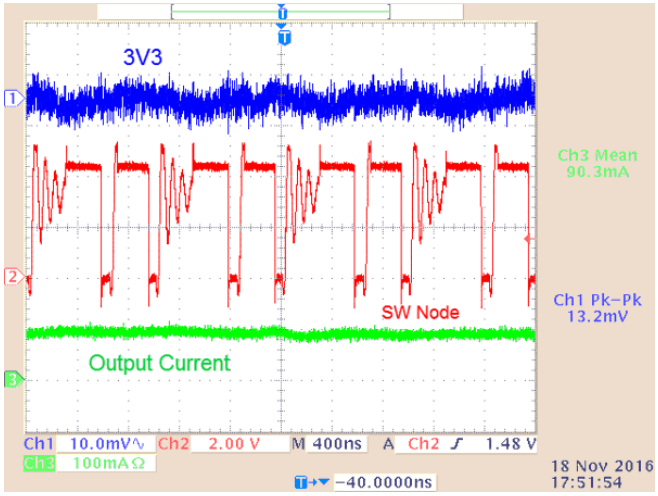


Figure 45. "3V3" Ripple (90-mA Load; 24-V_{AC} Source)

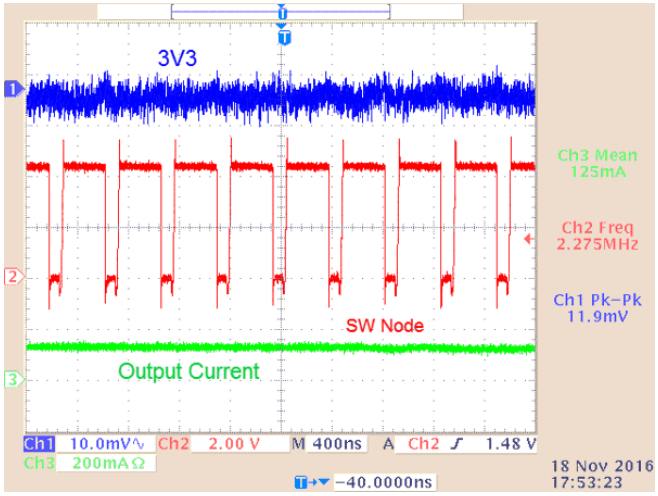


Figure 46. "3V3" Ripple (125-mA Load; 24-V_{AC} Source)

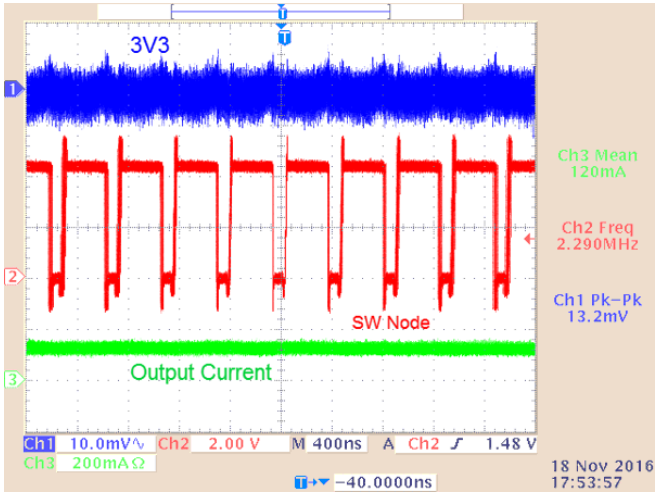


Figure 47. "3V3" Ripple Persist (120-mA Load; 24-V_{AC} Source)

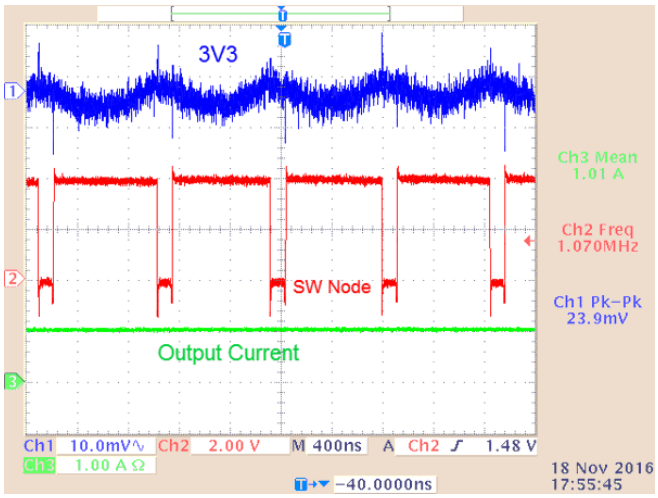


Figure 48. "3V3" Ripple (1-A Load; 24-V_{AC} Source Plus Battery)

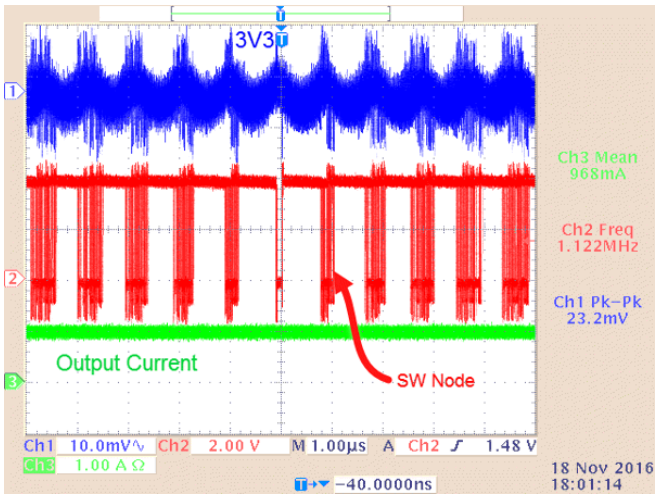


Figure 49. "3V3" Ripple Persist (1-A Load; 24-V_{AC} Source Plus Battery)

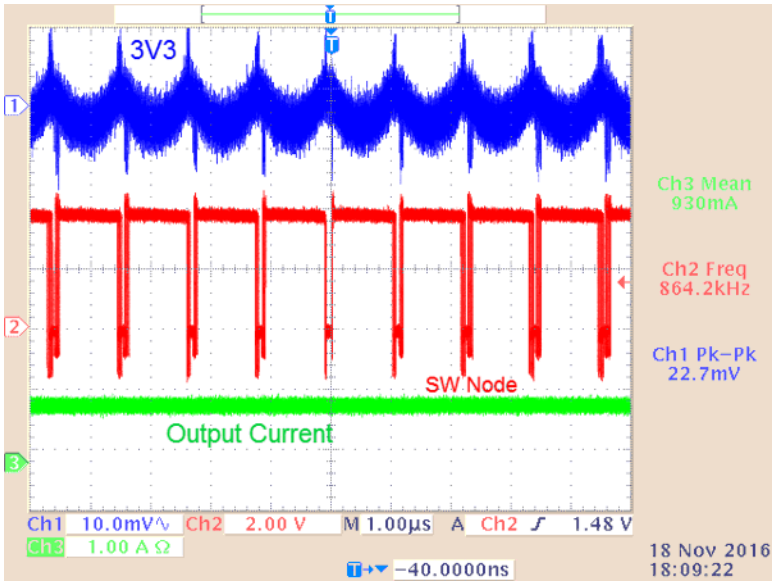


Figure 50. "3V3" Ripple Persist (1-A Load; Battery Powered Only)

4.3.2 LM5166 (LMOut Power Rail)

The LM5166 produces a larger ripple when operating in DCM when compared to CCM. Regardless of the mode, the LM5166 produces an output ripple of less than 3% across the entire load range. Jitter on the switch node as shown in Figure 54 is expected as the rectified 24 V_{AC} exhibits significant ripple that the LM5166 is constantly adjusting for. The amount of ripple exhibited on the rectified 24 V_{AC} increases with higher load currents thereby increasing jitter on the LM5166 switch node.

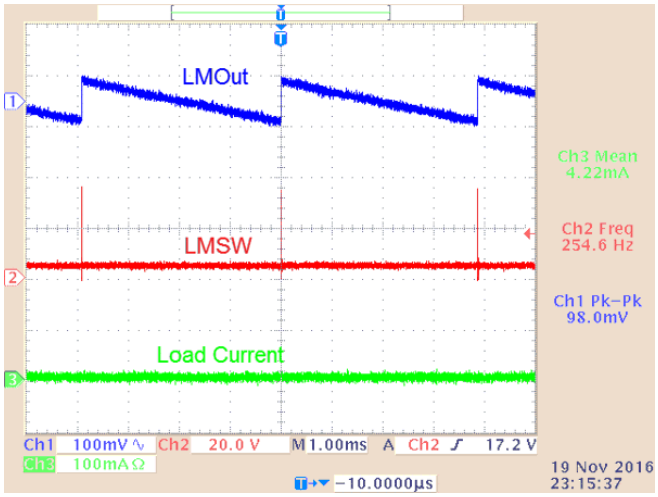


Figure 51. LMOut Ripple (No Load)

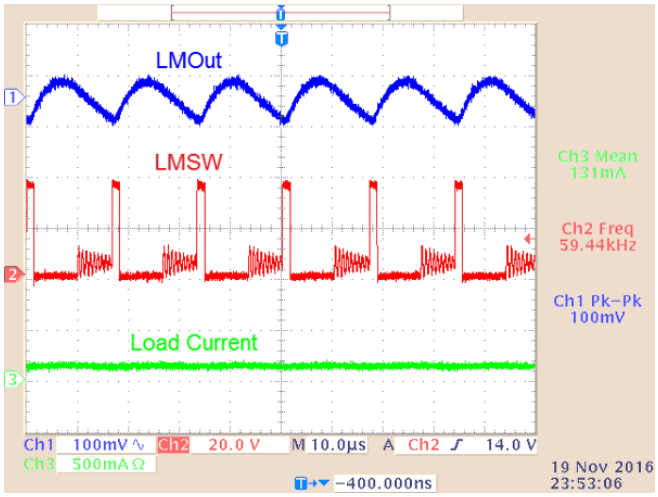


Figure 52. LMOut Ripple (130-mA Load)

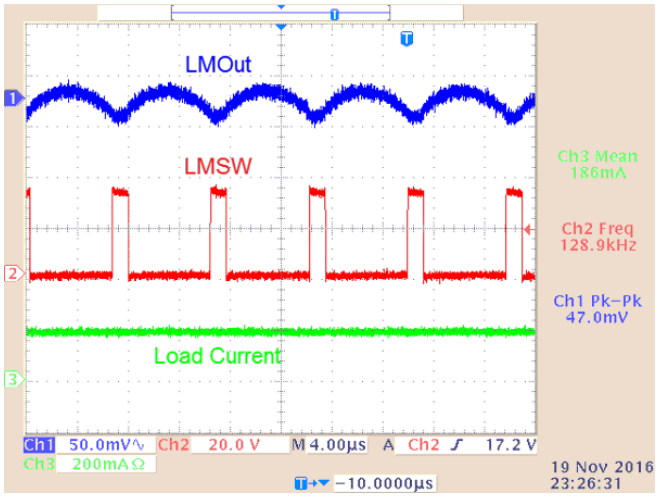


Figure 53. LMOut Ripple (180-mA Load)

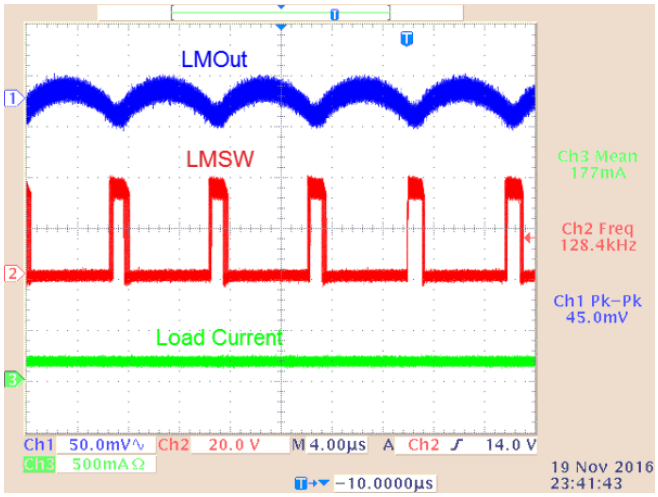


Figure 54. LMOut Ripple Persist (180-mA Load)

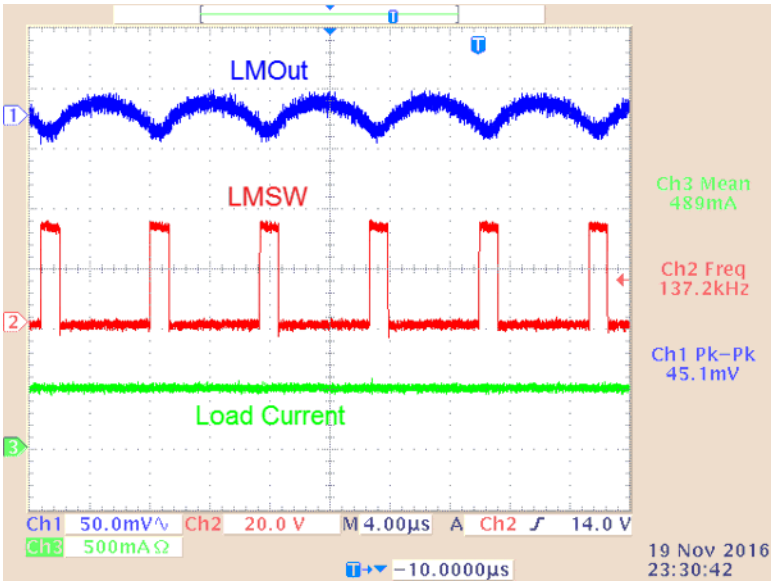


Figure 55. LMOut Ripple (490-mA Load)

4.3.3 BM24072 (BMOut Power Rail)

The ripple on the BMOut power rail varies significantly between battery usage only versus a PWRin source with battery power assist. When using only the battery, the BM24072 connects the battery to the output by closing an internal FET. As a result, the noise during purely battery operation is equal or less than the noise floor of the oscilloscope used for measurement. Figure 58, Figure 59, and Figure 60 show an increased ripple when using a source other than the battery.

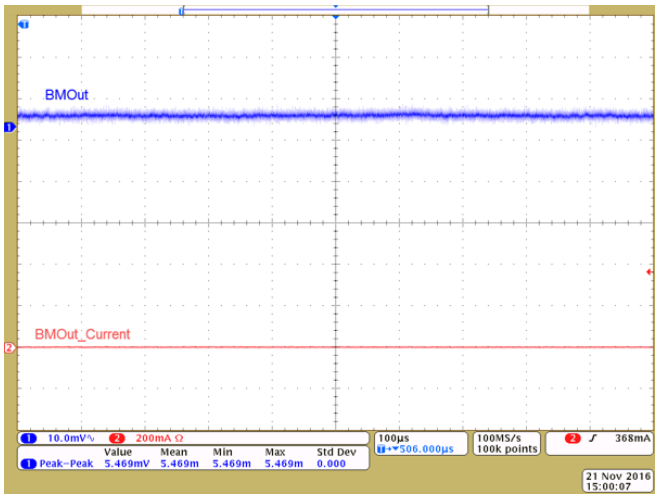


Figure 56. "BMOut" Ripple (0 A; Battery Source Only)

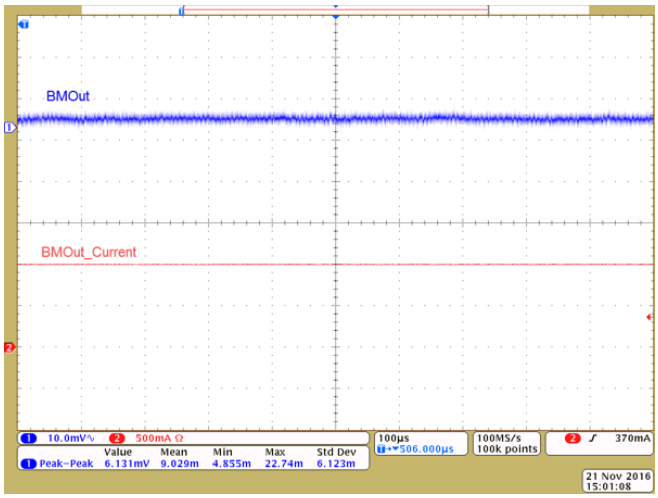


Figure 57. "BMOut" Ripple (1 A; Battery Source Only)

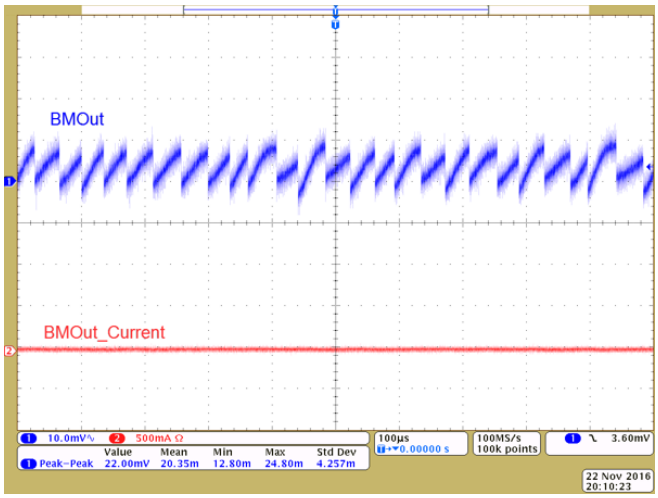


Figure 58. "BMOut" Ripple (1 mA; Battery and USB Sources)

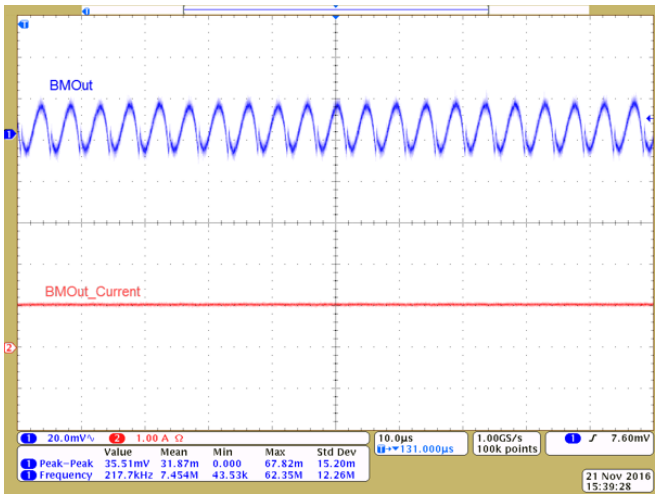


Figure 59. "BMOut" Ripple (1 A; Battery and USB Sources)

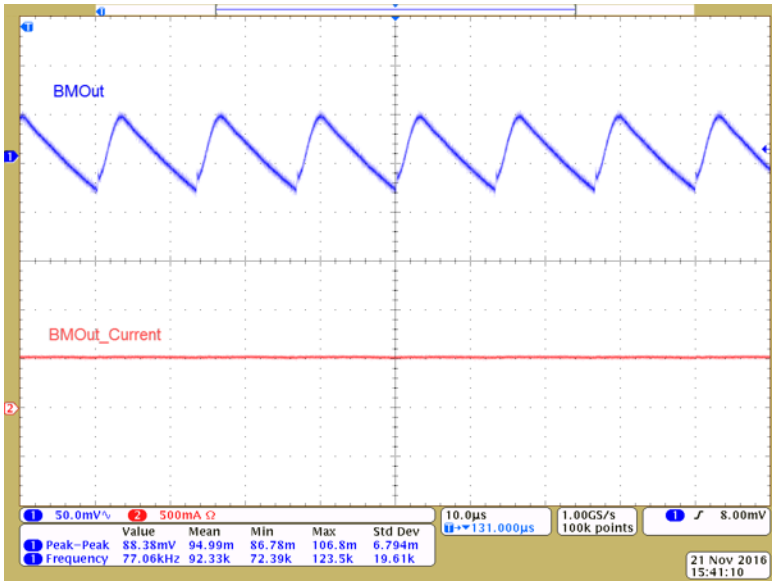


Figure 60. "BMOut" Ripple (500 mA; Battery and USB Sources)

4.4 Efficiency and Load Regulation

4.4.1 TLV62080

Efficiency on the BATT to 3V3 path is perhaps the most crucial as high efficiency on this path allows longer battery life and a smaller battery. The TLV62080 provides excellent efficiency, peaking at 96.6% efficiency at 165 mA at a nominal 3.7 battery voltage. The lower the battery voltage, the higher the efficiency of the BATT to 3V3 conversion. For this test, the input voltages were measured at C7 and the output voltages were measured at C10. The input current was fed at C7 and the output current to an electronic load was pulled from C10.

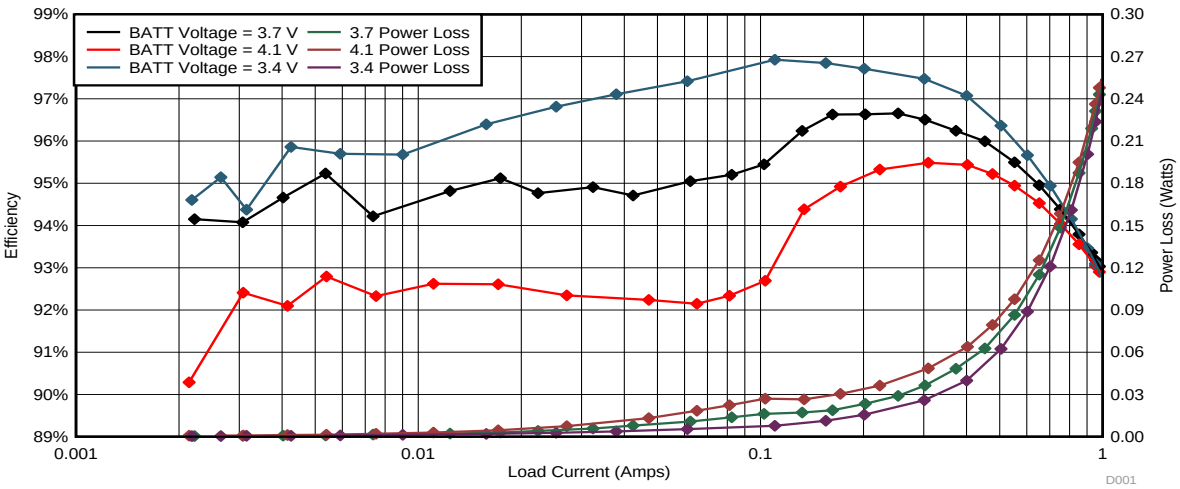


Figure 61. Battery to 3V3 Power Bus Efficiency and Power Loss

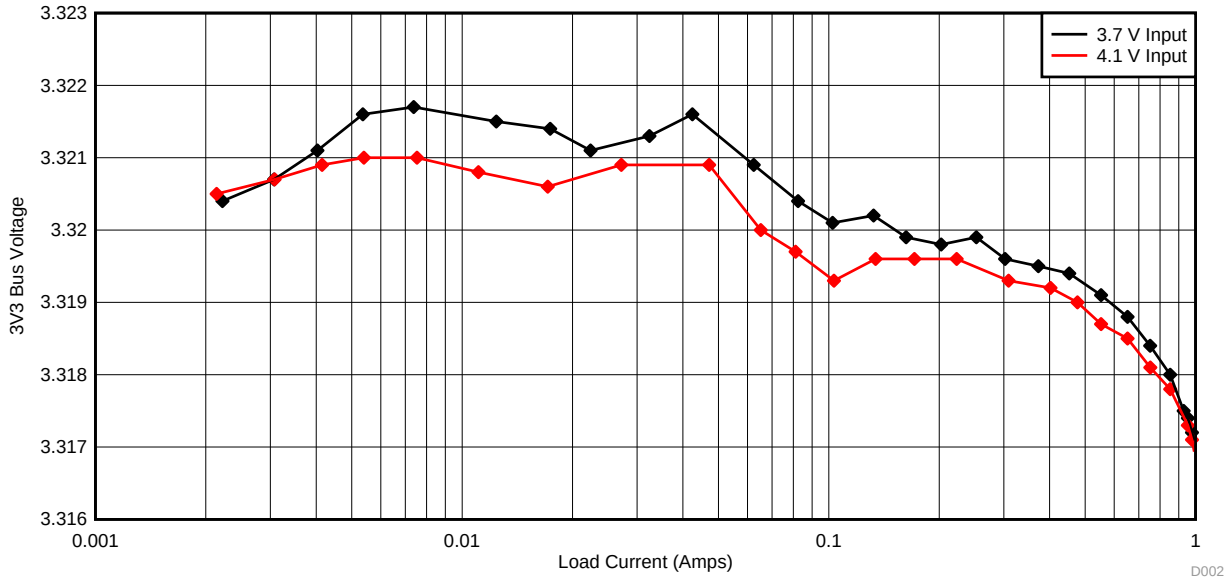


Figure 62. TLV62080 Load Regulation

4.4.2 LM5166

The LM5166 provides exceptional efficiency despite the large voltage difference between the input and output of the device. As with the BATT to 3V3 conversion, the efficiency of LM5166 increases as the input voltage decreases. The input voltage was measured at node RectOut side of R35 and the output voltage was measured at C23. The input current was fed through node RectOut and the output current was drawn from LMOut side of C23 and C24.

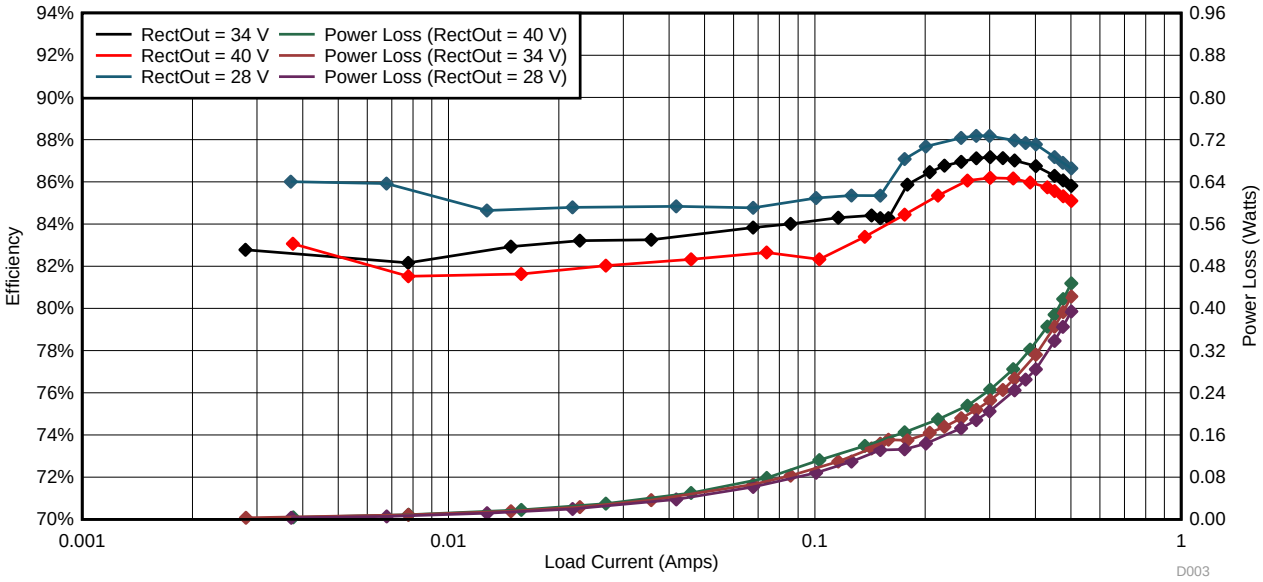


Figure 63. LM5166 Efficiency and Power Loss

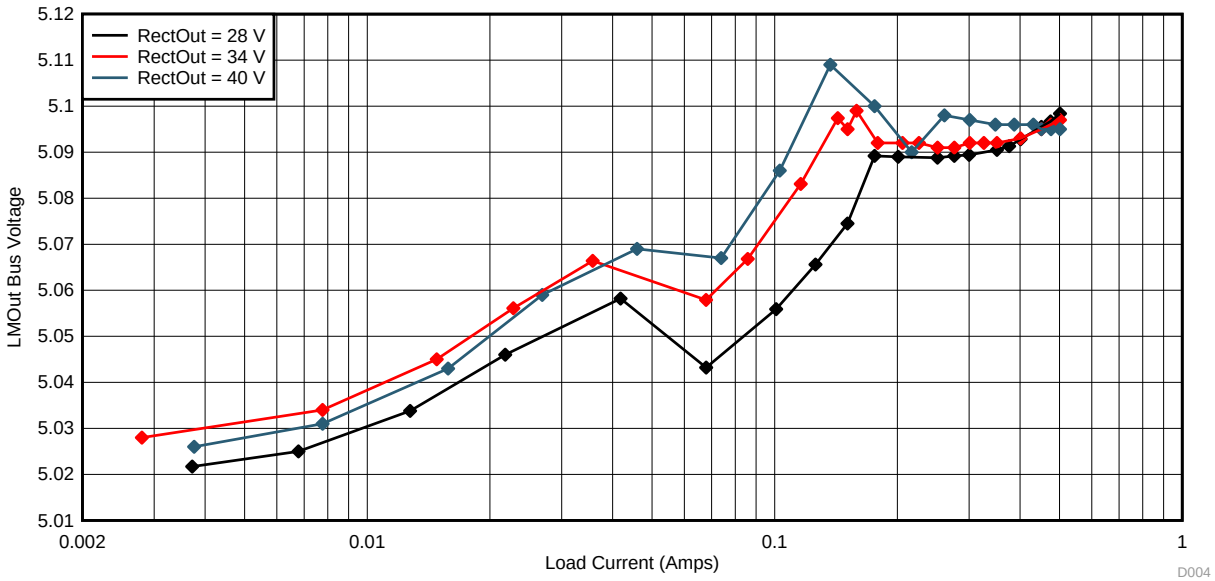


Figure 64. LM5166 Load Regulation

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01358.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01358.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01358.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01358.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01358.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01358.

6 Related Documentation

1. Texas Instruments, *Self-Powered AC Solid State Relay With MOSFETs Reference Design* , TIDA-00377 Design Guide (TIDUBR5)
2. Texas Instruments, *Low Cost AC Solid State Relay With MOSFETs Reference Design*, TIDA-01064 Design Guide (TIDUC87)
3. Texas Instruments, *Humidity and Temperature Sensor Node for Star Networks Enabling 10+ Year Coin Cell Battery Life*, TIDA-00374 Design Guide (TIDU797)
4. Texas Instruments, *Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs*, Application Note (SNVA166)
5. Texas Instruments, *LM5166 3-V to 65-V Input, 500-mA Synchronous Buck Converter with Ultra-Low IQ*, LM5166 Datasheet (SNVSA67)
6. Texas Instruments, *bq2407x 1.5-A USB-Friendly Li-Ion Battery Charger and Power-Path Management IC*, bq24072 Datasheet (SLUS810)
7. Texas Instruments, *TLV6208x 1.2-A and 2-A High-Efficiency Step-Down Converter in 2-mm × 2-mm WSON Package*, TLV62080 Datasheet (SLVSAK9)
8. Texas Instruments, *TPS27081A 1.2-V to 8-V, 3-A PFET High-Side Load Switch With Level Shift and Adjustable Slew Rate Control*, TPS27081A Datasheet (SLVSBE9)
9. Texas Instruments, *LMx93, LM2903 Dual Differential Comparators*, LM2903 Datasheet (SLCS005)
10. Texas Instruments, *TPD2E2U06 Dual-Channel High-Speed ESD Protection Device*, TPD2E2U06 Datasheet (SLLSEG9)
11. Texas Instruments, *TPD1E10B06 Single-Channel ESD Protection Diode in 0402 Package*, TPD1E10B06 Datasheet (SLLSEB1)

6.1 Trademarks

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7 About the Author

CASSIDY AARSTAD is a systems designer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Cassidy earned his master of science in electrical engineering (MSEE) from California Polytechnic State University in San Luis Obispo, California.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2016) to A Revision	Page
• Changed language and images to fit current style guide	1

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