TI Designs

48-V_{DC} Battery Powered Inverter Power Stage Reference Design for 5-kW Forklift AC Traction Motor

Description

This TI Design provides a reference solution for a three-phase MOSFET-based inverter to drive an AC induction motor for traction in forklifts. The inverter is powered from a 48-V_{DC} lead acid battery. It is designed to deliver 5 kW of output power from the motor and can handle continuous motor currents of up to 130 A_{RMS} with a suitable cooling setup. Its high current rating is achieved by using multiple MOSFETs (CSD19536) in parallel, mounted onto a thermal clad PCB. A 120-V half-bridge MOSFET gate driver with 4 A_{PK} source/sink current is used to control the MOSFETs. This TI Design incorporates techniques and measures to operate MOSFET in parallel.

Resources

TIDA-00364	Design Folder
CSD19536KTT	Product Folder
UCC27211	Product Folder
LAUNCHXL-F28069M	Tool Folder

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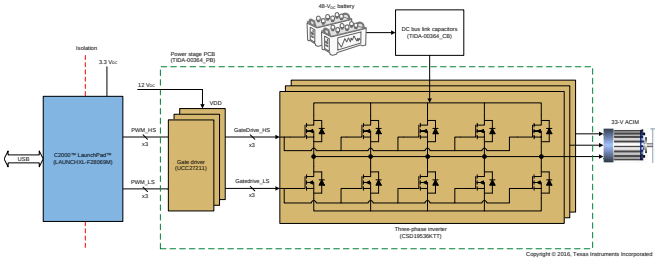
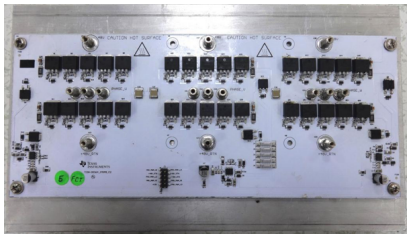
Features

- Operates From 48-V_{DC} Lead Acid Battery System
- Continuous Output Current up to 130 A_{RMS}
- Uses Five NexFET™ (CSD19536) in Parallel Having High Figure of Merit
- Half-Bridge Gate Driver (UCC27211) With 4 A_{PK} Source and Sink Capability
- Robust Gate Driver Withstanding –18 V for 100 ns at Switch Node
- Validated With Switching Frequencies up to 10 kHz
- Inverter Efficiency > 96 %
- Operating Temperature From –20°C to 55°C
- Use of Surface Mount MOSFET Package (D2PAK) Leads to:
  - Better Layout
  - Use of Insulated Metal Substrate (IMS) PCB for Better Cooling
  - Eliminates Need for Heatsink Clips, Screws, and Need for Manual Assembly Leading to Reduced Manufacturing Time and Cost
- Use of IMS PCB:
  - Increases Reliability of Inverter by Avoiding Hotspots at FET Junctions
  - Enables Using Forklift Chassis as Heatsink

Applications

- Forklift Traction Motor Drive
- Golf Cart Traction Motor Drive
- Tow Trucks





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1 System Overview

1.1 System Description

A forklift is an industrial truck used to move heavy loads over short distances. A typical electric forklift has three motors: a traction motor, a steering motor, and a hydraulic pump motor as shown in Figure 1. The traction motor and steering motor are used to maneuver the forklift, and the hydraulic pump motor provides the lifting power. Forklifts are typically operated by combustion engines or electric motors depending on the load carrying capacity and application area of the forklift. Outdoor applications that need lifting power beyond 2 tons typically use combustion engines. Electric forklift models are more suitable for moderate lifting power and indoor use because of its lower noise and zero emissions. Electric forklifts are typically powered from large, heavy lead-acid batteries, which also act as part of the overall counterweight to the load to be picked up. The typical battery voltages are 24, 36, and 48 V_{DC}, and the traction inverters are rated up to 8 kW. This necessitates using multiple MOSFETs in parallel to achieve the required current and power rating. This three-phase inverter design shows how to parallel TI MOSFETs and design the gate drive, and it demonstrates the performance of driving the 5-kW/33-V_{RMS} AC induction motor used for traction in forklifts.

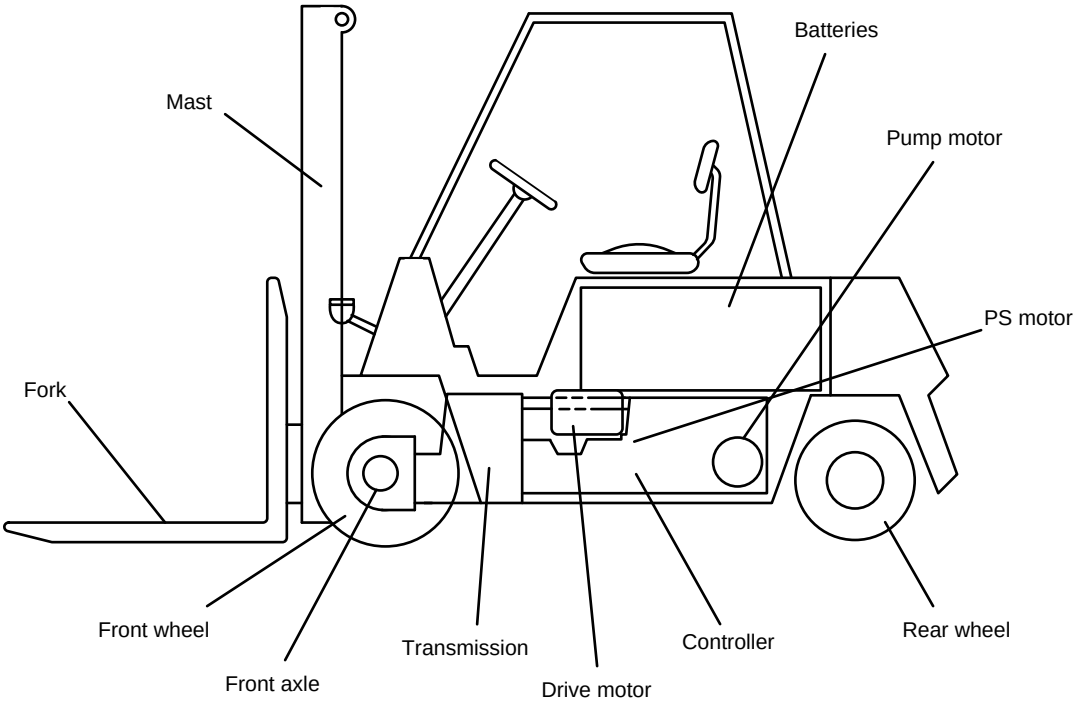

Figure 1. Forklift System

The traction motor used can be either a DC motor or an AC induction motor (ACIM). Traditionally, DC motors were used for traction drives, but recent advances in microcontroller technology have made them faster and powerful, resulting in easier implementation of AC motor control algorithms. Current forklift models use ACIM for their inherent advantages such as:

- Eliminates the need for brushes required to commutate a DC motor. This results in higher efficiency by eliminating the losses due to commutation. The maintenance costs are reduced as the brushes that need frequent replacements are no longer required.
- Superior power and torque performance
- More power per unit volume leading to compact motor size

The share of ACIM drives over their DC counterparts for forklift traction is steadily increasing. Using an AC motor requires an inverter power stage to convert DC voltage from the battery to a variable frequency voltage. This TI Design implements an AC traction motor controller powered by a 48-V_{DC} battery with a continuous output drive current rating of 130 A_{RMS}. The design uses the CSD19536 NexFET™ along with the UCC27211 half-bridge gate driver to implement the inverter drive. The LAUNCHXL-F28069M (microcontroller LaunchPad™) board is used to control the inverter.

Forklifts powered from low-voltage batteries result in high output current to the motor from the inverter stage. MOSFET paralleling is done to share the output current, which helps maintain the junction temperature within operating limits without using very large cooling systems. The advantages of MOSFET paralleling is described in Section 2.2.2. The inverter stage is built with SMD MOSFETs for ease of paralleling and increased robustness in the vibrating environment. Using SMD FETs require PCB backside cooling. This cooling mechanism can be made more effective by using insulated metal substrate (IMS) PCBs, which help transfer the heat generated from the MOSFETs through the PCB into the chassis of the forklift. The benefits of using an IMS PCB for this application is described in Section 2.3.

This TI Design offers the following key benefits:

- High-efficiency inverter stage due to low R_{DSon} of the CSD19536KTT NexFET. Paralleling NexFETs further reduce the effective R_{DSon}.
- Excellent figure of merit (R_{DSon} × Q_G) of the NexFET such that resistance is not lowered at the expense of excessive gate charge. This reduces the gate power required for achieving lower ON resistance.
- Excellent thermal capability due to the IMS PCB

Various parameters of the design like inverter losses, inverter drain-to-source waveforms, gate drive waveforms, and inverter phase current waveforms are tested and documented.

1.2 Key System Specifications

Table 1. Key System Specifications

SUB-SECTION	PARAMETER	SPECIFICATIONS			
		MIN	TYP	MAX	UNIT
Inverter	Input battery voltage	42	48	56	V_{dc}
	Continuous output current			130	A_{rms}
	Output frequency		50		Hz
	Efficiency	95			% at 130A_{rms}
	Switching frequency		8		kHz
Gate driver	Drive source capacity			4	A_{pk}
	Drive sink capacity with external PNP booster circuit			15	A_{pk}
	VDD		12		V_{dc}
Interface	Input signals	Six PWM signals			
Operating conditions	Operating temperature	–20		55	°C
Protection	Undervoltage lockout for half-bridge gate driver				

1.3 Block Diagram

The TIDA-00364 consists of two boards: an inverter board (TIDA-00364_PB) and a DC link capacitor board (TIDA-00364_CB) connected together as shown in Figure 2. In the forklift, the inverter can be placed at some distance away from the battery source and connected together with long wires. This necessitates the use of the DC link capacitor board, which is mounted closely on top of the power board. This board supplies the ripple current for the inverter instead of the battery. The outcome is reduced heating and extended lifetime of the battery.

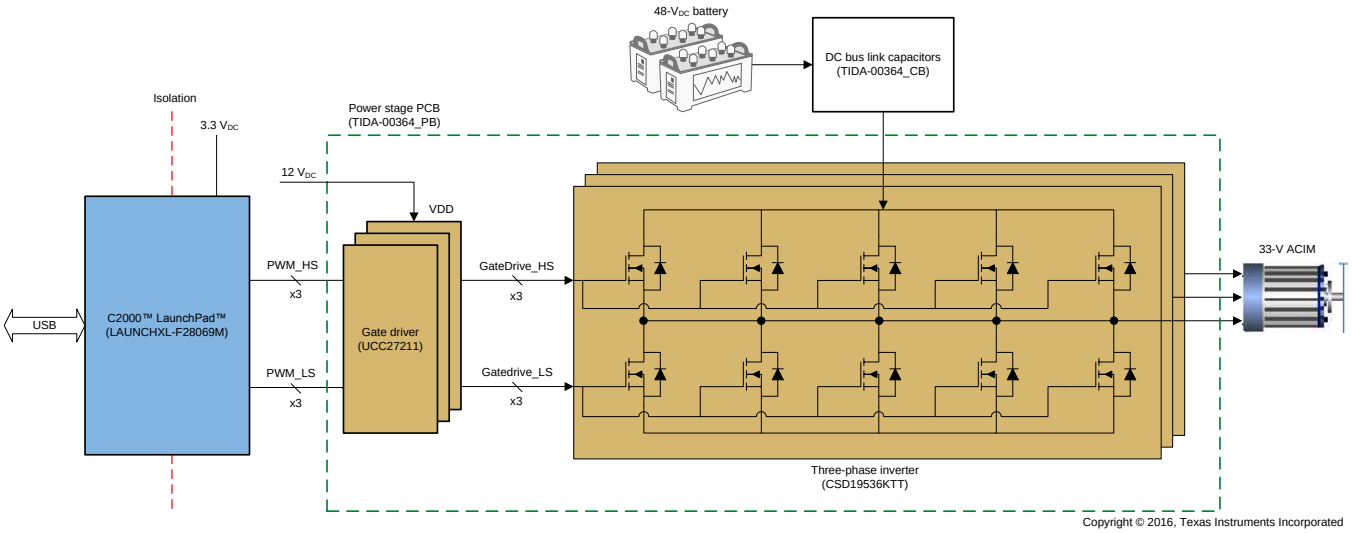

Figure 2. Block Diagram

The TIDA-00364 power board (TIDA-00364_PB) consists of two main sections: the gate driver section and the inverter section.

The gate driver section uses the UCC27211, which is a half-bridge gate driver with a 4-A_{PK} source and sink capability. The low-side driver is powered from an external 12-V_{DC} power supply. The high-side driver is powered from a floating power supply, which is generated using a bootstrap circuit. The switch node (HS pin) of the UCC27211 can handle –18 V maximum for 100 ns, which allows the high-side channel to be protected from inherent negative voltages caused by parasitic inductance and stray capacitance of the traces. The inputs to the UCC27211 are TTL compatible signals.

The inverter section uses five CSD19536KTT in parallel for the high-side and low-side switches in each phase. This helps share the output current resulting in reduced losses. The power dissipated in the MOSFET is also shared equally between the five FETs, improving the thermal performance of the inverter.

The input signals to the power board are the six PWM signals generated by the C2000™ controller for controlling the three-phase inverter. The controller board used in this design is the LAUNCHXL-F28069M. A 3.3-V_{DC} supply has to be provided externally to power the LaunchPad. The LaunchPad provides isolated USB communication to the PC for debugging and motor control functions. Open loop V/f control algorithm is implemented to drive the motor and load the inverter stage.

The motor used in this design is a three-phase low voltage AC induction motor. The nameplate information is listed in Table 2.

Table 2. Motor Nameplate Information

PARAMETER	VALUE
Model	HPQ5-48-18N
Rated power	5 kW
Rated speed	3000 rpm
Maximum speed	6800 rpm
Rated phase-to-phase voltage	33 V_{RMS}
Rated phase current	130 A_{RMS}
Rated frequency	102 Hz
Number of magnetic poles	4
Rated torque	16 Nm
Insulation class	H
Duty	S2-60 min
Ambient	40°C

1.4 Highlighted Products

The TIDA-00364 reference design features the following devices from Texas Instruments.

1.4.1 CSD19536KTT

The device is a 100-V N-channel surface mount NexFET with a continuous package limited drain current rating of 200 A. The R_{DSon} of the device is 2 mΩ; this parameter is very important for this TI Design because of the large output current rating of the inverter helping reduce conduction losses and improve efficiency. Low Q_g of 118 nC makes sure that low R_{DSon} is not achieved at the cost of excessive gate charge. The D2PAK plastic package has a low thermal resistance of 0.4°C/W, which helps in effective PCB backside cooling.

1.4.2 UCC27211

The device is a half-bridge gate driver with a bootstrap power supply for the high-side switch. It has a 4-A_{PK} source and sink capability, TTL compatible inputs, an up to 20-V power supply input range, and operating temperature range of –40°C to 140°C.

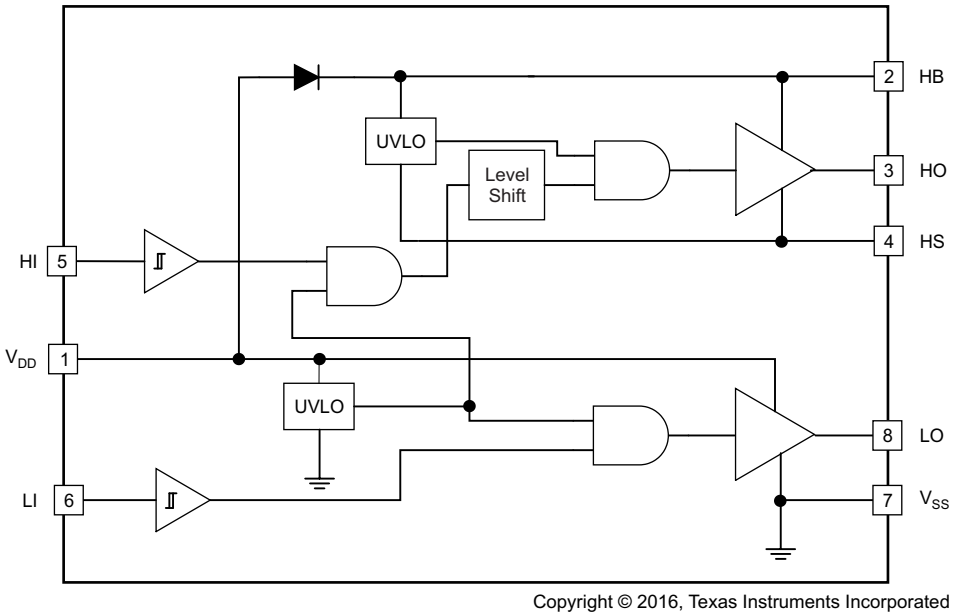

Figure 3. UCC27211 Functional Block Diagram

The features of the device with benefits to the design are listed in Table 3

Table 3. UCC27211 Features and Benefits

FEATURE	BENEFIT
Switch node (HS pin) able to handle –18 V maximum for 100 ns	Allows the high-side channel to have extra protection from inherent negative voltages caused parasitic inductance and stray capacitance
Robust ESD circuitry to handle voltage spikes	Excellent immunity to large dV/dt conditions
18-ns propagation delay with 7.2-ns / 5.5-ns rise/fall times	Best-in-class switching characteristics and extremely low-pulse transmission distortion
Symmetrical UVLO circuit	Ensures high-side and low-side shut down at the same time
TTL optimized thresholds with increased hysteresis	Increased hysteresis offers added noise immunity, which is important because of the large amounts of current the inverter switches generating noise

For more information on each of these devices, see their respective product folders at www.TI.com or click on the links for the product folders on the first page of this reference design under Resources.

2 System Design Theory

2.1 Gate Driver Subcircuit

The gate driver selected for this design is the UCC27211. The gate driver performs the function of level shifting (3.3 to 12 V) and buffering the PWM output of the microcontroller to the MOSFET gate. Three half-bridge gate drivers are used to control the three-phase inverter. The gate circuit for the low-side switch for phase U is described in this section. The subcircuit is shown in Figure 4. The gate drive components placed close to the MOSFETs are shown in Figure 5

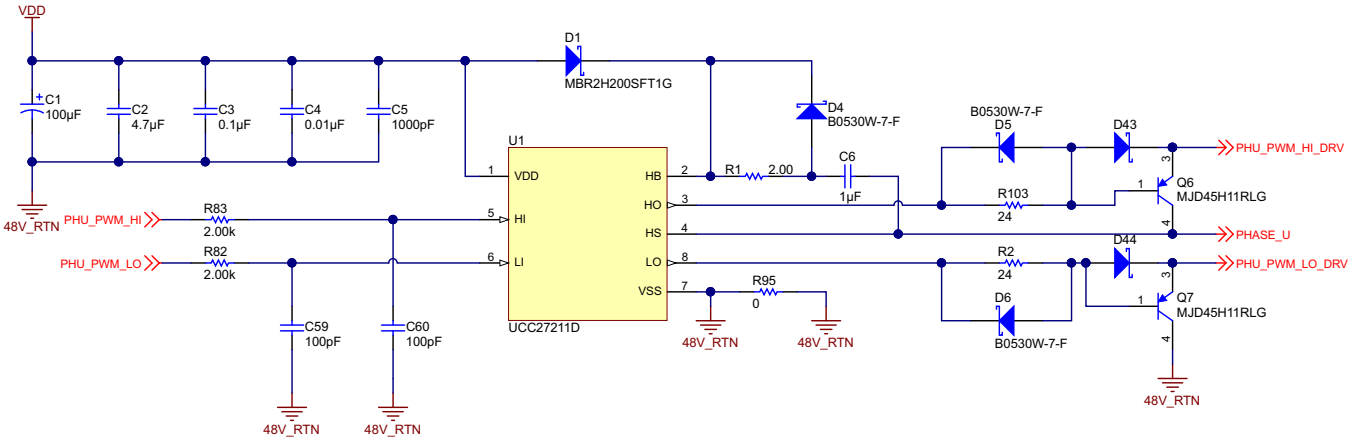

Figure 4. Half-Bridge Gate Driver Subcircuit

The gate driver is powered from an external power source (VDD = 12 V). C1 is the bulk capacitor placed close to the gate driver and helps prevent droop on the 12 V_{DC} rail during load transients. C2 through C5 are high-frequency decoupling capacitors that provide the fast rising current edges required by the gate driver output stages. This prevents high-frequency current edges from flowing through the long tracks from the power supply input helping reduce noise on the 12-V_{DC} rail

The gate drive inputs LI and HI are driven from the PWM output pins of LAUNCHXL-F28069M, which is connected to the power board through ribbon cable. RC filters are placed close to the gate driver inputs to prevent false triggering of the gate driver due to noise. It also helps prevent overshoot and undershoot on the input signals due to the parasitic track or cable inductance from the controller to the gate inputs.

A floating power supply is required to drive the high-side MOSFETs. This floating power supply is generated by the gate driver with a bootstrap circuit. D1, R1, and C6 are the main components of the bootstrap circuit. When the Phase U switch node toggles to 0 V, VDD charges the capacitor C6 to 12 V minus the diode forward voltage drop through D1 and R1. R1 is used to limit the inrush current into C6. When Phase U switches to the DC bus voltage, diode D1 gets reverse biased and the charge stored in C6 is used to drive the high-side MOSFETs. D4 is used to bypass the resistor R1 while driving the high-side MOSFETs.

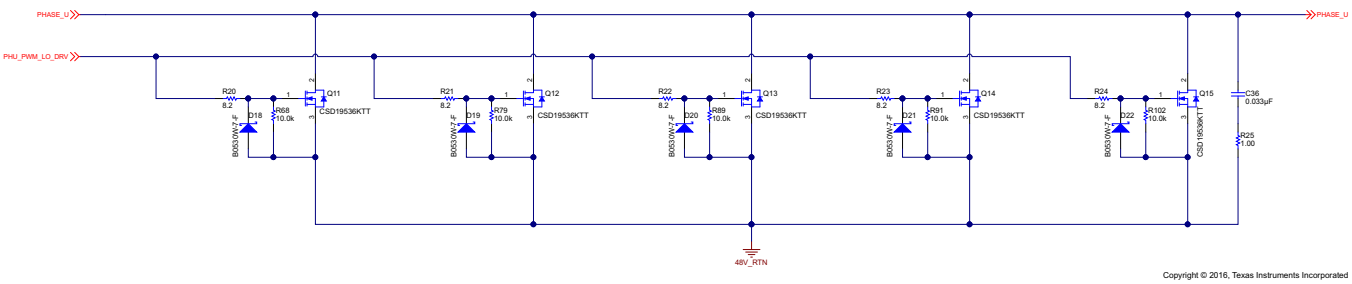

Figure 5. Gate Drive Components Close to MOSFET

The turnon and turnoff times of the MOSFETs are independently controlled. A slow turnon is used to minimize overshoot and ringing on the phase output due to unavoidable circuit layout parasitics. The turnon gate current path is through resistor R2 and diode D44, and then splits into the individual gate resistors (R20 through R24) placed close to each of the parallel MOSFETs as shown in Figure 5. If the same path is used for the turnoff gate current, the turnoff time will also be very slow. A large dead time will be required to prevent current shoot-through in the half-bridge. A gate turnoff speed enhancement circuit is added to accelerate the gate discharge time of the MOSFETs. The speed enhancement circuit provides two benefits:

- It provides a sink current capability that is greater than what is provided by the gate driver alone.
- It can be placed close to the parallel MOSFET section, which helps reduce the turnoff current loop. This makes the turnoff circuit more effective against suppressing Miller capacitance induced false turnon.

The speed enhancement circuit comprises of Q7 and D6. The turnoff gate current of each MOSFET passes through the individual gate resistors (R20 through R24) and then combines into the BJT Q7. D6 is added to bypass R2 and provide sufficient base current for the BJT Q7 for rapidly turning it on. The V_{BEmax} of Q7 is 5 V. D44 helps clamp the V_{BE} of Q7 to ≈ 0.4 V when it is in the off state. Schottky diodes D18 through D22 are placed in parallel to corresponding MOSFET gate to source terminals. These diodes help clamp the gate voltage to ≈ –0.4 V helping suppress negative gate ringing.

Note the use of split gate resistors R2, which is common to all the parallel MOSFETs, and R20 through R24, which are individual to each MOSFET. R2 helps to easily change the turnon gate current of all the parallel FETs by changing a single resistor instead of changing each of the individual resistors. R20 through R24 help in suppressing the circulating current between the gate of the MOSFETs, which may cause gate voltage ringing. To describe the mechanism, consider only two FETs in parallel as shown in Figure 6. Due to the layout, the parasitic common source inductance (CSI) of all the FETs will not be equal. If both the FETs are turned on the same instant and if the di/dt of the drain currents are equal, the voltage across CSI of both FETs (VLs1 and VLs2) will not be equal. This drives a circulating current as shown in Figure 6. Another possibility is if there is a skew in the V_{DS} rise and fall time of the parallel FETs, circulating current can flow through the C_{GD} as shown in Figure 7 and cause unwanted behavior. Using individual gate resistors help to suppress the circulating current and help damp unwanted ringing effects.

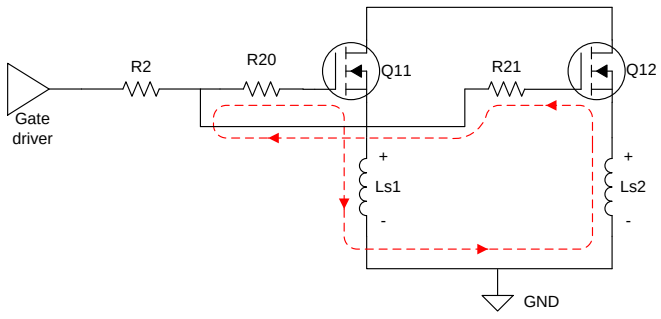

Figure 6. Gate Circulating Current Due to CSI

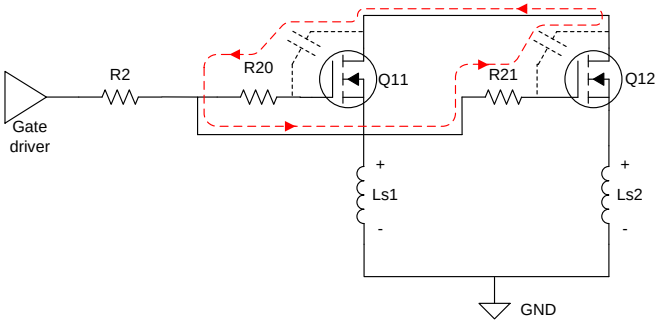

Figure 7. Gate Circulating Current Due to Skew

The V_{DS} fall time is slowed down to ≈ 250 ns and the rise time close to ≈ 50 ns. The slow switching helps to reduce high-frequency ringing between the FETs due to circuit layout parasitics. An estimate of the rise and fall times can be calculated from Equation 1 through Equation 5.

$$i_{Gsource/FET} \approx \frac{\left(\frac{V_G - V_{MILLER}}{R_{PULLUP} + R2 + R_{EQ}}\right)}{n} \approx \frac{\left(\frac{12 - 4}{0.9\ \Omega + 24\ \Omega + 1.92}\right)}{5} \approx 0.06\ A \quad (1)$$

where:

- $i_{Gsource/FET}$ is the gate source current per FET
- V_G is the gate voltage applied
- V_{MILLER} is the miller plateau voltage, which can be determined from the FET datasheet gate charge curve
- R_{PULLUP} is the gate driver IC internal pullup resistance
- R_{EQ} is the equivalent resistance seen by the gate driver after R2
- n is the number of FET's in parallel

$$R_{EQ} = \left(\frac{R20 + R_{Gint}}{n}\right) = \left(\frac{8.2\ \Omega + 1.4\ \Omega}{5}\right) = 1.92\ \Omega \quad (2)$$

where:

- R_{Gint} is internal gate resistance of the MOSFET, which can be determined from the MOSFET datasheet

$$t_{FALL\_TIME} \approx \frac{Q_{GD}}{i_{Gsource/FET}} \approx \frac{17\ nC}{0.06\ A} \approx 283\ ns \quad (3)$$

where:

- Q_{GD} is the gate-to-drain charge, which can be determined from the MOSFET datasheet

$$i_{Gsink/FET} \approx \frac{V_{MILLER}}{R20 + R_{Gint}} \approx \frac{4}{8.2 + 1.4} \approx 0.417\ A \quad (4)$$

where:

- $i_{Gsink/FET}$ is the gate sink current per FET

$$t_{RISE\_TIME} \approx \frac{Q_{GD}}{i_{Gsink/FET}} \approx \frac{17\ nC}{0.417\ A} \approx 40.77\ ns \quad (5)$$

2.2 Inverter

2.2.1 Inverter Subcircuit

One of the three-phase inverter's half-bridge is shown in Figure 8. Five FETs (Q1 through Q5) are paralleled for the high-side switch of the inverter, and five FETs (Q11 through Q15) are paralleled for the low-side switch. This is done to share power dissipated in the inverter between multiple FETs helping maintain the junction temperature of the FETs within limits with lesser cooling requirements. The total loss in the inverter comprises of the conduction loss, switching loss, dead time losses (due to body diode conduction), loss due to charging and discharging the output capacitance of the FETs, and the reverse recovery power loss in the body diode. The advantages of paralleling on inverter loss is described in Section 2.2.2.

C22 is a high-frequency decoupling capacitor that is placed close to the half-bridge subcircuit. This capacitor provides the high initial transient current while switching the FETs. Absence of this capacitor results in excessive ringing voltages on the V_{DS} of the MOSFETs. C29 and R13 comprise the snubber circuit for the high-side switch and C35 and R25 for the low-side switch. A snubber circuit is required to slow down the dV_{DS}/dt switching transitions helping avoid high-frequency ringing on the switch node, which in turn helps reduce EMI. The snubber also helps reduce the magnitude of overshoot on the V_{DS} of the FETs.

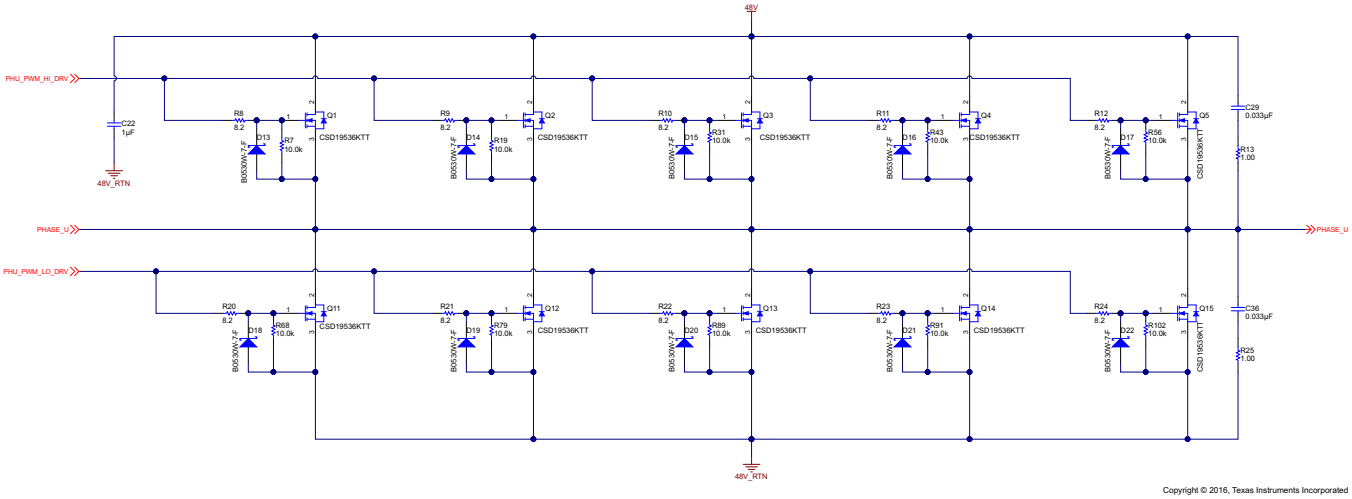

Figure 8. Inverter Stage Half-Bridge With Five FETs in Parallel

2.2.2 Advantages of Paralleling FETs

Paralleling FETs provides three main benefits. It reduces conduction, switching loss per FET, and thermal resistance from the top of the PCB through the heatsink to ambient. The effect on each of these parameters is explained in the following subsections.

2.2.2.1 Effect on Conduction Losses

This is the loss occurring in the MOSFET when it is fully turned on and conducting current. Its magnitude depends on the drain current (I_D) flowing through the MOSFET and its on resistance (R_{DSon}). In the three-phase AC inverter drive, the output phase current flows complementarily between the high-side switch and the low-side switch. During the positive half cycle of the motor phase current, the high-side switch conducts and the low-side switch freewheels and vice versa during the negative half cycle. Assuming symmetrical PWM operation in both the positive and negative half cycles of motor phase current, the current through each FET can be estimated to be equal to the RMS value of one half cycle of motor phase current waveform

The conduction loss per FET in the inverter can be estimated by Equation 6. Note that the loss per FET gets scaled down by square of the total number of FETs in parallel. This is one of the most important advantages of paralleling FETs.

$$P_{C/FET} \approx \left(\frac{I_{PHRMS}}{n\sqrt{2}}\right)^2 \times R_{DSon} \approx \frac{\left(\frac{I_{PHRMS}}{\sqrt{2}}\right)^2 \times R_{DSon}}{n^2} \quad (6)$$

where:

- I_{PHRMS} is the motor phase current
- n is the total number of FETs in parallel

The total conduction loss in the inverter is estimated by Equation 7. The total conduction loss is divided by the number of FETs in parallel.

$$P_C \approx \left(\frac{I_{PHRMS}}{n\sqrt{2}}\right)^2 \times R_{DSon} \times n \times 2 \times 3 \approx \frac{\left(\left(\frac{I_{PHRMS}}{\sqrt{2}}\right)^2 \times R_{DSon} \times 6\right)}{n} \quad (7)$$

The effect of paralleling on conduction loss can be better described with the help of Table 4 and Figure 9. Table 4 shows the losses per FET and total inverter conduction loss when the number of FETs paralleled changes and Figure 9 shows the normalized plot. The data is calculated using Equation 6 and Equation 7. The motor phase current is 130 A_{RMS} and the R_{DSon} is 2 mΩ. The conclusion is that the loss per FET decreases by 25 times and total inverter loss decreases by five times when five FETs are paralleled.

Table 4. Conduction Loss versus Number of FETs in Parallel

NUMBER OF FETs IN PARALLEL	CONDUCTION LOSS PER FET (W)	TOTAL INVERTER CONDUCTION LOSS (W)
1	16.900	101.40
2	4.225	50.70
3	1.880	33.80
4	1.060	25.35
5	0.680	20.28

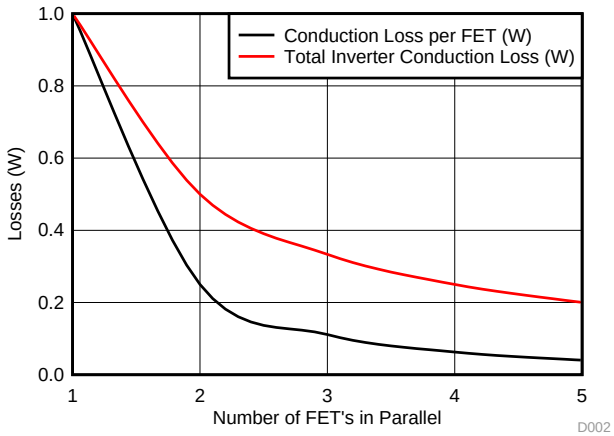

Figure 9. Normalized Conduction Loss versus Parallel FET's

2.2.2.2 Effect on Switching Losses

The loss occurring in the MOSFET during its transition from an on to off state and vice versa is the switching loss of the MOSFET. The switching loss depends on the switching frequency, current, and voltage being switched through the MOSFET, the magnitude of rise and fall times of both the MOSFET V_{DS}, and the MOSFET drain current I_D as well as whether the MOSFET is being hard switched or soft switched. Hard and soft switching conditions in the AC inverter drive are described in Section 2.4.

During positive half cycle of motor phase current the low-side switch gets soft turned on and the high-side switch is hard turned on. Similarly, during the negative half cycle the low-side switch is hard turned on and the high-side switch is soft turned on. Assuming switching losses to be negligible during soft switching, the majority of the switching losses in the high-side switch will occur when current is positive and the low-side switch when the current is negative. The switching loss per FET is estimated using Equation 8. A scaling factor of 0.5 is used to eliminate the soft switching losses. Note that the switching loss per FET is scaled down by a factor equal to the number of FETs in parallel.

$$P_{SW/FET} \approx 0.5 \times 0.5 \times V_{DC} \times \left(\frac{I_{PHRMS}}{n}\right) \times \left(t_{ON} + t_{OFF}\right) \times f_{SW}$$

$$P_{SW/FET} \approx \frac{\left(0.5 \times 0.5 \times V_{DC} \times I_{PHRMS} \times \left(t_{ON} + t_{OFF}\right) \times f_{SW}\right)}{n} \quad (8)$$

where:

- V_{DC} is the DC bus voltage
- I_{PHRMS} is the motor phase current
- t_{ON} is the sum of rise time of V_{DS} and fall time of I_D
- t_{OFF} is the sum of fall time of V_{DS} and rise time of I_D
- f_{SW} is the inverter switching frequency
- n is the number of FETs in parallel

The total switching loss for the half bridge is estimated by Equation 9. Although the switching loss per FET decreases the total switching loss remains the same. Paralleling helps in decreasing the loss per FET helping in thermal management but does not help in reducing the total switching losses.

$$P_{SW} \approx \left(0.5 \times 0.5 \times V_{DC} \times \left(\frac{I_{PHRMS}}{n}\right) \times \left(t_{ON} + t_{OFF}\right) \times f_{SW}\right) \times n \times 2 \times 3$$

$$P_{SW} \approx \left(0.5 \times 0.5 \times I_{PHRMS} \times I_D \times \left(t_{ON} + t_{OFF}\right) \times f_{SW}\right) \times 6 \quad (9)$$

The effect of paralleling on switching loss can be better described with the help of Table 5 and Figure 10. Table 5 shows the switching losses per FET and the total inverter switching loss when the number of FETs paralleled changes and Figure 10 shows the normalized plot. The data is calculated using Equation 8 and Equation 9. The motor phase current is 130 A_{RMS}, the switching frequency is 8 kHz, the DC bus voltage is 48 V, and the on and off times are taken as 250 ns each for analysis purpose. The conclusion is that the loss per FET decreases by five times and total inverter switching loss is the same when five FETs are paralleled.

Table 5. Switching Loss versus Number of FETs in Parallel

NUMBER OF FETs IN PARALLEL	SWITCHING LOSS PER FET (W)	TOTAL SWITCHING LOSS (W)
1	6.24	37.44
2	3.12	37.44
3	2.08	37.44
4	1.56	37.44
5	1.25	37.44

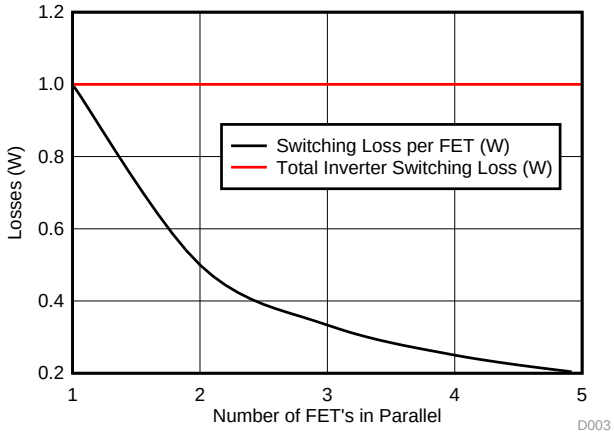

Figure 10. Normalized Switching Loss versus Parallel FETs

2.2.2.3 Effect on Thermal Resistance

The thermal resistance from the FET junction to the ambient is a very important parameter for the inverter. It determines the junction temperature of the FET for a given power dissipation. The IMS PCB is used for this TI Design. The PCB thermal stackup for this design is shown in Figure 11. A 2-oz copper layer is used for increased current carrying capacity. A very thin thermally conductive dielectric material is used between the copper layer and the metal substrate. The thinner the dielectric layer, the lower its thermal resistance. The metal base is made up of aluminum substrate; this layer together with the thermally conductive laminate layer provides a very low thermal resistance laterally as well as perpendicularly helping spread heat on the PCB surface uniformly and conduct the heat into the heatsink effectively. A thermal interface material or paste can be used between the aluminum substrate and the heatsink for reducing the PCB contact thermal resistance to the heatsink. An appropriate heatsink is selected based on the total power to be dissipated in the inverter, the maximum operational ambient temperature of the inverter system, and the cooling system available.

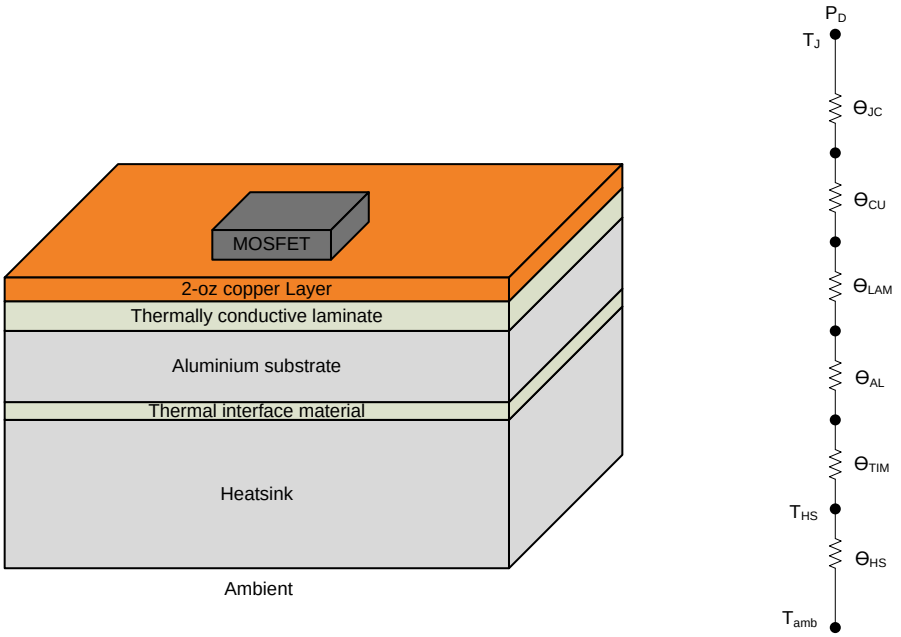

Figure 11. Thermal Stackup

The equivalent electrical model for the thermal stackup is also shown in Figure 11. The thermal resistances are as follows:

- θ_{JC} is the junction to bottom case thermal resistance of the MOSFET
- θ_{CU} is the thermal resistance of the copper layer
- θ_{LAM} is the thermal resistance of the thermally conductive dielectric layer
- θ_{AL} is the thermal resistance of the aluminum substrate
- θ_{TIM} is the thermal resistance of the thermal interface material/paste
- θ_{HS} is the junction to case thermal resistance heatsink to ambient

The thermal resistance of each layer can be calculated by Equation 10:

$$\theta = \frac{t}{(W \times L \times K)} \tag{10}$$

where:

- t is the thickness of the layer
- W = 8.6 mm is the width of the MOSFET pad
- L = 8.6 mm is the length of the MOSFET pad
- k is the thermal conductivity of the material composing the layer

If only one FET is used then the junction temperature of the FET is calculated by Equation 11:

$$T_J \approx T_A + (P_D \times \theta_{HS}) + \left[P_D \times (\theta_{JC} + \theta_{CU} + \theta_{LAM} + \theta_{AL} + \theta_{TIM})\right] \tag{11}$$

The thermal resistance model for n FETs is shown in Figure 12. Note that the model has been simplified by considering only the perpendicular thermal resistances. For n FETs, the thermal resistances are in parallel and the equivalent thermal resistance from the top of PCB to the heatsink is scaled down by n times. The junction temperature is calculated by Equation 12:

$$T_J \approx T_A + (P_D \times \theta_{HS}) + \left[P_D \times \frac{(\theta_{JC} + \theta_{CU} + \theta_{LAM} + \theta_{AL} + \theta_{TIM})}{n}\right]$$

$$T_J \approx T_A + (P_D \times \theta_{HS}) + \frac{1}{n}\left[P_D \times (\theta_{JC} + \theta_{CU} + \theta_{LAM} + \theta_{AL} + \theta_{TIM})\right] \tag{12}$$

The reduced thermal resistance and the reduced power dissipation on paralleling FETs help in keeping the board temperature low for high current inverters. Note that an exact thermal resistance calculation requires both the lateral and perpendicular thermal resistances for each layer to be accounted. Due to the complexity involved, this can be best done by a computational fluid dynamic (CFD) tool.

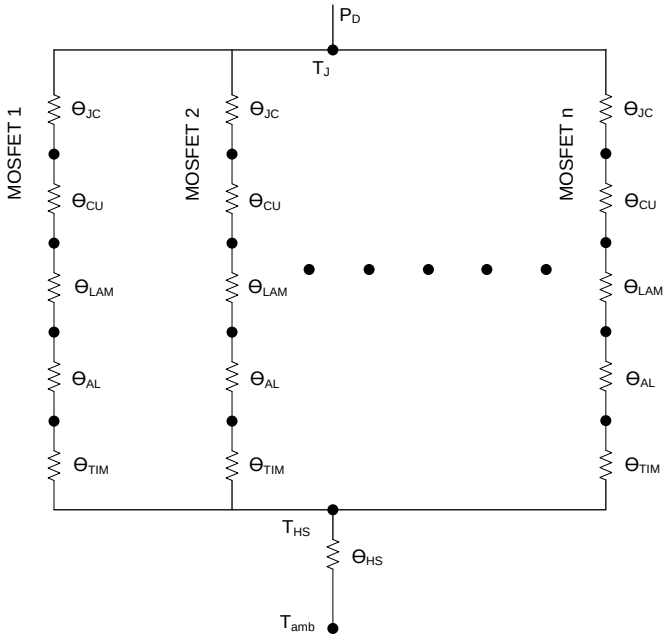

Figure 12. Thermal Resistance Model for n FETs in Parallel

2.2.3 Parameters Affecting FET Paralleling

When paralleling FETs, current sharing becomes very important. All the parallel FETs are expected to carry equal current so that the losses are equally distributed. The FET operation can be split into conduction phase and switching phase. The effect of various parameters effecting current sharing in each of these phases is described in the following subsections.

2.2.3.1 Conduction Phase

In the conduction phase, the FETs are continuously conducting. The main parameter that affects current sharing during this phase is the R_{DSon} of the FET. If R_{DSon} of the FET's are not equal then the FET with the highest on resistance carries the least current and the one with lowest on resistance carries the highest current. Because MOSFETs have a positive temperature coefficient of on resistance (see Figure 13), the current sharing gets self regulated. The FET carrying the highest current has the most conduction losses; this leads to temperature increase of the FET. Increased FET temperature causes an increase in the R_{DSon} of the FET, which in turn reduces the current through the FET. This self-regulating mechanism makes the current through each FET close to each other over time.

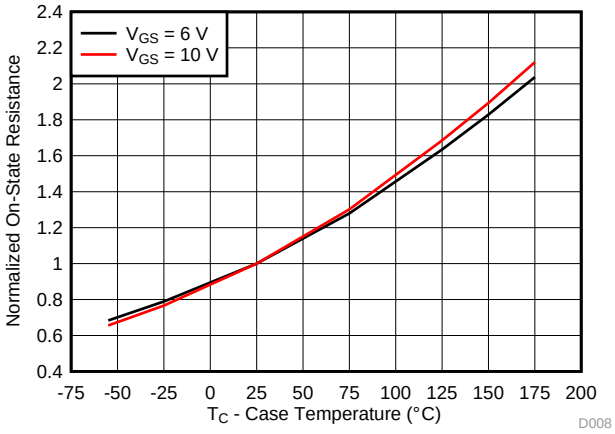

Figure 13. R_{DSon} Variation With Temperature

2.2.3.2 Switching Phase

The current sharing during the switching phase of the FET is affected by asymmetries in the gate drive circuit, differences in the circuit parasitics, and variations in device parameters such as transconductance g_{FS}, threshold voltage V_{TH}, and the input capacitances C_{GD} and C_{GS}. The effects of each parameter on current sharing are as follows:

- In order for all the FETs to be turned on at the same time, the gate drive circuit for each FET has to be very similar. The gate charge current for each parallel FET has to be equal. The gate voltage applied by the gate driver must be the same. Also there should be no skew in the gate-to-source voltages applied to the different FETs. If all these parameters are kept within tight tolerance, the dynamic current sharing remains equal. One way to keep all these parameters in tight tolerance is to use a single gate driver IC to drive all the parallel FETs. This ensures minimal skew between the V_{GS} of FETs and the V_{GS} voltage remains the same. The gate current into each FET can be maintained close to each other by choosing gate resistor values that have a tight tolerance.
- Circuit parasitics like the source (L_S) and drain (L_D) inductances affect the turnon and turnoff times of the FET. If one FET has a higher L_S compared to the others, a higher voltage is induced across L_S when current flows through it. This reduces the effective V_{GS} applied to the FET, which in turn slows down the turnon time of the FET effecting dynamic current sharing. One solution to avoid the effect of L_S is to bypass it by connecting the gate current return path directly to the source pin of the FET. Another solution is to make the layout symmetric so that the L_S and L_D of each of the FETs are close to each other. Matching L_S and L_D also ensures that the rise and fall times of current in each FET is close.
- The threshold voltage of FETs is another important parameter affecting current sharing. Usually the V_{TH} varies in the range of 2 to 4 V. As a result of this, the FET having the lowest V_{TH} turns on first and carries the highest current. Therefore, the FETs selected should have a tight tolerance in V_{TH}. Usually the FETs from one production batch have V_{TH} close enough that by the time the current through one FET rises significantly, the gate voltage of other FETs reach their V_{TH} reasonably quick and start conducting. Also, it is important to have individual gate resistances for each of the FET. If individual gate resistances are absent and all the gates are shorted together, then the FET—which reaches its V_{TH} first—goes into the Miller region faster and clamps the gate of the other FETs to its Miller voltage, which further slows down the gate voltages of the remaining FETs. This significantly effects the turn on behavior. V_{TH} is also dependent on temperature. The higher the temperature, the lower the V_{TH}; this ensures that the FET turns on even faster, which may lead to runaway conditions. Therefore, it is important to maintain all the FETs at equal temperature. The IMS PCB helps in this.
- Transconductance g_{FS} of the FET also affects the dynamic current sharing between the FETs. The FET with the highest g_{FS} has a faster rate of change of drain current with change in the gate-to-source voltage. So, during turnon, the FET with the highest g_{FS} conducts the most current, and during turnoff the FET with the lowest g_{FS} conducts current for a longer time.
- The input gate-to-source capacitance C_{GS} and gate-to-drain capacitance C_{GD} also affect dynamic current sharing. If the gate drive for all the FETs is symmetric (that is, drive voltages and currents are

equal), then the FET with the lowest input capacitance C_{ISS} reaches its threshold voltage first and conducts the most current during turnon. During turnoff, the FET with the highest input capacitance reaches its threshold voltage last and conducts current for a longer time. To reduce the impact of the input capacitance on current sharing, it is important to use individual gate resistors with low values. Using low values ensures that all the FETs with variations in C_{ISS} reach their threshold values fairly close to each other. Selecting gate resistors is a trade-off between suppressing circulating currents and suppressing the effect of variations in C_{ISS} and V_{TH}.

2.3 Insulated Metal Substrate PCB

As explained in Section 2.2.3.2 for equal current sharing between parallel SMD FETs, the parameters of each MOSFET have to be kept equal. As most of these parameters are temperature dependent, it becomes essential to maintain each FET at the same temperature and avoid thermal hotspots at a single FET. Also high-power density requires good thermal conduction from the FETs to the heatsink. For these reasons, an IMS PCB is to be used. The stackup of the IMS PCB has already been described in Section 2.2.2.3. Additional advantages gained by using IMS PCB over FR4 PCB are as follows:

- High thermal conductivity. IMS PCBs are 8 to 10 times more conductive than FR4 counterparts. This allows to them to dissipate more heat per square inch for similar rise in temperature, leading to increased power density.
- Increases the current carrying capacity of current traces for a given rise in track temperature. This enables a PCB track of specific width and thickness to carry more current as compared to a similar track on a FR4 PCB
- Reduces the working temperature of PCB. PCB hotspots are avoided as heat generated easily spreads to a region of lower temperature.
- Use of metal base plate increases the mechanical strength and durability of the PCB
- PCB backside cooling enables the use of surface mount FETs, which are easier to parallel on the PCB. Using surface mount FETs eliminates the accessories required to mount through-hole FETs, namely through-hole heatsinks, heat sink clips, screws, and sil pads. This in turn reduces the manual assembly steps and increases automation of PCB assembly, leading to cost savings and faster assembly.

2.4 Hard and Soft Switching of Inverter

The FETs in the inverter can either be hard switched or soft switched. A switch is said to be hard switched when both the current through the FET and the voltage across it are non-zero. This overlap leads to power losses when switching the FET. The losses during hard switching can be minimized by decreasing the rise and fall times during switching. But high dv/dt and di/dt due to fast switching leads to high EMI and ringing issues when multiple FETs are paralleled. For the soft-switching mechanism, either the current through the FET or the voltage across it is zero. Soft switching leads to negligible losses while switching the FET.

In the TIDA-00364 inverter drive, the convention used for motor phase current is as follows:

- Positive current: Current enters the motor terminal from the inverter board phase terminal.
- Negative current: Current enters the inverter phase terminal from the motor phase terminal.

In the design, the low-side switches are hard switched when motor current is negative (figureFigure 14). In this condition, the high-side diode was freewheeling before turning on the low-side switch. When the low-side switch is turned on, the voltage across it starts decreasing towards its on resistance drop and the current starts commutating from the high-side freewheeling diode into the low-side FET conduction channel. As both V_{DS} and I_D overlap during the switching transient the switch on is said to be hard to turn on. The low-side switches are soft switched when the motor current is positive (see Figure 15). In this condition, the freewheeling diode of the low-side switch was conducting before the low-side switch is turned on. This ensures that the V_{DS} was clamped to the forward voltage drop of the body diode. When switch is turned on the current simply commutates from the body diode to the FET channel while the V_{DS} does not change much. As one of the parameter V_{DS} was zero in this case, the low-side switch is soft turned on. The high-side switches follow a similar mechanism and get hard switched when the motor current is positive (see Figure 16) and soft switched when the motor current is negative (see Figure 17). Switching losses get concentrated in the low-side switch when motor current is negative and losses are concentrated in the high-side switches when the motor current is positive.

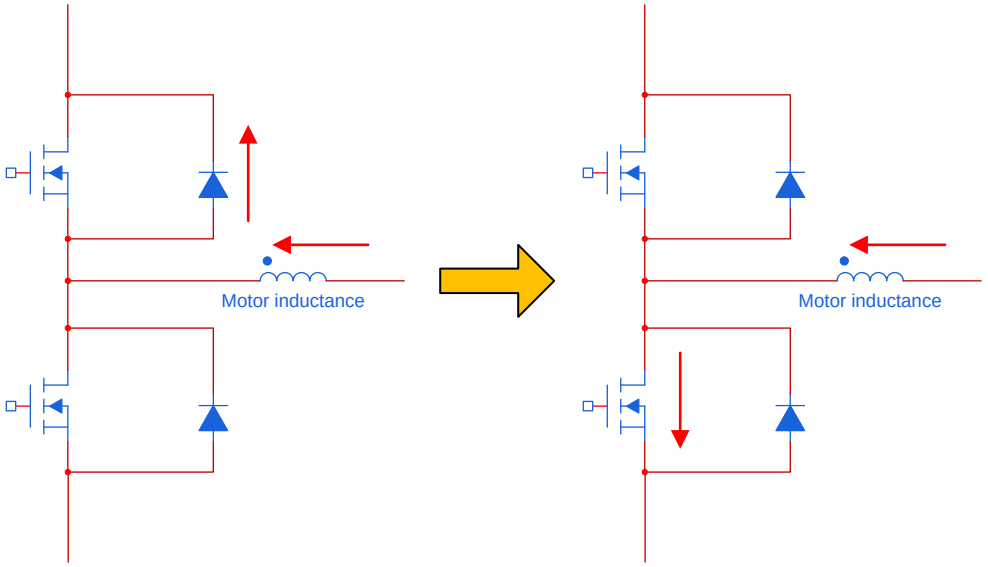

Figure 14. Hard Switching of Low-Side Switch

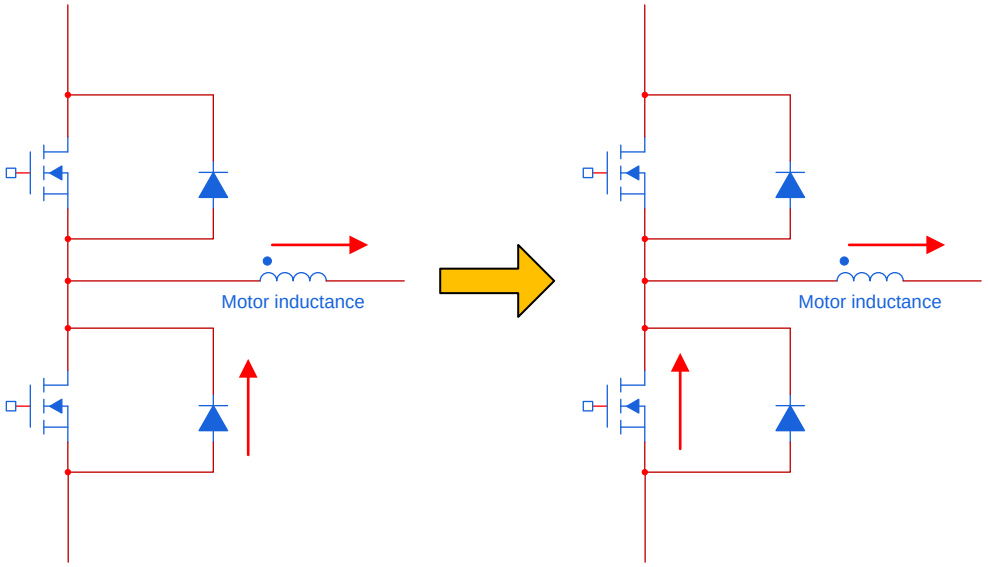

Figure 15. Soft Switching of Low-Side Switch

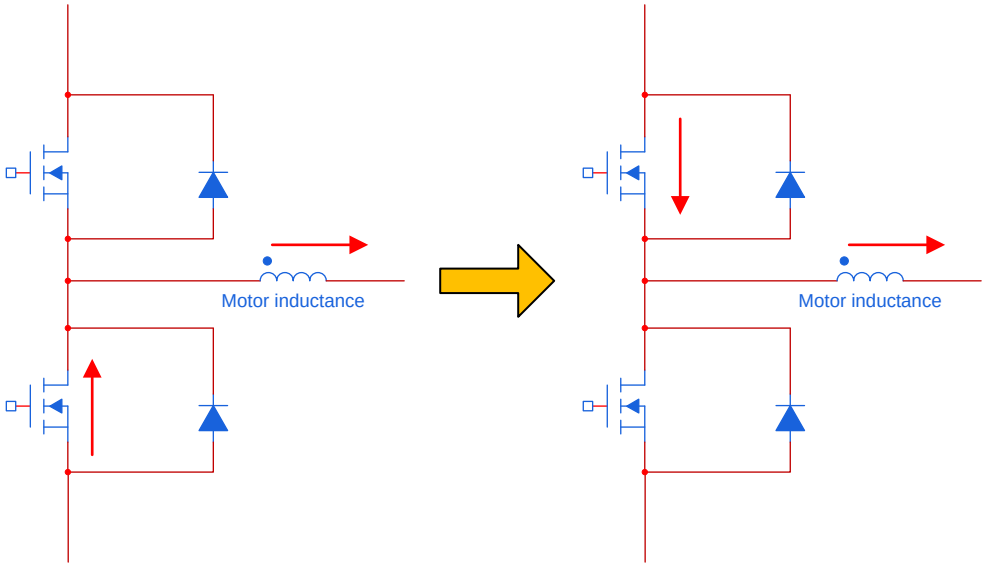

Figure 16. Hard Switching of High-Side Switch

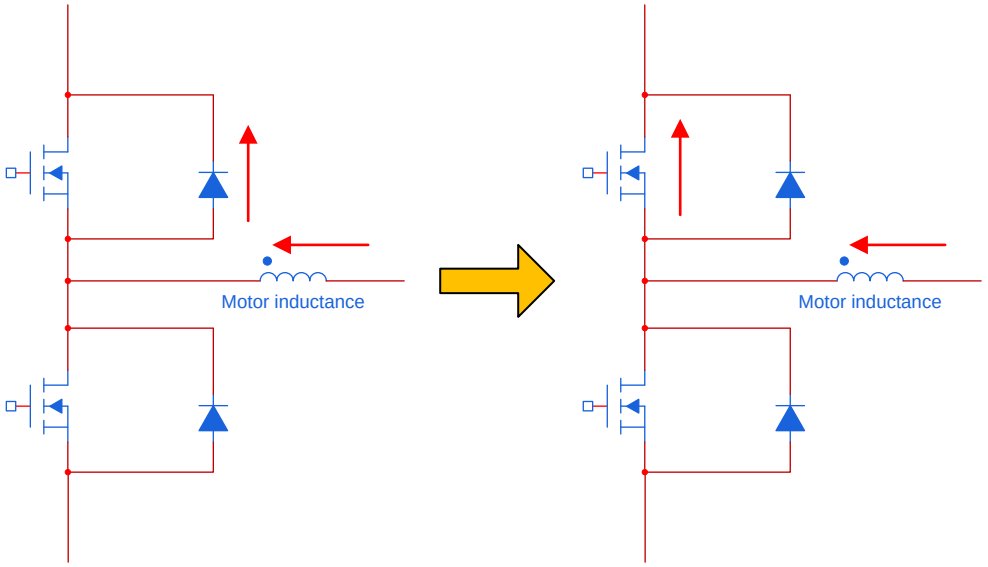

Figure 17. Soft Switching of High-Side Switch

3 Getting Started Hardware

3.1 Board Description

The design hardware comprises of two boards, which are connected together and mounted on a heat sink as shown in Figure 18.

- TIDA-00364_PB: Inverter board with FETs and gate driver circuit
- TIDA-00364_CB: DC link capacitor board

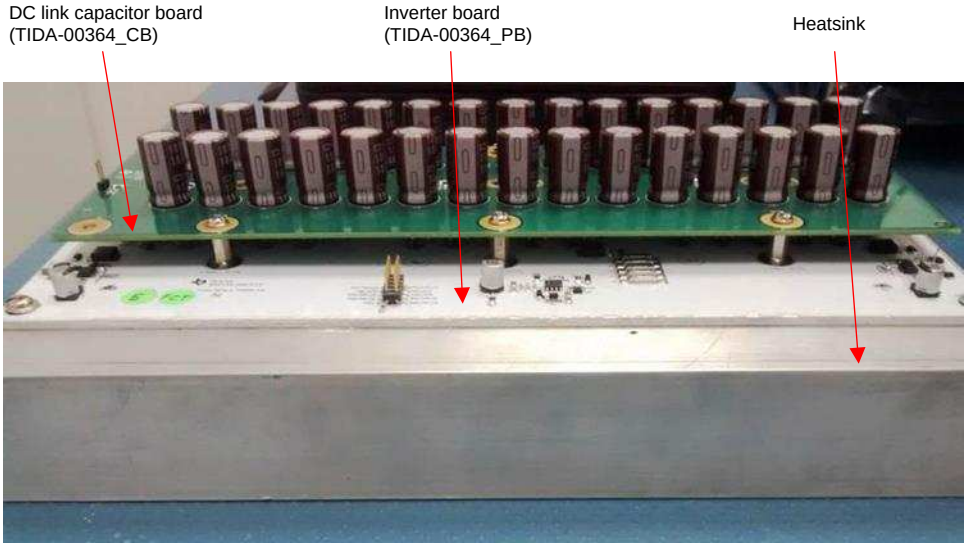

Figure 18. Board Stackup

The 48-V_{DC} supply is connected to the capacitor board and the motor phase connections are taken out from the capacitor board as shown in Figure 19.

Figure 19. Power Connections

The location of the half bridges, the corresponding gate drivers, and PWM connector on the inverter board is shown in Figure 20.

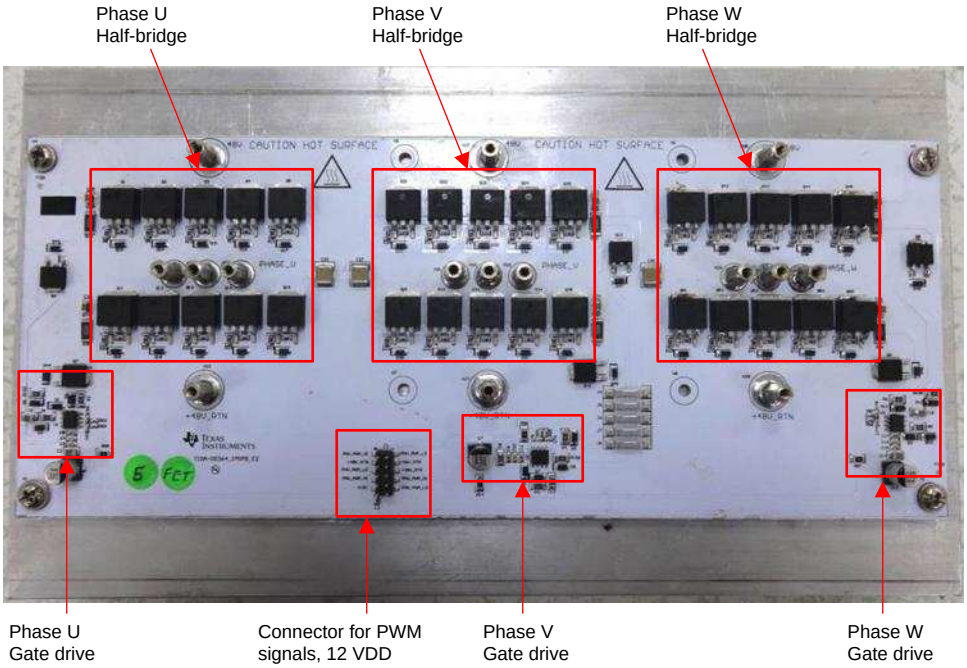

Figure 20. Inverter Board Description

The inverter board is compactly screwed onto the heat sink as shown in Figure 21. Note that there must be no air gap between the inverter board metal substrate and the heatsink if good thermal conductivity is to be maintained. A thin layer of heatsink compound can be applied between the metal substrate and the heatsink to make the thermal connection more compact.

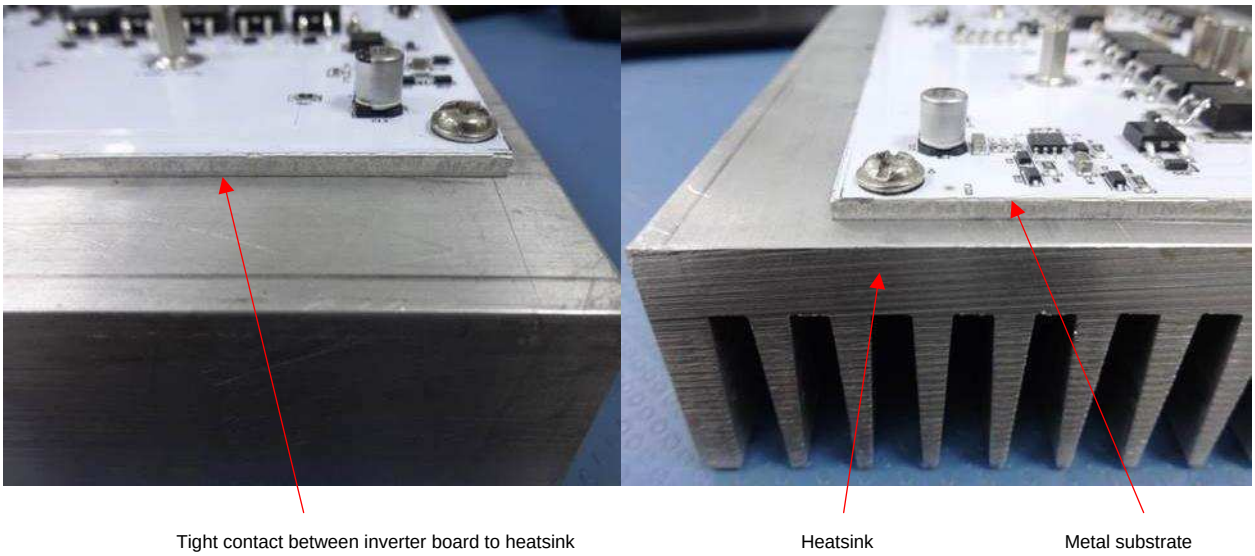

Figure 21. Tight Connection to Heatsink

3.2 Controller Interface Connector Description

The microcontroller is connected to the inverter board through connector J1 with ribbon cables. Each pin name is identified in Figure 22 and the pin function described in Table 6.

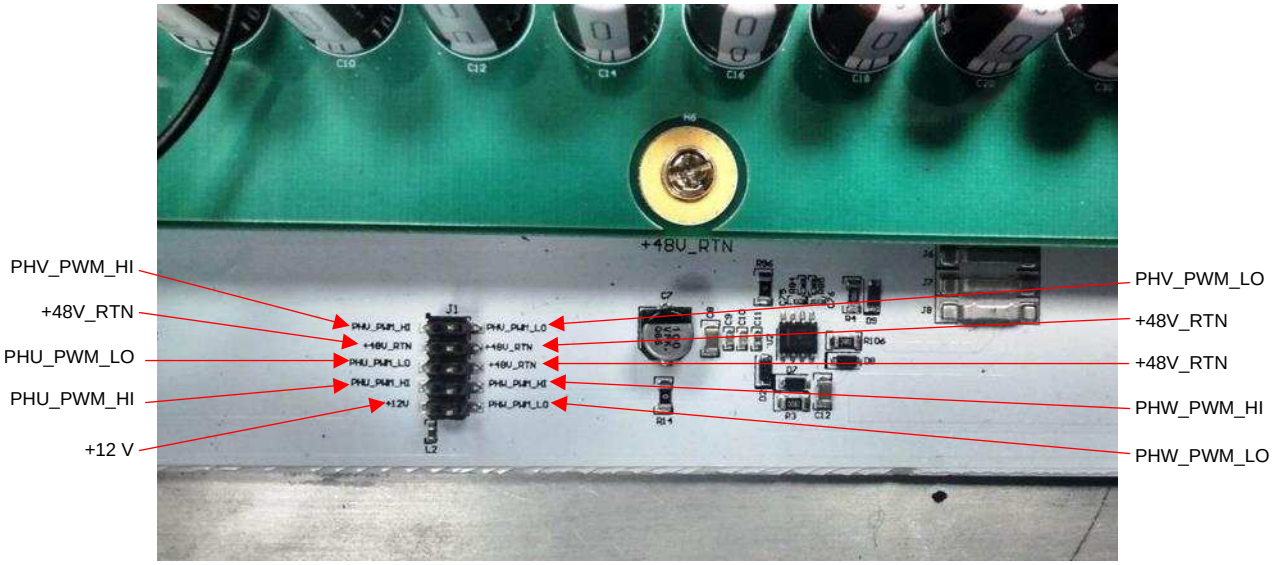

Figure 22. Controller Interface Connector Description

Table 6. Connector Pin Description

PIN NUMBER	PIN NAME	I/O	DESCRIPTION
1	PHV_PWM_HI	INPUT	Phase V high-side switch gate driver PWM input
2	PHV_PWM_LO	INPUT	Phase V low-side switch gate driver PWM input
3	+48V_RTN	GND	GND for 12-V power supply and PWM signals
4	+48V_RTN	GND	GND for 12-V power supply and PWM signals
5	PHU_PWM_LO	INPUT	Phase U low-side switch gate driver PWM input
6	+48V_RTN	GND	GND for 12-V power supply and PWM signals
7	PHU_PWM_HI	INPUT	Phase U low-side switch gate driver PWM input
8	PHW_PWM_HI	INPUT	Phase W high-side switch gate driver PWM input
9	+12V	POWER INPUT	12-V power supply for gate drivers
10	PHW_PWM_LO	INPUT	Phase W low-side switch gate driver PWM input

4 Testing and Results

4.1 Test Setup

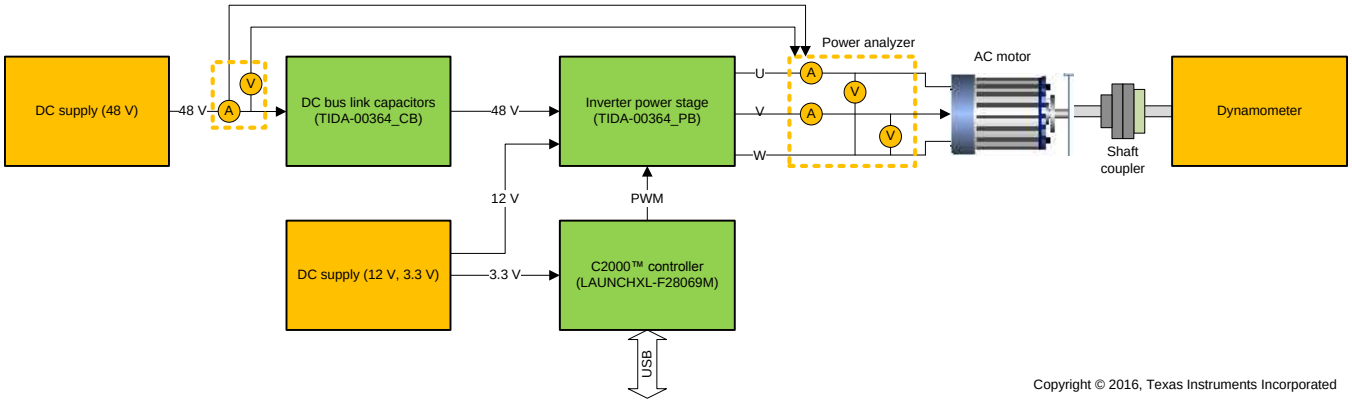

Figure 23. Test Setup Block Diagram

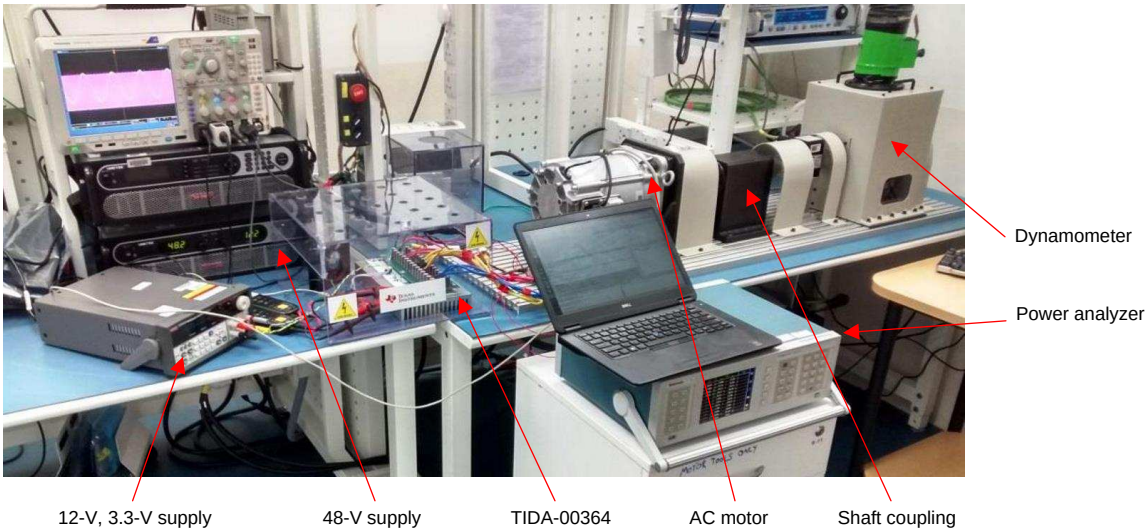

Figure 24. Test Setup

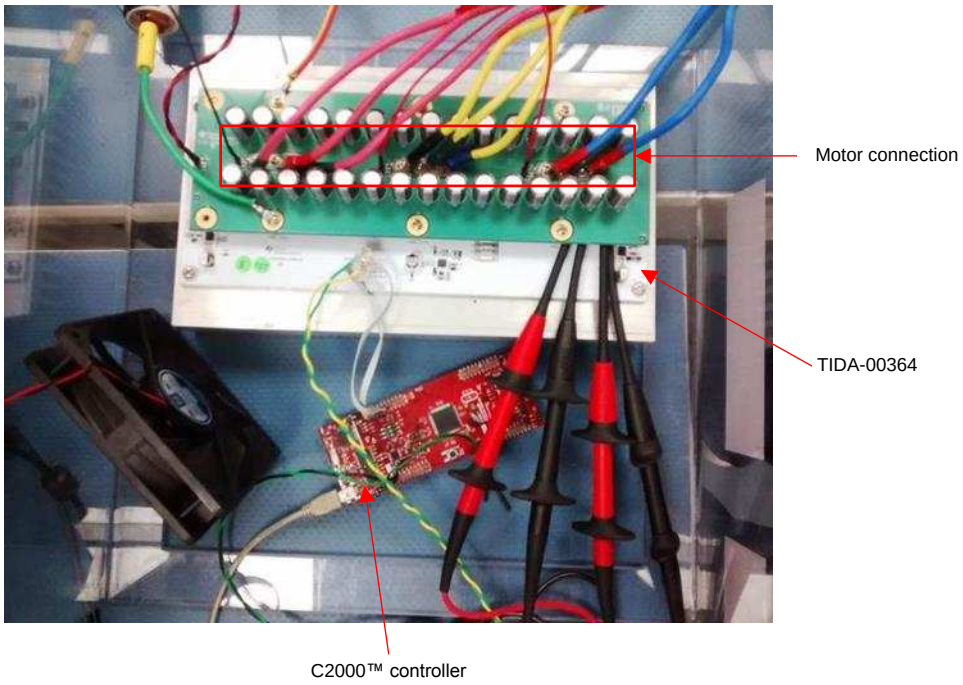

Figure 25. Test Setup Showing Controller Interface

For the test setup, external 48-V_{DC} supply is used instead of lead acid battery. This supply is connected to the inverter board through the DC link capacitor board. Another external power supply provides the 12 V for the gate driver and 3.3 V for the LaunchPad. The inverter board is connected to the motor through the power analyzer. A two wattmeter configuration is used in the analyzer for measuring the output power of the inverter board, and a one-phase, two-wire configuration is used to measure the input power to the inverter. The AC motor is connected to the dynamometer setup through a mechanical shaft coupler. Variable torque is applied to the motor shaft through the dynamometer, which is controlled by a computer.

4.2 Motor Control Algorithm for Testing

Scalar open loop V/f control algorithm is used for driving the motor. In this control algorithm, the speed of induction motor and torque output is controlled by the adjustable magnitude of stator voltages and frequency such that the air gap flux is maintained constant. If V/f remains constant for any change in frequency, the air gap flux remains constant and the torque output becomes independent of the motor current frequency. This can be done by proportionally increasing the voltage applied to the motor with increasing speed. Also a startup ramp in V/f is used to reduce the inrush current into the motor during motor startup. Detailed implementation of the algorithm is explained in the document *Scalar (V/f) Control of 3-Phase Induction Motors*[5].

4.3 MOSFET Switching Waveforms

This section shows the functional waveforms for the inverter power stage. The setup used for the test is shown in Figure 24. Begin by turning on the 12-V_{DC} supply to the gate driver, then turn on the 3.3-V power supply to the C2000 LaunchPad and finally turn on the 48-V_{DC} supply. The motor is started by giving appropriate commands to the controller from the CCS debugger running in a PC. The load on the shaft of the motor is gradually increased until the phase current of the motor reaches ≈ 130 A_{RMS}, which is the continuous current rating of the inverter power stage. The V_{DS} and V_{GS} waveforms of the top and bottom FETs of the half-bridge are captured at the maximum positive and negative current instant's to show soft and hard switching behaviors.

4.3.1 V_{DS} and V_{GS} Waveforms for First and Fifth FET Showing Hard and Soft Switching Behavior

Waveforms from Figure 27 to Figure 34 are for the MOSFETs that are closest to the gate driver (first FET). Waveforms from Figure 35 to Figure 42 are for the MOSFETs that are farthest from the gate driver (fifth FET). Note that all the measurements are taken for phase W.

NOTE: Green: V_{DS} of MOSFET
Red: V_{GS} of MOSFET
Pink: Motor phase current (Convention: Positive current means current flowing into the motor)

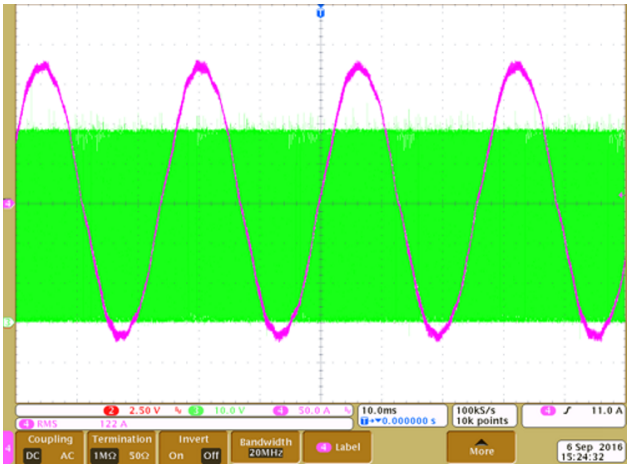

Figure 26. Motor Phase Current Waveform

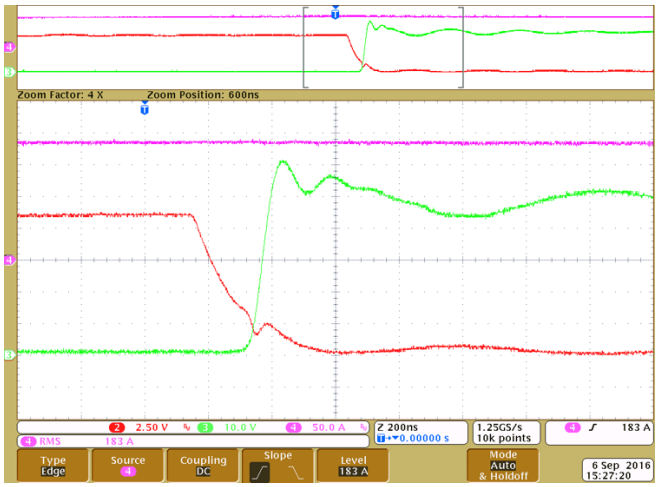

Figure 27. Top FET Hard Switch OFF

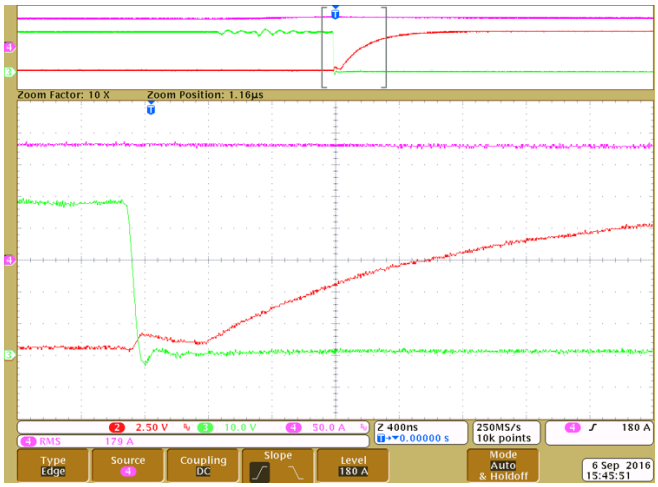

Figure 28. Bottom FET Soft Switch ON

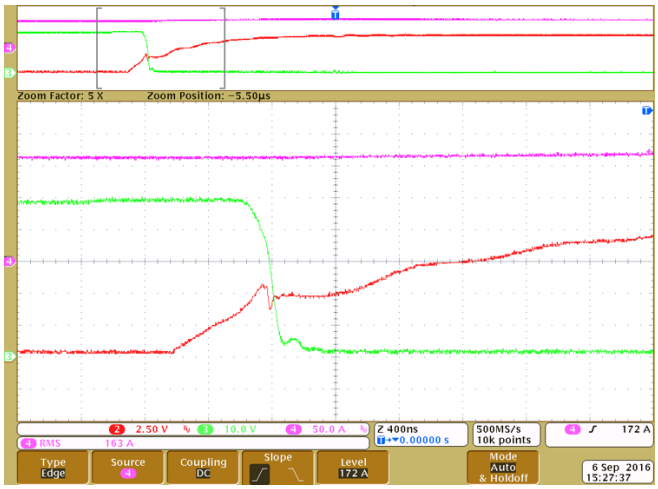

Figure 29. Top FET Hard Switch ON

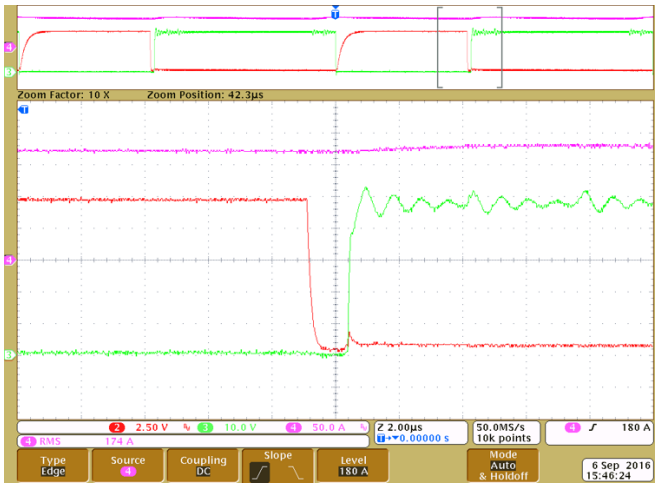

Figure 30. Bottom FET Soft Switch OFF

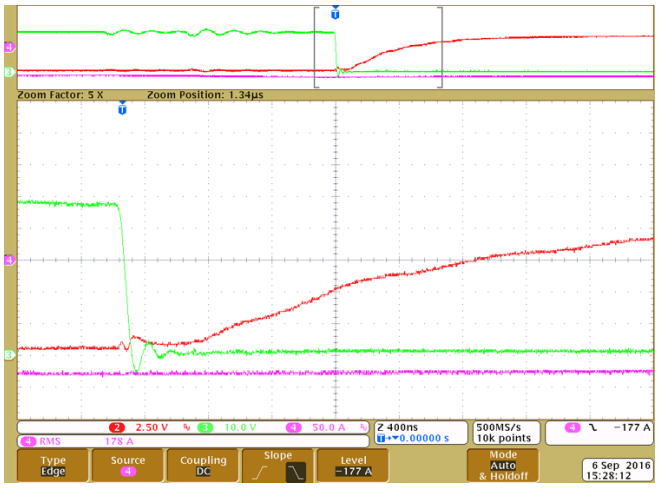

Figure 31. Top FET Soft Switch ON

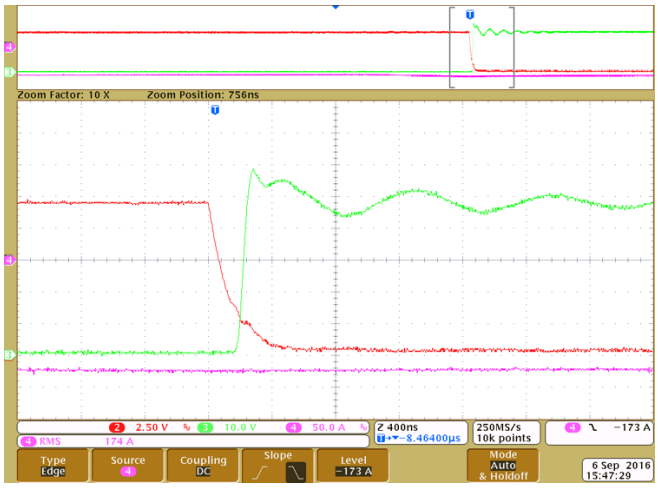

Figure 32. Bottom FET Hard Switch OFF

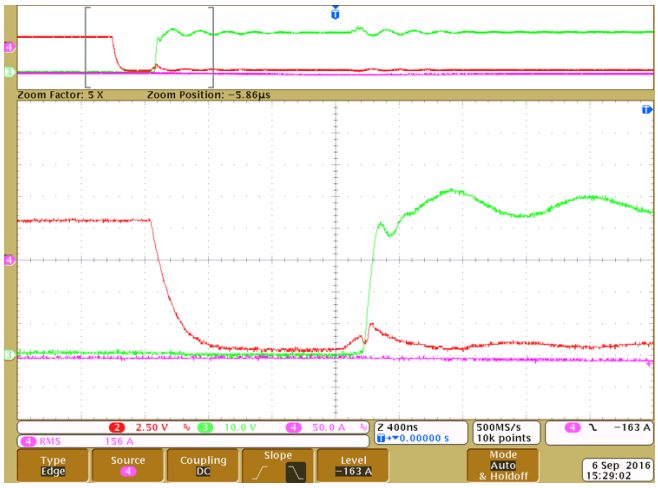

Figure 33. Top FET Soft Switch OFF

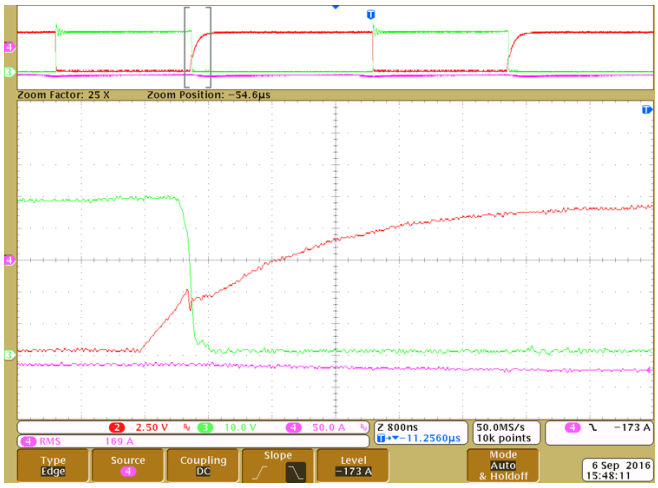

Figure 34. Bottom FET Hard Switch ON

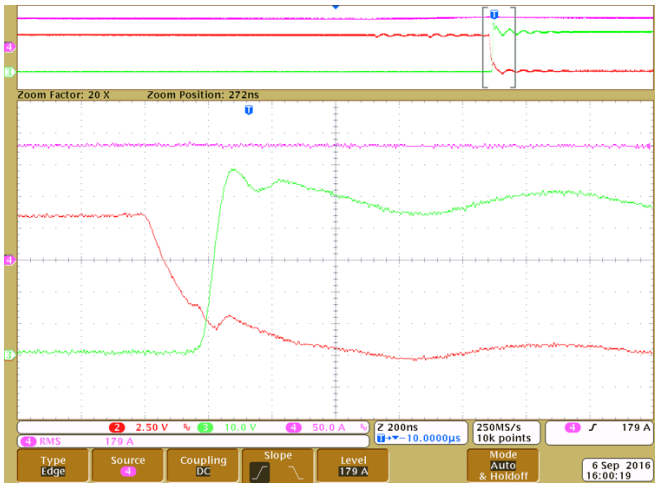

Figure 35. Top FET Hard Switch OFF

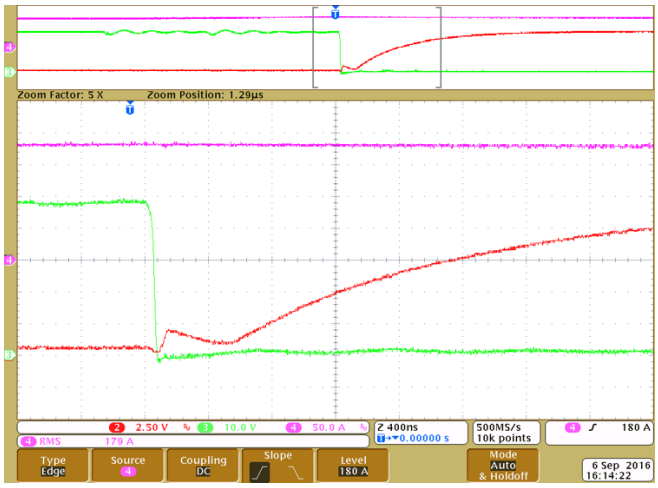

Figure 36. Bottom FET Soft Switch ON

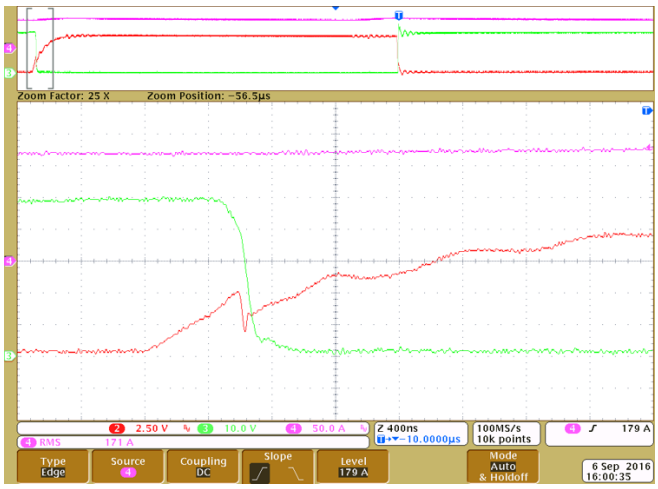

Figure 37. Top FET Hard Switch ON

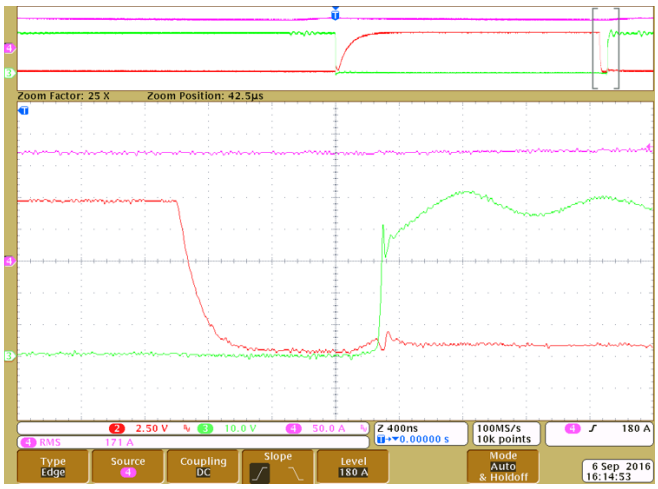

Figure 38. Bottom FET Soft Switch OFF

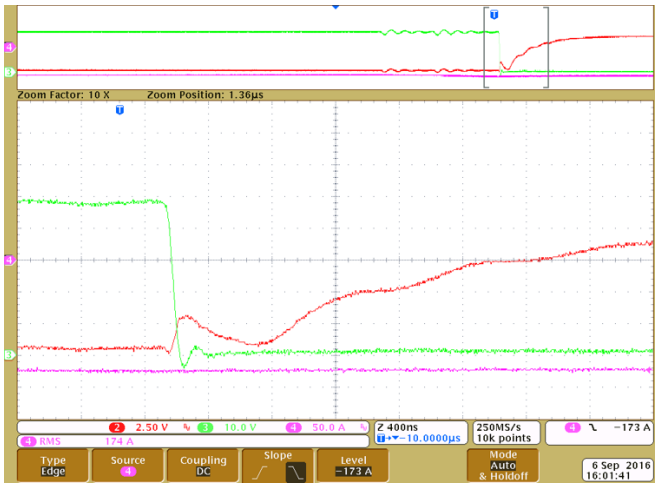

Figure 39. Top FET Soft Switch ON

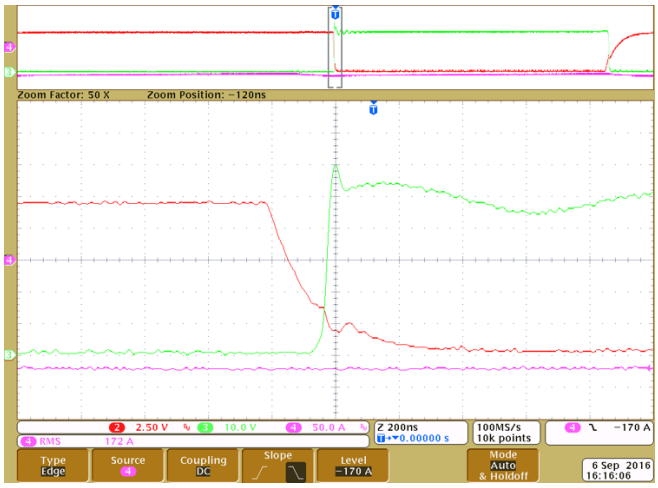

Figure 40. Bottom FET Hard Switch OFF

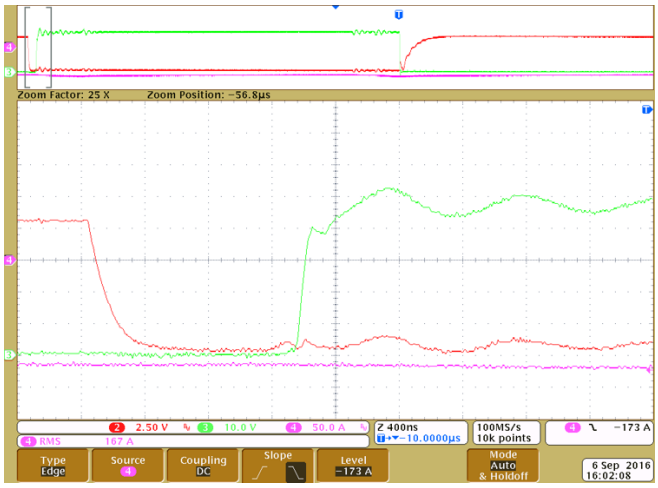

Figure 41. Top FET Soft Switch OFF

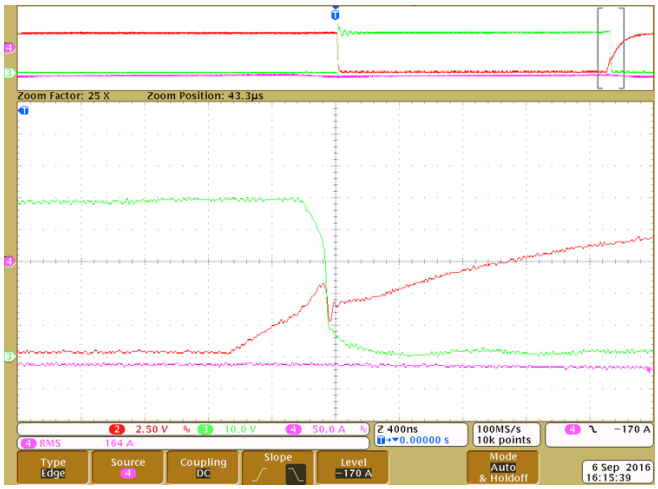

Figure 42. Bottom FET Hard Switch ON

4.3.2 Skew in V_{GS}

Waveforms from Figure 43 to Figure 46 show the skew in V_{GS} when comparing the FET closest and farthest from the gate driver. Note that all the measurements are taken for phase W.

NOTE: Green: V_{GS} of MOSFET closest to gate driver
Red: V_{GS} of MOSFET farthest from the gate driver
Pink: Motor phase current (Convention: Positive current means current flowing into the motor)

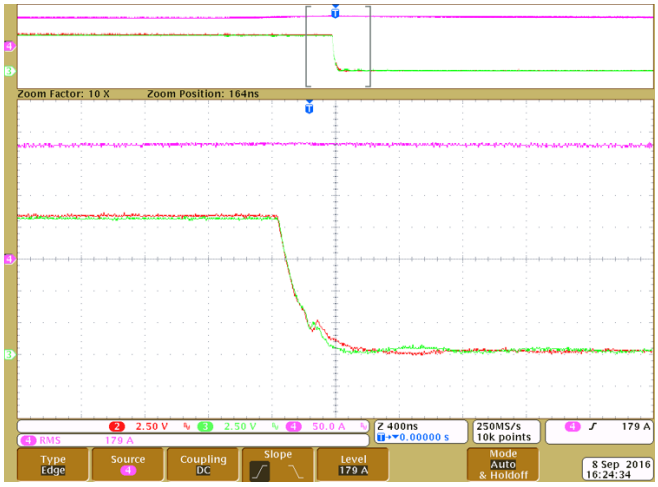

Figure 43. Top FET Hard Switch OFF

Figure 44. Top FET Hard Switch ON

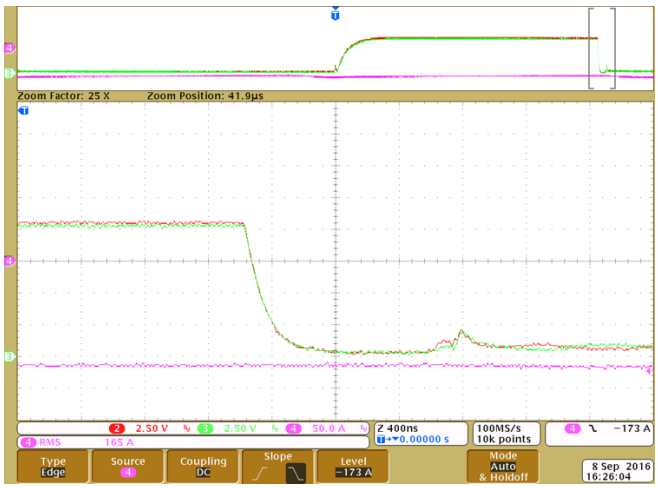

Figure 45. Top FET Soft Switch OFF

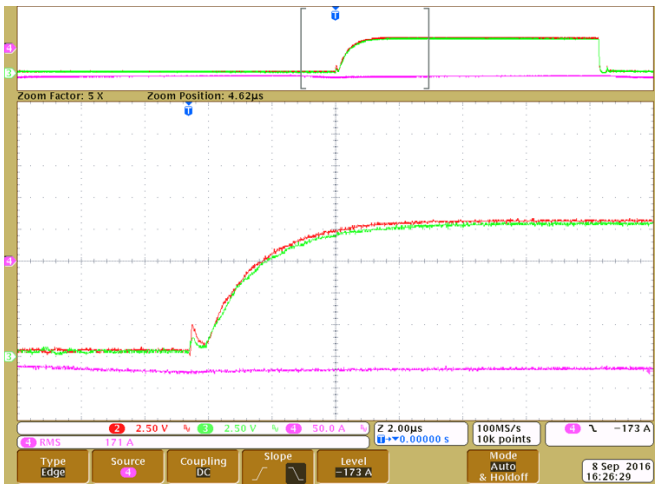

Figure 46. Top FET Soft Switch ON

4.3.3 Skew in V_{DS}

Waveforms from Figure 47 to Figure 50 show the skew in V_{DS} when comparing the FET closest and farthest from the gate driver. Note that all the measurements are taken for phase W.

NOTE: Green: V_{DS} of MOSFET closest to gate driver
Red: V_{DS} of MOSFET farthest from the gate driver
Pink: Motor phase current (Convention: Positive current means current flowing into the motor)

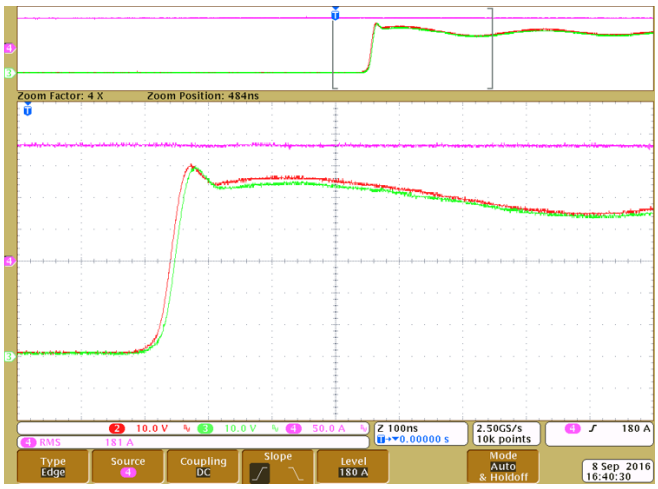

Figure 47. Top FET Hard Switch OFF

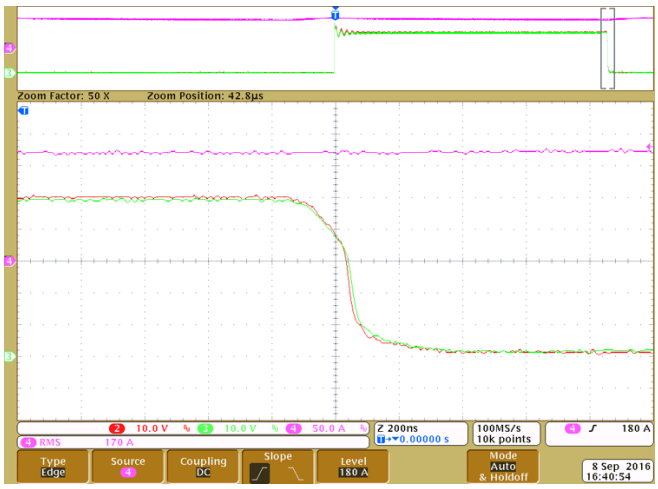

Figure 48. Figure 43 Top FET Hard Switch ON

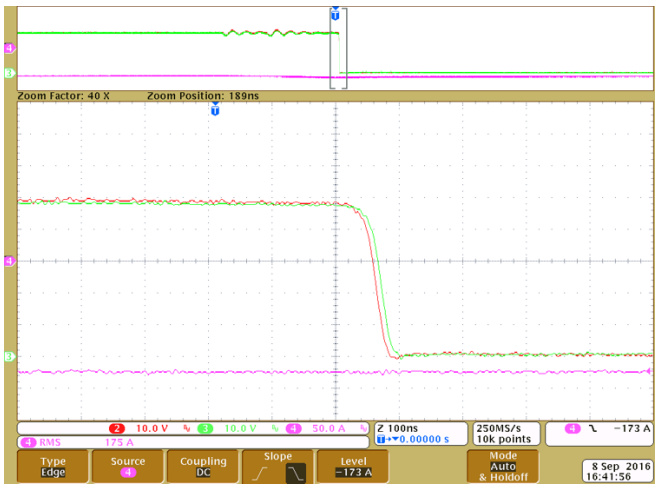

Figure 49. Top FET Soft Switch OFF

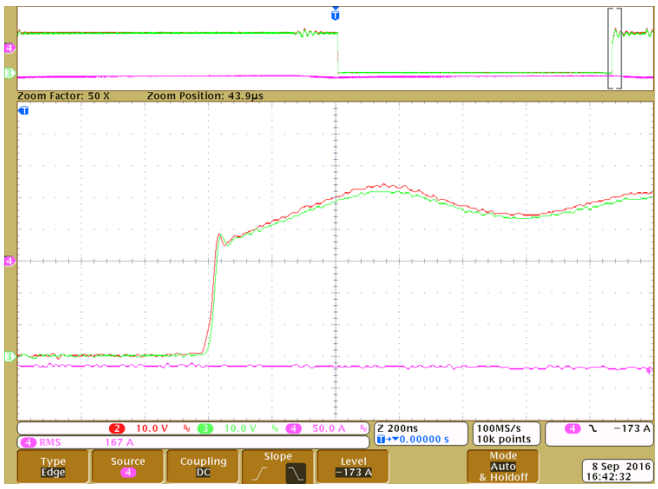

Figure 50. Top FET Soft Switch ON

4.4 Efficiency of Inverter Stage

The efficiency of the inverter is found out using a power analyzer as shown in Figure 23. The power analyzer is configured to measure power using the two wattmeter method. External closed loop current output Hall effect current sensors are used to provide the motor phase current information to the analyzer.

The motor is driven, the load on the shaft is increased in steps of 0.5 Nm. The motor phase current is measured. The input and output power are measured with the analyzer. The inverter losses are calculated for 8- and 10-kHz switching frequencies and shown in Table 7 and Table 8, respectively

Table 7. Inverter Loss Data—8-kHz Switching

TORQUE APPLIED TO MOTOR (Nm)	MOTOR PHASE-TO-PHASE VOLTAGE (V_{RMS})	MOTOR PHASE CURRENT (A_{RMS})	DC BUS VOLTAGE (V_{DC})	DC INPUT CURRENT (I_{DC})	INVERTER INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER LOSS (W)
0	16.35	26.58	48.29	1.86	88.74	76.69	12.06
0.5	16.15	27.54	48.21	3.21	154.01	141.11	12.90
1.0	15.96	30.19	48.12	4.66	224.00	210.28	13.72
1.5	15.80	34.41	48.02	6.19	296.95	281.52	15.43
2.0	15.69	39.88	47.93	7.79	373.02	355.10	17.92
2.5	15.60	46.28	47.83	9.46	452.40	431.34	21.07
3.0	15.54	53.47	47.73	11.29	535.22	510.16	25.06
3.5	15.49	61.41	47.62	13.07	622.01	592.86	29.15
4.0	15.43	70.17	47.49	15.04	714.24	679.28	34.95
4.5	15.37	79.87	47.35	17.16	812.49	770.46	42.03
5.0	15.30	90.80	47.21	19.49	919.72	868.45	51.27
5.5	15.14	119.69	46.86	25.29	1184.88	1105.08	79.80
6.0	14.89	131.27	46.79	26.66	1247.03	1154.61	92.42

Table 8. Inverter Loss Data—10-kHz Switching

TORQUE APPLIED TO MOTOR (Nm)	MOTOR PHASE-TO-PHASE VOLTAGE (V_{RMS})	MOTOR PHASE CURRENT (A_{RMS})	DC BUS VOLTAGE (V_{DC})	DC INPUT CURRENT (I_{DC})	INVERTER INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER LOSS (W)
0	16.20	26.55	48.31	1.92	91.27	76.02	15.25
0.5	15.97	27.34	48.22	3.19	153.20	138.00	15.19
1.0	15.74	30.15	48.13	4.66	223.66	207.49	16.17
1.5	15.56	34.65	48.05	6.19	296.88	278.60	18.28
2.0	15.44	40.44	47.96	7.80	373.61	352.55	21.05
2.5	15.36	47.23	47.86	9.49	453.99	429.24	24.74
3.0	15.30	54.91	47.75	11.29	538.76	509.69	29.07
3.5	15.24	63.36	47.64	13.18	627.68	593.60	34.08
4.0	15.18	72.68	47.51	15.20	722.08	681.28	40.80
4.5	15.12	83.15	47.38	17.41	824.50	775.07	49.43
5.0	15.04	95.27	47.21	19.87	937.87	877.99	59.88
5.5	14.96	110.00	47.04	22.77	1070.66	995.33	75.33
6.0	14.85	131.11	46.79	26.68	1248.19	1148.41	99.78

Figure 51 shows the losses in the inverter stage as a function of inverter output current. As the current increases the switching losses become less dominant and the conduction losses become more dominant. It is observed that the loss is ≈ 92 W at 130 A_{RMS} for 8-kHz switching and ≈ 100 W at 10-kHz switching frequency. Using the loss at 130 A_{RMS}, for 5-kW motor output power and 0.8 power factor the efficiency of the inverter can be estimated to be around ≈ 98% for a 8-kHz switching frequency. Note that during the test, 130 A_{RMS} is pumped into the motor by overloading the reactance part of the motor load and not the real part because of test setup limitations. This is the reason to see lower real power measured at the inverter output at 130 A_{RMS} in the data provided in Table 7 and Table 8.

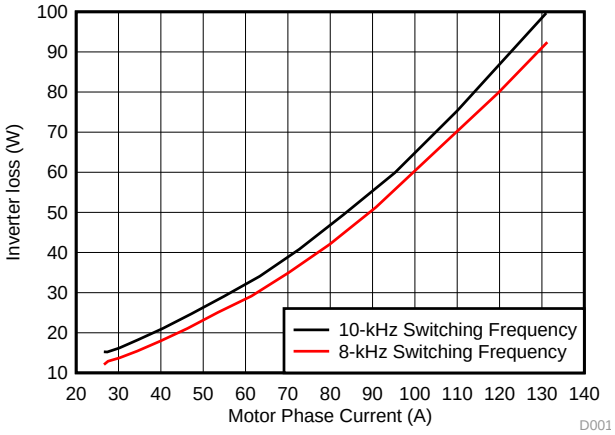

Figure 51. Inverter Loss versus Motor Phase Current

5 Design Files

All design files in Section 5.1 through Section 5.6 have two subfolders: one is for the NexFET-based inverter board (TIDA00364_PB) and the other is for the DC link capacitor board (TIDA00364_CB).

5.1 Schematics

To download the schematics, see the design files at TIDA-00364.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00364.

5.3 PCB Layout Recommendations

Layout is very important for proper functioning of the half-bridge. In general, all the switching loops have to be kept as small as possible to reduce EMI and stray parasitics, which can cause unwanted ringing issues.

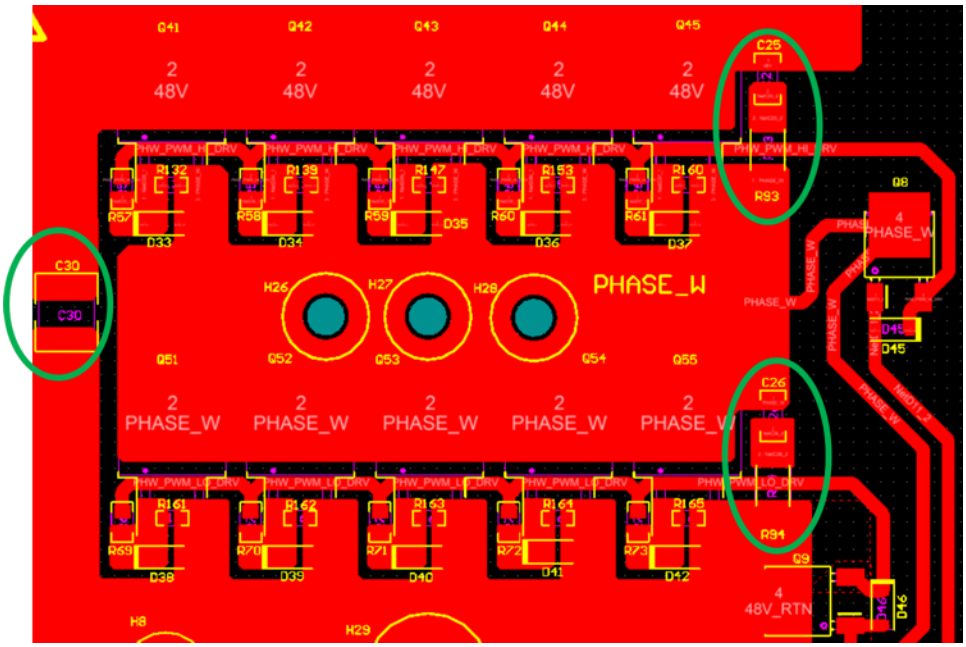

Figure 52. Location of Decoupling Capacitor and Snubber Circuit

- Place the decoupling capacitor C30 as close as possible to the parallel MOSFET half-bridges. Lacking this capacitor causes significant overshoots on the MOSFET V_{DS}.
- The snubber for the high-side switches (Q41 to Q45) comprising C25 and R93 must be kept close to the high-side switches as shown in Figure 52.
- Similarly, the snubber for the low-side switches (Q51 to Q55) comprising C26 and R94 must be kept close to the low-side switches as shown in Figure 52.

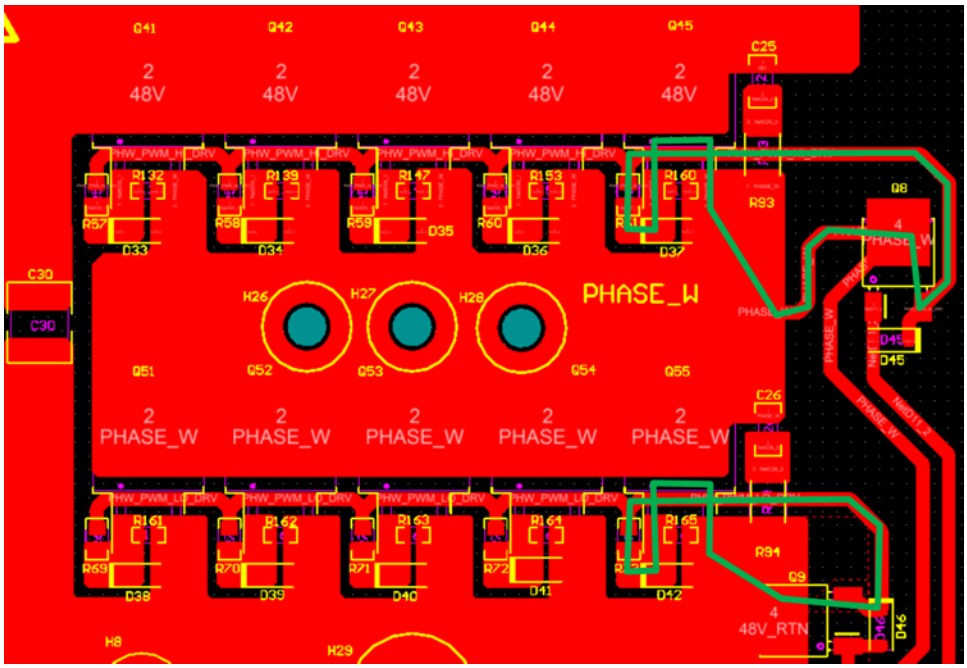

Figure 53. MOSFET Gate Turnoff Loop

- The MOSFET gate turnoff loop for the high-side and low-side switches (highlighted in green in Figure 53) must be kept small to avoid stray track inductance, which may slow down the turnoff process and make the pulldown less effective against Miller induced false turnon.

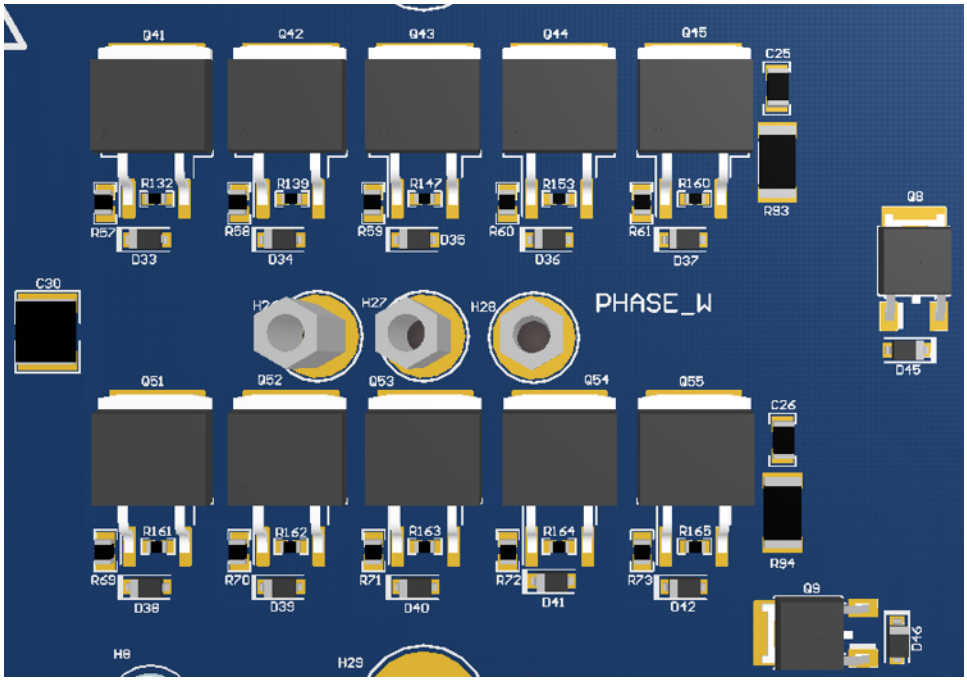

Figure 54. FET Placement

- All the paralleled FETs must be placed as close as possible so that they are at similar temperature, which leads to similar R_{DSon}, g_{FS}, and V_{TH} for the FETs. This helps in equal static and dynamic current sharing between the FETs.

- Place the input DC bus and output phase connectors in the center of the parallel FET module. This ensures that the distance from the FET to the connectors is fairly symmetric for all the FETs. If the connectors are placed at one corner of the parallel FET module, then the FET closest to the connectors conducts the highest current and the FET farthest from the connectors conducts the least current.

5.3.1 Layout Prints

The PCB board size is 270 mm × 112.39 mm. The board area is 30345.3 mm^2.

To download the layer plots, see the design files at TIDA-00364.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00364.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00364.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00364.

6 References

1. Texas Instruments, *Thermal Considerations for Surface Mount Layouts* (Link)
2. Texas Instruments,*Constructing Your Power Supply—Layout Considerations*, 2004/2005 Power Supply Design Seminar (SLUP224)
3. NCAB Group, *IMS—Insulated Metal Substrate*, Presentation (PDF)
4. Bergquist Company, *Bergquist Thermal Clad—Tools for an Optimal Design*, White Paper (PDF)
5. Texas Instruments, *Scalar (V/f) Control of 3-Phase Induction Motors*, Application Report (SPRABQ8)

7 Terminology

ACIM— AC induction motor

PWM— Pulse width modulation

IMS— Insulated metal substrate

CSI— Common source inductance

8 About the Authors

PAWAN NAYAK is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the Motor Drive segment within Industrial Systems.

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