TI Designs

An Efficient Power Supply Reference Design for Optimizing Spur and Phase Noise in RF-Sampling DAC

Description

TI High-Speed Designs are analog solutions created by TI's analog experts. High-speed designs offer the theory, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of useful circuits. This TI Design also addresses circuit modifications that help to meet alternate design goals.

Resources

TIDA-01215	Design Folder
DAC38RF83	Product Folder
LM27761	Product Folder
TPS62095	Product Folder
TPS74401	Product Folder

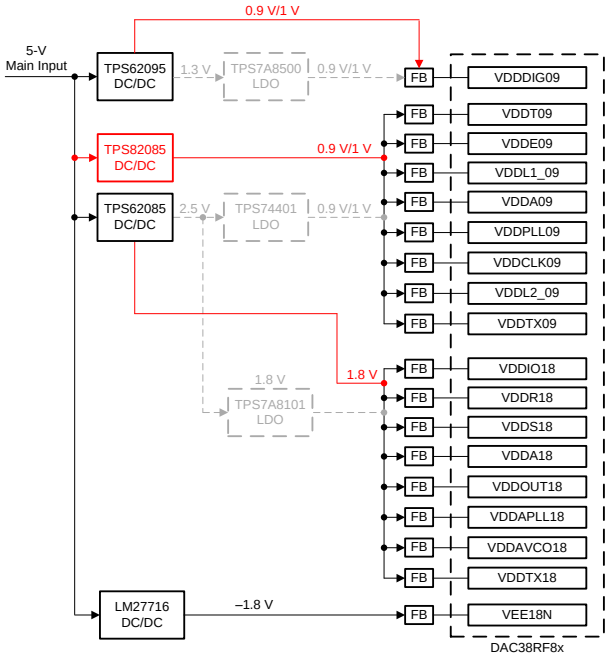
TI E2E™ Community — ASK Our E2E Experts

Features

- Efficient Power Solution for RF Sampling DAC
- Optimal Spur and Phase Noise Performance
- Reduced Board Area
- Reduced Cost of BOM

Applications

- Wireless Base Stations
- Radar System
- RF Waveform Generator



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Overview

1.1 System Description

Traditionally, in order to achieve optimal performance of high-speed data converters, systems designers use low dropout (LDO) voltage regulators to power up all the power supply rails. This is because LDOs have low noise and no switching frequency spurs. However, LDO voltage regulators have poor power efficiency and must be used together with switching voltage converters for better efficiency. However, this increases the area and component cost of a printed circuit board (PCB).

Because direct radio frequency (RF) sampling data converters can generate or sample a signal directly in the RF frequency domain, the sampling rates are in the RF frequency spectrum. This leads to more current consumption because of the increase in the dynamic power dissipation. From literature, dynamic power consumption (P) is directly proportional to frequency (f), voltage (V), and capacitance (C) by:

$$P = C \times V^2 \times f \quad (1)$$

An LDO-only power solution will lead to less efficiency and more waste of power caused by high current flowing through the finite on-resistance of the pass transistor inside the LDO. This is not desirable in applications like a wireless base station, where the total power consumption is a key consideration. Also, the reduced power efficiency leads to the PCB heating up and creating a big challenge to the thermal engineer to effectively dissipate the excess heat without damaging the PCB.

This TI Design shows a more efficient power supply scheme to power-up Texas Instruments' (TI) RF sampling digital-to-analog data converter (DAC38RF8x) without sacrificing performance. This design uses both DC/DC switchers and an LDO to power up the DAC38RF8x for the best analog performance (spurious and phase noise) and best power efficiency trade-off. The design method outlined here can be extended to power supply design of other RF sampling data converters.

1.1.1 DAC38RF8x: JESD204B 9-GSPS High-Speed DAC

The DAC38RF8x are a family of high-performance 8-, 12-, or 14-bit, 9.0-GSPS interpolating digital-to-analog converters (DACs), capable of synthesizing wideband signals from 0 to 4 GHz in the first Nyquist zone and up to 6 GHz in the second Nyquist zone. A high dynamic range allows the DAC38RF8x to generate 2G/3G/4G signals for wireless base stations for all 3GPP bands, including simultaneous generation of multiple bands. The devices have a low-power, 8-lane JESD204B interface with a maximum bit rate of 12.5 Gbps. The full output rate is achieved by using interpolation filters, after which the signal can be upconverted to RF using a digital NCO (with a 48-bit resolution) and digital quadrature modulator. Two signals can be tuned to different frequencies and digitally combined, allowing wide output spectrums. An optional low jitter PLL/VCO simplifies the DAC clock generation by allowing use of a lower frequency reference clock.

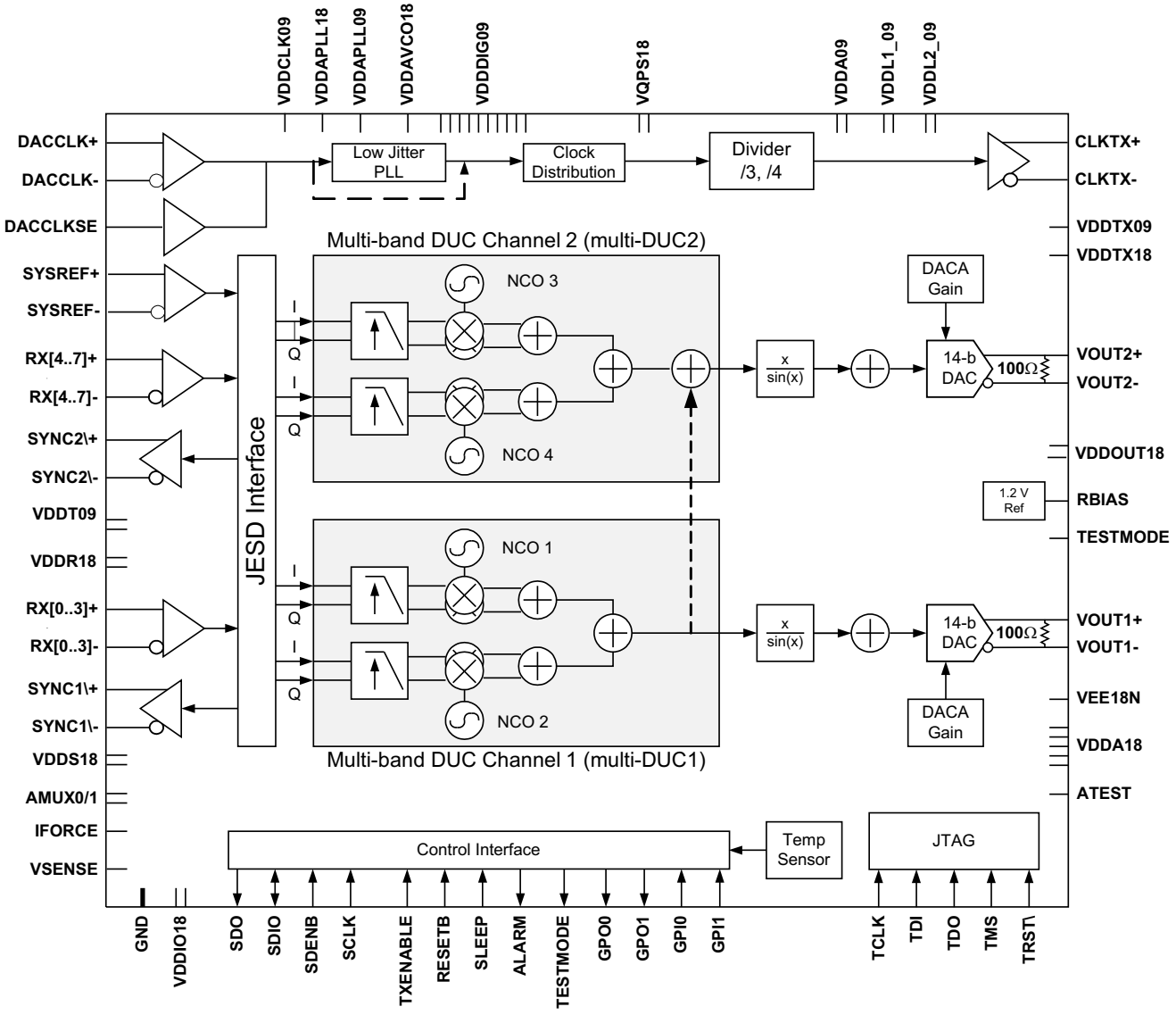


Figure 1. Internal Block Diagram of DAC38RF8x

1.1.2 Power Supply Domains in DAC38RF8x

Internally, the DAC38RF8x comprises a digital subsystem, an analog subsystem, and a clock subsystem. Ideally, the power supply scheme must be partitioned according to these three relatively independent blocks to minimize interactions between them. Most importantly, sensitive analog and clock circuit power supply must be separated from digital switching noise to reduce direct coupling and mixing of switching spurs. Table 1 shows the detailed power rail for the DAC38RF8x grouped under their respective power domains.

Table 1. Definition of DAC38RF8x Power Rails

NAME	VOLTAGE	DESCRIPTION
DIGITAL SUPPLY DOMAIN		
VDDIG1	1.0 V	Digital supply voltage for internal digital block
VDDIO18	1.8 V	All digital I/O and CMOS I/O supply voltage
VDDR18	1.8 V	SerDes supply voltage
VDDS18	1.8 V	LVDS SYNC0/1 supply voltage
VDDT1	1.0 V	SerDes termination supply voltage
VDDE1	1.0 V	Digital supply voltage for DAC core
VDDL1_1	1.0 V	DAC core supply voltage
ANALOG SUPPLY DOMAIN		
VEE18N	–1.8 V	Analog supply voltage
VDDA1	1.0 V	Analog supply voltage
VDDA18	1.8 V	Analog supply voltage
VDDOUT18	1.8 V	DAC output supply
CLOCK SUPPLY DOMAIN		
VDDPLL1	1.0 V	Analog supply voltage for PLL
VDDAPLL18	1.8 V	Analog supply voltage for PLL
VDDAVCO18	1.8 V	Analog supply voltage for VCO
VDDCLK1	1.0 V	Internal clock buffer supply voltage
VDDL2_1	1.0 V	DAC core supply voltage
VDDTX1	1.0 V	Divided clock output supply voltage
VDDTX18	1.8 V	Divided clock output supply voltage

- VDDE1, VDDL1_1, and VDDL2_1 are the power supplies for the encoder stage between digital and analog blocks.
- The most sensitive DAC supplies are in the clock domain and include the following: VDDCLK1, VDDL2_1, VDDPLL1, VDDAPLL18, and VDDAVC018 (the latter three if the internal DAC PLL is active). If the divided clock output is used, the supply voltage for it, VDDTX1 and VDDTX18, should also be considered as sensitive power rails.
- In addition to the primary concern of coupling into the clock domain-related supplies, another concern is about coupling into the analog domain-related supplies: VEE18N, VDDA18, VDDA1, and VDDL1_1. However, this would be to a lesser extent because of relatively higher supply rejection in the analog domain compared to the clock domain.

To achieve the high performance expected of the DAC38RF8x, the revision D of the evaluation module (EVM) by default uses LDOs to directly power up all the power rails as shown in Figure 2.

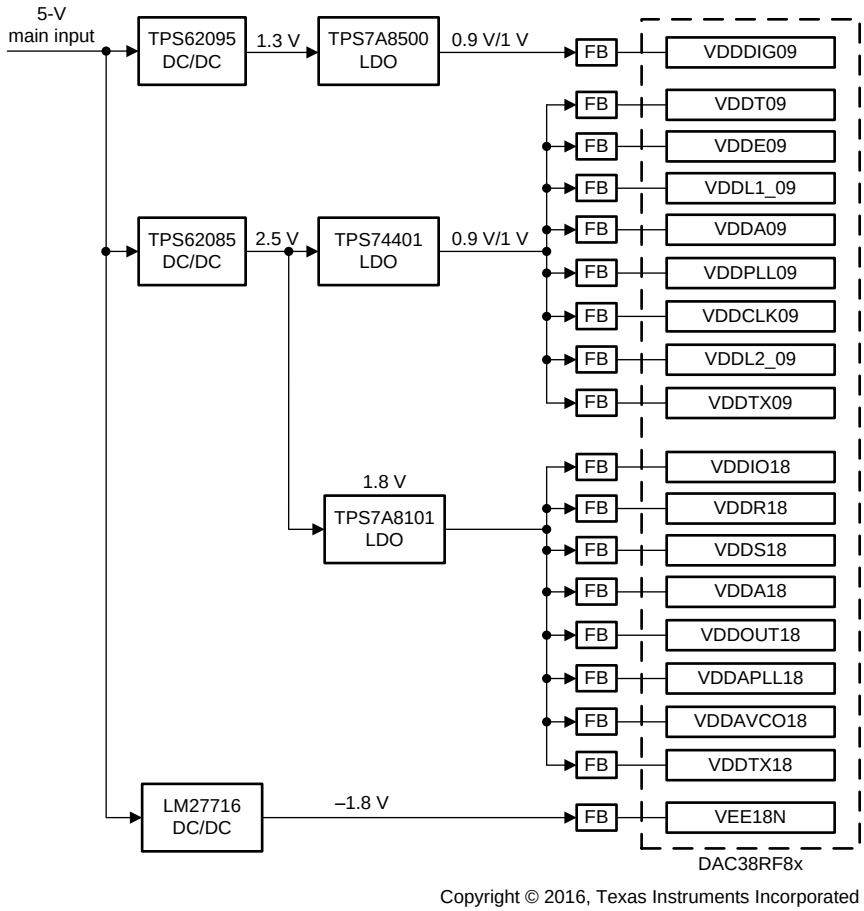


Figure 2. Default Power Tree of DAC38RF8x

From Figure 2, the main digital domain power supply rail, the VDDDIG1, uses a dedicated DC/DC+LDO to power it. This helps to achieve better isolation between this rail and other power rails and to avoid any spur coupling between rails.

Also, for each other power rail, a feedthrough capacitor or ferrite bead (FB) is used to isolate it from all other power rails of the DAC. Two groups of bypass capacitors are also placed close to the power supply device (LDO) and also close to the DAC supply pin to filter high frequency noise and spurs.

This default power supply scheme will be optimized for both efficiency, area and performance in the rest of this document.

1.2 Highlighted Products

1.2.1 DAC38RF80 and DAC38RF83

For more information on these devices, view their respective datasheet at www.TI.com.

2 System Design Theory

2.1 Power Consumption

Table 2 gives the measured power consumption for each rail at various modes of operation. An external sampling clock was used for these measurements. All current values are in milliamperes.

Table 2. DCA38RF8x Power Consumption

MODE (LMFSHd)	NO OF TX	MAX FDAC	INTP	VDDTX	VDDR	VDDE	VDDT	VDDL1	VDDCLK	VDDPLL18	VDDPLL09	VDIG09	VDDOUT18	VEE	VDDVCO18*	VDD L2	VDDA09	VDDA18	TOTAL POWER (mW)
—	—	—	—	1.8	1.8	1	1	1	1	1.8	1	1	1.8	1.8	1.8	1	1	1.8	—
81180	1 TX	9000	1	14	62.0	343	307	21	222	18	30	444	98.0	152.0	0	21	19	45	2058.6
41380	2TX	3333	1	14	66.0	221	322	16	154	18	14	501	98.0	152.0	0	15	19	45	1920.8
41380	2TX	6666	2	14	66.0	429	322	32	306	18	23	821	98.0	152.0	0	29	19	45	2639.8
41121	2TX	2500	1	14	66.0	173	324	12	116	18	13	469	98.0	152.0	0	12	19	45	1796.8
41121	2TX	5000	2	14	66.0	334	323	24	228	18	19	735	98.0	152.0	0	22	19	45	2362.8
41121	2TX	9000	4	14	62.0	576	306	42	402	18	30	1017	98.0	152.0	0	39	19	45	3082.6
82121	1TX	9000	6	14	75.0	380	338	21	222	18	30	907	98.0	152.0	0	21	19	45	2613.0
82121	1TX	9000	8	14	62.0	379	289	21	222	18	30	824	98.0	152.0	0	21	19	45	2456.6
82121	1TX	9000	12	14	75.0	379	327	21	222	18	30	805	98.0	152.0	0	21	19	45	2499.0
82121	1TX	9000	16	14	62.0	379	281	21	222	18	30	328	98.0	152.0	0	21	19	45	1952.6
42111	2TX	7500	6	14	66.0	517	323	35	341	18	26	1425	98.0	152.0	0	33	19	45	3377.8
42111	2TX	9000	8	14	62.0	627	307	42	402	18	30	1542	98.0	152.0	0	39	19	45	3661.4
42111	2TX	9000	10	14	86.0	624	371	42	402	18	30	1580	98.0	152.0	0	39	19	45	3801.8
42111	2TX	9000	12	14	75.0	625	336	42	402	18	30	1513	98.0	152.0	0	39	19	45	3681.0
42111	2TX	9000	16	14	62.0	624	288	42	402	18	30	1363	98.0	152.0	0	39	19	45	3458.6
42111	2TX	9000	18	14	58.0	625	272	42	402	18	30	1377	98.0	152.0	0	39	19	45	3450.4
42111	2TX	9000	24	14	74.0	626	325	42	402	18	30	1383	98.0	152.0	0	39	19	45	3539.2
22210	2TX	5000	8	14	46.0	358	163	24	228	18	19	903	98.0	152.0	0	23	19	45	2359.8
22210	2TX	7500	12	14	46.0	516	163	35	341	18	26	1232	98.0	152.0	0	33	19	45	2987.8
22210	2TX	9000	16	14	44.0	622	155	42	402	18	30	1340	98.0	152.0	0	39	19	45	3268.2
22210	2TX	9000	18	14	43.0	624	146	42	402	18	30	1357	98.0	152.0	0	39	19	45	3276.4
22210	2TX	9000	20	14	56.0	624	188	42	402	18	30	1462	98.0	152.0	0	39	19	45	3446.8
22210	2TX	9000	24	14	51.0	622	169	42	402	18	30	1347	98.0	152.0	0	39	19	45	3301.8
12410	2TX	5000	16	14	46.0	354	89	24	228	18	19	789	98.0	152.0	0	23	19	45	2167.8
12410	2TX	7500	24	14	46.0	512	89	35	341	18	26	1132	98.0	152.0	0	33	19	45	2809.8
44210	2TX	5000	8	14	66.0	363	323	24	228	18	19	1502	98.0	152.0	0	23	19	45	3159.8
44210	2TX	7500	12	14	66.0	522	322	35	341	18	26	2050	98.0	152.0	0	33	19	45	4006.8
44210	2TX	9000	16	14	62.0	631	306	42	402	18	30	2233	99.0	152.0	0	39	19	45	4357.2
44210	2TX	9000	24	14	75.0	629	335	42	402	18	30	2244	99.0	152.0	0	39	19	45	4416.8
24410	2TX	5000	16	14	46.0	361	163	24	228	18	19	1292	98.0	152.0	0	23	19	45	2751.8
24410	2TX	7500	24	14	46.0	521	163	35	341	18	26	1870	98.0	152.0	0	33	19	45	3630.8

Table 2. DCA38RF8x Power Consumption (continued)

MODE (LMFSHd)	NO OF TX	MAX FDAC	INTP	VDDTX	VDDR	VDDE	VDDT	VDDL1	VDDCLK	VDDPLL18	VDDPLL09	VDIG09	VDDOUT18	VEE	VDDVCO18*	VDD L2	VDDA09	VDDA18	TOTAL POWER (mW)
24310	2TX	9000	24	14	44.0	628	154	42	402	18	30	2141	98.0	152.0	0	39	19	45	4074.2

*VCO_18 current = 40mA (for the 9GHz PLL) and 21mA (6GHz PLL)

2.2 Spur Transfer Model From Power Supply Rail to DAC Output

Coupling from the power supply to the DAC output can occur in two main ways as illustrated in Figure 3:

- Spur f_2 (can also be noise) showing up at the power supply pin will be mixed with the DAC RF output frequency f_1, and then generate sideband spurs around the main output frequency.
- The power supply spur or noise can directly feed through to the DAC output.

The level of spur or noise from the power supply that shows up at the output is measured by the power supply rejection ratio (PSRR).

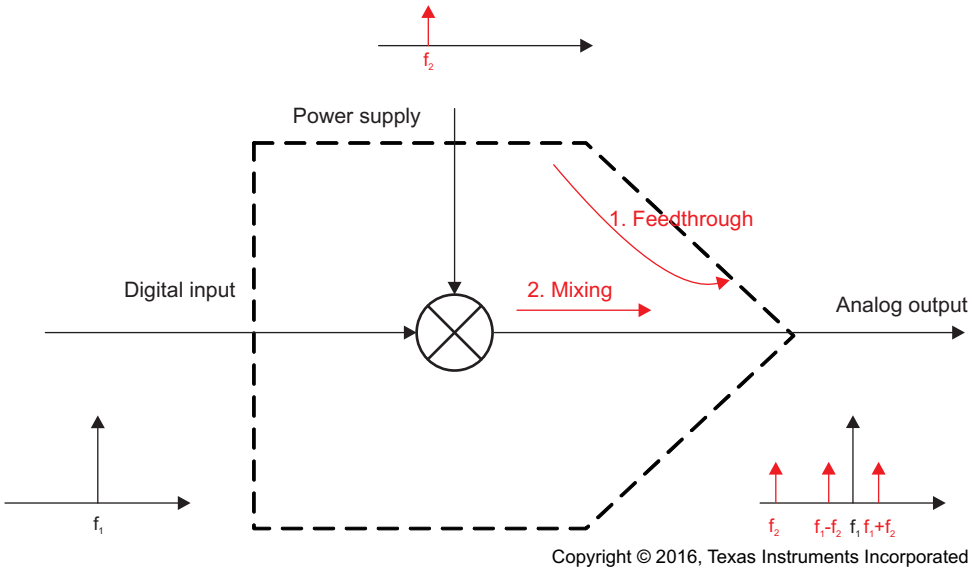


Figure 3. Spur Transfer Model of Power Supply to DAC Output

2.3 PSRR Measurement on DAC38RF8x

Measuring the PSRR of the DAC38RF8x involves injecting a ripple of known frequency and amplitude at the DAC power supply pin. The spectrum of the DAC output can subsequently be analyzed to determine the power level of the injected spur at the output.

2.3.1 Ripple Injection on VDDCLK1 Power Supply

All clock-related and analog-related power rails are the most sensitive to power supply noise and spurs. Spurs at the power supply rail will show up as double-side bands at the DAC output (or mix with the signal at the DAC output) as described in Figure 3. In order to characterize the spur suppression performance of VDDCLK1, the setup in Figure 4 is used to inject a known ripple to this rail.

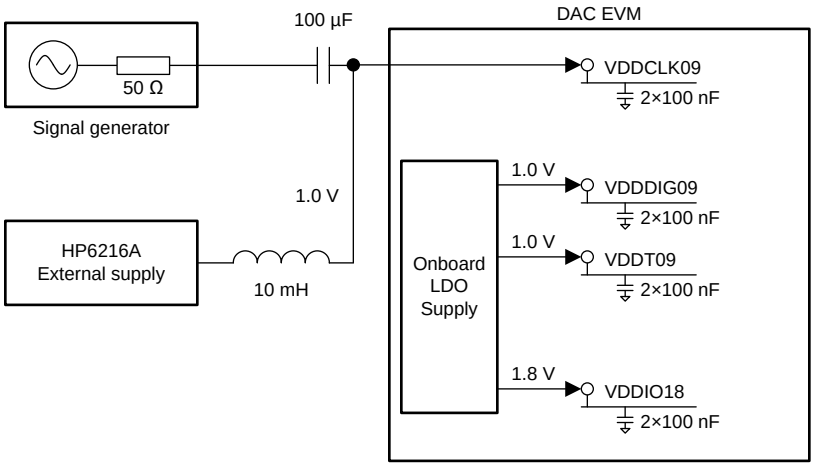


Figure 4. Setup for Ripple Injection Measurement

On the DAC38RF8x EVM, the PSRR of VDDCLK1 rail is performed as follows:

- The ferrite bead in series with VDDCLK1 is removed, and VDDCLK1 is powered from external bench power supply (HP6216A). All other power rails are powered by default onboard regulators.
- A signal generator is used to generate a sine wave of known frequency and subsequently injected to the VDDCLK1 power net through a "large" 100-µF DC blocking capacitor. Also bulk capacitors that are greater than 1 µF are removed to avoid low load impedance, which is seen by signal generator. Only small value, local decoupling capacitors at each power supply rail are kept.
- Set up DAC38RF8x to output a single tone at 1 GHz with a power of 1.38 dBm.
- Sweep the signal generator output frequency from 100 kHz to 2.5 MHz. At each frequency step, measure the peak-to-peak voltage ripple at the VDDCLK1 pin and adjust the signal generator amplitude so that the injected ripple amplitude is 40 mVpp at the pin. Figure 5 shows the DAC output spectrum when the injected ripple frequency is set to 500 kHz. Notice the sidebands at ±500-kHz offset from the output tone at 1 GHz.

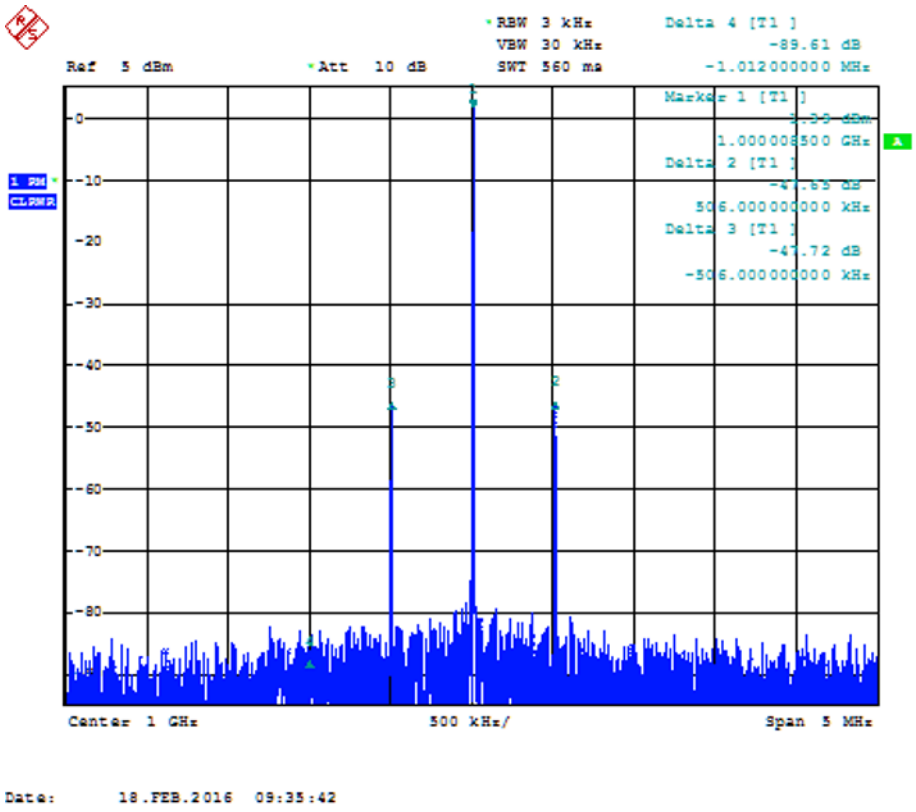


Figure 5. DAC Output Single Tone Spectrum at 1 GHz

- At each frequency step, measure the sideband spur power level relative to the power of the tone at 1 GHz.

Figure 6. Spur Suppression at VDDCLK1 versus Injected Ripple Frequency

2.3.1.1 Supply Rejection and DAC Output Frequency Relationship

The previous tests used an output tone at 1 GHz from the DAC38RF8x to estimate the power supply rejection. The dependency of the supply rejection on the DAC output frequency is investigated next.

1. Set the signal generator used to inject ripple to output a 500-kHz sine wave with a swing of 1200 mVpp (this level ensures the voltage at DAC VDDCLK09 supply pin is 40 mVpp).
2. Keep the DAC output power constant at 1.38 dBm CW tone and sweep the output frequency from 250 to 3500 MHz.
3. Measure the spur suppression in dBc at each frequency step.

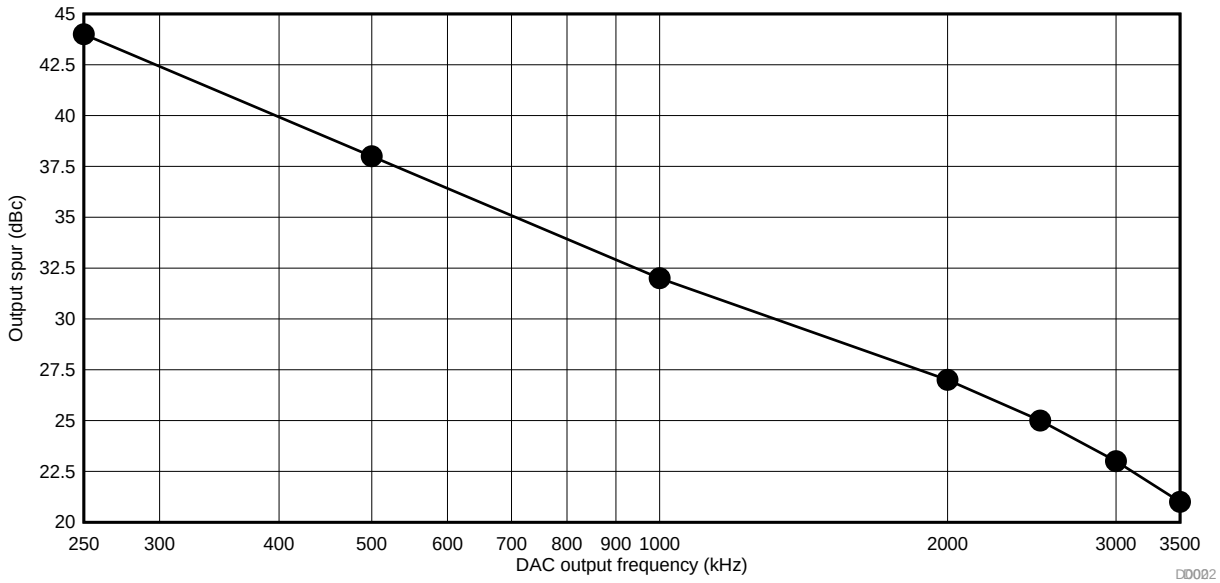


Figure 7. Spur Suppression Across DAC Output Frequency

The –20 dB/decade slope shows that the spur level (in dBc) is linearly dependent on the DAC output frequency. Consequently, doubling the DAC output frequency degrades the supply rejection by 6 dB. This phenomenon is similar to the relationship between the sampling clock frequency/phase noise and the DAC output frequency/phase noise [see *Effects of Clock Noise on High-Speed DAC Performance* (SLAA566). Consequently, since VDDCLK 1.0-V power rail is used to power the clock distribution circuits (and switching array at the analog output) any spur at this rail will couple directly to the sampling clock and show up as sidebands at the DAC output.

2.3.1.2 Supply Rejection and DAC Output Power Relationship

The following steps show how the DAC output power level is reached.

1. Set the signal generator to output a 500-kHz sine wave with a swing of 1200 mVpp.
2. Set DAC to output a single tone at 1 GHz.
3. Sweep the DAC output tone power from –21d to 0 dBFs with a step of 3 dB (take 1.38 dBm as 0 dBFs).
4. Measure the spur suppression at the DAC output (in dBc).

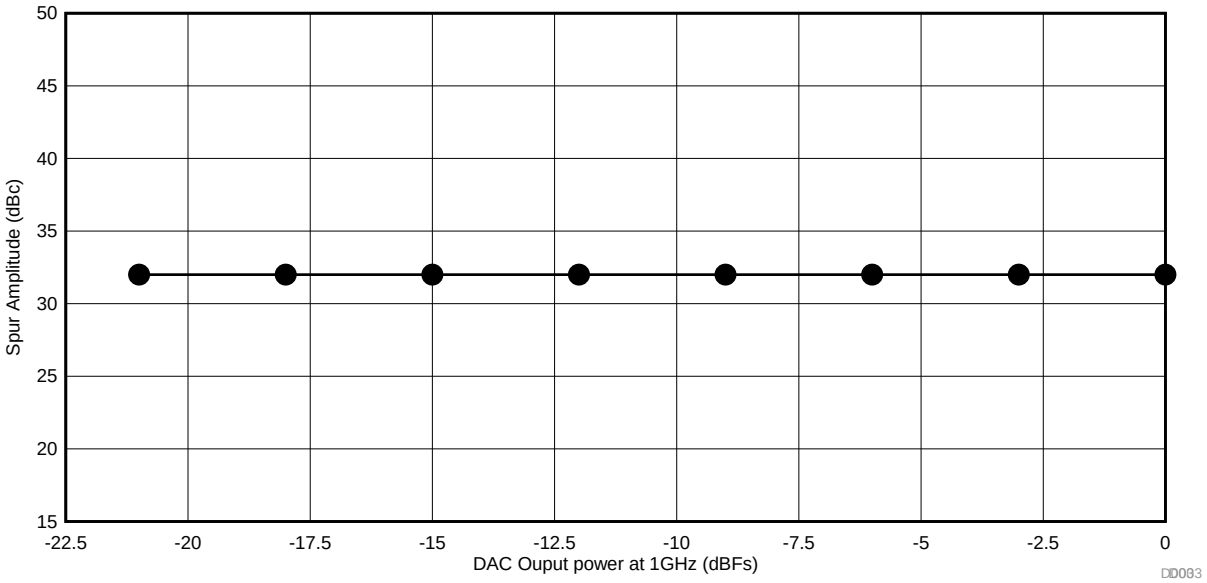


Figure 8. Spur Suppression Across DAC Output Tone Power

The spur level in dBc stays constant as the DAC output power level is varied.

2.3.2 Ripple Injection on VDDA1 and VDDPLL1

Similar to the results discussed for the VDDCLK1 power rail, the ripple injection performance of VDDA1 and VDDPLL1 power rails are also measured. The results are shown in Figure 9:

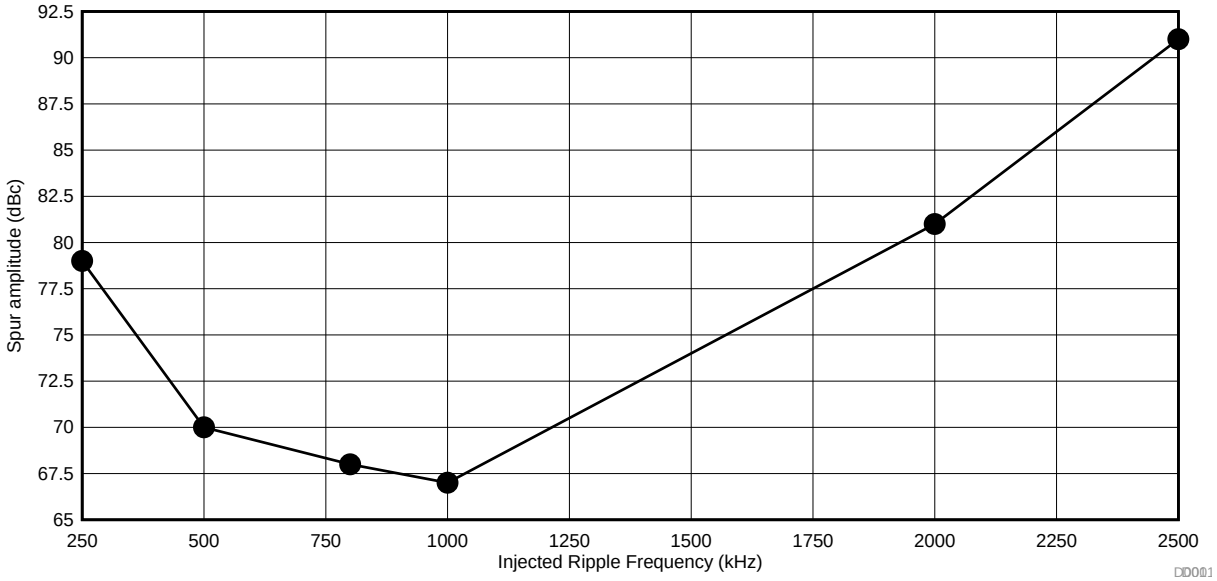


Figure 9. Spur Suppression at VDDA1 versus Injected Ripple Frequency

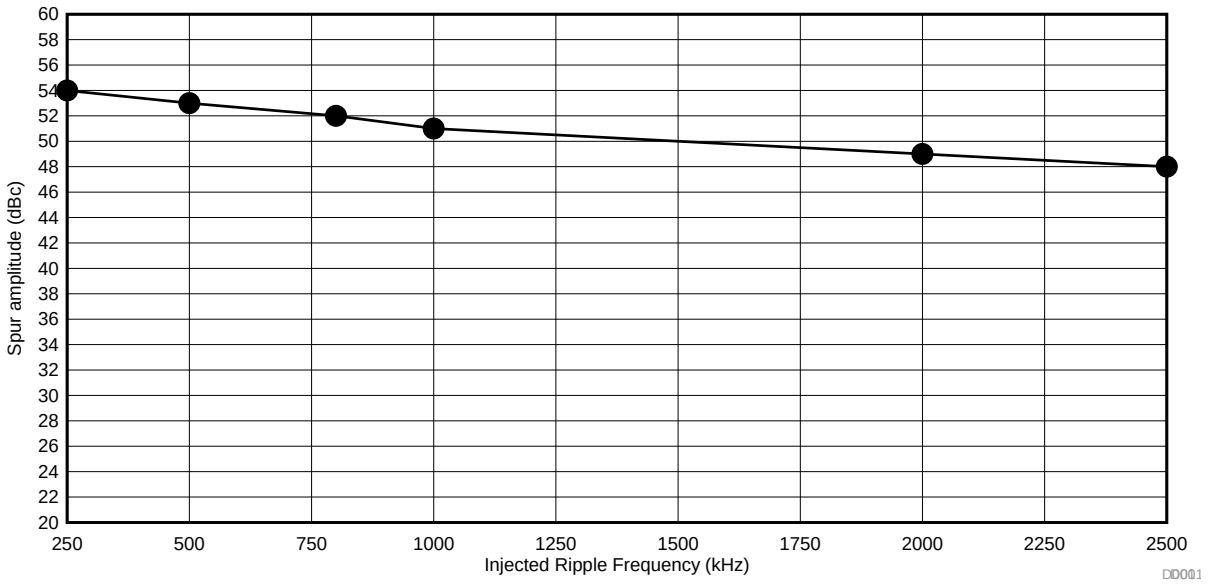


Figure 10. Spur Suppression at VDDPLL1 versus Injected Ripple Frequency

The average spur suppression of VDDA1 and VDDPLL1 rails is about 80 dBc and 50 dBc, respectively. Compared to the average spur suppression of 32 dBc of the VDDCLK1, both the VDDA1 and VDDPLL1 are less sensitive to the same level of injected ripple.

3 Power Supply Scheme and Performance

Based on the power supply rejection results obtained in Section 2, a new DC/DC converter based power scheme is proposed as shown in Figure 11.

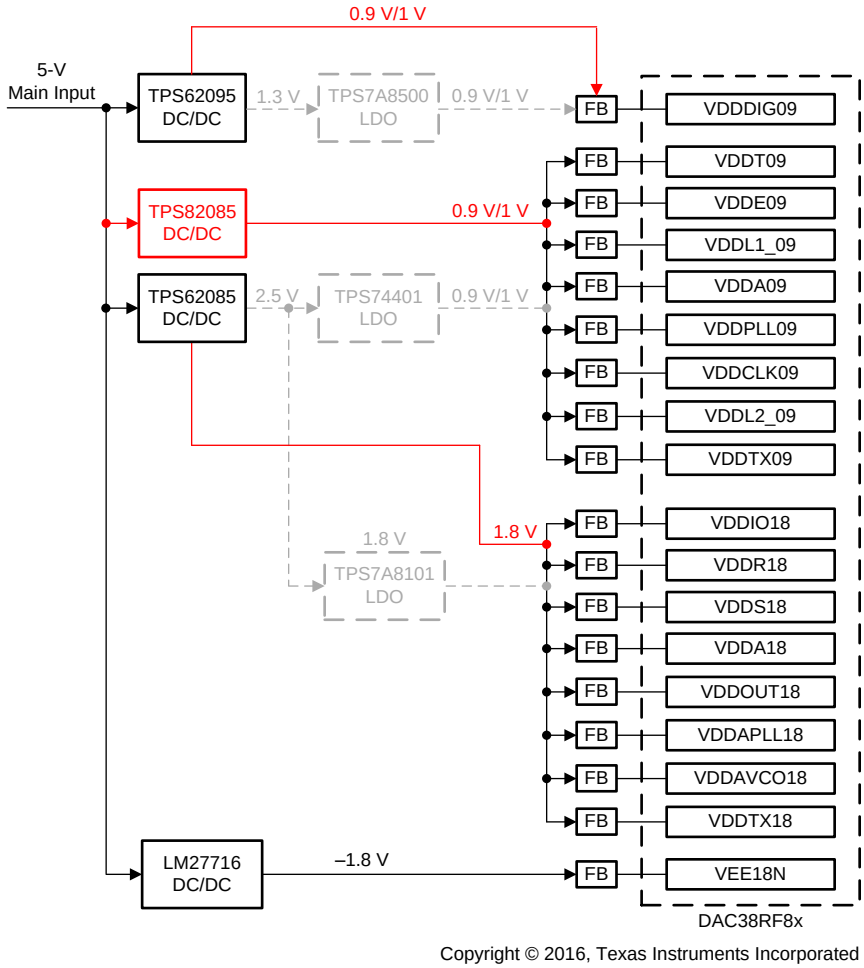


Figure 11. Modified Power Tree for All DC/DC Power Solution

The following subsections will compare the spurious and phase noise performance of the DAC for the power supply schemes in Figure 11 and Figure 2.

3.1 Required Hardware

- DAC38RF8x EVM Rev D (or higher)
- Signal generator used to provide sampling clock to DAC
- Phase noise analyzer (example is the Keysight E5052A)
- External bench power supply (example is HP6216A)

3.1.1 DAC38RF8x EVM Setup

See the *DAC38RF8x-EVM User's Guide* (SLAU671) for details.

3.2 Required Software

The DAC38RF8x EVM GUI (SLAC722) is required. The DAC38RF8x EVM GUI is used to control and program the onboard DAC38RF8x and onboard LMK04828.

4 Testing and Results

Follow this step-by-step guide to output a single tone at 1 GHz from DAC Channel A:

1. Connect jumper JP10 of DAC38RF8x EVM.
2. Apply a 5-V power supply to connector J21 of the DAC38RF8x EVM. LED D11 will turn green when power is provided.
3. Use USB 2.0 type B cable to connect PC with J16 of the DAC38RF8x EVM.
4. Connect external 5898.24-MHz/16-dBm clock from the signal generator to J1 SMA input of the DAC38RF8x EVM.
5. Launch the DAC38RF8x EVM GUI. Click the "Reconnect FTDI?" button on the top-right side to establish the link between the PC and DAC38RF8x EVM onboard FTDI chip.
6. Toggle the "Not in RESET" button by twice to reset the DAC38RF8x. Click the "LOAD DEFAULT" button to load the DAC38RF8x and LMK04828 default register values.
7. Set the value as shown in Figure 12, then click on "CONFIGURE DAC" to configure the DAC38RF8x according to the setting just completed.

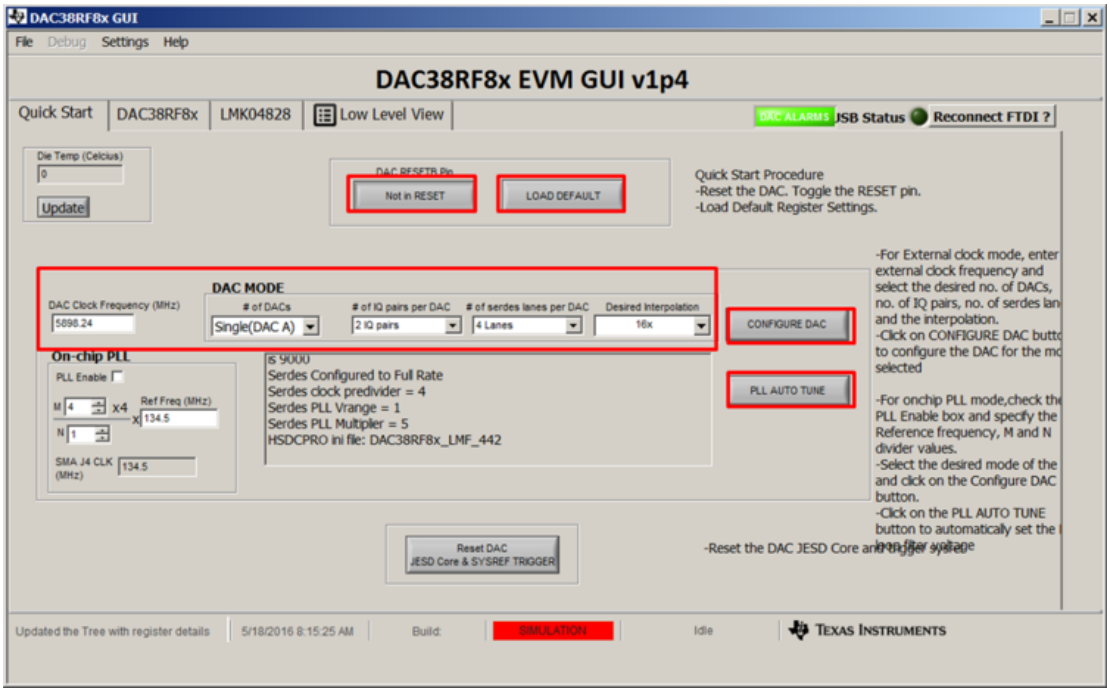


Figure 12. Quick Start Page of GUI

8. Click on "Reset DAC JESD Core & SYSREF TRIGGER".

9. Set the "Digital(DAC A)" tab as in Figure 13. One NCO is enabled with frequency setting of 1000 MHz. Enable constant input data block and set the value to 0x5A73, which is –3 dB back off from the full scale to avoid digital saturation. Click on "UPDATE NCO" to re-sync the NCO output.

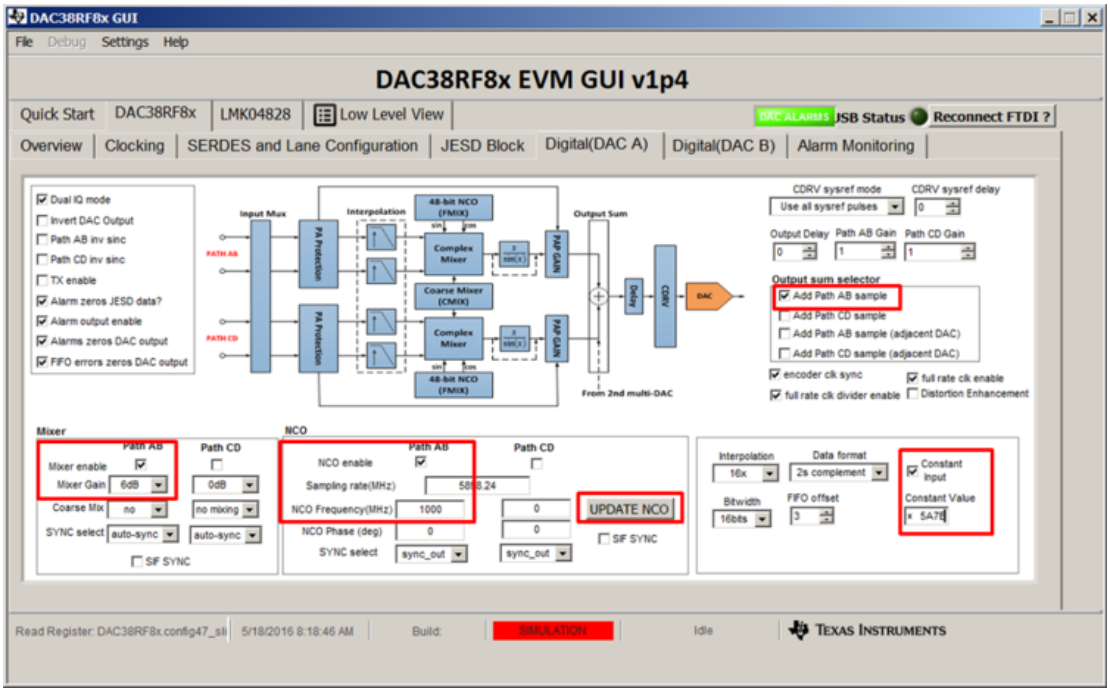


Figure 13. Digital Setting of DAC A

4.1 Test Data

4.1.1 Spur Performance

This section discusses the spur performance of the DAC38RF8x powered by only DC/DC switchers (see Figure 11). This document treats spur performance of the DAC38RF8x with all the power rails powered by LDOs as the baseline (Figure 2).

The spur contribution at the DAC output from the sampling clock (generated from Keysight E4438C signal generator) is measured. This is shown in Figure 14.

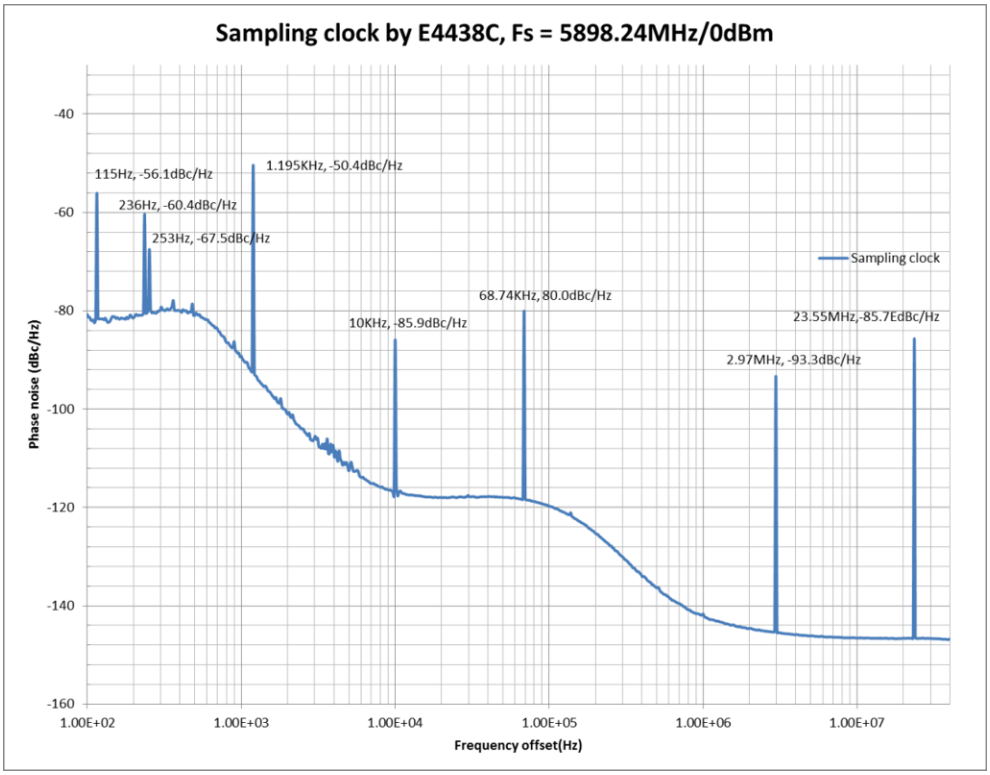


Figure 14. Spur Performance of External Sampling Clock From Signal Generator (E4438C)

The DAC38RF8x EVM (REV D) default power scheme is shown in Figure 2. Using this scheme and the sampling clock (Figure 14) to drive DAC38R8x, the resulting output tone spurious performance (from 100-Hz to 40-MHz offset) is shown in Figure 15.

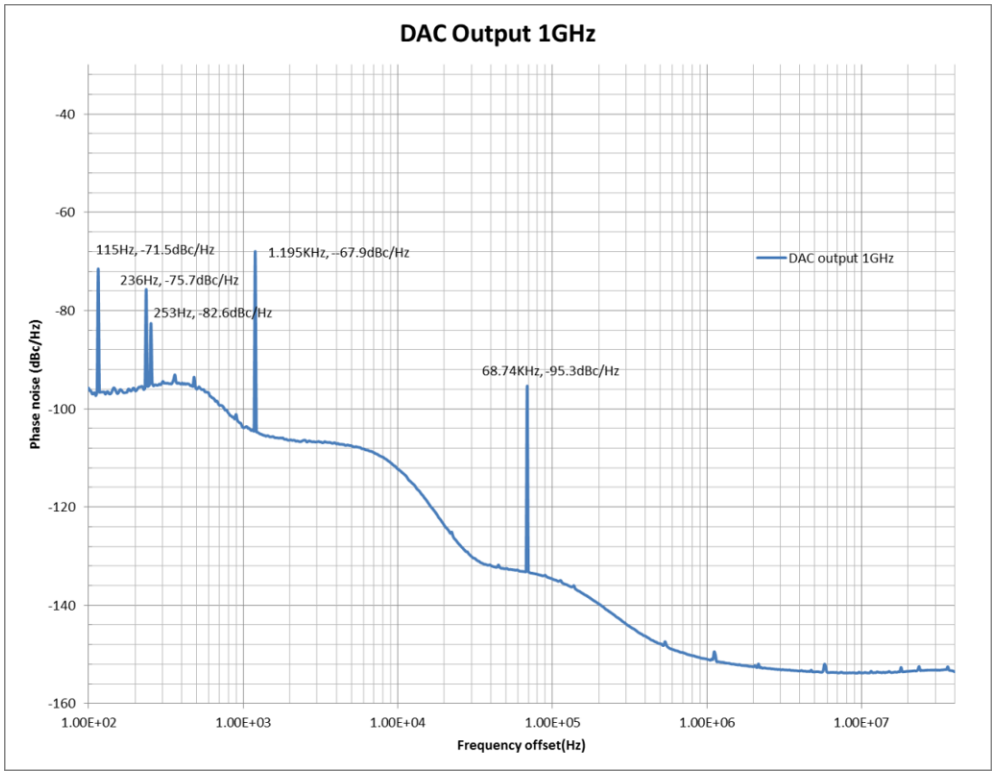


Figure 15. Spur Performance of DAC Output at 1GHz Under Default All LDO Power Solution

All the spurs marked out are from the sampling clock and the DAC itself does not generate any new spurs. This is treated as our baseline (or reference) spurious performance.

The power supply scheme is then modified to Figure 11 (all the power rails are powered from DC/DC switchers). Using this scheme and the sampling clock (Figure 14) to drive DAC38R8x, the resulting output tone spurious performance (from 100-Hz to 10-MHz offset) is shown in Figure 16.

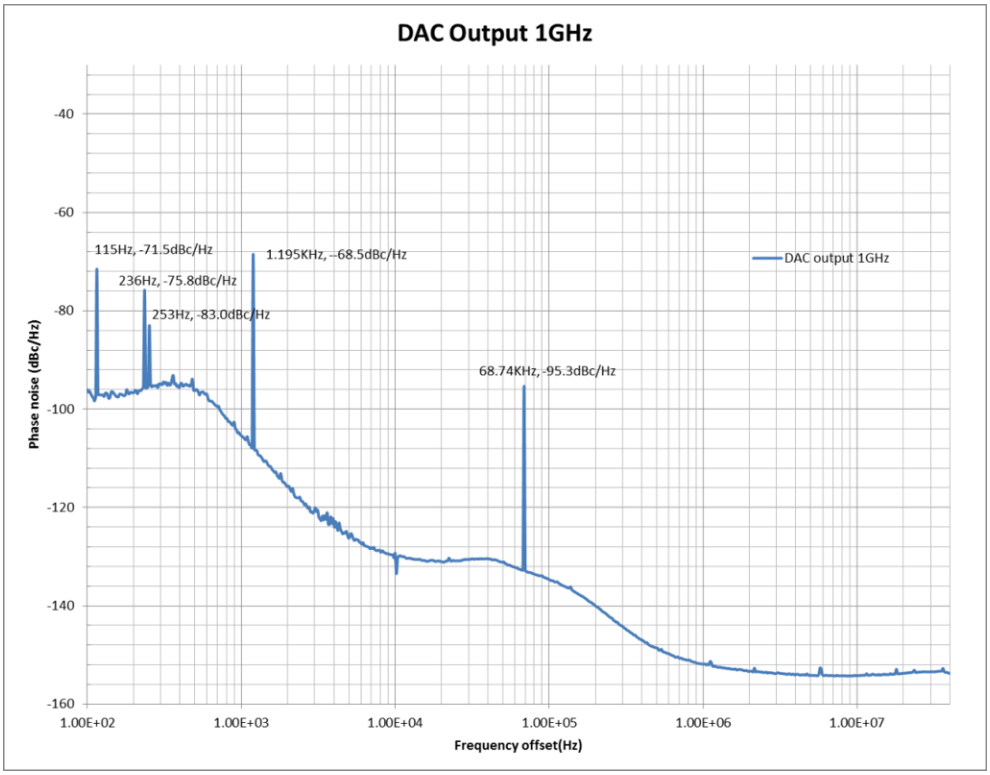


Figure 16. Spur Performance of DAC Output at 1 GHz Under Modified All DC/DC Power Solution

For this DC/DC switcher power supply scheme, all the spurs marked out are also from the sampling clock and compared to the baseline performance (Figure 15), the spur locations and amplitudes are the same. Hence the all DC/DC power supply solution does not degrade the spurious performance of the DAC.

4.1.2 Phase Noise Performance

Besides the spur performance, the phase noise performance of DAC under the all DC/DC power scheme is investigated. Any noise induced from the power supply will also be mixed to the DAC output.

By using the power tree scheme in Figure 2, DAC output phase noise at the 1-GHz output tone is measured (Figure 17) to establish the baseline performance. The jitter performance is calculated by integrating the phase noise from the 1-kHz offset to 20 MHz. This results in a measured RMS jitter of 38.854 fs.

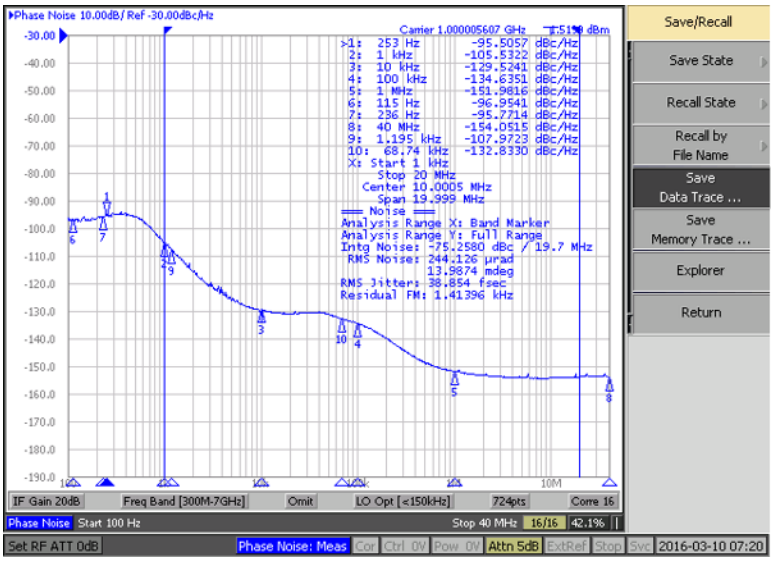


Figure 17. Phase Noise of DAC Output at 1 GHz Under Default All LDO Power Solution

By using the modified power tree scheme in Figure 11, the corresponding phase noise can also be measured (Figure 18). With this DC/DC power solution, the phase noise plot shows up a hump from a 1- to 30-kHz offset, which leads to a degraded RMS jitter of 91.416 fs.

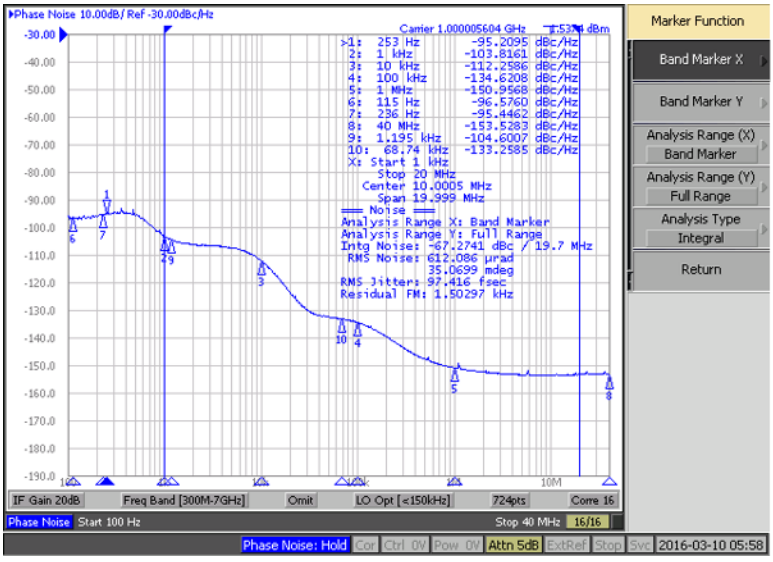


Figure 18. Phase Noise of DAC Output at 1 GHz Under Modified All DC/DC Power Solution

To eliminate the hump caused by the noise from DC/DC switcher, an external linear power module HP6216A is used to power up the VDDCLK1 (this was shown to be the most sensitive rail in Section 2). The resulting power scheme is shown in Figure 19.

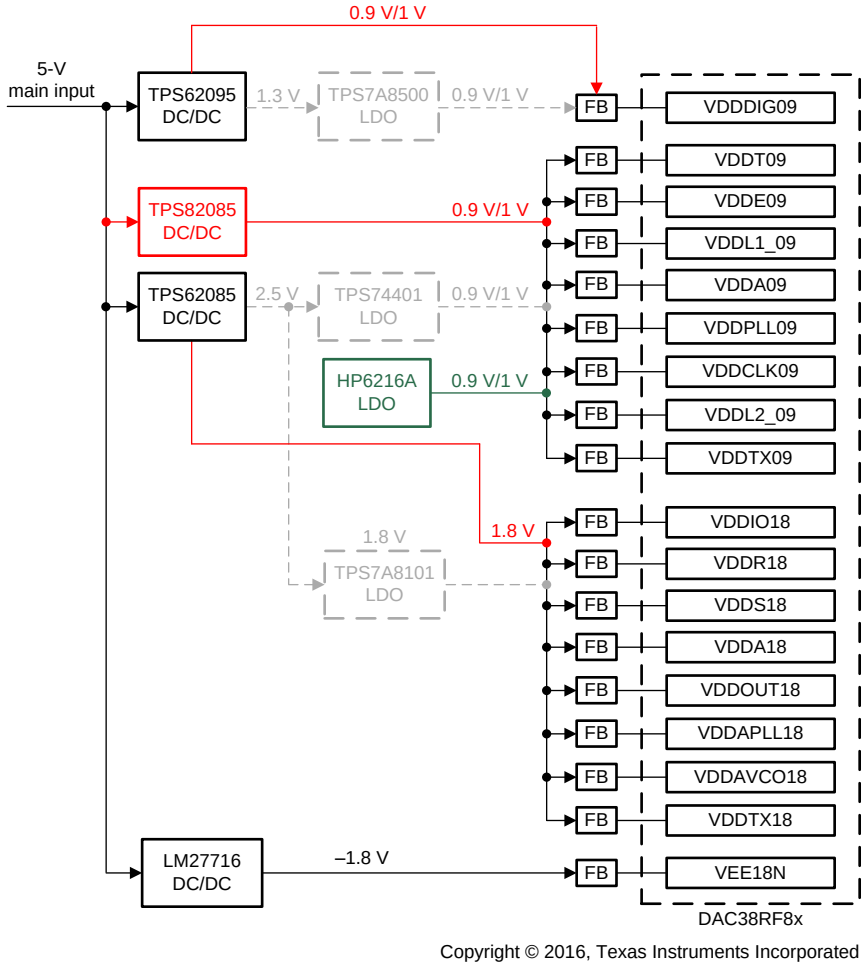


Figure 19. Modified Power Tree for DC/DC+LDO Power Solution

Figure 20 shows the phase noise performance improved when the VDDCLK1 was powered from the HP6216A source. The measured RMS jitter at 1 GHz is 38.104 fs, which is almost the same as the result for the baseline performance (Figure 17).

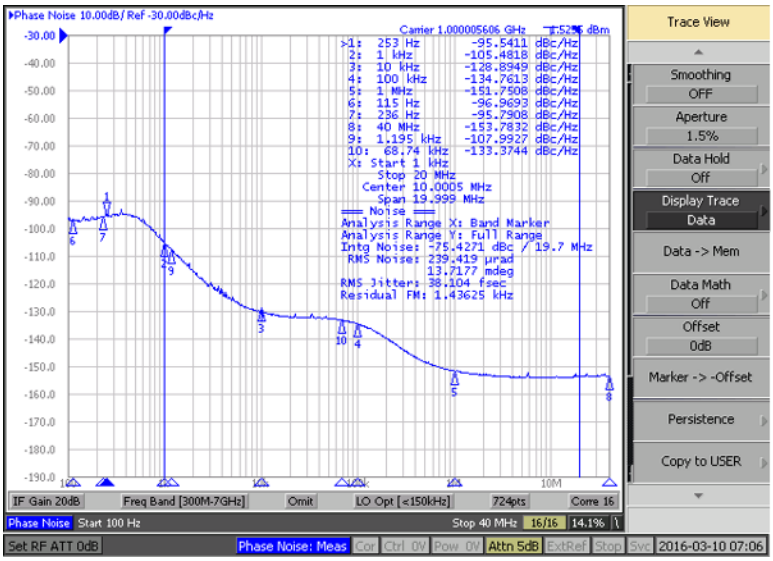


Figure 20. Phase Noise of DAC Output at 1 GHz Under Modified DC/DC+LDO Power Solution

Finally, Figure 21 compares the phase noise curve between power scheme in Figure 19 and the baseline Figure 2.

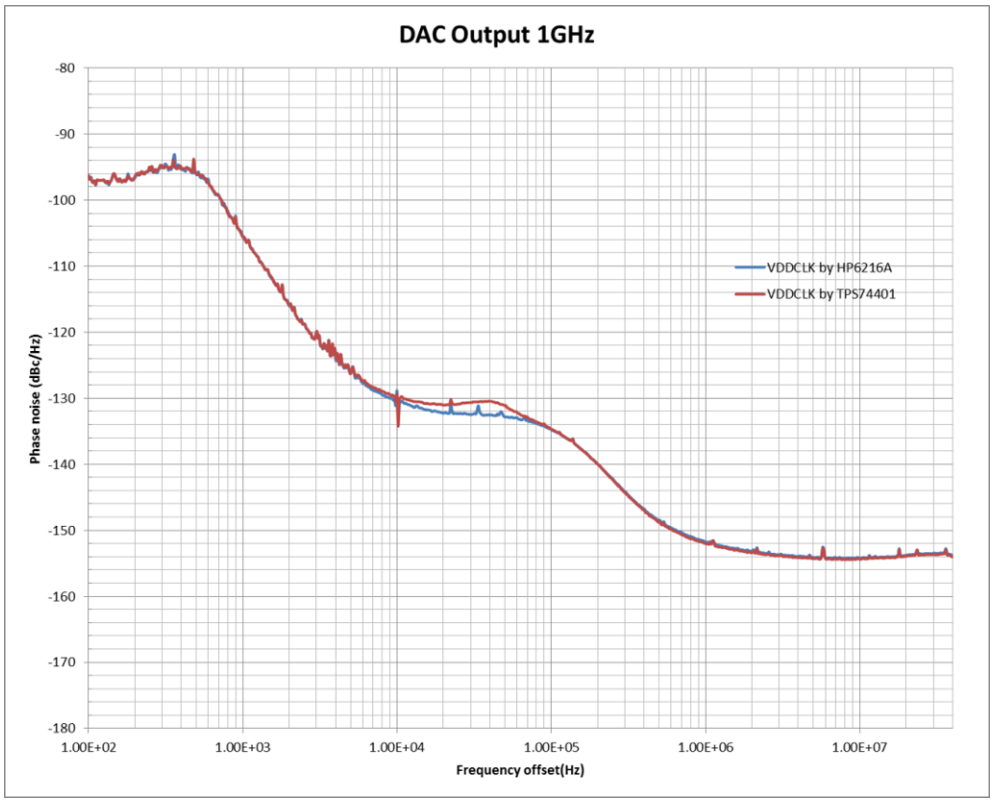


Figure 21. Phase Noise of DAC Output at 1-GHz Comparison Between Modified DC/DC+LDO Power Solution and All LDO Power Solution

The phase noise performance of powering up the VDDCLK1 by HP6216A is a little bit better than the onboard LDO TPS74401. Considering that this difference is small, for optimal output phase noise and power efficiency, an LDO can be used to power up the VDDCLK1 and DC/DC switchers can be used to power up all the other power rails.

4.1.3 On-chip PLL mode

The results above for the power supply scheme were obtained using external clock as the sampling clock. When using the on-chip PLL as the sampling clock a slightly modified power supply scheme is recommended. This modified supply requires an LDO for the 1.8V supply rails due to the sensitivity of the VCO_1.8V rail to power supply noise. The modified power supply scheme suitable for on-chip PLL mode is shown in Figure 22 This modified scheme uses a low noise LDO for all the 1.8V rails.

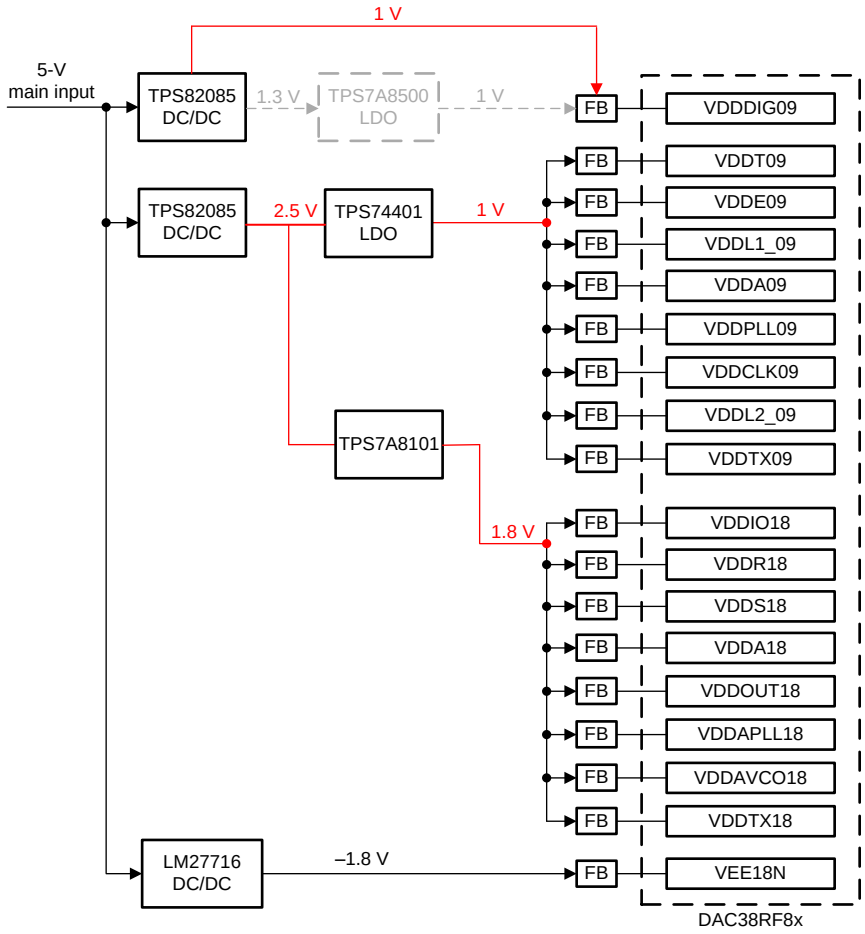


Figure 22. Recommended power supply scheme for On-chip PLL mode

4.2 Conclusion

This reference design mainly discusses the implementation of different power schemes for DAC38RF8x, a high-speed RF sampling digital to analog converter. Output signal phase noise and spurs are the two key performance metrics used to compare different power supply schemes in this reference design.

The following conclusions are made from the measured results:

- In order to achieve optimal phase noise performance, supply VDDCLK1 with a low-noise LDO (like TPS74401 or TPS7A8300), and power up all the other power rails with DC/DC switchers. An example is shown in Figure 19. Note that the DAC38RF8x EVM revision E and latter implements this power supply scheme.
- If the end application can tolerate the phase noise degradation caused by powering VDDCLK1 with a switcher, all the power rails can be powered up by DC/DC regulators as shown in Figure 10. This power supply scheme provides the best power efficiency.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01215.

5.2 Bill of Materials

To download the bill of materials, see the design files at TIDA-01215.

5.3 PCB Layout Recommendations

5.3.1 Layout Plots

To download the layout plots, see the design files at TIDA-01215.

5.4 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01215.

6 Software Files

To download the software files, see the design files at TIDA-01215.

7 Trademarks

All trademarks are the property of their respective owners.

8 Terminology

DAC— Digital-to-analog converter

PSRR— Power supply rejection ratio

RF— Radio frequency

LDO— Low dropout voltage regulator

9 About the Authors

YARN GUO is an analog field applications engineer at Texas Instruments (TI) serving the Shenzhen, China area. After he earned his MSEE from South China University of Technology in 2015, he went through TI's Analog Rotational Program under High Speed Products and supported various high-speed ADCs and DACs. Yarn is an active member of the TI E2E™ Community and can be reached through e2e.ti.com for support.

EBENEZER DWOBENG is an applications engineer at Texas instruments. His primary focus is on high-speed data converters and end applications in wireless infrastructure. He can be contacted through e2e.ti.com.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ('TI") reference designs are solely intended to assist designers ("Designer(s)") who are developing systems that incorporate TI products. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.

TI's provision of reference designs and any other technical, applications or design advice, quality characterization, reliability data or other information or services does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such reference designs or other items.

TI reserves the right to make corrections, enhancements, improvements and other changes to its reference designs and other items.

Designer understands and agrees that Designer remains responsible for using its independent analysis, evaluation and judgment in designing Designer's systems and products, and has full and exclusive responsibility to assure the safety of its products and compliance of its products (and of all TI products used in or for such Designer's products) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to its applications, it has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any systems that include TI products, Designer will thoroughly test such systems and the functionality of such TI products as used in such systems. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

Designers are authorized to use, copy and modify any individual TI reference design only in connection with the development of end products that include the TI product(s) identified in that reference design. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of the reference design or other items described above may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS AND OTHER ITEMS DESCRIBED ABOVE ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNERS AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS AS DESCRIBED IN A TI REFERENCE DESIGN OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

TI's standard terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products. Additional terms may apply to the use or sale of other types of TI products and services.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265