TI Designs

75-V/10-A Protected Full-Bridge Power Stage Reference Design for Brushed DC Motors

Description

Low-voltage brushed DC drives are used in many applications. TI offers a rich family of brushed DC motor driver solutions with flexible control interface options for one or more brushed DC motors up to 60 V. For applications that require higher torque and power, often voltages above 60-V DC are used. The TIDA-00365 protected full-bridge operates at a nominal 75-V DC input and a 10-A output current and features bipolar high-side current sensing leveraging a 100-V full-bridge gate driver SM72295 with integrated amplifiers and four 100-V NexFET™ power MOSFETs with ultra-low gate charge and small SON5x6 package with low thermal resistance. The power stage is protected against over-temperature, overcurrent, and short-circuit between the motor terminals and motor terminals to ground. The host processor interface is 3.3-V I/O to connect a host MCU like C2000™ Piccolo™ MCU for brushed DC motor current control.

Resources

TIDA-00365	Design Folder
SM72295	Product Folder
CSD19534Q5A	Product Folder
LM5018	Product Folder
LM2901V	Product Folder
ATL431	Product Folder
TIDA-00210	Product Folder

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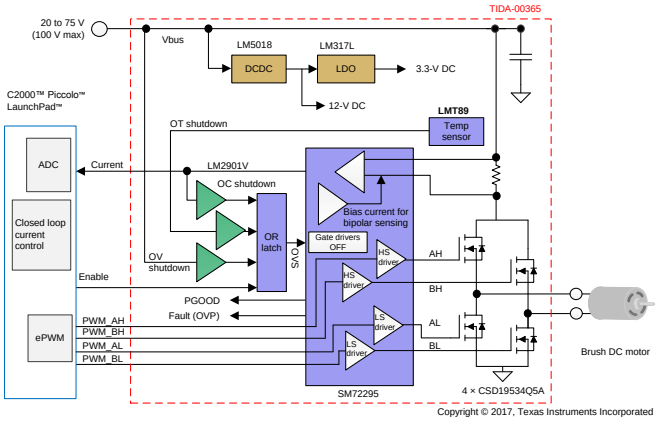
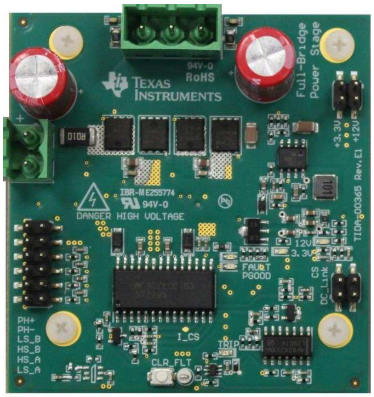
Features

- Protected Full-Bridge Power Stage With Input Voltage up to 100-V DC (75-V DC nominal) and 10-A Output Current
- BOM Reduction Through SM72295 100-V Full-Bridge Gate Driver With Integrated Amplifiers Used for High-Side Bipolar Phase Current Sensing
- Calibrated Current Sense Accuracy ±1% (Over Full Range ±10 A and ±0.2% (Within ±1-A range)
- Full-Bridge Optimized for Low EMI With 25-ns Rise and Fall Time on Switch-Node Voltages With No Over- and Undershoot
- Full-Bridge Protected Against Over-Temperature, Undervoltage, Over- and Short-Circuit Current Between Motor Terminals and Motor Terminals to GND
- 95% Efficiency at 16-kHz PWM; No Heatsink Required at 25°C Ambient and Nominal Load Due to TI NexFET Power MOSFET
- Host Processor Interface With Dual Complementary PWM Inputs (3.3-V CMOS) and Analog Outputs (0 to 3.3 V) for Bipolar High-Side Current Sense and Motor Terminal Voltage

Applications

- Brushed DC Motors
- Bipolar Stepper Motors





1 System Overview

1.1 System Description

Brushed DC motors with a wired-wound rotor and permanent magnet stator are still a popular option for motor designs due to their low cost and easy control scheme. The commutation of the motor is achieved mechanically through brushes, which scrape against the commutator rings. The torque of the brushed DC motor is proportional to the stator current, which allows for easy torque as well as direction and speed control. A speed-variable brushed DC drive typically consists of a full-bridge (H-bridge) power stage with PWM control, current sense and voltage sense, and a microcontroller to implement the current control and speed control. A mechanical speed (or angle) sensor is typically use for precise speed control and low speed operation. Protection against overcurrent, overvoltage, over-temperature, and so on can be implemented with the microcontroller or integrated in the full-bridge power stage in the hardware.

Low-voltage brushed DC drives are used in many applications operating typically from 12- to 48-V DC. TI offers a rich family of brushed DC motor driver solutions that are easy to use and make motors simple to spin. With flexible control interface options and multiple current range offerings, users can control one or more brushed DC motors with a single chip from 1.8 to 60 V.

For applications that require higher torque and power, often voltages above 60-V DC are used. The TIDA-00365 protected full-bridge is designed for use with a higher DC link voltage at a nominal 75-V DC input voltage and can source a 10-A output current for brushed DC motors. For the H-bridge, this TI Design uses four 100-V NexFET power MOSFETs with ultra-low gate charge and small SON5x6 package with low thermal resistance. To reduce PCB space, it features a 100-V full-bridge gate driver SM72295 in a SOIC-28 package with integrated high-side amplifiers, which are used for bipolar high-side current sensing. It uses a single DC-link current shunt for bipolar output current sensing as well as protection against overcurrent and short-circuit.

The TIDA-00363 full-bridge power stage is protected against over-temperature, overcurrent, and short-circuit between the motor terminals and motor terminals to ground. This can be caused for example due to a fault of the brushed DC motor fault or miss-wiring. To detect both, a short across the motor terminals and a short from any of the motor terminals to GND, a common high-side DC-link current sense are typically used.

For cost, BOM, and PCB space reduction, the same high-side DC-link current sense is intended to be used for motor current sense and control as well. On the other hand, there are also some limitations with this approach, depending on PWM control. For both unipolar and bipolar PWM switching, time synchronized sampling of the DC-link current is required to measure the correct motor current magnitude and sign. During the inactive state in unipolar switching, the motor current is freewheeling through either both low-side switches or both high-side switches and hence cannot be measured through either high-side or low-side DC-link current sense. With a microcontroller, which can switch between unipolar and bipolar PWM, these limitations can be mitigated in most cases to take advantage of a single current shunt only.

Onboard power supplies with wide input up to 100-V DC provide the 12- and 3.3-V rails for the gate driver and signal chain.

The host processor interface is a 3.3-V I/O to connect a host MCU like C2000 Piccolo or MSP430™ for brushed DC motor control. The interface provides four inputs for the dual complementary PWM signals to switch the full-bridge, an analog outputs for the bipolar high-side current sense, scaled from ±16.5 A to 0 to 3.3 V and the motor terminal voltages scaled from 0 to 100 V to 0 to 3.3 V. A simplified picture of the TI Design used with a brushed DC motor is shown in Figure 1.

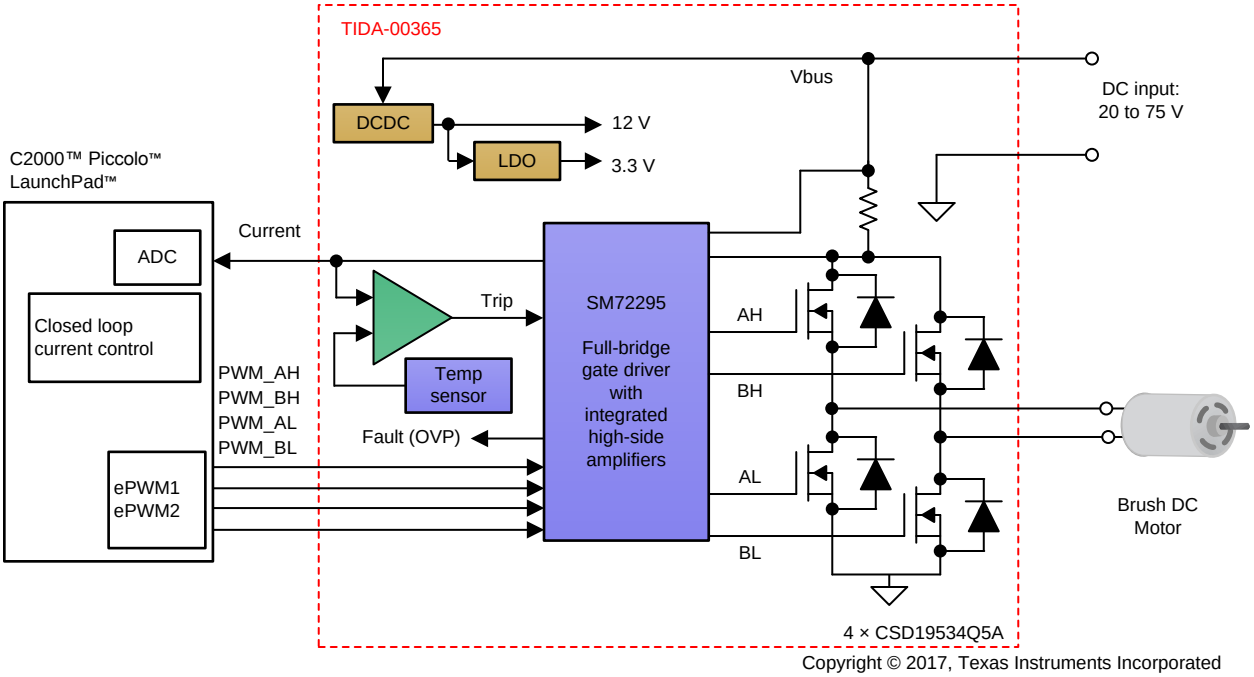


Figure 1. TIDA-00365 Simplified Block Diagram and C2000 MCU for Brushed DC Drive Current Control

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
DC input voltage range	75-V nominal, 20-V min., 100-V max.
PWM switching frequency	16 to 25 kHz (nominal)
Gate driver type	Full-bridge gate driver with integrated high-side amplifiers
Power FET type	100 V N-Channel NexFET Power MOSFET
Current range (phase)	10-A nominal, 15 A (peak, max)
Current sense topology	High-side shunt
Current shunt	10 mΩ
Current sense accuracy	Uncalibrated < 5%
	Calibrated gain and offset error: < 1% (±10-A range), < 0.2% (within ±1-A range)
Efficiency	95% (estimated)
Protections	UVP, OCP, OTP, and OVI
Overcurrent protection (OCP)	15 A ± 4%
Over-temperature protection (OTP)	120°C ± 4%
Overvoltage indicator (OVI)	84 V ± 3%
Undervoltage protection (UVP)	18-V rising UVLO, 16-V falling UVLO
Short-circuit protected against	Phase to GND and phase to phase
Operating ambient temperature	–40°C to 85°C
Onboard gate drive power supply rail	12-V ± 5%, 50-mA max
Onboard gate drive logic supply rail	3.3-V ± 5%, 20-mA max
Host processor interface signals	4 × PWM (dual complementary PWM signals, nominal dead band 80 ns)
	High-side current
	Motor terminals to GND voltage (phase+ and phase– to GND)
Host processor interface signal level	3.3-V CMOS for digital input signals (PWM)
	0 to 3.3 V for analog output signals (phase current and phase to GND voltages)
PCB layers	4 layers, 2-oz copper
PCB size	64 mm × 68.3 mm

1.3 Block Diagram

The block diagram of the TIDA-00365 block diagram is showed in Figure 2:

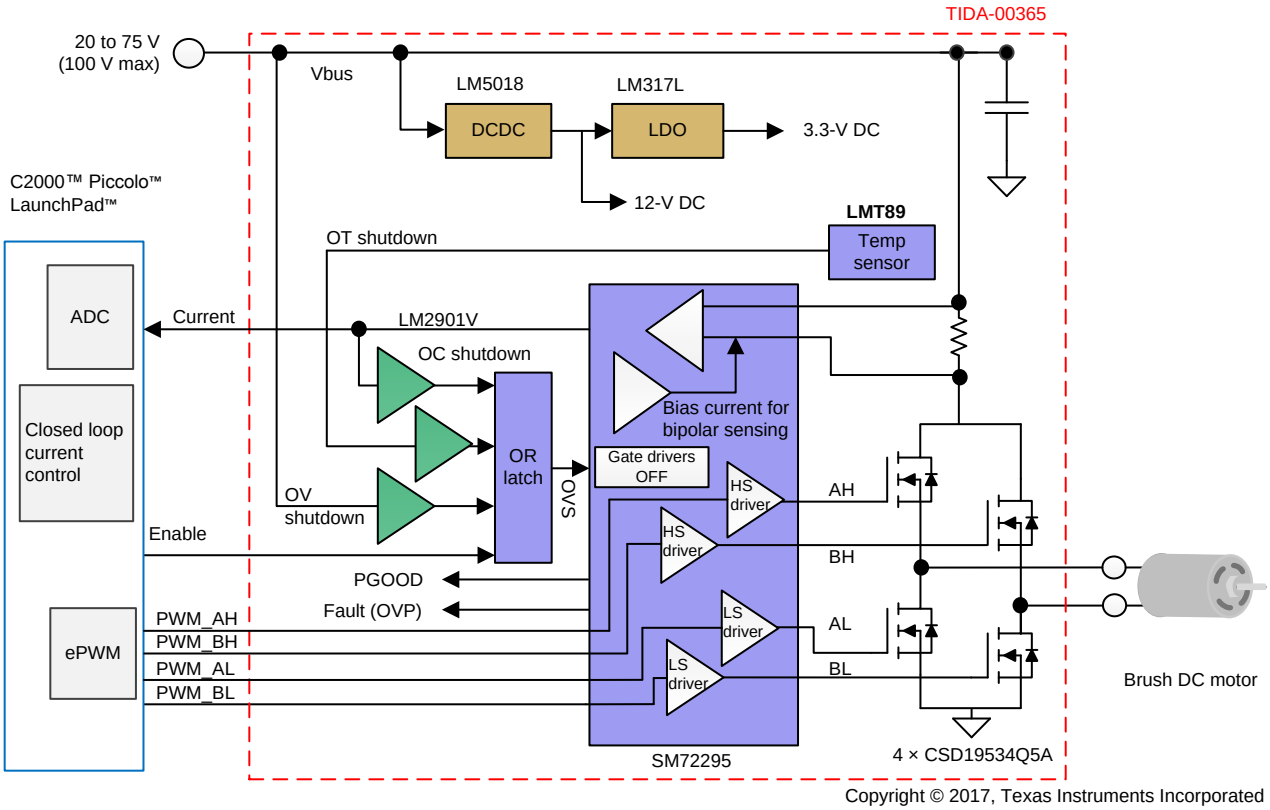


Figure 2. TIDA-00365 Block Diagram

1.4 Highlighted Products

1.4.1 SM72295

The SM72295 is designed to drive four discrete N-type MOSFETs in a full-bridge configuration. The drivers provide 3 A of peak current for fast efficient switching and integrated high-speed bootstrap diodes. Current sensing is provided by two trans-conductance amplifiers with externally programmable gain and filtering to remove ripple current to provide average current information to the control circuit. The current sense amplifiers have buffered outputs available to provide a low-impedance interface to an analog-to-digital converter (ADC) if needed. An externally programmable input over voltage comparator is also included to shut down all outputs. Undervoltage lockout (UVLO) with a PGOOD indicator prevents the drivers from operating if VCC is too low.

The main features of this device are:

- Integrated 100-V bootstrap diodes
- Bootstrap supply voltage range up to 115 V
- Independent high and low driver logic inputs
- Two current sense amplifiers with externally programmable gain and buffered outputs
- Programmable overvoltage protection (OVP)

1.4.2 CSD19534Q5A

This 100-V, 12-mΩ, SON 5-mm×6-mm (SON5x6) NexFET power MOSFET is designed to minimize losses in power conversion applications.

The main features of this device are:

- Ultra-low Q_g and Q_{gd}
- Very-low Q_{rr}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free

NOTE: Depending on the needs, a different FET could suit better for performance, like the CSD19532Q5A or CSD19533Q5A (pin-to-pin compatible). The CSD19534Q5A seems the best performing part for EMI (no voltage spikes, no ringing on the software nodes), offering the best balance between Q_{rr} of the body diode and R_{DSon}.

1.4.3 Shunt Voltage Reference (ATL431, TL431, TLV431)

The ATL431 and ATL432 are three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and industrial temperature ranges. The output voltage can be set to any value between the reference voltage (2.5 V or 1.25 V, depending on the version) and 36 V with two external resistors. Active output circuitry provides a very sharp turnon characteristic, making these devices excellent replacements for Zener diodes in many applications.

The ATL43x has > 20× improvement cathode current range over its TL43x predecessor. It also is stable with a wider range of load capacitance types and values.

The ATL431 and ATL432 are the exact same parts but with different pinouts and order numbers. The ATL43x is offered in two grades, with initial tolerances (at 25°C) of 0.5% and 1% for the B and A grade, respectively. In addition, low output drifts versus temperature ensures good stability over the entire temperature range.

The ATL43xxI (industrial) devices are characterized for operation from –40°C to 85°C, and the ATL43xxQ (automotive) devices are characterized for operation from –40°C to 125°C.

The main features of this device are:

- Very-low operating current: $I_{KA(min)}$ = 35 μA (max)
- Internally compensated for stability: Stable with no capacitive load
- Very-low reference voltage tolerances at 25°C
- Typical temperature drift: 5 mV (I version) and 6 mV (Q version)
- Extended cathode current range: 35 μA to 100 mA

1.4.4 LM5018

The LM5018 is a 100-V, 300-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant-on-time (COT) control scheme employed in the LM5018 requires no loop compensation, provides excellent transient response, and enables very low step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high-voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers.

A peak current limit circuit protects against overload conditions. The UVLO circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply UVLO.

The main features of this device are:

- Wide 7.5- to 100-V input range
- Integrated 300-mA high-side and low-side switches
- No bootstrap diode required
- COT control:
  - No loop compensation required
  - Ultra-fast transient response
- Nearly constant operating frequency
- Intelligent peak current limit
- Adjustable output voltage from 1.225 V with 2% accuracy
- Frequency adjustable to 1 MHz
- Adjustable UVLO

NOTE: Beside the LM5018, when higher or lower current is required, consider the pin-to-pin parts from the same family LM5017 (600 mA) or LM5019 (100 mA).

1.4.5 LM2901V

The LM2901V consists of four independent voltage comparators that are designed specifically to operate from a single supply or split supply over a wide range of voltages. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships; this is useful when using the comparators to implement the various protections.

The main features of this device are:

- Wide supply ranges
  - Single supply: 3 to 32 V
  - Dual supplies: ±1 to ±16 V
- Low supply-current drain independent of supply voltage: 0.8 mA typical
- Low input bias and offset parameters
  - Input offset voltage: 2 mV typical
  - Input offset current: 3 nA typical
  - Input bias current: 25 nA typical
- Internal frequency compensation
- Common-mode input voltage range includes ground
- Differential input voltage range equal to maximum-rated supply voltage
- Low output saturation voltage

1.4.6 LM317LIPK

The LM317LIPK fixed-output, low-dropout regulator offers exceptional, cost-effective performance for both portable and non-portable applications. Available in voltages of 1.8 V, 2.5 V, 2.8 V, 2.9 V, 3 V, 3.1 V, 3.3 V, 5 V, and 10 V, the device has an output tolerance of 1% for the A version (1.5% for the standard version) and is capable of delivering a 150-mA continuous load current. Standard regulator features such as OCP and OTP are included.

The main features of this device are:

- Tight output tolerance: 1% (A grade) or 1.5% (standard grade)
- Ultra-low dropout: 280 mV at full load of 150 mA, 7 mV at 1 mA
- Wide V_{IN} range: 16 V max
- Low IQ: 850 μA at full load at 150 mA
- Shutdown current: 0.01 μA typ
- Low noise: 30 μV_{RMS} with 10-nF bypass capacitor
- Stable with low-ESR capacitors, including ceramic
- OCP and OTP
- High peak-current capability
- ESD protection exceeds JESD 22

The LM317L-N is available in a different package as well. The LM317L-N is available packaged in a standard, easy-to-use TO-92 transistor package.

NOTE: For a more cost effective solution, consider the LM317LIPK; however, the accuracy decreases from 1.5% to 5%. This could limit the applicability of the LM317LIPK versus the LP2985-33, when for example a 3.3 V ±5% is needed.

1.4.7 LMT89

The LMT89 is a precision analog output CMOS integrated-circuit temperature sensor that operates over a –55°C to 130°C temperature range. The power supply operating range is 2.4 to 5.5 V. The transfer function of the LMT89 is predominately linear, yet has a slight predictable parabolic curvature. When specified to a parabolic transfer function, the accuracy of the LMT89 is typically ±1.5°C at an ambient temperature of 30°C. The temperature error increases linearly and reaches a maximum of ±2.5°C at the temperature range extremes.

The quiescent current of the LMT89 is less than 10 μA. Therefore, self-heating is less than 0.02°C in still air. Shutdown capability for the LMT89 is intrinsic because its inherent low power consumption allows it to be powered directly from the output of many logic gates or does not necessitate shutdown at all.

The LMT89 is a cost-competitive alternative to thermistors. The relationship between the output voltage and the sensed temperature (in Celsius) is:

$$V_{OUT} = 1.8639 - 1.15 \times 10^{-2} \times T - 3.88 \times 10^{-6} \ T^2 \cong 1.8639 - 1.15 \times 10^{-2} \times T \quad (1)$$

2 Hardware Design

NOTE: Most of the dividers in the TIDA-00365 use two or more resistor in series to reduce the voltage drop over one resistor.

2.1 Power Management

Given the specifications (20- to 75-V DC input, Vout1 = 12 V at 20 mA, and Vout2 = 3.3 V at 15 mA), in which the 12 V is minded to supply the gate driver while the 3.3 V the signal conditioning and processor interface circuits.

A simplified block diagram of the power management solution is showed in Figure 3:

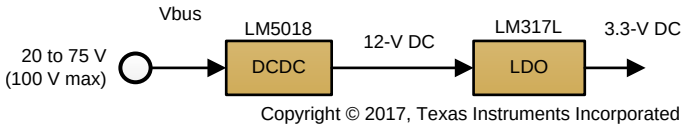


Figure 3. Power Management Solution Block Diagram

Because of the little current level, the 3.3 V could be simply achieved by using a common LDO, like the LM317L (the most affordable option).

The supply for the driver (12 V at 20 mA) turns into the new specification 12 V at 35 mA because the load of the LDO directly applies to the input. Indeed the driver switches at a nominal frequency of 16 kHz and having a peak current of 3 A the RMS value is very little.

Looking at the SM72295 datasheet the consumption of the driver is around 3 mA (LS drivers) + 1 mA (HS drivers) = 4 mA; on top the gate charge has to be added, so assuming a rise and fall time of 50 ns, a 3-A peak current, the RMS value at 16-kHz switching frequency is 50 ns × 3 A × 16 kHz × 4 FET drivers ≈ 4 mA, leading to a total current consumption of the SM72295 < 10 mA.

Because of the little current again a linear regulator could be used, in particular when the cost is key factor of the design: something like the TL783 (http://www.ti.com/product/TL783) is a valid choice. In this TI Design, the efficiency is the key factor, so a SMPS is chosen instead: the LM5017/LM5018/LM5019 offer a valid selection pattern for a wide V_{IN} and good price-to-performance ratio. The LM5018 has been used in order to leave the flexibility to supply other 12-V rated devices such as a cooling fan.

In case of different needs, the LM5019 (100 mA) or the LM5017 (600 mA) could be replaced instead because all the three parts are pin-to-pin compatible.

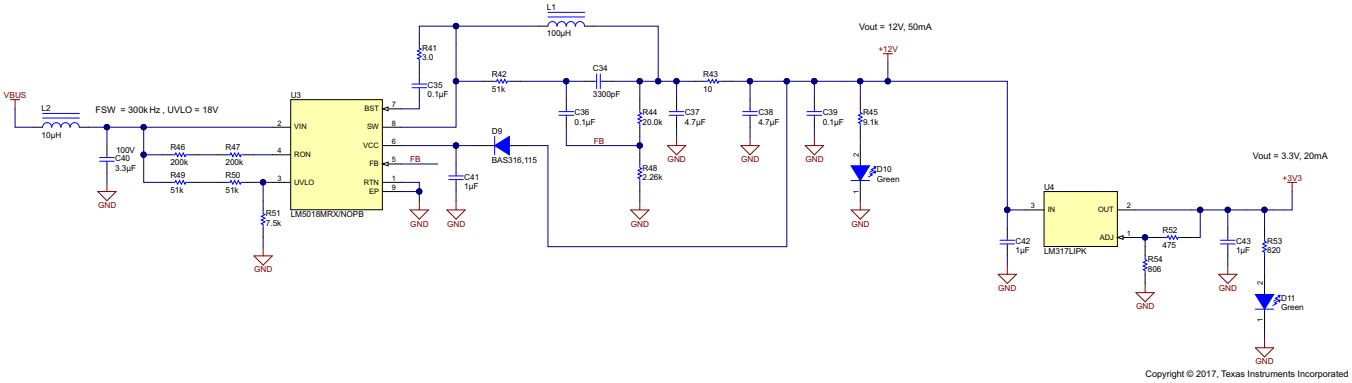


Figure 4. Schematic of Power Management Solution

To design the solution, the spreadsheet associated to the part can be used. Also note that the output supplies and override the internal LDO for a better efficiency performance of the LM501x.

An input filter is also proved to reduce conducted EMI. Because of the big input capacitor needed for the motor driver power stage, the input inductor could be selected as small as possible. The switching frequency could be also reduced down to 300 kHz maximum. UVLO is set at an 18-V input (rising) with a hysteresis of 2 V (meaning the turn off threshold is at a 16-V input).

For more details, see the LM501x design guidelines.

2.2 Full Bridge

The full-bridge gate driver can be split into three main parts:

- The FET gate driver
- The FET bridges
- The current sense circuit

2.2.1 Full-Bridge Gate Drivers

The actual driver is implemented by using the SM72295, a general purpose four-switch (buck-boost) controller. To supply these drivers, two rails are required: one for the actual power driver (12 V nominal) and one for the control logic (3.3 V or 5 V).

The expected current consumption on these rails is in the range of 10 mA for the 12 V (due to the fact that the typical switching frequency in motor drives application is 16 kHz, and the drivers embedded into the SM72295 can provide 3 A max, the RMS current would be very low) and around 5 mA for the logic. This simply because the peak current of the driver is 3 A (in both direction) that, over a nominal switching frequency of 16 kHz, leads to an RMS gate drive current of a few milliamps. Any SM72295 has two half-bridge drivers embedded: for the high-side driver section, two gate resistors are provided to provide flexibility to independently fine tune the switching time (on and off). A single gate resistor can be used to optimize BOM cost.

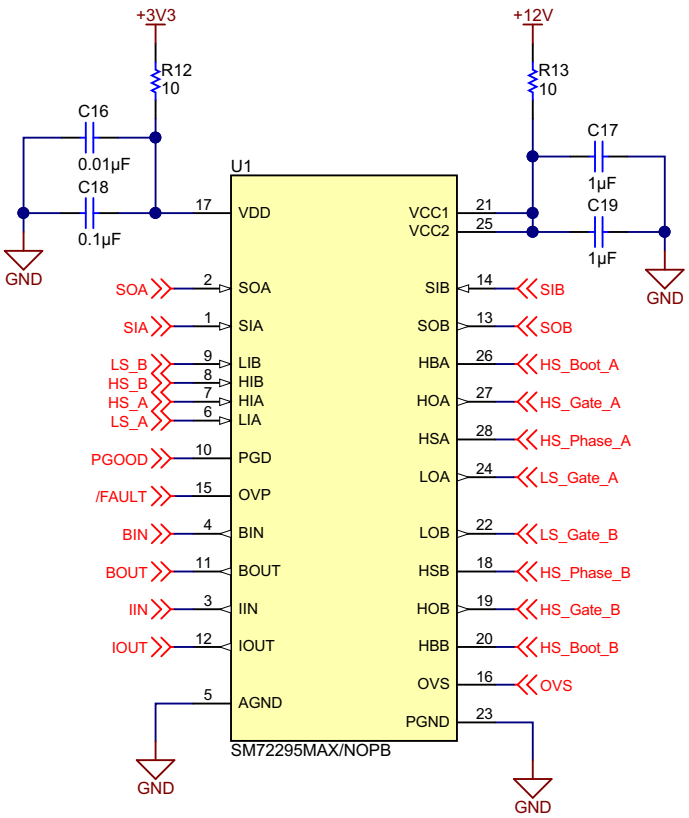


Figure 5. Schematic of Full-Bridge Gate Driver

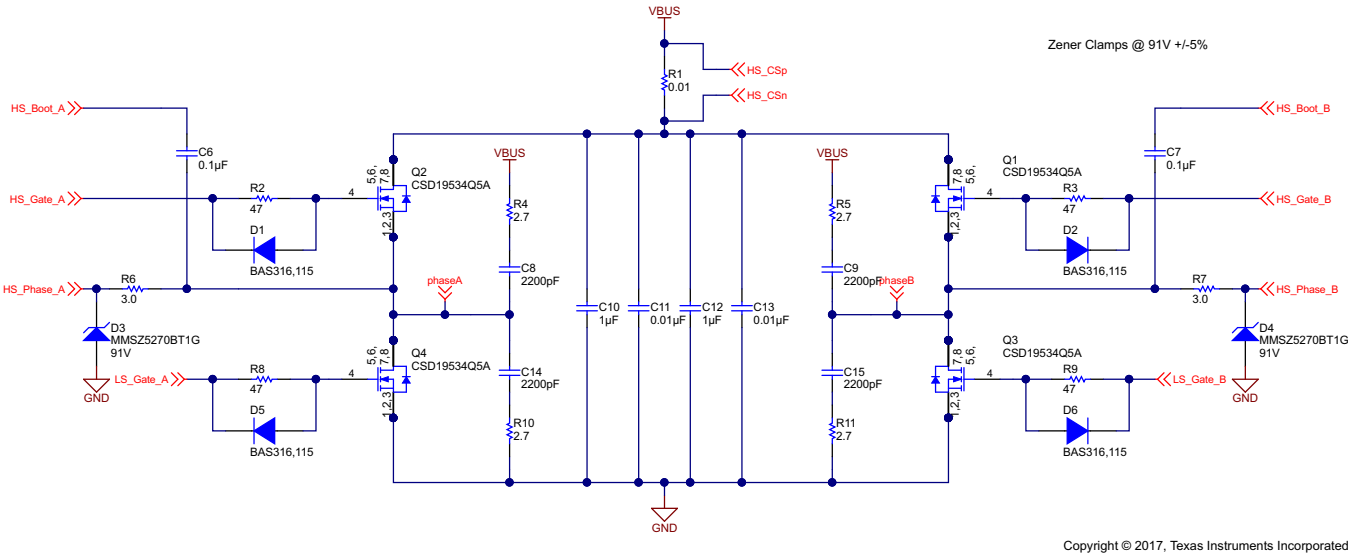


Figure 6. Schematic of Full-Bridge Power Stage

Because the TIDA-00365 is 100 V rated, a Resistor-Zener network is provided on the switch nodes of the driver to protect it from overshoots and undershoots. Further, a 47R gate resistor is provided to reduce the EMI due to the too fast switching of the NexFET.

2.2.2 Full-Bridge (FET Selection Guide)

The biggest challenge of this TI Design is selecting the best FET for the application, where "best" means the right one in terms of trade-off between price, size, and performance.

First of all, the total power losses for the FET have to be calculated; because of the symmetry of the system, losses in HS and LS MOSFETs can be considered identical in the first instance:

$$P_{LS} = P_{HS} = P_{Switching} + P_{Conduction} + P_{DeadTime} \quad (2)$$

$$P_{Switching} = V_{DS} \times I_{Phase} \times f_{SW} \times \frac{(T_{Rise} + T_{Fall})}{2} \quad (3)$$

$$P_{Conduction} = R_{DSon} \times I_{Phase}^2 \times D \quad (4)$$

$$P_{DeadTime} = V_F \times I_{Phase} \times f_{SW} \times T_{DeadTime} \quad (5)$$

The two currents in the phases are 90° phase shifted. Depending on the motion control technique (if full-step or micro-step driving), these currents are square or sine waves, respectively. Regardless, for the thermal analysis purpose, consider the RMS values so that:

- Duty cycle = D = 50%
- I_{Phase} = 10 A_{RMS}
- V_{DS} = 75 V (the maximum value is considered)
- f_{SW} = 16 kHz
- V_F = 1 V typ
- R_{DSon} = 23 mΩ at 125°C
- Dead time = 100 to 120 ns

Assuming a T_{Rise} = T_{Fall} = 30 ns (which is expected with a 47R gate resistor + CSD19534Q5A), then

$P_{LS} = P_{HS} \cong 1.5$ W

IMPORTANT: The device needs a proper heat sink or air cooling system to guarantee proper system functionality and to detect overcurrent (threshold at 15 A). Also, the SON5x6 package allows superior layout optimization versus other package options as well as spikes and ringing reduction on the switch nodes because of the smaller stray (parasitic) inductances. See Section 5.3 for more details.

NOTE: Snubber networks are also provided with the design. To calculate the best value to achieve ringing reduction on the switch nodes, both high-side and low-side snubbers are provided. The best results are obtained with $C_{snubber}$ = 2.2 nF and $R_{snubber}$ = 2.7 Ω. See snubber design application notes for more details.

2.2.3 Current Sense Circuit

The SM72295 provides two embedded current sense amplifiers with a high common-mode voltage (100 V) to measure both input and output currents (because the driver itself is minded for a buck-boost converter).

These amplifiers are used to sense the HS current per phase; sensing the high-side current allows for a higher degree of protection since any potential short circuit could be detected by triggering the overcurrent protection.

Figure 7 shows the block diagram of the SM72295 integrated current sensing amplifiers.

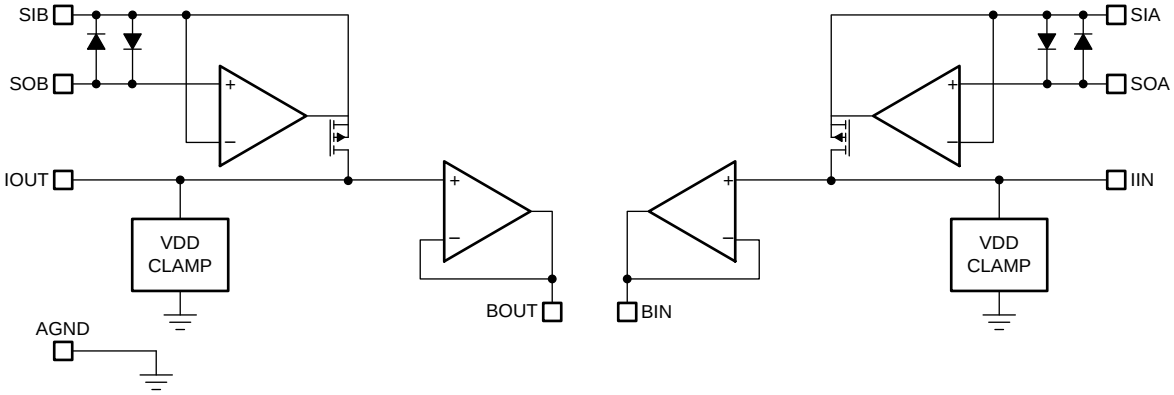


Figure 7. Block Diagram of SM72295 Integrated Current Sense Amplifiers

The pin descriptions for the integrated amplifiers and several guidelines are:

- SIA and SIB (inputs): Tie to the positive side of the sense resistor through an external gain programming resistor (RI). RI is in series with the SIA/SIB pin. Make sure the value of RI at the SIA/SIB pin is the same value at the SOA/SOB pin.
- SOA and SOB (inputs): Tie to the negative side of the sense resistor through an external gain programing resistor (RI). RI is in series with the SOA/SOB pin. Make sure the value of RI at the SOA/SOB pin is the same value at the SIA/SIB pin.
- IIN and IOUT: The output of the input current sense amplifier. Requires an external resistor to ground (RL). Do not connect this pin to anything else. The gain is RL/RI, where RI is the external resistor in series with both the SIA and SOA pin, and the SIB and SOB.
- BIN and BOUT (outputs): Buffered output of the IIN and IOUT, respectively. The voltage at BIN/BOUT is linear with the current through the sense resistor.
- The recommended differential voltage between current sense amplifier inputs (SIA to SOA, SIB to SOB) must be less ±0.5 V, with an absolute max differential voltage of ±0.8 V.
- The gain can be programmed to any value with the max output of the amplifier limited to VDD (3.3 V or 5 V). There is a VDD clamp at the current sense amplifier output BIN and BOUT.

Figure 8 shows the resistor connections of these pins and their implementation, according to Equation 6:

$$\left(R_{Sense}\right) \times \left(I_{Sense}\right) \times \left(\frac{RL}{RI}\right) = \text{Voltage at BIN and BOUT pins} \quad (6)$$

where the maximum voltage is clamped at VDD.

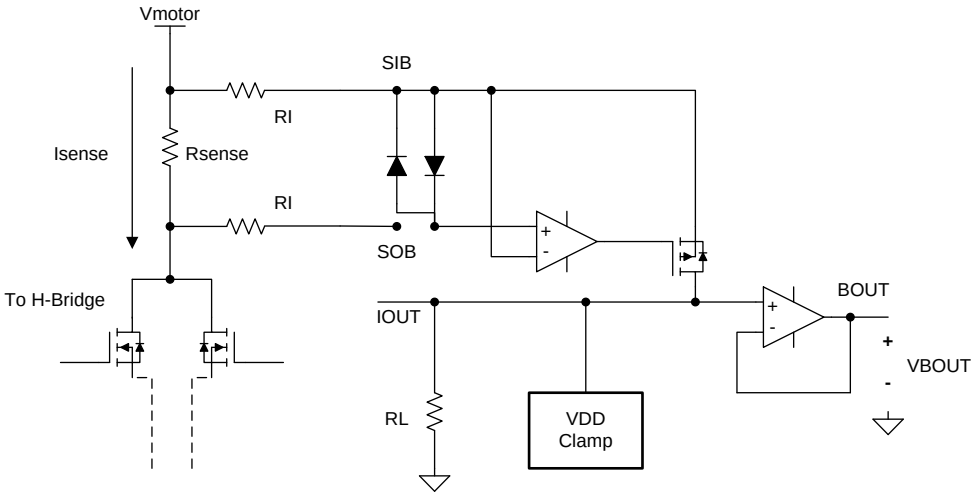


Figure 8. Current Sense Amplifier Connections

These amplifiers are natively unipolar, meaning no bipolar current could be detected. In order to turn the unipolar current sense amplifiers into a powerful bipolar one, the two amplifiers are combined. To do this, a positive offset to the sensed current is applied. Because this current offset has to be precise and stable over temperature, time, input voltage, and so on, a current mirror is recommended (preferably with a matched pair of transistors).

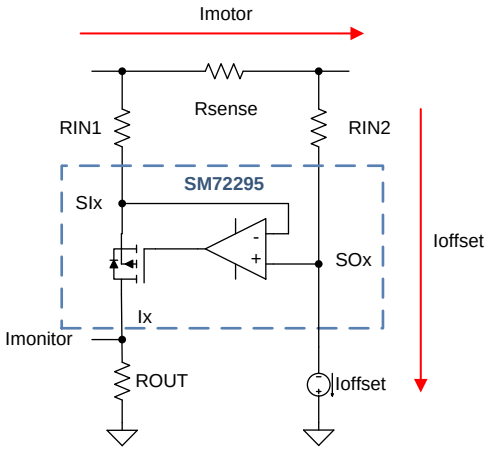


Figure 9. Current Offset to Turn Unipolar Current Sense Amplifier Into Bipolar

2.2.3.1 Basic Solution

A basic solution consists in using a high-voltage rated matched pair of transistors (like the DMMT5551) to implement the current offset. However, this solution is quite expensive:

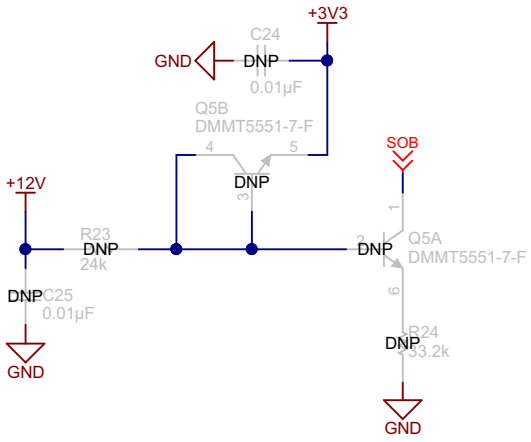


Figure 10. Current Offset Performed by Matched Pair of Transistors

The matched pair of transistors, connected in an emitter follower configuration, work in a way that the 3.3 V is replicated on top of R54; in this way the $I_{Offset} = \frac{3.3\ V}{R54}$ is applied to the current sense amplifier (SOBx pin). The precision and stability of this current depends mainly on the quality of the 3.3-V rail.

For more details about how this solution works, see the TIDA-00558 reference design.

2.2.3.2 Implement (Advanced) Solution

Another way to provide the current offset is to use the second (embedded) amplifier without extra external components (except for a voltage reference to guarantee the current offset is stable over temperature, and so on). *This solution has been implanted in the TIDA-00365 design (and then in the TIDA-00210 design).*

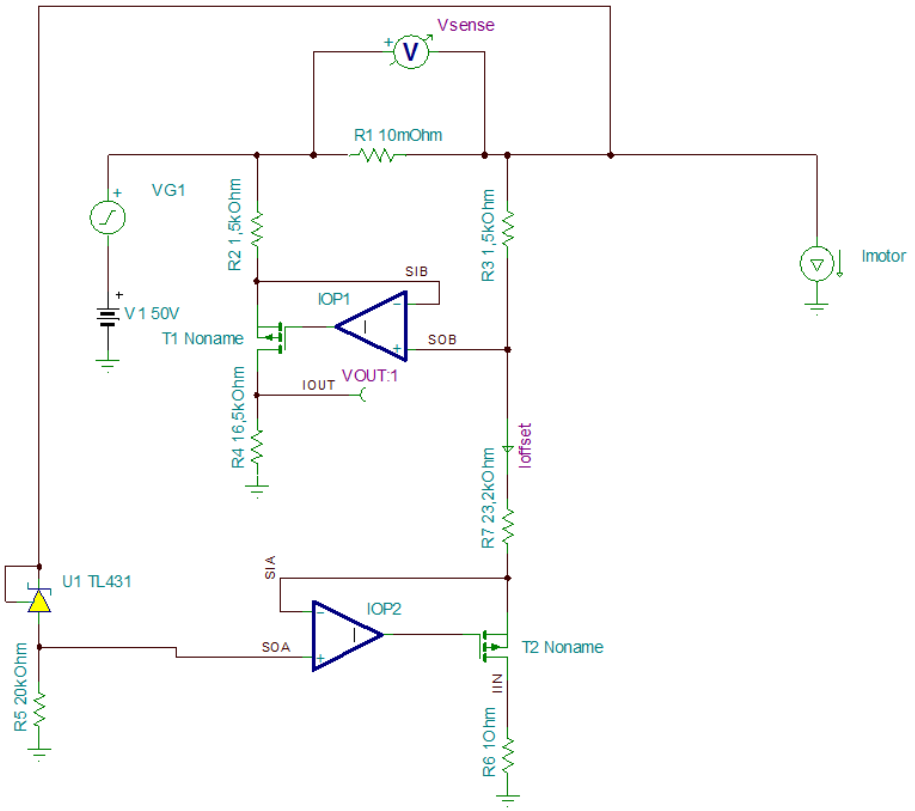


Figure 11. TI-TINA™ Simulation Circuit of Implement Current Sense Solution

In which:

- R1 is the sense resistor
- I_{Motor} is a generator that emulates the motor load
- IOP1 + T1 is one of the two unidirectional embedded current sense circuit of the SM72295
- R2, R3, and R4 are the external components to achieve the current sense, according to Equation 7
- IOP2 + T2 is the second embedded current sense configured as current sink to perform the I_{Offset}

The loop of the IOP2 works in the way that the voltage of the reference TL431 is the same on the series R3+R7 while R5 is placed to guarantee the U1 is in regulation at any possible V_{IN}. R6 has no actual purpose, except to have a signal referred to GND proportional to I_{Offset} (debug). The advantages of this solution (and also the one implemented in the TIDA-00210) versus the "state of the art" are:

- No extra components are necessary (higher integration level)
- Lower cost compared to a typical current sense solution
- Higher protection level because the current sensing is performed on the high side of the bridge
- Accuracy is guaranteed by the TL431, which offers the best performance in voltage reference at the lowest possible cost

Both the simulation model and the TIDA-00210 reference design have been set to have a 0- to 3.3-V voltage scale signal for a –15- to 15-A phase current, or:

$$V_{CurrentSense} = V_{Offset} + Gain \times I_{Motor} = 1.65\ V + I_{Motor} \times \frac{1.65\ V}{15\ A} = 1.65\ V + 110\ m\Omega \times I_{Motor} \quad (7)$$

The following equations achieve the optimized current sense circuit:

- $V_{OUT} = (I_{Motor} \times R_{Sense} + I_{Offset} \times R3) \times R4 / R2$
- $I_{Offset} = V_{REF} / (R3 + R8)$
- $V_{REF} = 2.5\ V$ (TL431)
- I_{Offset} and R3 are chosen in order to have
- $I_{Offset} \times R3 = I_{Motor\_max} \times R_{Sense}$

while R4 and R2 defines the scale range of the output (0 to 3.3 V in this example is used for the simulation).

2.2.3.3 Step-by-Step Design of Current Sensing Network

First, the current per phase is 10 A_{RMS} (by spec) at a 15-A peak (overcurrent). In order to guarantee a good signal-to-noise ratio over the sense resistor, a minimum value of 10 mΩ is recommended. In this design, the 10 mΩ, 3 W from BOURNS has been selected as the current sense resistor.

The output of the current sense circuit feeds the A/D converter, whose scale is 0 to 3.3 V, meaning that at 15 A the maximum output has to be 3.3 V. The 10 A_{RMS} means that $I_{Max} = I_{RMS} \times \sqrt{2}$ when a microstepping mode with sinusoidal current is implemented.

With this information, it has to be decided where to set the positive offset: this depends on how big the negative current could be (generating mode) and directly affect the ENOB of the converter. The simplest way is to set the offset at exact middle of the full-scale of the ADC, meaning that at a 0-A phase current the output of the current sense circuit has to be 1.65 V; under these conditions, the actual resolution is the ADC one minus 1 bit (half scale is actually used to sense the real current, meaning the positive one going to the motor).

Now that R_{Sense} and I_{Peak} (overcurrent) are known, the rest of the network can be designed. Referring to Figure 11, the following equations are applied:

- $V_{OUT} = (I_{Motor} \times R_{Sense} + I_{Offset} \times R3) \times R4 / R2$
- $I_{Offset} = V_{REF} / (R3 + R8)$
- $V_{REF} = 2.5\ V$ (TL431)
- I_{Offset} and R3 are chosen in order to have
- $I_{Offset} \times R3 = I_{Motor\_max} \times R_{Sense}$

while R4 and R2 defines the scale range of the output (0 to 3.3 V in this example used for the simulation).

So

- $R_{Sense} = 10\ m\Omega$
- $I_{Motor\_max} = 15\ A$
- $V_{REF} = 2.5\ V$
- I_{Offset} is set equal to 100 µA

$$100\ \mu \times R3 = 10\ m \times 15\ A \rightarrow R3 = 1.5\ k\Omega \quad (8)$$

$$100\ \mu = \frac{2.5\ V}{(R3 + R8)} \rightarrow R3 + R8 = 25\ k\Omega \rightarrow R8 = 23.5\ k\Omega \quad (9)$$

The closest commercial value 23.2K has been chosen. R5 is chosen to guarantee the TL431 is in regulation all the time, that is the minimum cathode current equal to 1 mA. Having V_{IN} = 18 V, the maximum R5 value has to be (20 V – 2.5 V) / 1 mA = 17.5 kΩ. 16.4 kΩ has been selected for R5 while at max VIN (OVP is triggered at a 84-V input), the current into R5 is around 5 mA.

The power rating of this resistor has to be then 16.4 K × 5 mA × 5 mA = 410 mW, which cannot be achieved with a single resistor. For this purpose, two resistors at 8.2 kΩ 1206 5% 0.25-W rated connected in series have been selected.

And then the last one sets the gain to match the FSR of the ADC (0 to 3.3 V):

$$V_{OUT} = \left(I_{Motor} \times R_{Sense} + I_{Offset} \times R3\right) \times \frac{R4}{R2} \quad (10)$$

And because the offset is placed in the middle:

$$3.3\ V = 15\ A \times 10\ m\Omega \times 2 \times \frac{R4}{R2} \rightarrow \frac{R4}{R2} = 11 \quad (11)$$

Selecting R2 = R3 = 1.5 kΩ → R4 = 16.5 kΩ

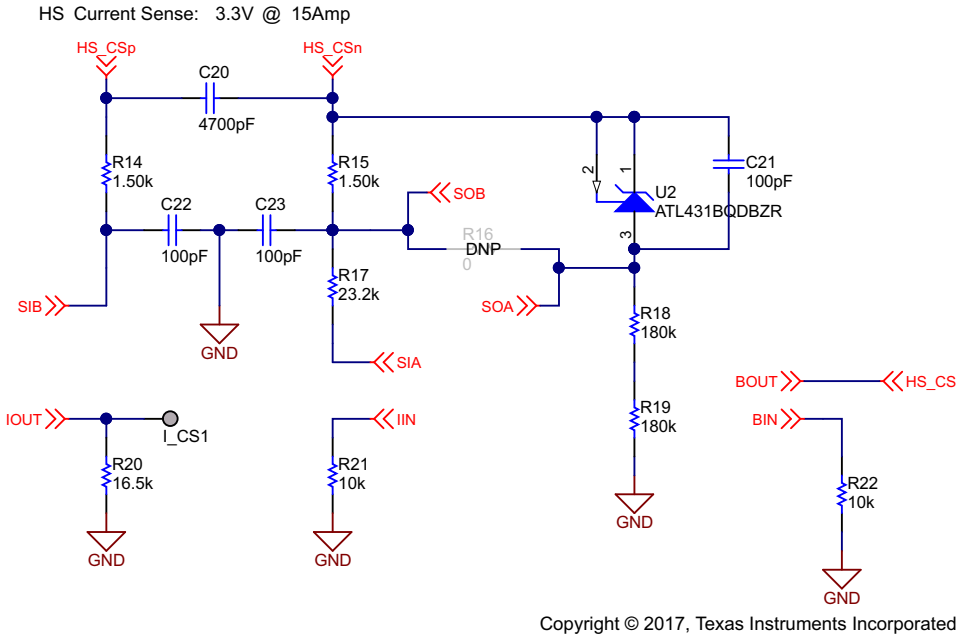


Figure 12. Implementation of Bipolar High-Side Current Sense Solution

A few low-pass filters have been placed on the noisy nodes: also for this purpose, R2 and R3 are chosen for the same values.

Due to the excessive size (and cost) of the 2×1206 bias resistor for the TL431, a better choice is to use the ATL431, a bit more expensive than the sufficient TL431, but these require only a minimum current of 35 µA to guarantee regulation.

Assuming then a 50-µA bias current, the correspondent R5 becomes R5 = (20 V – 2.5 V) / 50 µA = 350 kΩ → 360K has been chosen as the commercial value

Now at the maximum input voltage, the loss on the bias resistor is only

$$\text{Power over R5} = \frac{(84 - 2.5\ V)^2}{360K} < 25\ mW \quad (12)$$

Meaning a single 0402 resistor (63 mW rated) can do the job.

IMPORTANT: The embedded current sense amplifiers have limited bandwidth (around 400 kHz). This bandwidth also means that the slew rate of the output signal is limited to roughly 0.8 to 1 V/µs, meaning to swing the full range would take 3 to 4 µs (half because the full range has been halved). Having F_{SW} = 16 kHz leads to a period of about 62 µs. Both of these values provide the minimum duty cycle the system could manage (in closed loop current control), that is, 4/62 ≈ 6.4%, which becomes 3.2% when considering half of the full-range swing. Adding about a 1-µs conversion time of the ADC, it leads to a minimum duty cycle of 3/62 ≈ 4.8% (< 5% specified as system performances). This is not a real limitation because duty cycles < 25% leads to high current into the motor. The switching frequency can be increased to reduce phase current ripple up to eight times the nominal one.

2.3 Protections

The following protections are provided for this stepper driver:

- Overcurrent
- Over-temperature
- Overvoltage
- UVLO

All these protections can be easily implemented using a general purpose open drain output comparator barrier and combining the outputs in wiring OR/AND fashion.

Note that overvoltage is not a real protection, but it basically disables the gate drive as the input voltage overcomes the 85-V nominal.

A constant and well-regulated voltage reference (as a threshold for the comparator) is provided by the most affordable TL431 while phase current, input voltage, and system temperature are scaled down with simple voltage dividers.

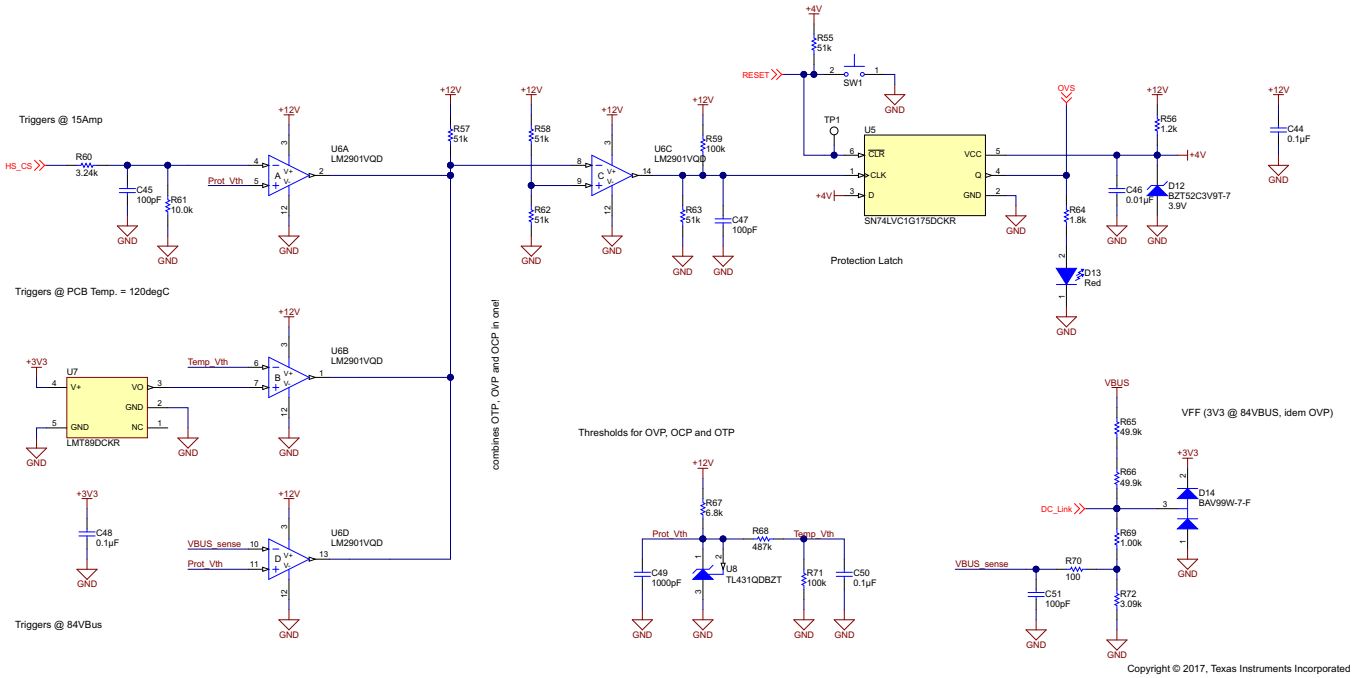


Figure 13. OVP, OCP, and OTP With Latch, Adjacent Thresholds, and Voltage Feed Forward (VFF) Network

Last but not least, UVLO is performed by the LM5018. When the bus or input voltage drops below 18 V, then the LM5018 shuts down, removing the supply to the driver.

2.3.1 Step-by-Step Design

- *Overcurrent*
  The input signal is the HS_CS_x, a voltage signal from 0 to 3.3 V, for a phase current from –15 to 15 A. The comparator U6 compares the voltage HS_CS_x to the reference provided by using a TL431, equal to 2.5 V. This means that to trigger the OCP at 15 A, a voltage divider from 3.3 V to 2.5 V is needed:

$$3.3\ \text{V} \times \frac{\text{R61}}{(\text{R61} + \text{R60})} = 3.3 \times \frac{10\text{K}}{13.24\text{K}} = 2.492\ \text{V} \tag{13}$$

- *Over-temperature*
  The input signal is the output voltage of the precise temperature sensor LMT89. When

$$V_{OUT} \cong 1.8639 - \left(1.15 \times 10^{-2} \times \text{T}\right) = 1.001\ \text{V} \tag{14}$$

  and then the voltage divider R68 / R71 is used to scale down the 2.5-V reference down to 1 V to trigger the OTP. Act on this divider to move up or down the trip temperature of the protection. Setting the threshold at 110°C, for example, leads to

$$V_{OUT} \cong 1.839 - \left(1.15 \times 10^{-2} \times \text{T}\right) = 0.6\ \text{V} = 2.5\ \text{V} \times \frac{\text{R71}}{\text{R68} + \text{R71}} \rightarrow \text{R71} = 100\text{K}, \text{R7} = 316\text{K}$$

  Furthermore, to avoid false OTP tripping at the start-up, a delay is applied on the Temp_Vth signal (see Section 5.1 for details). In particular, C50 is chosen equal to 100 nF and R8/R7 in the ballpark of tens—even hundreds—of kΩ, depending on the delay necessary to avoid a false OTP trip.

$$V_{OUT} = 1.8639 - \left(1.15 \times 10^{-2} \times \text{T}\right) - \left(3.88 \times 10^{-6} \times \text{T}^2\right) = 1.8639 - 1.38 - 0.0559 = 428\ \text{mW}$$

  for example, setting the threshold at 120°C leads to

$$428\ \text{mW} = 2.5\ \text{V} \times \frac{\text{R68}}{\text{R71} + \text{R68}} \rightarrow \text{R71} = 100\text{K},\ \text{R68} = 484\text{K}$$

- *Overvoltage Indicator*
  OVP threshold is set at VBUS = 84 V through resistor divider R65 to R72:

$$84\ \text{V} \times \frac{\text{R72}}{(\text{R65} + \text{R66} + \text{R72} + \text{R69})} = 84\ \text{V} \times \frac{3.09\text{K}}{(49.9\text{K} + 49.9\text{K} + 3.09\text{K} + 1\text{K})} = 2.498\ \text{V} \tag{15}$$

  On the same divider the VBUS sense for the VFF feature is achieved. Indeed:

$$84\ \text{V} \times \frac{(\text{R72} + \text{R69})}{(\text{R65} + \text{R66} + \text{R72} + \text{R69})} = 84\ \text{V} \times \frac{4.09\text{K}}{(49.9\text{K} + 49.9\text{K} + 3.09\text{K} + 1\text{K})}$$

All the outputs of the comparators are OR-wired and feed the OVS pin of the drivers to turn them off. To add a latching feature on the protection (so that a power cycle needs to be performed to clear the protection latch), a D-Type Flip-Flop With Asynchronous Clear (the TI SN74LVC1G175) is adopted. 4 V is selected as the supply voltage of the flip-flop because the internal comparator on the OVS pin of the SM72295 drivers are clamped to VDD; the voltage on these pins has to be higher than VDD itself, meaning it is not recommended to use the 3.3-V rail to supply the flip-flop.

NOTE: The LM2901V is used as a comparator. It is one of the most affordable on the market and, because of that, not the fastest one. This also helps avoid triggering false protection conditions due to potential noise. Also, for the same reason, no hysteresis has been added to the comparator, but a latching protection is preferred.

2.4 3.3-V I/O Host Processor Interface

A host processor is needed to provide the right PWM sequence to the driver and then step the motor. A bunch of I/Os need to be connected to the TIDA-00365 design; in particular:

- Eight digital inputs (PWMs) for the total eight FET of the one full-bridges (the TIDA-00365 digital input, CMOS level)
- Eight analog outputs including:
  - the high-side currents in the phases of the stepper motor
  - the DC_Link voltage for the VFF function
  - the two phase terminal voltages, for the BEMF analysis

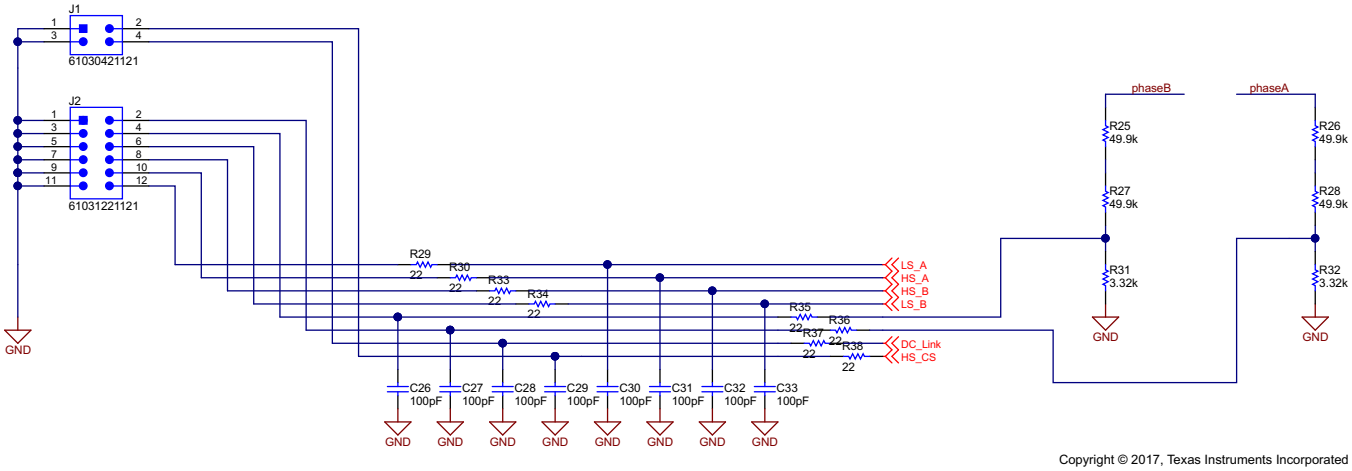


Figure 14. TIDA-00365 Host Processor Interface

The motor terminal voltage phase A and phase B is scaled by 3.3/100 so that 100-V DC voltage yields 3.3 V at the host processor interface.

$$100\ \text{V} \times \frac{3.4\text{K}}{(49.9\text{K} + 49.9\text{K} + 3.4\text{K})} = 3.295\ \text{V} \tag{16}$$

An HF filter with 22R/100 pF is applied on all the I/Os to limit noise on these signals.

3 Getting Started Hardware

Figure 15 shows an overview of the board and its main functional areas.

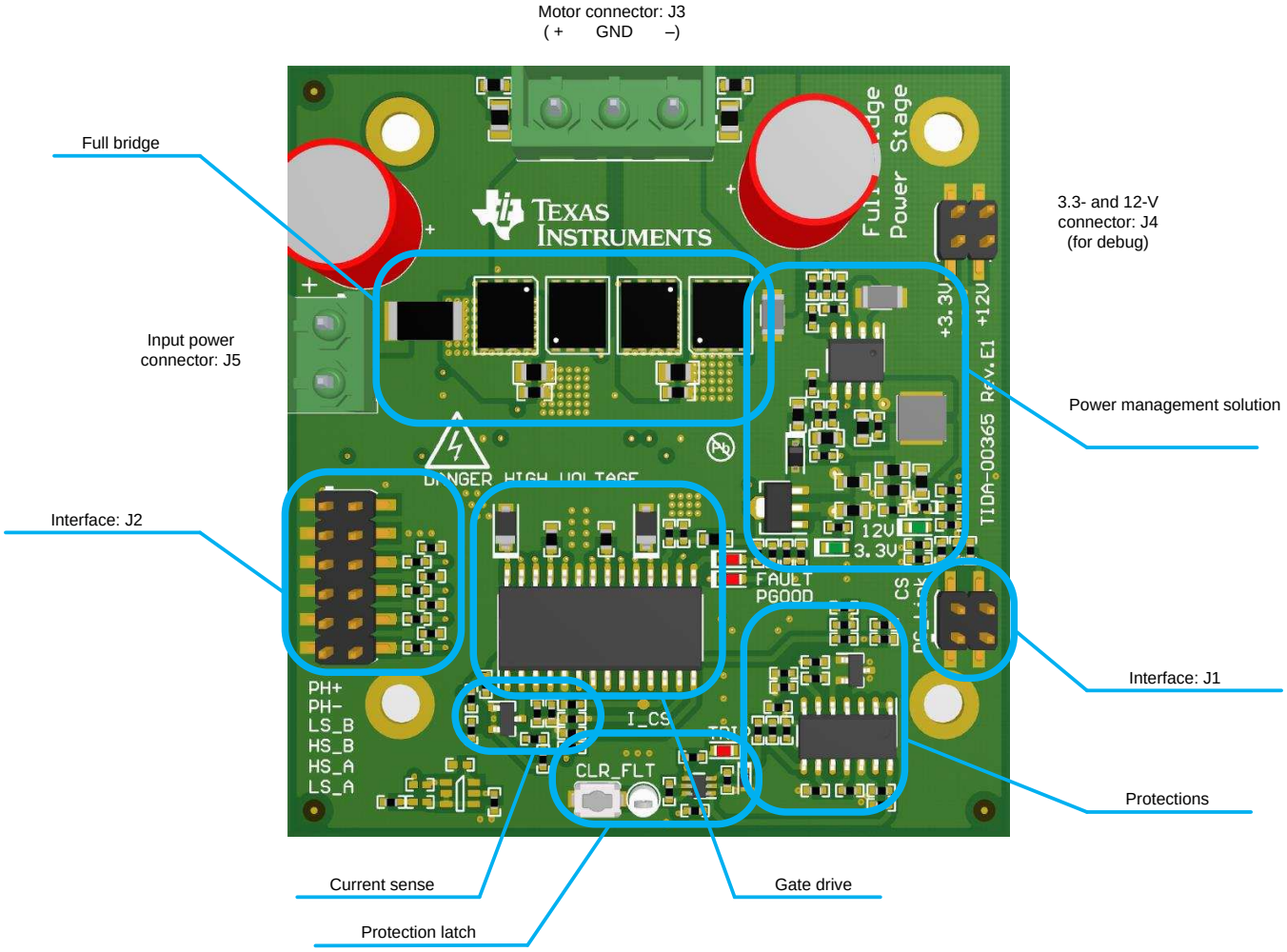


Figure 15. TIDA-00365 Functional Blocks (Top View)

Furthermore, note that the four mounting holes have been placed in a relative position to match a potential heat-sink (the Wakefield Engineering 518-95AB) that could be connected on the bottom in case of thermal problems.

Table 2 through Table 6 detail the pin assignments on the connectors.

Table 2. Interface J1

J1 PIN	FUNCTION	J1 PIN	FUNCTION
1	GND	2	DC_Link voltage
3	GND	4	Phase current

Table 3. Interface J2

J2 PIN	FUNCTION	J2 PIN	FUNCTION
1	GND	2	LS_A
3	GND	4	HS_A
5	GND	6	HS_B
7	GND	8	LS_B
9	GND	10	Phase voltage B–
11	GND	12	Phase voltage A

Table 4. Interface J3

J3 PIN	FUNCTION
1	Phase B
2	GND
3	Phase A

Table 5. Interface J4

J4 PIN	FUNCTION	J2 PIN	FUNCTION
1	GND	2	12-V rail
3	GND	4	3V3 rail

Table 6. Interface J5

J5 PIN	FUNCTION
1	DC link
2	GND

4 Testing and Results

4.1 Test Setup

Table 7. Test Equipment for TIDA-00365

TEST EQUIPMENT	PART NUMBER
Low-speed oscilloscope (suitable for power management tests)	Tektronix TDS2024B
High-speed oscilloscope (suitable for analog signal tests)	Tektronix TDS784C
Adjustable SMPS	Knuerr-Heinzinger Polaris 125-5
True RMS multimeter	Fluke 179
Differential probes	Tektronix P6630
Single ended probes (2×)	Tektronix P6139A
Current probe	Tektronix TCPA300
Current probe	PR30 LEM
Thermal camera	Fluke TI40
Full bridge driver for DC motor (2×)	TIDA-00365
MCU	C2000 LaunchPad™
Brushed DC motor	RX330CR1000
Load emulator	3 × 1-Ω and 10 mH in series

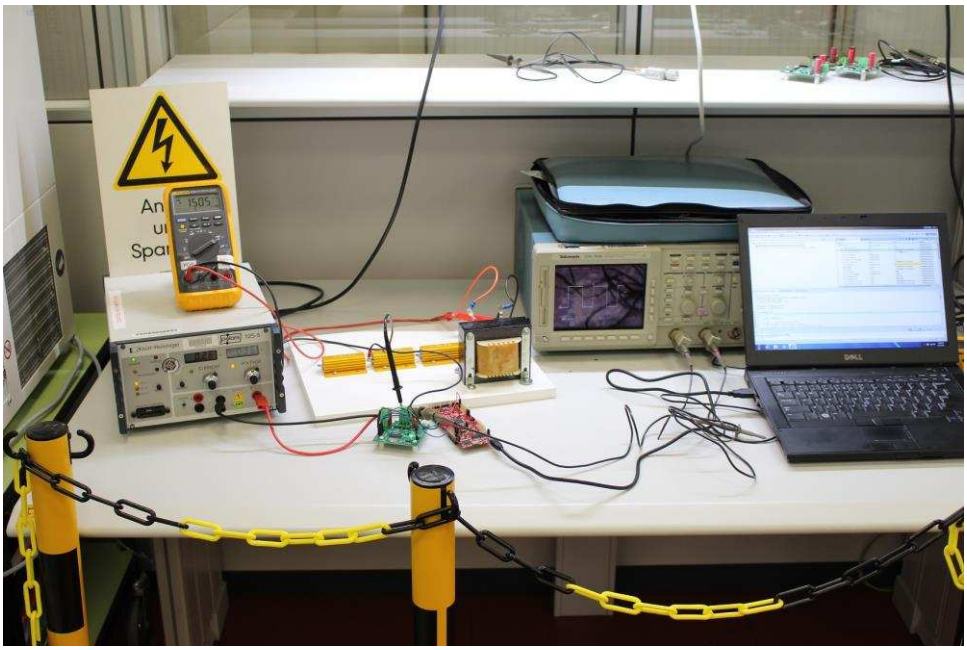


Figure 16. TIDA-00365 Test Setup With Load Emulator

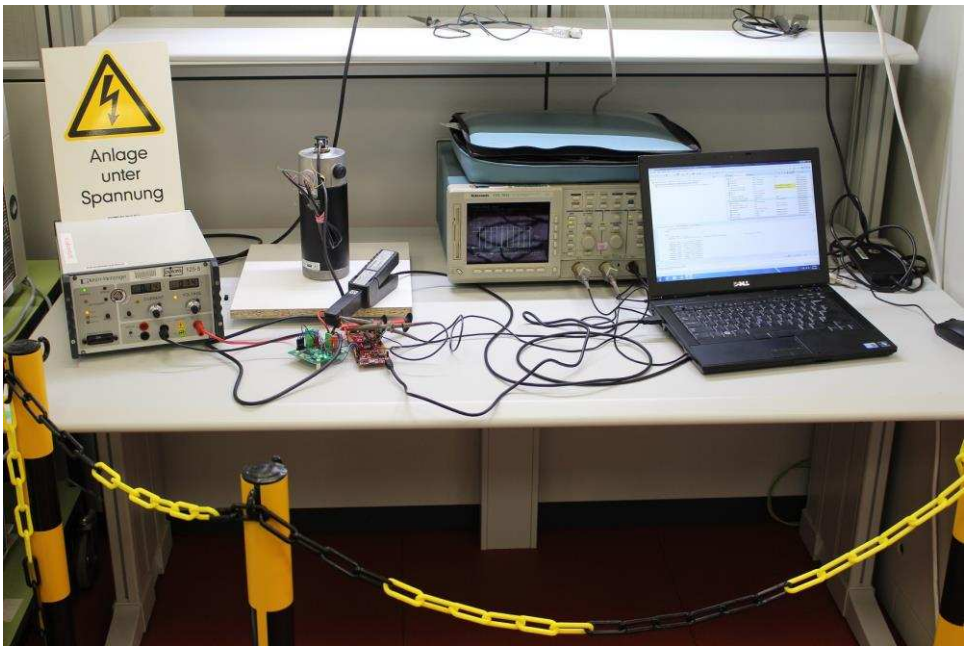


Figure 17. TIDA-00365 Test Setup With Brushed DC Motor

The InstaSPIN-MOTION™ LaunchPad with the TMS320M28069M was used generate the complementary PWM (hard-chopping) for the TIDA-00365 full-bridge power stage and measure the phase current. A closed loop current control was implemented as well. Figure 18 shows the corresponding connections.

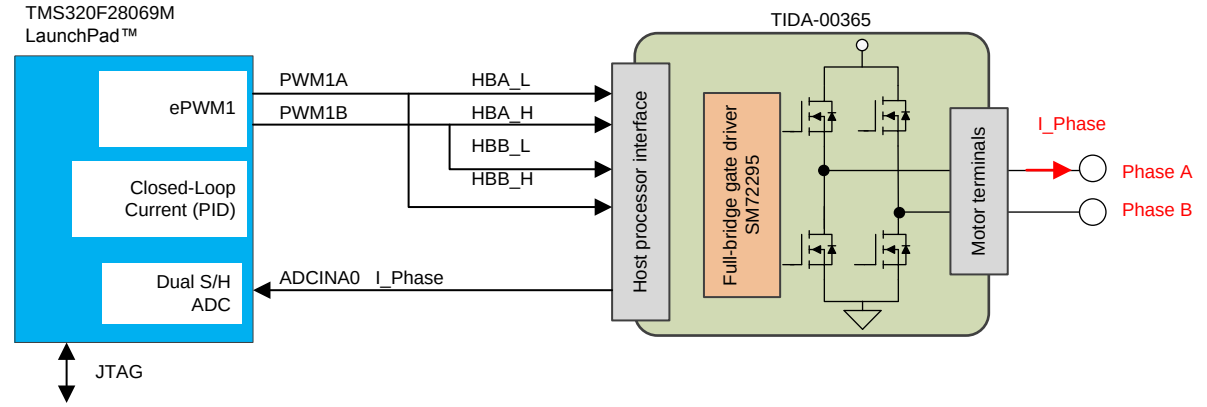


Figure 18. InstaSPIN-MOTION LaunchPad Connection to TIDA-00365 Full-Bridge

The TMS320F28069M was configured as follows:

- PWM1A/PWM1B: Complementary active high symmetric PWM with a 25-kHz period and 100-ns deadband for both rising and falling edge delay.
- The phase current was sampled at 25 kHz at the center of the PWM cycle, when there is no switching.
- PI controllers with anti-reset windup for closed-loop phase current control

4.2 Power Management

A minimum set of tests on the power management solution has been performed. More in particular the performance of LM5018 could be evaluated looking at the LM5018 user's guide (SNVA666).

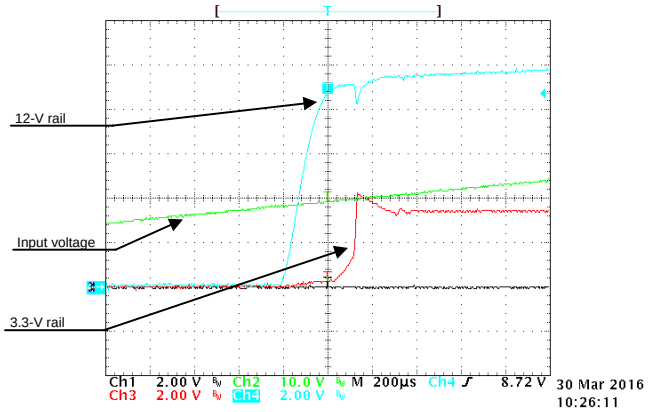


Figure 19. Point-of-Load Power-Up at 50-V DC Input

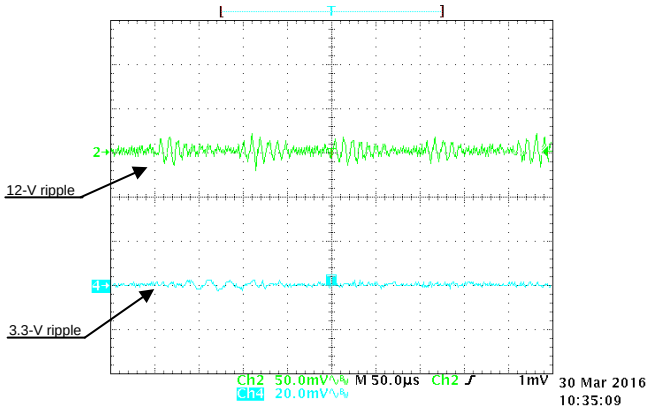


Figure 20. Point-of-Load Voltage Ripple at 3.3-V and 12-V at Nominal Operation

Line and load regulations show that the 3.3 V and 12 V are all the time well regulated, meaning in the range of nominal voltage ±5%. Consumption at nominal operating conditions is below 10 mA on both rails.

4.3 Full Bridge Driver

Note that the phase current in the following test pictures has been measured using a current sense probe with voltage output and a trans-impedance gain of 1 V/10 A (ideal).

If not otherwise specified, all the tests have been performed at a 75-V input, 10-A output PWM frequency: 25 kHz.

4.3.1 PWM—Gate Driver

This section shows the SM72295 gate driver output voltage measured at the SN72295 gate driver output versus DC-(GND) with complementary PWM input signals with a 100-ns dead band.

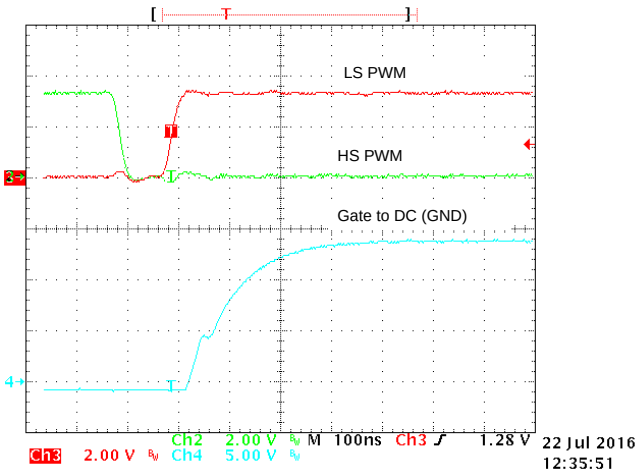


Figure 21. SM72295 Low-Side Gate Driver Output Voltage During Turnon

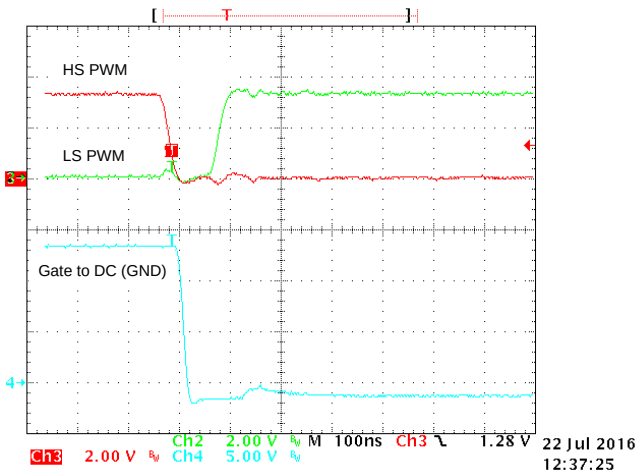


Figure 22. SM72295 Low-Side Gate Driver Output Voltage During Turnoff

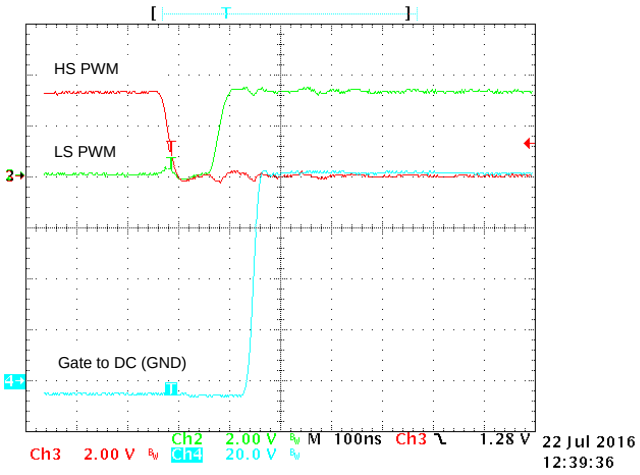


Figure 23. SM72295 High-Side Gate Driver Output Voltage versus GND During Turnon

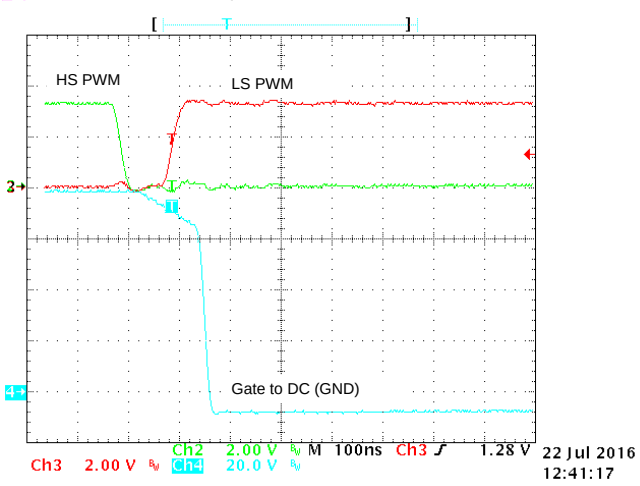


Figure 24. SM72295 High-Side Gate Driver Output Voltage versus GND During Turnoff

4.3.2 PWM—Gate Driver to Switch Node (Half Bridge)

This section shows the SM72295 gate driver output voltage measured at the SN72295 gate driver output versus the switch node voltages phase A and Phase B of the H-bridge power MOSFETs. The test was done at a 75-V DC input and various positive and negative load currents to illustrate the hard- and soft turnon switching of a full-bridge configuration driving a brushed DC motor.

Figure 25 shows the soft turnon switching of the low-side FET. Figure 26 shows the hard turnon switching of the high-side FET.

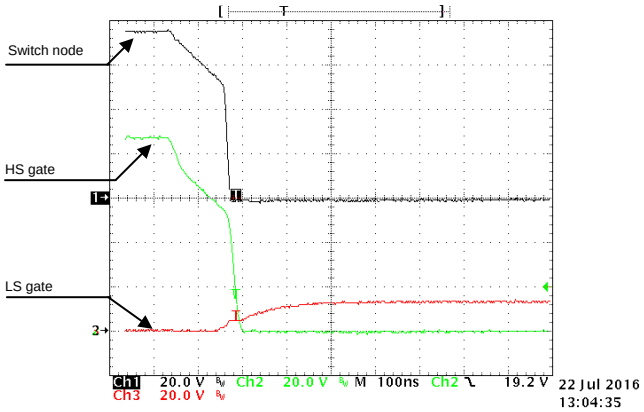


Figure 25. Phase A Falling Switch Node Voltage, High-Side, and Low-Side Gate to GND at 1-A Output Current

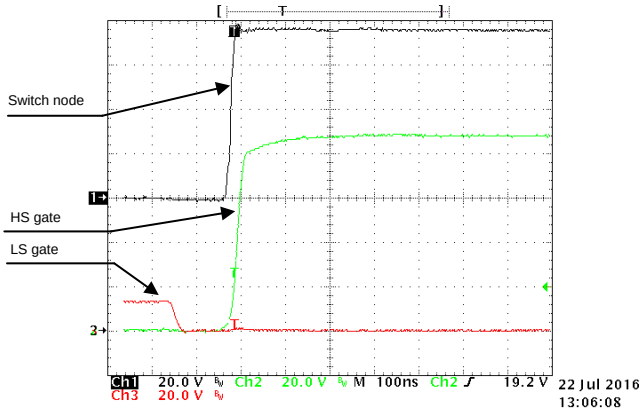


Figure 26. Phase A Rising Switch Node Voltage, High-Side, and Low-Side Gate to GND at 1-A Output Current

Figure 27 shows the soft turnon switching of the high-side FET. Figure 28 shows the hard turnon switching of the low-side FET.

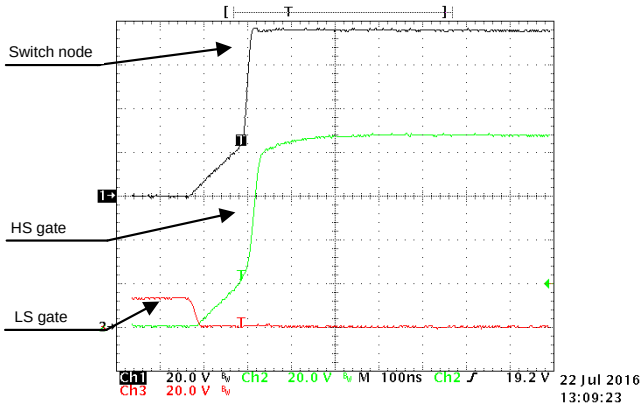


Figure 27. Phase A Rising Switch Node Voltage, High-Side, and Low-Side Gate to GND at –1-A Output Current

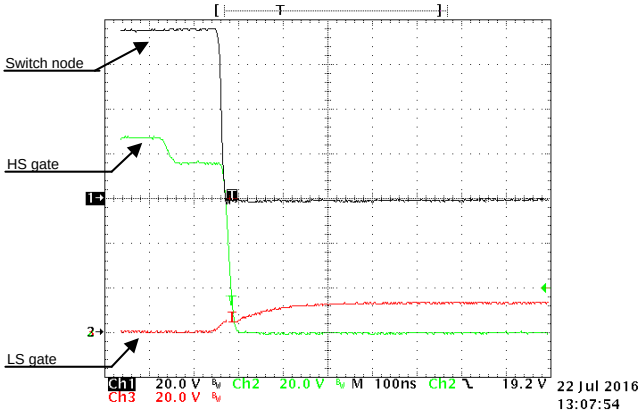


Figure 28. Phase A Falling Switch Node Voltage, High-Side, and Low-Side Gate to GND at –1-A Output Current

Figure 29 shows the soft turnon switching of the low-side FET. Figure 30 shows the hard turnon switching of the high-side FET.

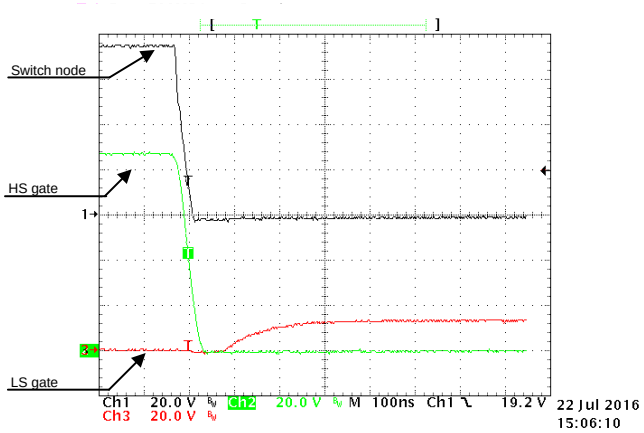


Figure 29. Phase A Falling Switch Node Voltage, High-Side, and Low-Side Gate to GND at 10-A Output Current

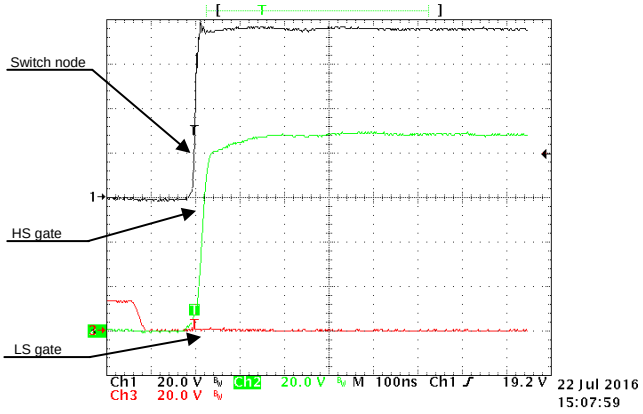


Figure 30. Phase A Rising Switch Node Voltage, High-Side, and Low-Side Gate to GND at 10-A Output Current

Figure 31 shows the soft turnon switching of the high-side FET. Figure 32 shows the hard turnon switching of the low-side FET.

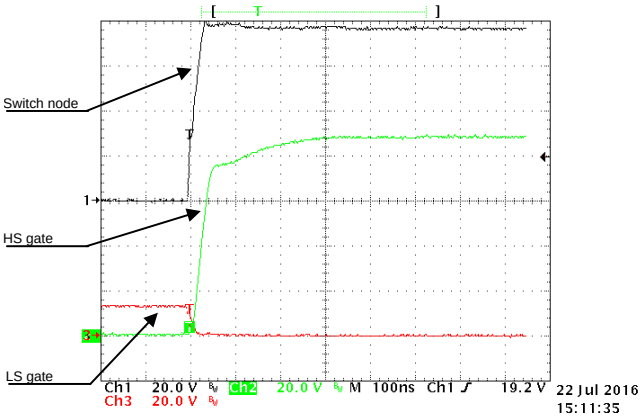


Figure 31. Phase A Rising Switch Node Voltage, High-Side, and Low-Side Gate to GND at –10-A Output Current

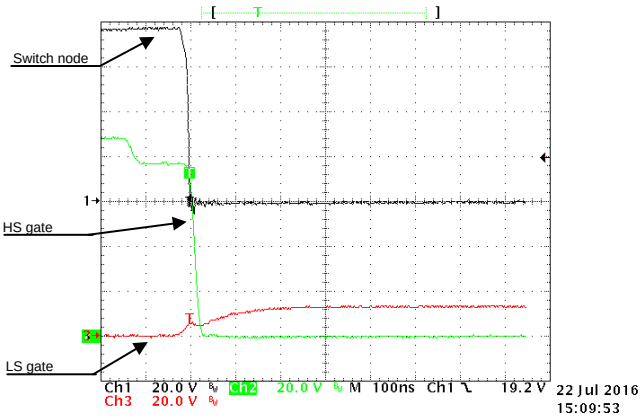


Figure 32. Phase A Falling Switch Node Voltage, High-Side, and Low-Side Gate to GND at –10-A Output Current

The figures in this section show that the full-bridge switching exhibits hard-switching of MOSFETs as well as soft switching depending on the output current. Also, the Miller capacity impact on the gate to source voltage can be seen: a faster transition with higher currents.

4.3.3 Phase Voltages and Output Current

This section shows the output phase voltages (switch node voltages) of the full-bridge measured at the motor terminals Jxx along with the output current. For these tests, the load emulator was used.

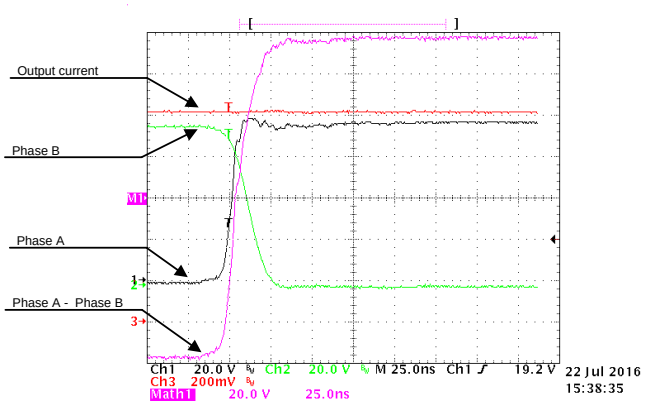


Figure 33. Rising Edge of Output Voltage, Phase A and B Voltage to GND at 10-A Output Current

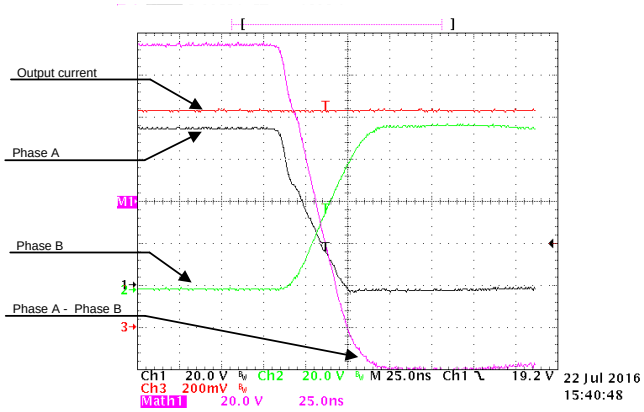


Figure 34. Falling Edge of Output Voltage, Phase A and B Voltage to GND at 10-A Output Current

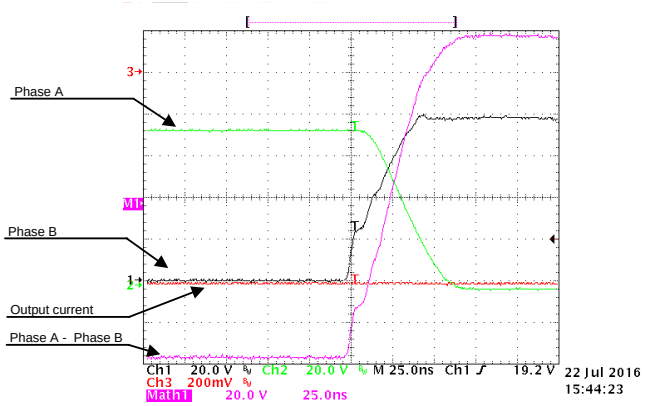


Figure 35. Rising Edge of Output Voltage, Phase A and B Voltage to GND at –10-A Output Current

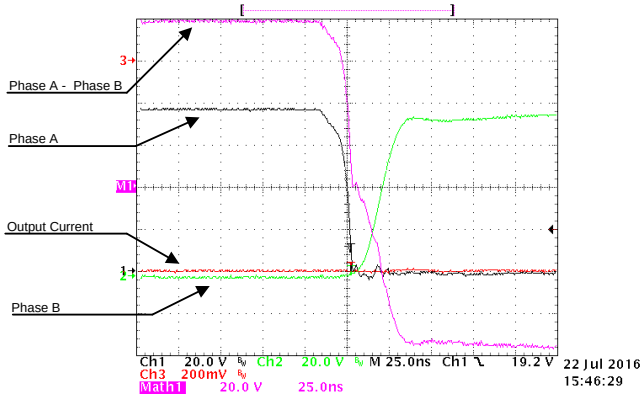


Figure 36. Falling Edge of Output Voltage, Phase A and B Voltage to GND at –10-A Output Current

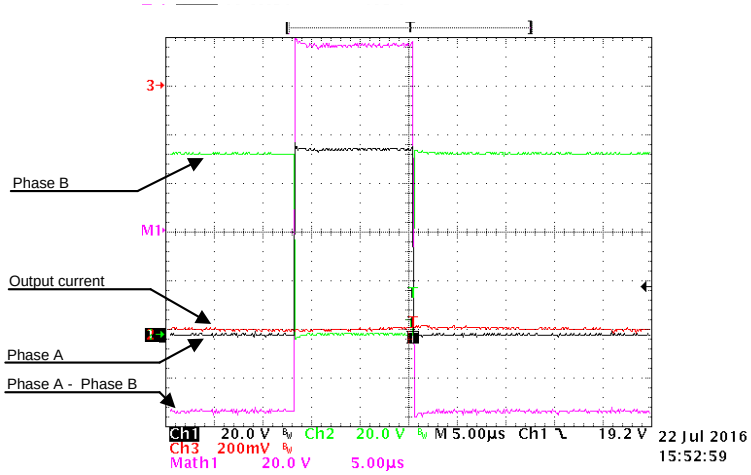


Figure 37. Output Voltage, Phase A and B Voltage to GND at –10-A Output Current Over One PWM Cycle

4.4 High-Side Current Sense and Phase Voltage Sense

To evaluate the performance of the high-side current sense using the dual high-side amplifiers integrated in the SM72295 full-bridge gate driver, the InstaSPIN-MOTION LaunchPad with the TMS320M28069M was used to sense and control the phase current of the TIDA-00365 full-bridge power stage. The following parameters have been used:

- DC-link voltage: VDC = 75 V
- PWM frequency = 25 kHz
- PWM type: Bipolar switching
- PI current control at 25 kHz, phase current measurement triggered at PWM center
- Programmable phase current magnitude (torque)
- Load emulator, 3-Ω in series with 10 mH

The following figures show the transient response of the high-side current sense amplifier output using the SM72295 dual high-side amplifiers. The analog signal was measured at the pin J5-2. Additionally, the phase current of the DC motor winding was measured with an LEM current probe as well as the low-side PWM signal of one half-bridge at Pin J7-12 (ePWM1A).

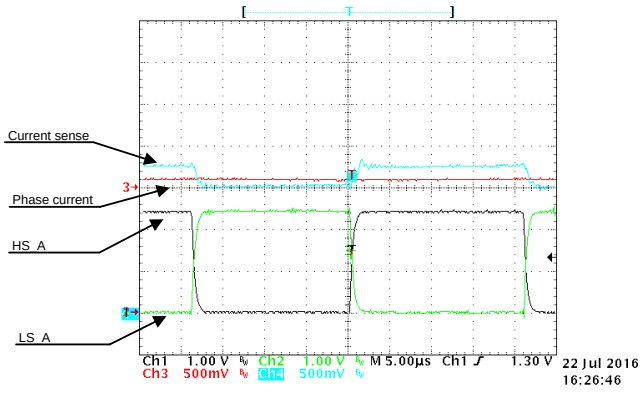


Figure 38. Host Interface Analog Signals, Current Sense Amplifier at J2-2 With I_ref 1 A at 25-kHz PWM, Phase A and Phase B J2-2

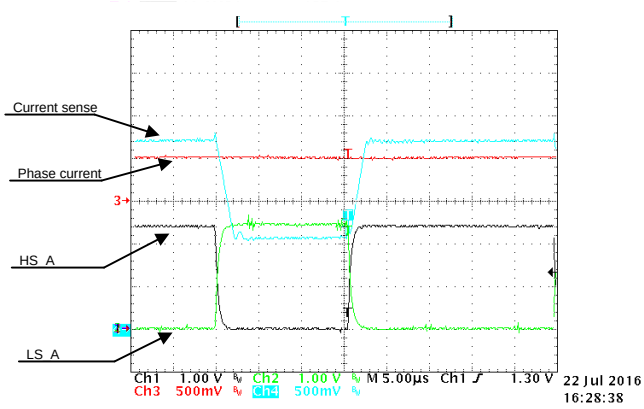


Figure 39. Host Interface Analog Signals, Current Sense Amplifier at J2-2 With I_ref 5 A at 25-kHz PWM, Phase A and Phase B J2

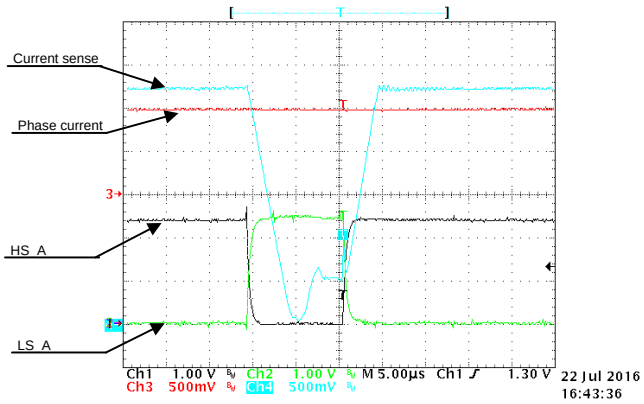


Figure 40. Host Interface Analog Signals, Current Sense Amplifier at J2-2 With I_ref 10 A at 25-kHz PWM, Phase A and Phase B J2

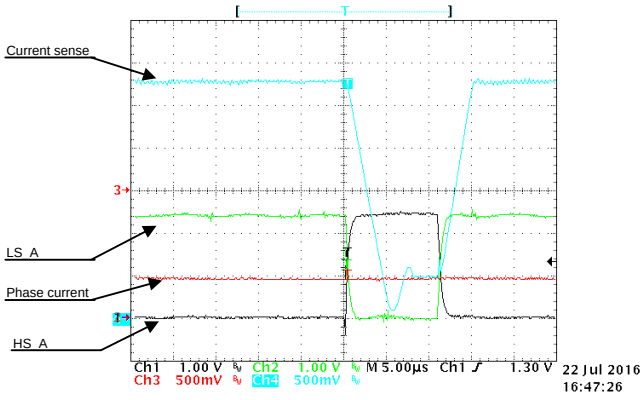


Figure 41. Host Interface Analog Signals, Current Sense Amplifier at J2-2 With I_ref –10 A at 25-kHz PWM, Phase A and Phase B J2

The slew rate of the SM72295 integrated amplifiers of around 1 V/µs will limit the minimum PWM duty cycle to sense the high-side current to around 3 µs at worst case to be able to sense maximum current amplitudes. To reduce the minimum PWM duty cycle further, the gain can be reduced, which reduces the voltage swing respectively to mitigate the slew rate. For example, by reducing the gain by 50% the minimum duty cycle will be reduced to around 1.5 µs; however, the signal-to-noise ratio drops by 6 dB. Hence it is a trade-off between accuracy and minimum duty cycle.

The following figures show the measured average phase current (using a Fluke ampere meter) versus the high-side current sense output voltage measured at connector J2-2 and sampled center aligned to the PWM on the TMS320F28069M MCU.

The absolute error within the ±5-A range for the winding current remains below 100 mA, which is less than 0.4% with respect to the full-scale range of 30 A (–15 to 15 A).

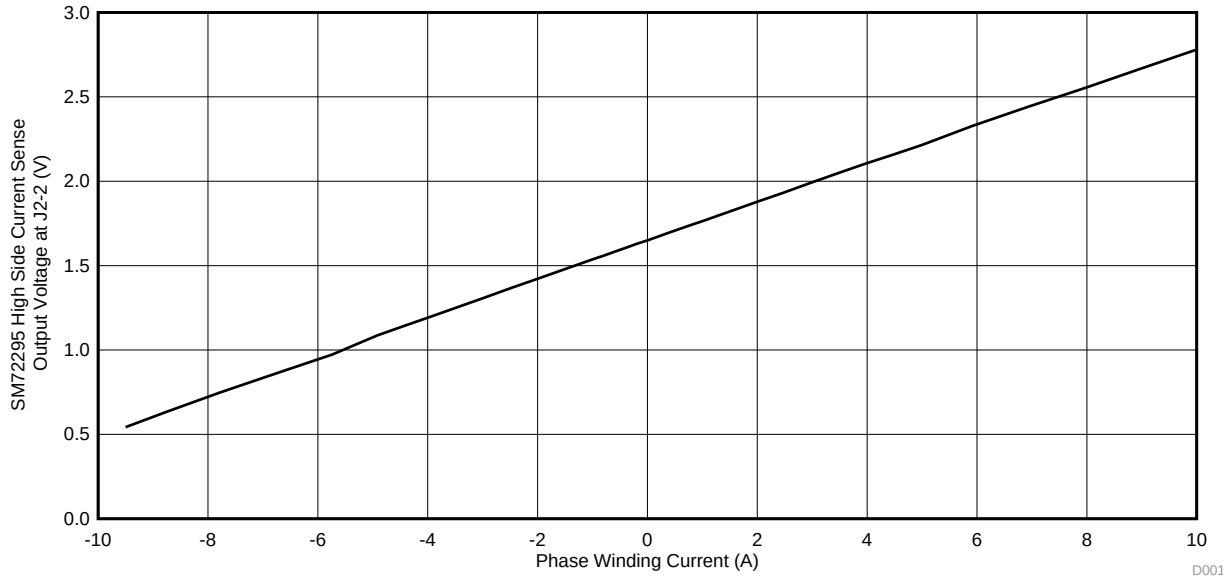


Figure 42. SM72295 Current Sense Amplifier Output Voltage at J5-2 Sampled at PWM Center versus Measured Phase Winding Current (Fluke Ampere Meter)

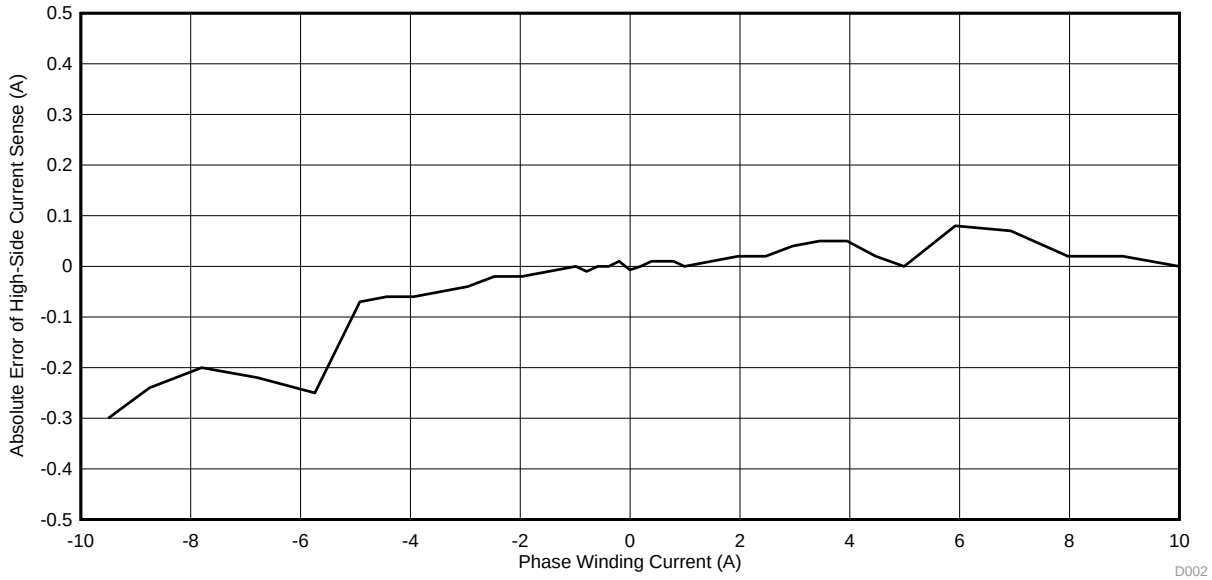


Figure 43. Absolute Error (in A) of SM72295 Current Sense Amplifier Output

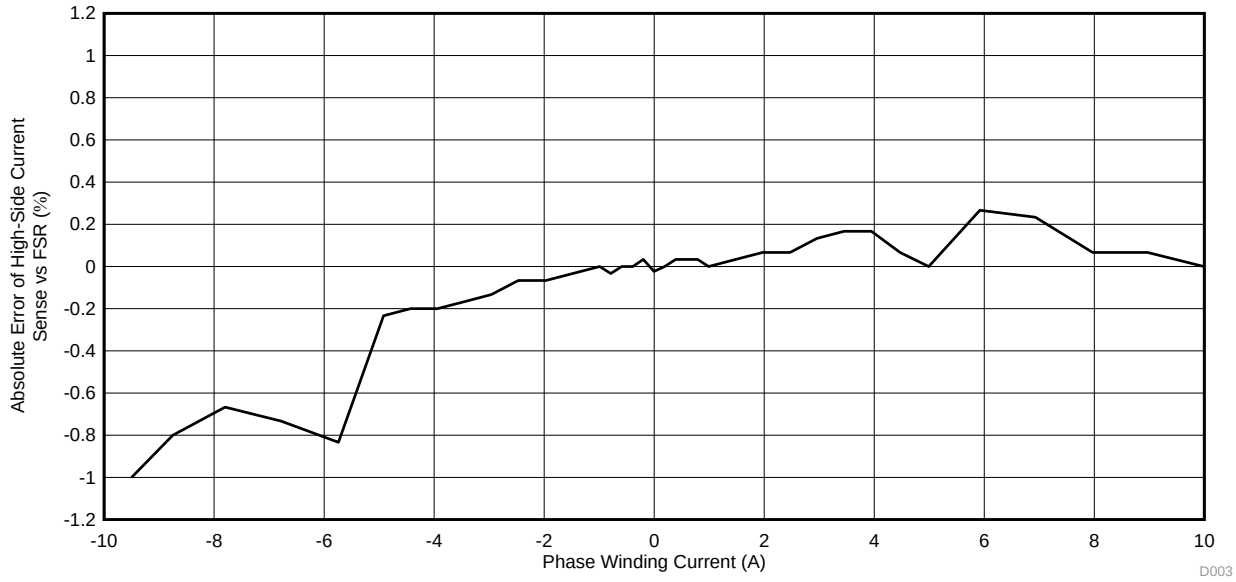


Figure 44. Absolute Error versus Full-Scale Range (–15 to 15 A in %) of SM72295 Current Sense Amplifier Output

4.5 Thermal Performance Without Heat Sink

The efficiency at a 75-V DC input and maximum load current of 10 A with a 25-kHz PWM is estimated using the thermal picture.

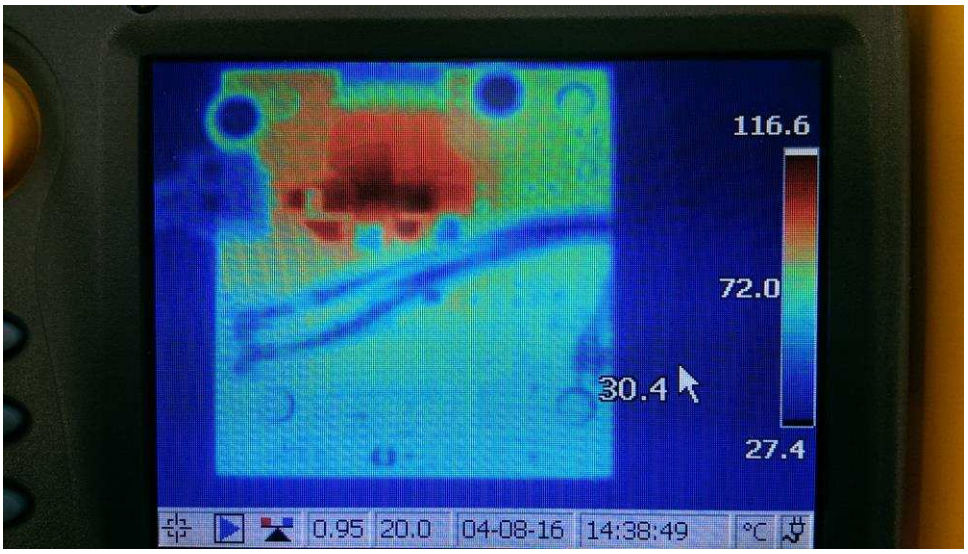


Figure 45. Peak Temperature of TIDA-00210 at 75 V, 10 A, No Air Cooling, No Heat Sink

The peak case temperature detected at a 75-V input, 10-A phase current is < 120°C. The worst case efficiency at 116°C junction temperature can be estimated as follows:

$$\text{Efficiency} = \frac{P_{OUT}}{P_{IN}} = \frac{\left(P_{IN} - P_{Losses}\right)}{P_{IN}} = 1 - \frac{P_{Losses}}{P_{IN}} \tag{17}$$

$$P_{IN} = 75\ \text{V} \times 1.03\ \text{A} = 77\ \text{W}$$

$$P_{Losses} \approx 4 \times \text{PonFET}$$

$$P_{LossOnFET} = P_{Switching} + P_{Conduction} + P_{DeadTime}$$

$$= V_{DS} \times I_{Phase} \times f_{SW} \times \frac{\left(T_{Rise} + T_{Fall}\right)}{2} + R_{DSon} \times I_{Phase}^2 \times D + V_F \times I_{Phase} \times f_{SW} \times T_{DeadTime} \tag{18}$$

$$= 75\ \text{V} \times 10\ \text{A} \times 25\ \text{kHz} \times 25\ \text{ns} + 22\ \text{m}\Omega \times 100\ \text{A}^2 \times 0.5 + 1\ \text{V} \times 10\ \text{A} \times 25\ \text{kHz} \times 100\ \text{ns}$$

$$= 0.46\ \text{W} + 1.1\ \text{W} + 0.02\ \text{W} = 1.58\ \text{W}$$

That is less than half of the package capability.

$$P_{Losses}\ (116°\text{C, 25 kHz PWM}) \approx 4 \times \text{PonFET} \approx 6.32\ \text{W}$$

$$\text{Efficiency}\ (116°\text{C, 25 kHz PWM}) = 1 - \left(\frac{6.32\ \text{W}}{77\ \text{W}}\right) \approx 92\%$$

Because the R_{DSon} is temperature dependent and the typical use case would be with heatsink, the maximum efficiency can be achieved at 25°C.

$$= 75\ \text{V} \times 10\ \text{A} \times 25\ \text{kHz} \times 25\ \text{ns} + 12\ \text{m}\Omega \times 100\ \text{A}^2 \times 0.5 + 1\ \text{V} \times 10\ \text{A} \times 25\ \text{kHz} \times 100\ \text{ns}$$

$$= 0.46\ \text{W} + 0.6\ \text{W} + 0.02\ \text{W} = 1.08\ \text{W}$$

$$P_{Losses}\ (25°\text{C, 25 kHz PWM}) \approx 4 \times \text{PonFET} \approx 4.32\ \text{W}$$

$$\text{Efficiency}\ (25°\text{C, 25 kHz PWM}) = 1 - \left(\frac{4.32\ \text{W}}{77\ \text{W}}\right) \approx 94.4\%$$

With a 16-kHz PWM, the efficiency is:

$$\text{Efficiency}\ (25°\text{C, 16 kHz PWM}) = 1 - \left(\frac{3.72\ \text{W}}{77\ \text{W}}\right) \approx 95.2\%$$

Higher efficiency can be achieved by using NexFET power MOSFET CSD19533Q5A or the CSD19532Q5A with even lower R_{DS_ON}.

4.6 Brushed DC Motor Tests

The following tests where done to evaluate the performance of TIDA-00365 full-bridges connected to a high torque, high power brushed DC motor. The motor current was measured with the high-side current sense using the dual high-side amplifiers integrated in the SM72295. The motor was run in current (torque) control mode. The current was togged between positive and negative magnitude. The following parameters have been used:

- DC-link voltage: VDC = 75 V
- PWM frequency = 25 kHz
- PWM type: Bipolar switching
- PI current control at 25 kHz, phase current measurement triggered at PWM center
- Phase current toggling between negative and positive reference current at 80 ms
- Load: DC servo motor RX330CR1000 (Parker Hannifin), no load torque

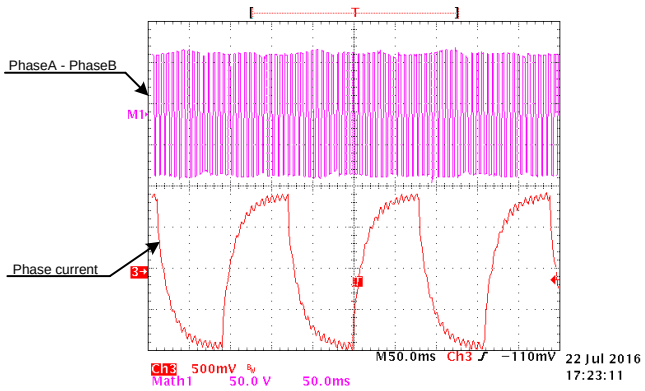


Figure 46. Full-Bridge Output Voltage and Output Current at ±9.4-A Current Magnitude Toggling at 80 ms

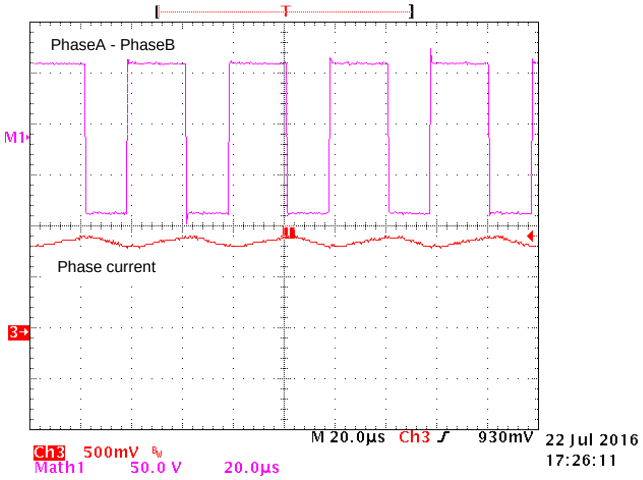


Figure 47. Zoom Into Figure 46

4.7 Protections

4.7.1 Undervoltage Lockout (UVLO)

The UVLO has been implemented based on the UVLO feature of the LM501x family. This provides indeed the 12-V rails for the gate driver and also generates the 3.3 V (from the LDO LM317) that enables the host processor interface.

By design, UVLO is set at 18 V (rising input voltage) with an hysteresis of 2 V, meaning that the turnoff threshold (falling UVLO) is around 16 V nominal.

The values measured during test bench session are 18.2 V and 15.6 V, respectively.

4.7.2 Overvoltage Indicator (OVI)

OVI threshold has been set at 85 V nominal.

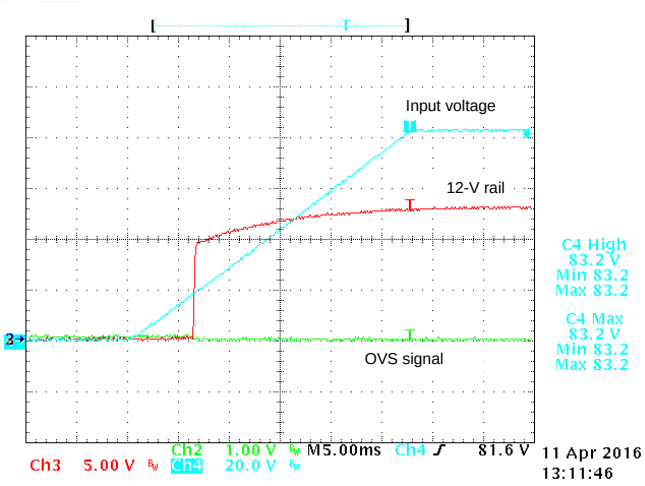


Figure 48. Start-Up Voltage at 84-V Input; CH4 = Vin, CH3 = 12-V Rail, CH2 = OVS Signal (See Section 5.1 for Details)

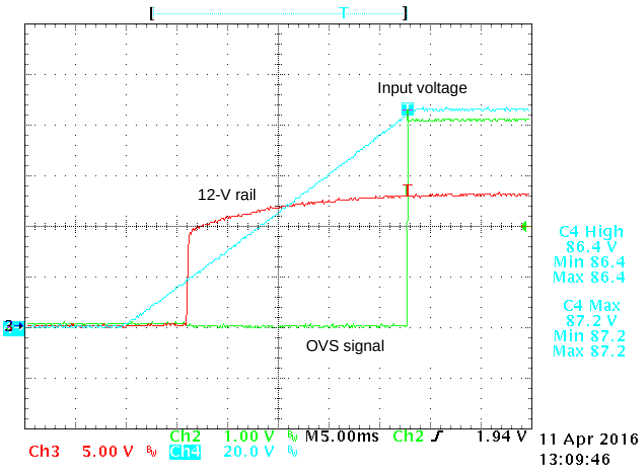


Figure 49. Start-Up Voltage at 86-V Input; CH4 = Vin, CH3 = 12-V Rail, CH2 = OVS Signal (See Section 5.1 for Details)

These waveforms show the input voltage ramp-up (blue trace), the 12-V rail (red) and the OVS signal (green trace; see Section 5.1 for details). These also show that the OVP measured level is between 83.2 V and 87.2 V (average 85.2 V, as expected).

4.7.3 Short-Circuit Protection (SCP)

In order to test the short-circuit protection and trip response time of the design, the following short-circuit conditions were tested, as illustrated in Figure 50:

- Short between the motor terminals Phase_A and Phase B (see Figure 51)
- Short between from motor terminals Phase_A to GND (see Figure 52)
- Short between from motor terminals Phase_B to GND (see Figure 53)

The input voltage was 75 V and the C2000 MCU was configured 50% duty cycle at low 1-kHz PWM to force an overcurrent condition over a longer period. A current probe with 100 mV/A was used.

Note that the current was limited to 28-A due to the capabilities of the selected 75-V DC power supply.

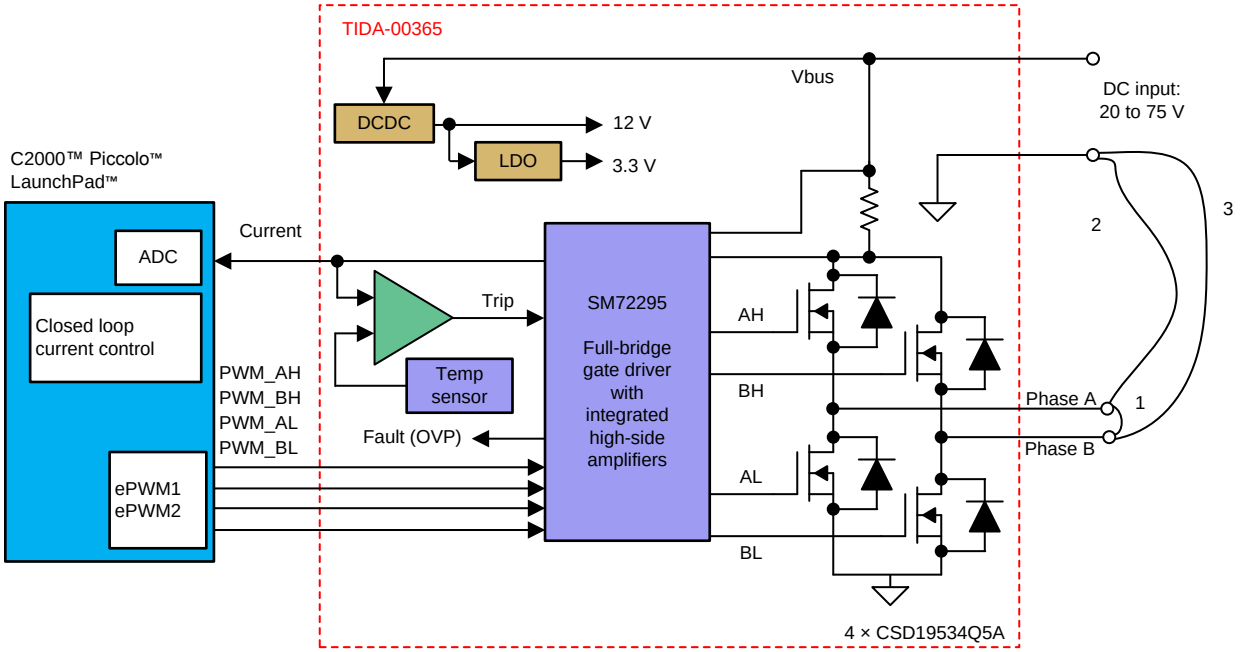


Figure 50. TIDA-00365 Short-Circuit Test Setup

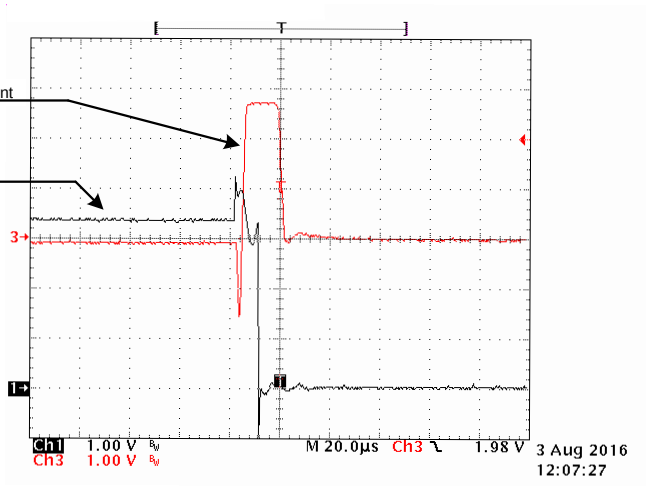


Figure 51. Short-Circuit Current Between Motor Terminals Phase A to Phase B and SM72295 nFAULT Signal

The nFAULT signal of the SM72295 gate driver is triggered in less than 10 µs after the output current exceeds the threshold of 16 A. The power FETs are turned off within 10 µs.

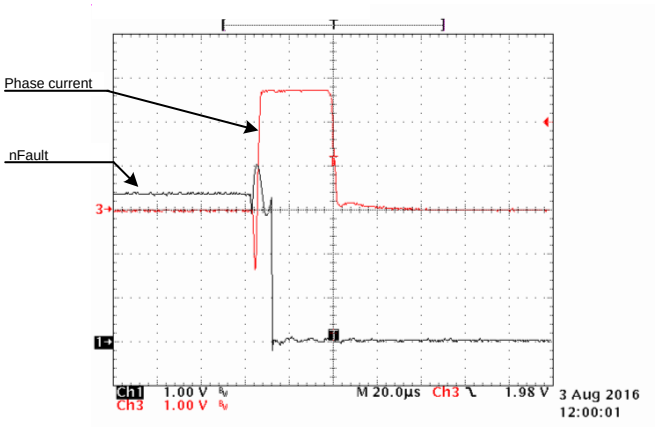


Figure 52. Short-Circuit Current Between Motor Terminal Phase A to GND and SM72295 nFAULT Signal

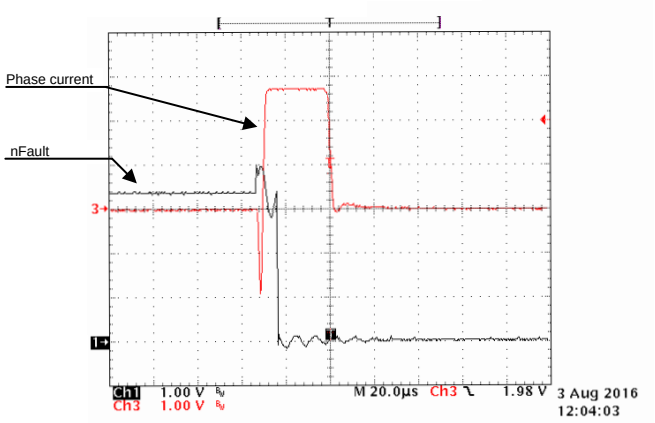


Figure 53. Short-Circuit Current Between Motor Terminal Phase B to GND and SM72295 nFAULT Signal

The nFAULT signal of the SM72295 gate driver is triggered below 10 µs after the output current exceeds the threshold of 16 A. The power FET is turned off within 25 µs.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00365.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00365.

5.3 PCB Layout Recommendations

Because of the complexity of the whole system, a complete section is dedicated to the layout design guidelines. The power management stage is not discussed in detail (see the layout guidelines in the IC datasheets) while for the motor drive power stage, see the application notes for the business units. In particular, see the following:

- *Reducing Ringing Through PCB Layout Techniques* (SLPA005)
- *Class-D Output Snubber Design Guide* (SLOA201)
- *Controlling switch-node ringing in synchronous buck converters* (SLYT465)

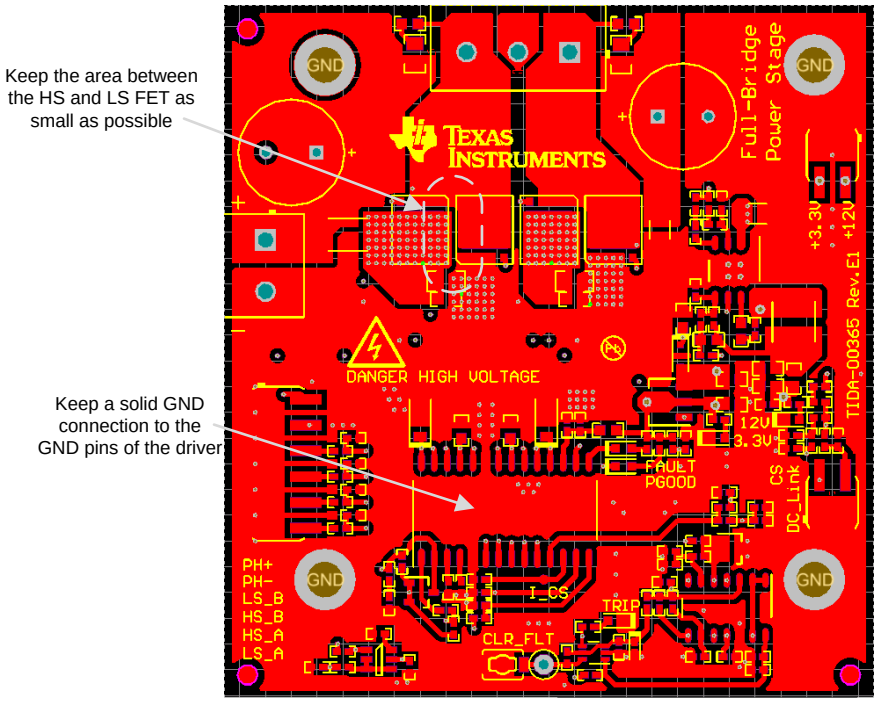


Figure 54. Top Layer

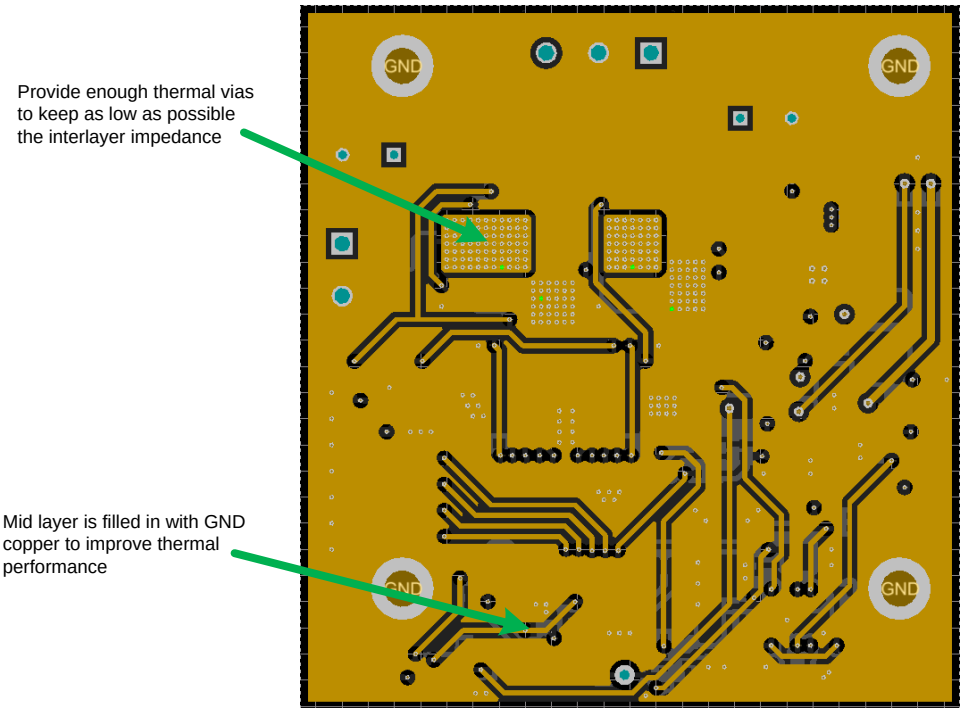


Figure 55. Mid Layer

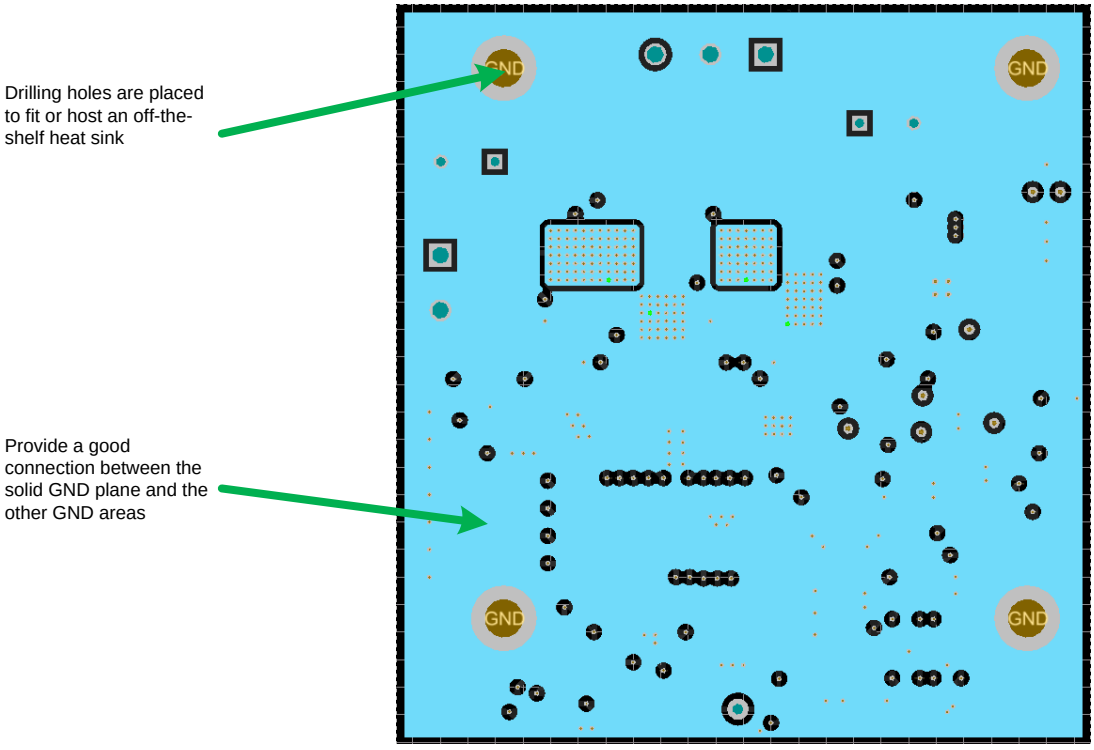


Figure 56. GND Plane

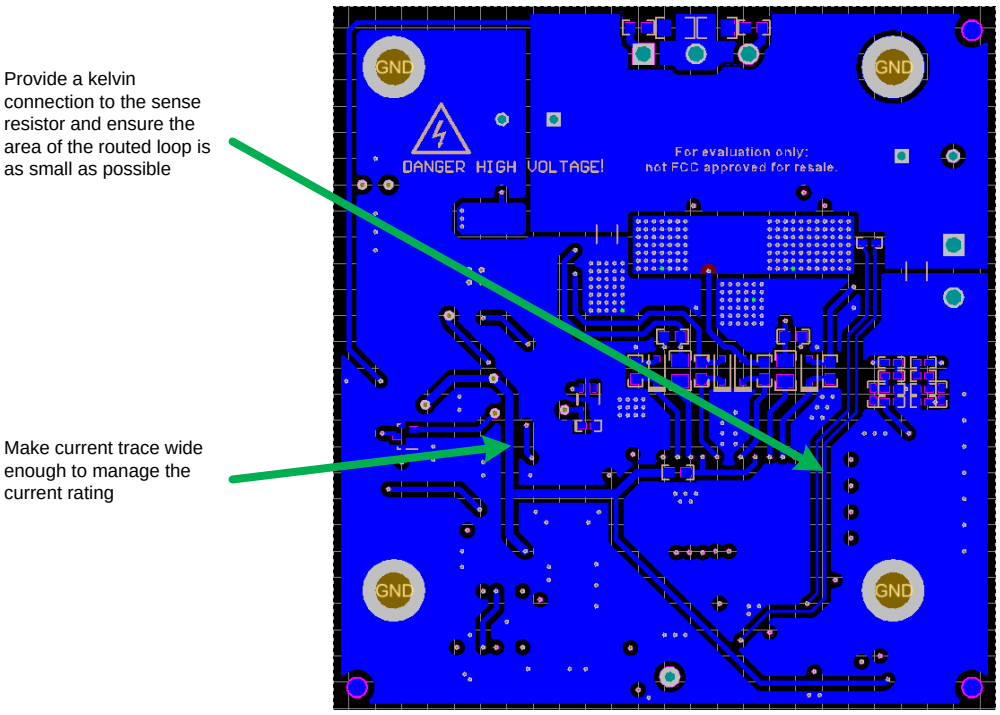


Figure 57. Bottom Layer (Flip View)

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00365.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00365.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00365.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00365.

6 Related Documentation

1. Texas Instruments, *SPICE-Based Analog Simulation Program*, TINA-TI Product Page (http://www.ti.com/tool/TINA-TI)
2. Texas Instruments WEBENCH® Design Center (http://www.ti.com/webench)
3. Texas Instruments, *Reducing Ringing Through PCB Layout Techniques*, Application Report (SLPA005)
4. Texas Instruments, *Class-D Output Snubber Design Guide*, Application Report (SLOA201)
5. Texas Instruments, *Controlling switch-node ringing in synchronous buck converters*, Application Report (SLYT465)
6. Texas Instruments, *12V to 24V, 27A Brushed DC Motor Reference Design*, TIDA-00620 Test Results (TIDUAW3)
7. Triad Magnetics Inductor, 10mH, 12.5A, 100-mΩ DC resistance (http://catalog.triadmagnetics.com/Asset/C-59U.pdf)
8. Parker Hannifin Corp., *Low-Cost DC Servo Motor RX Series*, RX330CR1000 Product Page (http://ph.parker.com/us/en/low-cost-dc-servo-motor-rx-series/rx330cr1000)

6.1 Trademarks

7 Terminology

OTP— Over-temperature protection

OCT— Overcurrent protection

UVP— Undervoltage protection

OVI— Overvoltage indication

OVP— Overvoltage protection

SCP— Short-circuit protection

FSR— Full-scale range

8 About the Authors

MARTIN STAEBLER is a system architect in the Industrial Systems-Motor Drive team at Texas Instruments, who is responsible for specifying reference designs for industrial drives.

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2016) to A Revision	Page
• Changed language and images to fit current style guide	1

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