TI Designs

600-V Unidirectional Current, Voltage, and Power Monitoring for Solar Smart Combiner Box

Overview

This reference design is a non-isolated high-side current and voltage sensing design for a smart combiner box in a grounded or ungrounded system. The current sensing topology enables non-isolated sensing for high-voltage systems.

Resources

TIDA-00639	Design Folder
OPA333	Product Folder
INA226	Product Folder
LMT84	Product Folder
TPS7A6533	Product Folder

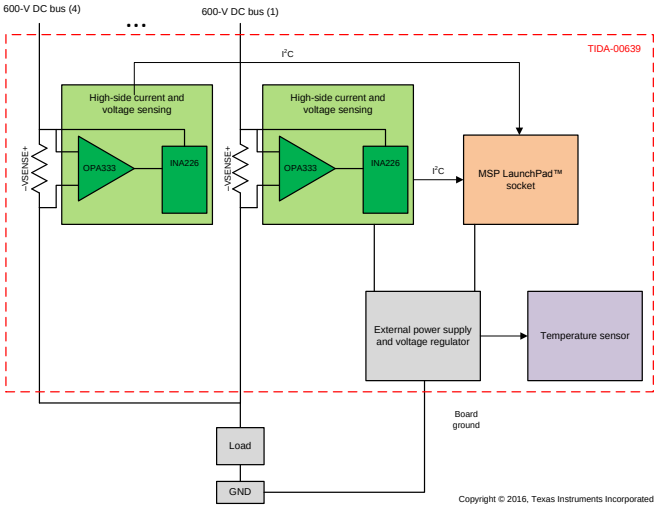
TI E2E™ Community — ASK Our E2E Experts

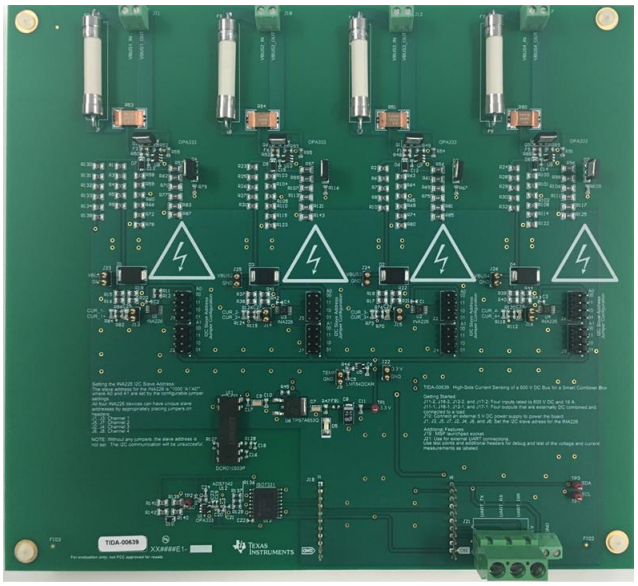
Features

- Non-Isolated High-Side Current and Voltage Monitoring of One to Four Photovoltaic Strings
- Capable of Monitoring Voltage Within ±1% Full Scale Accuracy
- Capable of Uncalibrated Current Monitoring Within ±1.25% Full Scale Accuracy and Capable of Calibrated Current Monitoring Within ±0.75% Full Scale Accuracy
- Integrates With RS-485 Communication Board
- Option to Connect Four TIDA-00639 Boards to One MCU

Applications

- Smart Combiner Box
- Solar Inverter





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1 System Overview

1.1 System Description

While the deployment of photovoltaic (PV) systems has grown exponentially over the past 10 years, solar energy still powers only a small percentage of the grid. The two major challenges are cost (amount per watt) and efficiency. When developing new solar technology (solar inverters, power optimizers, and so on), a system designer must increase efficiency through intelligent system and subsystem topologies that also decrease the cost per watt.

For PV arrays with a power capacity greater than 50 kW, it is necessary to combine the PV strings into a high-voltage direct current (DC) bus before the inverter. This system is known as a solar combiner box. The solar combiner box in relation to the solar power system is shown in Figure 1.

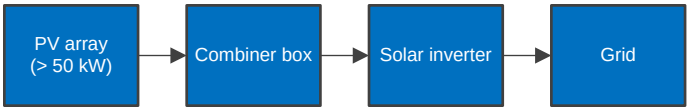

Figure 1. Solar Power System

The solar combiner box reduces the total system cost by decreasing the external cabling and copper DC buses. Solar combiner boxes are connected to one or more PV strings. One PV string is typically rated to 600-V, 1000-V, 1200-V, or 1500-V DC, and 8 to 25 A. This varies depending on the layout of the PV array and the solar power system.

Traditionally, power monitoring occurred at a multi-string level, but now, with increasing array sizes, string level power monitoring becomes critical to immediately detect a solar panel operating at a diminished capacity and the corresponding damage. The solar combiner box became the smart combiner box when current and voltage sensing technology was moved from the solar inverter (multi-string level) to the solar combiner box. The smart combiner box with a basic feature set is displayed in Figure 2.

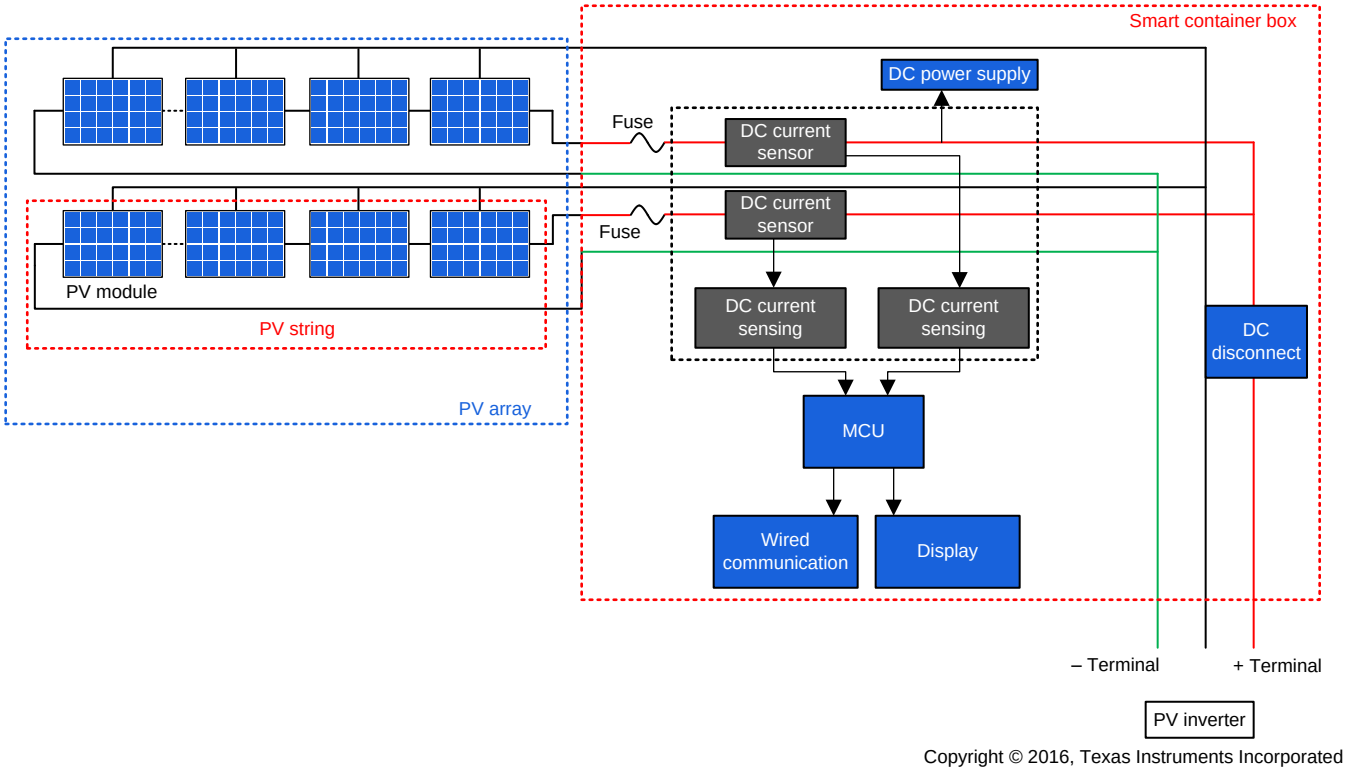

Figure 2. Smart Combiner Box in PV System (1)

(1) http://www.homepower.com/articles/solar-electricity/equipment-products/pv-combiner-box-buyers-guide

The TIDA-00639 is the power sensing subsystem shown within the black dotted box in Figure 2. The board is also designed to enable connection to an MCU and RS-485 communication board, the most common form of communication in smart combiner boxes.

1.1.1 Power Sensing Subsystem

The input current of a smart combiner box can be measured by isolated and non-isolated current sensing methods depending on the accuracy, size, and cost restrictions. Isolated solutions are widely used in smart combiner boxes. Isolated sensors cost more than non-isolated sensors and also require an analog front end for high-precision measurements. With high-voltage considerations taken into account for the schematic design and PCB layout, non-isolated current sensing is a viable alternative with the potential to lower the system cost.

The currents of PV strings can be measured with non-isolated high-side or low-side current sensing techniques, depending on the solar power system's accuracy requirements and grounding configuration. In the United States, the National Electric Code requires PV modules or strings over 50-V DC to be a grounded system to decrease safety risks. A grounded system is defined as either the positive or negative terminal being tied directly to earth ground. [2] Low-side and high-side sensing are viable options for a grounded system. The majority of regional standards regarding solar power systems worldwide do not require PV installations to be grounded systems. Grounded and ungrounded systems are pictured in Figure 3.

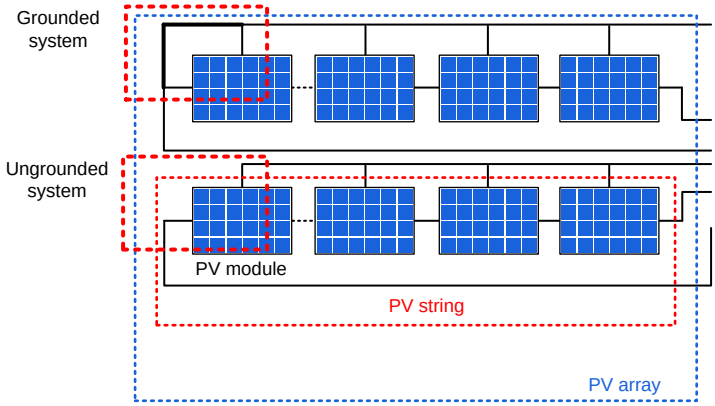

Figure 3. Smart Combiner Box With Ungrounded and Grounded Systems

Low-side current sensing is less expensive than high-side sensing. However, this method cannot detect load shorts in ungrounded or grounded systems and cannot account for grounding inconsistencies. High-side current sensing directly measures the current through the load (before DC combination) and can accurately measure the current in relation to a common ground, the PV string ground. When the smart combiner box is connected to a grounded system and high-accuracy current sensing is not a requirement, low-side current sensing could be the preferred option. When accuracy, load shorts, or grounding inconsistencies are a concern, high-side sensing is the preferred method. Consequently, the majority of smart combiner boxes employ high-side current sensing.

Smart combiner boxes also measure PV string voltage. Because the PV strings are connected in parallel, the string voltages will all be equal. Consequently, one voltage measurement is necessary for power monitoring. In a grounded or ungrounded system, TI's power monitor can be used for DC bus voltage and current measurements. The bus voltage and current will be measured in relation to PV string ground.

The TIDA-00639 evaluates non-isolated high-side current and voltage sensing for ungrounded and grounded systems. Figure 4 and Figure 5 depict how to connect the TIDA-00639 within a smart combiner box in an ungrounded or grounded system. The voltage and current of the PV string are sensed in relation to the negative terminal of the PV string. The TIDA-00639 measures a maximum of 15 A and 600-V DC at ±1% full scale.

[2] http://solarabcs.org/about/publications/reports/systemgrounding/pdfs/SystemGrounding_studyreport.pdf

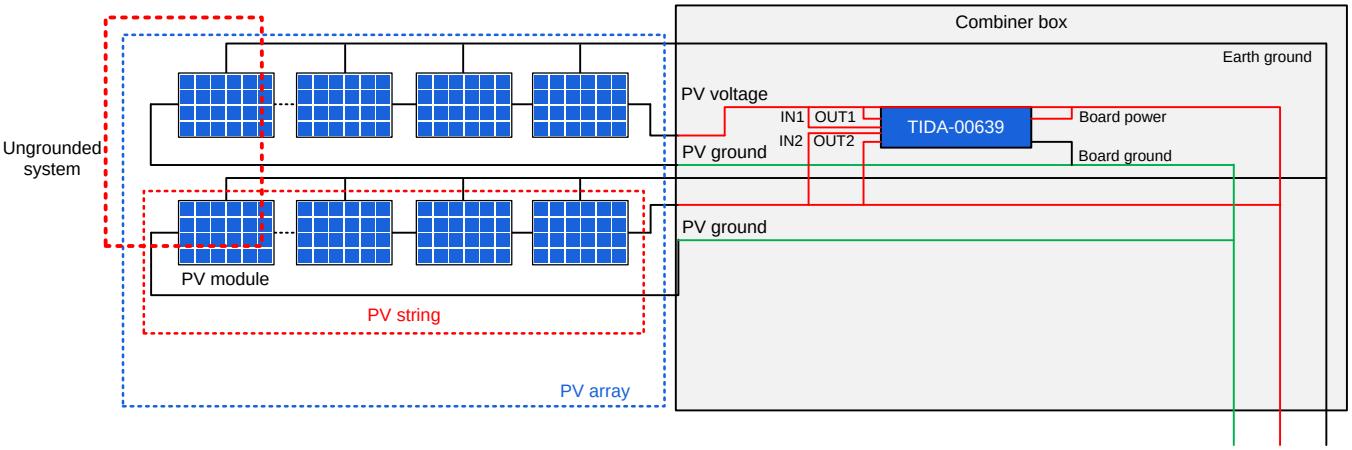

Figure 4. TIDA-00639 in Ungrounded PV System

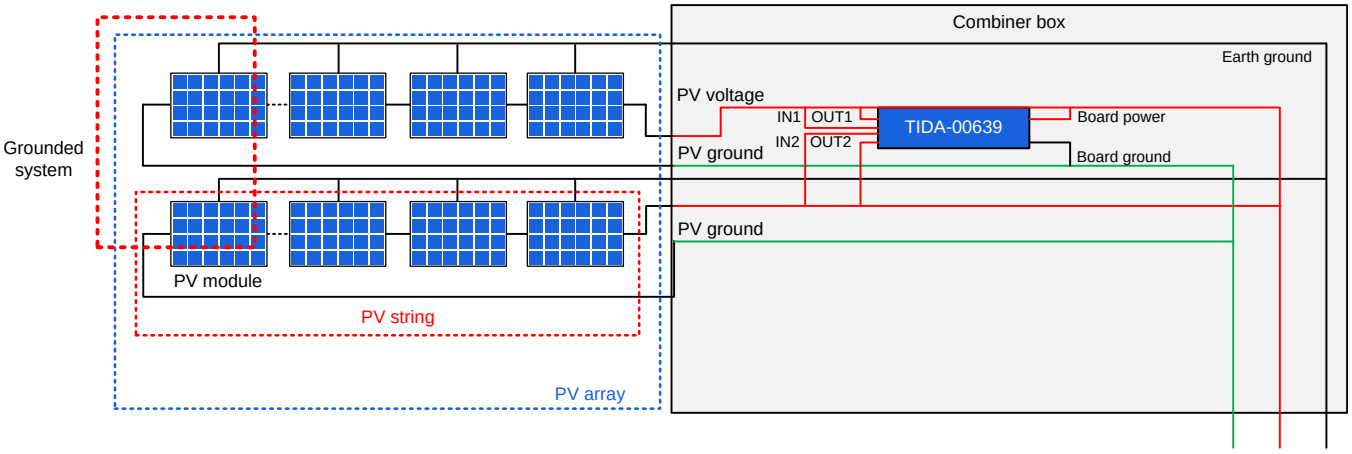

Figure 5. TIDA-00639 in Grounded PV System

1.2 Key System Specifications

Table 1. System Specifications

PARAMETER	SPECIFICATION
Uncalibrated I sense accuracy	±1.25% full scale
Calibrated I sense accuracy	±.75% full scale
Uncalibrated V sense accuracy	±1.0% full scale
DC bus current	0.5 to 15 A
DC bus minimum voltage	95 V
DC bus maximum voltage	600 V
Number of PV string inputs	4 per board
Operating temperature range	-40ºC to 85ºC

1.3 Block Diagram

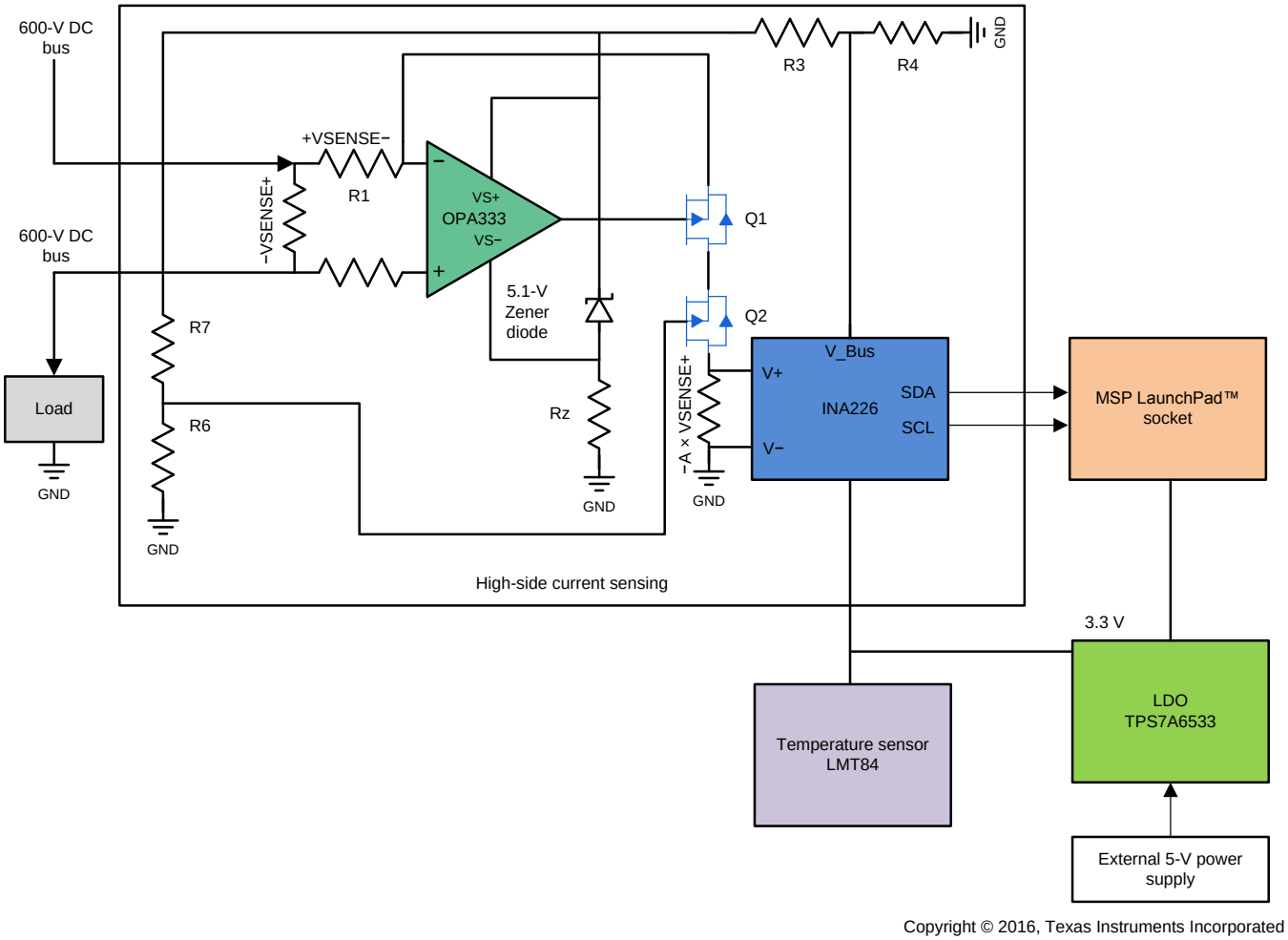

Figure 6. TIDA-00639 Block Diagram

1.4 Highlighted Products

The TIDA-00639 reference design features the following devices:

- OPA333: Precision amplifier with zero drift and low offset voltage
- INA226: Current shunt and power monitor with I^{2}C or SMBUS-compatible interface
- LMT84: Analog output temperature sensor
- TPS7A6533-Q1: 40-V LDO with ultra-low quiescent current

1.4.1 OPA333

- Low offset voltage: 10 μV (maximum)
- Zero drift: 0.05 μV/ºC (maximum)
- 0.01- to 10-Hz noise: 1.1 μV_{PP}
- Quiescent current: 17 μA
- Single-supply operation
- Supply voltage: 1.8 to 5.5 V
- Rail-to-rail input/output
- microSize packages: SC70 and SOT23

1.4.2 INA226

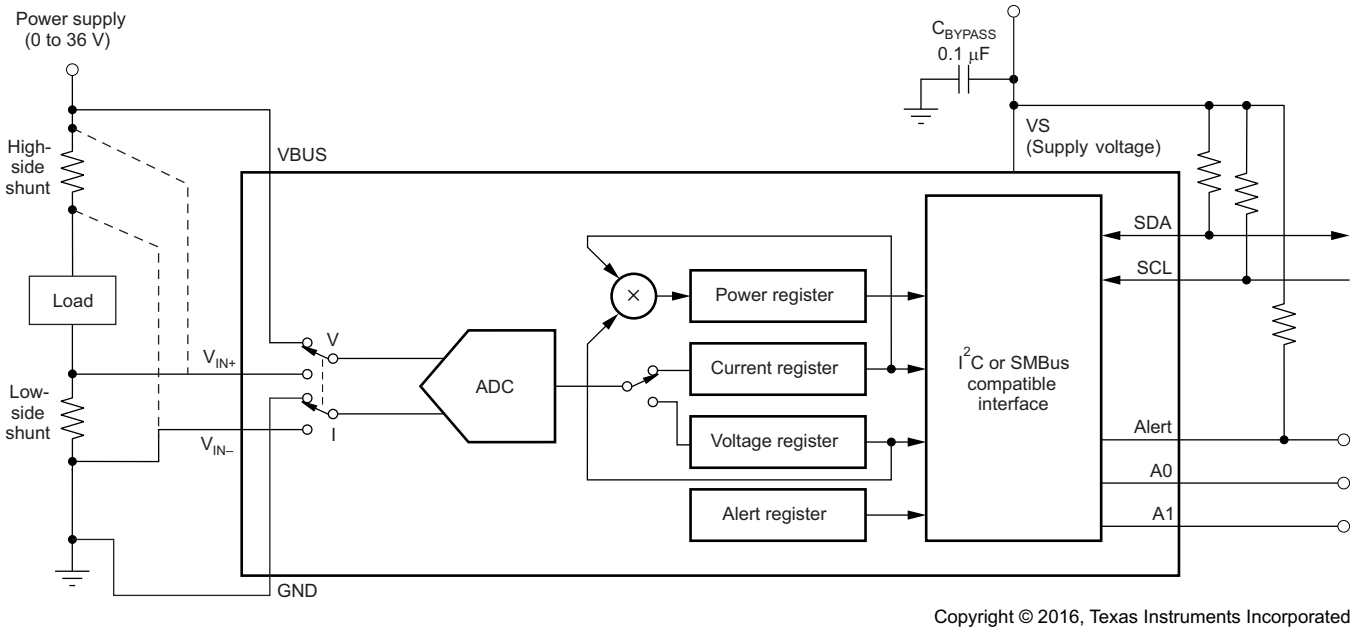

Figure 7. INA226 Simplified Schematic

- Senses bus voltages from 0 to 36 V
- High-side or low-side sensing
- Reports current, voltage, and power
- Configurable averaging options
- 16 programmable addresses
- Operates from 2.7- to 5.5-V power supply
- 10-pin DGS (VSSOP) package
- High accuracy:
  - 0.1 % gain error (maximum)
  - 10-µV offset (maximum)

1.4.3 LMT84

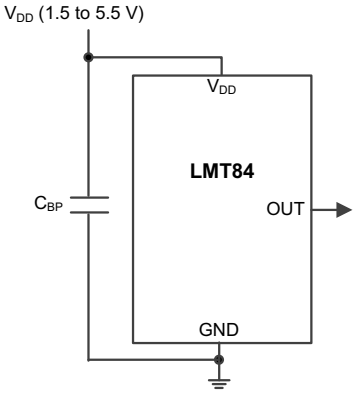

Figure 8. LMT84 Simplified Schematic

- AEC-Q100 Grade 0 qualified and manufactured on an automotive grade flow
- Low 1.5-V operation
- Very accurate: ±0.4ºC typical
- Wide temperature range of –50ºC to 150ºC
- Low 5.4-μA quiescent current
- Average sensor gain of –5.5 mV/ºC
- Output is short-circuit protected
- Push-pull output with ±50-μA drive capability
- Footprint compatible with industry-standard LM20/LM19 and LM35 temperature sensors
- Cost-effective alternative to thermistors
- Packages:
  - Small SC70 (SOT 5-lead) surface mount
  - Leaded TO-92

1.4.4 TPS7A6533-Q1

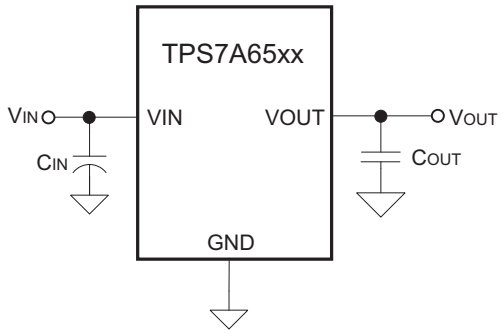

Figure 9. TPS7A6533-Q1 Simplified Schematic

- Low dropout voltage
  - 300 mV at I_{OUT} = 150 mA
  - 4- to 40-V wide input voltage range with up to 45-V wide input voltage range with up to 45-V transients
  - 300-mA maximum output current
  - 25-μA (typical) ultra-low quiescent current at light loads
  - 3.3- and 5-V fixed output stability capacitor
  - Low input-voltage tracking
  - Thermally enhanced power package
    - 3-pin TO-252 (KVU/DPAK)
    - Integrated fault protection
      - Short-circuit and overcurrent protection
      - Thermal shutdown

2 System Design Theory

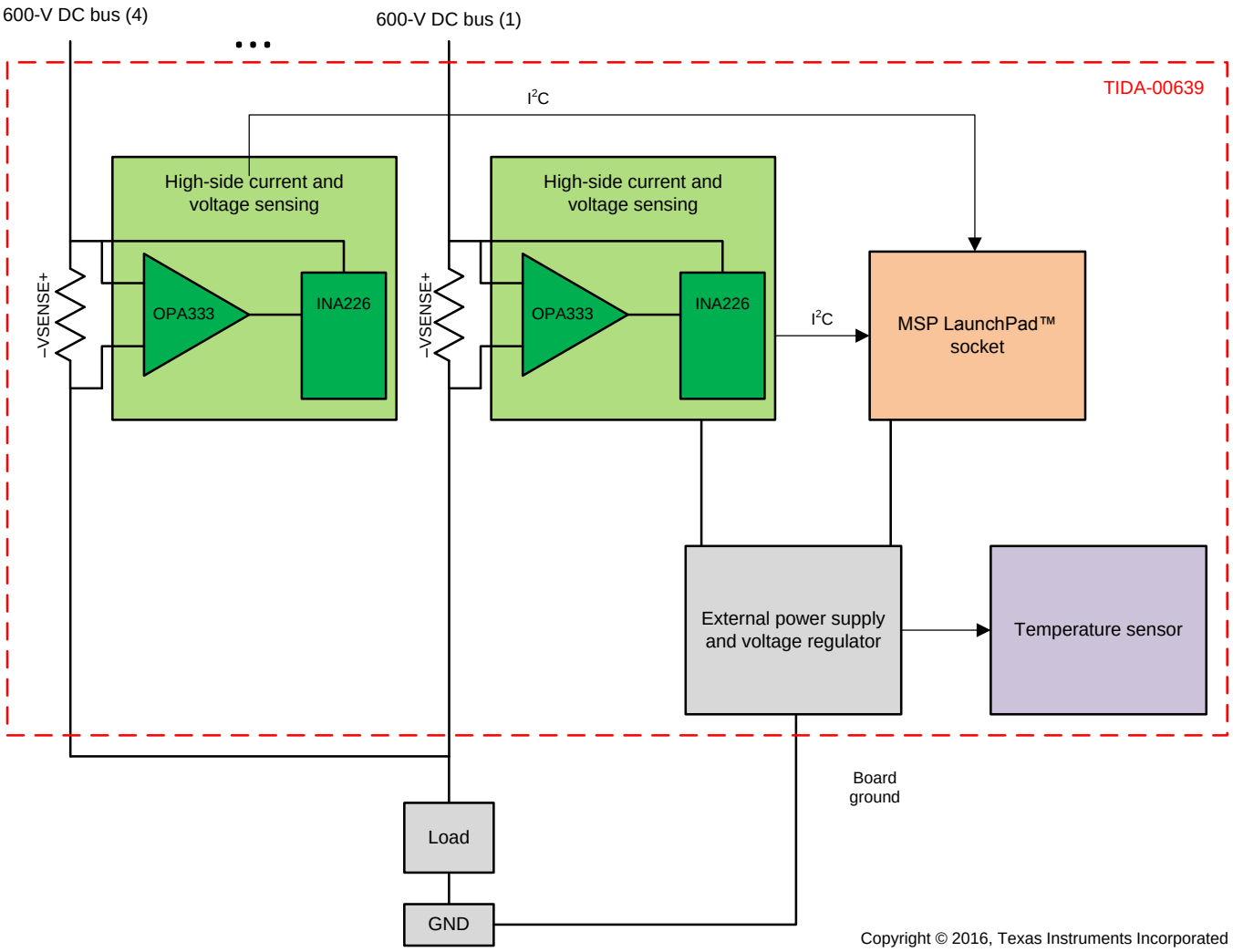

Figure 10. High-Level System Block Diagram

The TIDA-00639 is a shunt-based current and voltage sensing subsystem for a smart combiner box, as pictured in Figure 10. The shunt resistor is on the high-side of the load, directly measuring the current flowing into the load from each input. The shunt resistor was chosen to minimize heat dissipation and power losses while maximizing the voltage measured by the current sensing circuit. In order to lower the power losses to a negligible level, a shunt resistance of 1 mΩ was chosen. At maximum current, the power dissipation for one channel can be calculated as shown in the following equations.

$$\text{Maximum power dissipation} = V_{SENSE} \times I_{SHUNT} = 15\,\text{mV} \times 15\,\text{A} = 0.225 \quad (1)$$

$$\%\ \text{power dissipation from shunt} = \frac{\text{Maximum power dissipation}}{\text{Maximum total power}} \times 100 = \frac{0.225\,\text{W}}{600\,\text{V} \times 15\,\text{A}} \times 100 \quad (2)$$

when

- $V_{SENSE} = R_{SHUNT} \times I_{SHUNT} = 1\,\text{m}\Omega \times 15\,\text{A} = 15\,\text{mV}$

The 1-mΩ shunt resistor is rated at 1% tolerance and 170 ppm. This shunt resistor was chosen with cost in mind. The ppm rating was lowered to a practical level for a smart combiner box, which operates at a maximum temperature of 60ºC to 85ºC. To use a cost competitive shunt resistor, the tolerance was minimized at 1%. The shunt resistor's tolerance can be improved at the expense of component price or ppm rating. The shunt resistor's 1% tolerance equates to variances in channel-to-channel sensing accuracy.

This 1-mΩ shunt resistor is paired with a signal conditioning circuit to maximize the accuracy of the current sensing circuit. The shunt resistor and sensing circuit are designed so that V_{SENSE} across the shunt resistor is mirrored across the input resistor of the op amp. The op amp and high-voltage P-FETs are designed in a current follower configuration to drop the DC bus voltage and mirror V_{SENSE} to the current shunt monitor, the INA226. Currently, P-FET technology is limited to 600 V, and P-FETs rather than N-FETs are necessary for the current follower topology. Consequently, two 400-V P-FETs are connected in series to drop 600 V. Low leakage FETs are necessary for this high-precision application. See Section 2.1 for more details.

The INA226 can also monitor each PV string voltage. See Section 2.2 for more details.

Smart combiner boxes are typically powered by an internal power supply from a PV string. The DC/DC power supply block is not within the scope of the TIDA-00639, so an external power supply is used. For more information about possible DC/DC converter topologies for the power supply, TI offers Power Reference Designs to evaluate power subsystems. See Section 2.3 for more details on the power supply for the TIDA-00639.

Smart combiner boxes have a temperature sensor to monitor the temperature within the box. The smart combiner box is typically outside, and it can become overheated. Monitoring the temperature is necessary to verify the internal temperature is less than the box's operating temperature. The LMT84 enables highly accurate temperature sensing, and is described in Section 2.4.

A LaunchPad™ socket enables the connection of the TIDA-00639 to a TI MCU LaunchPad board. This design is further discussed in Section 2.5.

2.1 High-Side Current Sensing

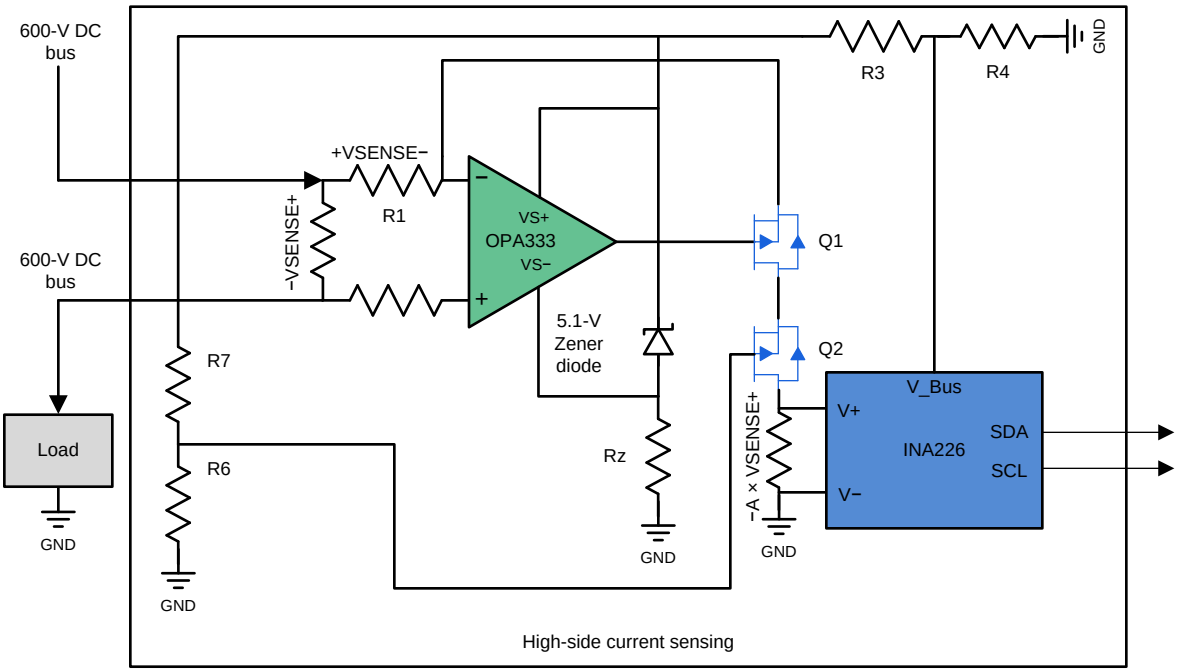

Figure 11. High-Side Current Sensing Block Diagram

The voltage drop across the shunt resistor is mirrored across R1. In Figure 11, this voltage is V_{SENSE}. The op amp and P-FET, Q1, are designed in a current follower configuration. The current through R1 flows through the op amp's feedback loop and the biased P-FETs. To bias the P-FETs:

$$v_{sg} \geq v_{th}$$

$$v_{sd} \geq v_{sg} + v_{th} \quad (3)$$

The P-FET (IRFU9310PBF) was chosen for its high-voltage capability and its low v_{sg} specification, which supports using a precision, low-voltage op amp for the drive. The IRFU9310PBF was also chosen due to the low leakage current specifications, I_{GSS} and I_{DSS} . The current flowing through R1, Q1, Q2, and R2 varies between 0.5 and 1.5 mA. To accurately measure the bus current, the total leakage current must be less than 1% full scale of 1.5 mA.

The OPA333 was chosen for its low offset and zero drift. The OPA333's positive and negative power supply terminals can have a maximum delta of 5.5 V. To pair the OPA333 with this P-FET configuration, the P-FET must have a $|v_{th}| \leq 5$ V. The IRFU9310PBF has a $v_{th\_MAX} = -4$ V.

A 5.1-V Zener diode is used to float the OPA333 to the high-voltage rail to bias the P-FET. The Zener resistor, R_Z, is sized correctly for proper biasing of the Zener diode and the op amp. The MMSZ4689TI Zener diode was chosen for its low nominal current of 50 µA. The Zener resistor needs to accommodate the op amp and Zener diode's currents for proper biasing.

$$R_Z \leq \frac{\text{Bus supply} - V_Z}{I_{ZENER} + I_{OPA333}} = \frac{V_{R\_Z}}{I_{ZENER} + I_{OPA333}} = \frac{600\,V - 5.1\,V}{50\,\mu A + 25\,\mu A} = 7.932\ M\Omega \quad (4)$$

For this design, R_Z is 4.08 MΩ. With a significantly lower R_Z, the design can also work at lower DC bus voltages. The resistance R_Z is split into six series resistors of 680 kΩ to divide the 600-V drop and ease the power dissipation requirement for each resistor.

$$\text{Power rating} \geq \frac{V^2}{R} = \frac{\left(\frac{(600 - 5.1)}{6}\right)^2}{4.08\ M\Omega} = 2.409\ m \quad (5)$$

Choosing a lower power Zener diode and op amp will lower wattage requirements for resistors and, consequently, reduce board space and cost.

The second P-FET, Q2, is biased by a voltage divider where R7 = R6. When both P-FETs are biased, their equivalent circuits are two resistors, R_{sd}, in series. Consequently, the current flowing through R1 is equal to the current flowing through Q1, Q2, and R2. The voltage across R2 is determined by a gain factor A, where:

$$A = \frac{R2}{R1} \quad (6)$$

The INA226 measures the differential voltage across R2. The INA226's full scale voltage is 80 mV. When the maximum current is flowing through the shunt resistor, the voltage across R2 must be approximately 80 mV to maximize the INA226's accuracy.

$$\frac{V_{R2}}{V_{SENSE}} = \frac{R2}{R2} = \frac{80\,mV}{15\,mV} \approx 5 \quad (7)$$

With a gain factor of 5, R2 = 50 Ω and R1 = 10 Ω.

2.1.1 Power Losses

For non-isolated high-side current sensing applications, heat and power dissipation are two of the primary design considerations and challenges. The two P-FETs have the largest power dissipation. Heat or power dissipation methods need to be employed if operating at high power for a long duration of time. To calculate power and heat dissipation across one transistor at a bus voltage of 600 V and a bus current of 15 A:

$$\text{Power dissipation} = \frac{VBUS}{2} \times I_{PFET} = 300\,V \times 1.5\,mA = 0.45 \quad (8)$$

$$\%\ \text{power dissipation from PFET} = \frac{\text{Maximum power dissipation}}{\text{Maximum total power}} \times 100 = \frac{0.45\,W}{600\,V \times 15\,A} \times 100 = 0.005\% \quad (9)$$

where

- $I_{PFET} = \frac{V_{SENSE}}{R1} = \frac{15\,mV}{10\,\Omega} = 1.5\,mA$

2.1.2 Error Sources

High accuracy was one of the primary design requirements. The op amp has zero drift and low offset. The INA226 has low offset. Consequently, the primary source of error is the P-FET leakage, which increases at greater common-mode voltages. The current, I_{SD}, varies between 0.5 and 1.5 mA. To minimize the effects of the P-FET's inherent error, the signal current (I_{SD}) can be increased at the cost of increased power losses, or the P-FET leakage current can be calibrated out at the cost of additional time. The TIDA-00639 is designed to minimize power losses and maximize accuracy. Consequently, the signal current is minimized, and the P-FET leakage current can be calibrated out depending on accuracy requirements.

The second source of error is the shunt resistor's tolerance rating of 1%. This source of error causes channel-to-channel variances in current sensing measurement and is further explored in Section 4.2. To minimize this error source, a shunt resistor with a higher tolerance can be chosen.

2.2 Non-Isolated Voltage Measurement

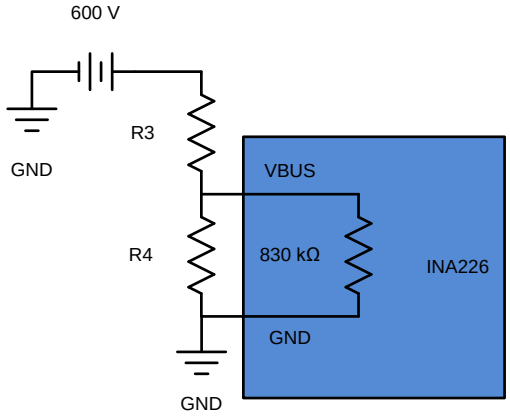

Figure 12. Non-Isolated Voltage Sensing Block Diagram

For grounded systems, accurate voltage monitoring can be integrated into the INA226. The INA226 can measure a maximum voltage of 36 V. The INA226's voltage monitoring is also limited by the input impedance of 830 kΩ, as seen in Figure 12. Therefore, R4 must be significantly smaller than the input impedance, so R3 and R4 divide the voltage down accurately.

In summary, the voltage divider (R3 and R4) must step down the bus voltage to V_{R4} < 36 V, and R4 << 830 kΩ (R4 = 12 kΩ and R3 = 500 kΩ).

$$V_{R4} = V_{BUS} \times \frac{R4}{R4 + R3} \tag{10}$$

When the bus voltage is 600 V, $V_{R4} = 600 \times \frac{12\,k\Omega}{12\,k\Omega + 500\,k\Omega} = 14.0625\ V$

2.3 Board Power Supply

The board is powered by a 5-V external supply through the terminal block input, J10. This power supply's ground terminal is connected to the PV string ground, and the terminal block input, J10, which stabilizes the PCB's ground plane. The 5-V power supply is stepped down to 3.3 V by the TPS7A6533, an LDO. The 3.3-V voltage rail powers the INA226, LMT84, and the LaunchPad socket.

2.4 Temperature Sensing

The LMT84 is a highly accurate temperature sensor, capable of measuring within ±0.4ºC. The temperature sensor also offers a wide temperature range of –50ºC to 150ºC. Consequently, the smart combiner box will be able to detect if the temperature has dropped below or elevated above the operating temperature range. The accuracy of the LMT84's analog output can be evaluated on header J9.

2.5 MCU LaunchPad Socket

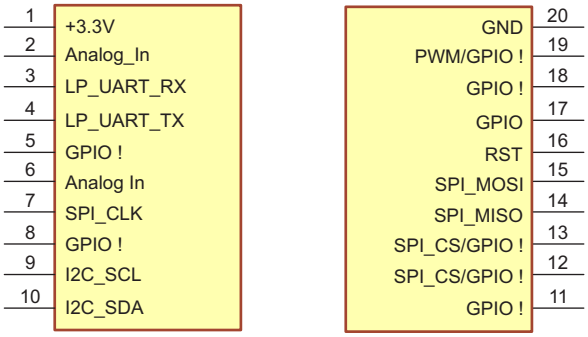

Figure 13. LaunchPad Socket

The standard LaunchPad socket is on board to enable connection to an MCU. The LaunchPad enables I^2C and UART communication.

2.6 Non-Isolated High-Side Sensing for 1000-V DC Bus

The high-side current sensing topology described in Section 2.1 can be redesigned to accommodate a 1000-V DC bus. The primary change is replacing Q1 and Q2 with two 600 V P-FETs. The resistor chains R6, R7, and RZ must be resized to dissipate the higher power and step down the higher voltage.

For the non-isolated voltage measurements, the resistor dividers must ensure the INA226's voltage threshold is not exceeded. The INA226's voltage bus threshold is 36 V. For this TI Design, the resistor dividers for the voltage measurements must be redesigned to drop 1000 V, and use caution in regards to the voltage and power ratings of the resistors.

With increased voltage, the components will have increased spacing on the PCB. The layout changes are addressed in Section 5.3.

The primary design challenges and concerns for a 1000-V DC design are accuracy and heat dissipation. As the voltage increases, the P-FET current leakage increases. The system designer will have two options to uphold ±1% full scale accuracy with a common-mode voltage of 1000 V. One option is increasing the current through Q1 and Q2 by decreasing R1 and R2. The leakage current must be less than 1% of I_SD with a DC bus rated at 1000 V and 15 A. This is at the cost of increased power losses. The second option is calibrating out the FET current leakage with an MCU. In order to mitigate heat dissipation concerns, heat sinking technology can be used.

3 Getting Started Hardware

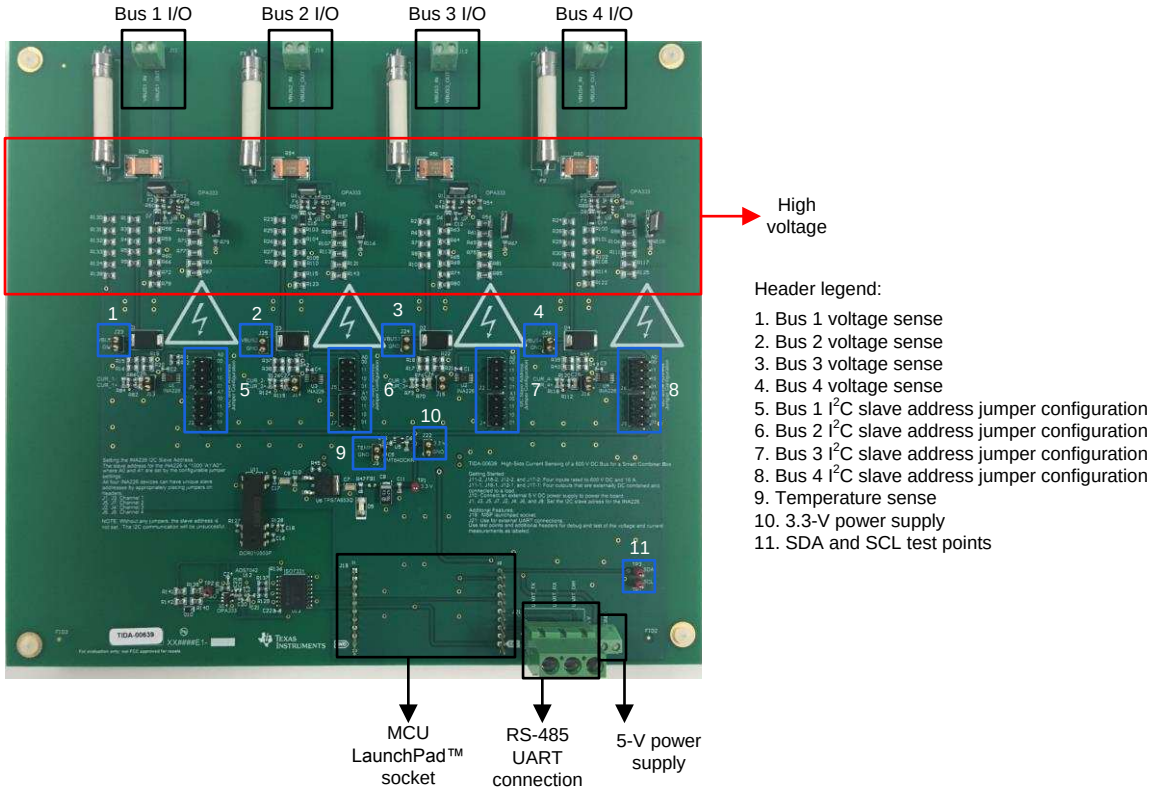

Figure 14. TIDA-00639 PCB

3.1 Board Setup

1. Connect the four high-power inputs to terminal screw blocks J11-1, J18-1, J12-1, and J17-1. These inputs are rated for 600-V DC and 16 A. If the voltage and current ratings are exceeded, the fuse will blow.
2. Connect the four high power outputs to the terminal screw blocks J11-2, J18-2, J12-2, and J17-2. These outputs can be tested individually or be DC combined in parallel and connected to a load rated for the output power.
3. Optional: Connect a LaunchPad board to the LaunchPad socket, J19. Configure the INA226 I^2C slave address. The slave address for the INA226 is "1000'A1"A0"', where A0 and A1 are set by the configurable jumper settings as described in Table 2. All four INA226 devices can have unique slave addresses by appropriately placing jumpers on the headers as described in Table 3.

Table 2. INA226 I^2C Slave Address Jumper Configuration

JUMPER CONFIGURATION	A0	A1
Pins 7-8: Ground	0	0
Pins 5-6: SCL	11	11
Pins 3-4: SDA	10	10
Pins 1-2: VCC	1	1

Table 3. INA226 I^2C Slave Address Headers and Corresponding Input Channels

CHANNEL	A0 HEADER	A1 HEADER
Channel 1	J1	J3
Channel 2	J5	J7
Channel 3	J2	J4
Channel 4	J6	J8

4. Connect an external 5-V DC power supply must be connected to J10 to power on the TIDA-00639 board.
5. Begin evaluating the performance of the TIDA-00639 through the appropriate headers and test points, as described in Section 3.2.

3.2 Evaluation Headers and Test Points

Table 4. Evaluation Headers and Test Points

COMPONENT DESIGNATOR	PIN NUMBER	SIGNAL
DC BUS CURRENT AND VOLTAGE TEST POINTS		
J23	1	Ground
	2	VBUS1
J25	1	Ground
	2	VBUS2
J24	1	Ground
	2	VBUS3
J26	1	Ground
	2	VBUS4
J13	1	Current1–
	2	Current1+
J14	1	Current2–
	2	Current2+
J15	1	Current3–
	2	Current3+
J16	1	Current4–
	2	Current4+
TEMPERATURE SENSOR TEST POINT		
J9	1	Temperature
	2	Ground
BOARD POWER TEST POINT		
J22	1	Ground
	2	3.3 V
ISOLATED VOLTAGE MEASUREMENT TEST POINT		
TP2	1	Isolated voltage (Channel 1)
I^2C TEST POINT		
TP3	1	SDA
TP4	1	SCL

4 Testing and Results

4.1 Test Setup

4.1.1 Current and Voltage Accuracy Test Setup

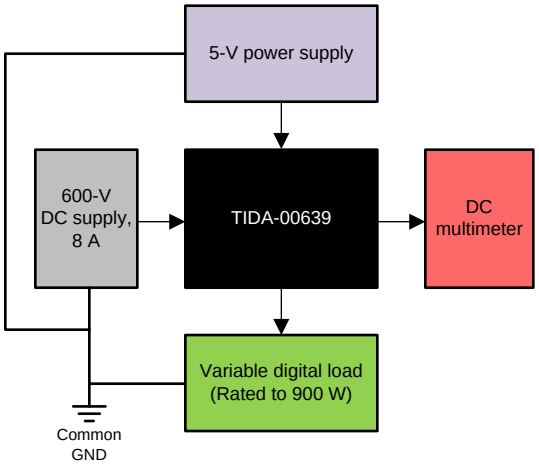

Figure 15. Current and Voltage Sensing Accuracy Test Setup

A Magna power supply rated at 600-V DC and 8 A was used to connect to the terminal block inputs (J11-1, J18-1, J12-1, J17-1). The variable digital load was connected to the output of the TIDA-00639 through the terminal block outputs (J11-2, J18-2, J12-2, J17-2). The power supply and digital load simulate the DC bus connected to the solar inverter.

The 5-V external power supply is connected to the terminal block J10. The ground from the 5-V power supply is connected to the PCB ground plane, and it must also be connected to the ground of the load and 600-V DC power supply to create a common ground.

The DC multimeter is used to monitor the DC voltage corresponding to the voltage sense or current sense measurement. Table 4 calls out the header pins tested to measure the current and voltage sense accuracy. The results are described in Section 4.2.

4.1.2 Full Current Range Sensing Accuracy Test Setup

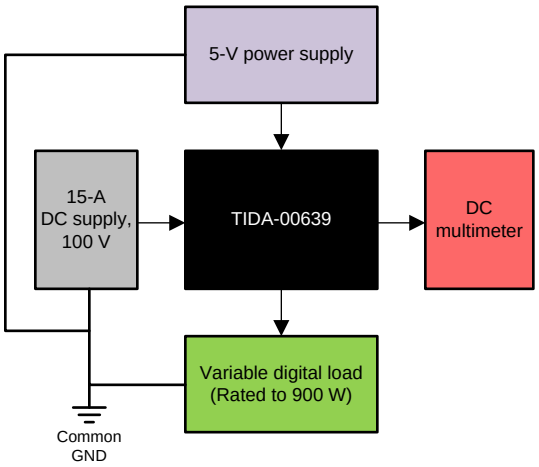

Figure 16. Full Current Range Sensing Accuracy Test Setup

A 100-V DC and 15-A power supply was used to connect to the terminal block inputs (J11-1, J18-1, J12-1, J17-1). The variable digital load was connected to the output of the TIDA-00639 through the terminal block outputs (J11-2, J18-2, J12-2, J17-2). The power supply and digital load simulate the DC bus connected to the solar inverter.

The 5-V external power supply is connected to the terminal block J10. The ground from the 5-V power supply is connected to the PCB ground plane, and it must also be connected to the ground of the load and 100-V DC power supply to create a common ground.

The DC multimeter is used to monitor the DC voltage corresponding to the voltage sense or current sense measurement. Table 4 calls out the header pins tested to measure the current and voltage sense accuracy. The results are described in Section 4.2.

4.2 Test Data

4.2.1 Current Sensing Accuracy

The current sense accuracy is dependent on the tolerances of the shunt resistor and the leakage current of the P-FETs. The drain-to-source and gate-to-source leakage currents increase as the drain-to-source voltage increases. As the current through the shunt increases, the current flowing through the P-FETs increases. As the source-to-drain current increases, the I_{SD} percent loss due to leakage decreases. Consequently, as the DC bus current increases the current sense measurement increases in accuracy.

As designed and without calibration, the full scale error is within ±1.25% full scale. There are three methods to maximize the current sense accuracy to ±1% full scale and beyond:

1. Increasing the shunt resistor tolerance at the expense of increased component cost (Section 2)
2. Increasing the signal current at the expense of increased power losses (Section 4.2.1.2)
3. Calibrating the data at the expense of time (Section 4.2.1.3)

4.2.1.1 Uncalibrated Accuracy

Using the test setup from Figure 15, the current sense accuracy was tested. This testing was limited to a total input power rating of 900 W and was run across three channels from two boards. The accuracy decreases with increasing voltage. As the voltage across the P-FET's source and drain increases, the leakage current increases. As the current increases, accuracy increases. The accuracy can be further improved by calibrating out the P-FET leakage losses. Figure 17 is the test results.

Using the test setup from Figure 15, the current sense accuracy was measured across the full common mode voltage range at four different currents (0.5 A, 1 A, 1.5 A, and 2 A). This test was run on three channels from two boards. Figure 18 is the test results. This test further proves that as the voltage increases, the accuracy decreases, and as the current increases, the accuracy increases.

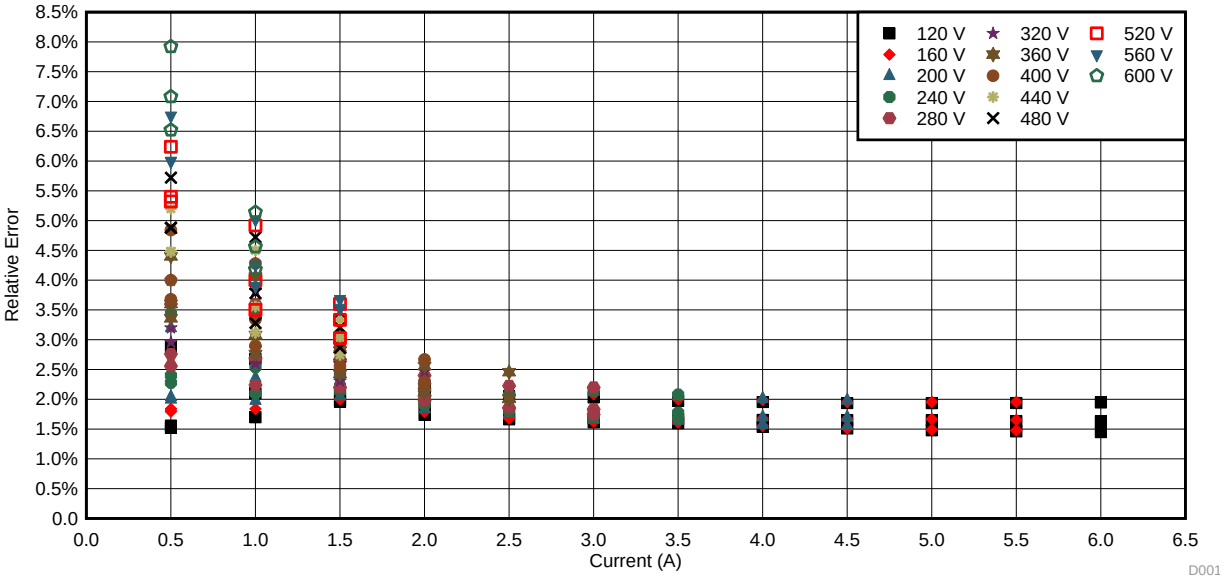

Figure 17. Uncalibrated Relative Error of Current Sense Measurement versus Current

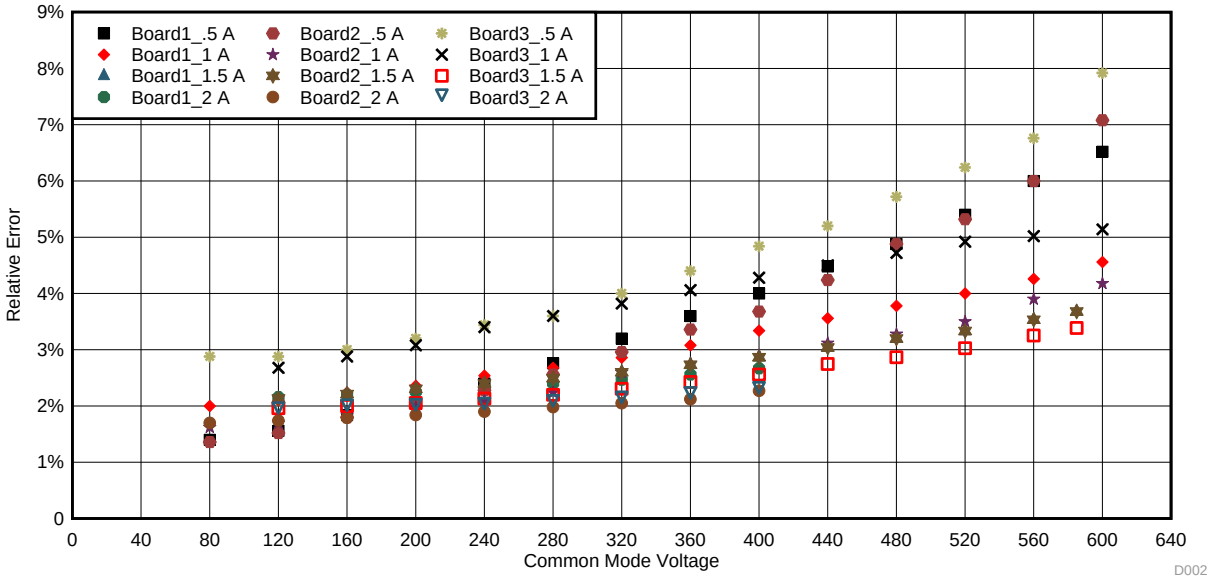

Figure 18. Uncalibrated Relative Error versus Common-Mode Voltage

Using the test setup from Figure 16, the full current range was swept across three channels. This test was run at a fixed DC bus voltage of 95 V. The current accuracy varies significantly channel to channel due to the 1% tolerance of the shunt resistor. All channels operate within ±1.25% full scale accuracy. To ensure the accuracy is below ±1% full scale for any channel, a universal calibration algorithm is implemented to calibrate out the P-FET leakage errors. If this error source is calibrated out but not the shunt resistor's tolerance, the accuracy will be less than 1% full scale. Consequently, one calibration equation will effectively lower the relative error for all channels, but there will still be channel-to-channel variances. Figure 19 shows the test results.

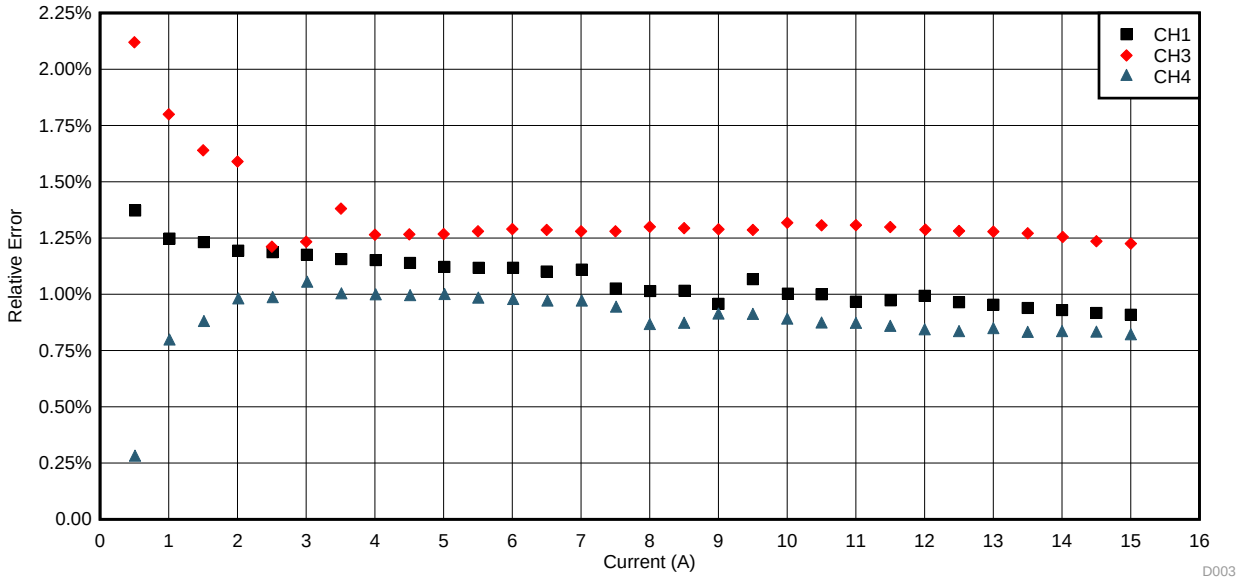

Figure 19. Uncalibrated Relative Error versus Current for 95-V DC Bus

4.2.1.2 Double I_{SD} to Improve Uncalibrated Error

As discussed in Section 2.1.2, the primary error source is the leakage current from the P-FETs. Consequently, if the signal current through the P-FETs is increased, the leakage current's effects will be minimized. To test this theory, the signal current was doubled by changing the value of R1 from 10 Ω to 5 Ω and R2 from 50 Ω to 25 Ω. As expected, the error decreased significantly when the signal current was doubled. The test results for three channels are shown in Figure 20. The relative error is less than 1% starting at a 2.5-A DC bus. To maximize the signal current and minimize the power losses, R1 and R2 can be sized to exactly enable the desired level of accuracy.

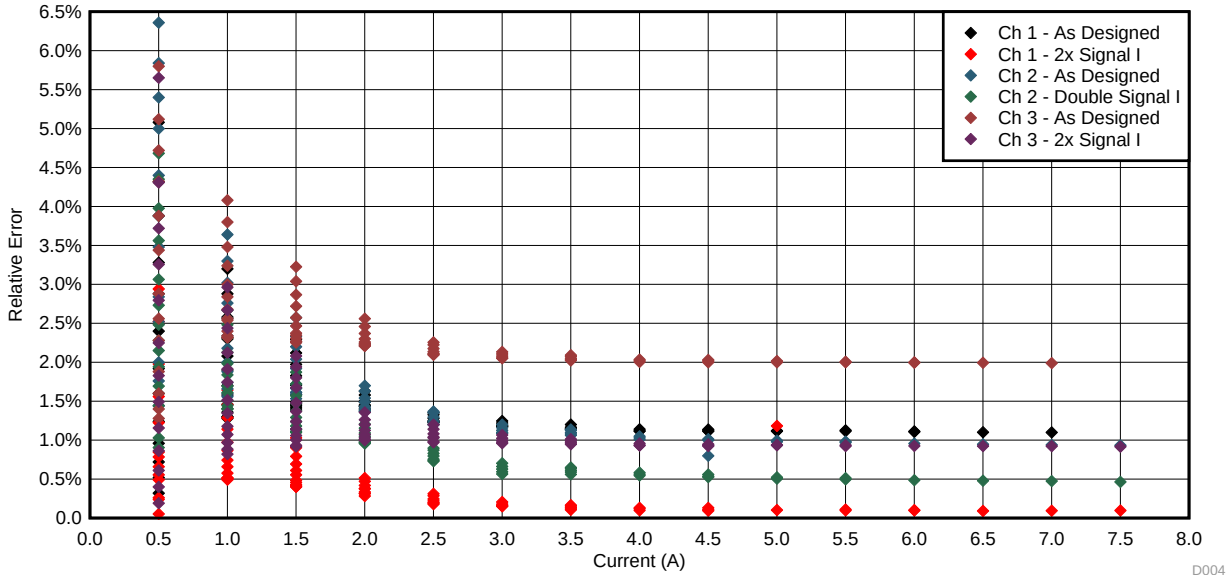

Figure 20. Uncalibrated Relative Error of Current Sense Measurement versus Current

4.2.1.3 Calibrated Error

To calibrate out the P-FET leakage error, a universal calibration equation was developed based on the linear relationship between the expected current and the actual output current. Figure 21 shows the linear relationship between the expected and actual current sense measurement. Figure 22 is the relative error versus current of the data from Figure 17 after calibration. Figure 23 is the relative error versus current of the data from Figure 19 after calibration. The full scale accuracy is under ±0.75%.

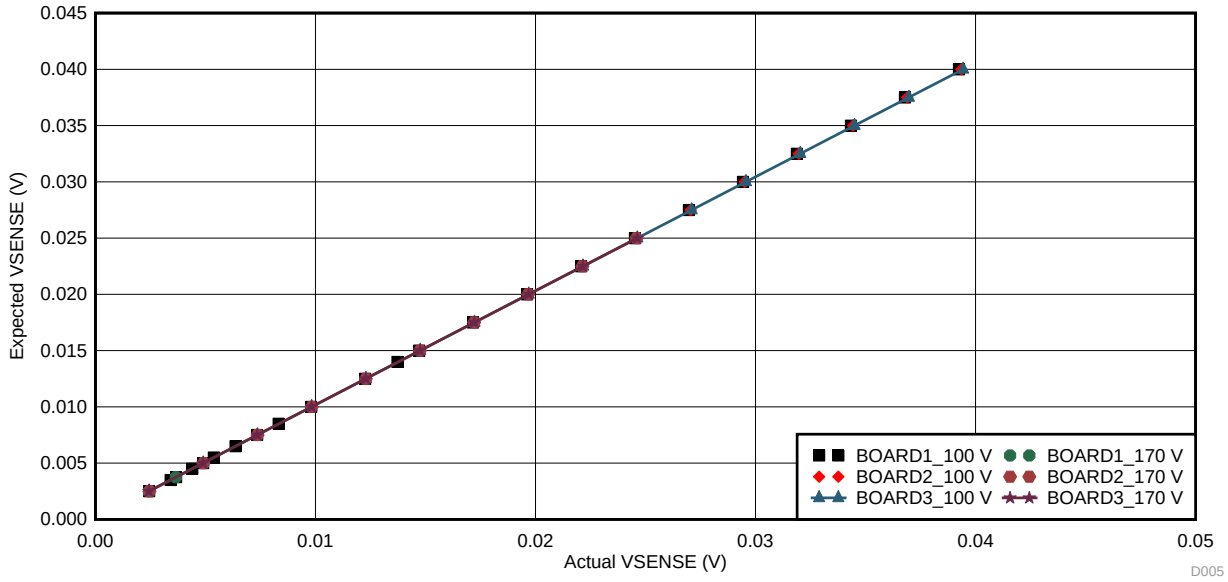

Figure 21. Expected I_{SENSE} versus Actual I_{SENSE}

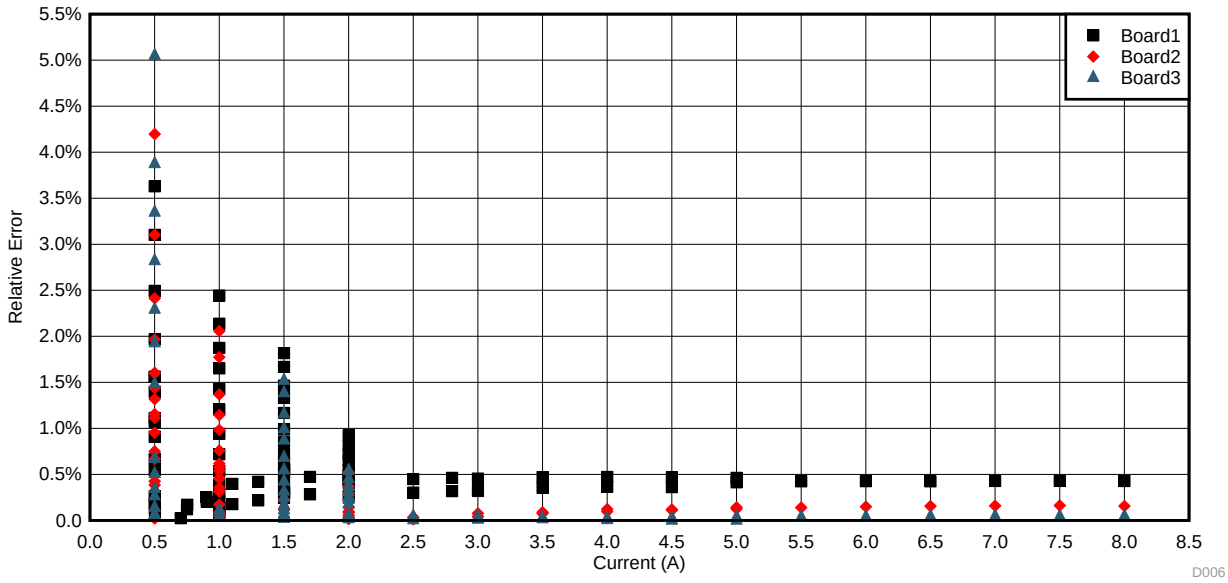

Figure 22. Relative Error versus Current With Calibration Across Full Voltage Range

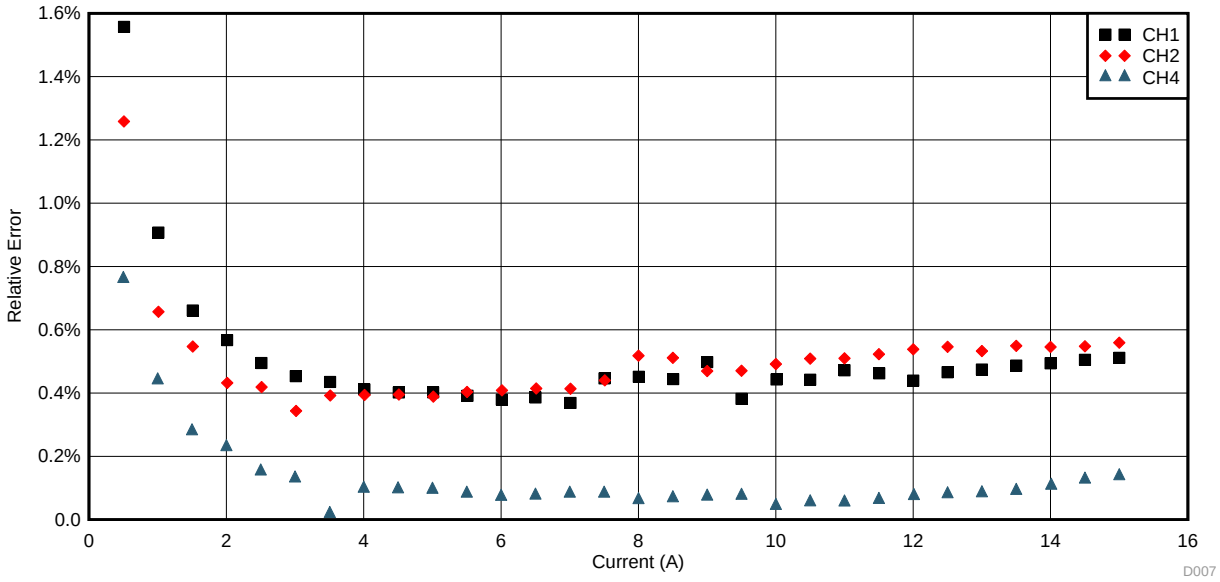

Figure 23. Relative Error versus Current With Calibration Across Full Current Range

4.2.2 Voltage Sensing Accuracy

The INA226 is capable of measuring the DC bus voltage. The voltage measurement is designed to operate at ±1% full scale accuracy. The maximum DC bus value for this design is 600 V. The voltage measurement was tested across two channels. The test results are shown in Figure 24.

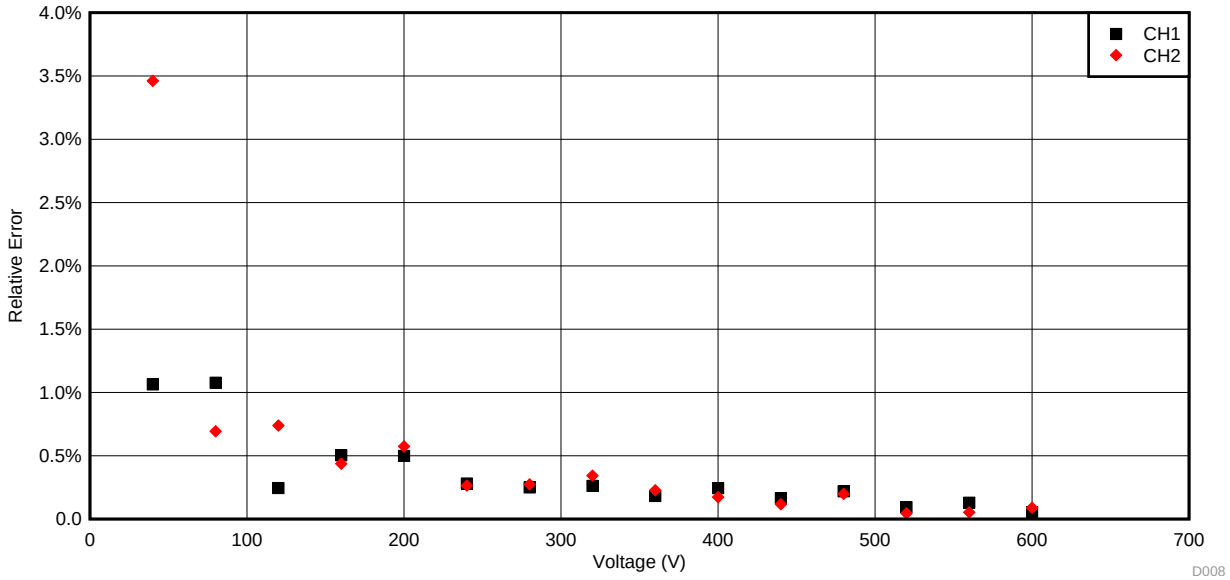

Figure 24. Relative Error of Voltage Sense Measurement versus Voltage

5 Design Files

5.1 Schematics

To download the schematics for each board, see the design files at TIDA-00639.

5.2 Bill of Materials

To download the bill of materials for each board, see the design files at TIDA-00639.

5.3 PCB Layout Recommendations

High-voltage PCB layouts require special consideration. Take care to add space between the traces that are several volts apart. The PCB trace spacing used in this design meet the requirements specified in Table 6-1 of the IPC-2221 standard for external conductors with conformal coating over assembly. The IPC-2221 "Generic Standard on Printed Board Design" specifies spacing requirements for various types of PCB construction, coating, and applications. Consequently, there must be sufficient spacing between the components within the high-voltage portion of the board, which is physically separated from the low-voltage portion of the board (see Figure 14).

The layout of the current-sensing resistor is critical (see Figure 25). Connect the input pins (RSENSE+ and RSENSE–) to the sensing resistor using a Kelvin connection or a four-wire connection. These connection techniques ensure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low resistance of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors.

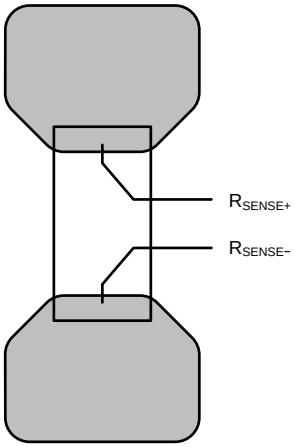

Figure 25. Kelvin Connected Shunt Resistor

The PCB carries high current through the input terminals (J11-1, J18-1, J12-1, J17-1) to the shunt resistor and out through the output terminals (J11-2, J18-2, J12-2, J17-2). The traces carrying the high current were created with polygon pours and the trace widths were maximized.

Placing bypass capacitors close to the OPA333 and INA226 is also critical. This improves stability and noise immunity.

5.3.1 Layout Prints

To download the layout prints for each board, see the design files at TIDA-00639.

5.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00639.

5.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00639.

5.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-00639.

6 References

1. Texas Instruments, *Noise Analysis in Operational Amplifier Circuits*, Application Report (SLVA043)
2. Texas Instruments, WEBENCH® Design Center (http://www.ti.com/webench)

7 About the Author

KATELYN WIGGENHORN is a systems and applications engineer in the Texas Instruments Grid Infrastructure team, focusing on renewable energy. Katelyn received her bachelor of science in electrical engineering from Villanova University.

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Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is **intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments**. If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
   (a) Keep work area clean and orderly.
   (b) Qualified observer(s) must be present anytime circuits are energized.
   (c) Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   (d) All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   (e) Use stable and nonconductive work surface.
   (f) Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   (a) De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   (b) With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   (c) After EVM readiness is complete, energize the EVM as intended.
   WARNING: WHILE THE EVM IS ENERGIZED, NEVER TOUCH THE EVM OR ITS ELECTRICAL CIRCUITS AS THEY COULD BE AT HIGH VOLTAGES CAPABLE OF CAUSING ELECTRICAL SHOCK HAZARD.
3. Personal Safety
   (a) Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

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