*TI Designs*

# *Small Footprint Isolated Analog DC/DC Converter Reference Design*

## Design Overview

Isolated power supplies are important for analog components like analog-to-digital converters (ADCs) and operational amplifiers (op amps) in factory automation and control. They prevent ground loops, reduces noise, and are essential for protection from surge. This TI Design shows an extreme low-profile, small form-factor isolated power solution for analog modules where space is a primary concern.

## Design Resources

| | |
|---|---|
| TIDA-00689 | Design Folder |
| TIDA-00237 | Product Folder |
| LM5160 | Product Folder |
| TPS65130 | Product Folder |

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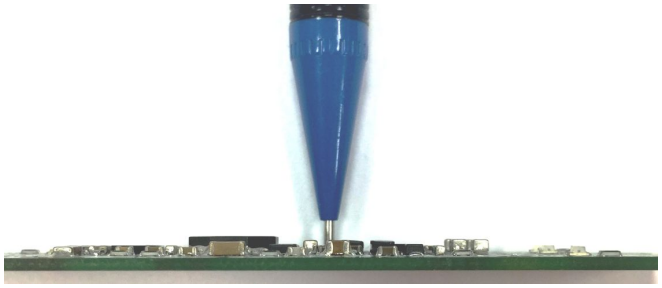
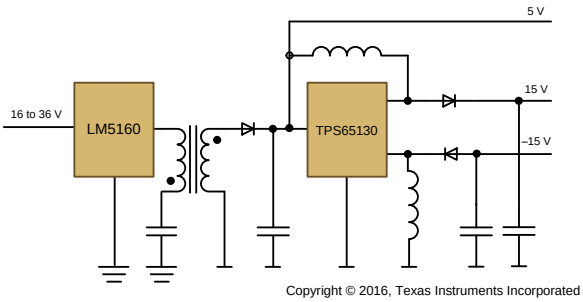
## Design Features

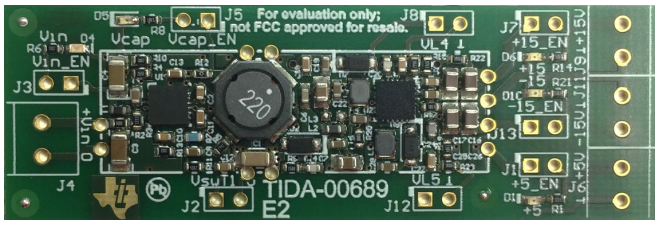
- Very Low Profile of 1.8 mm + PCB Thickness
- Isolated Output With Three Voltages
  - ±15 V for Analog
  - 5 V for ADC
- Very Small Real Estate Requirement: 12.7 × 40.8 $mm^2$

## Featured Applications

- PLC, DCS, and PAC
  - Analog Input Module
  - Analog Output Module
  - Transducer Module





# 1 Key System Specifications

**Table 1. Key System Specifications**

| SYMBOL | PARAMETER | CONDITIONS | SPECIFICATION | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{IN}$ | Input voltage | Normal operation | 16.0 | 24 | 32.0 (1) | V |
| $I_Q$ | Quiescent current | No output load | — | 15 | 20.0 | mA |
| $V_{J6}$ | Output voltage | $V_{IN} > V_{IN(min)}$, 10% < Load < 100% | 4.6 | 5 | 5.2 | V |
| $V_{J9}$ | | | 14.8 | 15 | 15.2 | V |
| $V_{J11}$ | | | –14.8 | –15 | –15.2 | V |
| $I_{J6}$ | Output current | $V_{IN} > V_{IN(min)}$ | 0 | 20 | 200 (2) | mA |
| $I_{J9}$ | | | 0 | 15 | 601.0 | mA |
| $I_{J11}$ | | | 0 | 15 | 601.0 | mA |
| $P_{OUT}$ | Output power | $V_{J6}$ as specified | 0 | — | 500 (3) | mW |
| $V_{ISO(AC)}$ | Isolation voltage | AC, 1 min | 490.0 | — | — | V |
| $V_{ISO(DC)}$ | | DC, 1 min | 700.0 | — | — | V |
| $V_{ISO(PERM)}$ | | DC, infinite min | 70.0 | — | — | V |
| h | Efficiency | $V_{IN}$ = 16 V, $P_{OUT}$ = max | — | 51 | — | % |
| | | $V_{IN}$ = 24 V, $P_{OUT}$ = max | — | 44 | — | % |
| | | $V_{IN}$ = 32 V, $P_{OUT}$ = max | — | 39 | — | % |
| $d_{CREEP\_B}$ | Creeping distance board | | 1.0 | — | — | mm |
| $d_{CREEP\_T}$ | Creeping distance transformer | | 0.2 | — | — | mm |
| H1 | Component height | Above PCB | — | — | 1.8 | mm |
| H2 | | Below PCB | — | — | 0 | mm |
| $A_A$ | Active area size | | — | — | 12.7 × 40.8 | $mm^2$ |

(1) The circuit has been tested up to 32 V. By design, it can operate up to 40 V.
(2) Each rail can have the maximum power $P_{OUT}$; however, the total power of all rails together may not exceed $P_{OUT}$.
(3) Output power can increase to 1 W if $V_{J6(min)}$ = 4.25 V is acceptable at $V_{IN}$ = 16 V.

## 2 System Description

A programmable logic controller (PLC) is a key component in factory automation. The PLC monitors inputs and outputs in real time and controls the process according to the requirements. Because of flexible I/O modules, PLCs can adapt to many different process requirements. The analog I/O modules, local or remote, acquire process data and set outputs to actuate the process. Figure 1 shows an analog input module with an emphasize on the power block.

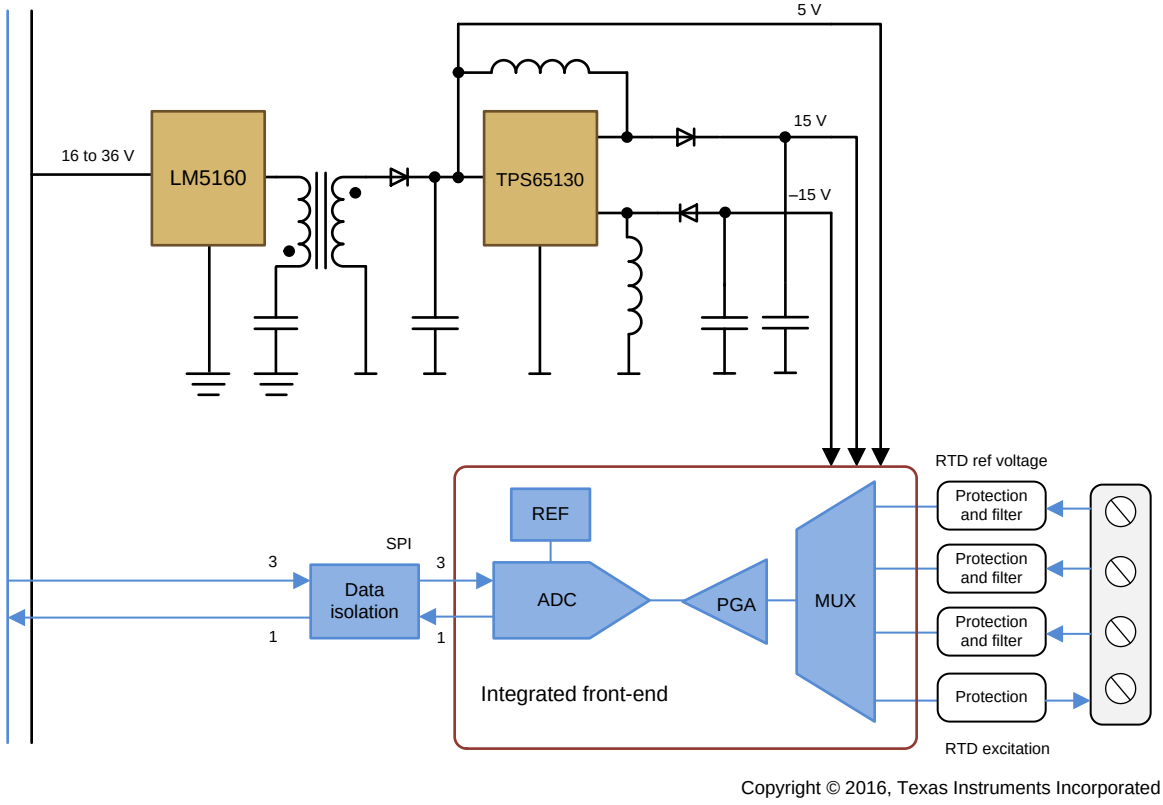





**Figure 1. Generic Illustration of Analog Input Module**

About 10% of all PLC I/O modules are analog input modules. Typical signals are currents from 4- to 20-mA current loops, or voltages from ±10-V voltage sources. The analog input modules use an ADC to convert analog process signals to digital values. These modules need an analog front-end for the different types of input signals. Such a front-end must perform the following tasks:

- Amplify if the signal is smaller than the conversion range of the ADC
- Attenuate if the signal level is larger than the conversion range of the ADC
- Filter if the signal has frequency content not suited for the ADC
- Common-mode shift if the signal has an offset to the ground of the ADC
- Protect against surge, EFT, and ESD

About 5% of all PLC I/O modules are analog output modules. These modules use a digital-to-analog converter (DAC) to convert digital values to an analog signal. These analog signals can be currents or voltages. Typical values for currents can range from –12 mA up to 12 mA or alternatively 4 mA to 24 mA with an overrange capability of 20% included. Voltages can range from –12 V to 12 V also with an overrange capability of 20% included. The overrange capability is used to signal error conditions. The adaptation to the required output signal type is done by buffer amplifiers or voltage-to-current converters. An isolated power supply like the TIDA-00689 is required to separate the ground for the inputs from the ground of the PLC. This ensures the expected performance from the data converter and the amplifier stage.

# 3 Block Diagram

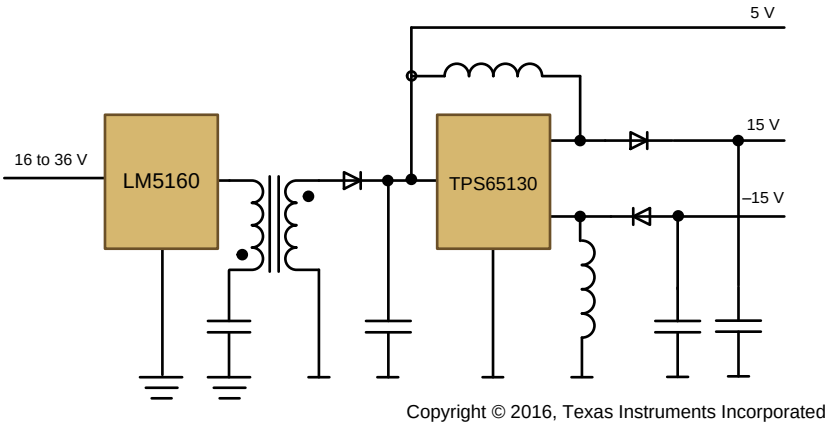





**Figure 2. TIDA-00689 Isolated Power Supply Diagram for Analog Input Module**

## *3.1 Highlighted Products*

The TIDA-00689 provides the isolated analog and digital supply voltages for PLC analog I/O modules. For the analog section of the module, the TIDA-00689 generates 15 V and –15 V. These voltages are accurate and have a ripple of 5 mV. It also generates 5 V for a data isolation device, the data converter and to supply a microcontroller. To keep the transformer small, it creates only one voltage of 5 V, and the 15-V rails are generated by using a DC/DC converter.

### 3.1.1 LM5160

The LM5160 is a 65-V, 1500-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant on-time (COT) control scheme employed in the LM5160 requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high-voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers.

A peak current limit circuit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout (VCC UVLO).

### 3.1.2 TPS65130

The TPS65130 is a dual-output DC-DC converter generating a positive output voltage up to 15 V and a negative output voltage down to –15 V with output currents of up to 200-mA. With a total efficiency up to 85%, the device is ideal for high environment temperature with limited cooling. The TPS6513x comes in a small 4-mm × 4-mm VQFN-24 package. Together with a minimum switching frequency of 1.25 MHz, the device enables designing small power supply applications because it requires only a few small external components.

The converter operates with a fixed frequency PWM control topology and, if power-save mode is enabled, it uses a pulse-skipping mode at light-load currents. Independent enable pins allow power-up and powerdown sequencing for both outputs. The device has an internal current limit overvoltage protection and a thermal shutdown for highest reliability under fault conditions.

## 4 System Design Theory

This TI Design uses the Fly-Buck™ topology for the isolating part of the power supply. It has a low part count and needs no optocoupler feedback circuit like flyback designs. This topology additionally generates a stabilized primary non-isolated power supply, which could be used with data isolators. The Fly-Buck is implemented using an LM5160. This device has a synchronous rectifier and uses forced PWM mode. It fulfils the Fly-Buck requirements with a small circuit footprint and arrives at a low BOM cost. Figure 3 shows the architecture of the LM5160.

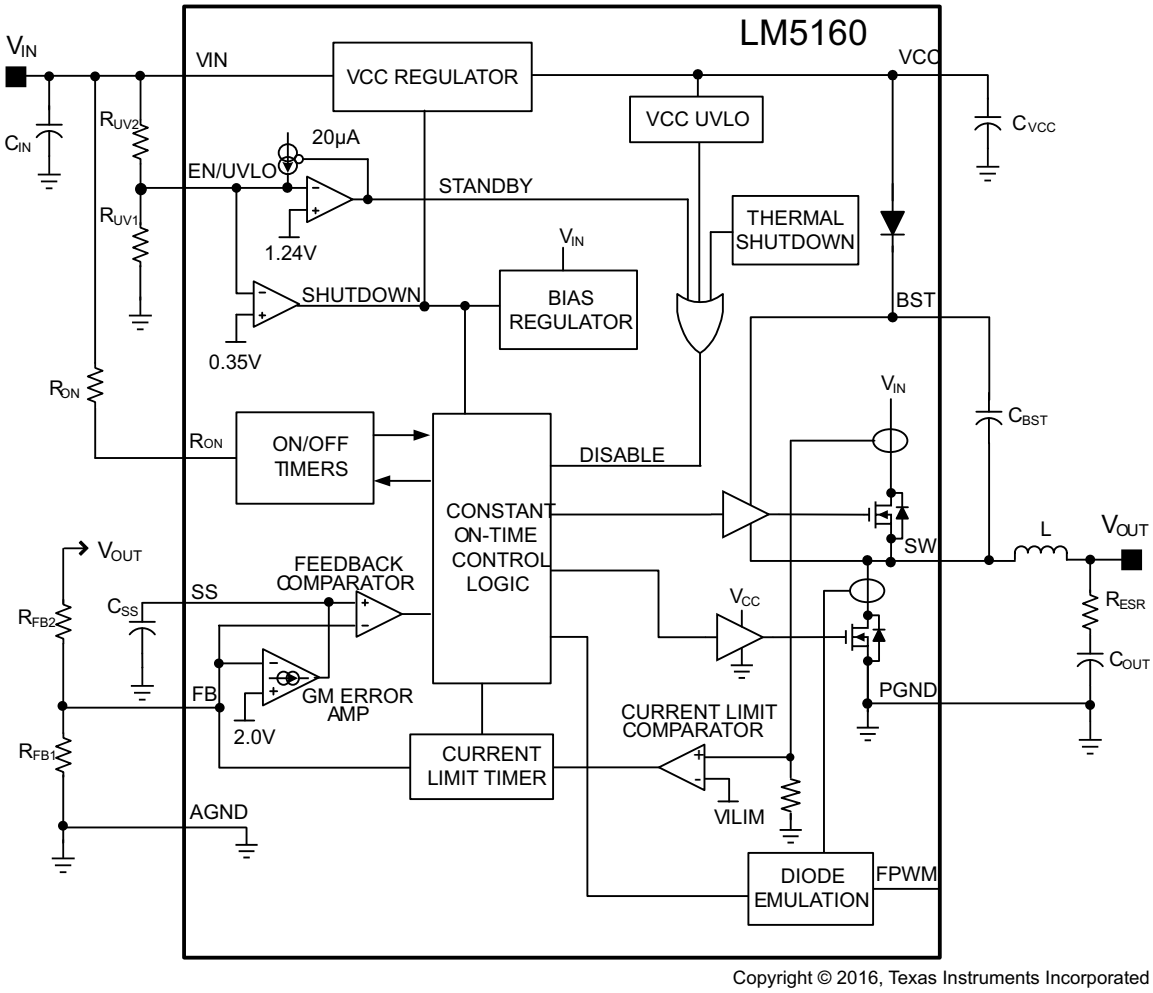





**Figure 3. LM5160 Block Diagram**

Most of the analog PLC I/O modules are space constrained. The TIDA-00689 is a solution for this space problem with small component height of only 1.8 mm and a footprint of 12.7 mm × 40.8 mm. This low profile is achieved with a drum core 1:1 transformer with integrated air gaps.

In this design, the isolating supply creates only one voltage, which is in this case 5 V. The ±15-V rails are generated using the single chip boost and inverting boost converter TPS65130. Figure 4 shows the block diagram of the TPS65130. To operate, it needs only two low-cost inductors of 5 to 10 µH and a small quantity of passive components. Together with the package size of 4 mm × 4 mm, this contributes to the very small footprint of the module.

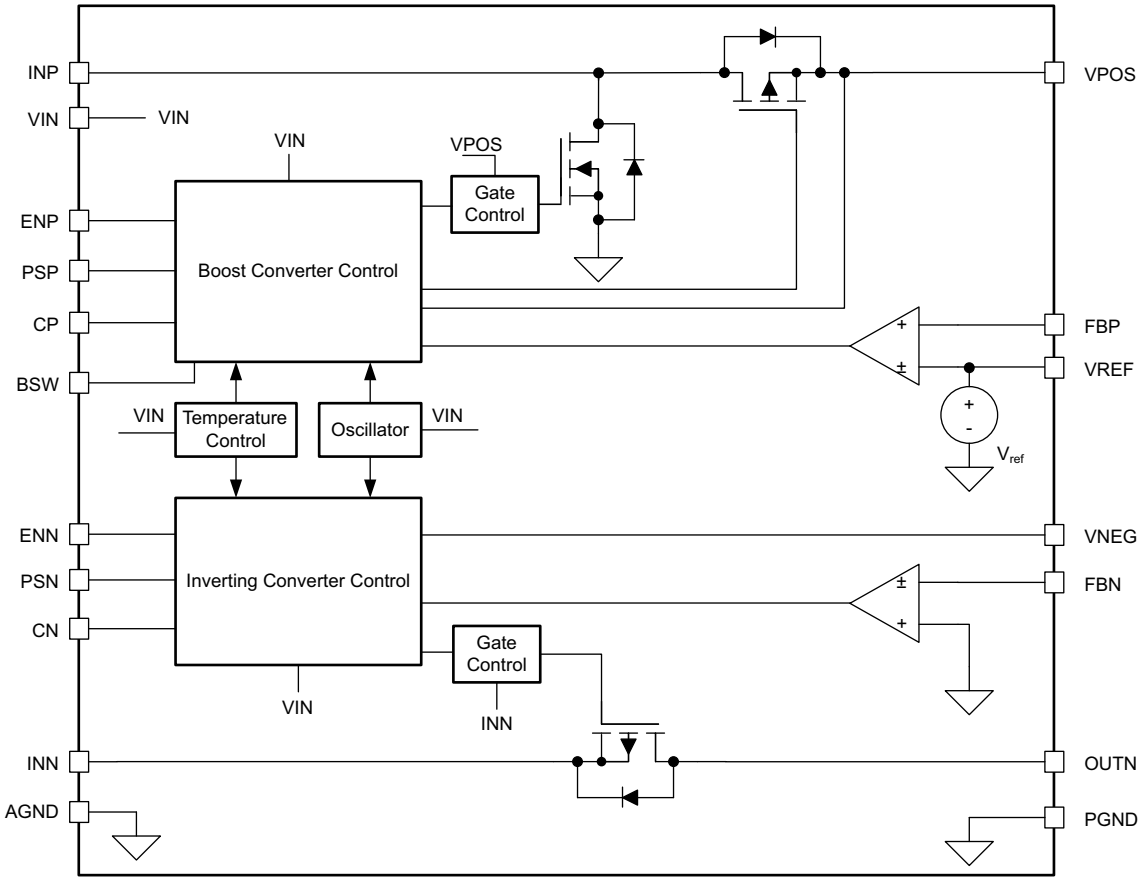





**Figure 4. TPS65130 Block Diagram**

## 4.1 Transformer

The transformer in this design is a drum core based coupled inductor with very low profile. It is available off the shelf with a 1:1 winding ratio. The secondary side needs a minimum of 4.6 V after rectification. The rectifier diode is a Schottky type with a drop voltage of 0.4 V. The design needs a Fly-Buck transformer primary voltage as calculated in Table 2.

**Table 2. $V_{J6}$ Transformer T1 Voltage Calculation**

| PARAMETER | CONDITIONS (SWITCHING FREQUENCY SET TO 500 kHz, $V_{IN}$ = 16 V) | VALUE |
|---|---|---|
| $V_{J6}$ | 100% load | 4.6 V |
| Diode D2 drop-out voltage | 250 mA average forward current during conducting time (160 mA by duty cycle 66%) | 0.4 V |
| Inductor L2 loss | 0.38 Ω, 160-mA average forward current | 0.1 V |
| Transformer T1, secondary winding loss | 0.48 Ω, 250-mA average forward current during conduction time | 0.1 V |
| Required transformer T1, secondary winding voltage | | 5.2 V |
| Transformer T1, primary winding voltage | Winding ratio 1:1 | 5.2 V |
| Transformer T1, primary winding loss | 0.48 Ω, 250-mA average forward current during conduction time | 0.1 V |
| Transformer T1, leakage inductance voltage loss | 0.35 µH, 1 µs, 250-mA average | 0.2V |
| U1 synchronous switch loss | 0.13 Ω, 320 mA average forward current during conduction time | 0.0 V |
| Required $V_{C1}$ voltage | Average | 5.5 V |
| $V_{IN(MIN)}$ duty cycle | $V_{IN(MIN)}$ = 16 V<br>$V_{C1(MIN)}$ = 5.5 V | 34% |

The relevant current for the saturation calculation of the transformer consists of two elements, which are the current ripple and the DC current offset as shown in Equation 3. The current ripple is determined by the switching process as in Equation 1 and the DC offset current from the required transfer power as in Equation 2:

$$I_{RIPPLE(PP)} = \frac{\Delta t \times \Delta V}{L} = \frac{\Delta t \times \left(V_{IN} - V_{C1}\right)}{L_{T1}} \quad (1)$$

$$I_{DC} = I_{SEC} = \frac{P_{TPS65130} + P_{J6}}{V_{J6(min)}} \quad (2)$$

$$I_{SAT} > I_{DC} + \frac{1}{2} \times I_{RIPPLE(PP)} \quad (3)$$

The starting point for the calculation is the secondary voltage $V_{J6}$. The minimum level for it is 4.6 V. At this level, the TPS65130 has an efficiency of 70% (interpolated from its datasheet). For the specified output power of 450 mW, therefore, the device needs 643 mW from the J6 rail. Together with the power from J6 of 92 mW at 4.6 V, this corresponds to a current of 160 mA. Based on Table 2, this corresponds to a voltage $V_{C1}$ of 5.5 V at 100% load. This voltage determines the duty cycle and as such affects the relevant timing for the ripple current.

The selected transformer T1 maintains 95% of its inductance up to a current of 600 mA and 80% of its inductance up to a current of 1100 mA. At a DC current of 160 mA per Equation 3, this leaves room for a 440-mA ripple current peak to peak without complicating the calculations. Based on Equation 1, this allows an on-time of 0.92 us at a $V_{IN}$ of 16 V and 0.32 us at $V_{IN}$ of 36 V. To support 36 V, the minimum frequency has to be calculated from the 0.32 us. With the duty cycle of 16% at 36 V, the cycle time is 2.1 us corresponding to a frequency of 480 kHz. Therefore, the 500 kHz in the initial calculations are safe to use and there is enough safety margin to prevent core saturation.

Based on Table 2, $V_{C1}$ needs to be 5.5 V. The feedback resistor network calculates as per Equation 4 and Equation 5. The resistor RFB1 is set to 2 kΩ, resulting in a divider current of 1 mA. If the design is located in a noise-free environment, a smaller divider current could be selected. However, 2 kΩ is a good starting point for an industrial design.

$$V_{OUT} = V_{FB} \times \left( \frac{R_{FB2}}{R_{FB1}} + 1 \right) = 2.0\ V \times \left( \frac{R_{R8}}{R_{R6}} + 1 \right) \quad (4)$$

$$\frac{R_{R8}}{R_{R6}} = \frac{5.5\ V}{2.0\ V} - 1 = 1.615 \quad (5)$$

R8 = 3.48 kΩ and R6 = 2 kΩ are chosen to respect standard resistor values. The power loss in the feedback divider is 5.5 V × 1 mA = 5.5 mW. The regulated voltage is then 5.48 V.

The regulator sets its switching trip point according to the bottom level of the ripple voltage so that the average voltage is higher by approximately half the ripple voltage. This means for an accurate regulated voltage, the voltage ripple of C1 has to be considered. With the capacitance of 2.2 µF (1 µF degraded) and a ripple current of 440 mA at a frequency of 500 kHz, the ripple voltage is simulated to be 67 mV resulting in an average voltage increase at C1 of 33 mV. R5, C6, R7, and C7 add an artificial ripple with the amplitude of 60 mV to the feedback input. With the calculated network, this corresponds to a virtual ripple of 164 mV at C1 and an average increase of 82 mV. Together with the real ripple of 33 mV, this results in an increase of the average voltage at C1 of 115 mV so that the voltage is 5.6 V (used in Equation 8). At a 100% load and $V_{IN}$ = 16 V, the voltage at J6 is therefore 4.7 V. At $V_{IN}$ = 32 V and a 10% load, it is 5.1. This is confirmed by the measurements in section 7 and covered by the specification.

### 4.2 LM5160 Switching Frequency

In Section 4.1, the switching frequency was determined with 500 kHz. It provides an efficiency of > 70% for the DC/DC converter and sets the time for energy transfer from the primary to the secondary transformer side to 1.3 us at 34% duty cycle ($V_{IN(MIN)}$). R4 sets the nominal switching frequency based on the following equations:

$$f_{SW} = \frac{V_{C1}}{10^{-10} \times R_{R4}} \quad (6)$$

$$R_{R4} = \frac{V_{C1}}{10^{-10} \times f_{SW}} \quad (7)$$

$$R_{R4} = \frac{5.6\ V}{10^{-10}\ A \times 500000} = 112\ k\Omega \quad (8)$$

The closest standard resistor value is 113 kΩ.

### 4.3 LM5160 Feedback Loop Design

The LM5160 uses a constant on-time control scheme, which requires an appropriate voltage ripple of > 25 mV at the feedback node. To ensure the correct ripple injection in the regulation loop, three different schemes are possible. This design follows the scheme as per *AN-2292 Designing an Isolated Buck (Flybuck) Converter* with some modifications required to support the large input voltage range and low input voltage. The ripple is simulated to 60 mV.

## 5 Getting Started Hardware

To evaluate the design, follow these steps:

1. Apply the loads to the connectors J6, J9, and J11.
2. Connect J4 to a settable power supply.
3. Set the power supply voltage to 16 V.
4. Enable the power supply.
5. Examine design behavior at required conditions.

## 6 Test Setup

This design is tested for a minimum starting input voltage of 16 V ($V_{IN(MIN)}$) and maximum of 36 V ($V_{IN(MAX)}$). The test wiring is shown in Figure 5.

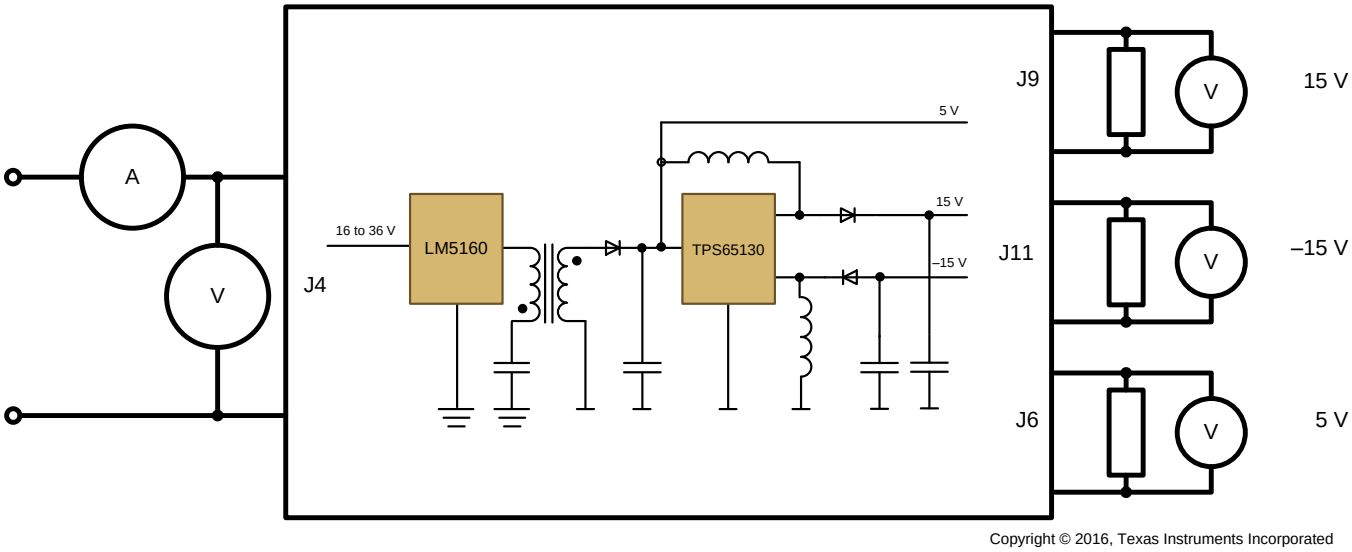





**Figure 5. Test Wiring**

The output load resistors were set according to Table 3.

**Table 3. Tested Output Loads**

| LOAD (%) | R (kΩ) at J6 | R (kΩ) at J9 and J11 |
|---|---|---|
| 0 | ∞ | ∞ |
| 10 | 2.500 | 10.0 |
| 20 | 1.251 | 5.0 |
| 100 | 0.250 | 1.0 |
| 200 | 0.125 | 0.5 |

## 7 Test Data

Table 4 to Table 8 show the results of the tested scenarios. The input voltage of 12 V is tested after startup by reducing the input voltage from 16 V down to 12 V. This simulates a drop-out scenario.

**Table 4. Test at No Load**

| PARAMETER | | DROP-OUT | MIN $V_{IN}$ | TYP $V_{IN}$ | MAX $V_{IN}$ |
|---|---|---|---|---|---|
| $V_I$ (V) | | 12 | 16 | 24 | 32 |
| $I_{IN}$ (A) | | 0.0132 | 0.0142 | 0.0152 | 0.016 |
| $P_{IN}$ (W) | | 0.1584 | 0.2272 | 0.3648 | 0.512 |
| $P_{OUT}$ (W) | | 0 | 0 | 0 | 0 |
| Eff (%) | | 0 | 0 | 0 | 0 |
| $V_o$ (V) | J6 | 5.39 | 5.47 | 5.67 | 5.96 |
| | J9 | 14.97 | 14.96 | 14.96 | 14.97 |
| | J11 | –14.95 | –14.95 | –14.95 | –14.95 |

**Table 5. Test at 10% Load**

| PARAMETER | | DROP-OUT | MIN $V_{IN}$ | TYP $V_{IN}$ | MAX $V_{IN}$ |
|---|---|---|---|---|---|
| $V_I$ (V) | | 12 | 16 | 24 | 32 |
| $I_{IN}$ (A) | | 0.0196 | 0.0189 | 0.0183 | 0.0183 |
| $P_{IN}$ (W) | | 0.2352 | 0.3024 | 0.4392 | 0.5856 |
| $P_{OUT}$ (W) | | 0.054821 | 0.054902 | 0.055053 | 0.055175 |
| Eff (%) | | 0.233082 | 0.181553 | 0.125348 | 0.09422 |
| $V_O$ (V) | J6 | 5.03 | 5.05 | 5.08 | 5.11 |
| | J9 | 14.95 | 14.95 | 14.96 | 14.96 |
| | J11 | –14.95 | –14.95 | –14.95 | –14.95 |

**Table 6. Test at 20% Load**

| PARAMETER | | DROP-OUT | MIN $V_{IN}$ | TYP $V_{IN}$ | MAX $V_{IN}$ |
|---|---|---|---|---|---|
| $V_I$ (V) | | 12 | 16 | 24 | 32 |
| $I_{IN}$ (A) | | 0.0261 | 0.0237 | 0.0216 | 0.0208 |
| $P_{IN}$ (W) | | 0.3132 | 0.3792 | 0.5184 | 0.6656 |
| $P_{OUT}$ (W) | | 0.108968 | 0.109126 | 0.109305 | 0.109465 |
| Eff (%) | | 0.347919 | 0.287781 | 0.210851 | 0.164461 |
| $V_O$ (V) | J6 | 4.94 | 4.96 | 4.99 | 5.01 |
| | J9 | 14.95 | 14.95 | 14.95 | 14.95 |
| | J11 | –14.96 | –14.96 | –14.95 | –14.95 |

**Table 7. Test at 100% Load**

| PARAMETER | | DROP-OUT | MIN $V_{IN}$ | TYP $V_{IN}$ | MAX $V_{IN}$ |
|---|---|---|---|---|---|
| $V_I$ (V) | | 12 | 16 | 24 | 32 |
| $I_{IN}$ (A) | | 0.085 | 0.066 | 0.05 | 0.043 |
| $P_{IN}$ (W) | | 1.02 | 1.056 | 1.2 | 1.376 |
| $P_{OUT}$ (W) | | 0.530587 | 0.534994 | 0.533144 | 0.536038 |
| Eff (%) | | 0.520184 | 0.506623 | 0.444286 | 0.389563 |
| $V_O$ (V) | J6 | 4.53 | 4.65 | 4.6 | 4.67 |
| | J9 | 14.94 | 14.94 | 14.94 | 14.95 |
| | J11 | –15.01 | –15.01 | –15.01 | –15.01 |

**Table 8. Test at 200% Load**

| PARAMETER | | DROP-OUT | MIN $V_{IN}$ | TYP $V_{IN}$ | MAX $V_{IN}$ |
|---|---|---|---|---|---|
| $V_I$ (V) | | 12 | 16 | 24 | 32 |
| $I_{IN}$ (A) | | 0.161 | 0.12 | 0.085 | 0.0675 |
| $P_{IN}$ (W) | | 1.932 | 1.92 | 2.04 | 2.16 |
| $P_{OUT}$ (W) | | 1.020039 | 1.039678 | 1.05067 | 1.053503 |
| Eff (%) | | 0.52797 | 0.541499 | 0.515035 | 0.487733 |
| $V_o$ (V) | J6 | 3.98 | 4.26 | 4.41 | 4.45 |
| | J9 | 14.91 | 14.92 | 14.93 | 14.93 |
| | J11 | –14.98 | –14.99 | –14.99 | –14.99 |

Figure 6 shows a thermal plot of the board when used at 100% of the specified load. The most warm spot is the secondary side Schottky rectifier diode of the 5-V rail. If necessary, its temperature could be reduced by increasing the copper area connected to the diode terminals. The temperature rise is 28 K so the board could operate beyond 100°C.

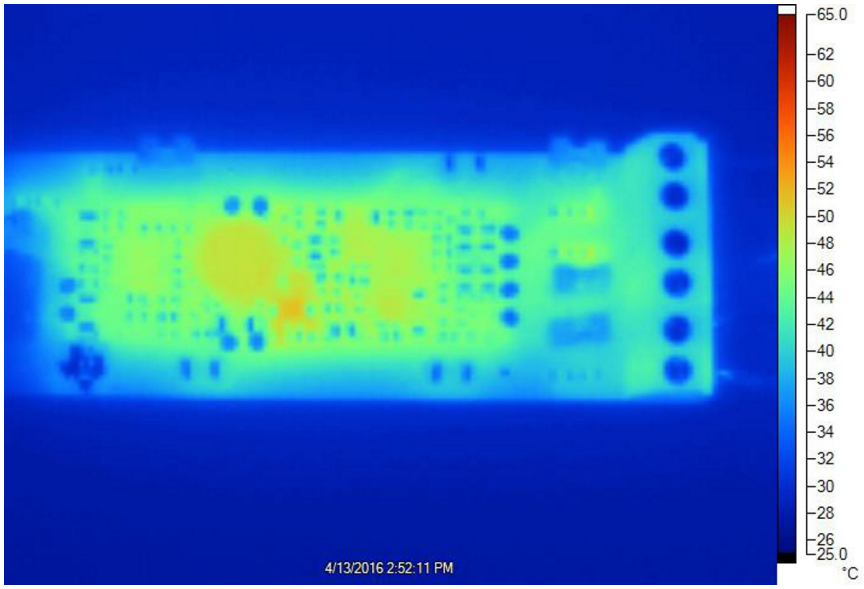



**Figure 6. Thermal Plot of TIDA-00689 at 100% Load**

Figure 7 shows the board at 200% of the specified load. Then the temperature rise is 40 K and the board could still work up to an environment temperature of 85°C.

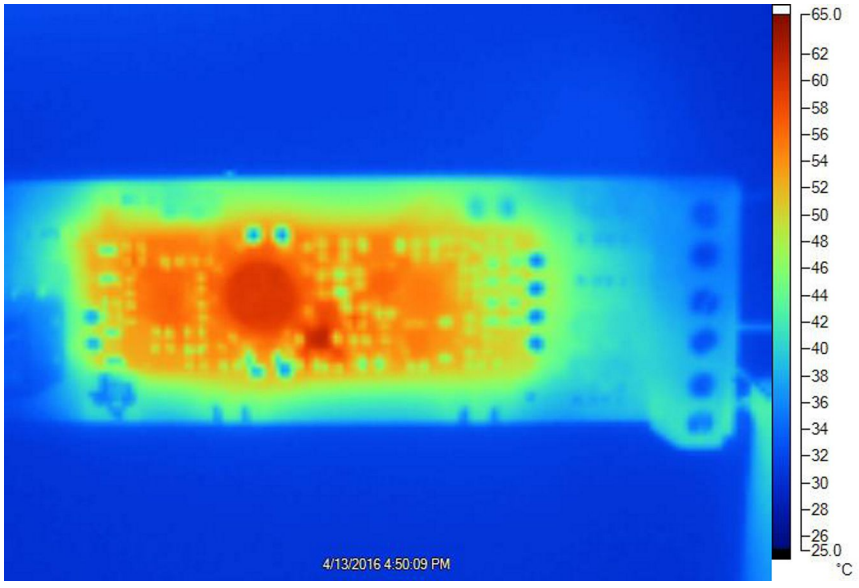



**Figure 7. Thermal Plot of TIDA-00689 at 200% Load**

Both plots show an even distribution of the thermal energy. This comes from the inner and bottom copper layers, which are working as heat spreaders.

# 8 Design Files

## 8.1 Schematics

To download the schematics, see the design files at TIDA-00689.

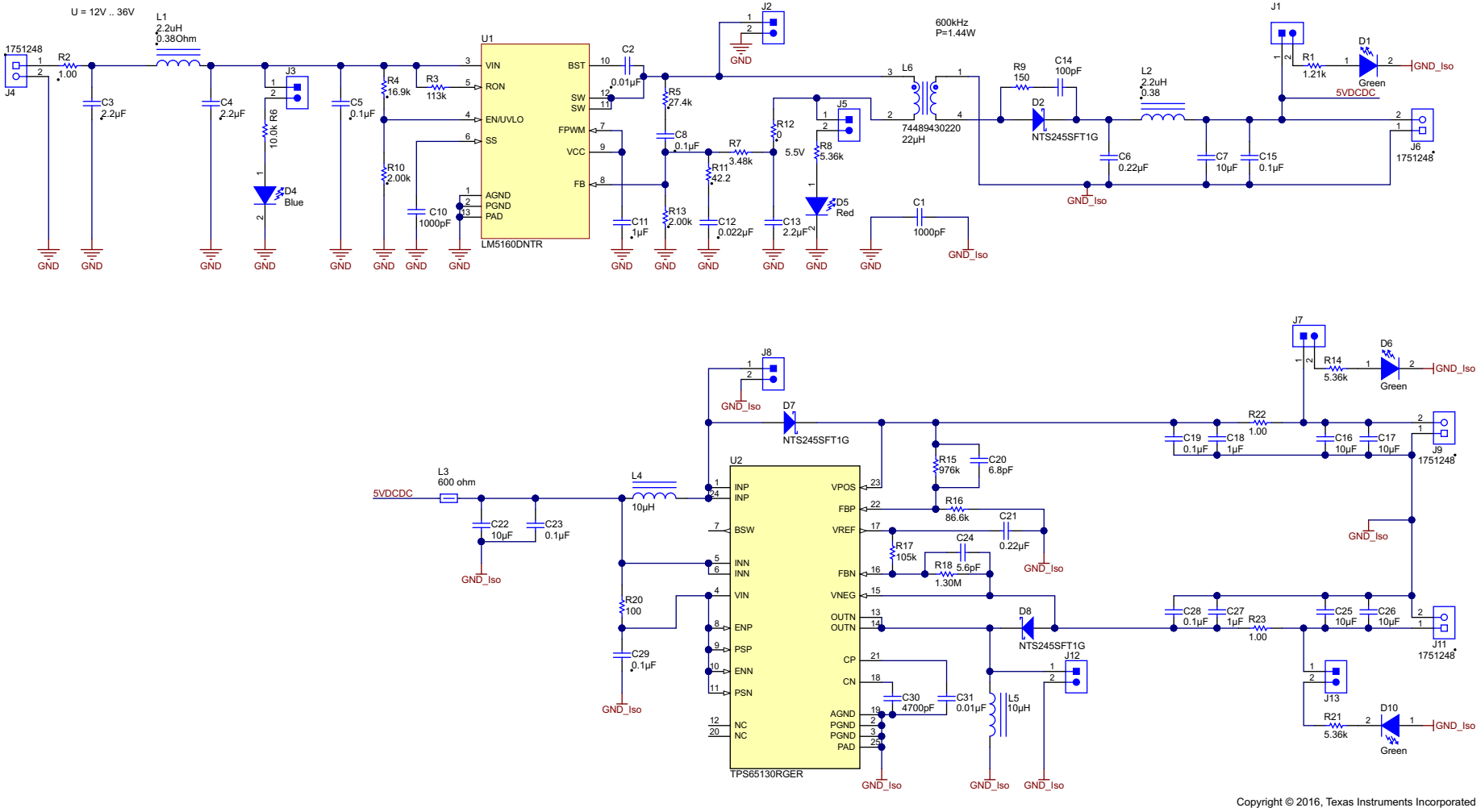





**Figure 8. TIDA-00689 Schematics**

## 8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00689.

## 8.3 PCB Layout Recommendations

The PCB layout is determined by contradicting requirements. The first design goal was a small form-factor design. The second design goal addressed cost. The other two goals were usability in industrial environment at ambient temperatures of up to 85˚C and low EMI as well as low output voltage noise. To get a small form factor, all components have been grouped together as much as possible without violating placement rules. To keep the cost low, only 0603-sized or larger components are used in the design. The layout has been implemented on a four layer board with 35-um copper. Each IC got enough copper heat sink area to provide the maximum specified power at an ambient temperature of 85˚C.

### 8.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00689.

## 8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00689.

## 8.5 Layout Guidelines

The following pre-cautions help to avoid excessive EMI generation and unstable behavior of the circuit. Figure 9 shows the primary side of the TIDA-00689 with the switching IC LM5160. Main energy reservoir for the switching edges is C5 in the white circle. It needs to be very close to the IC with shortest possible connections. In Fly-Buck operation the current flow through the primary side of the isolating transformer is alternatingly terminated into ground and Vin by the IC. For low EMI, it is important that the area around, which the switching current flows, is as small as possible. For stability, it is important that the positive and negative current flow through the transformer take the same route with only small deviations. This is shown in Figure 10 with the light purple current path 1 and light green current path 2. The ground connection of C13 should be located close to the ground connection of C5. No other components should have a ground connection on the direct path between C13 and C5 as it is the most noisy part. For the other components, the designer has more flexibility. Besides from keeping connections as short as possible, there are no further requirements.

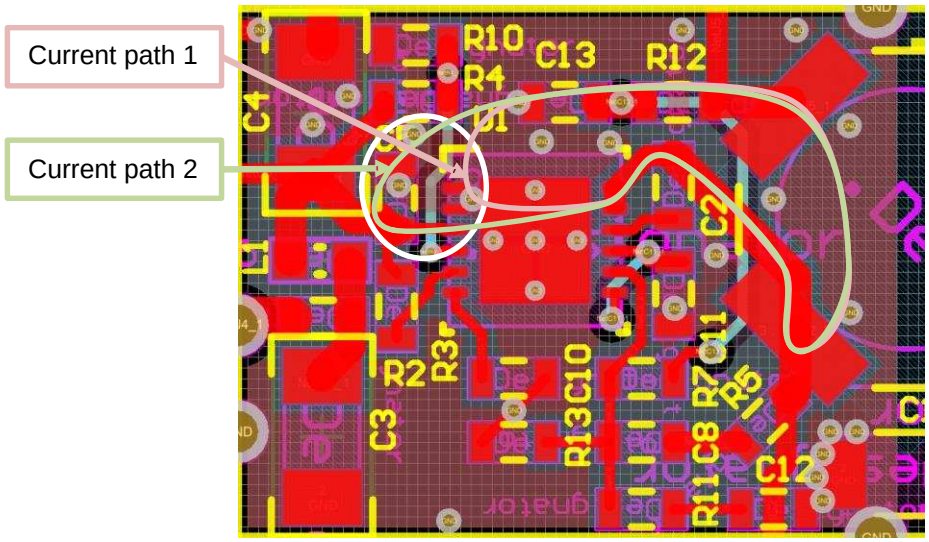



**Figure 9. Current Path on Primary Side of TIDA-00689**

Figure 10 shows the secondary side of the TIDA-00689. Current path 1 is the secondary side of the isolating transformer. The area is kept as small as possible and the connection point for other components is the ground connection of C18. The separation of the rest of the secondary side from this current path is done through L2. Filtering of the 5-V output rail is then done through C15 and C7. A direct trace connects the 5-V output terminal to the positive side of C7. The boost converter input is separated from this 5-V rail through L3. This keeps the switching noise from the converter separate from the 5-V rail. For best EMI performance, the current path areas of the positive and the negative switching sides are as small as possible. This is valid for the active switching part through the IC (current path 3 and 4) and also for the passive part through the rectifier diodes (current path 2 and 5). The output ripple and EMI from the switchers are filtered by RC combinations from R22, C16, and C17 as well as R23, C25, and C26.

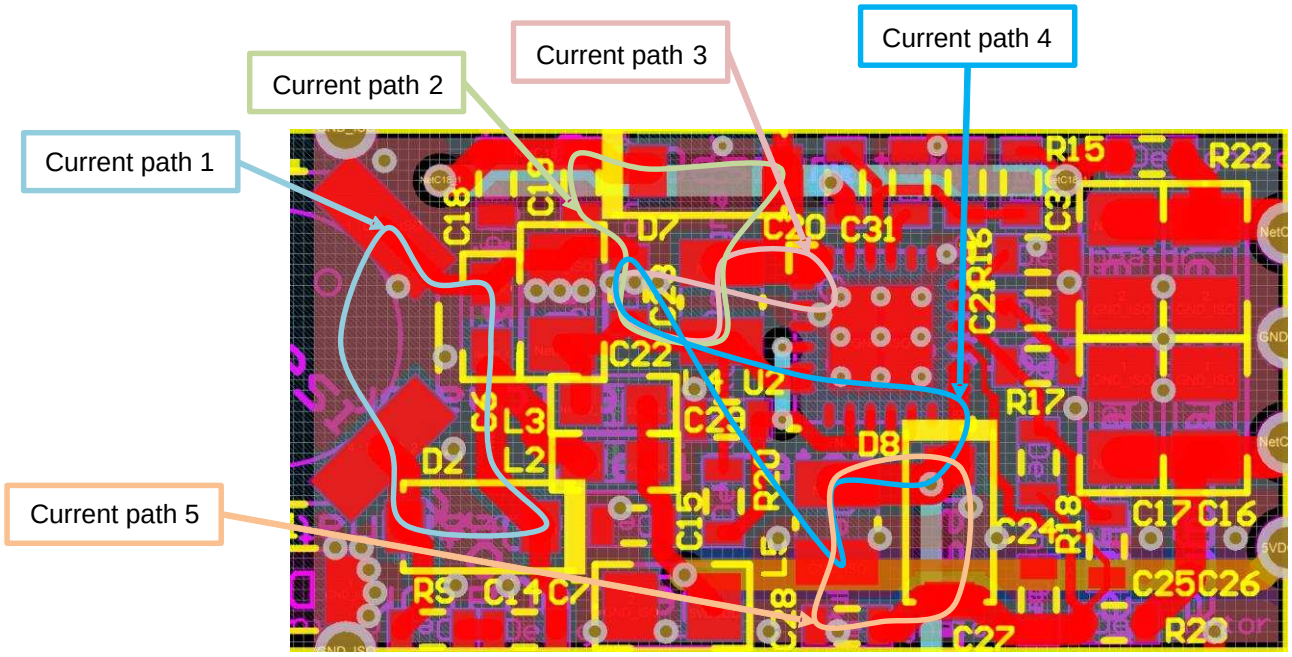



**Figure 10. Current Path on Secondary Side of TIDA-00689**

## 8.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00689.

## 8.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00689.

## 9 References


1. Texas Instruments, *1-W Small Form Factor Power Supply with Isolated Dual Output for PLC I/O Modules*, TIDA-00129 Design Guide (TIDU263)
2. Texas Instruments, *AN-2292 Designing an Isolated Buck (Flybuck) Converter*, Application Note (SNVA674)
3. Texas Instruments, *Ultra-Thin, Small Footprint 1-W, 12- to 36-V Isolated Power Supply With ±15 V and 5 V for Analog PLC Modules*, TIDA-00237 Design Guide (TIDU855)
4. Texas Instruments, *1-W Isolated Power Supply With Planar Transformer Reference Design*, TIDA-00688 Design Guide (TIDUB83)


## 10 About the Author

**INGOLF FRANK** is a systems engineer in the Texas Instruments Factory Automation and Control Team, focusing on PLC I/O modules. Ingolf works across multiple product families and technologies to leverage the best solutions possible for system level application design. Ingolf earned his electrical engineering degree (Dipl. Ing. (FH)) in the field of information technology at the University of Applied Sciences Bielefeld, Germany in 1991.

## Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (June 2016) to A Revision | Page |
|---|---|
| • Changed from preview page | 1 |

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