TI Designs

Self-Powered AC Solid State Relay With MOSFETs

Design Overview

The self-powered AC solid state relay with MOSFETs reference design is a single relay replacement that enables efficient power management for a low-power alternative to standard electromechanical relays in thermostat applications. This SSR reference design is self-powered through the 24-V AC power line, eliminating additional power consumption of a thermostat battery. The MOSFETs can switch fast enough to allow self-charging without affecting the load.

Design Resources

TIDA-00377	Design Folder
ATL431	Product Folder
LP339	Product Folder
SN74AUP1G74	Product Folder
SN74AUP1G17	Product Folder
SN74AUP1G14	Product Folder
SN74AUP2G08	Product Folder
CSD19537Q3	Product Folder
TIDA-00751	Tools Folder

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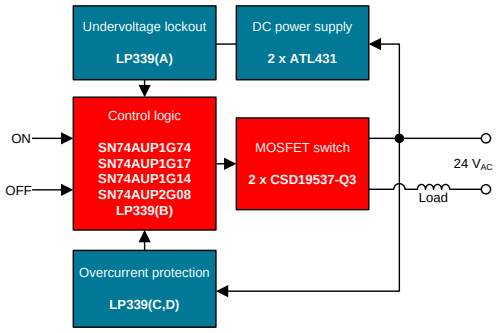
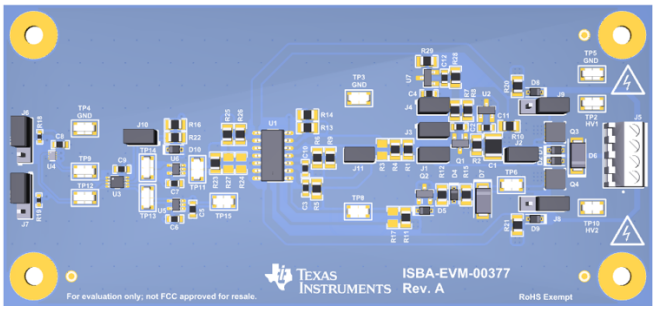
Design Features

- No Clicking Sound
- Cost Efficient BOM
- MOSFET Based Design for Fast ON/OFF Switching
- Self-Powered
- Zero Thermostat Battery Power Consumption
- Inherent Snubber Circuit Reducing Voltage Spike Created by Inductive Load
- Low Power and Quiescent Current Components
- Undervoltage and Overcurrent Protection

Featured Applications

- Building Automation
- HVAC Systems
- Thermostats





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1 Key System Specifications

Table 1. Key System Specifications

SPECIFICATION	VALUE	DETAILS
Logic input level range	3.3 V	See Section 2.3
Max voltage input range	84 V	See Section 2.1
Current range	2 to 6 A_{RMS}	—
Turnon and turnoff time	< 2 µs	See Section 7
On-state current consumption	< 0.4 mA	See Section 7
Off-state current consumption	< 0.3 mA	See Section 7
Operating temperature	0°C to 60°C	—
Working environment	Indoor building automation	—

2 System Description

A solid-state relay (SSR) is an electronic switching device that switches on or off when a small external voltage is applied across its control terminals. SSRs consist of an input logic to respond to an appropriate input (control signal), a solid-state electronic switching device to switch power to the load circuitry, and a coupling mechanism to enable the control signal to activate this switch without mechanical parts. The SSR may be designed to control either an AC or DC voltage or current load. It serves the same function as an electromechanical relay but has no moving parts.

SSRs use power semiconductor devices such as thyristors or transistors to switch currents up to 100 A. SSRs have fast switching speeds compared with electromechanical relays and have no physical contacts to wear out. To apply an SSR, the user must consider their lower ability to withstand momentary overload, compared with electromechanical contacts, and their higher "on" state resistance. Unlike an electromechanical relay, an SSR provides only limited switching arrangements (single-pole, single-throw switching).

This SSR reference design is for a single mechanical relay replacement in low-cost thermostat applications, which only uses one switching relay. The SSR is self-powered through the AC line of the HVAC system and provides undervoltage lockout (UVLO) as well as overcurrent protection (OCP). See Figure 1 for the block diagram.

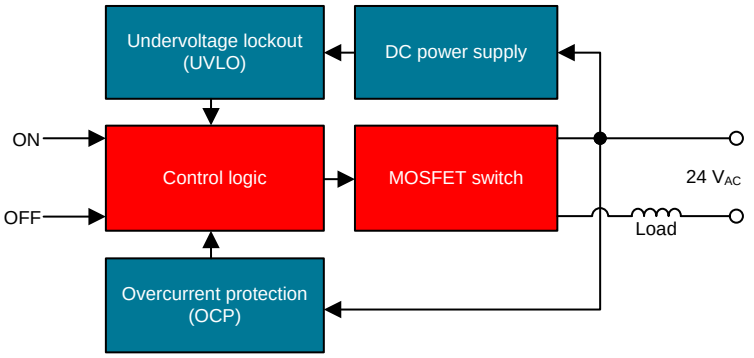

Figure 1. TIDA-00377 SSR With MOSFETs Block Diagram

2.1 Choosing Between SSR Reference Designs

The TI Designs portfolio has two available SSR reference designs, TIDA-00377 and TIDA-00751. They differ in terms of power consumption, galvanic isolation, and voltage and current protection. Table 2 compares features between the two designs.

Table 2. Comparison of SSR Reference Designs

FEATURE	TIDA-00377	TIDA-00751
Self-powered	√	
Isolation		√
Snubber Circuit	√	√
UVLO	√	
OCP	√	

2.1.1 Power Consumption

The TIDA-00377 does not consume any power from the thermostat battery. The device is self-powered and consumes < 0.4 mA from the HVAC system. Alternatively, the TIDA-00751 consumes power from the thermostat battery during both on and off states. The SSR consumes 1.2 mA from the battery during on-state and < 0.2 mA during off state.

2.1.2 Galvanic Isolation

The TIDA-00751 includes galvanic isolation, whereas the TIDA-00377 does not. The TIDA-00377 is designed for single relay replacement in low-cost thermostats connecting to one transformer and therefore isolation is not needed. If necessary, a small pulse transformer can be added to the design for galvanic isolation.

2.1.3 Voltage and Current Protection

The TIDA-00377 includes both protection circuits, whereas the TIDA-00751 does not. This OCP is to protect the MOSFET switch from overcurrent and to detect short circuits. The UVLO protects the DC power supply of the SSR, enabling the self-powering feature.

2.2 N-Channel Power MOSFET

In residential as well as commercial building automation applications, 24 V_{AC} is used as the standard power supply voltage. When an SSR is used in thermostat applications as replacement for the mechanical relay, the maximum operating voltage of the power switch can be two times the nominal voltage because some systems operate with two transformers. Taking into account the input voltage variations, 20 to 30 V_{AC}, the peak DC voltage rises up to 42 V. In the worst case, the power switch can operate at up to 84 V_{DC}. For that reason, this design uses power MOSFETs with a breakdown voltage of 100 V.

2.3 Input Logic Control

In thermostat applications, power consumption is a main concern. To ensure a long battery life, the control logic, in most cases a dedicated microcontroller, provides a control signal for a short period of time before it goes in a low power or sleep mode. Turn-on and turn-off signals are two different signals that are active for short periods of the time. For that reason, the input control logic uses the Texas Instruments a low-power AUP D-type flip-flop, the SN74AUP1G74 with a 3.3-V supply voltage. This circuit will set the output signal high on a short, low ON pulse and reset the output signal low when a short, low OFF signal is applied.

2.4 Power Management

Power consumption is another main concern in thermostat applications because the circuitry, which makes up the thermostat control, consumes its power from an onboard battery. To avoid additional power consumption and increase the lifetime of the battery, this SSR reference design is self-powered through the 24-V_{AC} power line. By using the body diodes of the power MOSFETs and two additional diodes, the 24 V_{AC} is rectified to 33 V_{DC}, which is further stepped down to provide power to the remaining of the SSR circuitry. The voltage regulation is performed by two low-power shunt regulators, ATL431, with a quiescent current of 25 μA.

2.5 UVLO

For proper voltage regulation of the DC power supply, the input DC voltage must maintain a certain threshold level. If the rectified AC voltage of the load, V_{DC}, drops below the desired rail voltages, the shunt regulators will no longer be able to regulate, disabling the operability of the SSR. Due to the nature of the DC power supply during the ON time of the MOSFETs, the DC supply capacitor will want to fully discharge. To prevent this, a reference voltage is set on the UVLO to turn off the MOSFETs when the minimum voltage is met and allows the DC supply capacitor to recharge. This will keep V_{DC} at a voltage where the shunt regulators can regulate properly.

2.6 Overcurrent Protection

An additional technique to monitor the functionality of the system is monitoring the current levels through the saturation voltage of the MOSFET. When a component fails, it can result in an open or short circuit. By monitoring the load current level of the 24-V_{AC} power supply, different issues can be detected including overcurrent and short circuits in the entire SSR system and malfunctioning of the MOSFETs.

3 Block Diagram

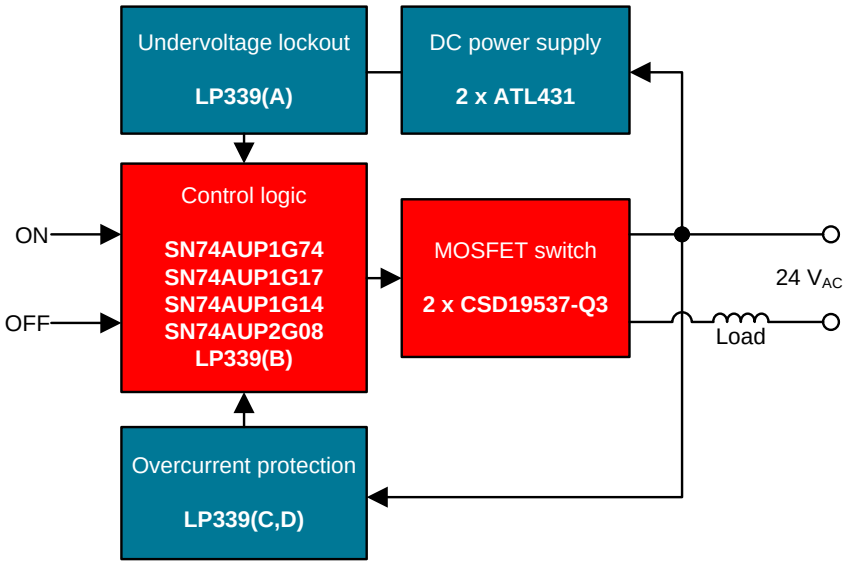

Figure 2. TIDA-00377 SSR With MOSFET Block Diagram With Component List

3.1 Highlighted Products

The SSR reference design features the following devices:

- CSD19537Q3: 100-V N-Channel NexFET Power MOSFET
- SN74AUP1G74: Low-Power Single Positive-Edge-Triggered D-Type Flip-Flop
- SN74AUP1G17: Low-Power Single Schmitt-Trigger Buffer
- SN74AUP1G14: Low-Power Single Schmitt-Trigger Inverter
- SN74AUP2G08: Low-Power Dual 2-Input Positive-AND Gate
- ATL431: 2.5V Low I_Q Adjustable Precision Shunt Regulator
- LP339: Low-Power Quad Differential Comparators

3.1.1 CSD19537Q3

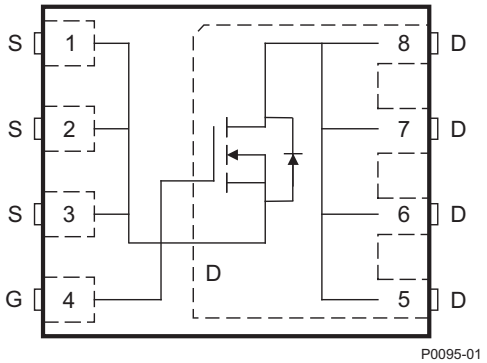

Figure 3. CSD19537-Q3 Functional Block Diagram

Features:

- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free
- SON 3×3-mm plastic package

3.1.2 SN74AUP1G74

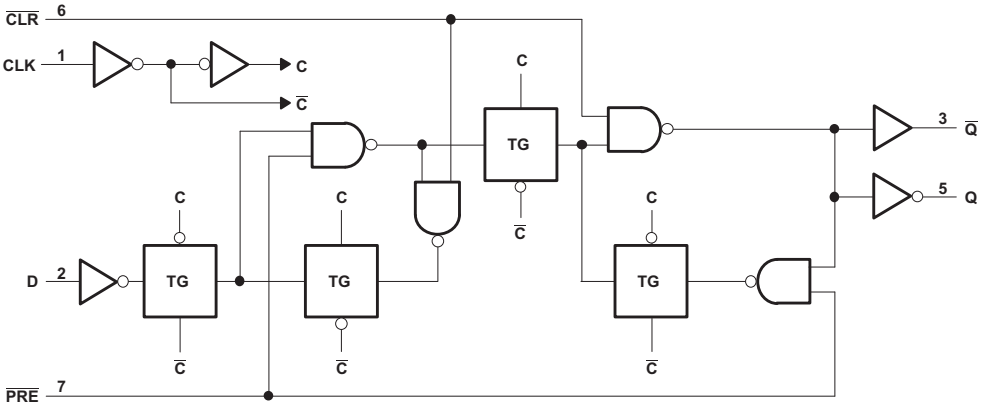

Figure 4. SN74AUP1G74 Functional Block Diagram

Table 3. SN74AUP1G74 Logic Table

INPUTS			OUTPUTS		
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
X	L	X	X	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Features:

- Available in the Texas Instruments NanoStar package
- Low static-power consumption: I_{CC} = 0.9 μA maximum
- Low dynamic-power consumption: C_{pd} = 5.5 pF typical at 3.3 V
- Low input capacitance: C_i = 1.5 pF typical
- Low noise: overshoot and undershoot < 10% of V_{CC}
- I_{OFF} supports partial-power-down mode operation
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the input (V_{HYS} = 250 mV typical at 3.3 V)
- Wide operating V_{CC} range of 0.8 to 3.6 V
- Optimized for 3.3-V operation
- 3.6-V I/O tolerant to support mixed-mode signal operation
- t_{PD} = 5 ns maximum at 3.3 V
- Suitable for point-to-point applications
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested per JESD 22
  - 2000-V human-body model (A114-B, Class II)
  - 1000-V charged-device model (C101)

3.1.3 SN74AUP1G17

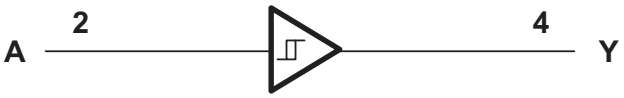

Figure 5. SN74AUP1G17 Functional Block Diagram

Table 4. SN74AUP1G17 Logic Table

INPUT A	OUTPUT Y
H	H
L	L

Features:

- Available in the Texas Instruments NanoStar™ package
- Wide operating VCC range of 0.8 to 3.6 V
- Optimized for 3.3-V operation
- Low static-power consumption (I_{CC} = 0.9 μA max)
- 3.6-V I/O tolerant to support mixed-mode signal operation
- Low dynamic-power consumption (C_{pd} = 4.4 pF typ at 3.3 V)
- t_{pd} = 5.1 ns max at 3.3 V
- Suitable for point-to-point applications
- Low input capacitance (C_i = 1.5 pF typ)
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- Low noise overshoot and undershoot < 10% of V_{CC}
- I_{OFF} supports partial-power-down mode operation
- Includes Schmitt-trigger inputs
- ESD performance tested per JESD 22
  - 2000-V human-body model (A114-B, Class II)
  - 1000-V charged-device model (C101)

3.1.4 SN74AUP2G08

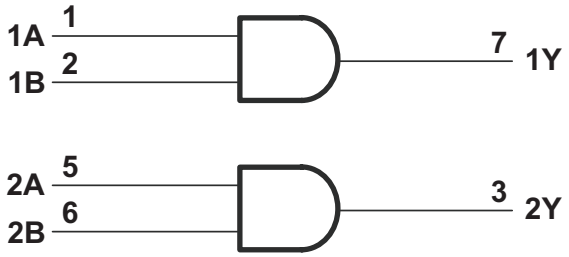

Figure 6. SN74AUP2G08 Functional Block Diagram

Table 5. SN74AUP2G08 Logic Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

Features:

- Available in the Texas Instruments NanoStar™ package
- Wide operating VCC range of 0.8 to 3.6 V
- Optimized for 3.3-V operation
- Low static-power consumption (ICC = 0.9 mA max)
- 3.6-V I/O tolerant to support mixed-mode signal operation
- Low dynamic-power consumption (C_{pd} = 4.3 pF typ at 3.3 V)
- t_{pd} = 5.9 ns max at 3.3 V
- Suitable for point-to-point applications
- Low input capacitance (Ci = 1.5 pF typ)
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- Low noise overshoot and undershoot < 10% of V_{CC}
- ESD performance tested per JESD 22
  - 2000-V human-body model (A114-B, Class II)
  - 1000-V charged-device model (C101)
- I_{OFF} supports partial-power-down mode operation
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the input (V_{HYS} = 250 mV typ at 3.3 V)

3.1.5 ATL431

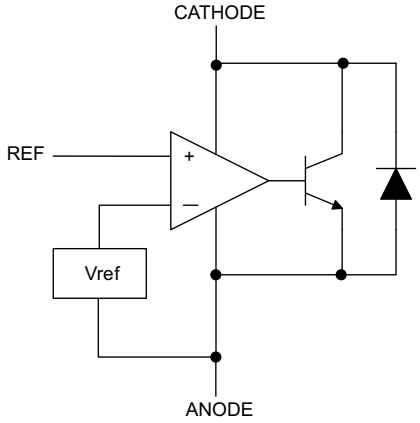

Figure 7. ATL431 Functional Block Diagram

Features:

- Adjustable regulated output of 2.5 to 36 V
- Very-low operating current
  - $I_{KA(min)}$ = 35 μA (max)
  - I_{REF} = 150 nA (max)
- Internally compensated for stability
  - Stable with no capacitive load
- Reference voltage tolerances at 25°C
  - 0.5% for ATL43xB
  - 1% for ATL43xA
- Typical temperature drift
  - 5 mV (–40°C to 85°C); I version
  - 6 mV (–40°C to 125°C); Q version
- Extended cathode current range of 35 μA to 100 mA
- Low output impedance of 0.3 Ω (max)

3.1.6 LP339

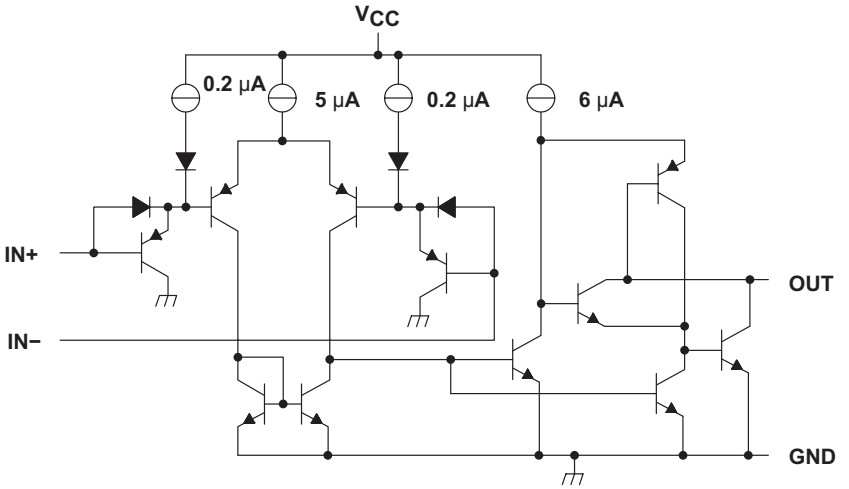

Figure 8. LP339 Schematic Diagram (Each Comparator)

Features:

- Ultra-low power supply current drain
- (60 µA)—independent of the supply voltage
- (75 µW/comparator at 5 VDC
- Low input biasing current: 3 nA
- Low input offset current: ±0.5 nA
- Low input offset voltage: ±2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at V_O = 2 V_{DC})
- Supply input protected against reverse voltages

4 System Design Theory

4.1 Basic SSR Theory

An alternative to the electromechanical switch is an SSR with a MOSFET. SSRs are integrated electrical circuits that act as a mechanical switch. The relays can be switched much faster and are not prone to wear because of the absence of moving parts. Another advantage is that less current and voltage is needed for SSRs to control high-voltage AC loads.

This design uses a two N-channel MOSFET topology serving two main functions. The first function is to perform the switching. By using two MOSFETs, both positive and negative currents are allowed to flow during the ON time by using the body diode of one of the MOSFETs for the positive current and the other for the negative current, as shown in the left side of Figure 9. During the OFF time, the body diodes block the current flow because the top and bottom body diode become reverse bias, as shown in the right side of Figure 9.

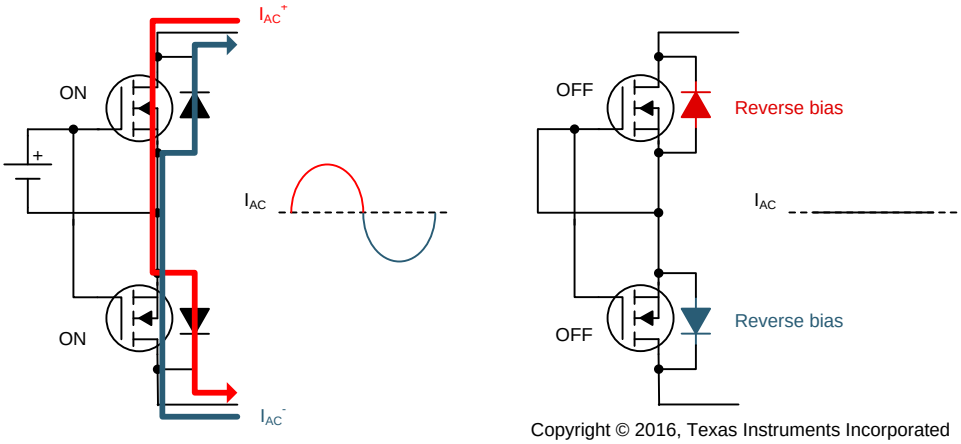

Figure 9. Functionality of MOSFETs for (Left) ON and (Right) OFF Times

The second function of the two N-channel MOSFET topology is to self-power the system by assisting in the AC voltage rectification. See Section 4.2 for further description.

4.2 Basic Power Management Theory

The two MOSFET body diodes of the switch and two external diodes create a full wave rectification circuit that converts the AC power supply at the load to a DC voltage that can then be stepped down to desired levels. The control logic and gate driver are powered by the resulting DC voltage and therefore does not consume any power from the thermostat battery.

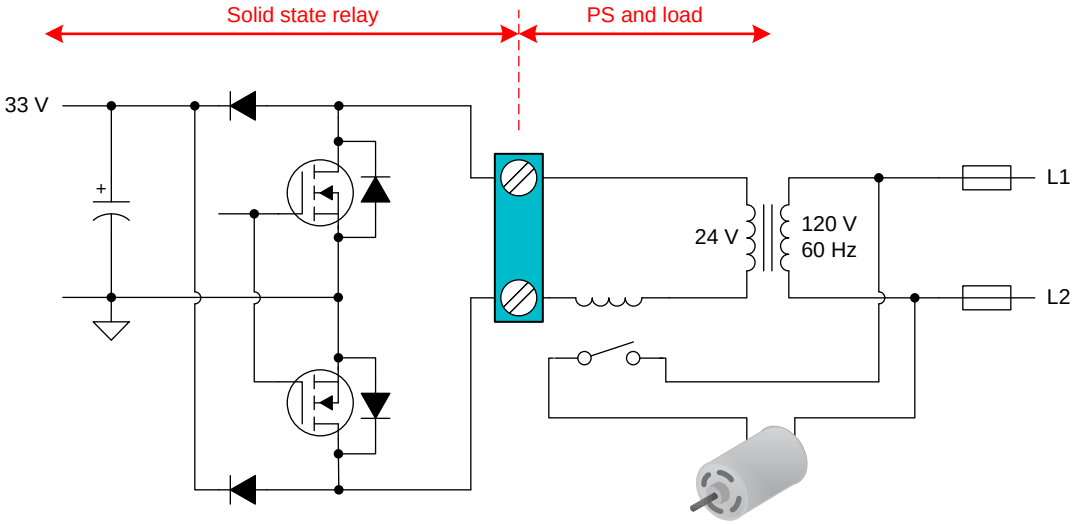

Figure 10. Power Supply of SSR in HVAC System

4.2.1 Full-Wave Rectification

When the SSR is not active, the 24-V_{AC} voltage from the HVAC system, across HV1 and HV2, is rectified using D1 and D2 in addition to the two body diodes of the MOSFETs. When the MOSFETs are off, the resulting full-wave rectified waveform has a peak DC voltage of 34 V, calculated by Equation 1.

$$V_{P\_DC} = \sqrt{2} \times V_{AC} - 2 \times V_F \quad (1)$$

By adding the capacitor, the rectified AC waveform is smoothed out providing a nominal average DC voltage. The ripple of the DC voltage is determined by the value of the capacitor and the current flowing through it over a period of time, as described in Equation 2.

$$\Delta V_{DC} = \frac{i \times \Delta t}{C_{DC}} \quad (2)$$

The resulting waveforms are shown in Figure 11.

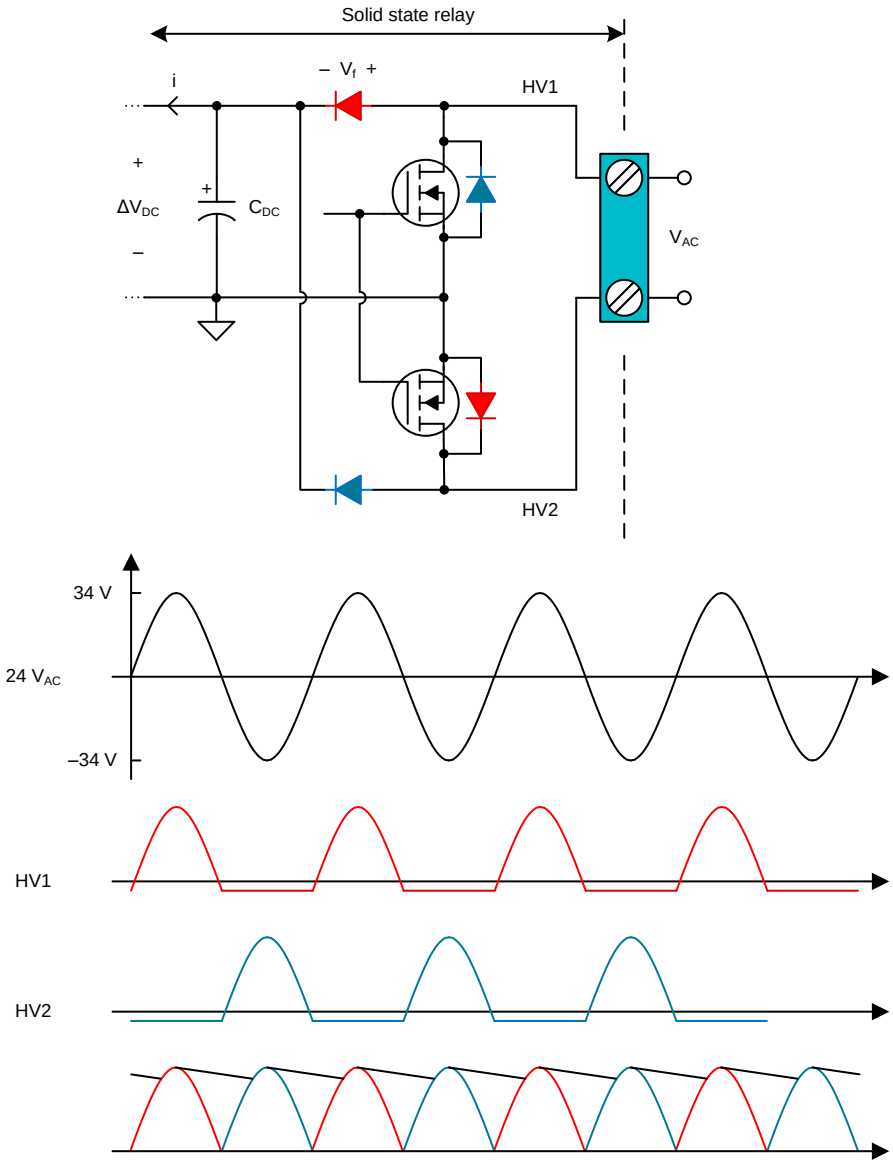

Figure 11. Full-Wave Rectification Circuitry and Waveforms

When the switch is active, allow a discharge time of approximately 6 cycles of the full-wave rectification waveform to prevent the capacitor voltage decreasing below the reference voltage of the UVLO (18 V) when the AC input voltage is low. This increases the delay to turn on the MOSFETs and increases the chances of instability of the DC power supply. The discharge time of 6 cycles prevents frequent recharging of the capacitor and ensures that the capacitor is not too large. The capacitor value of 3.3 μF allows for the capacitor to discharge 6 V_{PP} over 6 cycles when the SSR is active.

4.2.2 DC Power Supplies

The two DC rail voltages used in this reference design are 10 V and 3.3 V. The 10-V supply rail is chosen based on the gate-to-source voltage on the MOSFETs to provide a low on-state resistance (Figure 12). The 3.3-V supply rail is chosen due to the required supply range of the logic components used in the logic control portion of this reference design.

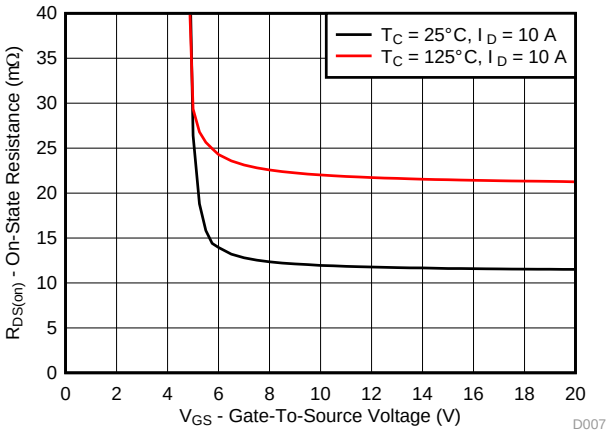

Figure 12. On-State Resistance as a Function of Gate-to-Source Voltage of CSD19537Q3

4.2.2.1 10-V Power Supply

The 10-V supply uses the low I_q adjustable precision shunt regulator ATL431. Along with the regulator are three resistors with the DC supply voltage provided by the rectified AC input voltage. One of the resistors, R_3, provides the cathode current, I_{KA}, and the other two creates a resistive divider to set the output voltage, V_{OUT}. The NPN transistor provides power to the 3.3-V supply, logic control, and protection blocks of the SSR, reducing the total power consumption of R_3.

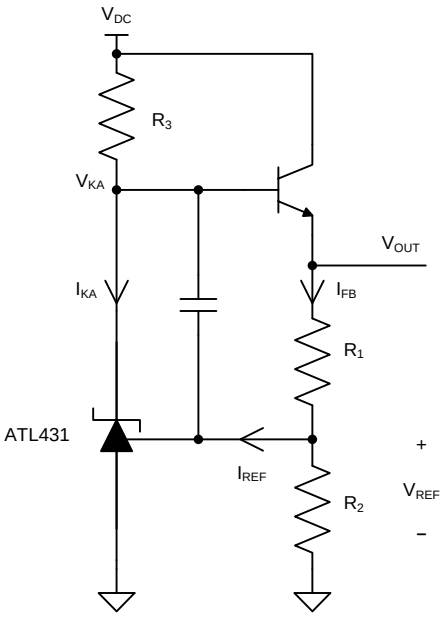

Figure 13. Schematic of 10-V Supply

Table 6. ATL431 Electrical Characteristics Over Recommended Operating Conditions 25˚C(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_{KA} = 1 mA		2475	2500	2525	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range	$V_{KA} = V_{REF}$ I_{KA} = 1 mA	ATL43xAI; T_A = –40°C to 85°C		5	15	mV
			ATL43xAQ; T_A = –40°C to 125°C		6	34	
ΔV_{REF} / ΔV_{KA}	Ratio of change in reference voltage to change in cathode voltage	I_{KA} = 1 mA	ΔV_{KA} = 10 V – V_{REF}		–0.4	–2.7	mV/V
			ΔV_{KA} = 36 V – 10 V		–0.1	–2	
I_{REF}	Reference input current	I_{KA} = 1 mA, R1 = 10 kΩ, R2 = ∞			30	150	nA
$I_{I(dev)}$	Deviation of reference input current over full temperature range	I_{KA} = 1 mA, R1 = 10 kΩ, R2 = ∞			20	50	nA
I_{MIN}	Minimum cathode current for regulation	$V_{KA} = V_{REF}$			20	35	µA
I_{OFF}	Off-state cathode current	V_{KA} = 36 V, V_{REF} = 0			0.05	0.2	µA
$\|Z_{KA}\|$	Dynamic impedance	$V_{KA} = V_{REF}$, f ≤ 1 kHz, I_{KA} = 1 to 100 mA			0.05	0.3	Ω

(1) Over recommended operating conditions, T_A = 25°C (unless otherwise noted)

Table 6 specifies when $V_{KA} = V_{REF}$ and I_{KA} is 1 mA the nominal V_{REF}, (labeled as V_{NOM}) is 2.5 V. The reference voltage varies with cathode voltage at two different rates; it is –0.4 mV/V from V_{REF} to 10 V, and –0.1 mV/V above 10 V. The reference pin current is 30 nA.

The Z_{KA} parameter offsets V_{REF} by ($I_{KA} – I_{NOM}$) × Z_{KA}. In addition, the $\Delta V_{REF}/\Delta_{VKA}$ parameter offsets V_{REF} by either –0.4 mV × (V_{KA} – 2.500 V), if V_{KA} ≤ 10 V, or –10.5 mV – 0.1 mV/V × (V_{KA}–10 V) if V_{KA}>10 V. The "–10.5 mV" constant is the V_{REF} offset as V_{KA} changes from V_{NOM} to 10 V, (10 V –2.500 V) × –0.4 mV/V.

For the 10-V supply, the parameters for V_{KA} > 10 V are used for Equation 3 because V_{KA} = 10.6 V due to the voltage drop across the NPN transistor.

$$V_{REF} = V_{NOM} + \left(I_{KA} - I_{NOM}\right) \times Z_{KA} + \left(V_{KA} - 10\right) \times \left(-0.1\,mV / V\right) - 10.5\,mV \quad (3)$$

Now that V_{REF} is solved, determine R_1 and R_2.

$$R_1 = \frac{\left(V_{KA} - V_{REF}\right)}{I_{FB}} \quad (4)$$

$$R_2 = \frac{V_{REF}}{\left(I_{FB} - I_{REF}\right)} \quad (5)$$

NOTE: R2 has less current than R1.

The design goal is to set the cathode of the ATL431 to 10.6 V by providing a minimum cathode current of 20 μA, and a feedback current and resistor bridge that will keep V_{KA} within a narrow supply range of ±2 to 3%. The following parameters are calculated using the formula derived in the general example for V_{KA} > 10 V.

$$V_{REF} = 2.500\,V + \left(20\,\mu A - 1\,mA\right) \times 0.05\,\Omega + \left(10.6\,V - 10\,V\right) \times \left(-0.1\,mV / V\right) - 10.5\,mV$$

$$V_{REF} = 2.4899\,V$$

$$R_1 = \frac{\left(10\,V - 2.4899\,V\right)}{2\,\mu A}$$

$$R_1 = 3.755\,M\Omega$$

$$R_2 = \frac{2.4899\,V}{\left(2\,\mu A - 30\,nA\right)}$$

$$R_2 = 1.264\,M\Omega$$

The closest standard 1% resistor value for R_1 is 3.74 kΩ. A value of 1.3 MΩ is chosen for R_2 to achieve the V_{KA} narrow supply range 10 V ±2% to 3%.

To calculate R_3, it is necessary to know the base current of the NPN transistor. Use the maximum required emitter current of 300 μA to sufficiently supply the 10-V load and 3.3-V supply and load current.

$$I_B = \frac{I_C}{h_{FE}} \quad (6)$$

$$I_B = \frac{300\,\mu A}{400}$$

$$I_B = 750\,nA$$

Use the maximum required base current, the minimum UVLO voltage of 18 V, the maximum cathode voltage, and the maximum value for the minimum cathode current of 35 μA to calculate the resistance R_3.

$$R_3 = \frac{\left(V_{DC} - V_{KA}\right)}{\left(I_{KA} + I_B\right)} \quad (7)$$

$$R_3 = \frac{\left(18\,V - 10.7\,V\right)}{\left(35\,\mu A + 750\,nA\right)}$$

$$R_3 = 204.196\,k\Omega$$

The closest standard 1% resistor value for R_3 is 205 kΩ.

4.2.2.2 3.3-V Power Supply

The 3.3-V supply uses the same low I_Q adjustable precision shunt regulator, ATL431, as the 10-V supply. Along with the regulator are three resistors with the DC supply voltage of 10 V. One of the resistors, R_3, provides the cathode current, I_{KA}, and the other two creates a resistive divider to set the output voltage, V_{KA}.

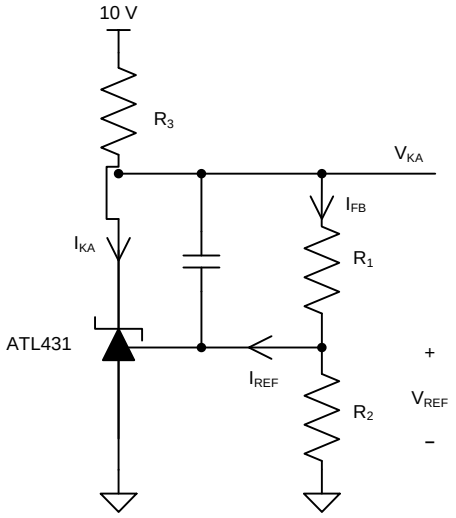

Figure 14. Schematic of 3.3-V Supply

For the 3.3-V supply, the parameters for $V_{KA} \leq 10$ V are used for Equation 8.

$$V_{REF} = V_{NOM} + \left(I_{KA} - I_{NOM}\right) \times Z_{KA} + \left(V_{KA} - V_{NOM}\right) \times \frac{\Delta V_{REF}}{\Delta V_{KA}} \tag{8}$$

Now that V_{REF} is solved, determine R_1 and R_2.

$$R_1 = \frac{\left(V_{KA} - V_{REF}\right)}{I_{FB}} \tag{9}$$

$$R_2 = \frac{V_{REF}}{\left(I_{FB} - I_{REF}\right)} \tag{10}$$

NOTE: R_2 has less current than R_1

The design goal is to set the cathode of the ATL431 to 3.3 V by providing a minimum cathode current of 20 µA, and a feedback current and resistor divider that will keep V_{KA} within a narrow supply range of ±2%. The following parameters are calculated using the formula derived in the general example for $V_{KA} < 10$ V.

$$V_{REF} = 2.500\ \text{V} + \left(20\ \mu\text{A} - 1\ \text{mA}\right) \times 0.05\ \Omega + \left(3.3\ \text{V} - 2.500\ \text{V}\right) \times \left(-0.4\ \text{mV/V}\right)$$

$$V_{REF} = 2.4996\ \text{V}$$

$$R_1 = \frac{\left(3.3\ \text{V} - 2.4996\ \text{V}\right)}{1\ \mu\text{A}}$$

$$R_1 = 800.369\ \text{k}\Omega$$

$$R_2 = \frac{2.4996\ \text{V}}{\left(1\ \mu\text{A} - 30\ \text{nA}\right)}$$

$$R_2 = 2.577\ \text{M}\Omega$$

The closest standard 1% resistor value for R_1 is 806 kΩ. A value of 2.8 MΩ is chosen for R_2 to achieve the V_{KA} narrow supply range 3.3 V ± 2%.

With the standard resistor values for R_1 and R_2, the estimated V_{KA} and I_{FB} can be calculated to determine the value of R_3. Use the maximum parameters in the ATL431 datasheet (SLVSCV5) to calculate the resistance.

$$V_{REF} = V_{NOM} + \left(I_{KA} - I_{NOM}\right) \times Z_{KA} + \left(V_{KA} - V_{NOM}\right) \times \frac{\Delta V_{REF}}{\Delta V_{KA}} \tag{11}$$

$$V_{REF} = 2.500\ V + \left(35\ \mu A - 1\ mA\right) \times 0.3\ \Omega + \left(3.3\ V - 2.500\ V\right) \times \left(-2.7\ mV / V\right)$$

$$V_{REF} = 2.523\ V$$

$$V_{KA} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) + I_{REF} \times R_1 \tag{12}$$

$$V_{KA} = 2.523\ V \times \left(1 + \frac{806\ k\Omega}{2.8\ M\Omega}\right) + 150\ nA \times 806\ k\Omega$$

$$V_{KA} = 3.370\ V$$

$$I_{FB} = \frac{\left(V_{KA} - V_{REF}\right)}{R_1} \tag{13}$$

$$I_{FB} = \frac{\left(3.370\ V - 5.523\right)}{806\ k\Omega}$$

$$I_{FB} = 1.051\ \mu A$$

$$R_3 = \frac{\left(V_{15V} - V_{KA}\right)}{\left(I_{LOAD} + I_{KA} + I_{FB}\right)} \tag{14}$$

$$R_3 = \frac{\left(10\ V - 3.370\ V\right)}{\left(30\ \mu A + 35\ \mu A + 1.051\ \mu A\right)}$$

$$R_3 = 100.382\ \Omega$$

The closest standard 1% resistor value for R_3 is 100 kΩ.

For stability reasons, ceramic capacitors are placed in the feedback loop of each regulator, between the cathode and reference nodes. The capacitors introduce a zero to each system, and when properly placed will increase the phase margin of each regulator as to avoid oscillation and decrease ringing on the output voltages.

4.3 MOSFET Selection

Low-cost thermostats can be connected up to two separate 24-V_{AC} connections. If both loads are 180 degrees out of phase from each other, then that is a maximum peak DC voltage of 84 V. A standard 24-V_{AC} power relay with a current rating of 40 A has a coil resistance of 660 Ω. The 120- to 24-V_{AC} transformer output voltage can range from 20- to 30-V_{AC}. Therefore, each MOSFET must be able to handle a drain-to-source voltage and current of 84 V_{DC} and 0.12 A, respectively. The CSD19537-Q3 was chosen for its 100-V drain-to-source voltage and package size/cost.

When an SSR is used to turn on and off the inductive load, take care to limit overvoltage spikes during the turnoff process. The capacitor and external rectification diodes create a snubber circuit to absorb the energy from inductive load during turn off. When the switch is turned off, the current from the inductive load is interrupted and causing the voltage to spike. For additional precaution, a transient voltage suppression (TVS) diode is added across the MOSFETs. For the DC application unidirectional TVS is sufficient, where for AC application a bidirectional TVS is needed.

4.4 UVLO Design Theory

During the time that the relay is not active, the rectification circuit capacitor charges. When the relay is active, the voltage across the MOSFETs reduces down to zero, causing the rectification capacitor to start to discharge, as shown in Figure 15 and Figure 16. If the DC source voltage becomes too low, the two ATL431 shunt regulators will not regulate and the SSR will no longer be able to function. An UVLO circuit is included in this reference design to turn off the MOSFETs and allow the capacitor to recharge.

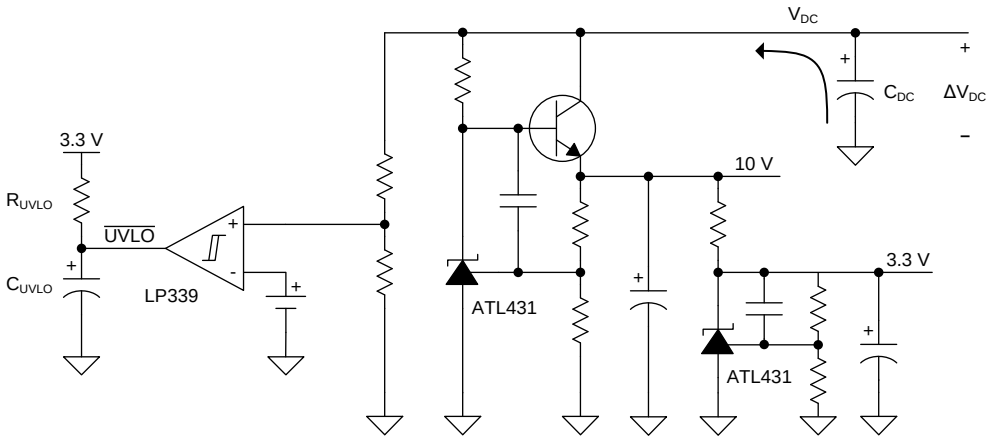

Figure 15. Mode of DC Supply When MOSFETs are ON

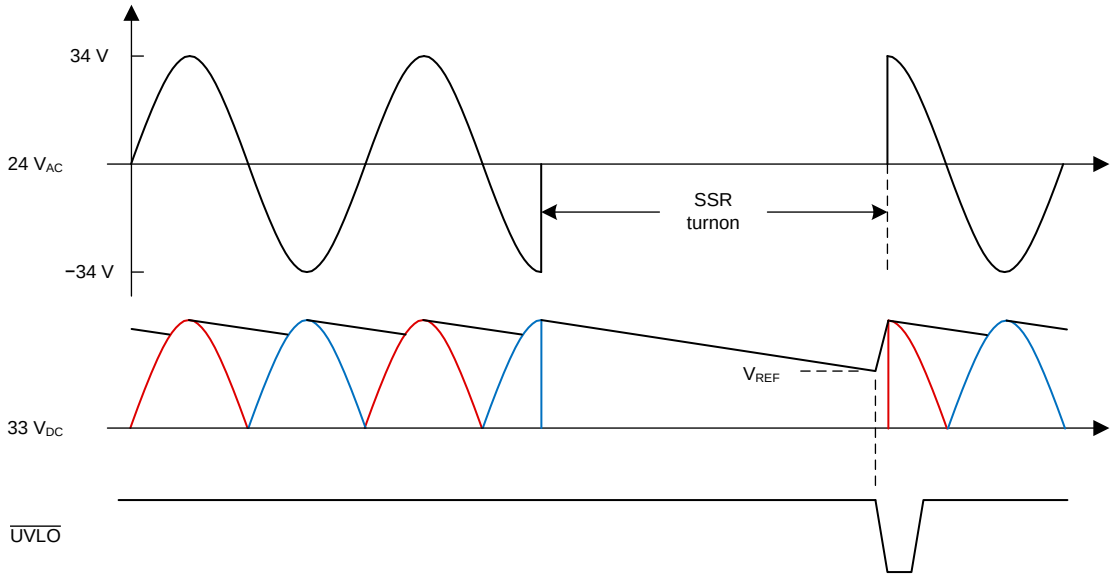

Figure 16. Resulting Waveforms for DC Supply and UVLO When SSR Cycles ON and OFF

A minimum voltage of 18 V is chosen to maintain the DC source voltage above the ATL431 cathode voltage. When the DC source voltage goes below 18 V, the LP339 will output a logic low, which will be sent to the logic control to turn off the MOSFET. The duration of the low output is determined by the time constant for the RC network at the output of the UVLO comparator and allows enough time for the capacitor to charge up to enough voltage to where the DC supply capacitor can discharge over approximately 6 cycles (that is, ΔV_{PP} = 6 V). To calculate the required delay time, use the peak current provided from the HVAC load (typically the current through HVAC relay), the DC supply capacitor value calculated in Section 4.2.1, and the desired peak voltage for Equation 15:

$$\Delta t_{UVLO\_DELAY} = \frac{C_{DC} \times \Delta V_{DC}}{i_S} \quad (15)$$

To calculate values of the RC network, use the delay time result in Equation 16.

$$\tau = R_{UVLO} \times C_{UVLO} \quad (16)$$

$$V_{REF} = V_{UVLO}(t) = 10\ V \times \left(1 - e^{-\frac{t}{\tau}}\right) \quad (17)$$

4.5 OCP Design Theory

The OCP circuit uses a current sensing method by means of voltage level detection on the drain of the MOSFETs, as shown in Figure 17. When the MOSFETs are on and the drain voltage is low, the diodes at HV1 and HV2 will conduct, pulling current through the pullup resistors at the input of the LP339 comparators. As the current through the MOSFET increases, the voltage at the input of the comparators will increase. Setting the reference voltage of each LP339 comparator determines the maximum level of excess MOSFET current at each HV line. The excess current could be due to a malfunctioning MOSFET or other component, or there could be a short circuit.

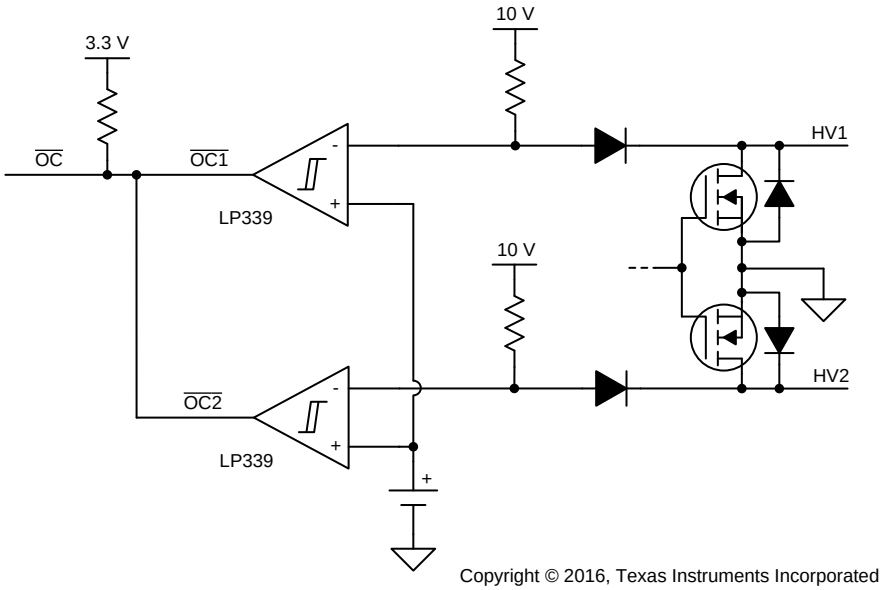

Figure 17. Simplified Schematic of OCP

When the MOSFETs are off, the HV lines will see the 24-V_{AC} power supply, as shown in Figure 18. Due to the comparator voltage reference level, there will be times when one comparator output is high while the other is low and vice versa. There will also be times when both comparator outputs are high. This will cause pulsing at the OCP output that would normally be used to turn off the MOSFETs. Since they are already off in this case, this will have no effect on the system.

In a similar case when the SSR is actively controlling the HVAC load, the OCP will output a low during the charging time of the DC supply capacitor and a high during the discharging time. The low time is because the HV lines will see the AC load voltage which is charging the supply capacitor and above the reference voltage. The high time is because the MOSFETs are on and the voltages at the HV lines are below the reference voltage. This function is accounted for in the logic control block of the SSR by means of diode, D7, and capacitor, C5, as to not falsely reset the output of the flip-flip.

The basic functionality of the OCP provides that the output of the comparators will remain high as long as the voltages at the negative input terminals of the comparators remain below the reference voltage. When the input voltage rises above the reference voltage the output will go low. By connecting the output terminals of the comparators together, as they are open collector, the output levels will be treated in a logic AND function. If either of the outputs is low, the final output will be low.

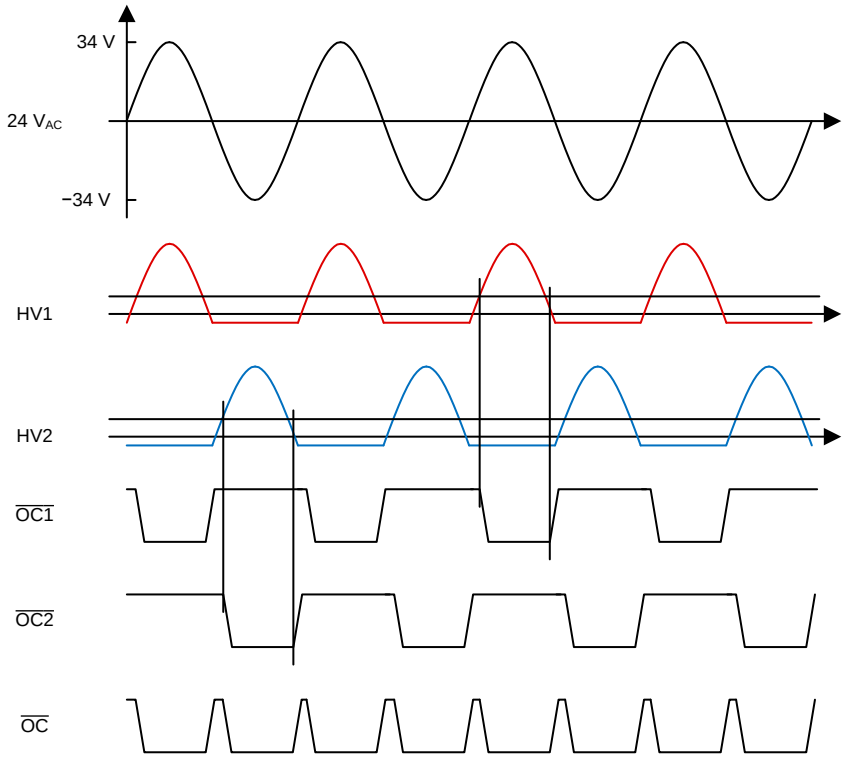

Figure 18. Resulting Output Waveforms of OCP When MOSFETs are Off

4.6 Control Logic Design Theory

The control logic circuitry uses short, LOW logic level pulses at the inputs of the D-type flip-flop, SN74AUP1G74, to turn on and off the MOSFETs. See Table 3 for the logic levels on output Q in reference to the input levels of PRE and CLR. Output Q is sent to the AND gate, SN74AUP2G08, along with the output of the UVLO, as shown in Figure 19. The result of the AND gate output, EN, is used for two different functions. The first function is turn on and off the MOSFETs and the second is to control the use of the OCP signal.

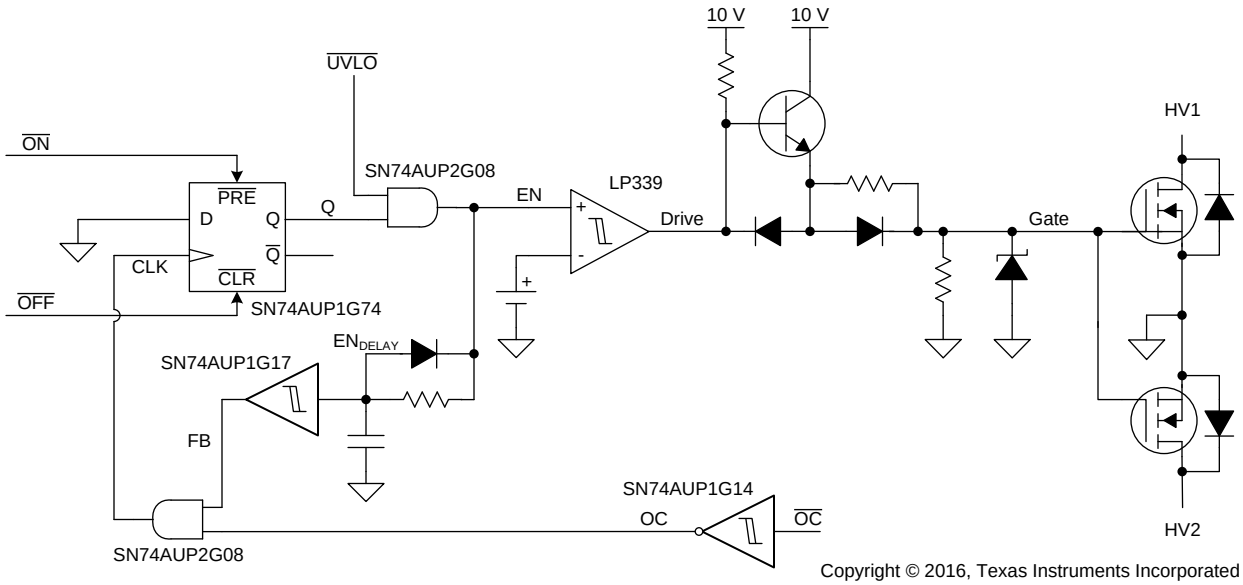

Figure 19. Control Logic and Gate Driver Schematic

The first function of EN is to drive the gates of the MOSFETs through the comparator. For fast turnon time of the MOSFETs, a sufficient amount of current must be available to charge the gate-to-source capacitance, C_{GS}, as shown in Figure 20. When EN is high, the open collector output of the comparator is also high and the gate is driven from the common collector circuit. This configuration amplifies the current provided by R_{CB} at the base at the NPN transistor to provide the necessary current to C_{GS}. During this process, D_{ON} conducts, shorting R_{OFF} as not additionally to limit the current to the gates of the MOSFETs.

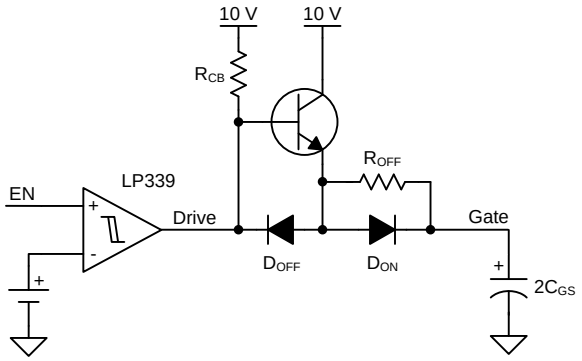

Figure 20. Gate Driver Schematic With Gate-to-Source Capacitance of MOSFETs

For fast turnoff time of the MOSFETs, a sufficient discharge path must be provided for C_{GS}. When EN goes low, the output of the comparator is pulled down to ground, sinking current. The diode at the gates, D_{ON}, is reversed biased allowing R_{OFF} to control the current discharging of C_{GS}, and turnoff time of the MOSFETs. To protect the base-emitter junction of the transistor from overvoltage, an additional diode is used to limit the VEB voltage to the forward voltage of the diode, D_{OFF}.

The second function of EN is to control the use of the OCP. As previously stated, when the SSR is active and the switch is cycling through on and off, the pulse at the output of the OCP must not falsely reset the output of the flip-flop. When OC, the inverted output of the OCP, and EN are both a logic level HIGH, the active rising edge CLK input of the flip-flop resets output Q, turning off the switch. To prevent this at turnon, an RC network is connected at EN, as shown in Figure 19, adding a delay to the low-to-high level transition of EN_{DELAY}, as shown in Figure 21.

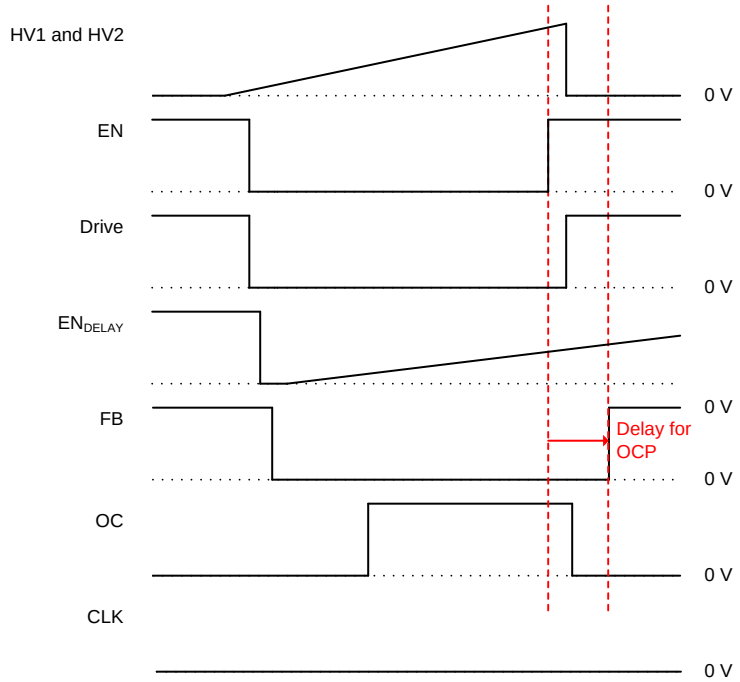

Figure 21. Delay Results for OCP Functionality

During the charging time of the DC supply capacitor, the UVLO outputs a low to turn off the MOSFETs. At the time the MOSFETs turnoff, the HV lines at the input of the OCP goes high and outputs high pulses on OC to deactivate the flip-flop. The flip-flop needs to stay active during the ON time of the SSR, so it is important for FB to be low during this time. Due to the RC network at EN_{DELAY}, the voltage level when OC goes high is determined by the discharge time of the capacitor. To ensure fast discharge and not falsely deactivate the flip-flop, a diode is connected between EN_{DELAY} and EN, as shown in Figure 19.

For improved functionality and protection, a resistor and Zener diode can be connected to the gate of the MOSFETs. The resistor provides an additional discharge path for C_{GS}, ensuring a full discharge of the capacitance during the turn off of the MOSFETs. The Zener diode sets a peak voltage limit to the gate of the MOSFETs as to avoid overvoltage of the gate-source junction.

For the full logic sequence for the switch turnon and turnoff through the D-type flip-flop, see Figure 22.

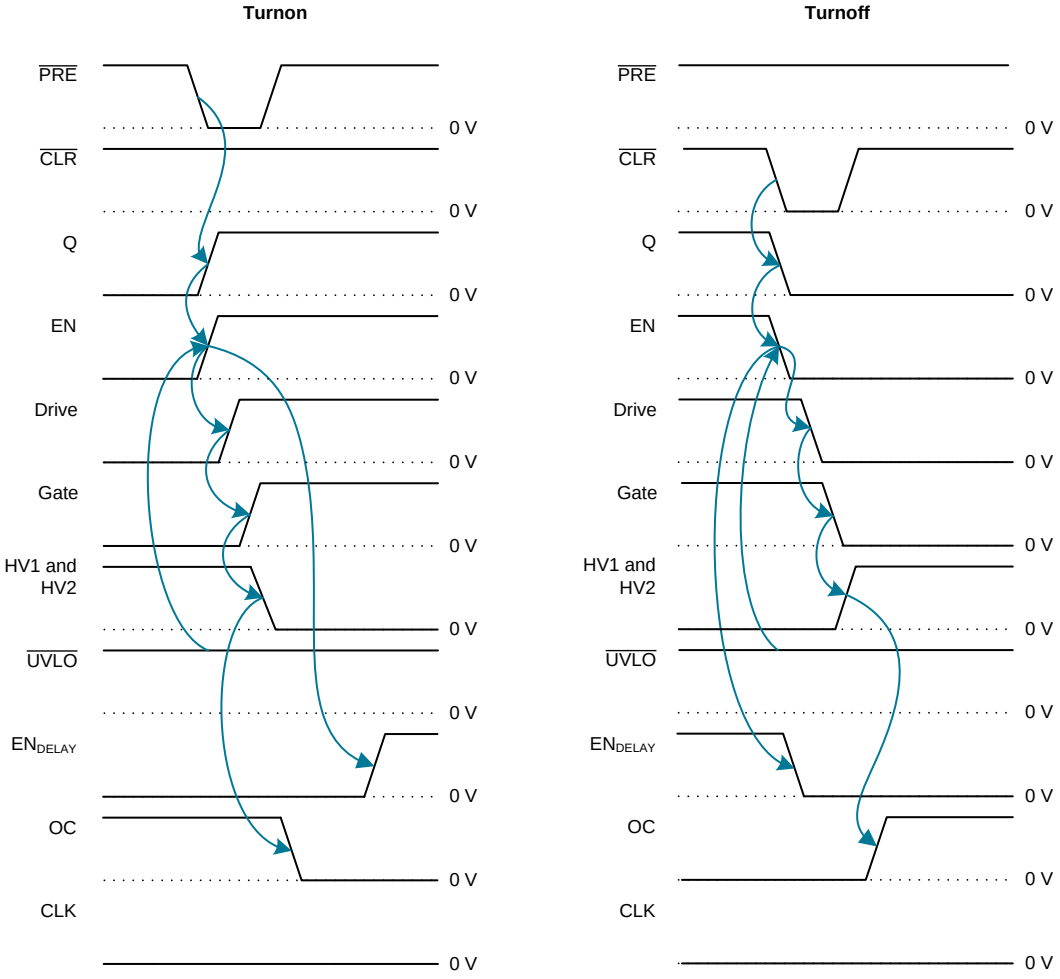

Figure 22. SSR Turnon and Turnoff Logic Sequence

5 Getting Started Hardware

5.1 Board Overview

For ease of use, all of the components, headers, and test points are located on the top side of the board, as shown in Figure 23. The signal chain starts on the left side of the board and moves to the right side of the board in a linear fashion. The input headers, J6 and J7, are located on the left edge of the board has connection points ON and OFF for active logic level LOW inputs of the D-type flip-flop. Moving to the right side of the board, a set of three headers connects the 3.3-V_{DC} supply (J4) and 10-V_{DC} supply (J3) rails to the corresponding loads and the rectified AC load voltage to the UVLO (J1). The next header to the right (J2) connects the rectified AC load voltage to the DC power supply. To the right are two headers (J9 and J8) that connect the 24-V_{AC} HVAC load to the OCP. The last header on the far right (J5) is the terminal block which connects the circuit to the 24-V_{AC} HVAC load. Black and yellow test points denote signal chain test points including three ground connections.

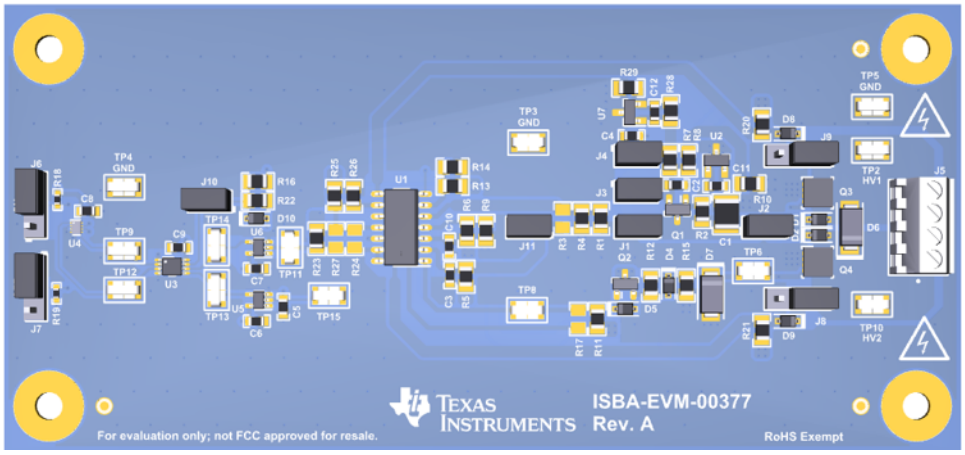

Figure 23. TIDA-00377 Reference Design Hardware

5.2 Operating the Circuit

Before powering the board, set the headers in the orientation described in Table 7. Connect the HVAC system load last to power the board.

Table 7. Header Connections at Startup

HEADER	CONNECTION
J1	Short
J2	Short
J3	Short
J4	Short
J5	24-V AC HVAC load
J6	Pin 2/3 shorted
J7	Pin 1/2 shorted
J8	Short to HV2
J9	Short to HV1

When the board is first powered on, the rectification diodes provide the voltage to the DC power supply, which enables the logic control and gate driver. The MOSFETs will not be active due to the short across pins 1 and 2 of J7. To turn on the MOSFETs, move the jumper from pins 1 and 2 on J7 to short pins 2 and 3. Next, provide a short, logic level LOW pulse to ON through pins 1 and 2 of J6. Since both inputs are active low and have pullup resistors, the pulse must pull down the signal to logic zero. The simplest way to do this is to short the pin to ground for a short period of time. The same method goes for the OFF signal, shorting the OFF pin to ground will turn on the MOSFETs.

6 Test Setup

Following the header orientation listed in Table 7, the circuit is tested using a White Rogers 120- to 24-V_{AC} 40-VA transformer, 90-T40F3, similar to what is used in HVAC systems. A 24-V light bulb is connected in series across terminal block J5 to provide 0.18 A, as shown in Figure 24. The initial testing procedure was to activate and deactivate the switch to see the light turn on and off. There was no flicker in the light, providing the initial results that the charging time of the DC supply capacitor was not too long. This also shows there were no short circuits or malfunctioning parts to cause the UVLO and OCP to activate and turn off the MOSFETs.

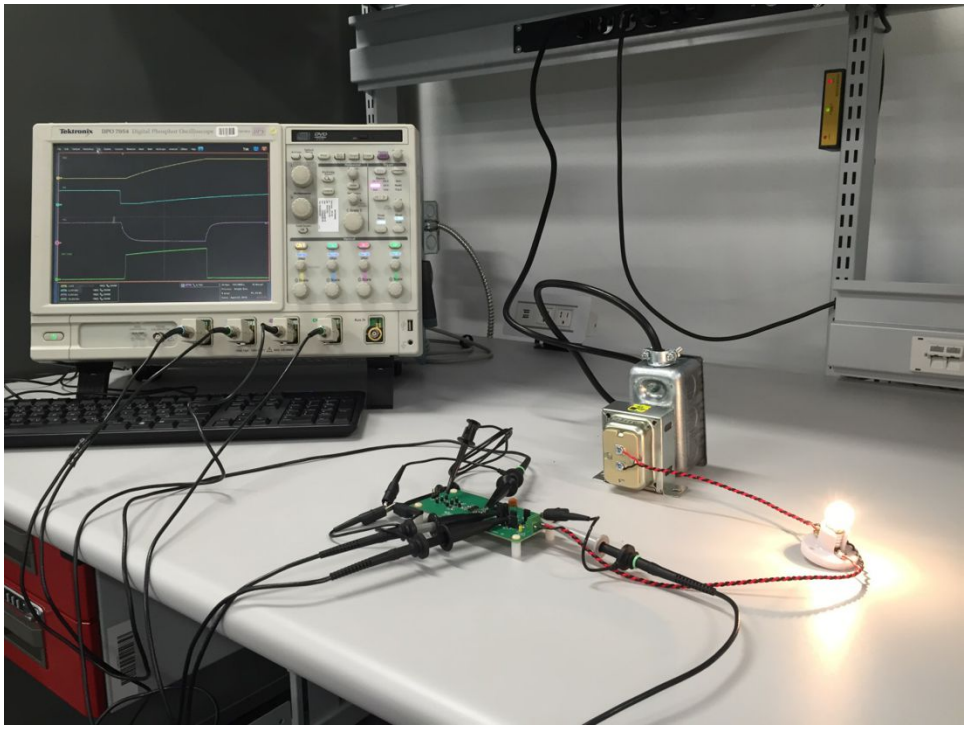

Figure 24. Test Setup of TIDA-00337 EVM, Light Bulb, and Transformer

To verify specific functionality of this reference design there are two necessary tests, which includes the current consumption from the 24-V_{AC} line and timing of the signal chain waveforms to validate the low self-powering and fast switching. The first test performed is the current consumption. These values were collected measuring the current flow through available headers using an ammeter during on and off states. The data was then verified by calculating the current through resistors by means of voltage measurements in addition to current rating of components from their datasheets.

The second test is to measure the timing of the control signals which includes four sets of signals. The first is charging time of the DC supply capacitor. This is seen by probing J1, TP1 (J11 on Rev E2), TP6, and HV1/HV2 as shown in Figure 25.

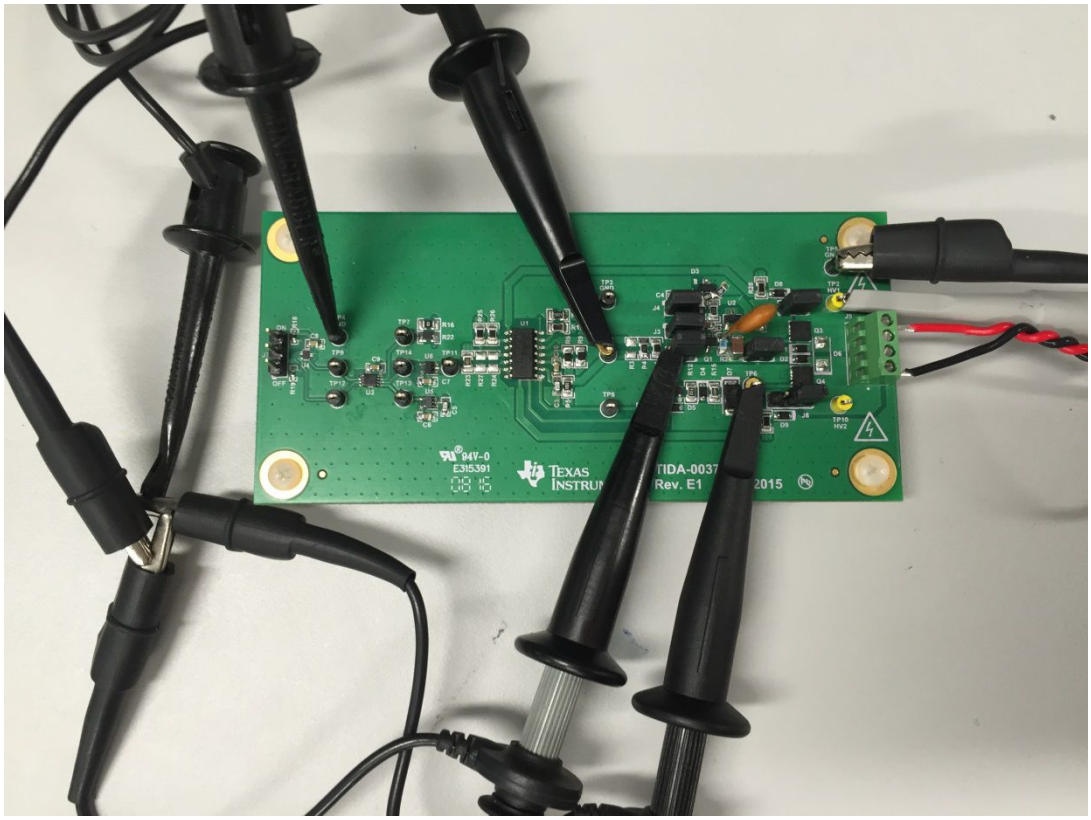

Figure 25. Probe Connections for Signal Chain Waveforms

The second and third signals are to check the turn on and off delay of the MOSFETs. The turnon and turnoff functionality has been verified visually by the lightbulb, but it is important to verify the speed of the switching as to efficiently charge the DC supply capacitor during active time. The waveforms captured are ON#, TP9, TP6, and HV1/HV2, which can be found in Figure 29 and Figure 30 in Section 7.

The fourth signal is to verify the integration of the over current protection. The sequence of waveforms captured is HV1/HV2, TP14, TP13, and TP12. Check that the delay time between the edges of TP13 and TP14 during switch turnon and turnoff is long enough to prevent the OCP from falsely deactivating the switch.

7 Test Data

The total steady-state current consumption for both on and off times are found in Table 8. The steady-state currents for each block of the SSR for both on and off times are shown in Figure 26 and Figure 27.

Table 8. Total Steady-State Current Consumption

STATE	CURRENT (µA)
ON time	242.36
OFF time	385.78

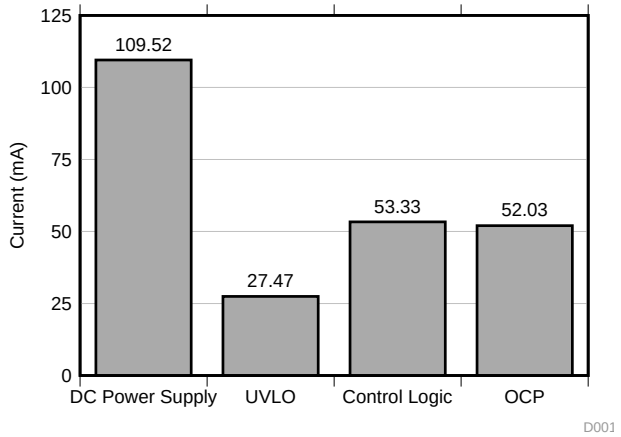

Figure 26. Steady-State Current Consumption During ON Time

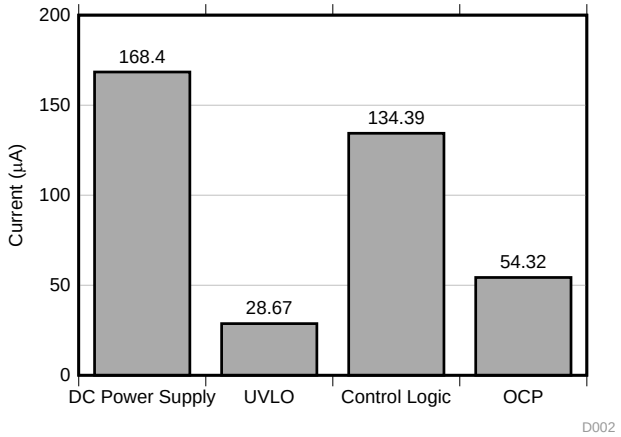

Figure 27. Steady-State Current Consumption During OFF Time

Figure 28 displays the charging time of the DC supply capacitor during the active time of the SSR. Active time of the SSR is when it is controlling the HVAC load and MOSFETs are on also cycling through on/off recharging the DC supply capacitor. The time between the rising and falling edge of the HV1 and HV2 waveform corresponds with the V_{DC} charging time of 80 µs, as shown in Figure 28. This also corresponds with the edges of TP1 (UVLO) and TP6 (V_{GS}) with the consideration of delay. TP1 (J11 on Rev E2) waveform exhibits the effects of the RC network at the output of the UVLO providing the delay time of the DC supply capacitor by crossing ~2 V, the V_{IH} of the AND gate, at the time V_{DC} stops charging.

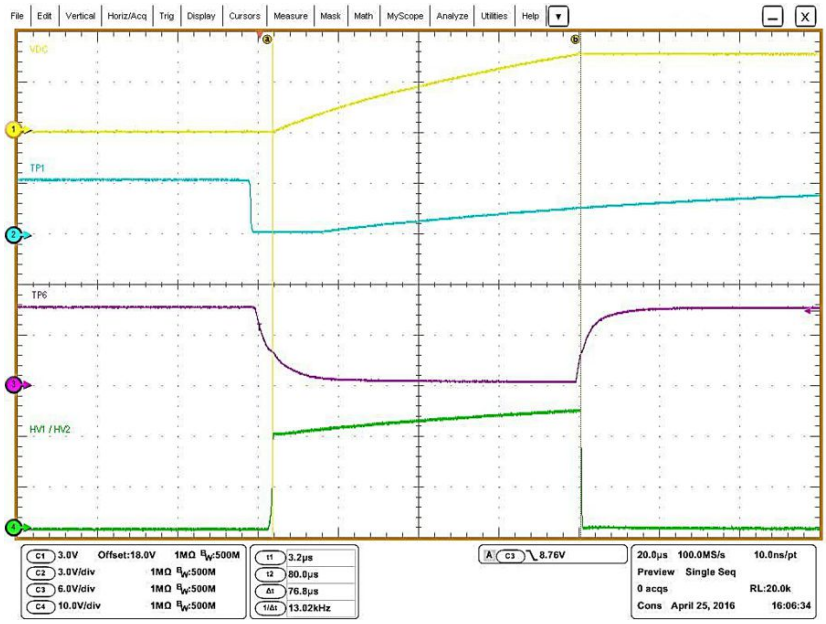

Figure 28. Charging Time of DC Supply Capacitor (Yellow) in Reference to TP1 (Blue), TP6 (Purple), and HV1/HV2 (Green)

Figure 29 shows the turnon delay time through input pulse to the D-type flip-flop. The falling edge of the ON# low pulse to the low transition of the voltage across the MOSFET is 2.76 µs. The turnon time of the MOSFETs (HV1/HV2 = V_{DS}) is 0.6 µs.

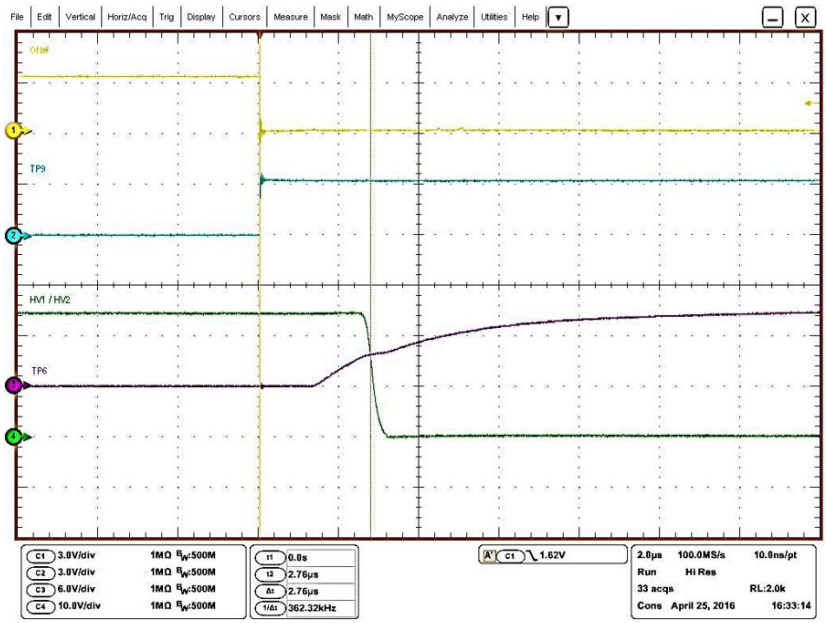

Figure 29. ON Delay Waveforms From Logic Enable Input (Yellow) to TP9 (Blue), TP6 (Purple), and Load of the MOSFETs (Green)

Figure 30 shows the turnoff delay time through input pulse to the D-type flip-flop. The delay time from the falling edge of the OFF# low pulse to the low transition of the voltage across the MOSFETs is 5.6 μs. The turnoff time of the MOSFETs (HV1/HV2 = V_{DS}) is 1.6 μs.

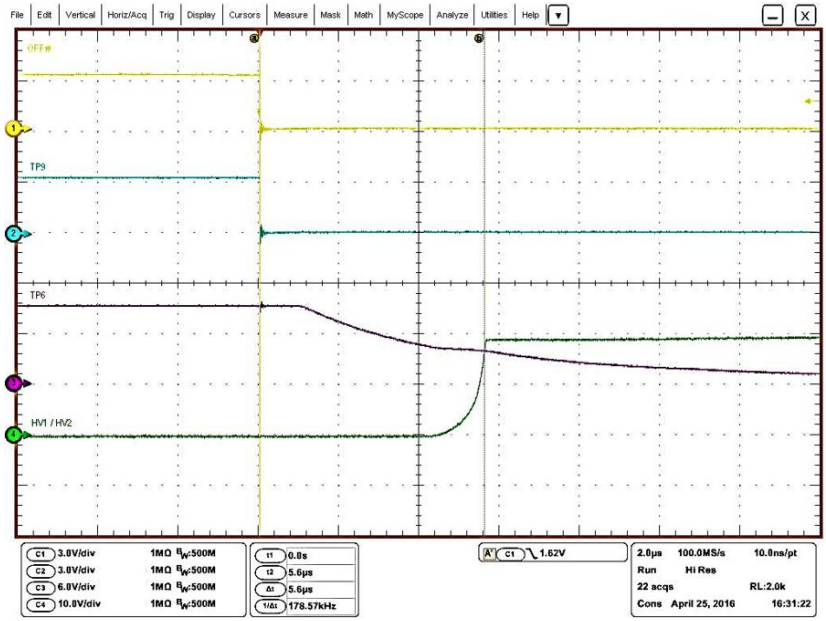

Figure 30. OFF Delay Waveforms From Logic Disable Input (Yellow) to TP9 (Blue), TP6 (Purple), and Load of the MOSFETs (Green)

Figure 31 displays the integration of the OCP with the UVLO and flip-flop signals. The waveforms included are HV1/HV2, the delayed flip-flop output of TP13, OCP output of TP14, and the CLK input of TP12. When HV1/HV2 (yellow) increases above 5 V (or vice versa), TP14 provides a pulse that is within the low time of TP13, successfully not sending a high pulse to the CLK input of the flip-flop through TP12. This proves the capacitor value is sufficient and the diode provides enough discharge time. There is a margin of 100 μs that can be adjusted to be smaller.

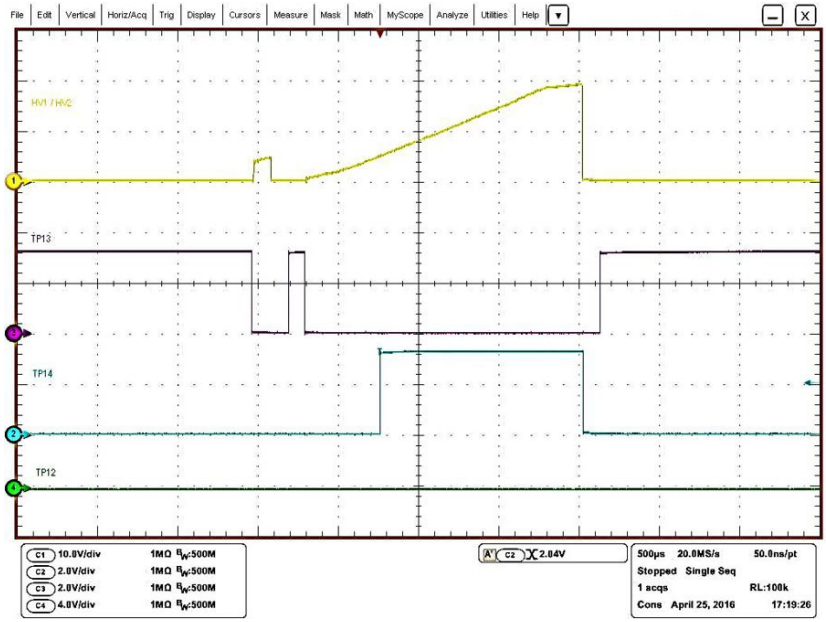

Figure 31. OCP Waveform During Charging Time in Reference to HV1/HV2 (Yellow), TP13 (Purple), TP14 (Blue), and TP12 (Green)

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00377.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00377.

8.3 PCB Layout Recommendations

A careful PCB layout is critical and extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. As with all switching power supplies, pay attention to detail in the layout to save time in troubleshooting later on.

8.4 Layout Prints

To download the layout prints, see the design files at TIDA-00377.

8.5 Altium Project

To download the Altium project files, see the design files at TIDA-00377 .

8.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00377.

8.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00377.

9 References

1. Texas Instruments, *Designing with the "Advanced" TL431, ATL431*, Application Report (SLVA685)
2. Texas Instruments, *Setting the Shunt Voltage on an Adjustable Shunt Regulator*, Application Report (SLVA445)
3. Texas Instruments, *Compensation Design with TL431 for UCC28600*, TL431 Application Report (SLUA671)
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10 About the Author

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