TI Designs
1-GHz Signal Bandwidth RF Sampling Receiver Solution

TI Designs

The RF sampling architecture offers an alternative to the traditional super-heterodyne architecture. RF sampling analog-to-digital converter (ADC) operates at a high sampling rate and converts signals directly from radio frequencies (RF) to digital. The ADC32RF45 ADC is an RF sampling converter used in telecommunication applications. The device is a dual, 14-bit resolution ADC that samples at 3 GSPS. Because of the high sampling rate, the device supports signal bandwidths that are 1 GHz and larger (up to 1.5 GHz at max sampling rate). Further, the device's input bandwidth is 3 GHz, which supports high bandwidth signals in either the first or second Nyquist zone. High sampling is not enough. For telecommunication applications, the dynamic range of the device is critical. This design showcases the ADC32RF45 operating in bypass mode to support a 1-GHz signal bandwidth with the LMX2582 clocking solution to achieve the best signal-to-noise (SNR) performance.

Design Resources

TIDA-01161	Design Folder
ADC32RF45EVM	Tools Folder
ADC32RF45	Product Folder
LMX2582	Product Folder
LMK04828	Product Folder

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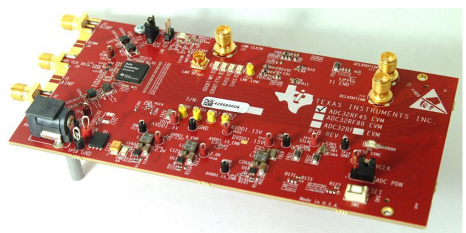
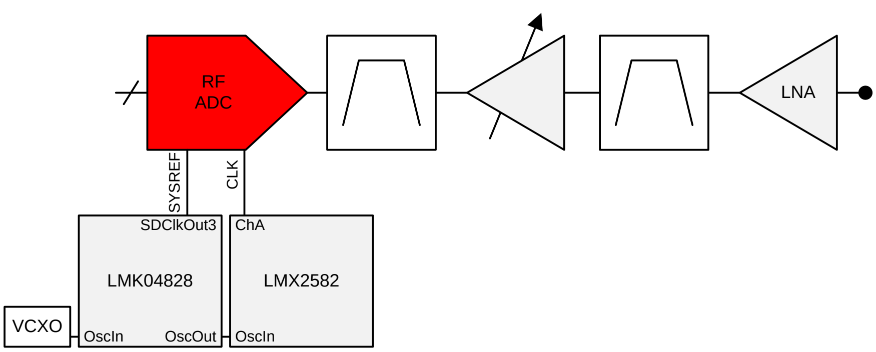
Design Features

- 3-GSPS RF Sampling ADC Solution
- 1 GHz and Larger Signal Bandwidth Capability
- Low-Noise, High Dynamic Range RF Sampling Receiver Solution
- Low-Phase Noise Clocking Solution for RF Sampling ADC

Featured Applications

- Wireless Base Station Multi-band or Multi-mode Receiver
- Digital Pre-Distortion Feedback Receiver
- Radar
- Large Antenna Arrays
- Cable Infrastructure
- Microwave and Millimeter-Wave Receivers
- Communication Test Equipment





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1 ADC32RF45 Reference Design

The ADC32RF45 EVM provides a variety of options for clocking ADC. This design focuses on the LMX2582 RF synthesizer as the input clock source. The LMX2582 operates up to (and beyond) 3 GHz and achieves very low clock jitter that rivals external test equipment. This device is preferred for the clock source of the RF ADC in order to present the lowest noise floor needed for wideband signals. The ADC32RF45 is clocked at 2949.12 MHz (768 × 3.84 MHz). The clock is generated directly from the LMX2582. The LMK04828 clock jitter cleaner supplies the reference frequency to the LMX2582 and the SYSREF low frequency clock to the ADC32RF45 needed to properly operate the JESD204B SERDES.

2 ADC32RF45 EVM Setup

2.1 Test Configuration

The ADC32RF45 EVM is connected to the TSW14J56 EVM capture card as seen in Figure 1. The TSW14J56 interfaces with the HSDC Pro GUI to analyze the captured patterns.

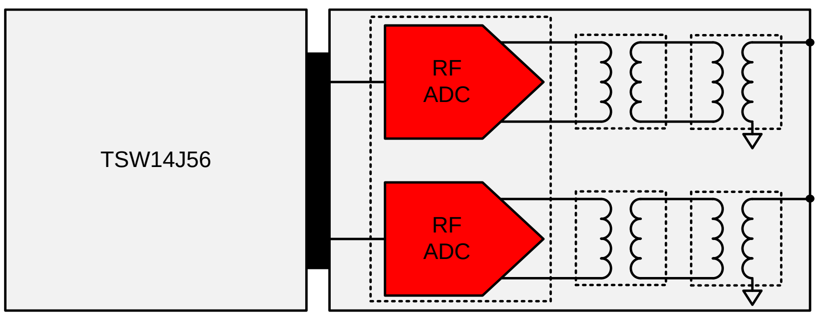

Figure 1. ADC32RF45 EVM Test Setup

2.2 LMX2582 Programming

The LMX2582 programming tab is shown in Figure 2. The LMX2582 is programmed to 2949.12 MHz. The reference frequency is 122.88 MHz, which is passed through from the LMK04828. The EVM has a hardware jumper to set the RF switch to the internal clock, which properly routes the LMX output to the ADC clock input. Ensure the clock signal is present before programming registers of the ADC.

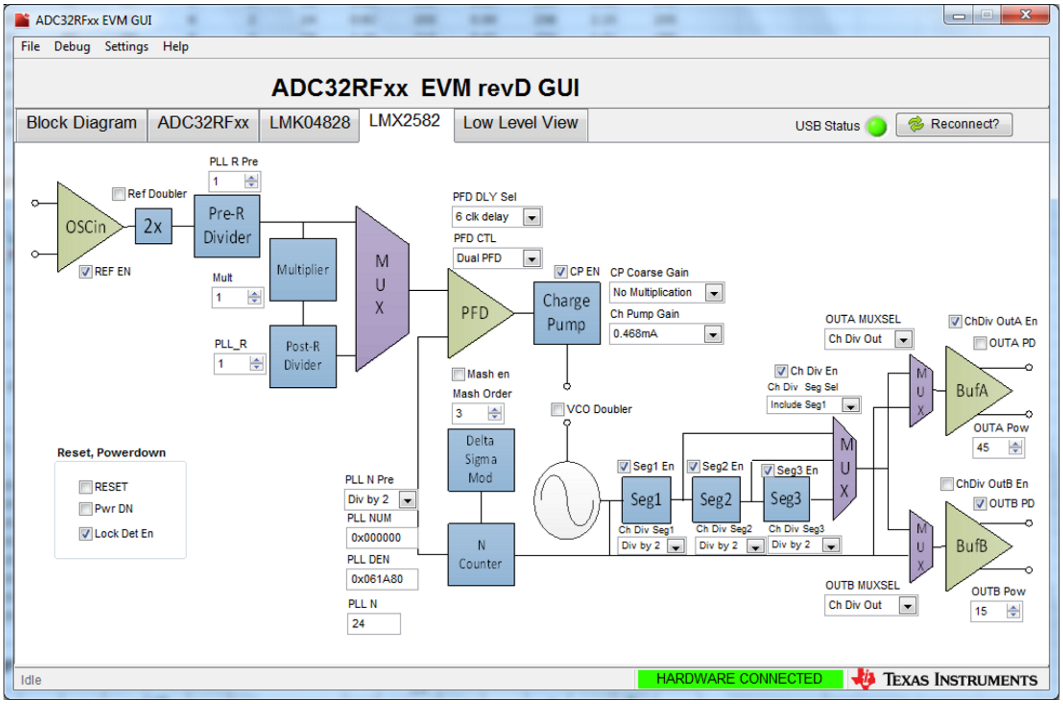

Figure 2. LMX2582 Programming Tab

2.3 ADC32RF45 Programming

The ADC32RF45 EVM is put into bypass mode to use the full Nyquist zone of the device. The device is set up using 5-sample mode with a JESD lane configuration corresponding to 82820. Follow the ADC32RF45 EVM user's guide (SLAU620) to load the configuration file "ADC32RF45_5sample_lmfs82820" once the clock signal is established.

3 Block Diagram

The block diagram of the receiver solution including the clocking solution is shown in Figure 3. The complete solution includes the front-end low-noise amplifier (LNA) and appropriate channel filtering along with an RF variable gain amplifier to maintain an optimum dynamic range to the ADC.

The clocking solution circuit for the ADC32RF45 is shown in Figure 4. It is critical to maintain a low-phase noise or low-jitter clock solution to maintain the low-noise floor needed for wideband captures. The LMK04828 provides the low-frequency SYSREF signal needed for the JESD204B SERDES interface. The LMK04828 also provides the reference frequency for the LMX2582. The LMX2582 is a wide tuning range synthesizer with very low-phase noise. The LMX2582 provides the clock frequency up to 3 GHz. Clock amplitude level is also important, so keep the interface between the LMX2582 and the ADC32RF45 to as low of a loss as possible.

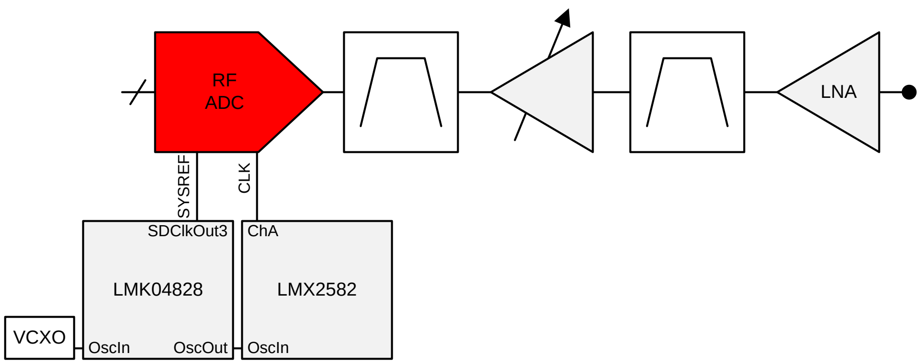

Figure 3. Receiver Solution Block Diagram

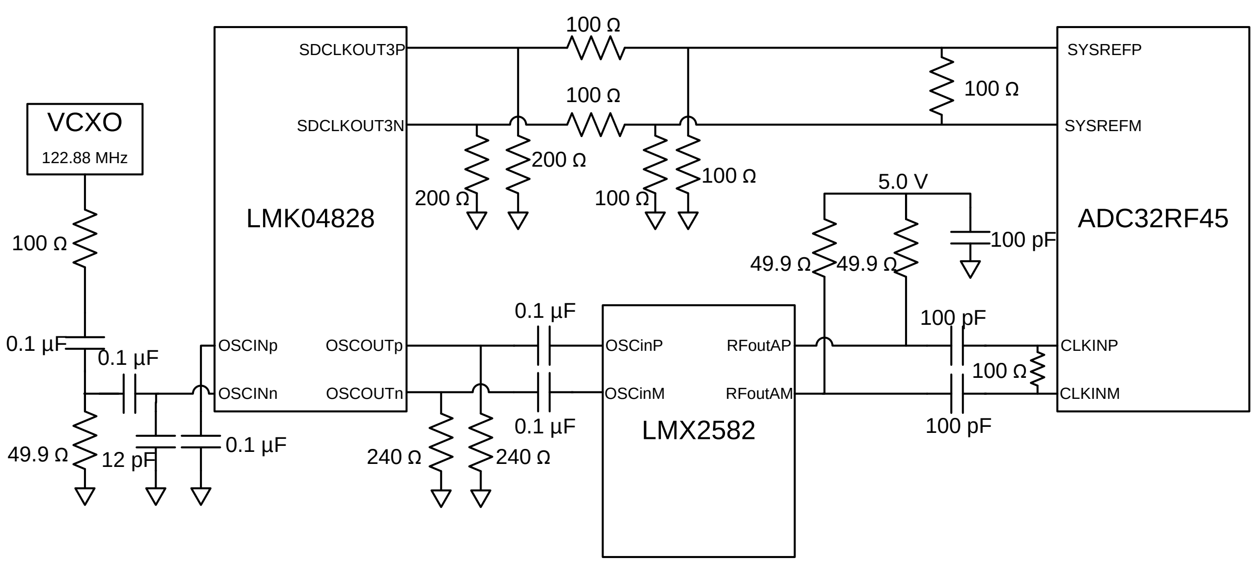

Figure 4. Clocking Circuit Solution for ADC32RF45

4 Measured Performance

The input signal to the ADC has a total bandwidth of 1 GHz. The signal includes four groups, each with a 200-MHz bandwidth. The four groups are separated by approximately 65 MHz so that the edge-to-edge bandwidth is 1 GHz. Each group is a combination of ten 20-MHz wide LTE carriers. This signal represents a high multi-carrier scenario or multi-band scenario that would be used for next generation telecommunication systems. Overall, there are 40 20-MHz LTE carriers in the entire signal. The signal is centered at 2.2 GHz so that it falls in the middle of the second Nyquist zone. Figure 5 shows the captured results of the 1-GHz wide signal. The power within the entire bandwidth is approximately –30 dBFS. Note the noise floor is less than –100 dBFS in this scenario, which is limited by the input noise from the signal.

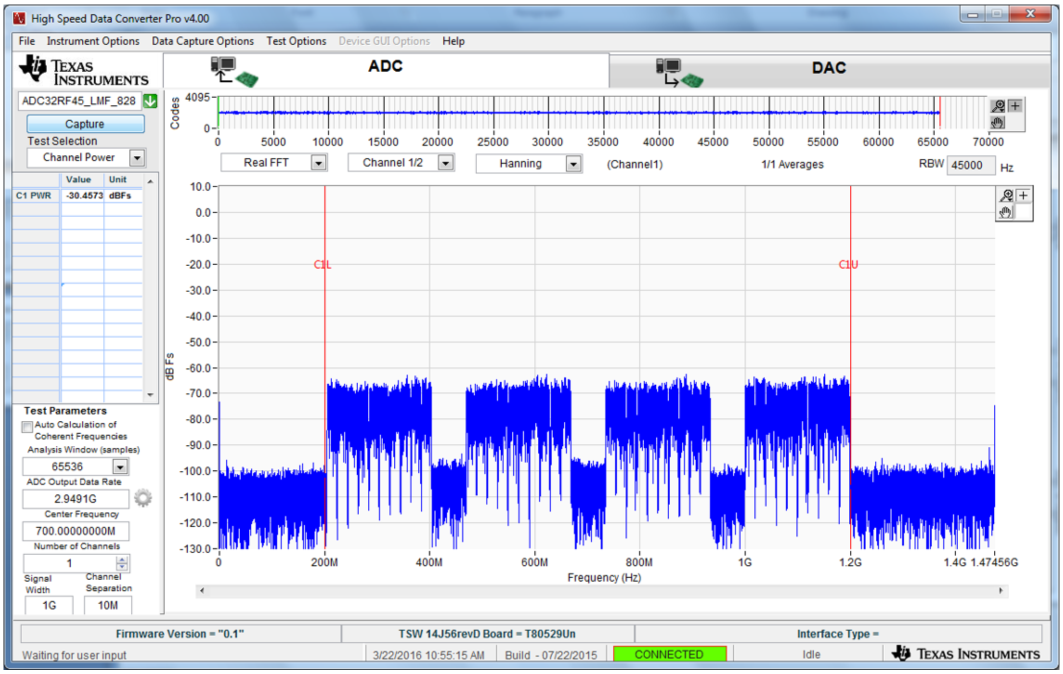

Figure 5. ADC32RF45 Capture With 1-GHz Signal Bandwidth

5 Conclusion

The ADC32RF45 is the key device in an RF sampling receiver for large signal bandwidths. The device facilitates capturing 1-GHz signal bandwidths and larger needed for multi-mode applications and next generation telecommunication standards like 5G. The device is also well suited for digital pre-distortion (DPD) applications where the expansion bandwidth is up to five times higher than the signal bandwidth.

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-01161.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01161.

6.3 PCB Design Files

To download the PCB design files, see the design files at TIDA-01161.

7 Software Files

To download the software files, see the design files at TIDA-01161.

8 About the Author

RUSSELL J. HOPPENSTEIN is the HSP-WI Application Manager at Texas Instruments. He is responsible for high-speed data converters, discrete RF devices, and integrated transceivers. Russell earned his master of science in electrical engineering (MSEE) from the University of Texas at Arlington and his bachelor of science in electrical engineering (BSEE) from the University of Texas at Austin.

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