TI Designs

1-kW, Compact, 97.5% Efficiency, Digital PFC for AC/DC PSUs With eMeter Reference Design

TI Designs

The TIDA-00707 is a 1-kW, compact (100-mm×80-mm) power factor correction (PFC) circuit designed for telecom, server, and industrial power supplies. This reference design is a continuous conduction mode (CCM) boost converter, implemented using a UCD3138A Digital Power Supply controller with all protections built-in. Hardware is designed and tested to pass conducted emissions, surge, and EFT (as per EN55014) requirements.

Key highlights of this reference design:

- Provides a ready platform of front-end PFC to address various power supplies up to 1 kW
- Improves overall system performance with lower bus ripple, lower bus capacitance, lower RMS currents, and front-end protections
- Meets stringent current THD and power factor norms
- Protects for output overcurrent, overvoltage, and undervoltage conditions

Design Resources

TIDA-00707	Design Folder
UCD3138A	Product Folder
UCC28881	Product Folder
UCC27517A	Product Folder
TLV704	Product Folder
OPA2376	Product Folder
ISO7321C	Product Folder

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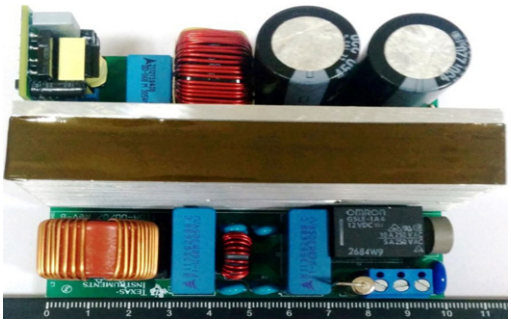
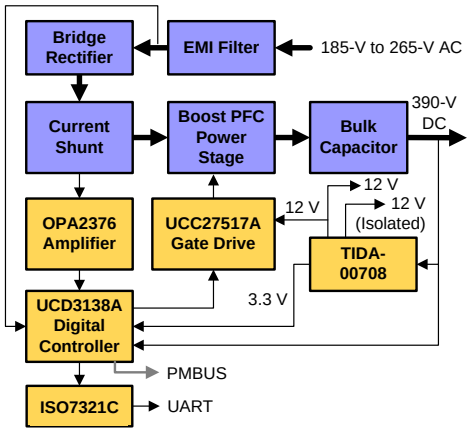


Design Features

- Wide Operating Input Range: 195-V to 270-V AC
- Designed to Drive Wide Range of Downstream DC/DC Converters and Inverter-Fed Motors up to 1 kW
- High Power Factor > 0.99 and < 5% THD From Medium-to-Full Load (50% to 100%); Meets Current THD Regulations as per IEC 61000-3-2
- High Efficiency of > 97% at Full Load Over Entire Operating Voltage Range
- No Need for External Cooling up to 55°C Ambient Operation for Loads ≤ 900 W
- Communicates Input Power Consumption Information of the Unit Precisely for all Load Conditions
- Built-in 12-V/3-W Supply for Housekeeping Power Needs
- PMBUS and Isolated UART for Communication
- Meets the Requirements of Conducted Emissions Standard – EN55011 Class A, EFT Norm IEC6000-4-4, and Surge Norm IEC61000-4-5
- PFC Converter Designed With a Small PCB Form Factor (100 mm × 82 mm)

Featured Applications

- Telecom Rectifiers
- Server and Industrial Power Supplies
- Online UPS
- Power Storage Banks
- Motor Drives



1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage (V_{INAC})		195	230	270	VAC
Frequency (f_{LINE})		47	50	63	Hz
No load power (P_{NL})	V_{INAC} = 230 V, I_{OUT} = 0 A	—	2.2	—	W
OUTPUT CONDITIONS					
Output voltage		—	390	—	V
Output current		—	—	2.56	A
Line regulation		—	—	0.5	%
Load regulation		—	—	0.5	%
Output voltage ripple	Peak to peak	—	20	—	V
Output power (P_O)		—	1000	1000	W
SYSTEM CHARACTERISTICS					
Efficiency (η)	V_{IN} = V_{NOM} and full load	—	97	—	%
Protections	Output overcurrent	—	—	—	—
	Output overvoltage	—	—	—	—
	Output undervoltage	—	—	—	—
	Open-loop detection	—	—	—	—
Operating ambient	Open frame	–10	25	55	°C
Standards and norms	Power line harmonics	As per EN55011 / EN55022 Class A			
	Conducted emissions	As per IEC 61000-3-2 Class A			
	EFT	As per IEC-61000-4-4			
	Surge	As per IEC-61000-4-5			
Board form factor (FR4 material, 2 layers)	Length × Breadth × Height	100 × 80 × 40			mm

2 System Description

The power supplies for telecom, server, and industrial systems convert AC line power to isolated constant DC voltage of –48 V in telecom systems, 12 V in server systems, and 24 V in industrial systems. These high-power systems typically range from 1 to 5 kW. These power supplies need a front-end power factor correction circuit to shape the input current of the power supply and to meet the power factor and current THD norms such as IEC61000-2-3.

A power factor correction (PFC) circuit shapes the input current of the power supply to be in phase with the mains voltage and aids to maximize the real power drawn from the mains. In addition, a PFC front-end offers several benefits:

- *Reduces RMS input current*
  A power circuit with a 230-V/5-A rating is limited to about 575 W of available power with a PF of 0.5. Increasing the PF to 0.99 will double the deliverable power to 1138 W, allowing higher-power loads to be operated.
- *Facilitates power supply holdup*
  The active PFC circuit maintains a fixed intermediate DC bus voltage that is independent of the input voltage, so the energy stored in the system does not decrease as the input voltage decreases. This allows the use of smaller, less expensive bulk capacitors.
- *Improves efficiency of downstream converters*
  The PFC reduces the dynamic voltage range applied to the downstream inverters and converters, reducing voltage ratings of rectifiers results in lower forward drops, and increasing operating duty cycle results in lower current in switches.
- *Increases the efficiency of the power distribution system*
  A lower RMS current reduces distribution wiring losses.
- *Reduces the VA rating of standby power generators and stresses on neutral conductors*
  Reducing harmonics eliminates the risk of triplen harmonics (the third and multiples thereof) that can add up to dangerous levels in the neutral conductor of Y-connected 3-phase systems.

This reference design is a boost power factor converter implemented by using the UCD3138A as the PFC controller for telecom, sever, and industrial systems that demand a PFC up to 1 kW. The design provides a ready platform of active front-end to operate downstream DC/DC converters or inverters operating on Hi-line AC voltage range from 195-V to 270-V AC.

Telecom, server, and industrial power supplies require high efficiency over their entire operating voltage range and wide load variations from 50% to 100% load. This design demonstrates a high-performance power factor stage in a small form factor (165 mm × 95 mm), operating from 195-V to 270-V AC, and delivers up to 1 kW of continuous power output at an efficiency of greater than 97%. The design also provides precise information on power consumption of the end equipment from the AC input line, which can be used for energy calculations and control the load for power optimization on need basis. The EMI filter at the front end of the circuit is designed to meet EN55011 class-A conducted emission levels.

The design uses a 5-W housekeeping power supply board (TIDA-00708), which is designed to meet the auxiliary needs of a general power supply. It supports an input voltage range from 100-V to 450-V DC and provides a 3.5-V DC (1.5-W) and 12-V DC (2.5-W) non-isolated outputs. In addition, a 12-V DC (1-W) isolated output is also provided to support downstream auxiliary power needs. The features of the power supply board include easily pluggable, compact size (LXBXH), high efficiency, low no-load power consumption, and low cost. Find more details of this power supply in the design guide of the power supply, TIDA-00708 (TIDUBK7).

This TI Design meets the key challenges of telecom, server, and industrial power supplies to provide safe and reliable power with all protections built in while delivering high performance with low power consumption and a low bill-of-material (BOM) cost.

3 Block Diagram

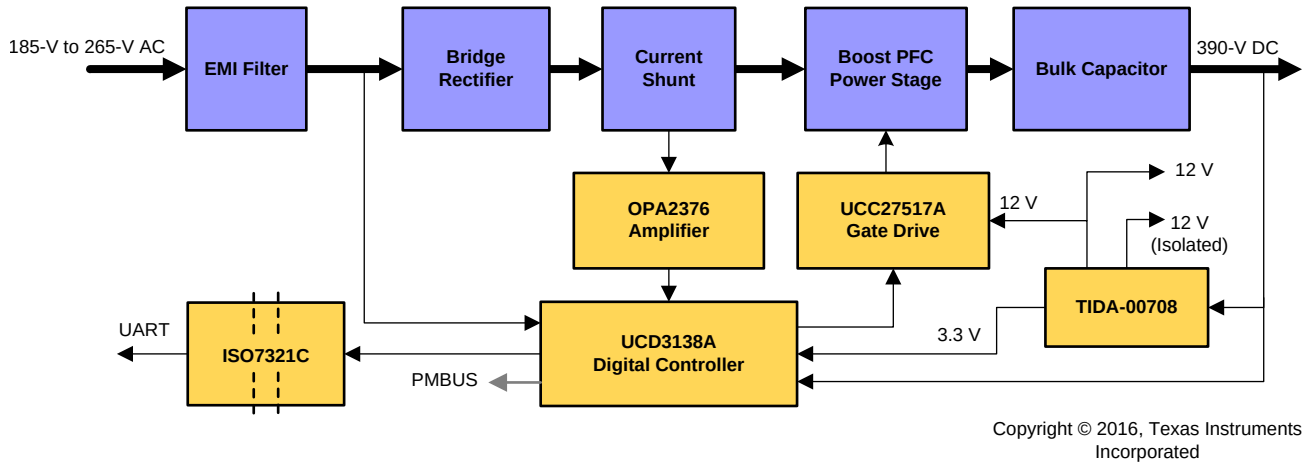


Figure 1. Block Diagram of 1-kW PFC Regulator

3.1 Highlighted Products and Key Advantages

The following highlighted products are used in this reference design. Key features for selecting the devices for this reference design are revealed in the following sections. Find more details of the highlighted devices in their respective product datasheets.

3.1.1 UCD3138A—Digital Power Supply Controller

To implement high performance and a small form factor PFC design at 1-kW power, the UCD3138A is the preferred controller as it offers a series of benefits to address the next generation needs of low THD norms and provides a digital interface for health monitoring and controls.

The UCD3138A is a fully programmable, power-optimized digital controller solution that offers the benefits of a simple design to speed up time to market while maintaining ample ability to develop high-performing and well-differentiated power supply solutions. The device is built to include a configurable digital state machine, optimized to meet the performance requirements of telecom and server isolated power applications, along with a general purpose microcontroller. The controller features optimized digital hardware for implementing a number of cutting edge power management functions such as burst mode, ideal diode emulation, mode switching, synchronous rectification, and reduced quiescent current draw in the controller. In summary, the UCD3138A addresses all key concerns such as high efficiency across the entire operating range, high degree of flexibility for various control schemes and topologies, high integration for increased power density, high reliability, and lowest overall system cost.

Other key features include:

- Digital control of up to three independent feedback loops
- Up to 16-MHz error analog-to-digital converter (EADC)
- Up to eight high-resolution digital pulse width modulated (DPWM) outputs
- Fully programmable, high-performance, 31.25 MHz, 32-bit ARM7TDMI-S processor
- 14-channel, 12-bit, 267-ksps general purpose ADC with integrated filters
- Communication peripherals (I2C/PMBus, UART)
- Configurable PWM edge movement
- Configurable feedback control
- Configurable modulation methods
- Fast, automatic, and smooth mode switching
- High efficiency and light load management
- Soft start and stop with and without pre-bias

- Fast input voltage feed forward hardware
- Rich fault protection options
- Internal temperature sensor
- Timer capture with selectable input pins
- Up to five additional general purpose timers
- Built-in watchdog: BOD and POR
- Operating temperature: –40°C to 125°C

3.1.2 UCC27517A—Low-Side Gate Driver

Lower switching losses are necessary to achieve high efficiency. The switching losses of a MOSFET are a function of drive current that needs to pass quickly through the Miller Plateau Region of the power-MOSFET's switching transition. A high-current gate driver placed closely to FET helps achieve faster turn on and turn off by effectively charging and discharging voltage across its gate-to-drain parasitic capacitor (CGD), thus reducing switching losses effectively.

The UCC27517A is a simple, low-cost, low-side gate-driver device that offers superior replacement of standard NPN and PNP discrete solutions with peak-source and a sink current of 4 A. The device is a single-channel, high-speed gate driver and has symmetrical drive with negative input voltage handling (–5 V) ability. The UCC27517A operates over a wide VDD range of 4.5 to 18 V and wide temperature range of –40°C to 140°C.

Other key features include:

- Fast propagation delays (13 ns typical)
- Outputs held low during VDD UVLO (ensures glitch-free operation at power up and power down)
- Hysteretic-logic thresholds for high-noise immunity
- Output held low when input pins are floating
- 5-pin DBV (SOT-23) package helps to optimize the space

3.1.3 TLV70433—700-V Lowest Quiescent Current Off-Line Switcher

To optimize no load power loss and meet the control circuit power needs, the low dropout (LDO) linear regulator TLV70433 is selected. The TLV70433 operates over a wide input voltage range of 2.5 to 24 V and provides 2% typical accuracy. The device is stable with an effective capacitance of 0.47 μF. It is an ideal solution for always on systems that require very little idle state power dissipation.

Other key features include:

- Current output up to 150 mA
- Low power I_Q = 3.2 μA

3.1.4 OPA2376—High-Speed, Single-Supply, Rail-to-Rail Operational Amplifier

An operational amplifier (op amp) strengthens signals to accommodate the measurement range of the UCD3138 for current sensing feedback. The op amp should have sufficient bandwidth and rail-to-rail operation for exact detection of current sense feedback. The OPA2376 is a perfect fit, as it is a low-noise, rail-to-rail swing, high-speed op amp. These features make it ideal for driving sampling ADCs used for control loops. In addition, the amplifier's wide operating temperature range and wide common-mode range ensures device performance in the most demanding environments.

Other key features include:

- Rail-to-rail input and output
- Wide bandwidth: 5.5 MHz
- Low offset voltage: 5 μV
- Low noise: 7.5 nV/√Hz
- Single-supply operation: 2.2 to 5.5 V
- High CMRR

3.1.5 ISO7321C—Low-Power, Dual-Channel 1/1 Digital Isolator With Fail-Safe High

For a dual-channel isolator with an isolated communication interface, the ISO7321C is the preferred choice, as it provides up to 3000 V_{RMS} for 1 minute per UL 1577. The device is capable of operating up to 25 Mbps and has an integrated glitch filter to aid in low-frequency operation. In fail-safe condition, the ISO7321C output defaults to high level.

Other key features include:

- Low power consumption, typ I_{CC} per channel at 1 Mbps: 1 mA (3.3-V supply)
- Qualified for
  - IEC 61000-4-2 Level 3 ESD at 6 kV
  - IEC61000-4-4 Level 4 EFT at 4-kV power, 4-kV I/O
  - IEC 61000-4-5 Level 4 Surge at 6 kV (air), 8 kV (oil)
- Wide temperature range: –40°C to 125°C

4 System Design Theory

This reference design is a 1-kW boost power factor converter, operating in CCM and implemented using the UCD3138A Digital Power Supply controller. The design is specifically tailored for telecom, server, and industrial power supplies. This serves as a superior alternative to existing analog control based PFC circuits used to meet the power harmonic norms. This design is intended to operate at country specific line voltages between 195-V to 265-V AC. Under full load conditions, the system has greater than 97% efficiency over the wide input operating voltage range from 195-V to 270-V AC. The TIDA-00707 includes several protections embedded into this design, which includes output overvoltage protection and output short-circuit protection. In addition, the design provides precise information of the power consumption of the unit.

The main focus of this design is a low EMI, high efficiency, high power factor, and protected DC power rail for targeted applications.

4.1 PFC Regulator Operating Mode

The PFC shapes the input current of the power supply to maximize the real power available from the mains. The PFC must also comply with low harmonic (low THD) regulatory requirements such as IEC61000-3-2. Currently, two modes of operation have been widely used for PFC implementations: CCM and critical conduction mode (CrM). For higher power circuits, the topology of choice is the boost converter operating in CCM and with average current mode control. For lower power applications, the CrM boost topology is typically used.

For high power levels such as 1 kW, CCM operation is preferred as it has a lower peak and RMS currents. Lower peak currents significantly reduce the stress in power MOSFET, diode, and inductor. In addition, the filtering is easier as the current is more continuous through the boost inductor. Finally, the switching frequency remains constant for the CCM operation, so the boost inductor design and EMI filter designs are easier.

4.2 PFC Circuit Component Design

The UCD3138A is configured for fixed frequency in CCM and requires minimal external components for high-wattage PFC regulator implementation. The design process and component selection for this design are illustrated in the following sections.

4.2.1 Design Goal Parameters

Table 2 shows the design goal parameters for this design. These parameters are used in further calculations when selecting components.

Table 2. Design Goal Parameters

PARAMETER		MIN	TYP	MAX	UNIT
INPUT					
V_{IN}	Input voltage	195		270	VAC
f_{LINE}	Input frequency	47		63	Hz
OUTPUT					
V_{OUT}	Output voltage		390		VDC
P_{OUT}	Output power			1000	W
	Line regulation			5%	
	Load regulation			5%	
PF	Targeted power factor		0.99		
η	Targeted efficiency		96%		

4.2.2 Current Calculations

The input fuse, bridge rectifier, and input capacitor are selected based upon the input current calculations. First, determine the maximum average output current, $I_{OUT(max)}$:

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT}} = \frac{1000\ W}{390\ V} = 2.56\ A \quad (1)$$

The maximum input RMS line current ($I_{IN\_RMS(max)}$) is calculated using the parameters from Table 2 and the initial assumptions of efficiency and power factor:

$$I_{IN\_RMS(max)} = \frac{P_{OUT(max)}}{\eta \times V_{IN(min)} \times PF} = \frac{1000\ W}{0.96 \times 195\ V \times 0.99} = 5.40\ A \quad (2)$$

The maximum input current ($I_{IN(max)}$) and the maximum average input current ($I_{IN\_AVG(max)}$) can be determined based upon the calculated RMS value and assuming the waveform is sinusoidal:

$$I_{IN(max)} = \sqrt{2} \times I_{IN\_RMS(max)} = \sqrt{2} \times 5.40\ A = 7.63\ A \quad (3)$$

$$I_{IN\_AVG(max)} = \frac{2}{\pi} \times I_{IN(max)} = \frac{2}{\pi} \times 7.63\ A = 4.86\ A \quad (4)$$

4.2.3 Bridge Rectifier

The maximum input AC voltage is 270-V AC, so the DC voltage can reach voltage levels of up to 385-V DC. Considering a safety factor of 30%, select a component with voltage rating greater than 500-V DC. The input bridge rectifier must have an average current capability that exceeds the input average current ($I_{IN\_AVG(max)}$). A higher current bridge rectifier is recommended to optimize the power loss due diode forward voltage drop.

This design uses a 1000-V, 15-A diode GBJ1508 for input rectification. The forward voltage drop of bridge rectifier diode, V_{F_BRIDGE} = 0.85 V.

The power loss in the input bridge (P_{BRIDGE}) can be calculated as:

$$P_{BRIDGE} = 2 \times V_{F\_BRIDGE} \times I_{IN\_AVG(max)} = 2 \times 0.85\ V \times 4.86\ A = 8.26\ W \quad (5)$$

4.2.4 Inductor Ripple Current

The TIDA-00707 is designed to operate in CCM. If the chosen inductor allows a relatively high-ripple current, the converter will be forced to operate in discontinuous mode (DCM) at light loads and at the higher input voltage range. High-inductor ripple currents have an impact on the boundary of CCM and DCM and results in higher light-load THD. This also affects the choices for the input capacitor, current sense resistor (R_{SENSE}), and internal compensation values tuned in software of the UCD3138A. Allowing an inductor ripple current (ΔI_{RIPPLE}) of 20% or less results in CCM operation over the majority of the operating range; however, this requires a boost inductor that has a higher inductance value, and the inductor itself will be physically large. In this design, the inductor is sized to have 30% peak–to-peak ripple current to optimize performance with size and cost. The focus of the design minimizes space with the understanding that the converter operates in DCM at the higher input voltages and light loads but is optimized well for a nominal input voltage of 230-V AC at full load.

4.2.5 Input Capacitor

Select the input capacitor based on the input ripple current and an acceptable high frequency input voltage ripple. Allowing an inductor ripple current (ΔI_{RIPPLE}) of 30% and a high frequency voltage ripple factor (ΔV_{RIPPLE_IN}) of 2%, the maximum input capacitor value (C_{IN}) is calculated by first determining the input ripple current (I_{RIPPLE}) and the input voltage ripple, V_{IN_RIPPLE}:

$$I_{RIPPLE} = \Delta I_{RIPPLE} \times I_{IN(max)} = 0.3 \times (7.63\ A) = 2.289\ A \quad (6)$$

$$V_{IN\_RIPPLE} = \Delta V_{RIPPLE\_IN} \times V_{IN\_RECTIFIED(min)} = 0.02 \times (\sqrt{2} \times 195\ V) = 5.52\ V \quad (7)$$

The recommended value for the input X-capacitor can now be calculated as:

$$C_{IN} = \frac{I_{RIPPLE}}{8 \times 140\ kHz \times 5.52\ V} = \frac{2.289\ A}{8 \times 140\ kHz \times 5.52\ V} = 0.37\ \mu F \quad (8)$$

A standard value 0.68-µF X2 film capacitor is used , taking into consideration the conducted EMI performance.

4.2.6 Boost Inductor

Based upon the allowable inductor ripple current discussed in Section 4.2.4, the boost inductor (L_{BST}) is selected after determining the maximum inductor peak current, I_{L_PEAK}:

$$I_{L\_PEAK(max)} = I_{IN(max)} + \frac{I_{RIPPLE}}{2} = 7.63\ A + \frac{2.289}{2} = 8.775\ A \quad (9)$$

The minimum value of the boost inductor is calculated based upon the acceptable ripple current (I_{RIPPLE}) at a worst case duty cycle of 0.5:

$$L_{BST(min)} \geq \frac{V_{OUT} \times D \times (1-D)}{f_{SW} \times I_{RIPPLE}} \geq \frac{390\ V \times 0.5 \times (1-0.5)}{(140\ kHz \times 2.289\ A)} \geq 304\ \mu H \quad (10)$$

The actual value of the boost inductor used is L_{BST} = 327 µH.

The duty cycle of operation is a function of the rectified input voltage and will continuously change over the half line cycle. The duty cycle ($DUTY_{(max)}$) can be calculated at the peak of minimum input voltage:

$$DUTY_{(max)} = \frac{V_{OUT} - V_{IN\_RECTIFIED(min)}}{V_{OUT}} = \frac{390\ V - (1.414 \times 195\ V)}{390\ V} = 0.293 \quad (11)$$

4.2.7 Boost Diode

The output diode must have a blocking voltage that exceeds the output overvoltage of the converter and average current same as $I_{OUT(max)}$. The diode is generally an ultra-fast recovery diode or a silicon carbide Schottky diode.

For high wattages such as 1 kW, using a silicon carbide Schottky diode, although more expensive, eliminates the reverse recovery losses and results in less power dissipation. The C3D04060A, 600-V/7.5-A SiC diode is selected as the output diode.

$$P_{DIODE} = V_{F\_125C} \times I_{OUT(max)} + 0.5 \times f_{SW} \times V_{OUT} \times Q_{RR} \quad (12)$$

The estimated power loss with the SiC diode is V_{F_125C} = 1.25 V; Q_{RR} = 0.

$$P_{DIODE} = 1.25\ V \times 2.56\ A + 0.5 \times 100\ kHz \times 390\ V \times 0nC = 3.20\ W$$

In case an ultra-fast diode is preferred (over a silicon carbide Schottky diode), the BYV29FX-600, a 600-V/9-A diode, is the best choice for this design. The diode losses with ultra-fast diodes are estimated based upon the forward voltage drop (V_F) at 125°C and the reverse recovery charge (Q_{RR}) of the diode:

$$P_{DIODE} = 1.5\ V \times 2.56\ A + 0.5 \times 100\ kHz \times 390\ V \times 13\ nC = 4.09\ W$$

4.2.8 Switching Element

The MOSFET switch is driven by a UCC27517A gate driver for which VCC bias voltages are limited to (no more than) 12 V from the bias supply. An external gate drive resistor is recommended to limit the rise time and to dampen any ringing caused by the parasitic inductances and capacitances of the gate drive circuit; this will also help in meeting any EMI requirements of the converter. This design uses a 5.0-Ω resistor; the final value of any design is dependent upon the parasitic elements associated with the layout of the design. To facilitate a fast turnoff, a standard 100-V, 1-A Schottky diode or switching diode is placed anti-parallel with the gate drive resistor. A 10-kΩ resistor is placed between the gate of the MOSFET and ground to discharge the gate capacitance and protect from inadvertent dV/dt triggered turn on.

The drain-to-source RMS current (I_{DS_RMS}) through switching FET is calculated as

$$I_{DS\_RMS} = \frac{P_{OUT(max)}}{V_{IN\_RECTIFIED(min)}} \times \sqrt{2 - \frac{16 \times V_{IN\_RECTIFIED(min)}}{3 \times \pi \times V_{OUT}}} \tag{13}$$

$$I_{DS\_RMS} = \frac{1000\ W}{275\ V} \times \sqrt{2 - \left(\frac{16 \times 275\ V}{3 \times \pi \times 390\ V}\right)} = 3.24\ A$$

The maximum voltage across the FET is the maximum output boost voltage (that is, 420 V), which is the overvoltage set point of the PFC converter to shut down the output. Considering a derating of 30%, the voltage rating of the MOSFET must be greater than 550-V DC.

IPP60R190P6 MOSFET of 600 V and 25 A at 25°C / 12 A at 100°C is selected for the current design.

The conduction losses of the switch MOSFET in this design are estimated using the $R_{DS(on)}$ at 125°C, found in the device datasheet, and the calculated drain-to-source RMS current, I_{DS_RMS}:

$$P_{COND} = I_{DS\_RMS}^2 \times R_{DS(on)} = 3.24\ A^2 \times (0.37\Omega) = 3.884\ W \tag{14}$$

The switching losses are estimated using the rise time, t_r, and fall time, t_f, of the MOSFET gate and the output capacitance losses, C_{OSS}:

$$P_{SW} = f_{SW}\left[0.5 \times V_{OUT} \times I_{IN(max)} \times (t_r + t_f) + 0.5 \times C_{OSS} \times V_{OUT}^2\right] \tag{15}$$

$$P_{SW} = 100\ kHz \times \left[0.5 \times 390\ V \times 7.63\ A \times (12\ ns + 9\ ns) + 0.5 \times 61\ pF \times 390\ V^2\right] = 3.588\ W$$

Total FET losses:

$$P_{COND} + P_{SW} = 3.884 + 3.588 = 7.472\ W \tag{16}$$

An appropriately sized single heat sink is used for the MOSFET, boost diode, and bridge rectifier.

4.2.9 Sense Resistor

Selecting a current sense resistor is based on two key parameters:

- Optimizing the power loss in the circuit
- Requiring gain and bandwidth of the op amp used to amplify the current sense signal

For current sensing feedback, the OPA2376 op amp strengthens the signals and accommodates the signal range within the measurement range of the UCD3138. In the UCD3138, the ADC used from current sensing has the measurement range of –0 to 1.6 V and has the analog comparator range of 0 to 2.5 V. To have the best signal-to-noise ratio and maximum input signal corresponding to an overcurrent condition, R_{SENSE} selected is 0.008 Ω.

For the signal conditioning, each input signal must follow the subsequent guidelines to limit the amplified signal within the range of ADC previously mentioned. The maximum op amp gain is defined by

$$K_I \le \frac{1.6\ V}{I_{IN(max)} \times 1.2 \times R_{SENSE}} \tag{17}$$

In equation 17, a factor of 20% is taken for the overcurrent limit.

$$K_I \le \frac{1.6\ V}{7.63 \times 1.2 \times 0.008} = 21.84$$

A gain of 21.1 is set using resistors R24 and R26 across the current sense amplifier, U3, as shown in Figure 2.

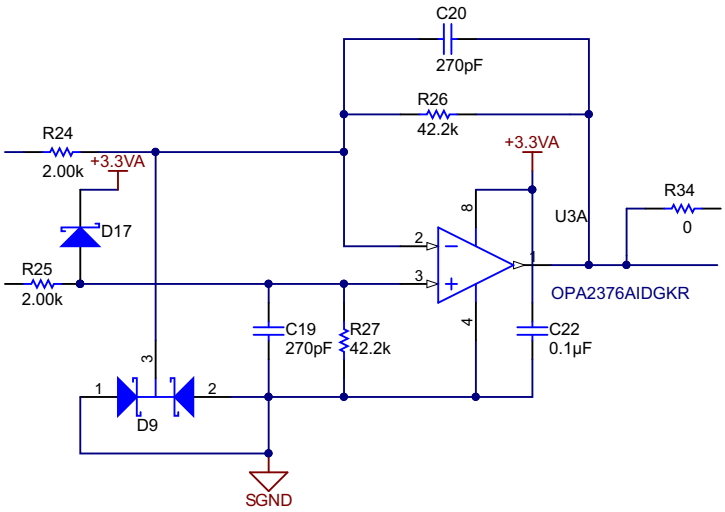


Figure 2. Amplifier Circuit for Current Sense Signal

Calculate the power dissipated across the sense resistor, P_{RSENSE}:

$$P_{RSENSE} = I^2_{IN\_RMS(max)} \times R_{SENSE} = 5.40\ A^2 \times 0.008 = 0.233\ W \tag{18}$$

4.2.10 Output Capacitor

The output capacitor, C_{OUT}, is sized to meet holdup requirements of the converter or the output ripple. In this design, the sizes of the output capacitors are based on a voltage ripple of less than 3% of the output DC voltage.

$$C_{OUT(min)} \geq \frac{I_{OUT}}{\pi \times 2 \times 2 \times f_{LINE(min)} \times V_{RIPPLE}} \tag{19}$$

Where V_{RIPPLE} = 0.03 × 390 V (assuming 3 % voltage ripple).

$$C_{OUT(min)} \geq \frac{2.56}{\pi \times 2 \times 2 \times 57 \times 0.03 \times 390} = 305\,\mu F$$

The actual capacitor used is 440 μF.

The required ripple current rating at twice the line frequency is equal to:

$$I_{COUT\_2fline} = \frac{I_{OUT(max)}}{\sqrt{2}} = \frac{2.56\ A}{\sqrt{2}} = 1.81\ A \tag{20}$$

There is a high-frequency ripple current through the output capacitor:

$$I_{COUT\_HF} = I_{OUT(max)} \times \sqrt{\frac{16 \times V_{OUT}}{3 \times \pi \times V_{IN\_RECTIFIED(min)}} - 1.5} \tag{21}$$

$$I_{COUT\_HF} = 2.56\ A \times \sqrt{\frac{16 \times 390\,V}{3 \times \pi \times 1.414 \times 195\,V} - 1.5} = 2.43\ A$$

The total ripple current in the output capacitor is the combination of both, and the output capacitor must be selected accordingly:

$$I_{COUT\_RMS(total)} = \sqrt{\left(I_{COUT\_2fline}\right)^2 + \left(I_{COUT\_HF}\right)^2} = \sqrt{(1.81)^2 + (2.43)^2} = 3.03\ A \tag{22}$$

4.2.11 Output Voltage Set Point

For low power dissipation and minimal contribution to the voltage set point, 600 kΩ is used for the top voltage feedback divider resistor, R_{FB1}. Multiple resistors in series are used due to the maximum allowable voltage across each resistor.

For each input signal to the UCD3138, its magnitude must accommodate the measurement range of the device. In the UCD3138, the ADC measurement range is 0 to 2.5 V. To have the best signal-to-noise ratio, the input signal must be as large as possible. For this reason, the signal conditioning for each input signal must follow these guidelines:

For V_{OUT}, the voltage divider:

$$K_{VOUT} \leq \frac{2.5\ V}{V_{OUT(max)}} \tag{23}$$

When the maximum output voltage $V_{OUT(max)}$ is 420-V DC, including the overvoltage protection set at 415-V DC:

$$K_{VOUT} \leq \frac{2.5\,V}{420\,V} = 0.00595$$

Considering these constraints on the gain, the bottom divider resistor, R_{FB2}, is selected to meet the feedback voltage of 2.0 V at V_{OUT} of 390 V.

$$R_{FB2} = \frac{V_{REF} \times R_{FB1}}{V_{OUT} - V_{REF}} = \frac{2.0\ V}{390\ V} \times R_{FB1} = 3.07\,k\Omega \tag{24}$$

A standard value 3.16-kΩ resistor is selected for R_{FB2}. A 0.1-μF capacitor is added across RFB2 to filter out noise.

4.3 Bias Power

An auxiliary housekeeping power supply is needed to power the UCD3138A control circuit, UCC27517A gate driver, and inrush current limiting bypass relay. In addition, external cooling is required when the converter is operated at power ≥ 900 W. To address each of these needs, an add-on auxiliary power supply board (TIDA-00708) of 5 W is used. This board is based on a Flyback design using the high voltage off-line switcher UCC28881. The TIDA-00708 provides a 3.3-V and two 12-V isolated outputs. For more details, see the TIDA-00708 design guide (TIDUBK7).

Note that the auxiliary power supply TIDA-00708 is already mounted in the TIDA-00707 design and hence is an integral part of TIDA-00707.

Table 3. Expected Auxiliary Power Consumption for Different Devices

DEVICE	VOLTAGE (V)	MAX CURRENT (mA)
UCD3138A controller	3.3	100
Relay	12	35
Gate driver	12	35
Fan (optional)	12	75

4.4 Designing the Firmware on UCD3138A Controller for Single-Phase PFC

The UCD3138 digital power supply controller has multiple peripherals inside the device, which have been specifically optimized to enhance the performance of PFC circuit.

A step-by-step guide for the design of the UCD3138A firmware required for the TIDA-00707 PFC is explained in the PMP10804 test results (TIDUAY4). This document covers the hardware interface, voltage loop and current loop implementation, system protection, firmware structure, internal state machines, and other advanced features. A graphical user interface (GUI) and a guide for tuning the coefficients of a PFC system are also presented in the guide.

5 Getting Started Firmware

This section details the necessary equipment, test setup, and procedure instructions to program the TIDA-00707 board with the provided software.

5.1 Programming the UCD3138A

The design needs the following equipment and necessary files to program the device:

- PMBus to USB Interface Adapter Kit (HPA172)
  Accessories include:
  - USB interface adapter
  - USB cable (5-pin B mini male to Type A male)
  - Ribbon cable (Socket to socket, 10 pins, 2 headers, polarized)
  - Four male-to-female interface wires to connect USB interface adapter to connecter J7 on TIDA-00707 control card

Figure 3. USB Adapter (HPA172) Outlook

- GUI installations file
  "TI-Fusion-Digital-Power-Designer-2.0.16.exe" or later version
- Firmware file
  UCD3138_PFC.x0 file, located in the software package folder path \TIDA-00707_1.0\Debug
- PC operating system
  Microsoft® Windows XP®, or Vista®, or Windows 7®.

5.1.1 GUI Setup

To use the GUI:

1. Find installation file.
   The GUI installation file is "TI-Fusion-Digital-Power-Designer-Version-2.0.16.exe" or later version.
2. Install the file.
   Double click and launch the .exe file to start the installation. Click "Next" all the way through. When presented, click "I accept the agreement" after reading it. Then click "Install".
3. Launch UCD3138 GUI.
   After the installation, click "Finish" to exit setup; then click "Exit Program". The GUI for the TIDA-00707 board can be launched through the following steps:

   (a) Click the Windows "Start" button.

   (b) Click "All Programs".

   (c) Click "Texas Instruments Fusion Digital Power Designer".

   (d) Click "Device GUIs".

   (e) Click "UCD3xxx & UCD9xxx Device GUI".

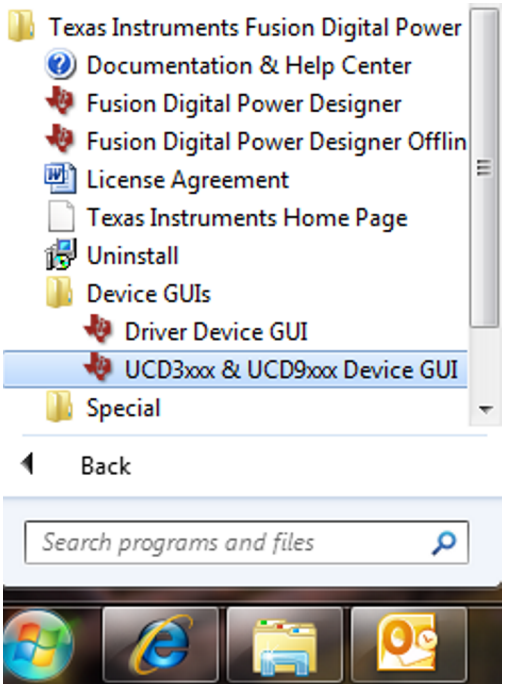


Figure 4. GUI Launch Path

5.1.2 Hardware Setup

5.1.2.1 Setup Overview

Figure 5 shows the connection between the TIDA-00707 and the PC computer through a USB interface adapter (HPA172).

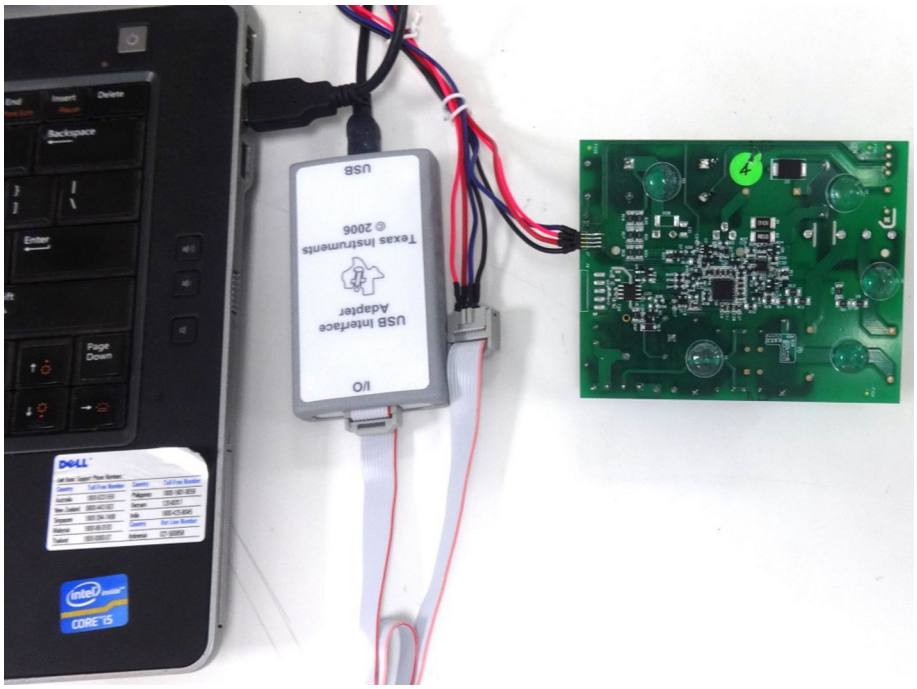


Figure 5. TIDA-00707 Setup for Programing UCD3138A

NOTE: In Figure 5, pin numbers connected on the board are 1 to 4 from top to bottom, respectively.

5.1.2.2 USB Adaptor Connection

1. Use four jumper cables (male on one end and female on the other end) to connect the connector J7 of the "TIDA00707 board" and the connector of USB interface adapter (HPA172). The connection details are shown in Table 4.

Table 4. Connections Between J7 and USB Interface Adapter for Programming

PIN NUMBER ON THE CONNECTOR OF HPA172 (FROM)	PIN NUMBER ON CONNECTOR J7 OF TIDA-00707 BOARD (TO)
5	1
6	4
9	2
10	3

2. Connect the mini connector of the USB cable to the USB interface adapter and connect the other end to the USB port of the PC.
3. The LED on HPA172 should be illuminated. If not, unplug the USB cable and reconnect. If the LED is still not illuminated, change with a new HPA172 USB adapter. If the LED is illuminated, proceed to the next step.

5.1.3 Procedure

1. Launch the GUI by the steps described in Section 5.1.1. Wait until the window shown in Figure 6 appears.
2. Click "Scan Device in ROM Mode", then wait and check Figure 6 on its "Log" and confirm "Found ROM v2 IC v3 – UCD31xx". If "Found ROM" is not shown, click "Device ID", then click "Command Program to jump to ROM (sendByte0xD9)", and then click "Scan Device in ROM Mode" again. If the device is found, proceed to the next step.

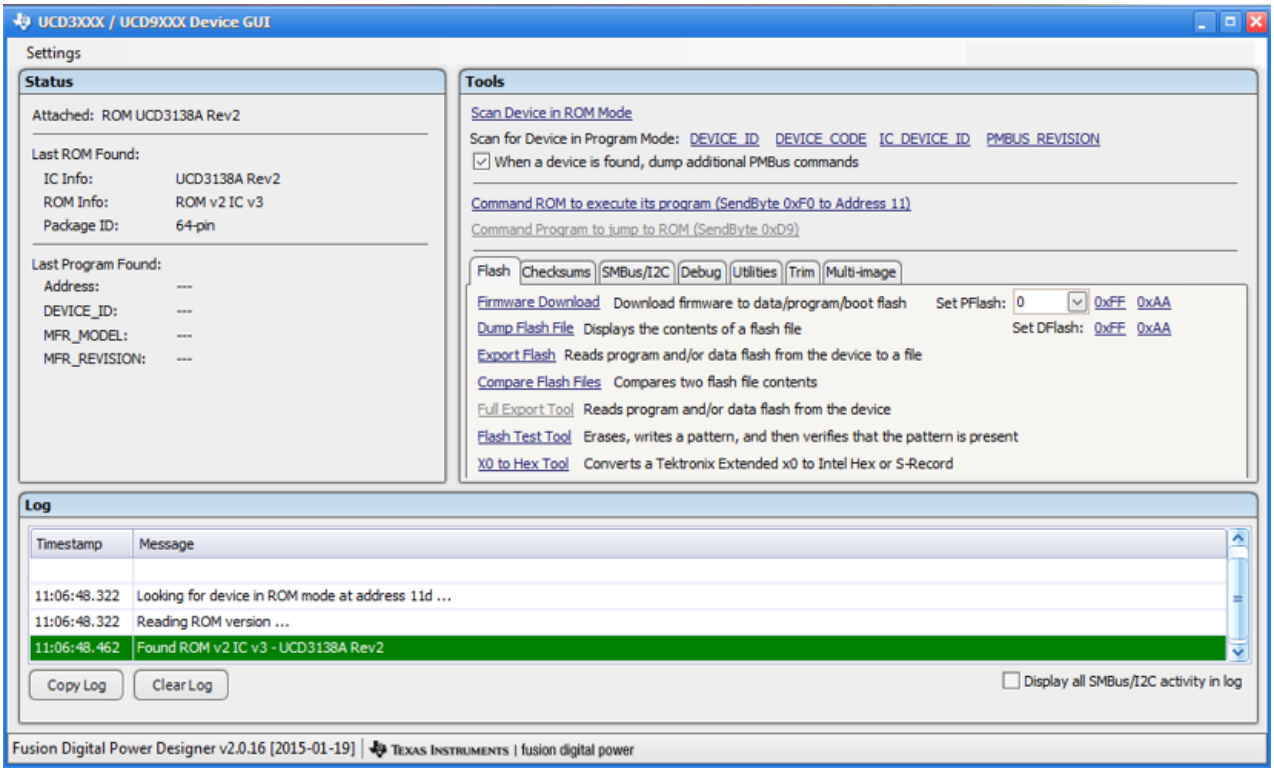


Figure 6. OK Indication (Found ROM)

3. On the GUI is shown as in Figure 6, click Firmware Download, then a new window appears, as in Figure 7. In this new window:

   (a) Check "Download data flash". If the “DO NOT write program checksum” radio button is chosen as shown in Figure 7, the firmware will not be executed once the PFC is powered up. Click "Command ROM to execute its program" to execute the program.

   If the "Write program checksum" radio button is chosen, the firmware will be executed automatically once the PFC is powered up.

   (b) Click "Select file" and find "UCD3138_PFC.x0", which is located in the software package folder path \TIDA-00707_1.0\Debug, and click "Download".

   (c) After downloading the program, click "Close" to close the window shown in Figure 7.

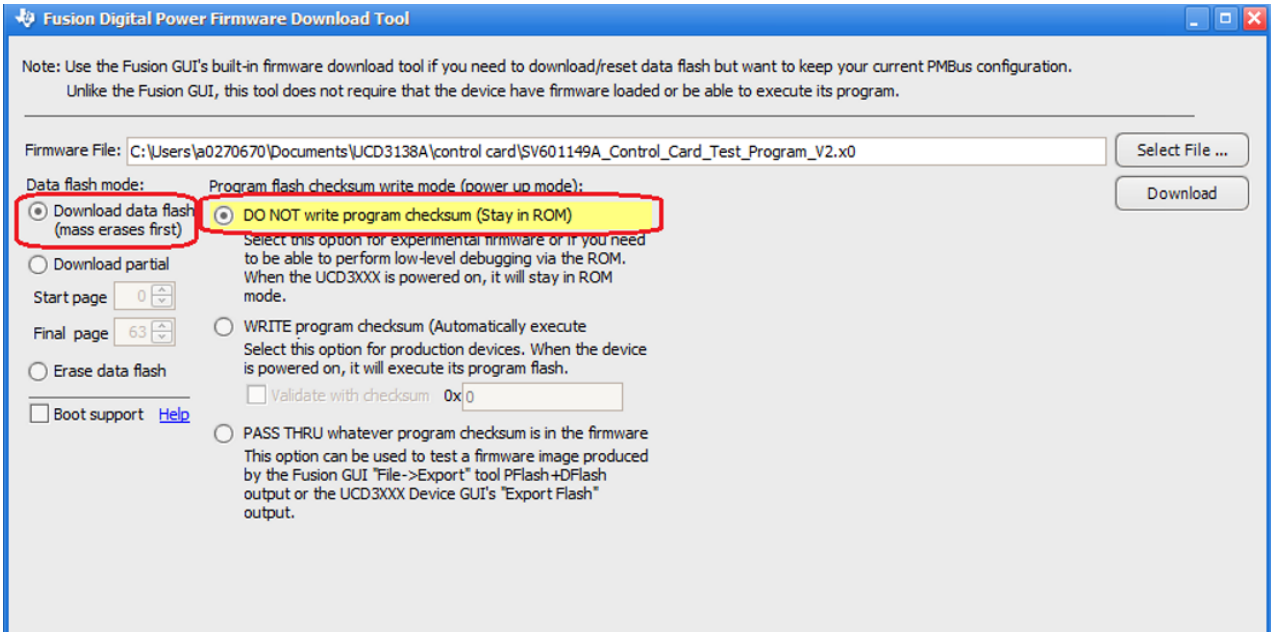


Figure 7. Download the Firmware

6 Getting Started Hardware

This section details the necessary equipment, test setup, and procedure instructions for the TIDA-00707 board testing and validation.

6.1 Test Conditions

For input, the power supply source (V_{IN}) must range from 195-V to 270-V AC. Set the input current limit of input AC source to 7.5 A.

For output, use an electronic variable load or a variable resistive load, which must be rated for ≥ 400 V and must vary the load current from 0 mA to 3 A.

6.2 Test Equipment Required for Board Validation

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multimeters
- Electronic or resistive load

6.3 Test Procedure

1. Connect input terminals of the reference board to the AC power source.
2. Connect output terminals to the electronic load, maintaining correct polarity. VDC and ground pins of the output are provided as test points. These test points can be removed to make proper soldered connections for loading the converter for testing.
3. Set and maintain a minimum load of about 10 mA.
4. Increase gradually the input voltage from 0 V to turn on voltage of 195-V AC.
5. Start the load to draw current from the output terminals of the PFC.
6. Observe startup conditions for smooth switching waveforms.
7. For a power of ≥ 900 W, an external fan can be used for cooling. A low-wattage, high LFM fan such as 612NMLE is recommended with a 12-V output provided at connector J3. Ensure that the fan is rated for 12-V operation and power ≤ 0.75 W.
8. Connect the fan at connector J3, maintaining correct polarity.
9. If a low-wattage fan is not available, a cooling fan can be powered from an external DC lab power supply.

7 Test Results

The test results are divided in multiple sections that cover the steady state performance, functional performance waveforms and test data, transient performance waveforms, thermal measurements, conducted emission measurements, and Surge and EFT measurements.

7.1 Performance Data

7.1.1 Efficiency and Regulation With Load Variation

Table 5 shows the data at a 230-V AC input:

Table 5. Efficiency and Regulation With Load Variation

V_{INAC} (V)	I_{INAC} (A)	PF	P_{INAC} (W)	i_{THD} (%)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFF (%)	% REG
230	0.23	0.80	41.5	13.59	390.8	0.10	37.1	89.4	0.07
230	0.37	0.94	79.6	12.90	390.7	0.19	74.6	93.7	0.04
230	0.70	0.97	156.2	12.12	390.7	0.38	149.2	95.6	0.04
230	1.03	0.99	233.4	9.50	391.0	0.58	224.8	96.3	0.12
230	1.36	0.99	309.7	7.00	390.9	0.77	299.4	96.7	0.10
230	1.69	0.99	386.6	2.96	390.9	0.96	374.5	96.9	0.10
230	2.02	1.00	462.7	2.30	390.8	1.15	449.0	97.0	0.07
230	2.35	1.00	539.4	2.00	390.8	1.34	524.1	97.2	0.07
230	2.68	1.00	615.7	1.99	390.8	1.53	598.7	97.2	0.07
230	3.02	1.00	694.0	1.85	390.7	1.73	674.7	97.2	0.04
230	3.35	1.00	770.2	1.72	390.5	1.92	748.2	97.1	–0.01
230	3.68	1.00	847.1	1.58	390.4	2.11	822.2	97.1	–0.03
230	4.01	1.00	923.0	1.41	390.1	2.30	895.7	97.0	–0.11
230	4.20	1.00	997.1	1.43	390.0	2.48	967.2	97.0	–0.15
230	4.50	1.00	1034.0	1.40	390.0	2.57	1002.6	97.0	–0.16

7.1.2 Standby Power

The standby power was noted at multiple AC input voltages with a constant negligible load on the output DC bus. The results are tabulated in Table 6:

Table 6. No Load Power Consumption

V_{INAC} (VAC)	ENERGY INPUT AFTER 3 MIN (mWh)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	NO LOAD INPUT POWER (W)
195	113.0	392	0.0	0.0	2.26
230	106.0	392	0.0	0.0	2.12
270	96.0	392	0.0	0.0	1.92

No load power is contributed by three main branches:

- Resistors used input AC voltage sensing
- Resistors used for output DC bus voltage sensing
- Power consumed by controller and relay

The power consumed by AC input and DC output sensing resistors is ~0.55 W, and this can be decreased by increasing the resistor values.

7.2 Performance Curves

7.2.1 Efficiency and Power Factor With Load and Line Variation

Figure 8 and Figure 9 show the measured efficiency and power factor in the system with AC input voltage variation.

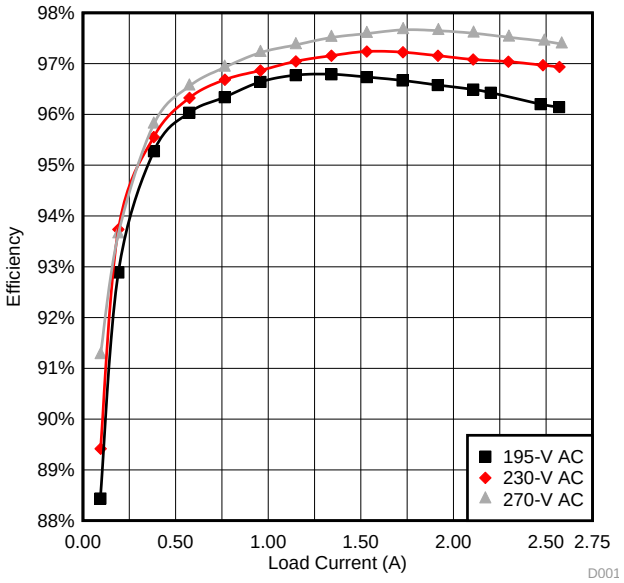


Figure 8. Efficiency versus Output Load Current (I_{OUT})

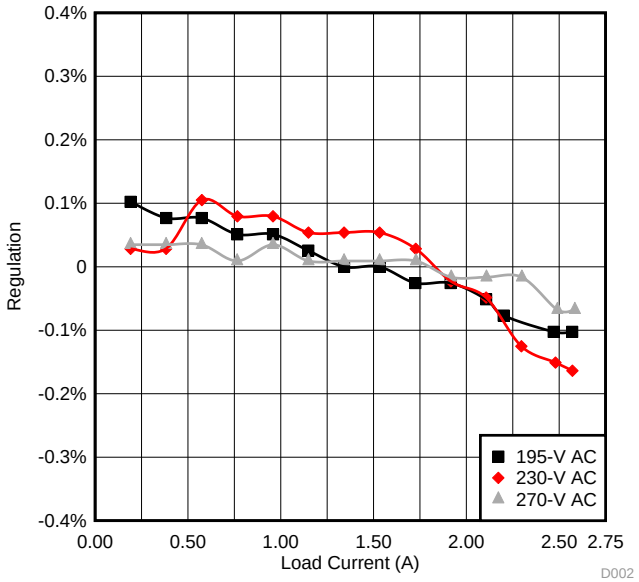


Figure 9. Power Factor versus Load Current

7.2.2 Input THD With Load and Line Regulation

Figure 10 shows the measured input THD of the system with AC input voltage variation. Figure 11 shows the measured load regulation of the output with AC input voltage variation.

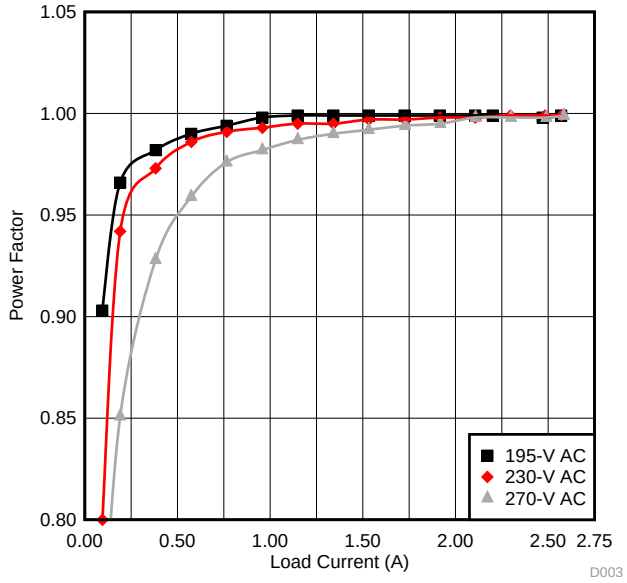


Figure 10. Input THD Variation With Load Current

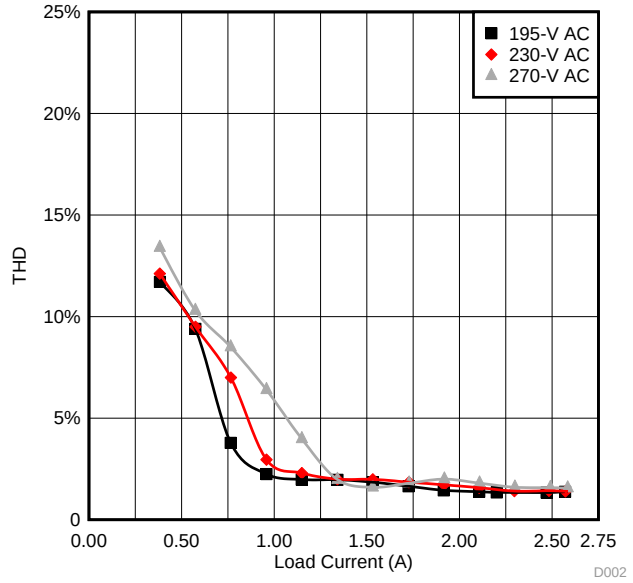


Figure 11. Output Voltage Variation With Load Current for Various AC Input Voltages

7.3 Functional Waveforms

7.3.1 Switching Node Waveforms

The waveform at switching node (SW) was observed along with the PFC inductor current for 230-V AC under full load (2.31 A) conditions.

NOTE: Red trace: Drain voltage, 100 V/div; Green trace: PFC inductor current, 5 A/div

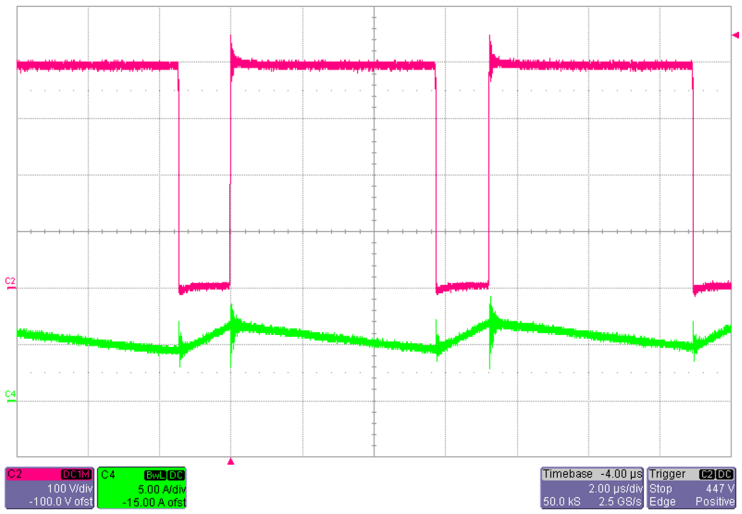


Figure 12. SW Node Waveform and MOSFET Current at V_{INAC} = 230-V AC, Full Load

NOTE: Red trace: Drain voltage, 100 V/div; Green trace: Drain current, 5 A/div

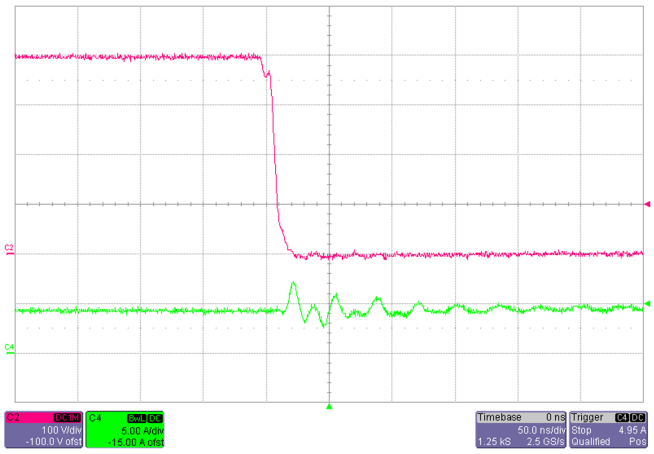


Figure 13. SW Node Waveform Turn-on Cycle at V_{INAC} = 230-V AC, Full Load

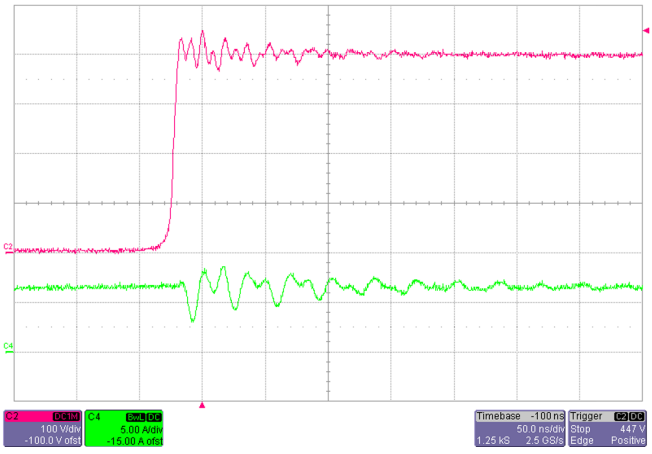


Figure 14. SW Node Waveform Turn-off Cycle at V_{INAC} = 230-V AC, Full Load

7.3.2 Input Voltage and Current Waveform

Figure 15 shows the input current waveform at 230-V AC with full load conditions.

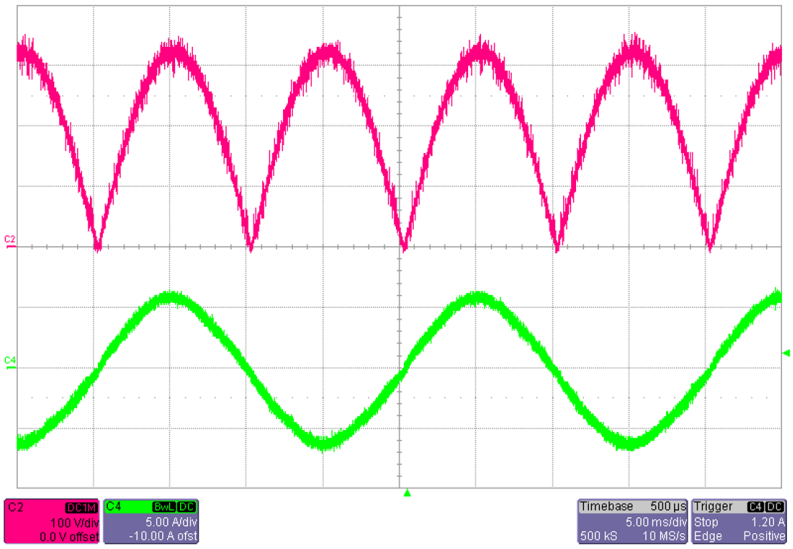


Figure 15. Input Voltage and Input Current at V_{INAC} = 230-V AC, Full Load

7.3.3 Inrush Current Waveform

Inrush current drawn by the system is observed and recorded at a maximum input voltage of 230-V AC.

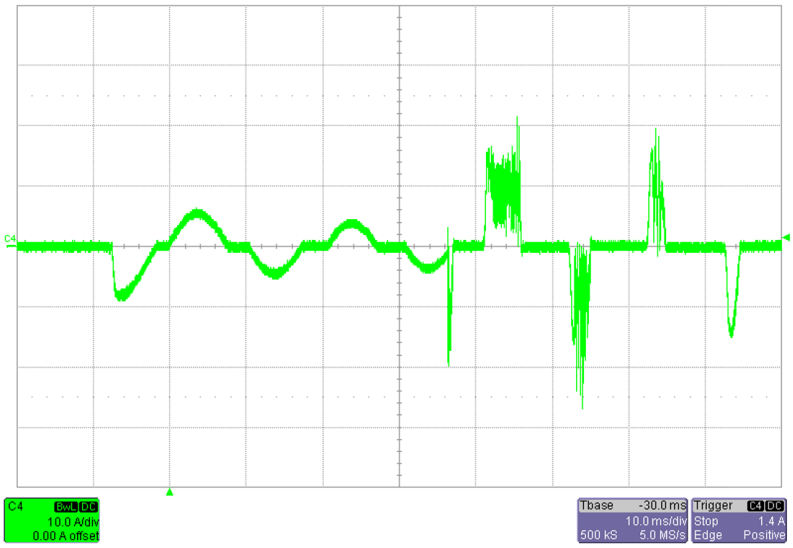


Figure 16. Output Voltage and Input Inrush Current at V_{INAC} = 230 V, Full Load

7.3.4 Output Ripple

A ripple observed at the 390-V DC output is loaded to 2.56 A at 230-V AC.

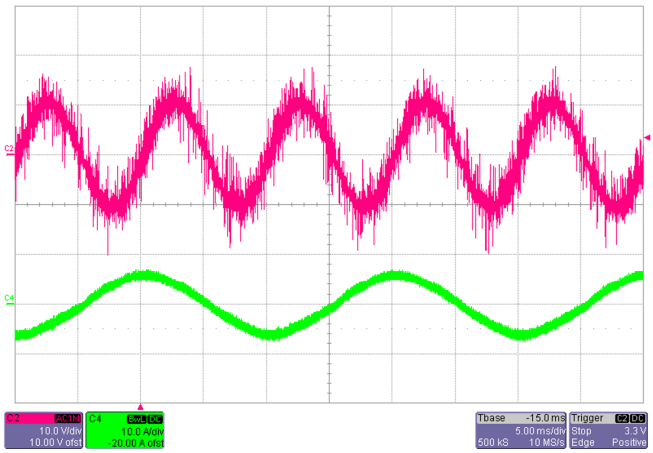


Figure 17. Output Voltage Ripple at V_{INAC} = 230 V, Full Load

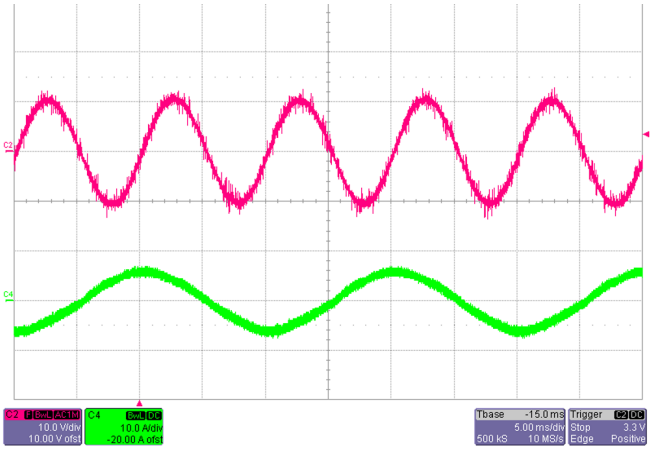


Figure 18. Output Voltage Ripple at V_{INAC} = 230 V, Full Load, Only 50-Hz Component

7.3.5 Turn-On Characteristics

The 390-V output turn on at full load (2.31 A) was recorded at 230-V AC.

NOTE: Red trace: Output DC bus, 100 V/div; Green trace: Output current, 0.5 A/div.

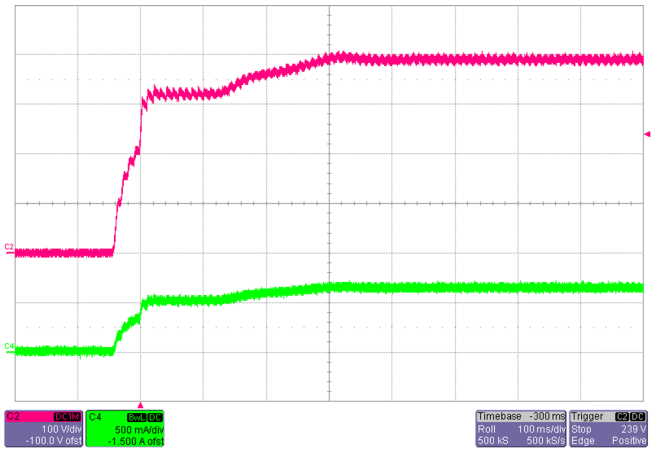


Figure 19. Output Turn-on Waveform at V_{INAC} = 230 V With Light Load of 0.5 A

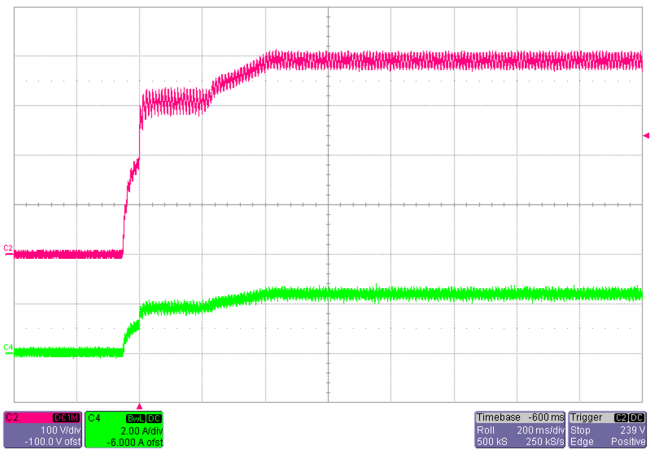


Figure 20. Output Turn-on Waveform at V_{INAC} = 230 V With Full Load of 2.56 A

7.4 Transient Waveforms

7.4.1 Transient Load Response

Load transient performance is observed with the load switched at a 0.2-m wire length. The output load is switched using electronic load.

V_{IN} = 230-V AC, load transient from 0.5 to 2.56 A and vice-versa performance at a 390-V output.

NOTE: Red trace: Output voltage, 20 V/div, AC coupling; Green trace: Output current, 1 A/div.

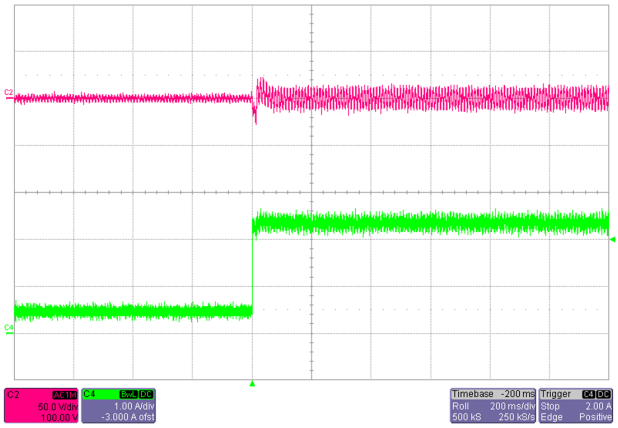


Figure 21. Output Voltage Waveform at V_{INAC} = 230 V, Load Transient From 0.5 to 2.56 A

NOTE: Red trace: Output voltage, 20 V/div, AC coupling; Green trace: Output current, 1 A/div.

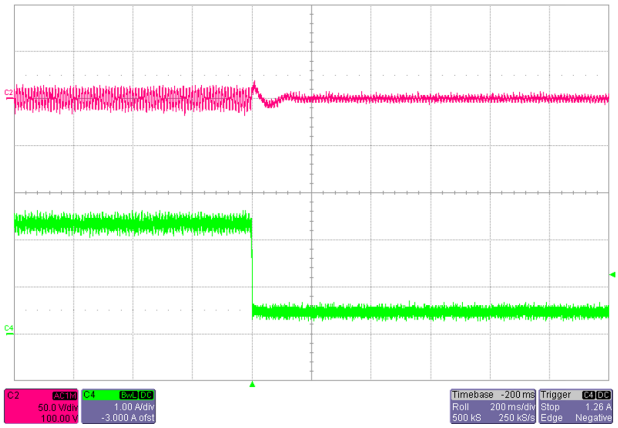


Figure 22. Output Voltage Waveform at V_{INAC} = 230 V, Load Transient From 2.56 to 0.5 A

7.5 Conducted Emissions

Generally, conducted emissions increase at full load. This operating point is chosen for measuring conducted EMI.

7.5.1 With Resistive Load at Output

The 230-V AC input, 2.56-A resistive load is connected to the PSU with short leads. The conducted emissions in a pre-compliance test setup were compared against EN55011 class-A limits and found to meet them satisfactorily.

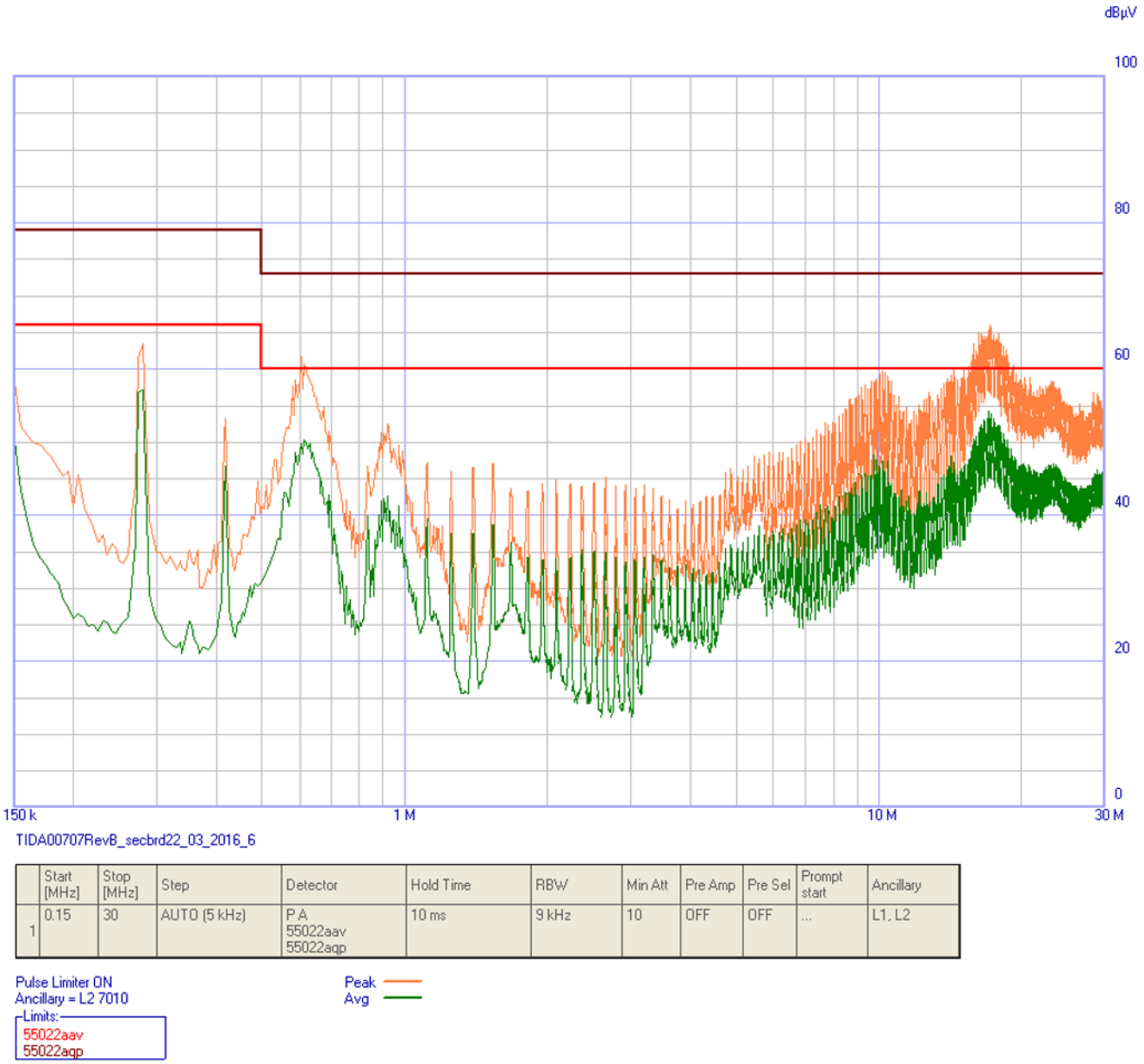


Figure 23. Conducted Emissions as per EN55011 Class A

7.6 Surge and Fast Transients Tests

Surge and EFT testing is done on the boards as per EN55014. The test condition and test results are tabulated in Table 7.

Table 7. Surge and EFT Test Results

BASIC STANDARD	PORT	IEC 61000-6-2/EN 50082-2 REQUIREMENTS[1]	PERFORMANCE CRITERION REQUIRED	TEST RESULT
IEC/EN 61000-4-4: Fast transients (burst)	AC input	±2 kV, 5 kHz	B[2]	Passed with performance criterion A[3]
IEC/EN 61000-4-5: Surge	AC input	±4 kV line to earth ±2 kV line to line	B[2]	Passed with performance criterion A[3]

(1) Immunity standard for industrial environments
(2) Temporary loss of function or degradation of performance which ceases after the disturbance ceases
(3) Normal performance within limits specified by the design or manufacturer

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00707.

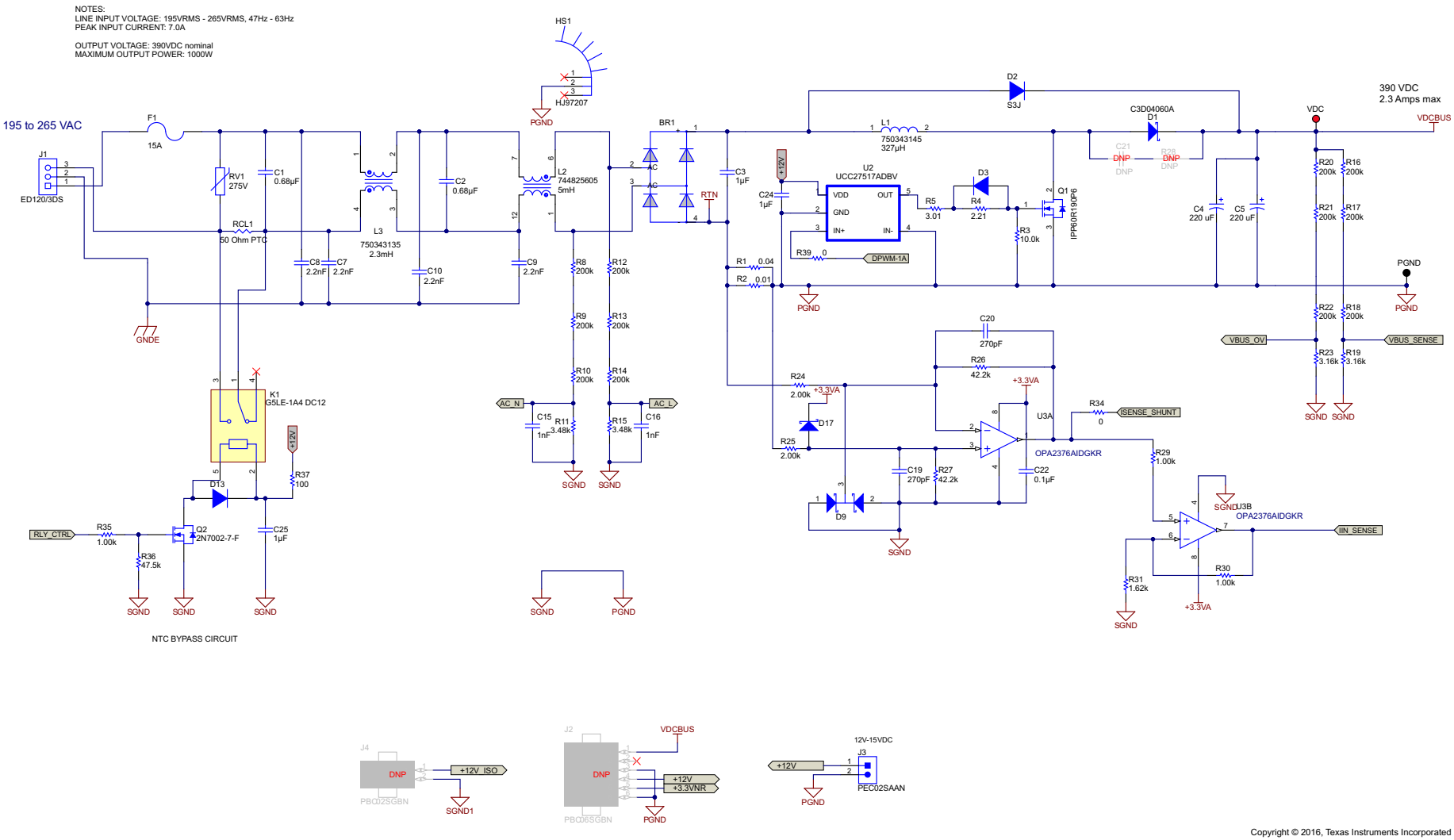


Figure 24. Power Stage, Current and Voltage Sensing Schematic

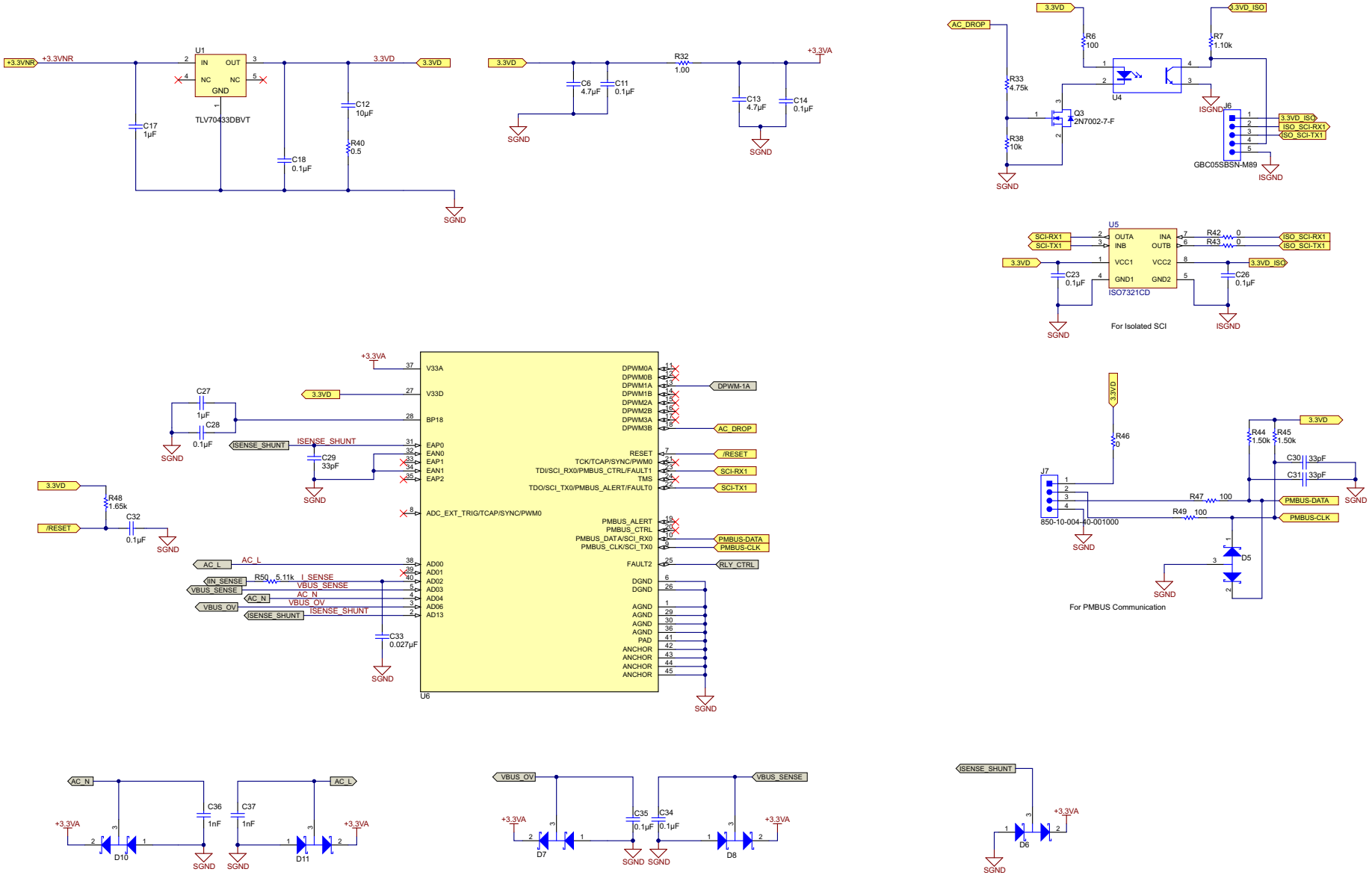


Figure 25. Controller and Communication Interface Schematic

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00707.

8.3 PCB Layout Recommendations

A careful PCB layout is critical in a high-current fast-switching circuit to provide appropriate device operation and design robustness. As with all switching power supplies, pay attention to detail in the layout to save time in troubleshooting later on.

8.3.1 Power Stage Specific Guidelines

Follow these key guidelines to route the power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high frequency switching currents. This will help reduce EMI and improve the converter's overall performance.
- Keep the switch node as short as possible. A short and optimal trace width helps to reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dt potential and high di/dt capability away from or shielded from sensitive signal traces with adequate clearance and ground shielding.
- Keep power ground and control ground separate for each power supply stage. Tie them together (if they are electrically connected) in one point near DC input return or output return of the given stage.
- When multiple capacitors are used in parallel for current sharing, the layout should be symmetrical across both capacitor leads. If the layout is not identical, the capacitor with the lower series trace impedance will see higher peak currents and become hotter (i2R).
- Tie the heat sinks of all the power switching components to their respective power grounds.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route with short traces to reduce inductance.
- Choose the width of PCB traces based on an acceptable temperature rise at the rated current as per IPC2152 as well as acceptable DC and AC impedances. The traces should withstand the fault currents (such as short circuit current) before electronic protection devices, such as fuses or circuit breakers, are activated.
- Determine the distances between various traces of the circuit according to the requirements of applicable standards. For this design, the UL 60950-1 safety standard is followed to maintain the creepage and clearance from live line to neutral line and to safety ground, as defined in the Tables 2K through 2N of this standard.
- Adapt the thermal management to fit the end-equipment requirements.

8.3.2 UCD3138A Controller Specific Guidelines

The UCD3138A is a highly integrated controller with a large number of mixed signals. Follow these key guidelines to route the controller components and signal circuits:

- To reduce noise coupling and prevent chip malfunction, group each pin, select good components, have appropriate connections to each pin, and place well on the PCB.
- To avoid chip malfunction, group all digital circuitry and analog circuitry, place digital circuitry close to each other, place analog circuitry close to each other and make trace connections among them.
- Locate all controller support components at specific signal pins close to their connection pin. Connect the other end of the component to the AGND or DGND, respectively, with shortest trace length.
- Find detailed recommendations of each pin connection and its associated component in the UCD3138A data manual (SLUSC66).
- Reference grounds AGND or DGND for the device can be common ground SGND (signal ground) or separate grounds. In either case, these grounds must be a copper plane or island. If there are separate AGND or DGND planes, tie them together close to the chip.
- Make the trace routing for the voltage sensing and current sensing circuit components to the device as short as possible to reduce parasitic effects on the current limit and current and voltage monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- Connect the SGND plane to high current ground (main power ground) at a single point that is at the negative terminal of DC IO capacitor, respectively.

8.3.3 Gate Driver Specific Guidelines

Follow these key guidelines to route the high-frequency high-current gate driver:

- Locate the driver device as close as possible to the power device to minimize the length of high current traces between the output pins of gate drive and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD.
- Minimize the turn-on and turn-off current-loop paths (driver device, power MOSFET, and VDD bypass capacitor) as much as possible to keep the stray inductance to a minimum.
- Minimize noise coupling with star point grounding from one current loop to another. Connect the driver GND to the other circuit nodes such as the power switch source or the PWM controller ground at one single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.

8.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-00707.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00707.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00707.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00707.

9 Software Files

To download the software files, see the design files at TIDA-00707.

10 References

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11 Terminology

SLYZ022 — TI Glossary: This glossary lists and explains terms, acronyms, and definitions.

Specific terms used in the document:

PWM— Pulse width modulation

FETs, MOSFETs— Metal–oxide–semiconductor field-effect transistor

IGBT— Insulated gate bipolar transistor

ESD— Electrostatic discharge

RMS— Root mean square

12 About the Authors

LATIF AMEER BABU is a Systems Architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Latif brings to this role his extensive experience in power electronics, high frequency DC-DC converter, and analog circuit design. Latif earned his master of technology in power electronics and power systems from Indian Institute of Technology, Mumbai; IN. Latif is a member of the Institute of Electrical and Electronics Engineers (IEEE) and has one US patent.

BOSHENG SUN is a Systems Engineer at Texas Instruments where he is responsible for systems solution, firmware design and collateral development for TI's high voltage power controller products. Bosheng earned a B.S. degree from Tsinghua University, China in 1995, and an M.S. degree from Cleveland State University, Ohio in 2003, both in electrical engineering. Bosheng has three US patents.

KRISHNA DORA is a Systems Engineer at Texas Instruments where he is responsible for developing reference design solutions for the Power Delivery, Industrial Segment. Krishna brings to this role his extensive experience in high power converters – Solar and UPS. Krishna earned a B.S degree from Andhra University, India in 2001, and M.Tech degree from IIT Bombay, Mumbai in 2004, both in electrical engineering. He has two US patents in his name.

Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (May 2016) to B Revision	Page
• Changed title from *1-kW, Compact, High Efficiency, Digital PFC Front-End Reference Design for Telecom and Server PSU*	1

Revision A History

Changes from Original (April 2016) to A Revision	Page
• Changed from preview page	1

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265