TI Designs
Isolated GaN Driver

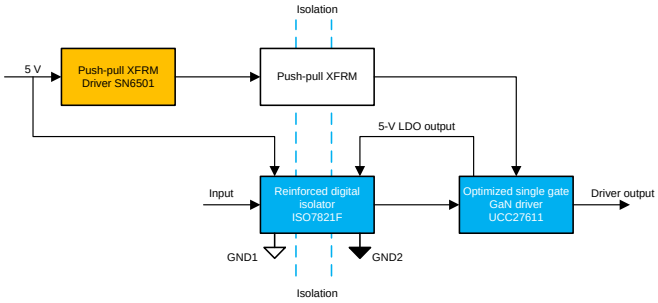
TI Designs

This reference design consists of a reinforced dual channel digital isolator, a GaN gate driver, and isolated power supplies. This compact reference design is intended to control GaN in power supplies, DC-to-DC converters, synchronous rectification, solar inverters, and motor control. An open-loop push-pull topology based power supply for gate drivers provides flexibility in PCB routing. The push-pull transformer driver used in the TIDA-00785 operates at 300 kHz, which helps in reducing the size of the isolation transformer, leading to a compact power supply solution.

Design Resources

TIDA-00785	Design Folder
ISO7821F	Product Folder
SN6501	Product Folder
UCC27611	Product Folder

TI E2E™ Community — ASK Our E2E Experts

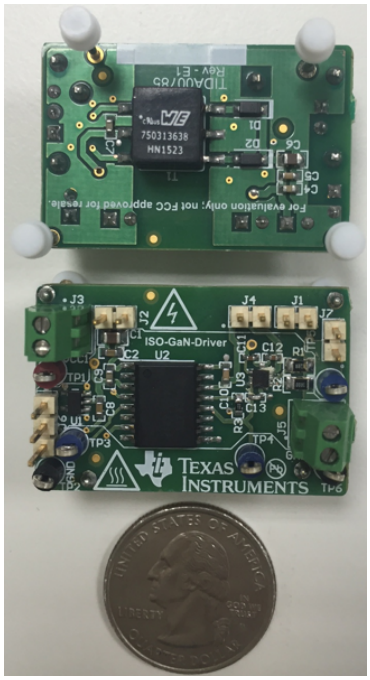


Design Features

- Suited for Low-Voltage GaN Drives (300 to 450 V)
- Rail-to-Rail Peak Current Drive Capability With 4-A Source and 6-A Current Suits Driving GaN Modules
- 5000-V_{RMS} Isolation for 1 Minute per UL 1577
- Industry Leading Common-Mode Transient Immunity (CMTI): ±100 kV/µs (Min)
- Spread Spectrum Operation of Transformer Driver Helps Reduce Emissions
- PWM Signals of Gate Drivers Can be Directly Interfaced to a Controller (3.3-V Operation)

Featured Applications

- Switch-Mode Power Supplies (SMPS)
- Uninterruptible Power Supplies (UPS)
- DC-to-DC Converters
- Synchronous Rectification
- Solar Inverters
- Motor Control
- Envelope Tracking Power Supplies



1 Key System Specifications

Table 1. Key System Specifications

FEATURE	PARAMETER	SPECIFICATION
GaN drive	Voltage	4- to 18-V single supply range
	Current	4-A peak source and 6-A peak sink
	Output power	1 W/GaN
Isolation	CMTI	100 kV/µs
	Isolation	5000 V_{RMS} for 1 minute
	Working voltage	1500 V_{RMS}
Interface	Voltage	5.0 V
	Input signals	PWM
System and drive specifications	Drive input voltage (GaN)	Up to 300-V AC
	Power supply input voltage	5 V ± 5%

2 System Description

GaN drivers are an inherent part of any power supply, high power inverters system, or motor control system. Isolation is required in these systems for the following purposes:

- Meeting safety requirements (Standards provided in ISO61800-5-1). The output power stage of the drive can have dangerously high voltages. Isolation is used to electrically separate the low-voltage operator side from the high-voltage drive stage.
- Driving the top switch of an inverter half bridge. In order to drive the top switch of an inverter half bridge, the applied gate voltage has to be with respect to the half bridge phase terminal. This point is floating, meaning the phase it switches between the DC bus voltage and ground.
- Managing voltage level translation. The MCU generates a PWM signal at low-voltage levels, such as 3.3 or 5 V. The gate controls required by the GaNs are in the range of 4 to 18 V, and need high current capability to drive the large capacitive loads offered by those power transistors.
- Avoiding high current ground loops. High current ground loops can be localized in the isolated ground plane, which protects the primary side sensitive electronics from ground bounce and switching noise. This increases the EMI/EMC performance by reducing the ground loop area.

2.1 System Block Diagram

The following system block diagram is a full bridge configuration for motor control using four sets of eGaN FET drivers.

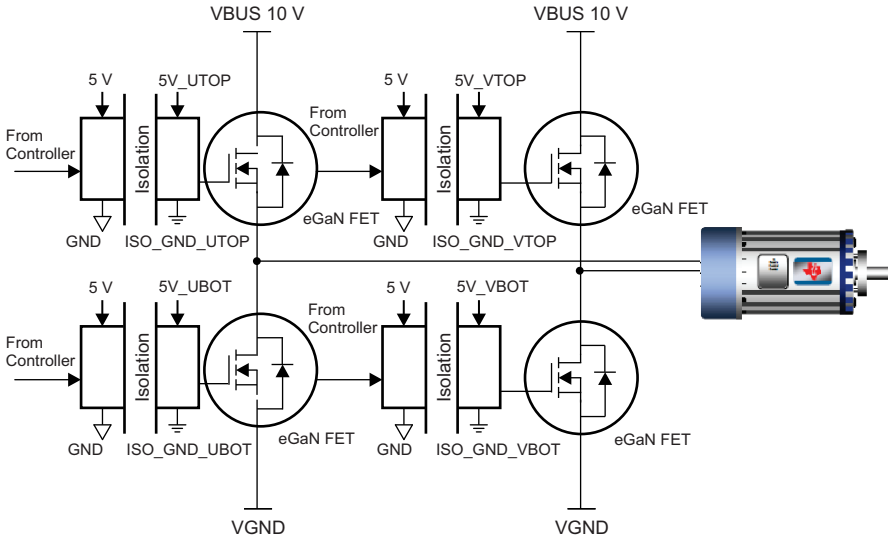


Figure 1. TIDA-00785 System Block Diagram

2.2 Functionality

This TI Design uses the SN6501 push-pull transformer driver to generate the isolated power supply for the UCC27611 GaN driver. The ISO7821F is used as a digital isolator for signals from a microcontroller to the GaN driver.

The reference design offers the following key benefits:

- High electromagnetic immunity and low missions at low power consumption while isolating CMOS or LVCMOS digital I/Os
- Small size of magnetics due to high switching speed (300 kHz) of the SN6501 transformer driver
- Drive voltage is precisely controlled to 5 V by internal regulator of the UCC27611
- Asymmetrical rail-to-rail peak current drive capability with 4-A source and 6-A sink of the UCC27611
- Turn-on and turn-off time optimization depending on GaN FET, allowed by split output configuration of the UCC27611
- Low EMI due to spread spectrum clocking of the push-pull transformer driver
- Distributed power supply architecture leading to flexibility in PCB routing

Various parameters of the design are tested and documented, like load and line regulation, efficiency of power supply, digital signal isolation, and GaN driver functionality.

3 Block Diagram

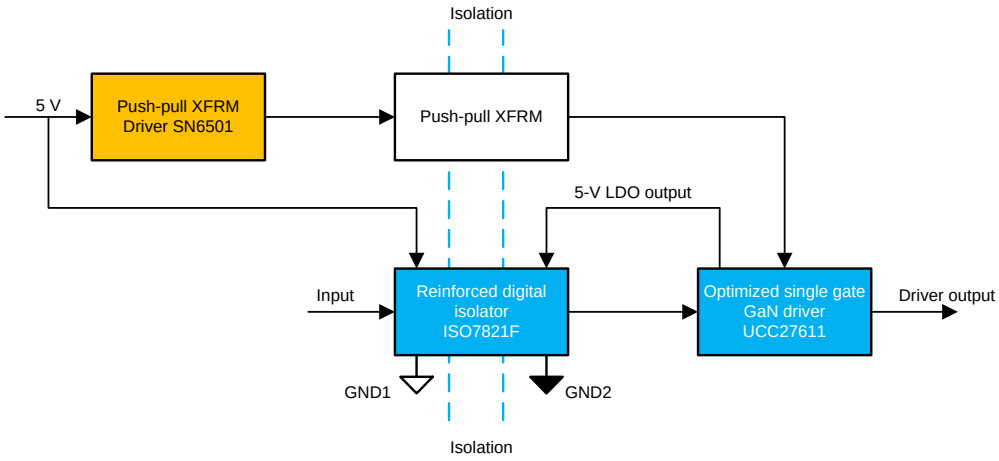


Figure 2. Isolated GaN Driver Block Diagram

The TIDA-00785 board consists of two main circuit blocks: the isolated GaN driver (ISO7821F+UCC27611) and the isolated power supply (SN6501 and transformer) for the GaN drive. The primary side of the gate driver is powered from a 5=V power supply and the secondary side (high voltage) is powered from a 5-V isolated power supply. The 5-V isolated supply is derived from a 5-V input rail with the help of a push-pull converter and LDO of the UCC27611. The converter uses the SN6501 push-pull transformer driver to drive a center-tapped transformer to generate the isolated power supply rail.

A full bridge circuit has four GaN switches; therefore, the GaN drive section needs to use four sets of the board. An individual gate drive and isolated power supply per switch helps achieve a distributed architecture, which increases the flexibility of design and PCB layout. The same design concept can be extended with six sets of boards for a three-phase circuit design.

Each board controls input PWM signals. An input signal along with a power supply can be connected to a 3-pin header. The input power supply can be connected to 2-pin header as well. The LDO in the UCC27611 is used to generate the 5-V rail from the 5-V input rail for the primary side of the isolated gate drivers.

3.1 Highlighted Products

The TIDA-00785 reference design features the following devices from Texas Instruments:

- SN6501
  - A monolithic oscillator and power driver
  - Specifically designed for small form factor
  - Low-noise, low-EMI push-pull transformer driver
  - Operates at an input range of 3.3 V at 150 mA to 5.5 V at 350 mA
  - Switches at 300 kHz, on-chip integrated ground-referenced N-channel power switches
  - –40°C to 125°C operating temperature range
  - Extremely small 5-pin SOT23 package
- ISO7821F
  - A high-performance, dual channel digital isolator with 8000-V_{PK} isolation voltage
  - High electromagnetic immunity, low emissions at low power consumption
  - Operates at an input range of 2.25- to 5.5-V input
  - Has low power consumption of 1.8 mA typically per channel at 1 Mbps, supports up to 100 Mbps
  - –55°C to 125°C operating temperature range
  - Available in both 16-pin SOIC wide-body (DW) and extra-wide body (DWW) packages
- UCC27611
  - With internal LDO, is a single-channel, high-speed, gate driver optimized for a 5-V drive
  - Specifically addressing enhancement mode GaN FETs (eGANFETs)
  - V_{REF} is precisely controlled by internal linear regulator to 5 V
  - Asymmetrical rail-to-rail peak current drive capability with 4-A source and 6-A sink
  - Split output configuration for individual turnon and turnoff time optimization
  - Fast rise and fall times (9-ns and 5-ns typical)
  - Fast propagation delay (14-ns typical)
  - Operates at a single supply range VDD of 4 to 18 V
  - –40°C to 140°C operating temperature range
  - Offered in a small 2-mm×2-mm SON-6 package (DRV) with exposed thermal and ground pad that improves the package power-handling capability

For more information on each of these devices, see their respective product folders at www.ti.com or click on the links for the product folders under Design Resources.

4 System Design Theory

Push-pull converters use center-tapped transformers to transfer power from the primary side to the secondary side. Figure 3 explains how the push-pull converter functions.

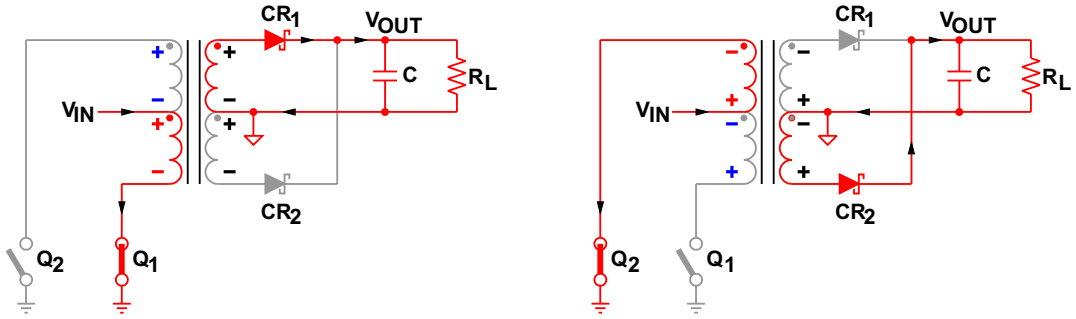


Figure 3. Push-Pull Converter Theory of Operation

When Q_1 conducts, current is sourced from V_{IN} into ground through the lower half of the primary of the transformer. This creates a negative potential at the lower half of the primary, winding with respect to the primary center tap. In order to maintain the previously established current through Q_2, which has now been opened, the upper half of the primary turns positive with respect to the center tap of the primary. This voltage is now transferred to the secondary of the transformer according to the dot convention and the turns ratio of the transformer. CR_1 is now forward biased and CR_2 is reverse biased; this in turn causes a current to flow through the upper half of the secondary, passing through CR_1 into C charging the capacitor and back into the secondary center tap.

Similarly, when Q_2 conducts voltage, polarities at the primary and secondary reverses. Now CR_1 is reverse biased and CR_2 is forward biased, which causes a current to flow from the bottom half of the secondary through CR_2 into C charging the output capacitor and back into the center tap of the transformer. Q_1 and Q_2 switch alternatively with approximately 50% duty cycle to transfer power from primary to secondary of the transformer.

Before either switch is turned ON, there must be a short time period during which both transistors are high impedance. Known as break-before-make time, this short period is required to avoid shorting out both ends of the primary.

Another important aspect to take care in push-pull designs is the transformer core magnetization. Figure 4 shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H as the magnetic field strength. When Q_1 conducts, the magnetic flux is pushed from A to A', and when Q_2 conducts, the flux is pulled back from A' to A. The difference in flux and thus flux density is proportional to the product of the primary voltage, V_P, and the time, t_{ON}. They are applied to the primary: $B = V_P \times t_{ON}$.

The volt-seconds (V-t) product is important as it determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swings result in an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps towards the saturation region.

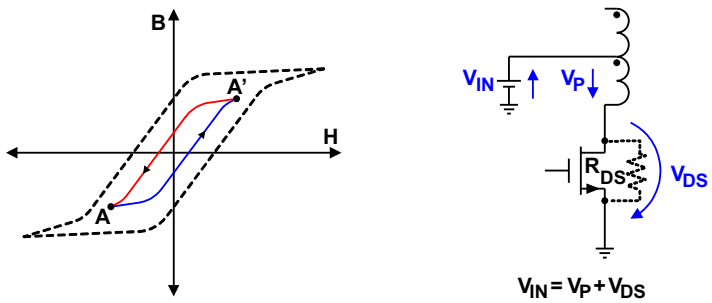


Figure 4. Push-Pull Transformer Core Magnetization and Self-Regulation Through Positive Temperature Coefficient of $R_{DS(on)}$

With SN6505 due to the positive temperature coefficient of a MOSFET's on-resistance, the output FETs of the SN6501 has a self-correcting effect on V-t imbalance. In the case of a slightly longer on-time, the prolonged current flow through a FET gradually heats the transistor, which leads to an increase in $R_{DS(on)}$. The higher resistance then causes the drain-source voltage, V_{DS}, to rise. Because the voltage at the primary is the difference between the constant input voltage, V_{IN}, and the voltage drop across the MOSFET, $V_P = V_{IN} – V_{DS}$, V_P is gradually reduced and V-t balance restored.

4.1 Design of Push-Pull Power Supply

This section describes how to design a push-pull power supply with the SN6501. The application circuit is shown in Figure 5. The power supply specifications are given in Table 2.

Table 2. Push-Pull Power Supply Specification

PARAMETER	SPECIFICATION
V_{IN}	5 V ± 5%
V_{OUT}	5 V
P_{OUT}	1 W

The design requires at least the following external discrete components: a transformer, rectifier diodes, and input and output bulk capacitors.

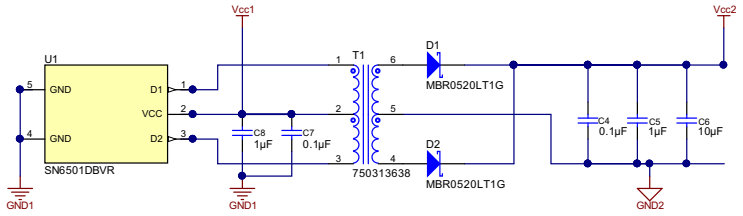


Figure 5. Isolated Power Supply Based on Push-Pull Topology

4.1.1 Rectifier Diode Selection

To increase the efficiency of the push-pull forward converter, the forward voltage drop of the secondary side rectifier diodes should be as small as possible. Also, as the SN6501 is a high frequency switching converter, the diode must possess a short recovery time. Schottky diodes are selected as they meet the requirements of low forward voltage drop and fast recovery time. The diode must also withstand a reverse voltage of twice the output voltage.

A good choice for low-voltage applications and ambient temperatures of up to 85°C is the low-cost Schottky rectifier MBR0520L with a typical forward voltage of 275 mV at a 100-mA forward current. For higher output voltages such as ±10 V and above, the MBR0530 provides a higher DC blocking voltage of 30 V.

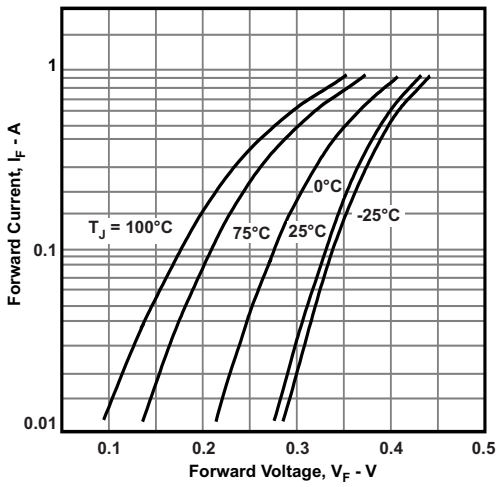


Figure 6. Diode Forward Characteristics for MBR0520L

4.1.2 Capacitor Selection

As with all high-speed CMOS ICs, the SN6501 requires a bypass capacitor in the range of 10 to 100 nF.

The input bulk capacitor at the center tap of the primary supports large currents into the primary during the fast switching transients. For minimum ripple, make this capacitor 1 to 10 µF. In a two-layer PCB design with a dedicated ground plane, place this capacitor close to the primary center tap to minimize trace inductance. In a four-layer board design with low-inductance reference planes for ground and V_{IN}, place the capacitor at the supply entrance of the board. To ensure low-inductance paths, use two vias in parallel for each connection to a reference plane or to the primary center tap.

The bulk capacitor at the rectifier output evens out the output voltage. Set this capacitor 1 to 10 µF. The small capacitor at the regulator input is not necessarily required. However, good analog design practice suggests using a small value of 47 to 100 nF improves the regulator's transient response and noise rejection.

The LDO output capacitor buffers the regulated output for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the datasheet. However, in most cases, a low-ESR ceramic capacitor in the range of 4.7 to 10 µF will satisfy these requirements.

4.1.3 Transformer Selection

Table 3 lists the required specifications of the push-pull transformer. V-t products and turns ratio calculations are explained in the subsequent sections.

Table 3. Transformer Requirements

PARAMETER	SPECIFICATION
Output power	1 W
Output voltage	5 V
Input voltage	5 V
Minimum operating frequency	300 kHz
Working voltage	1500-V DC
Minimum creepage distance	9.2 mm (as per IEC61800-5-1)
Minimum clearance distance	8 mm (as per IEC61800-5-1)
Insulation	Reinforced
Operating temperature range	–40ºC to 125ºC

4.1.3.1 V-t Product Calculation

To prevent a transformer from saturation, its V-t product must be greater than the maximum V-t product applied by the SN6501. The maximum voltage delivered by the SN6501 is the nominal converter input plus 10%. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the transformer's minimum V-t product is determined through Equation 1:

$$Vt_{min} \geq V_{IN\_max} \times \frac{T_{max}}{2} = \frac{V_{IN\_max}}{2 \times f_{min}} \quad (1)$$

Inserting the numeric values from the datasheet into Equation 1 yields the minimum V-t products of $Vt_{min} \geq \frac{5.5\ V}{2 \times 300\ kHz} = 9.1\ V\mu s$ for 5-V applications.

Common V-t values for low-power center-tapped transformers range from 22 to 150 Vµs with typical footprints of 10 mm x 12 mm. However, transformers specifically designed for PCMCIA applications provide as little as 11 Vµs and come with a significantly reduced footprint of 6 mm x 6 mm.

While Vt-wise all of these transformers can be driven by the SN6501, consider other important factors such as isolation voltage, transformer wattage, and turns ratio before making the final decision.

4.1.3.2 Turns Ration Estimate

Assume the rectifier diodes and linear regulator have been selected. Also, the transformer chosen must have a V-t product of at least 11 Vμs. However, before searching the manufacturer websites for a suitable transformer, the user still needs to know its minimum turns ratio that allows the push-pull converter to operate flawlessly over the specified current and temperature range. This minimum transformation ratio is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer's typical efficiency of 97% into account:

$$V_{P\_min} = V_{IN\_min} - V_{DS\_max} \quad (2)$$

V_{S_min} must be large enough to allow for a maximum voltage drop, V_{F_max}, across the rectifier diode and still provide sufficient input voltage for the regulator to remain in regulation. From the LDO criterion, this minimum input voltage is known and by adding V_{F_max} gives the minimum secondary voltage with:

$$V_{S\_min} = V_{F\_max} + V_{DO\_max} + V_{O\_max} \quad (3)$$

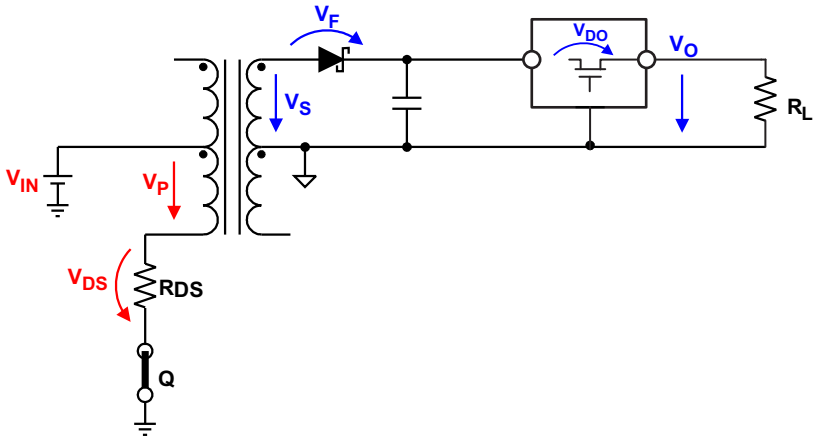


Figure 7. Establishing the Required Minimum Turns Ratio Through $N_{min} = 1.031 \times V_{S\_min} / V_{P\_min}$

Then calculating the available minimum primary voltage, V_{P_min}, involves subtracting the maximum possible drain-to-source voltage of the SN6501, V_{DS_max}, from the minimum converter input voltage V_{IN_min}:

$$V_{P\_min} = V_{IN\_min} - V_{DS\_max} \quad (4)$$

V_{DS_max}, however, is the product of the maximum $R_{DS(on)}$ and ID values for a given supply specified in the SN6501 datasheet:

$$V_{DS\_max} = R_{DS\_max} \times I_{D\_max} \quad (5)$$

Then inserting Equation 5 into Equation 4 yields:

$$V_{P\_min} = V_{IN\_min} - R_{DS\_max} \times I_{D\_max} \quad (6)$$

Inserting Equation 6 and Equation 3 into Equation 2 provides the minimum turns ration with:

$$n_{min} = 1.031 \times \frac{V_{F\_max} + V_{DO\_max} + V_{O\_max}}{V_{IN\_min} - R_{DS\_max} \times I_{D\_max}} \quad (7)$$

For example, for a 5-V_{IN} to 5-V_{OUT} converter using the rectifier diode MBR0520L and the 5-V LDO inside the UCC27611, the datasheet values taken for a load current of 50 mA are V_{F_max} = 0.2 V, V_{DO_max} = 0.05 V, and V_{O_max} = 5.075 V.

Then assuming that the converter input voltage is taken from a 5.0-V controller supply with a maximum ±2% accuracy makes V_{IN_min} = 4.9 V. Finally, the maximum values for drain-source resistance and drain current at 5.0 V are taken from the SN6501 datasheet with R_{DS_max} = 2 Ω and I_{D_max} = 350 mA.

Inserting the values above into Equation 7 yields a minimum turns ratio of:

$$n_{min} = 1.031 \times \frac{0.2\ V + 0.05\ V + 5.075\ V}{4.9\ V - 2\ \Omega \times 350\ mA} = 1.30$$

This TI Design uses a Würth Electronics transformer, 750313638. Table 4 provides the specifications of this transformer:

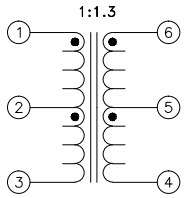


Figure 8. Push-Pull Transformer - 750313638 (Würth Electronics)

Table 4. Selected Transformer Specifications

PARAMETER	SPECIFICATION
Turns ratio (6 – 4):(1 – 3)	1.3 : 1, ±2 %
DC resistance (1 – 3)	0.33 W max at 20ºC
DC resistance (6 – 4)	0.33 W max at 20ºC
Inductance (1 – 2)	340 µH min at 100 kHz, 10 mVAC
Dielectric (1 – 6)	500 $0V_{RMS}$, 1 minute
Operating temperature range	–40ºC to 125ºC
Creepage distance (IEC61800-5-1)	9.2 mm
Clearance distance (IEC61800-5-1)	8 mm
Transformer dimensions	12.7 mm × 9.14 mm × 7.62 mm (see Figure 9)

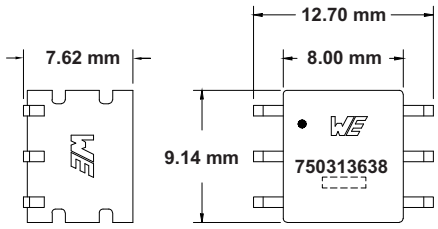


Figure 9. Transformer Dimensions in mm

4.2 Isolated GaN Driver Design

Four gate drivers are required to drive the four power switches in full bridge configuration. The requirements for individual GaN drivers are listed in Table 5.

Table 5. GaN Driver Specifications

PARAMETER	SPECIFICATION
Primary side input voltage	5.0 V ± 5 %
Secondary side input voltage	5.0 V ± 2 V
Gate drive source current capacity	4.0 A max
Gate drive sink current capacity	6.0 A max
Maximum output switching frequency	1Mhz
Maximum secondary side output power	1 W
Maximum output power to gate	0.85 W

The ISO7821F and the UCC27611 are selected as the reinforced digital isolator and GaN driver, respectively; both devices fit all the requirements in Table 5. Figure 10 shows the implementation of the reinforced digital isolator ISO7821F along with the GaN driver UCC27611.

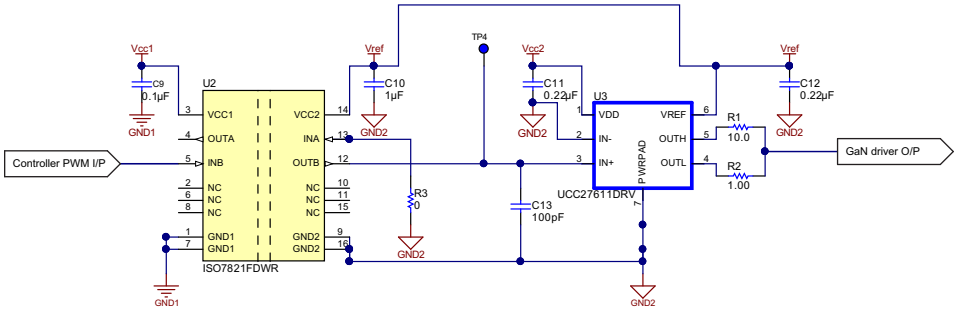


Figure 10. Isolated GaN Driver Circuit

The steps for gate driver component selection are described in Section 4.2.1 and Section 4.2.2.

4.2.1 Power Supply Capacitors

The primary side of the ISO7821F is powered from a 5-V supply, which may also be used to power the microcontroller. This 5-V rail is filtered by multiple capacitors before connecting to the isolator power supply.

The secondary side of the ISO7821F is powered from a 5-V isolated supply rail, which is generated from the push-pull power stage and V_{REF} output from the UCC27611 as described in section 4.1. A 1-µF bulk capacitor is suggested to connect next to VCC2 pin. The gate source current is drawn from this power pin and the 1-µF bulk capacitor provides this large transient current during the switching transient until power supply capacitors starts supplying the current. Also, a 0.22-µF high frequency noise decoupling capacitor is recommended on VCC2.

4.2.2 Gate Resistor Selection

Selecting a gate resistor selection is a very important part of designing the GaN driver. The value of the gate resistor affects the following parameters:

- GaN turn ON and turn OFF times
- Switching losses
- dv/dt across the GaN collector to emitter
- di/dt of the GaN current
- EMI due to GaN switching

Increasing the value of the gate resistor increases the turn-on and turn-off times of the GaN, which in turn reduces the dv/dt and di/dt, resulting in reduced EMI. However, this increases the switching losses. Decreasing the gate resistance has the opposite effect. Please see Section 8.2 of the UCC27611 datasheet for further details on calculations.

5 Getting Started Hardware

5.1 Board Description

Figure 11 shows the size of the isolated GaN drive solution and the size of individual gate driver section. The board measures at 1.46 cm × 3.12 cm.

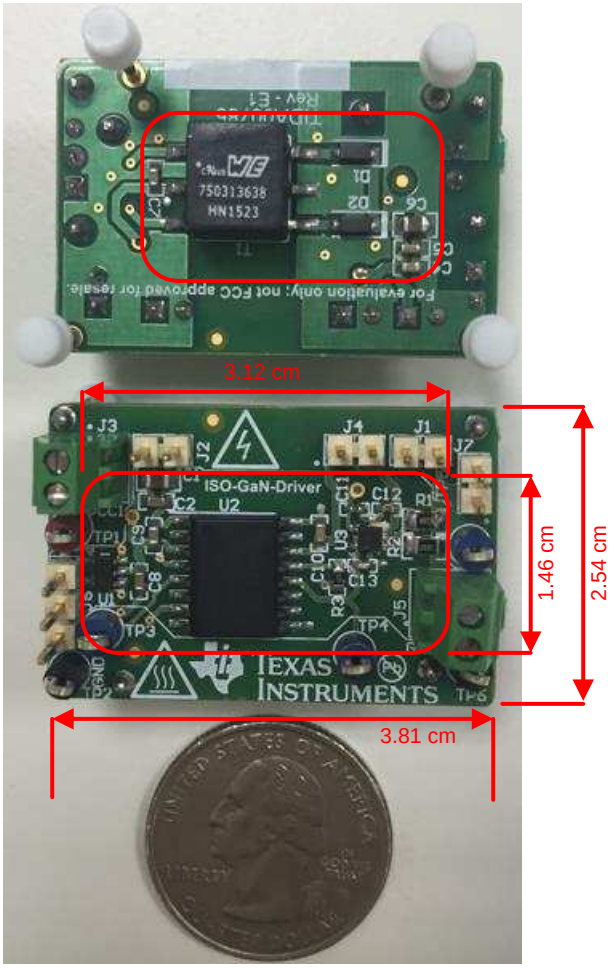


Figure 11. Complete PCB Board Size and Solution Size

Figure 12 shows the location of the subsections in the block diagram (Figure 2) on the actual board. The isolated GaN driver is placed directly underneath the isolated power supply section.

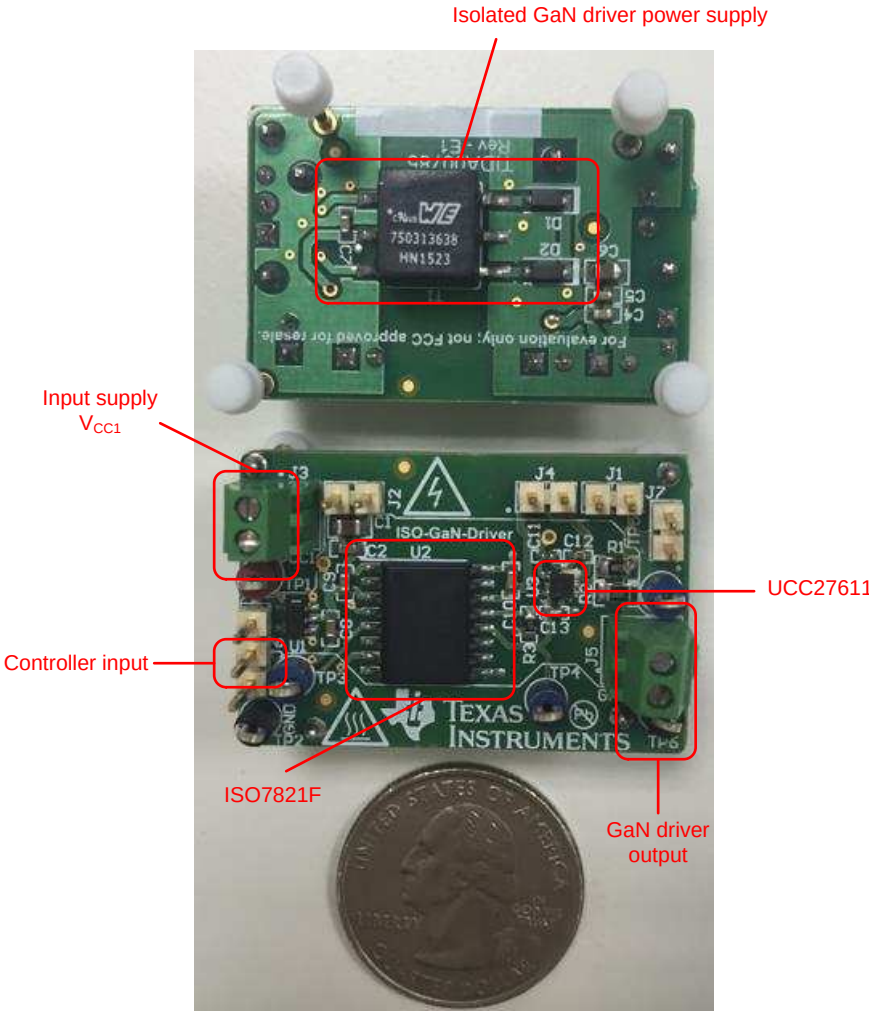


Figure 12. PCB Top and Bottom Sections

5.2 Connectors Description

Connections are as given in Figure 1, Figure 10, and Figure 12. Power supply inputs are given according to Table 6:

Table 6. Interface Connector

CONNECTOR	PIN NAME	I/O	DESCRIPTION
J3	1, 2	I	Power supply input
J6	2	I	Controller PWM input
J5	1, 2	O	GaN driver output

6 Test Setup

Figure 13 shows the test setup.

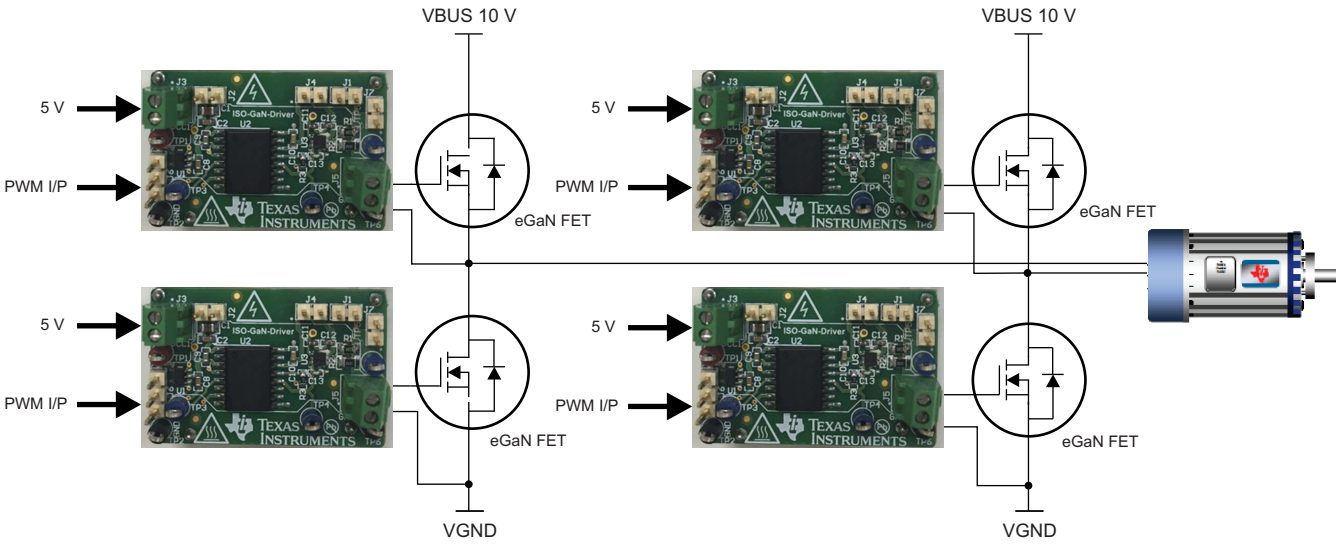


Figure 13. Test Setup

7 Test Data

7.1 PWM Signal of 1 MHz — GaN Driver Output

Figure 14 shows the GaN driver output with a PWM signal of 1 MHz.

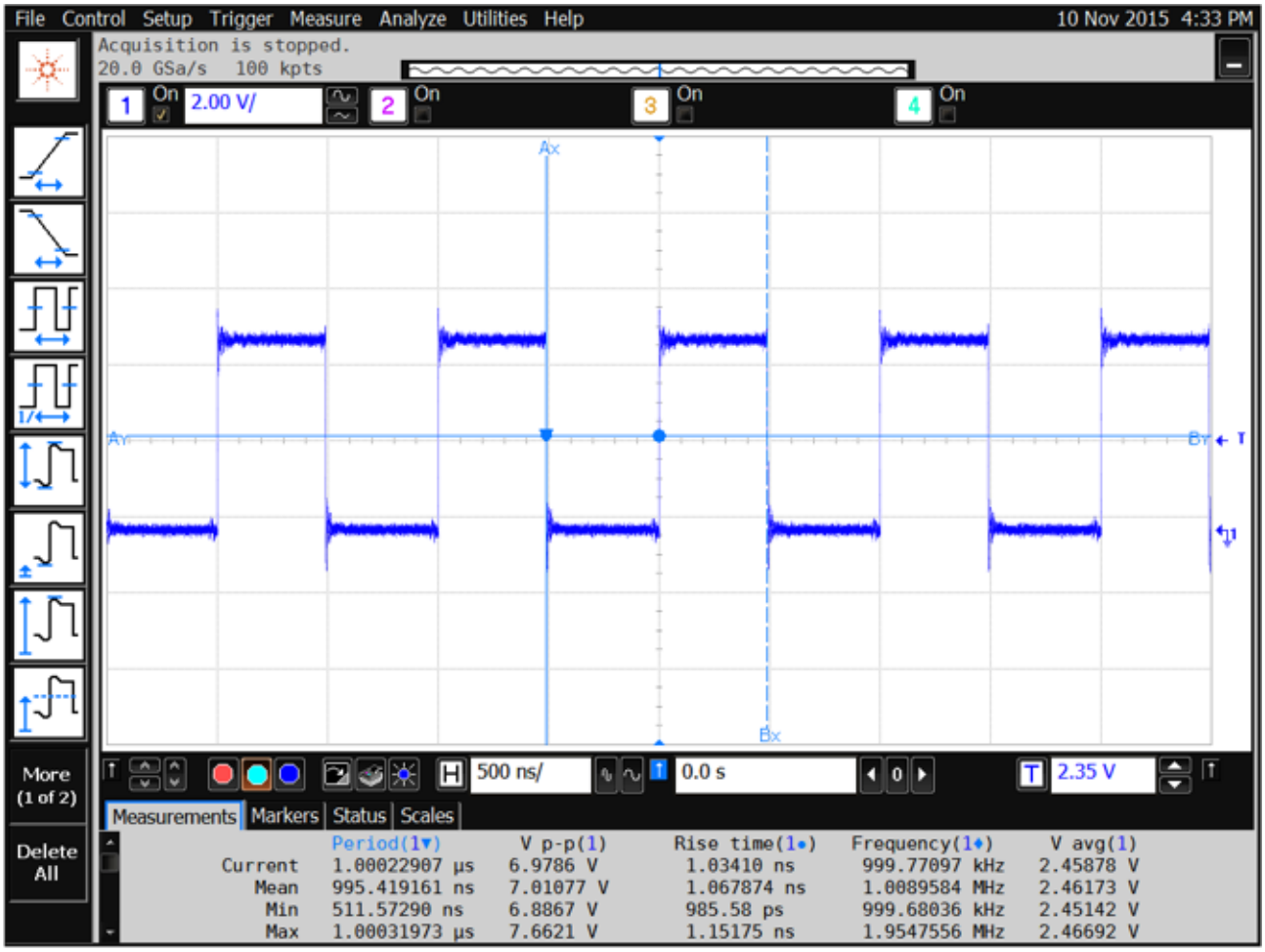


Figure 14. GaN Driver Output With 1-MHz Input

7.2 PWM Signal of 1 kHz at 50% Duty Cycle

Figure 15 shows the GaN Driver output in a half bridge configuration with a PWM signal of 1 kHz at 30% duty cycle.

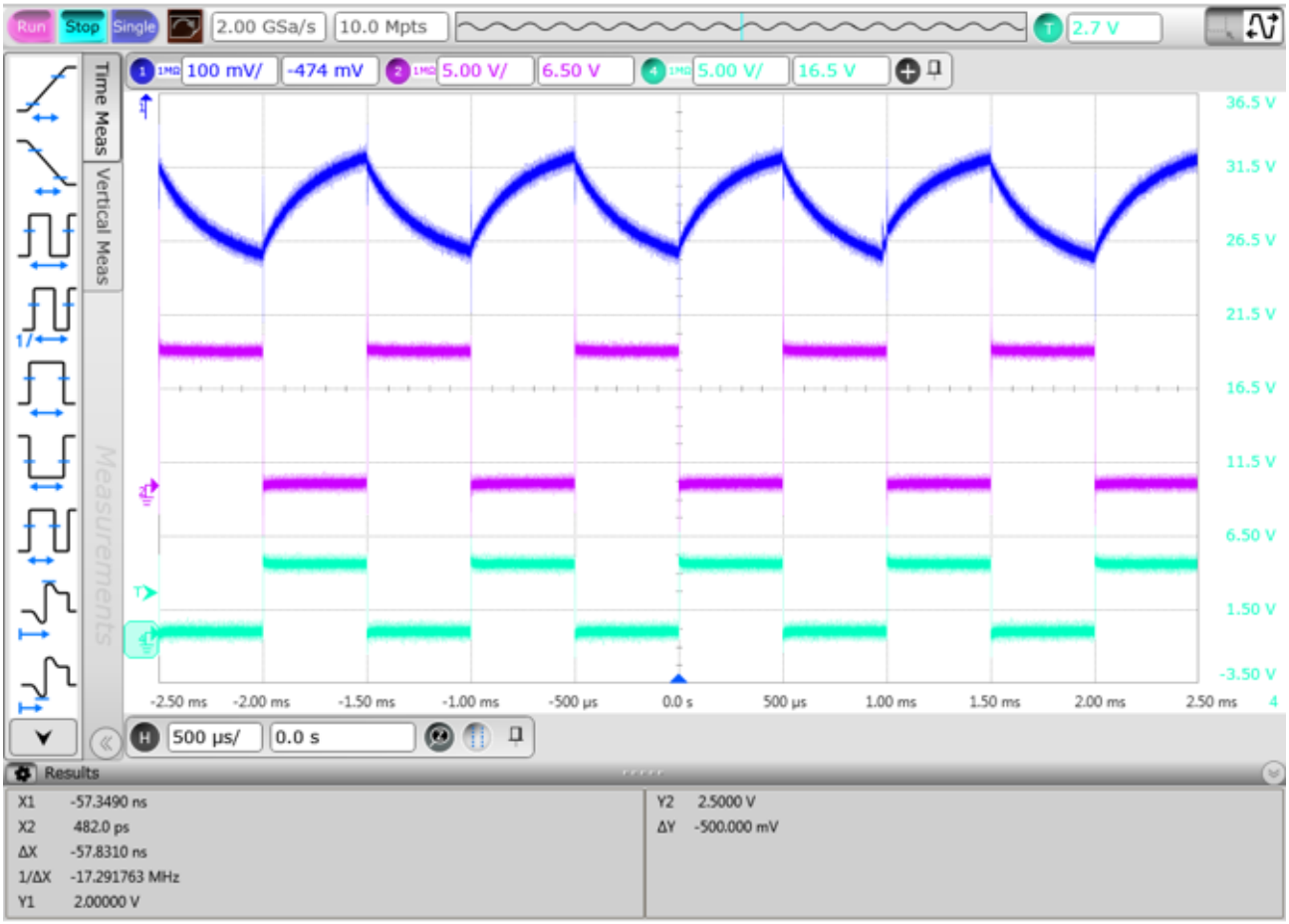


Figure 15. Half-Bridge Configuration With PWM Signal 1 kHz at 50% Duty Cycle

7.3 PWM Signal at 30% Duty Cycle

Figure 16 shows the GaN driver output with a PWM signal at 30% duty cycle.

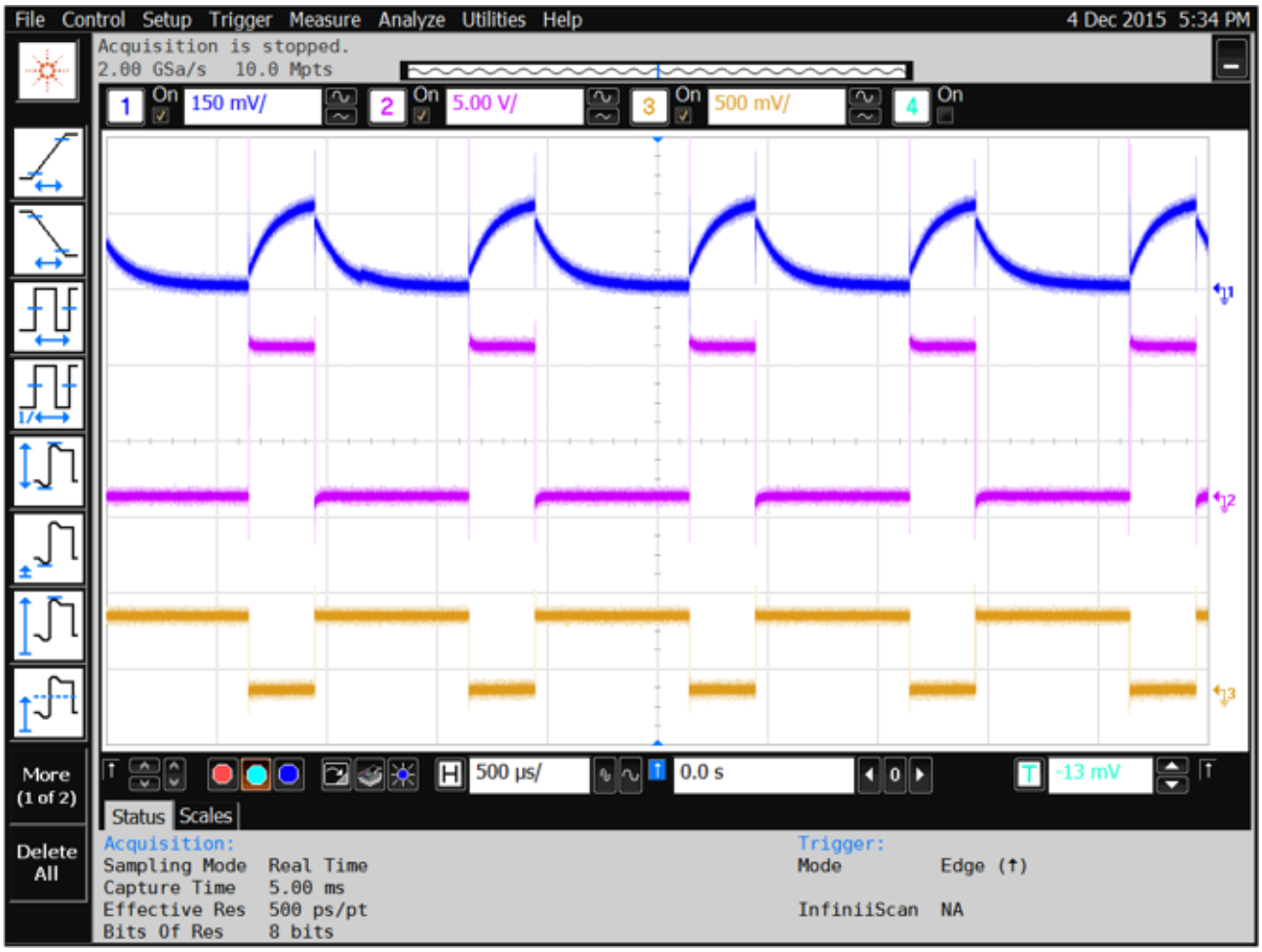


Figure 16. H-Bridge Configuration With 30% Duty Cycle Input

7.4 PWM Signal at 70% Duty Cycle

Figure 17 shows the GaN Driver output with a PWM signal at 70% duty cycle.

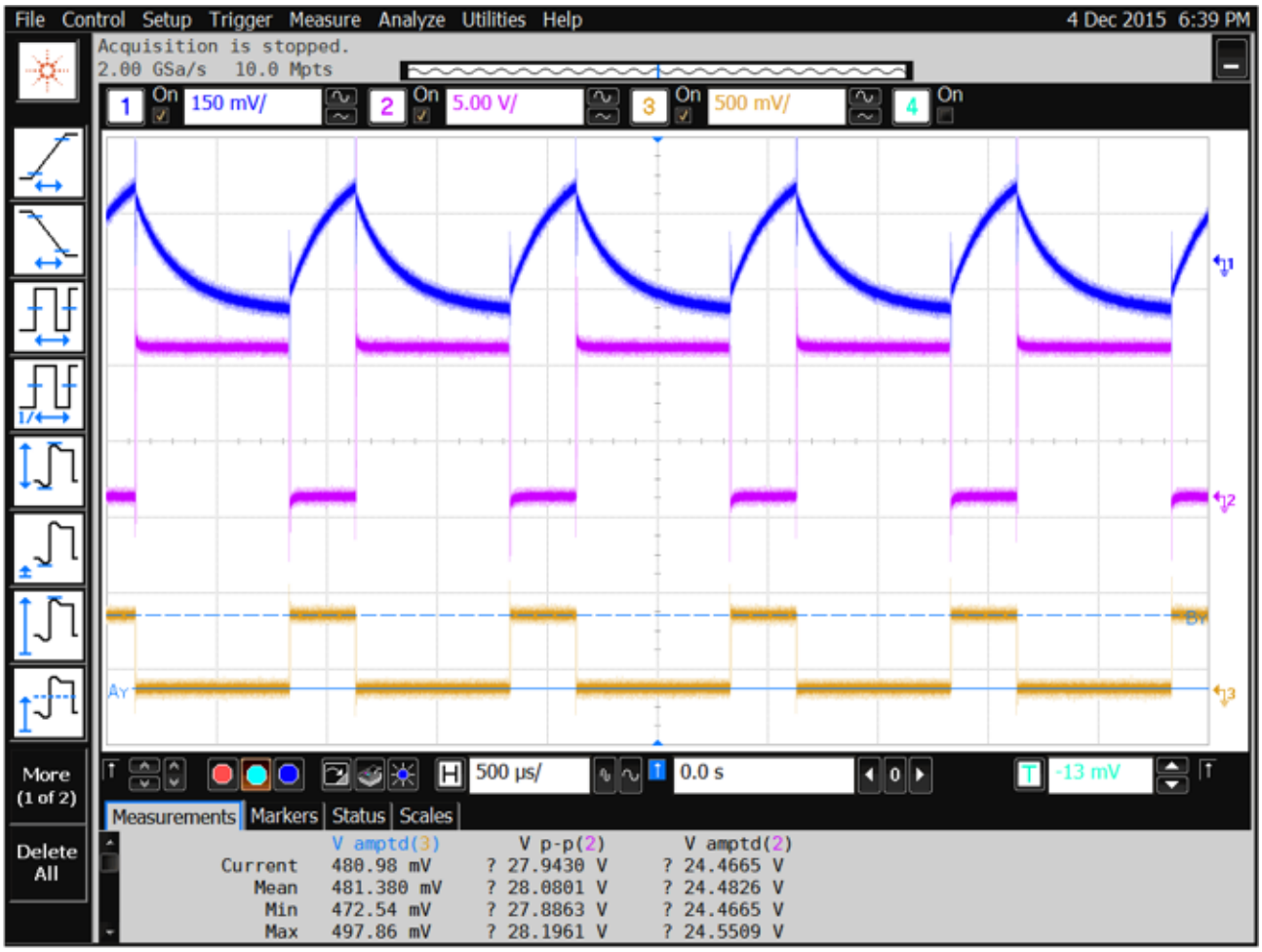


Figure 17. H-Bridge Configuration With 70% Duty Cycle Input

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00785.

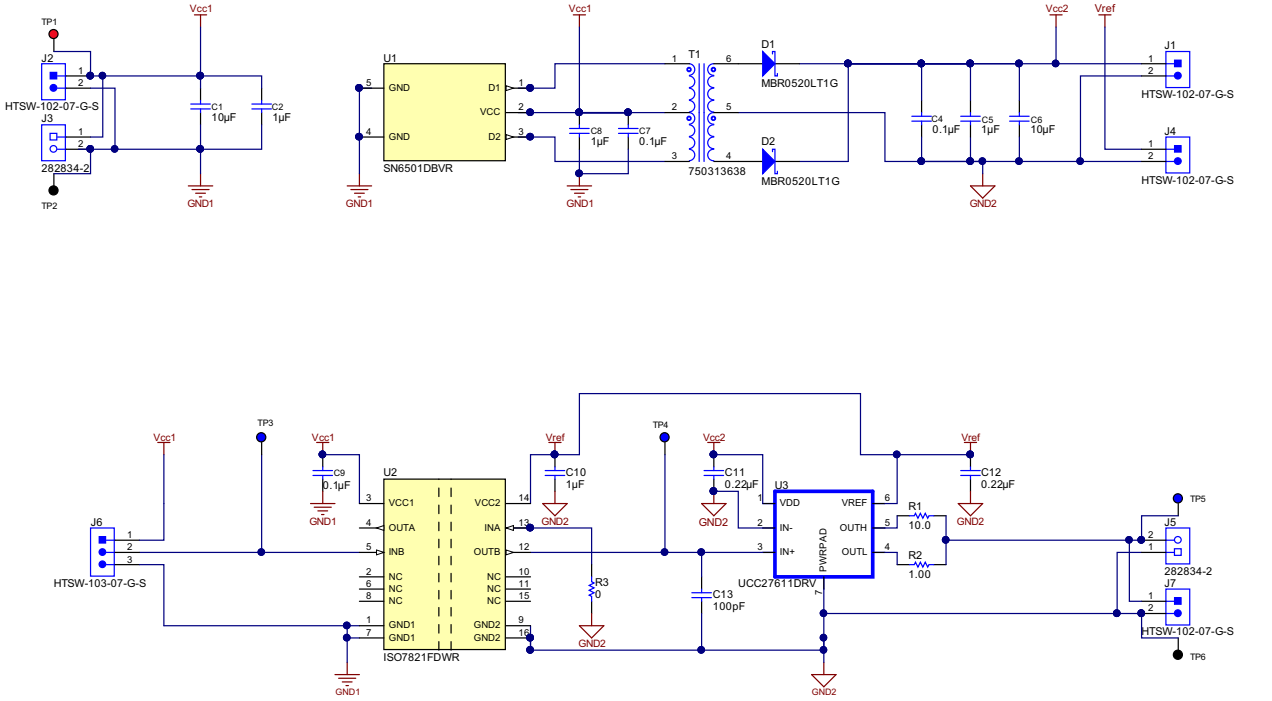


Figure 18. Isolation GaN Driver Schematic

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00785.

Table 7. BOM

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE / VALUE	FITTED
1	!PCB1	Printed Circuit Board	Any	TIDA-00785		Fitted
2	C1, C6	CAP, CERM, 10 µF, 35 V, +/- 10%, X5R, 0805	MuRata	GRM21BR6YA106KE43L	0805/10uF	Fitted
3	C2, C5, C8	CAP, CERM, 1 µF, 50 V, +/- 10%, X5R, 0603	MuRata	GRM188R61H105KAALD	0603/1uF	Fitted
3	C4, C7, C9	CAP, CERM, 0.1 µF, 25 V, +/- 5%, X7R, 0603	AVX	06033C104JAT2A	0603/0.1uF	Fitted
1	C10	CAP, CERM, 1 µF, 25 V, +/- 10%, X5R, 0603	MuRata	GRM188R61E105KA12D	0603/1uF	Fitted
2	C11, C12	CAP, CERM, 0.22 µF, 16 V, +/- 10%, X7R, 0402	TDK	C1005X7R1C224K050BC	0402/0.22uF	Fitted
1	C13	CAP, CERM, 100 pF, 25 V, +/- 5%, C0G/NP0, 0402	Kemet	C0402C101J3GACTU	0402/100pF	Fitted
2	D1, D2	Diode, Schottky, 20 V, 0.5 A, SOD-123	ON Semiconductor	MBR0520LT1G	SOD-123/20V	Fitted
0	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A		Not Fitted
3	FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A		Fitted
4	J1, J2, J4, J7	Header, 100mil, 2x1, Gold, TH	Samtec	HTSW-102-07-G-S		Fitted
2	J3, J5	Terminal Block, 2x1, 2.54mm, TH	TE Connectivity	282834-2		Fitted
1	J6	Header, 100mil, 3x1, Gold, TH	Samtec	HTSW-103-07-G-S		Fitted
4	M1, M2, M3, M4	CONN PC PIN CIRC 0.040DIA TIN	Keystone	11073		Fitted
1	R1	RES, 10.0, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080510R0FKEA	0805/10.0	Fitted
1	R2	RES, 1.00, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08051R00FKEA	0805/1.00	Fitted
1	R3	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603/0	Fitted
1	T1	Transformer, 340 uH, SMT	Wurth Elektronik	750313638	SMT/340uH	Fitted
1	TP1	Test Point, Compact, Red, TH	Keystone	5005	Red	Fitted
2	TP2, TP6	Test Point, Compact, Black, TH	Keystone	5006	Black	Fitted
3	TP3, TP4, TP5	Test Point, Compact, Blue, TH	Keystone	5122	Blue	Fitted
1	U1	Transformer Driver for Isolated Power Supplies, DBV0005A	Texas Instruments	SN6501DBVR		Fitted
1	U2	High-Performance, 8000 VPK Reinforced Dual Channel Digital Isolator, DW0016B	Texas Instruments	ISO7821FDWR		Fitted
1	U3	IC, 4A/8A Single Channel High-Speed Low-Side Gate Drivers	TI	UCC27611DRV	UCC27611DRV	Fitted

8.3 PCB Layout Recommendations

Layout is very important for proper and reliable operation of the circuit. Keep the switching loops to a minimum to reduce EMI.

8.3.1 Layout Recommendations for SN6501 Based Push-Pull Power Supply

- SN6501 switches at 300 kHz. To reduce loop inductance and EMI, keep the minimum area the switching loops on both the input and output sides as shown in Figure 19 and Figure 20.

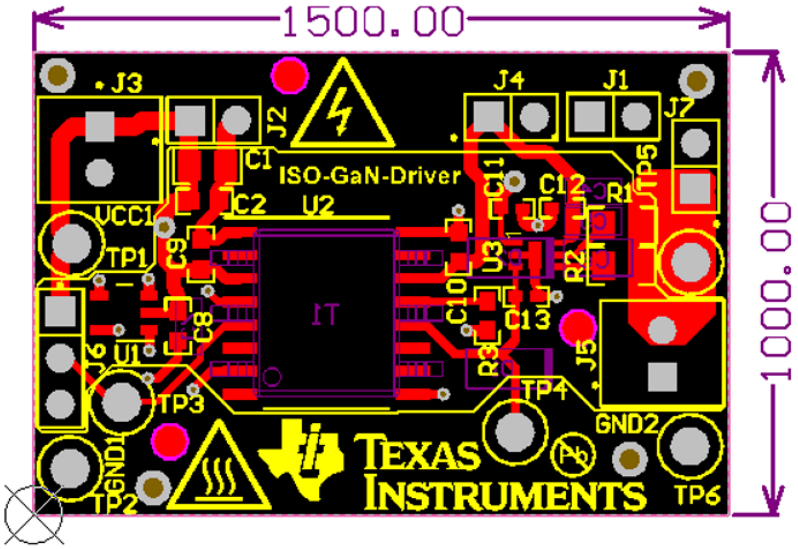


Figure 19. Top Layer Layout

- Place U1 of the SN6501 very close to the transformer T1.
- Keep capacitors C7 and C8 close to the U1 and T1 power pins and GND.
- Place capacitors C4, C5, and C6 to the power planes to provide a low inductance connection to the power planes.

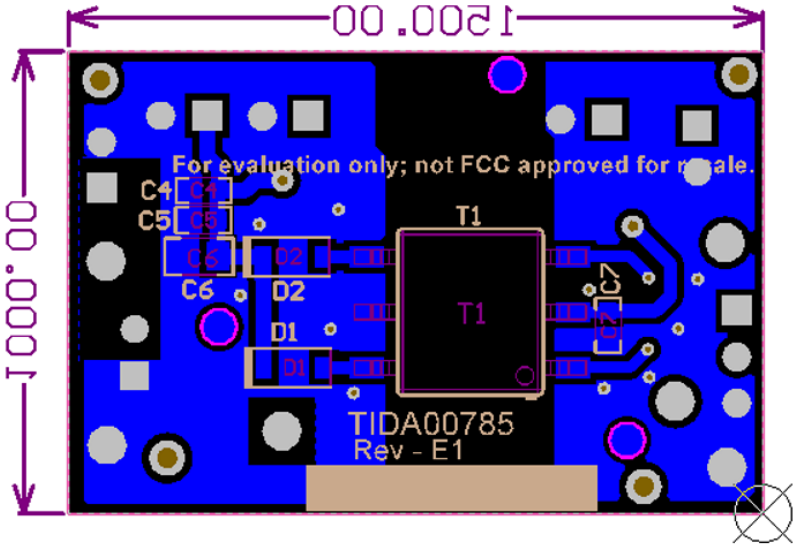


Figure 20. Bottom Layer Layout

8.3.2 Layout Recommendations for ISO7821F Digital Isolator and UCC27611 GaN Driver

- Place the 0.1-µF bulk capacitor C9 close to the power supply pin of the ISO7821F.
- Place the 0.22-µF bulk capacitors C11 and C12 close to the power supply pin of the UCC27611.
- Keep R1 and R2 close to the UCC27611 to keep this loop area also to a minimum.

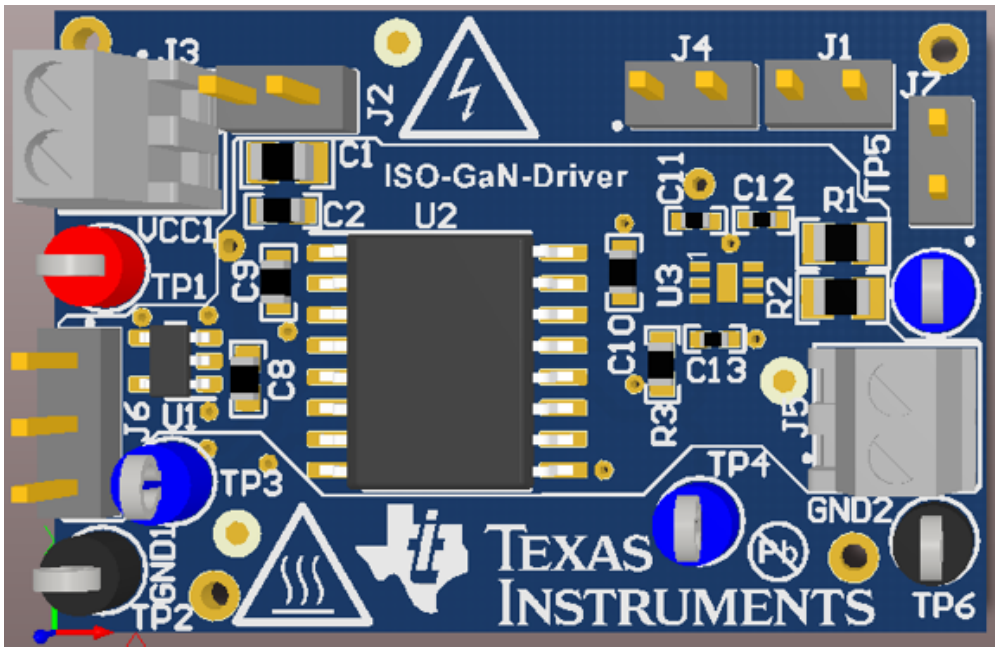


Figure 21. Top Board View

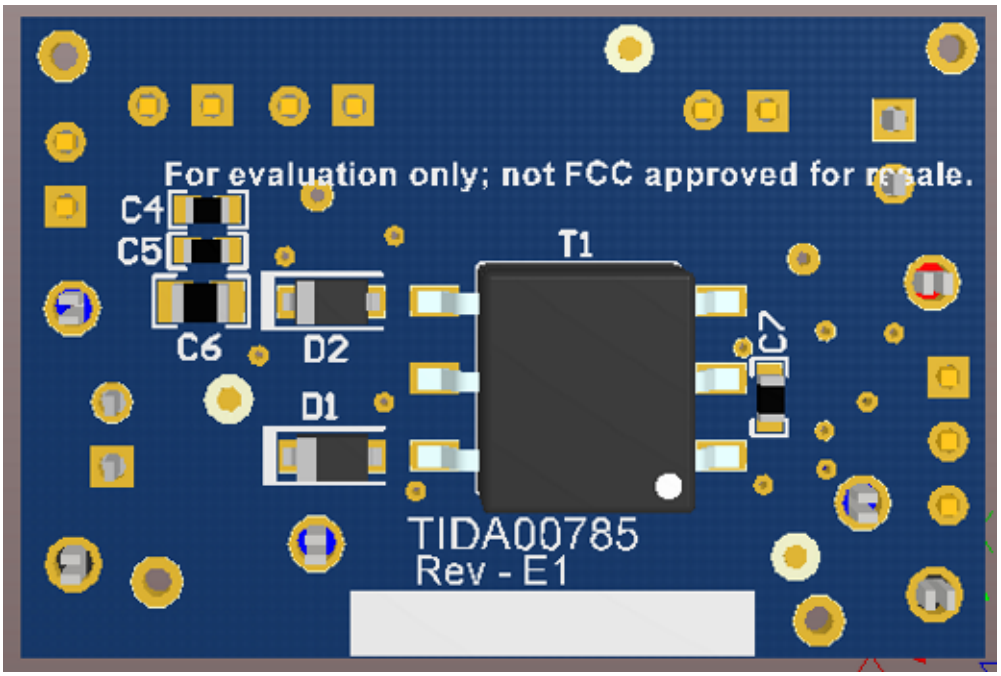


Figure 22. Bottom Board View

8.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-00785.

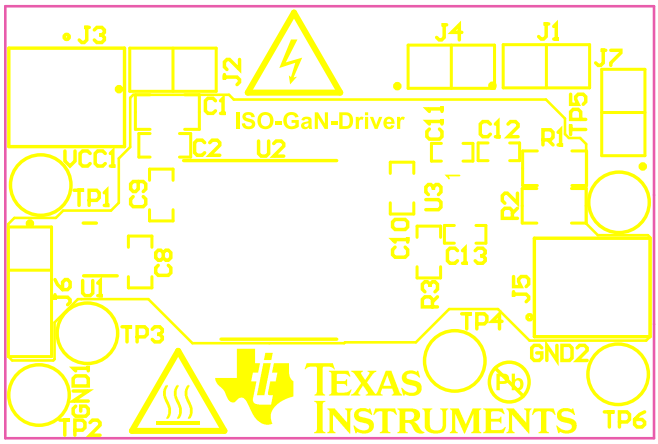


Figure 23. Top Silk Screen

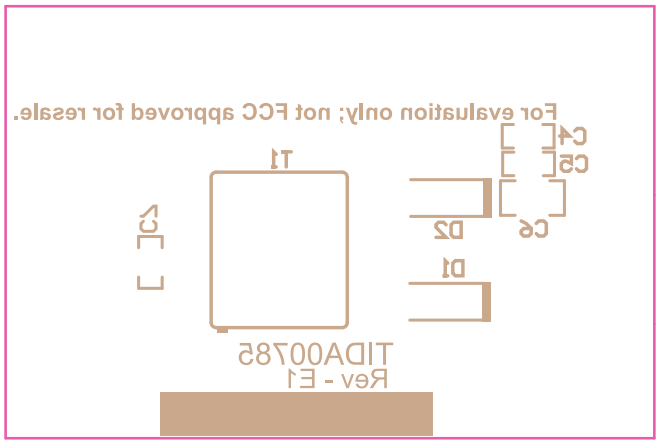


Figure 24. Bottom Silk Screen

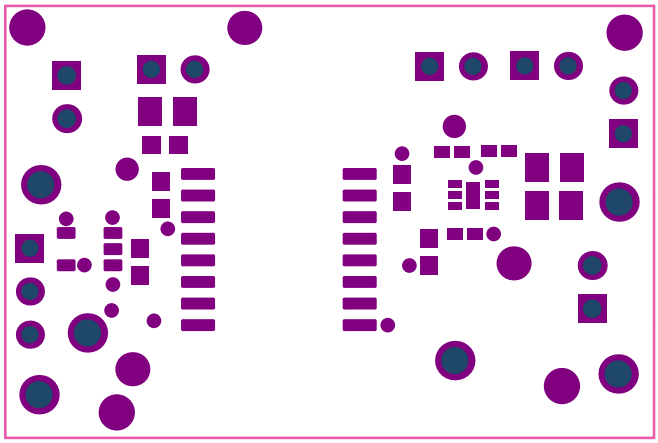


Figure 25. Top Solder Mask

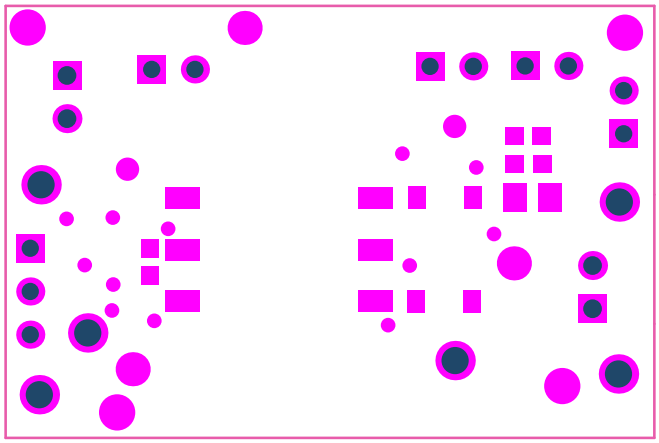


Figure 26. Bottom Solder Mask

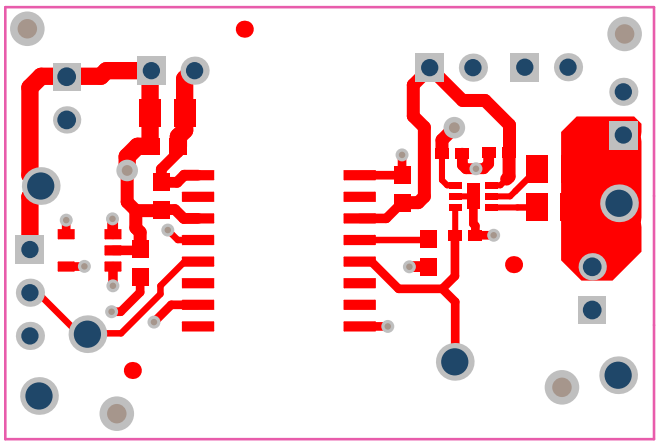


Figure 27. Top Layer Layout

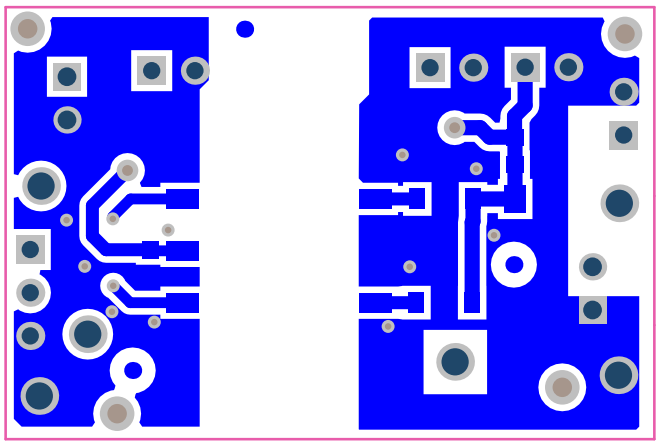


Figure 28. Bottom Layer Layout

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00785.

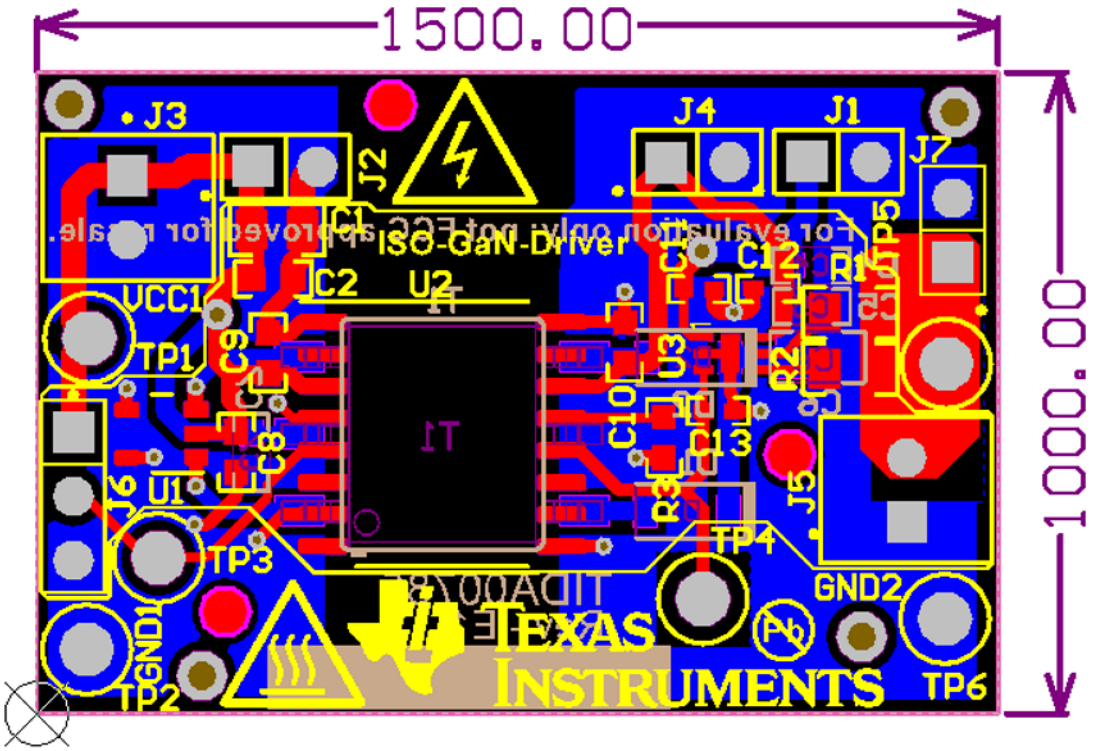


Figure 29. Altium Project PCB Layout

8.5 Layout Guidelines

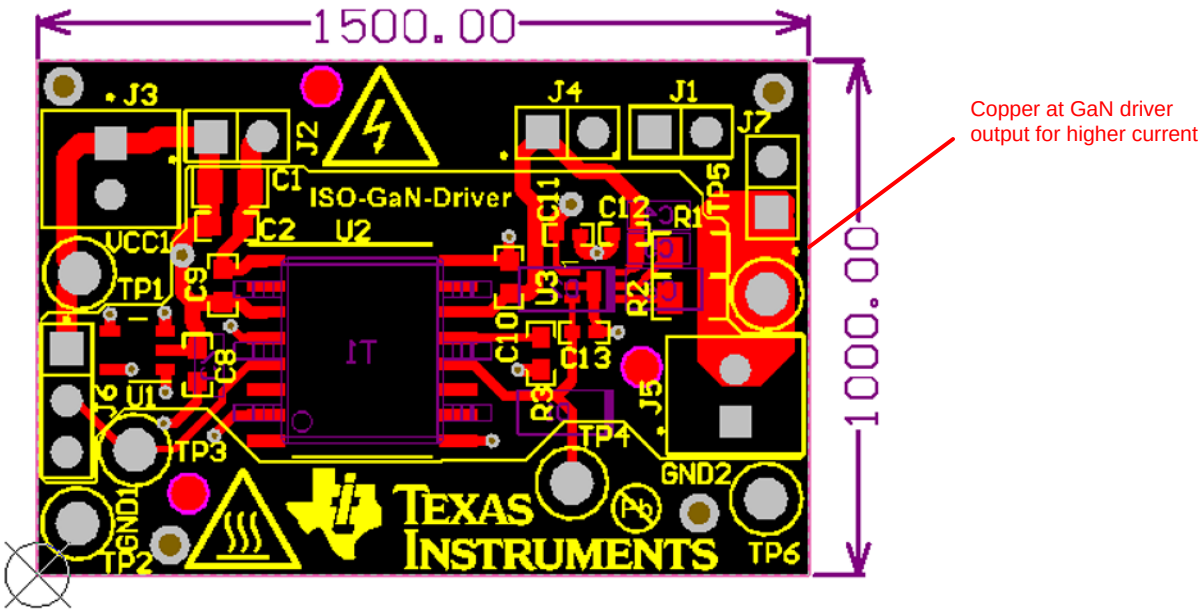


Figure 30. Top Layout Guidelines

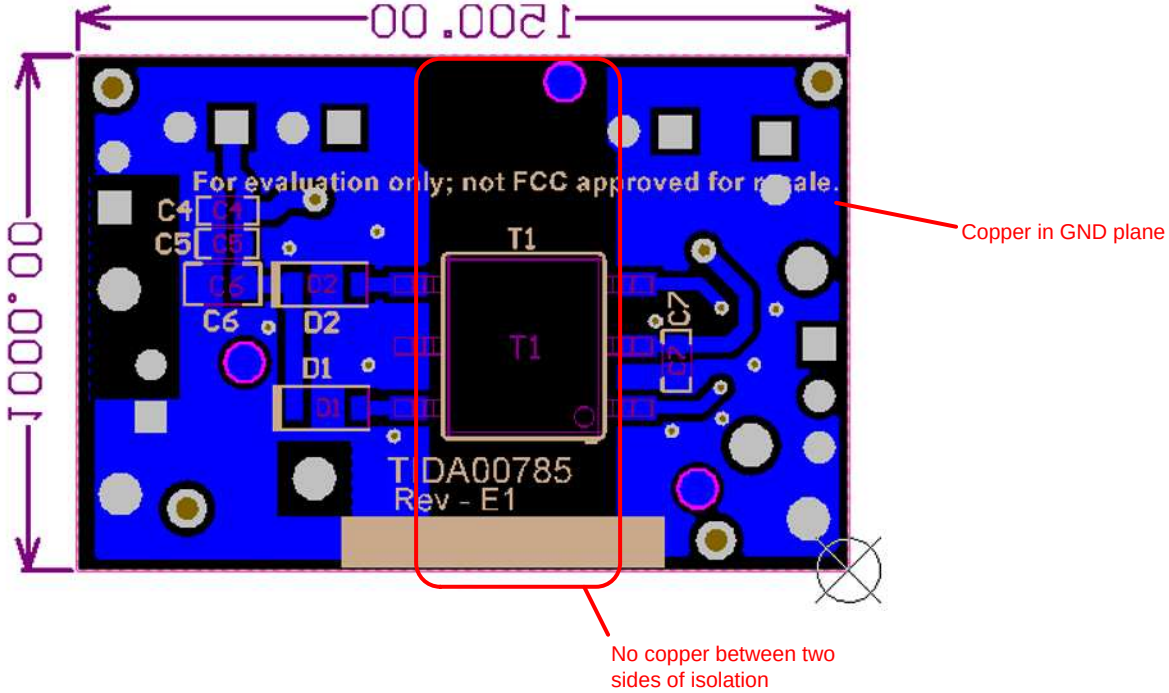


Figure 31. Bottom Layout Guidelines

8.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00785.

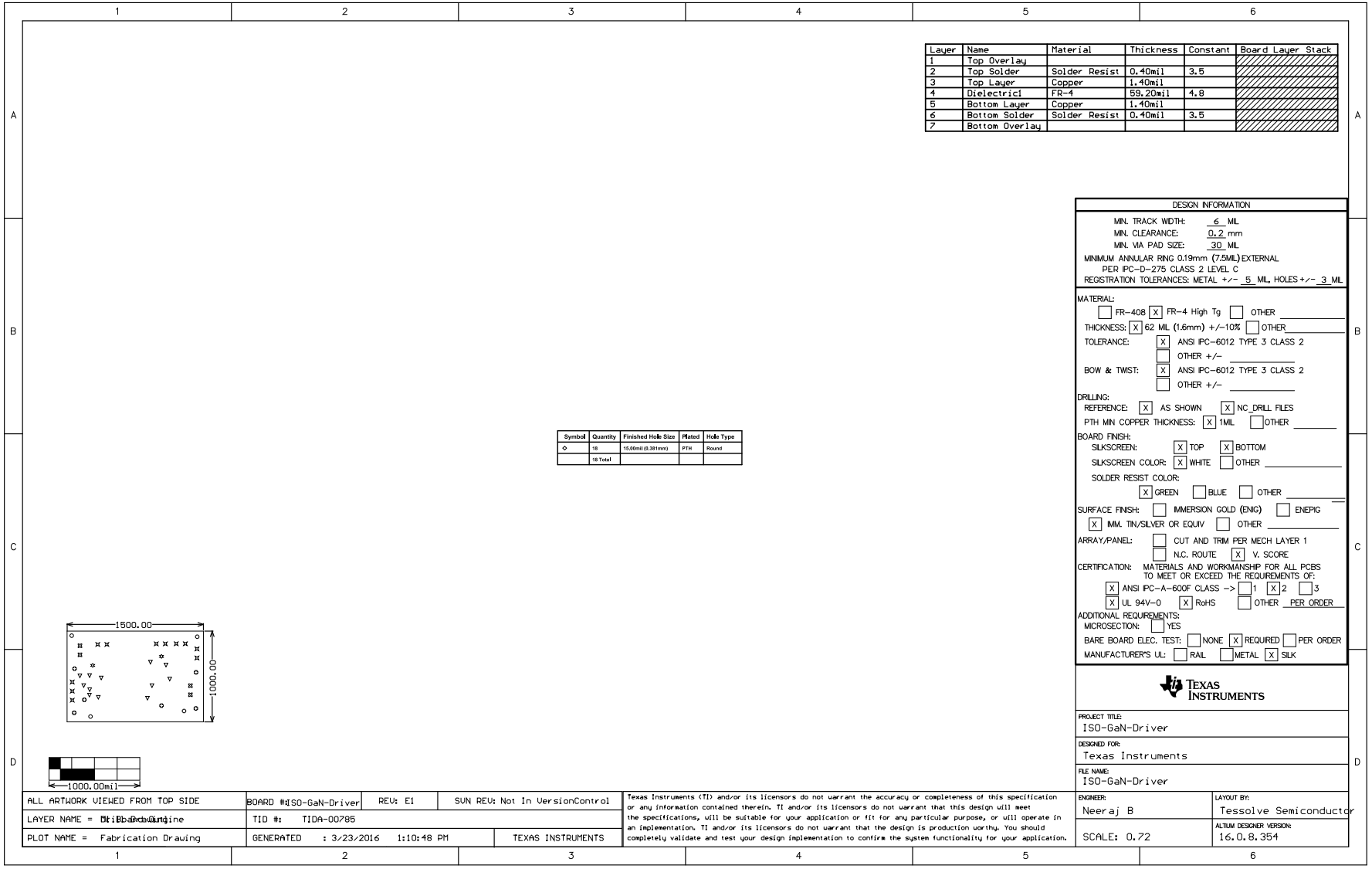


Figure 32. Fabrication Drawing

8.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00785.

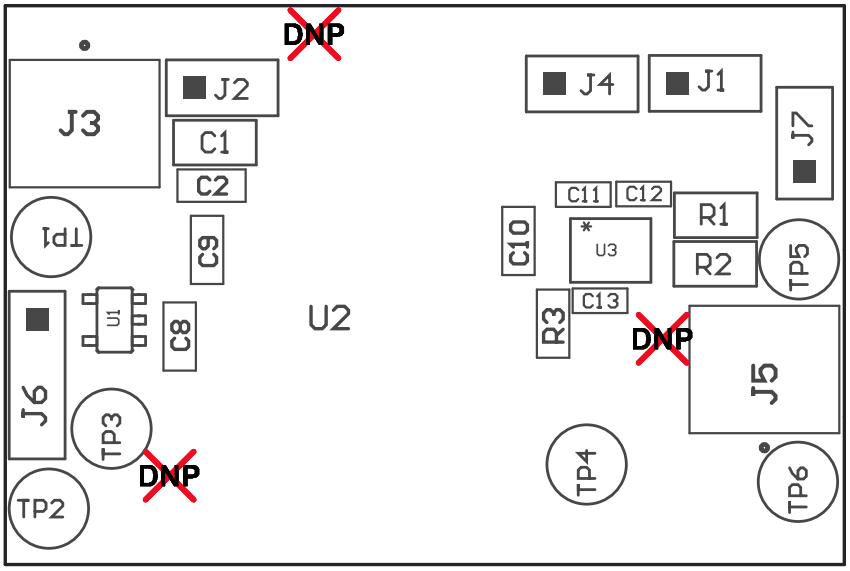


Figure 33. Top Assembly Drawing

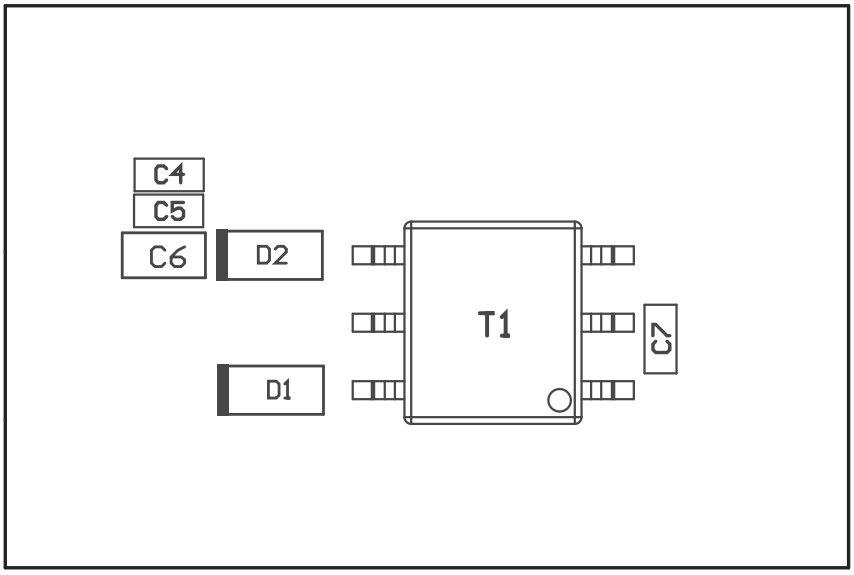


Figure 34. Bottom Assembly Drawing

9 References

1. Texas Instruments, *High-voltage reinforced isolation: Definitions and test methodologies*, Marketing White Paper (SLYY063)
2. Texas Instruments, *Small Form-Factor Reinforced Isolated IGBT Gate Drive Reference Design for 3-Phase Inverter*, TIDA-00446 Design Guide (TIDUAZ0)
3. Texas Instruments, WEBENCH® Design Center (http://www.ti.com/webench)

10 Terminology

GaN— Gallium Nitride

FET— Field Effect Transistors

eGaN FETs—Enhanced Mode Gallium Nitride FETs

CMTI— Common Mode Transient Immunity

DESAT— Desaturation

PWM— Pulse Width Modulation

11 Acknowledgments

The author would like to thank Anant Kamath, Sudhir Adinarayana, Sarangan Valavan, Anand Reghunathan, and Goda Devi (the Interface Isolation Business Unit at TI) for their technical contributions to this design.

12 About the Author

NEERAJ BHARDWAJ is an Applications Engineer at Texas Instruments, where he is responsible for defining new high-performance analog products and application support on existing products for industrial and automotive markets. He has a high level of experience in motor drive systems and high-voltage systems with an emphasis in safety applications, standards, test and characterization of mixed signal processors, and EMC cognizant systems design. In his previous role, he led the Systems and Applications team in Safety and Security Microcontroller Group in TI. He mentors teams on competitive robotics. He has over 19 years of experience in the industry and has worked for TI since 2005. He has a B.E. degree in electrical engineering specialized in high voltage and power electronics from the Government Engineering College Jabalpur and a M.Tech. degree in aerospace engineering specialized in control and guidance from the Indian Institute of Technology Bombay.

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