

TI Designs: TIDA-00826 Design Guide

50-Ohm 2-GHz Oscilloscope Front-end Reference Design



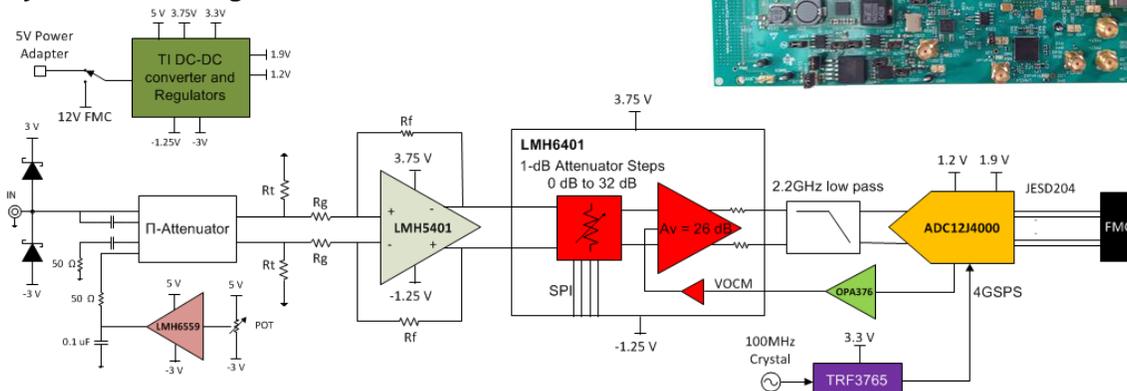
Design Features

- 50-Ω input, analog front-end with input signal bandwidth of 2 GHz.
- System ENOB of 6 to 8 bits is achieved with this signal chain.
- Supports a maximum input signal of $\pm 3V$, with user-selectable options for input AC or DC coupling.
- DC-offset correction feature available in DC-coupled input mode.
- Three input-amplitude voltage adjustment settings provided by the front-end π -attenuator: 1:1, 2:1 and 5:1
- Low noise, high-performance fully-differential amplifier (LMH5401) used for single-ended to differential conversion
- High performance digitally-controlled variable-gain amplifier (LMH6401) programmable from 26dB to -6dB gain in 1-dB steps to maintain full-scale input at the ADC
- 12-bit ADC12J4000 operating at 4GSPS for sampling input signals.
- Design supports +5 V supply using wall-mount power adapter or +12 V using internal FMC connection

Featured Applications

- Digital Oscilloscopes
- Time Domain Reflectometers
- High Speed Data Acquisition Capture Card

System Block Diagram



Design Description

This reference design is part of an analog front-end for 50Ω-input oscilloscope application. System designers can readily use this evaluation platform to process input signals from DC to 2 GHz in both frequency-domain and time-domain applications.

The first stage of the reference design is a three-step differential π -attenuator relay circuit that adjusts the input voltage amplitude. The low-noise, wideband, fully-differential amplifier (FDA) LMH5401 follows the π -attenuator circuit for single-ended to differential signal conversion. The LMH5401 output drives the digitally-controlled variable-gain amplifier (DVGA) LMH6401 for precise gain adjustment, which drives a fifth-order 2.2-GHz low-pass filter. An analog-to-digital converter (ADC12J4000) operating at 4-GSPS digitizes the filtered signal.

The design supports both AC and DC input coupling. For DC-coupled input, a potentiometer enables nulling the DC offset.

Design Resources

- [TIDA-00826](#)
- [TINA-TI™](#)
- [LMH5401](#)
- [LMH6401](#)
- [ADC12J4000](#)
- [LMH6559](#)

- All Design files
- SPICE Simulator
- Product Folder
- Product Folder
- Product Folder
- Product Folder



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1 Key System Specifications

PARAMETER	SPECIFICATION
Input Channels	1
Analog Bandwidth with 50-Ω inputs ($f_c = -3\text{dB}$)	2 GHz
Maximum Sampling Rate	4 GSPS
Maximum Input voltage	$\pm 3\text{V}$
Maximum system voltage gain	23 dB
Calculated Rise Time (10% to 90%)	175 ps
System SNR (LMH6401 $A_v = 6\text{dB}$)	48 dB
System ENOB (LMH6401 $A_v = 6\text{dB}$)	7.8 bits

2 System Description

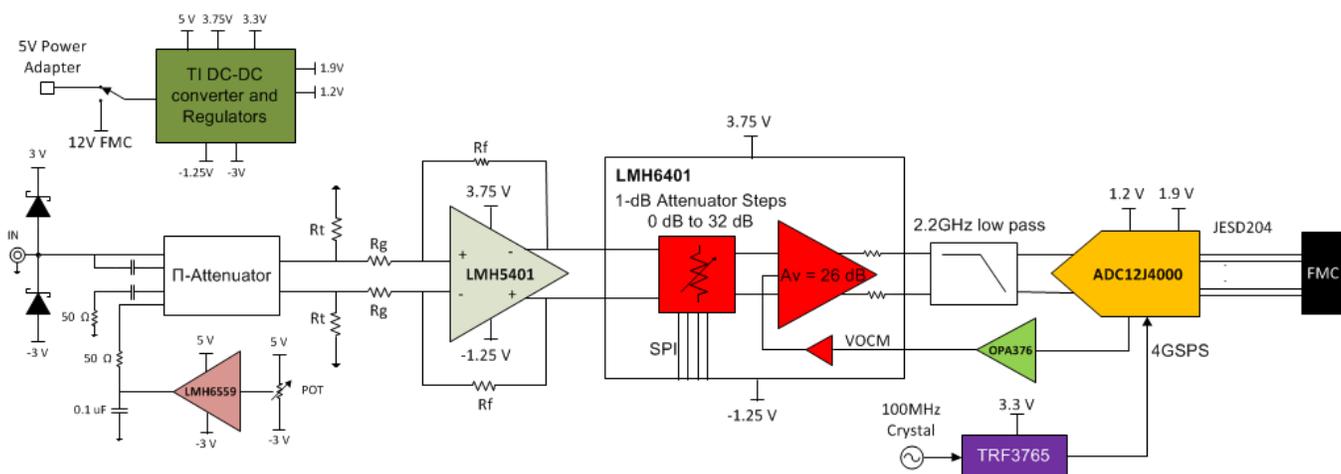


Figure 1: Block Diagram of the 50-Ohm 2GHz Oscilloscope Front-end System

The reference design has the following components selected for high performance and reliable operation:

2.1 LMH5401

- A fully-differential amplifier for 50-Ω input single-ended to differential conversion.
- 6 GHz bandwidth when configured for single-ended to differential gain of 4V/V (12dB).
- Excellent linearity performance from DC to 2GHz.
- Low input-voltage noise ($1.25\text{ nV}/\sqrt{\text{Hz}}$) and current noise ($3.5\text{ pA}/\sqrt{\text{Hz}}$) make the LMH5401 an ideal candidate for first-stage amplifier.

2.2 LMH6401

- A digitally-controlled variable-gain amplifier (DVGA) driving the ADC in an automatic gain control (AGC) loop.
- Gain control is performed via an SPI interface, allowing a 32-dB gain range from -6dB to 26dB in 1-dB steps.
- The device achieves a 3-dB bandwidth of 4.5GHz at 26-dB gain
- Excellent linearity performance from DC to 2GHz.
- An output common-mode control (VOCM) is provided in the device which allows the output common-mode (CM) voltage to match the ADC's optimum input common-mode voltage.

2.3 ADC12J4000

- 12-bit interleaved analog-to-digital converter (ADC) operating at 4GSPS.
- Excellent noise and linearity up to and beyond $f_{in} = 3\text{GHz}$.
- ENOB of 8.5 bits is sufficient for oscilloscope applications.
- The 95Ω differential input impedance with 1pF capacitance from each input to ground is ideal for a 100- Ω differential source and for a matched low-pass filter between the DVGA and the ADC.

2.4 LMH6559

- Provides a high-impedance buffer to the potentiometer, which connects to the undriven input of the LMH5401 in DC-coupled input mode.
- Provides the necessary DC-level shift on the undriven LMH5401 input to match the DC level of the input signal.
- Operated on a +5V and -3V supply, the LMH6559 can easily adjust the undriven FDA input from +4V to -2V.

2.5 OPA376

- Used in an integrator servo-loop configuration by comparing the average input common mode voltage at the ADC input pins $[(V_{IN+}) + (V_{IN-})]/2$ with the VCMO pin of the ADC, and applying the integrator output to the LMH6401 output common mode control (VOCM) pin.

2.6 TRF3765

- The TRF3765 is a wideband Integer-N/Fractional-N PLL with Integrated VCO that generates the 4GHz input clock to the ADC12J4000 using a 100MHz crystal oscillator.
- Low phase noise of -128dBc/Hz with 1MHz offset at VCO frequency of 4GHz makes it an ideal clock source to the ADC12J4000.

2.7 LMK04828

- The LMK04828 generates the SYSREF and DEVCLK signals to the ADC and the Virtex FPGA to properly synchronize the JESD204 digital outputs from the ADC.

3 System Block Diagram

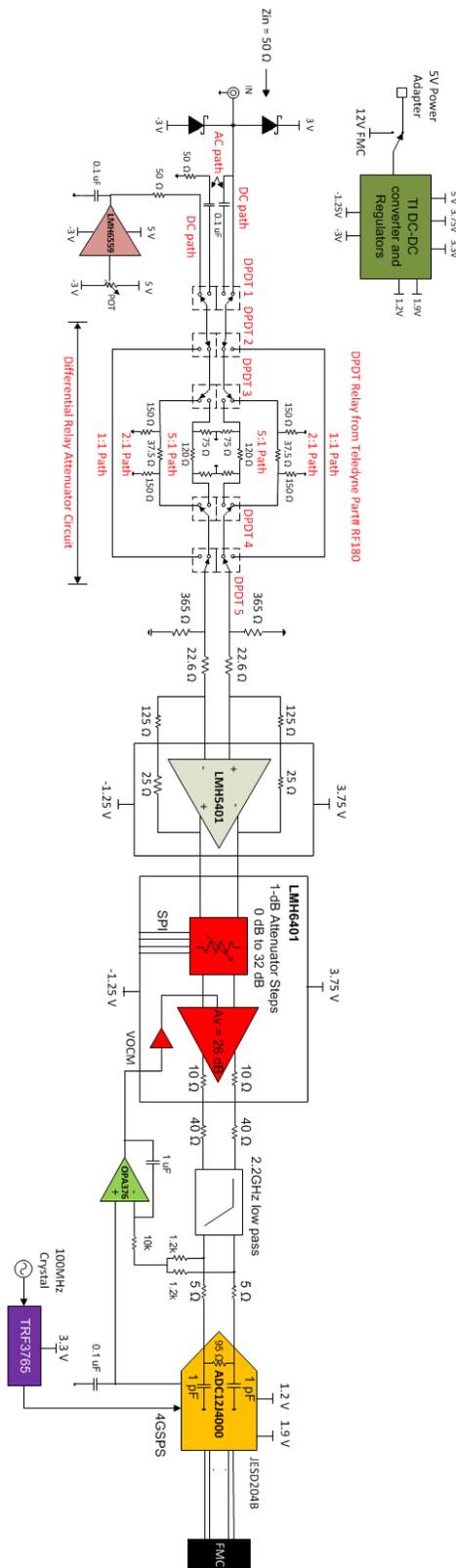


Figure 2: Complete System Block Diagram

4 Theory of Operation

4.1 π -Attenuator Relay Circuit Operation

Figure 3 shows the differential π -attenuator relay circuit cascaded to the LMH5401. The π -attenuator relay circuit provides the input voltage amplitude adjustment to prevent the saturation of analog front-end for large signal swings. The relay circuit has three attenuator settings: 1:1 (or 0-dB), 2:1 (or 6-dB) and 5:1 (or 14-dB). The relays switching between the π -attenuator settings are Teledyne dual-pole dual-throw (DPDT) RF-180 relays.

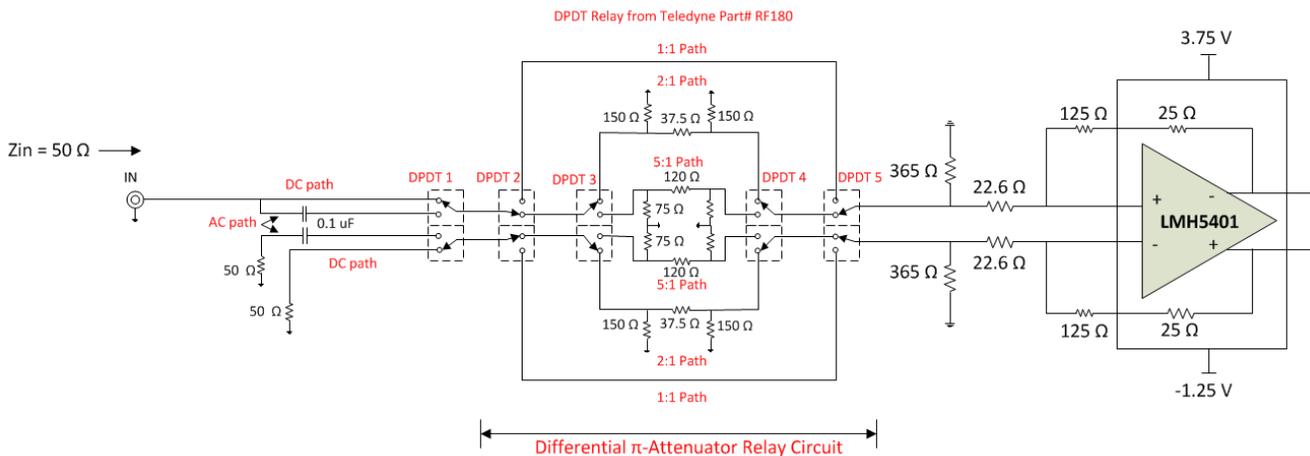


Figure 3: Differential π -attenuator circuit cascaded to the LMH5401

The differential π -attenuator relay circuit can be viewed as two single-ended π -attenuator circuits with matched ($Z_o = 50\text{-}\Omega$) source and load impedance. In a single-ended π -attenuator circuit, the two shunt arm resistors (R_p) have equal values in a matched-impedance configuration. Please refer to the below equations to calculate, for a given attenuation setting (A_T), the series (R_s) and shunt resistors (R_p) of the single-ended π -attenuator circuit. The attenuation setting (A_T) is expressed in V/V. See the appendix for the derivation of these equations.

Equation 1

$$R_p = Z_o * \frac{(1 + A_T)}{(1 - A_T)}$$

Equation 2

$$R_s = \frac{Z_o R_p}{(Z_o + R_p)} * \frac{(1 - A_T)}{A_T}$$

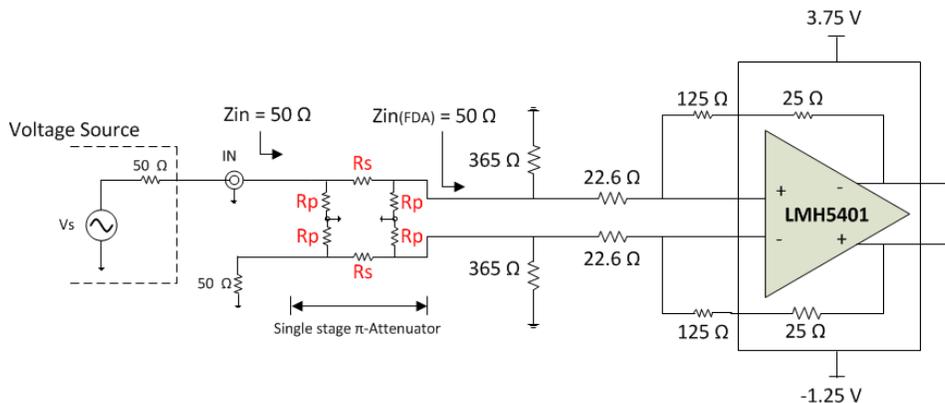


Figure 4: Single setting of the differential π -attenuator circuit

4.2 Input Coupling Options

The design supports 50-Ω input AC and DC coupling options.

4.3 Single-to-Differential Conversion

The LMH5401 fully-differential amplifier (FDA) follows the differential π-attenuator relay circuit for single-ended to differential signal conversion. This device offers the best wideband performance from DC to 2-GHz. The single-ended to differential signal conversion is done by including the π-attenuator relay circuit into the conversion loop to maintain symmetry across the LMH5401 inputs, as shown in Figure 4. The LMH5401 device datasheet contains the equations to calculate the feedback (R_F), gain (R_G), and termination (R_T) resistors of the LMH5401 for the single-ended to differential conversion.

4.4 Variable-gain Amplifier Circuit

The LMH6401 digitally-controlled variable-gain amplifier (DVGA) stage follows the FDA to provide fine voltage-level adjustments before the ADC. The LMH6401 works in an automatic gain control (AGC) loop in 1-dB steps to maintain a full-scale input to the ADC.

4.5 Filter Interface

A 2.2-GHz low-pass filter is implemented between the LMH6401 and ADC. This filter limits the out-of-band noise and harmonics from the first Nyquist zone. The filter has a fifth-order Chebyshev filter topology, which provides high stop-band attenuation with some pass-band ripple, reasonable phase response, and tolerance of component variations. The filter has an input and output impedance of approximately 100 Ω.

4.6 ADC Configuration

The selected ADC sample rate ensures that the entire signal bandwidth is within one Nyquist zone. This means that the sample rate must be within 0 to $F_s/2$, or $F_s/2$ to F_s , or F_s to $3F_s/2$, and so forth. Since the targeted signal bandwidth for this design is DC to 2GHz, the ADC sample rate is 4GSPS. The ADC was in the NCO-bypass mode for all the experimental results shown below.

The 4GHz clock to the ADC is derived from a 100MHz crystal oscillator using a TRF3765 PLL.

4.7 Calculation of the System Dynamic Range and Full-scale Input Range

As shown in Figure 2, the differential π-attenuator circuit works along with the LMH6401 to provide near continuous gain variability in the oscilloscope front-end. The front-end differential π-attenuator circuit provides three settings of coarse attenuation control with maximum attenuation of 0.2 V/V (or 14-dB). The LMH6401 provides fine 1-dB gain adjustment from 26 dB to -6 dB, thus having a 32-dB dynamic range.

The overall system dynamic range can be calculated by summing the maximum attenuation setting available in the differential π-attenuator circuit with the LMH6401 dynamic range.

Equation 3

$$\text{Dynamic Range}_{\text{System}} = \text{Pi_Attenuator}_{\text{Max}} + \text{Dynamic Range}_{\text{LMH6401}} = 46 \text{ dB}$$

The full scale (FS) input range of the oscilloscope front-end is determined by the minimum and maximum FS input that is applied to the system while maintaining a FS input at the ADC. The minimum system FS input is determined by the input signal level that is amplified by the maximum system gain in-order to maintain a FS signal at the ADC. The ADC12J4000 has a nominal FS input of 725 mV_{PP} from the datasheet and the maximum system voltage gain achieved at the ADC input is close to 23.2dB. Thus, the minimum system FS input achieved is 50 mV_{pp} as shown below:

Equation 4

$$\text{Min. Oscilloscope FS Input} = \frac{0.725}{10^{\left(\frac{23.2}{20}\right)}} = 50 \text{ mVpp}$$

The maximum FS input at the oscilloscope front-end can be determined by the input signal required to maintain the ADC full-scale for the maximum system attenuation. From the maximum system gain and dynamic range, we can determine the maximum system attenuation ($= 23.2 - 46$) as $- 22.8$ -dB which corresponds to a maximum FS input swing of 10Vpp. However, applying a 10Vpp signal with 14-dB (0.2 V/V) of maximum attenuation in the π -attenuator stage would saturate the LMH5401 in the single-ended to differential configuration. To prevent the saturation of LMH5401, the input signal has been restricted to ± 3 V or 6Vpp which is also the maximum oscilloscope FS Input.

Equation 5

$$\text{Max. Oscilloscope FS Input} = 6 \text{ Vpp}$$

The oscilloscope front-end can accommodate higher maximum FS input levels by adding more attenuation in the π -attenuator circuit. For example, to achieve maximum oscilloscope FS input of 10 Vpp, an attenuation of 20dB (0.1V/V) should be added in the π -attenuator stage.

Oscilloscopes typically have eight vertical divisions on the screen which translates to 6.25mV/DIV and 750mV/DIV for the minimum and maximum full-scale inputs, respectively.

Based on the minimum and maximum oscilloscope full scale input values, it is possible to establish the optimum SNR performance for a particular attenuator setting. Figure 5 shows a plot of the measured SNR performance versus scope FS input for the different π -attenuator settings. In the plot, each data point of a given π -attenuator curve represents an LMH6401 gain setting, with the minimum (maximum) SNR achieved for the highest (lowest) LMH6401 gain setting of 26-dB (-6 dB) and the data points increment in 2-dB gain steps of LMH6401.

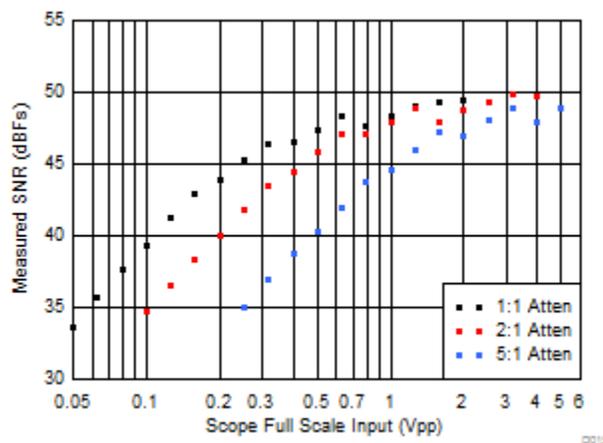


Figure 5: Plot of measured SNR vs Scope Full Scale Input (Vpp) across attenuation settings

Typically, high-speed oscilloscopes with a 2-GHz bandwidth limit the SNR performance to ~ 35 -dB at the highest gain setting. With 50 mVpp minimum full-scale input at the oscilloscope front-end, this translates to a 1mVpp noise on the oscilloscope screen, which is decent performance for 2-GHz oscilloscope front-ends.

If 40-dB SNR performance is the limit, the LMH6401 device gain can be fixed to 20-dB gain (or LMH6401 Maximum Gain – 6dB). Judicious choice of the front-end π -attenuator stage and the LMH6401 gain setting can maintain the SNR performance above 40-dB for 100mVpp and beyond full-scale input levels. For example, to display 250mVpp on the screen, set the π -attenuator stage to the 2:1 attenuator setting and the LMH6401 to $A_v = 18$ dB in-order to achieve an SNR of 42-dB. By comparison, setting the π -attenuator stage to the 5:1 setting and LMH6401 to maximum gain of 26 dB achieves 35-dB SNR.

5 Simulation

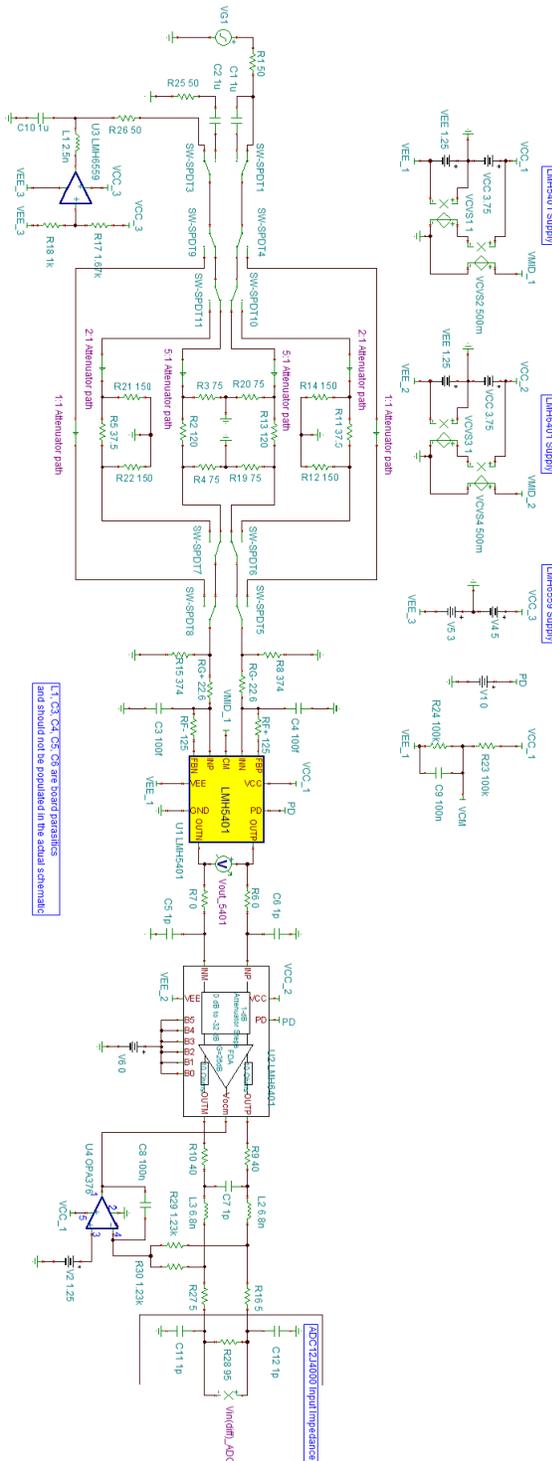


Figure 6: TINA-TI Simulation setup of DC-coupled 50-Ω input with the 5:1 Relay attenuator path enabled and the LMH6401 set to maximum voltage gain (A_v) = 26dB

Figure 6 shows the setup used in the TINA-TI simulator to simulate the 50-Ω input analog front-end in a DC-coupled configuration. In the TINA-TI simulator, the DPDT relay is modeled by two SPDT switches for the

differential relay attenuator circuit. The ADC12J4000 input impedance is modeled by a differential 95-Ω and 1-pF capacitor to GND on each input, as specified in the ADC12J4000 datasheet.

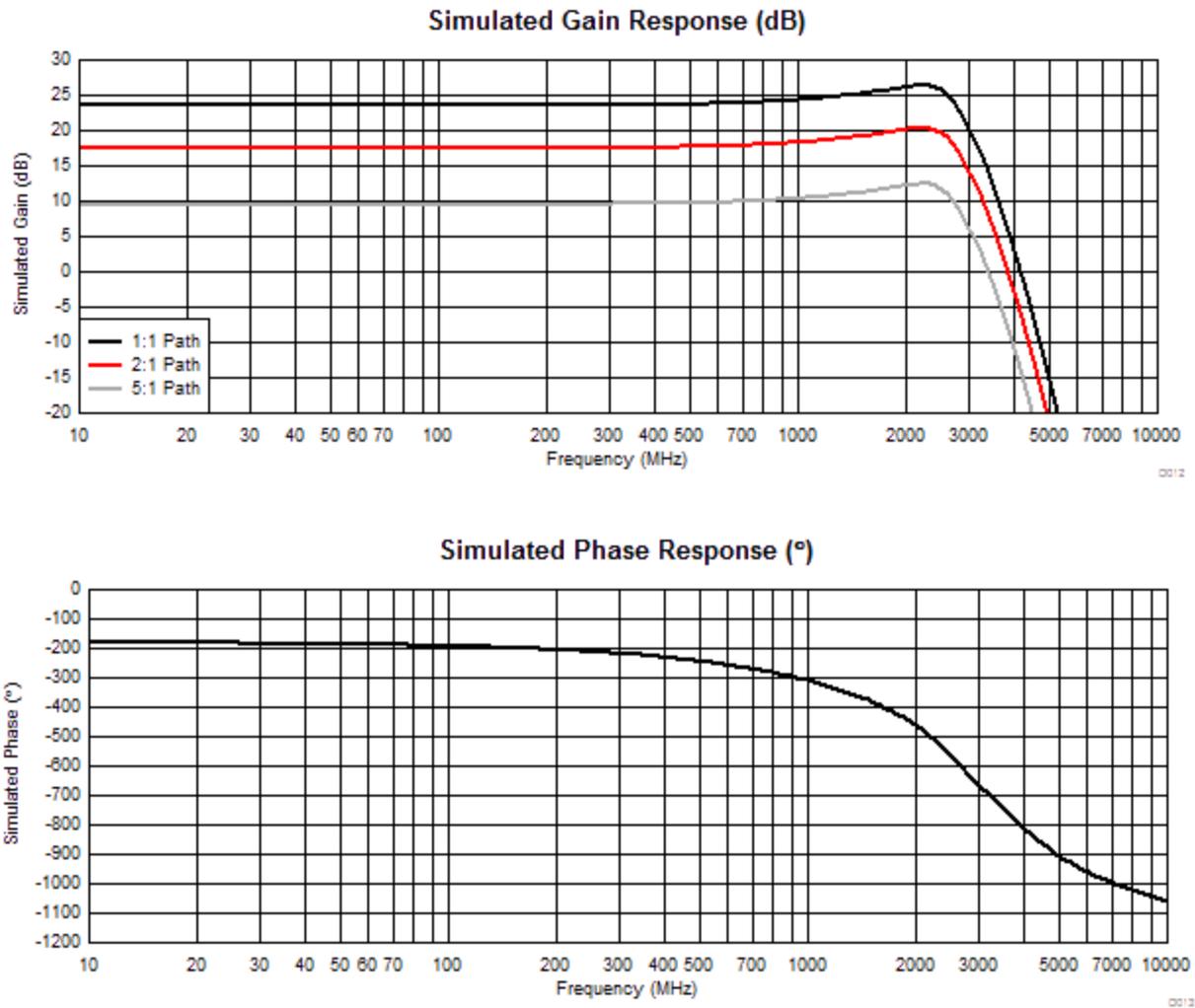
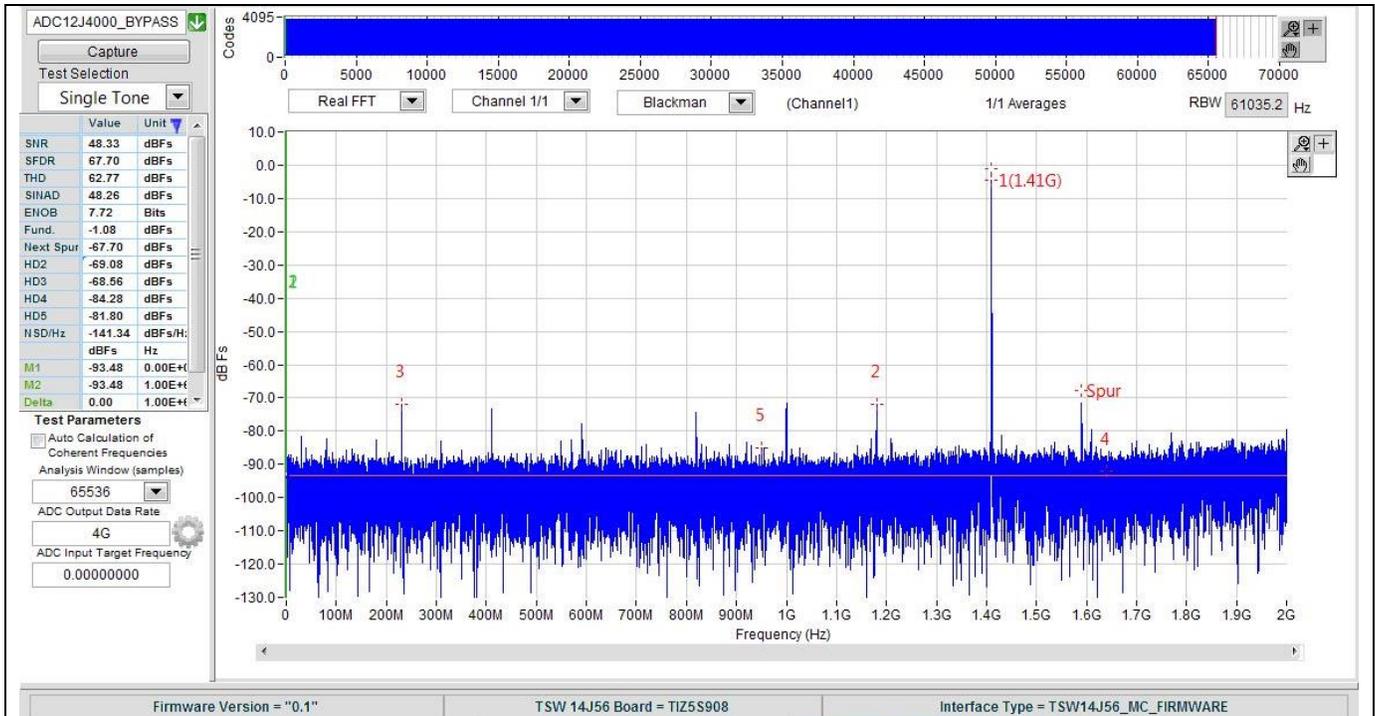


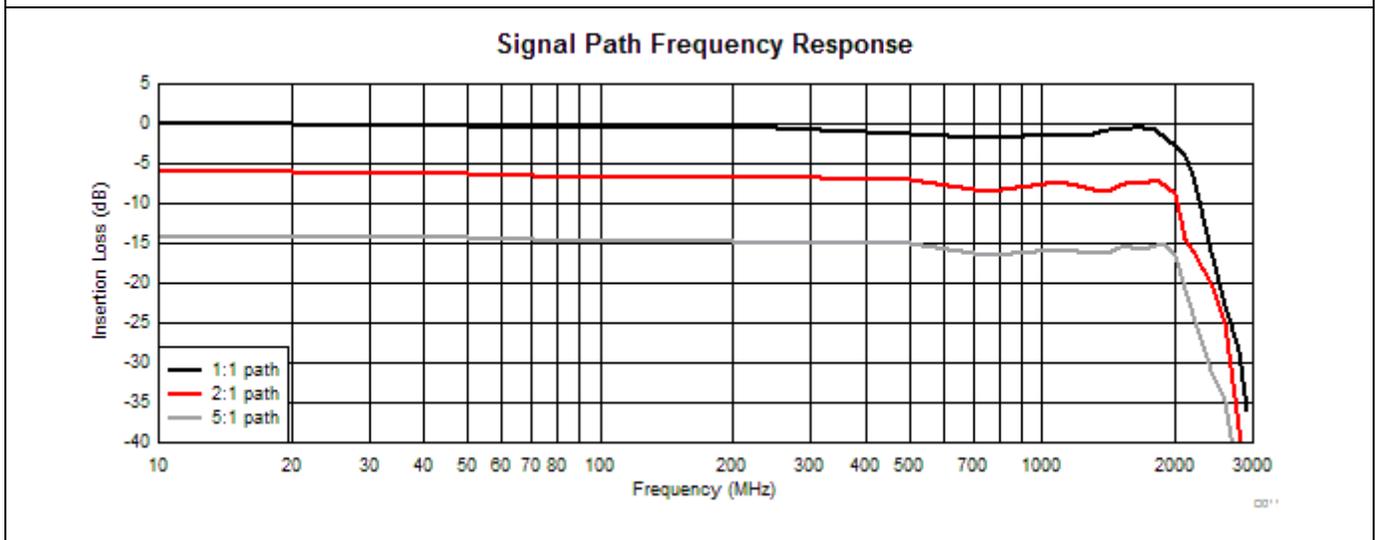
Figure 7: Simulated AC Small-signal Response at the ADC12J4000 input for 1:1, 2:1, and 5:1 attenuations with LMH6401 gain = A_v (max) = 26dB

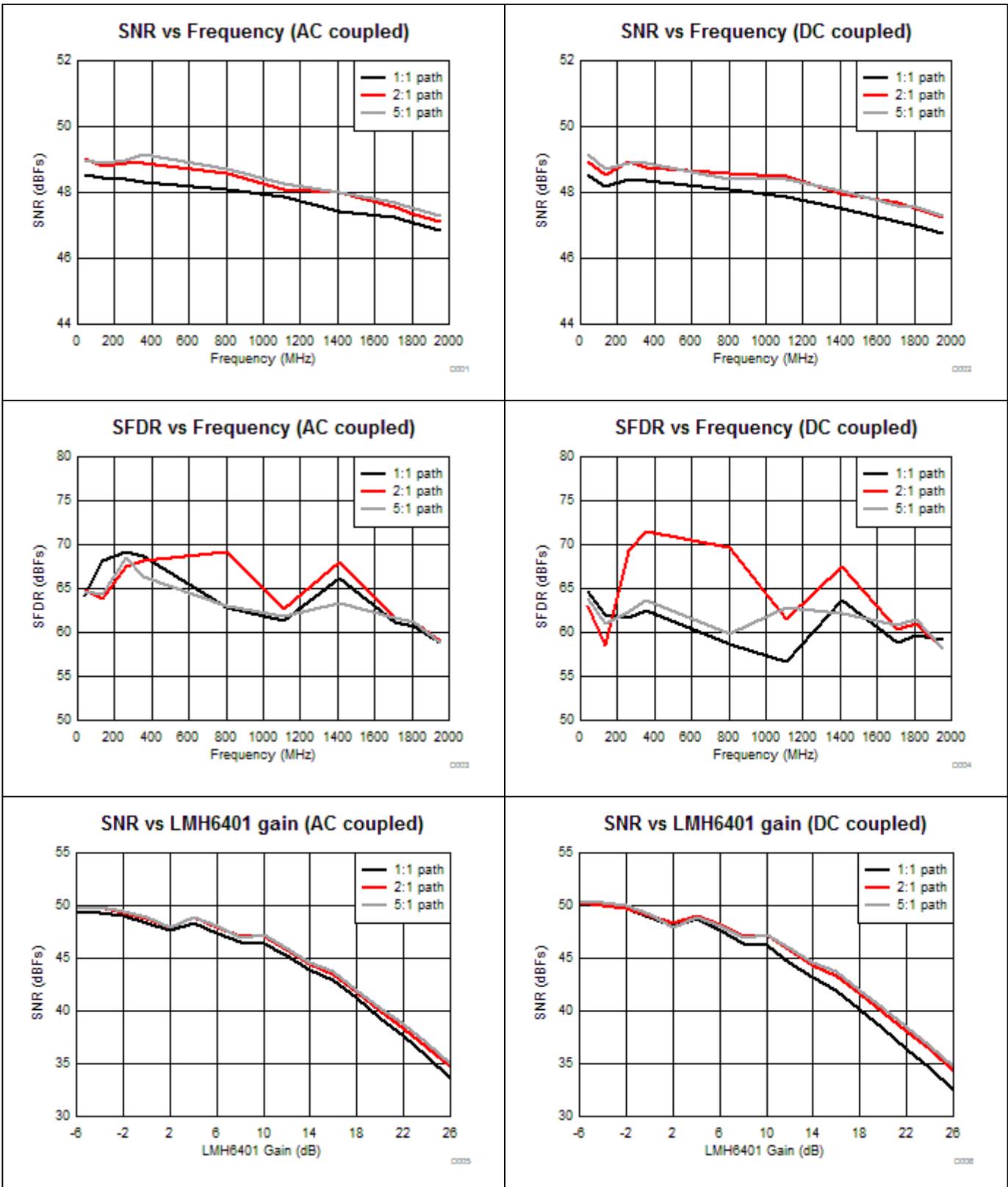
6 Experimental Results

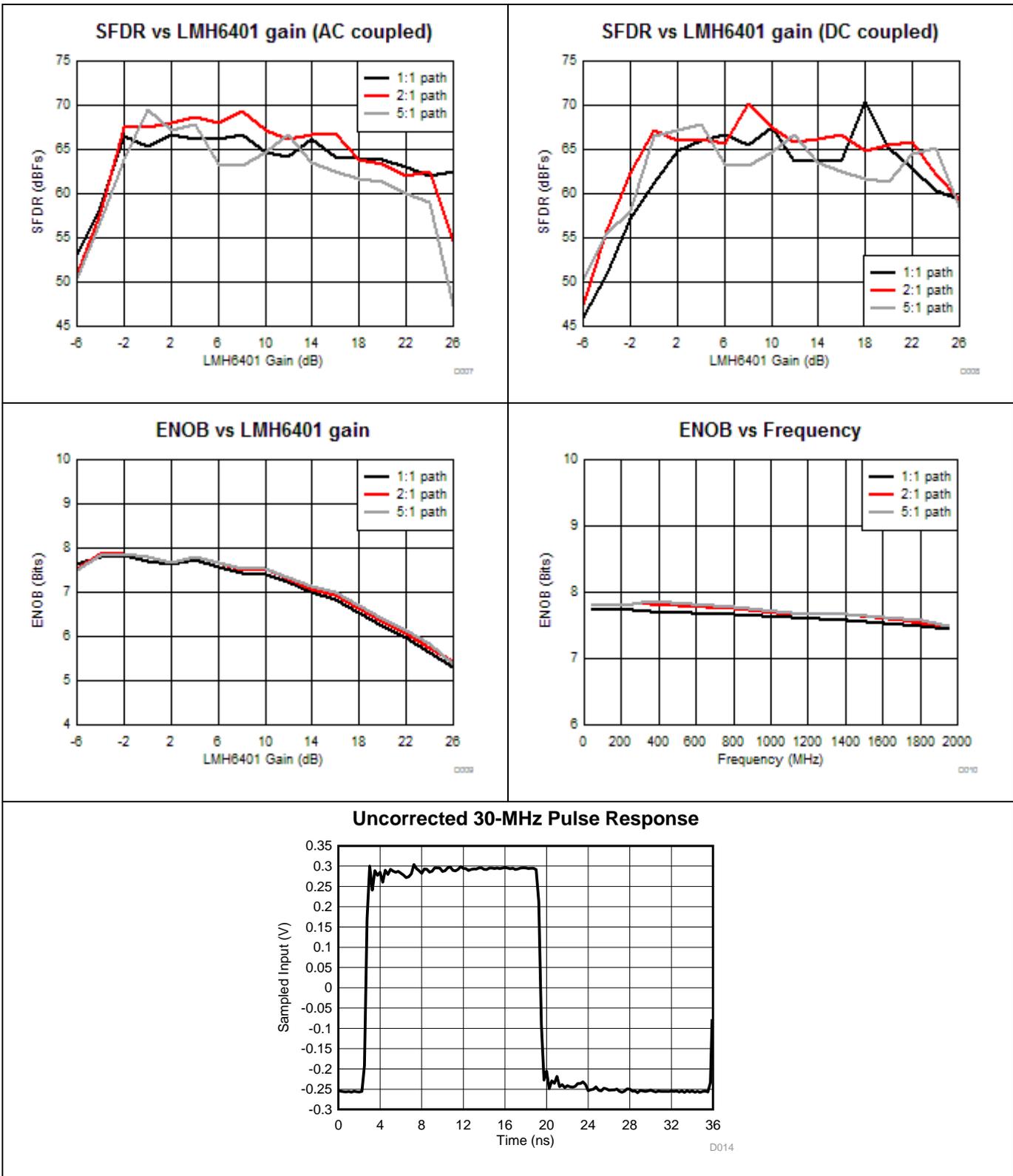
The below plots were generated using the TSW12J64EVM. Section 9 shows the test setup used for making the measurements.



Test condition: 1:1 Attenuator setting, LMH6401 Voltage gain (A_v) = 6-dB







7 Getting Started Hardware

The TSW12J64EVM evaluation board implements the reference design. The schematic, layer prints and bill of materials for the TSW12J64EVM are available in the reference design folder. Figure 8 and Figure 9 below show the top and bottom view of the TSW12J64EVM board.

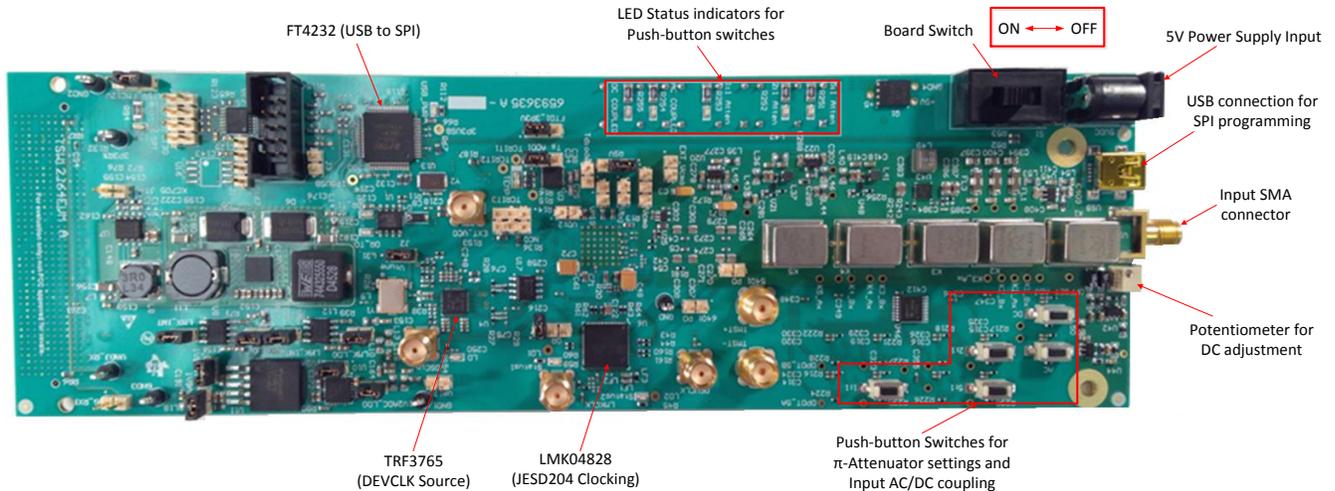


Figure 8: Top View of the TSW12J64EVM

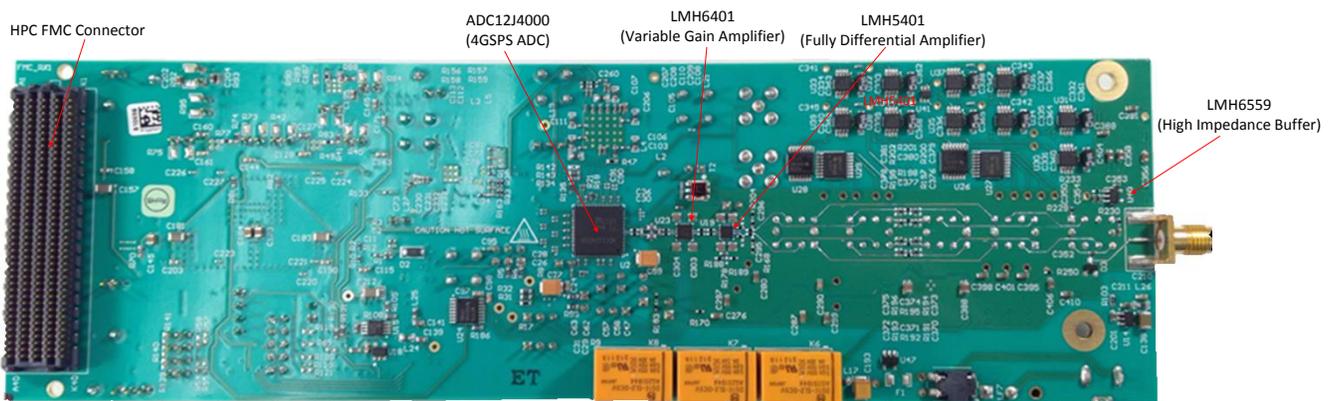


Figure 9: Bottom View of the TSW12J64EVM

The TSW12J64EVM requires the following inputs:

1. +5V power supply from the wall-mount power adapter
2. Mini-USB connection to PC to program the LMH6401 (Variable Gain Amplifier), ADC12J4000 (ADC) and LMK04828 (JESD204 Clocking).
3. Push-button switches are provided for selecting the different π -Attenuator settings and input AC- or DC-coupling selection. LEDs indicate the status of π -Attenuator settings and input coupling selection.

WARNING: Pressing two or more of the push-button switches simultaneously may put the relays in an unknown state.

4. In input DC-coupling mode, a potentiometer corrects the DC imbalance between the input signal and the undriven side of the differential π -Attenuator circuit.

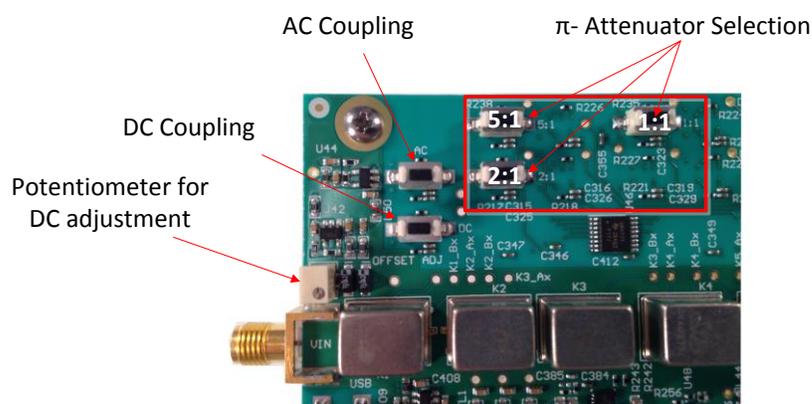


Figure 10: Push button switch assignment

5. The TSW12J64EVM GUI programs the LMH6401 gain.
6. TRF3765 provides the 4 GSPS device clock for the ADC12J4000.
7. LMK04828 provides the JESD204 signals for synchronizing the ADC digital output and the Virtex FPGA on the TSW14J56 data-capture board.

8 Getting Started Firmware

1. Contact TI Support at www.ti.com for the required TSW12J64EVM GUI software to program the TSW12J64EVM board.
2. Extract files from the TSW12J64_GUI.zip file, run the setup.exe executable file, and then follow the setup instructions.
3. Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.
4. The TSW12J64EVM GUI software is similar to the ADC12J4000EVM GUI software except for an added tab to program the LMH6401 device gain. Hence, follow the steps for programming the ADC and Clock in the ADC12J4000EVM User's guide www.ti.com/tool/adc12j4000evm.

9 Test Setup

Figure 11 shows the default bench setup for evaluating the reference design. A low-noise signal generator generates the required single-tone signal. A band-pass filter suppresses the signal-generator harmonics in the input signal. No additional clock sources are required for testing because the EVM has an onboard reference clock.

The TSW12J64VM connects to the TSW14J56EVM data-capture platform via an FMC connector and uploads data to a computer that is running the High Speed Data Converter Pro Software, which analyzes the data.

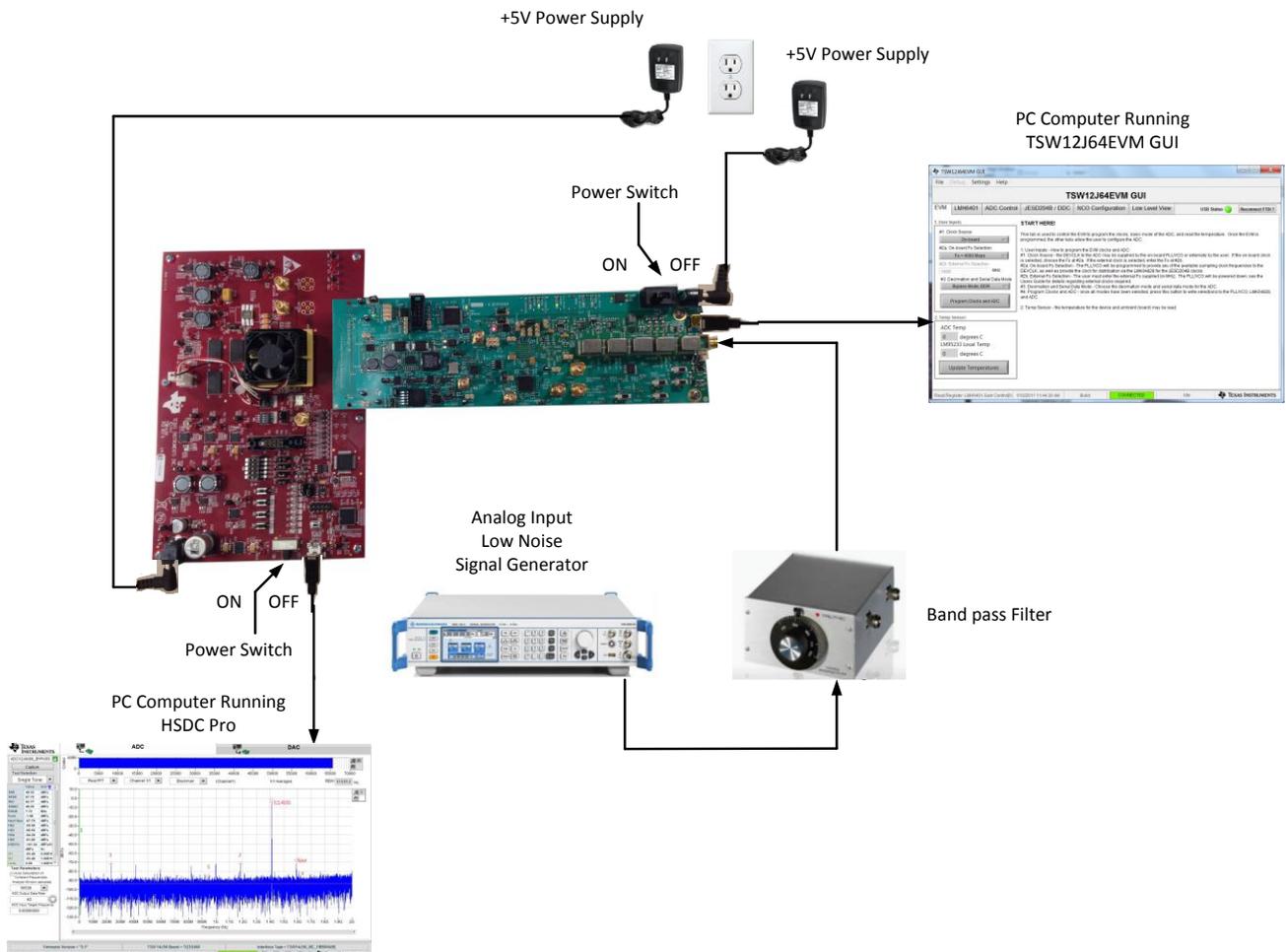


Figure 11: Test setup procedure for evaluating the TSW12J64EVM

NOTE: The HSDC Pro software must be installed before connecting the TSW14J56EVM to the PC for the first time.

9.1 AC-coupled Input Configuration

The TSW12J64EVM can be setup for AC-coupled input by clicking the AC push-button switch shown in Figure 10. The rest of the test setup is as shown in Figure 11.

9.2 DC-coupled Input Configuration

Set up the TSW12J64EVM for DC-coupled input by clicking the DC push-button switch shown in Figure 10. Adjust the potentiometer connected to the un-driven side of the differential π -attenuator to match the DC voltage of the input signal. This adjustment is required to maintain the ADC input common-mode DC offset to $< 0.1V$.

Another scenario that requires the adjustment of ADC common-mode DC offset using the potentiometer is while using an RF source for evaluating the TSW12J64EVM in DC-coupled input configuration. Low-noise RF sources are usually AC coupled (limited to 9 kHz operation). Connecting an AC-coupled RF source on one input of the differential π -attenuator with a DC-coupled path on the other input will generally create a DC offset at the ADC input. Again, DC-offset correction with the potentiometer is required to maintain $< 0.1V$ DC offset at the ADC inputs.

In an actual application, a servo-loop will generally create this DC adjustment by sensing the DC offset on the ADC inputs and applying an appropriate DC correction on the undriven input side of π -attenuator circuit.

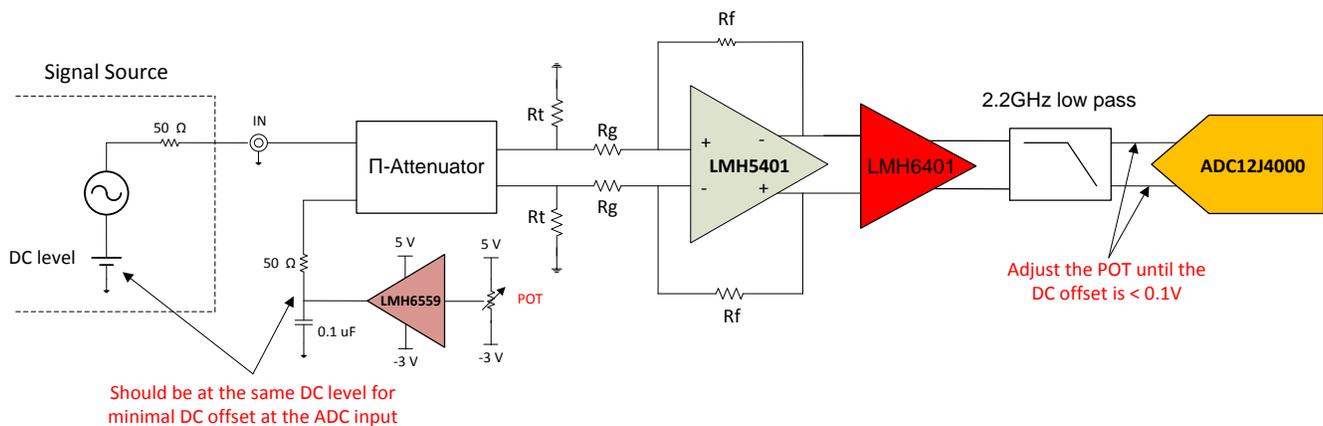


Figure 12: Potentiometer adjustment in DC-coupled Input Configuration

10 Appendix

10.1 Calculation of the π -Attenuator resistor values R_s and R_p

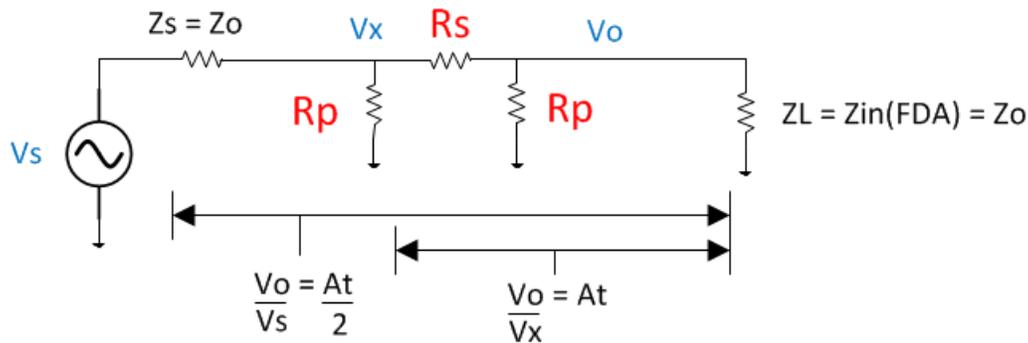


Figure 13: Single-ended π -Attenuator Circuit

From the circuit we know that,

Equation 6

$$A_T = \frac{V_X}{V_O} = \frac{R_P || Z_O}{(R_P || Z_O) + R_S}$$

We can solve for the attenuation value A_T by solving the voltage divider between V_x and V_o .

The equivalent resistive network presented to the source must equal Z_o

Equation 7

$$R_P || \{R_S + (R_P || Z_O)\} = Z_O$$

We can then Equation 6 for R_S as below,

$$A_T = \frac{R_P || Z_O}{(R_P || Z_O) + R_S}$$

$$A_T(R_P || Z_O + R_S) = R_P || Z_O$$

$$A_T(R_P || Z_O) + A_T R_S = R_P || Z_O$$

Divide both sides by $R_P || Z_O$ to give,

$$A_T = \frac{A_T R_S}{R_P || Z_O} + 1$$

$$\frac{A_T R_S}{R_P || Z_O} = 1 - A_T$$

$$A_T R_S = (R_P || Z_O)(1 - A_T)$$

We then yield Equation 8 by solving for R_S

Equation 8

$$R_S = (R_P || Z_O) \left(\frac{1 - A_T}{A_T} \right)$$

Now substitute Equation 8 into Equation 7,

$$R_P || \left\{ (R_P || Z_O) \left(\frac{1 - A_T}{A_T} \right) + (R_P || Z_O) \right\} = Z_O$$

$$R_P || \left\{ (R_P || Z_O) \left(\frac{1 - A_T}{A_T} + 1 \right) \right\} = Z_O$$

$$R_P || \left\{ (R_P || Z_O) \left(\frac{1 - A_T}{A_T} + 1 \right) \right\} = Z_O$$

$$R_P || \left\{ (R_P || Z_O) \left(\frac{1}{A_T} \right) \right\} = Z_O$$

$$R_P || \left\{ \frac{R_P || Z_O}{A_T} \right\} = Z_O$$

Expanding the main parallel combination,

$$\frac{1}{\frac{1}{R_P} + \frac{1}{\frac{R_P || Z_O}{A_T}}} = Z_O$$

$$1 = \frac{Z_O}{R_P} + \frac{Z_O}{\frac{R_P || Z_O}{A_T}}$$

Expanding the parallel combination of R_P and Z_O ,

$$1 = \frac{Z_O}{R_P} + \frac{Z_O}{\frac{R_P Z_O}{(R_P + Z_O) A_T}}$$

$$1 = \frac{Z_O}{R_P} + \frac{(R_P + Z_O) A_T}{R_P}$$

$$R_P = Z_O + A_T R_P + A_T Z_O$$

$$R_P - A_T R_P = Z_O + A_T Z_O$$

$$R_P (1 - A_T) = Z_O (1 + A_T)$$

Solving for R_P yields Equation 9,

Equation 9

$$R_P = Z_O \left(\frac{1 + A_T}{1 - A_T} \right)$$

11 Board Schematics

The schematic for the TSW12J64EVM board is available at [TIDA-00826](#).

12 Layer Prints

The layer prints for the TSW12J64EVM board are available at [TIDA-00826](#).

13 BOM

The bill of materials (BOM) for the TSW12J64EVM board is available at [TIDA-00826](#).

14 Gerber Files

The Gerber files for the TSW12J64EVM board are available at [TIDA-00826](#).

15 About the Author

Rohit Bhat has been an applications engineer with Texas Instruments since 2012. Rohit has been supporting TI's high-speed amplifiers in applications requiring high-speed analog signal processing which includes, but is not limited to, video, test and measurement, and communications.

References:

[LMH5401 datasheet](#)

[LMH6401 datasheet](#)

[ADC12J4000 datasheet](#)

[LMH6559 datasheet](#)

[LMH6518 datasheet](#)

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