TI Designs – TIDA-00421

Automotive 1.3M Camera Module Design with OV10640, DS90UB913A and power over Coax

Design Overview

This camera design demonstrates a very small solution size for 1.3 Megapixel automotive cameras. Only a single coax connection is required to provide digital video, power, camera control and diagnostics. Output video format is 10-bit up to 100MHz or 12-bit up to 75MHz.

Design Resources

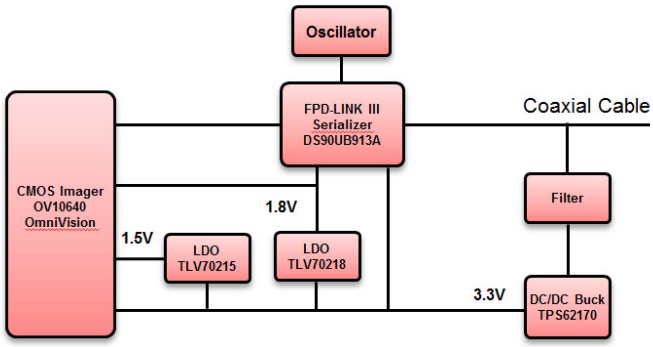
TIDA-00421	Camera Module	Design Folder
DS90UB913A-Q1	FPD-Link III Serializer	Product Folder
TPS62170-Q1	Buck Converter	Product Folder
TLV70215-Q1	1.5V LDO	Product Folder
TLV70218-Q1	1.5V LDO	Product Folder

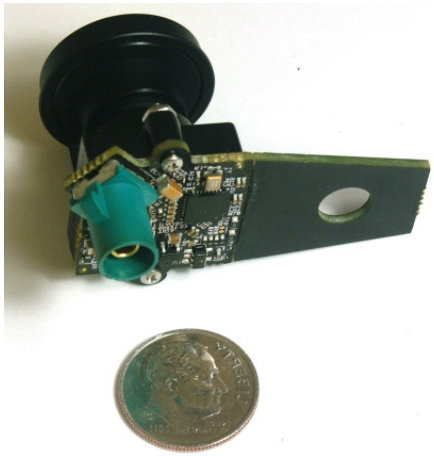
Design Features

- Size optimized design fits on a single PCB 20x20 mm
- Power supply optimized for small size and low noise
- Diagnostic and Built In Self Test (BIST)
- Single Rosenberger Fakra coax connector for digital video, power, control and diagnostics
- 1.3 Mpixel HDR image sensor OV10640 from OmniVision providing 12bit raw image data
- Includes mounting tab for attachment directly to tripod
- Power over Coax input can range from 4V to 17V

Featured Applications

- ADAS Vision Systems
- Surround View Systems
- Rear Camera





Contents

1 Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
System Input						
V_{IN}	Supply Voltage	Power Over Coax	4	12	17	V
P_{TOTAL}	Total Power Consumption	Vpoc = 12V		0.6	1.0	W
F_{PCLK}	Pixel Clock Frequency		25		100	MHz

Figure 1: System Specifications

2 System Description

For many automotive Advanced Driver Assistance Systems (ADAS), small cameras are required. This TI-Design addresses these needs by combining a 1.3 Megapixel imager with a 1.4 Gbit/s serializer and providing the necessary power supply for both. All of this functionality is contained on a 20mm x 20mm circuit card. The only connection required by the system is a single 50ohm coaxial cable.

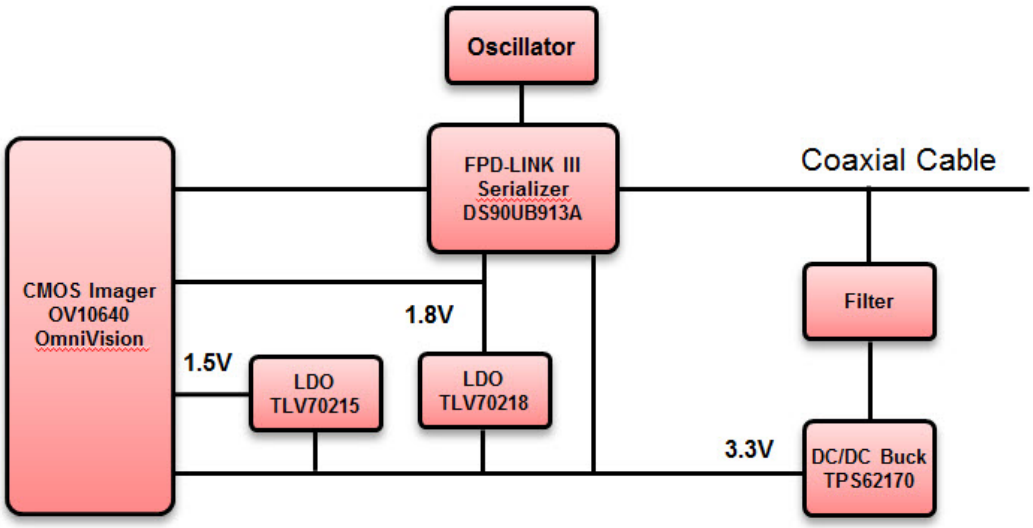


Figure 1: Camera Block Diagram

A combined signal containing the DC power and the FPD-Link front and back channels enters the board through the FAKRA coax connector. The filter shown in the diagram below blocks all of the high speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass.

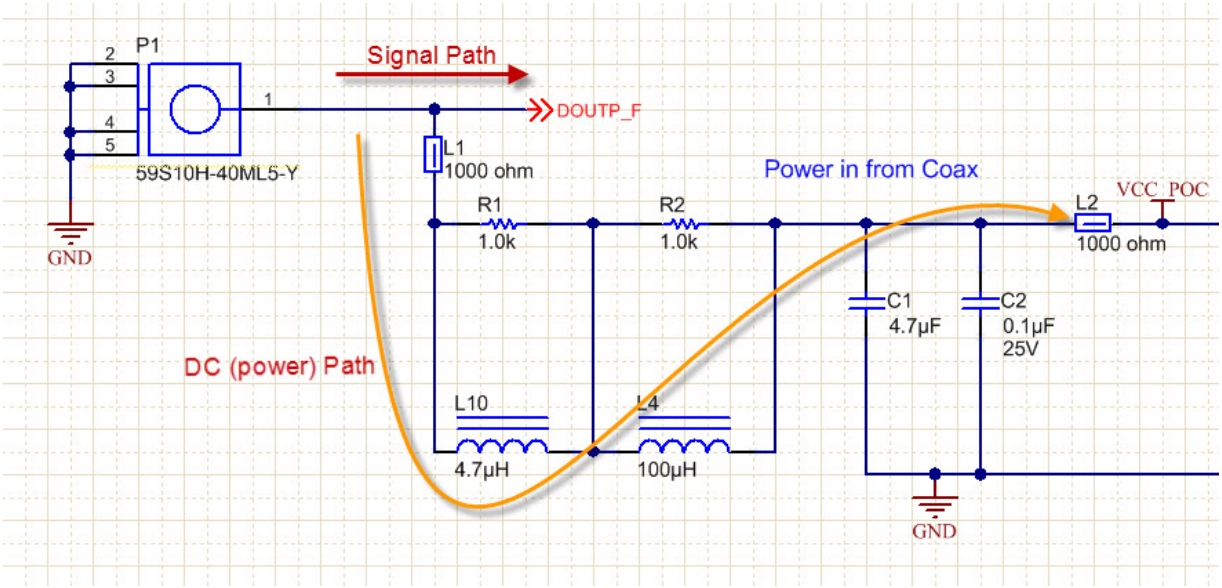


Figure 2: FPD-Link III Signal Path

The DC portion is connected to the input of the 3.3V buck converter. The two other rails required by the Serializer and the Imager are then created with Low DropOut regulators (LDO).

The high frequency portion of the signal is connected directly to the serializer. This is the path that the video data and the control backchannel will take between the Serializer and Deserializer.

The output of the CMOS imager is connected via Digital Video Port (DVP) to the Serializer. This 10-bit or 12-bit video data (with two sync signals) is converted to a single high-speed serial stream that is transmitted over a single coax cable to the Deserializer located on the other end of the cable.

On the same coax cable, there is separate low latency bidirectional control channel that transmits control information from an I2C port. This control channel is independent of video blanking period. It is used by the system microprocessor to configure and control the imager.

3 Block Diagram

3.1 Highlighted Products

This design utilizes the following TI products:

- **DS90UB913A-Q1** is the Serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer/deserializer pair is targeted for connections between imagers and video processors in an ECU (Electronic Control Unit).
- **TPS62170-Q1** is an automotive qualified step down DC converter optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response.
- **TLV70215-Q1** is an automotive qualified 300mA, Low IQ, Low-Dropout Regulator with a fixed output voltage of 1.5V
- **TLV70218-Q1** is an automotive qualified 300mA, Low IQ, Low-Dropout Regulator with a fixed output voltage of 1.8V

More information on each device and why they were chosen for this application follow in the next sections.

3.1.1 OV10640 Imager

Available from OmniVision Technologies Inc., this imager is a color 1.3 megapixel, CMOS imager with High Dynamic Range (HDR). It is suitable for automotive systems and can provide a 12-bit raw DVP output. Some additional features of the imager are:

- Supports image sizes: 1280x1080, VGA, QVGA and any cropped size.
- Low power consumption
- Requires three voltage rails
- Can be configured using I2C connection to serial camera control bus (SCCB)

3.1.2 DS90UB913A-Q1

Using a serializer to combine 12-bit video with a bi-directional control signal onto one coax or twisted pair greatly simplifies system complexity, cost and cabling requirements. The parallel video input of the DS90UB913A-Q1 mates well with the 12-bit parallel video output of the OV10640 imager. Once combined with the filters for the Power Over Coax (POC), video, I2C control, diagnostics and power can all be transmitted up to 15 meters on a single inexpensive coax cable. For more information on the cable itself, see the Cable Requirements application note at: SNLA229.

3.1.3 TPS62170-Q1

To keep the camera small, the power supply must be small. It must also be power efficient while not adding measurable noise to the video from the imager. Often, these two requirements stand in opposition. A switching power supply is more efficient than a linear regulator, but it can add noise to the system.

Camera sensor circuits usually are sensitive to noise at frequencies below 1 MHz. To avoid interference with the AM radio band, staying above 2 MHz is desirable in automotive applications. This means that the TPS62170-Q1 switching regulator operating at 2.25MHz meet both requirements. This high switching frequency also helps to reduce the size of the discrete components in the circuit.

3.1.4 TLV70215/18-Q1

The TLV702xx-Q1 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These automotive qualified LDOs are very small, allowing the1.5V and 1.8V rails to be created in a very small space. A precision bandgap and an error amplifier provide overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR) make these LDOs ideal for this application.

4 System Design and Component Selection

Below we will discuss the considerations behind the design of each subsection of the system.

4.1 PCB / Form Factor

This design was not intended to fit any particular form-factor. The only goal of the design with regards to the PCB was to make as compact a solution as possible. The square portion of the board is 20mm x 20mm. The area near the board edge in the second image is reserved for attaching the optics housing that holds the lens.

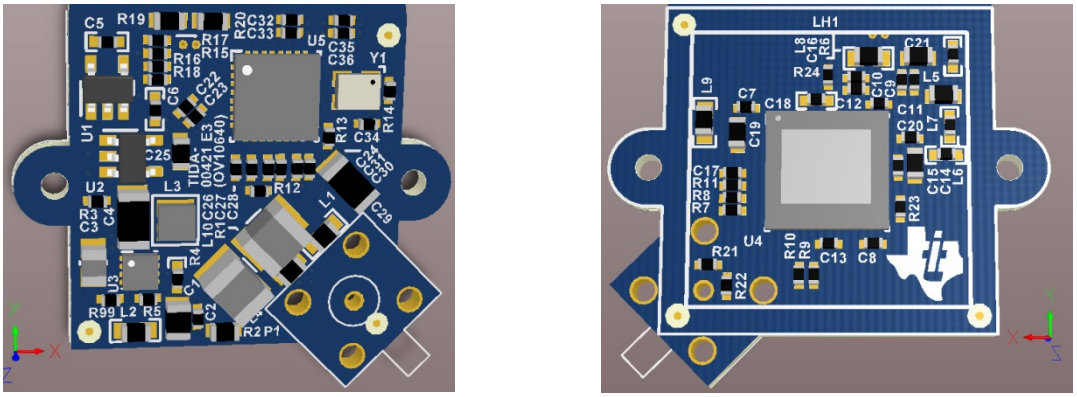


Figure 2: PCB Top and Bottom Views

4.2 I2C Addressing

4.2.1 Multiple Device Addressing

Some applications require multiple camera devices with the same fixed address to be accessed on the same I2C bus. The DS90UB913A provides slave ID matching/aliasing to generate different target slave addresses when connecting more than two identical devices together on the same bus. This allows the slave devices to be independently addressed. Each device connected to the bus is addressable through a unique ID by programming of the Slave alias register on Deserializer. This will remap the Slave alias address to the target SLAVE_ID address.

In this design, the OV10640 imager default address is 0x30 (0110000x). For a system utilizing more than one imager, GPIO 2/1 can be used to select different addresses for each imager. However, this would require that each camera in the system be built differently. Each system, then would have to be built with one of each unique camera. In a production environment, this is not desirable.

Instead, we can use the aliasing feature of the DS90UB913A. In the deserializer, unique addresses are assigned to each imager. These aliases are used to refer to the imagers that are all addressed at 0x30 (0110000x). The host microprocessor can now communicate with each imager by using its alias, even though the imagers in each camera are physically addressed identically.

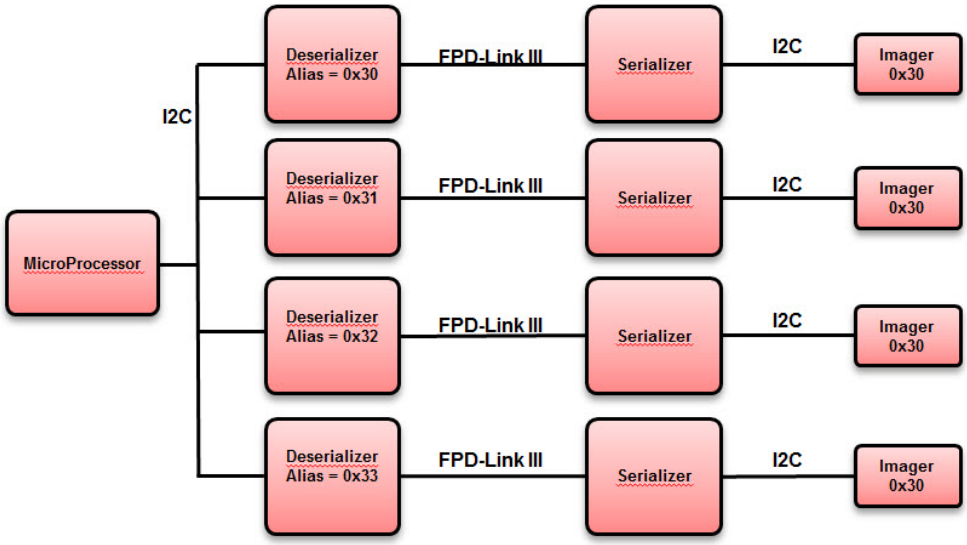


Figure 4: I2C Address Aliasing

4.2.2 Power Over Coax (POC) Filter

One of the most critical portions of a design which uses Power over Coax is the filter circuitry. The goal is twofold: 1) deliver a clean DC supply to the input of the switching regulators, and 2) protect the FPDLink communication channels from noise coupled backwards from the rest of the system.

The DS90UB913/914 SerDes devices used in this system communicate over two carrier frequencies, 700MHz at full speed ("forward channel") and a lower frequency between 1.75 and 3.25MHz ("back channel") determined by the deserializer device. The filter should attenuate this rather large band spanning both carriers, hoping to pass only DC. Luckily, by filtering the back channel frequency, we will also be filtering the frequencies from the switching power supplies on the board.

An ideal series 100 µH inductor could work as a low pass filter, with impedance >1KΩ at frequencies starting at 1MHz. However, due to parasitic capacitances, a real 100 µH inductor would cease to have high impedance around 70MHz. To cover the higher frequency band, we need another series inductor. A 4.7 µH inductor will ensure we have high impedance up to frequencies well above the 700MHz forward channel. See application note for more details: SNLA224

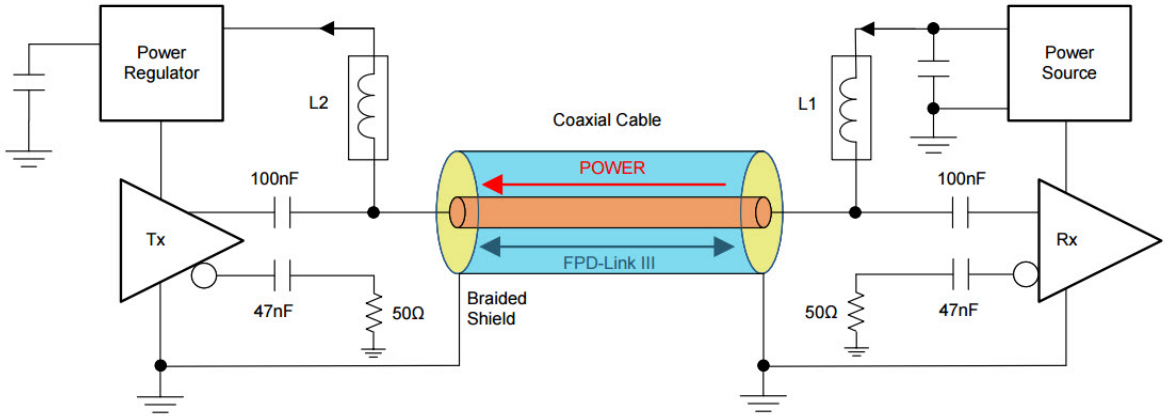


Figure 5: Power Over Coax

4.3 Step Down Converter

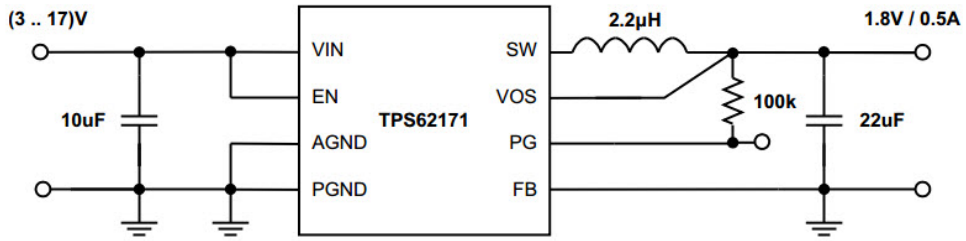


Figure 6: Typical Application Circuit

A lot of the component selection and design theory can be found in the Application Information section of the datasheet.

There are very few external components to choose.

Choosing the Output Inductor:
As mentioned above, it is important in this design that the switching frequency of the converter remain above 2 MHz. This means that the converter must always operate in continuous mode. Since input voltage and output voltage are fixed and the output current is almost constant and can be predicted easily, the minimum inductance, L, for the converter to operate with continuous inductor current can be calculated using this equation:

$$L = \frac{V_{out}(V_{in} - V_{out})}{2 * V_{in} * I_{out} * f} = \frac{3.3V(14V - 3.3V)}{2 * 14V * 0.12A * 2.1MHz} = 5uH$$

Since 5uH is between standard inductor values, the next higher value of 6.8uH is chosen.

Choosing the Output Capacitor:
Since the device is internally compensated, it is only stable for certain component values in the LC output filter. From the application note on optimizing the output filter, SLVA463A, we have the chart of stable values shown below in figure 76. 6.8uH falls between 4.7uH and 10 uH. This means that we can use a 22uF output capacitor and remain in the stable region of effective corner frequencies.

Nominal Inductance Value	Nominal Ceramic Capacitance Value (effective = 1/2 nominal)								
	4.7 µF	10.0 µF	22 µF	47 µF	100 µF	200 µF	400 µF	800 µF	1600 µF
	Effective Corner Frequencies								
0.47 µH	151.4 kHz	103.8 kHz	70.0 kHz	47.9 kHz	32.8 kHz	23.2 kHz	16.4 kHz	11.6 kHz	8.2 kHz
1.00 µH	103.8 kHz	71.2 kHz	48.0 kHz	32.8 kHz	22.5 kHz	15.9 kHz	11.3 kHz	8.0 kHz	5.6 kHz
2.2 µH	70.0 kHz	48.0 kHz	32.4 kHz	22.1 kHz	15.2 kHz	10.7 kHz	7.6 kHz	5.4 kHz	3.8 kHz
3.3 µH	57.2 kHz	39.2 kHz	26.4 kHz	18.1 kHz	12.4 kHz	8.8 kHz	6.2 kHz	4.4 kHz	3.1 kHz
4.7 µH	47.9 kHz	32.8 kHz	22.1 kHz	15.1 kHz	10.4 kHz	7.3 kHz	5.2 kHz	3.7 kHz	2.6 kHz
10.0 µH	32.8 kHz	22.5 kHz	15.2 kHz	10.4 kHz	7.1 kHz	5.0 kHz	3.6 kHz	2.5 kHz	1.8 kHz
	Recommended for TPS6213x/4x/5x/6x/7x								
	Recommended for TPS6213x/4x/5x only								
	Stable without Cff (within recommended LC corner frequency range)								
	Stable without Cff (outside recommended LC corner frequency range)								
	Unstable								

Figure 7: Stability vs Effective LC Corner Frequency

With our inductance value chosen, we now need an inductor with a proper saturation current. This is going to be the combination of the steady state supply current, as well as the inductor ripple current. We want the current rating to be sufficiently high, but minimize it as much as possible to reduce the physical size of the inductor. The following is the equation used to calculate the inductor ripple current (from the datasheet):

$$\Delta I_L = V_{out} * \left(\frac{\left(1 - \frac{V_{out}}{V_{in}}\right)}{L * f_{sw}} \right)$$

Here are the parameters for our design using the TPS62170:

$$V_{out} = 3.3V, V_{in} = 14V, L = 6.8\mu H, f_{sw} = 2.25MHz$$

Which yields an inductor current of ΔI_L = 165mA. The maximum current draw of the system through this regulator is 268mA. Finally, the following equation gives us our minimum saturation :

$$L_{sat} \geq \left(I_{max} + \frac{I_{ripple}}{2} \right) * 1.2 = \left(268mA + \frac{165mA}{2} \right) * 1.2 = \mathbf{420mA}$$

We chose a Coilcraft XPL2010-682MLB which has a saturation current of 450mA with only a 10% drop in inductance. This part comes in a very small 1.9 mm square package.

The output voltage is determined by the resistor divider to the feedback pin. The following is the calculation for our output voltage. We aim for 3.3V out, but wanted to work with readily available resistor values:

$$R_1 = R_2 * \left(\frac{V_{out}}{V_{ref}} - 1 \right) \rightarrow V_{out} = \left(\frac{R1}{R2} + 1 \right) * V_{ref} = \left(\frac{316k\Omega}{100k\Omega} + 1 \right) * 0.8V = 3.328V$$

This gives us a close enough output voltage to the desired 3.3V. For improved accuracy, all FB resistor dividers should use components with 1% or better tolerance.

4.4 Linear Low Dropout Regulators (LDO)

The TLV70215 and TLV70218 are very easy to design in. As the data sheet recommends, we just need to add a ceramic 1uF capacitor to the input of each device.

For ADAS applications, it is recommended that all ceramic capacitors use X7R dielectric material, which ensures minimum capacitance variation over the full temperature range. The voltage rating of the capacitors should be greater than the maximum voltage they could see, and 2x the typical voltage they see to avoid DC bias effects.

5 Getting Started Hardware

The TIDA-00421 needs only one connection to a system with a compatible deserializer. Simply connect the FAKRA connector on the coax cable between the serializer and deserializer.

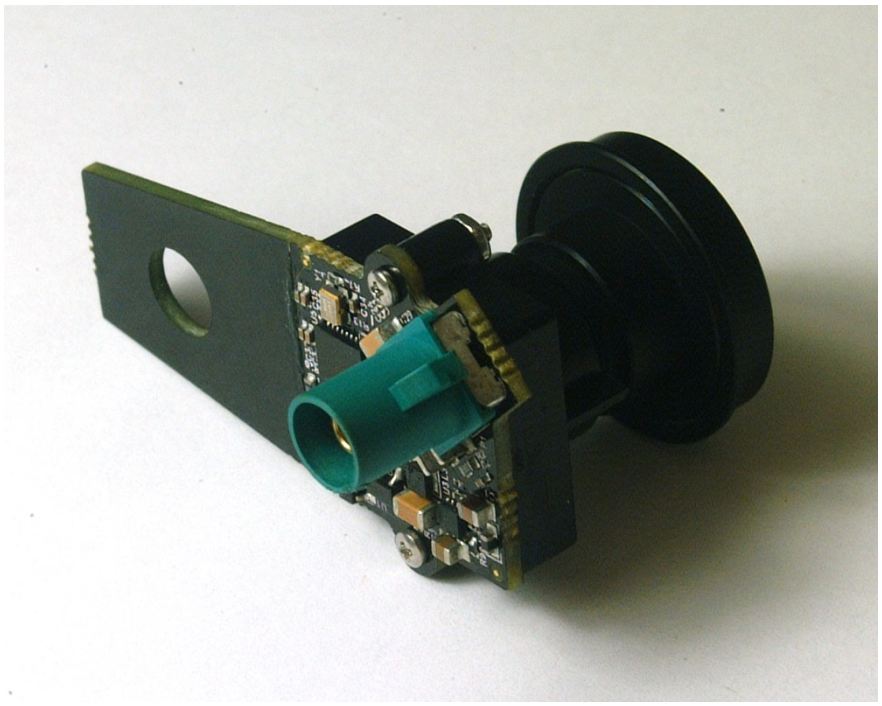


Figure 8: Getting started with the board

6 Test Setup

For the following tests, the camera was connected to a multiple camera surround view system.

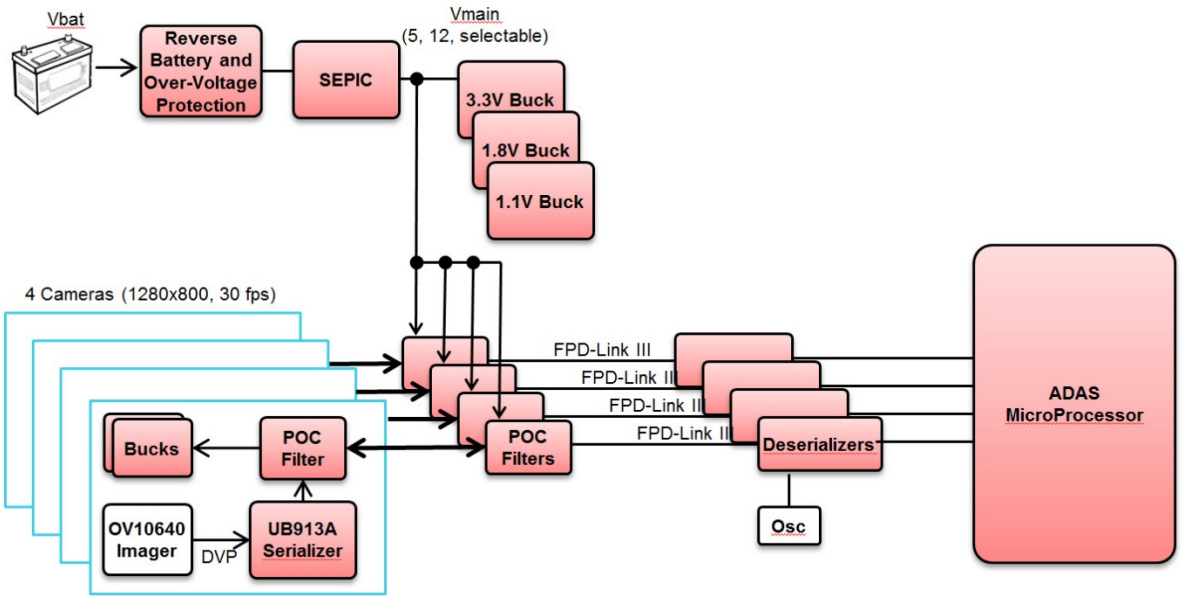


Figure 9: Simplified Surround View Block Diagram

6.1 Setup for Verifying Power Supply Startup - Vin, 3.3V, 1.8V and 1.5V Rails

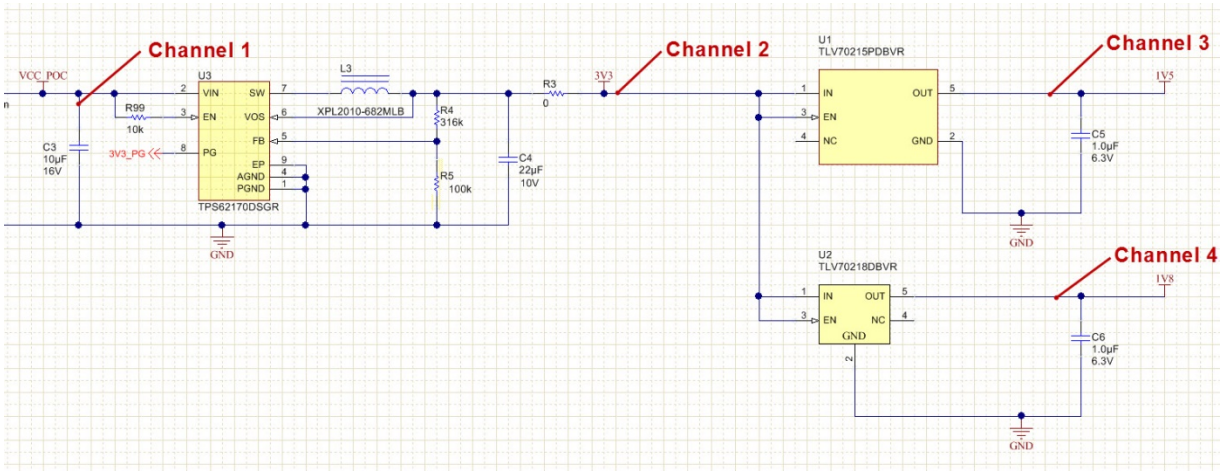


Figure 10: Setup for measuring all power rails

6.2 Setup for Verifying I2C Communications

For this test, a logic analyzer with I2C decode is used to monitor the I2C traffic on the buses. The two busses of interest are:

1. I2C connection from serializer to imager (shown as I2C_camera)
2. I2C connection from microprocessor to deserializer (shown as I2C_uC)

Connections must be made to both the clock and data lines of each bus.

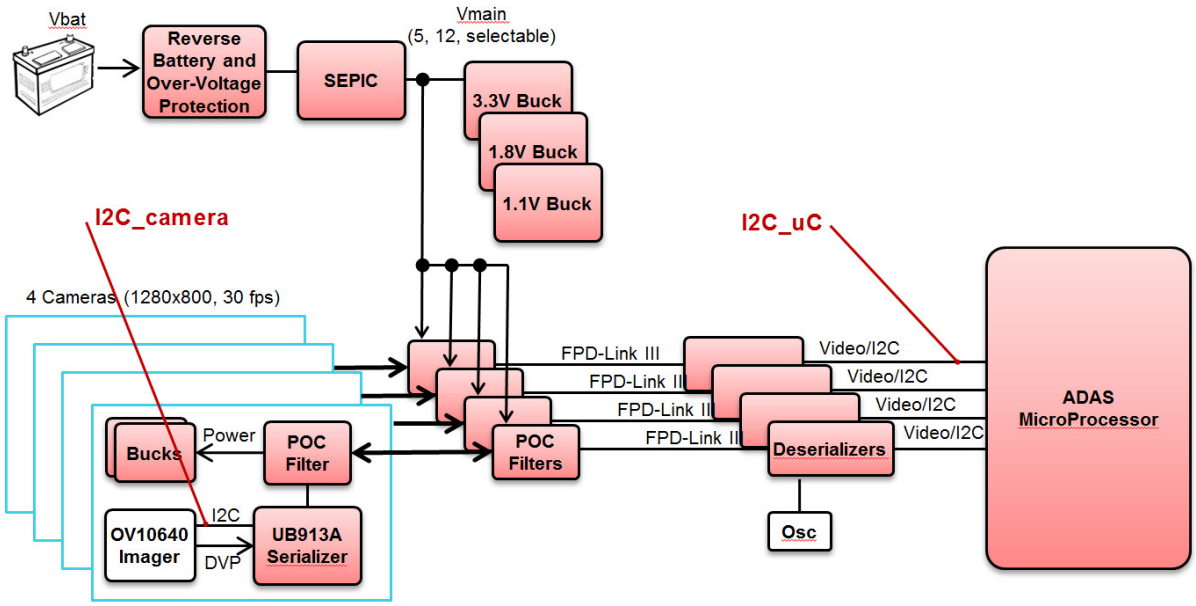


Figure 10: Setup for monitoring I2C transactions

7 Test Data

The following sections show the test data from verifying the functionality of the camera design.

7.1 Power Supply Startup - Vin, 3.3V, 1.8V and 1.5V Rails

The power supply startup waveforms are shown below.

- Channel 1 (yellow) 12V, Power Over Coax in
- Channel 2 (blue) 3.3V Switching Converter Output
- Channel 3 (pink) 1.5V LDO Output
- Channel 4 (green) 1.8V LDO Output

Figure 3: Power Supply Startup

7.2 I2C Communications

With the supplies up and running, we can now check the FPD-Link connection, the I2C aliasing and the state of the OV10640 imager in one step. The image below shows the initial communication between the microprocessor and the imager. This occurs after the microprocessor configures the deserializer on the other end of the link. Since this communication starts on the ECU board and is acknowledged by the camera(imager), this shows that the communication through the FPD-Link III is working. See figure 19.

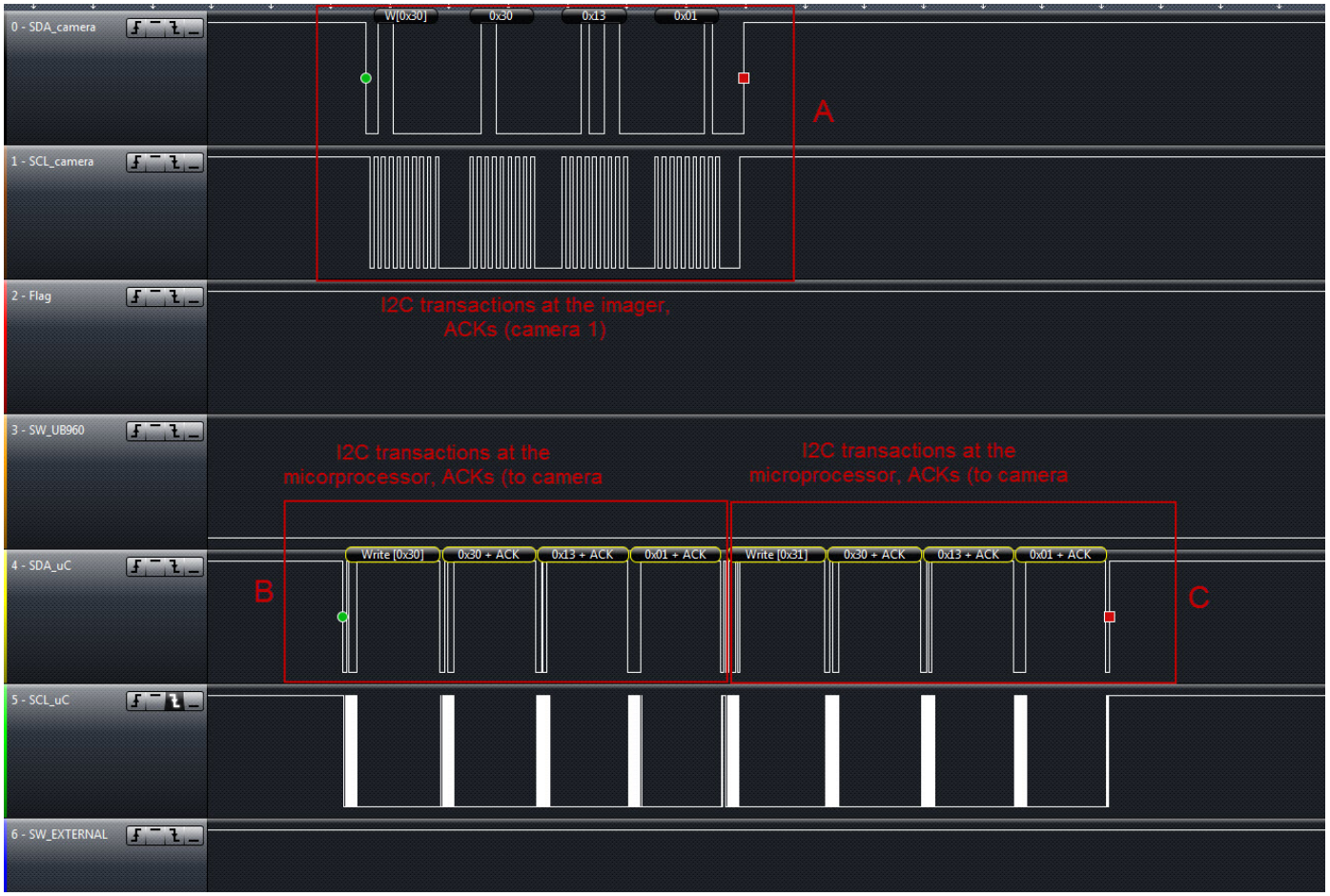


Figure 4: I2C Transactions

The box labeled B contains the first write from the microprocessor. It is addressed to address 0x30, the register address is 0x3013 and the data to be written is 0x1. Since the address is 0x30, the logic on the deserializer passes this transaction to the first camera in the system. It is routed to the imager, and the address is aliased to 0x30.

In box A, you can see the same communication, slightly delayed. This is the communication present on the camera 1 I2C bus, measured at the imager.

The write to address 0x31 in box C is for camera 2. (see figure 20) The deserializer on the ECU board passes this transaction to camera 2 and the address is aliased to 0x30. As you can see, this transaction is not present on the camera 1 I2C bus, because it is not intended for this camera.

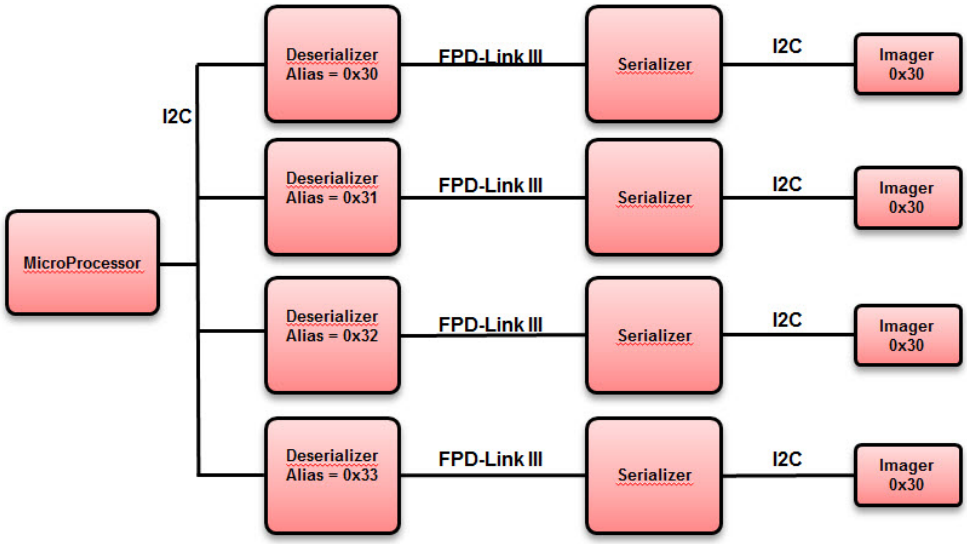


Figure 20: I2C Address Aliasing

By acknowledging the I2C write, the imager has confirmed that it is present and alive. Reading the status registers can confirm the status of the imager as well as verify that the correct imager was installed during assembly.

8 Design Files

8.1 Schematics

To download the Schematics or to view them as a high resolution PDF file, see http://www.ti.com/tool/tida-00421

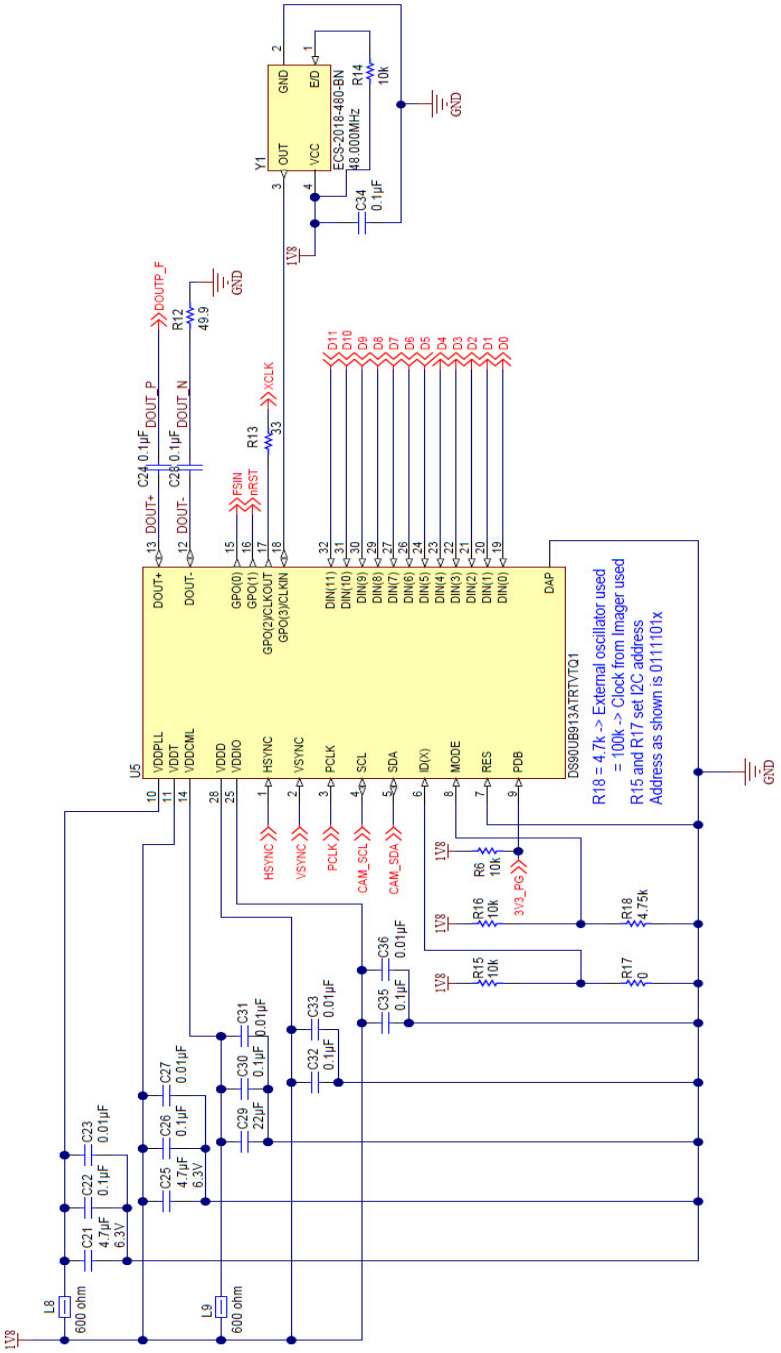


Figure 21: Serializer Schematic

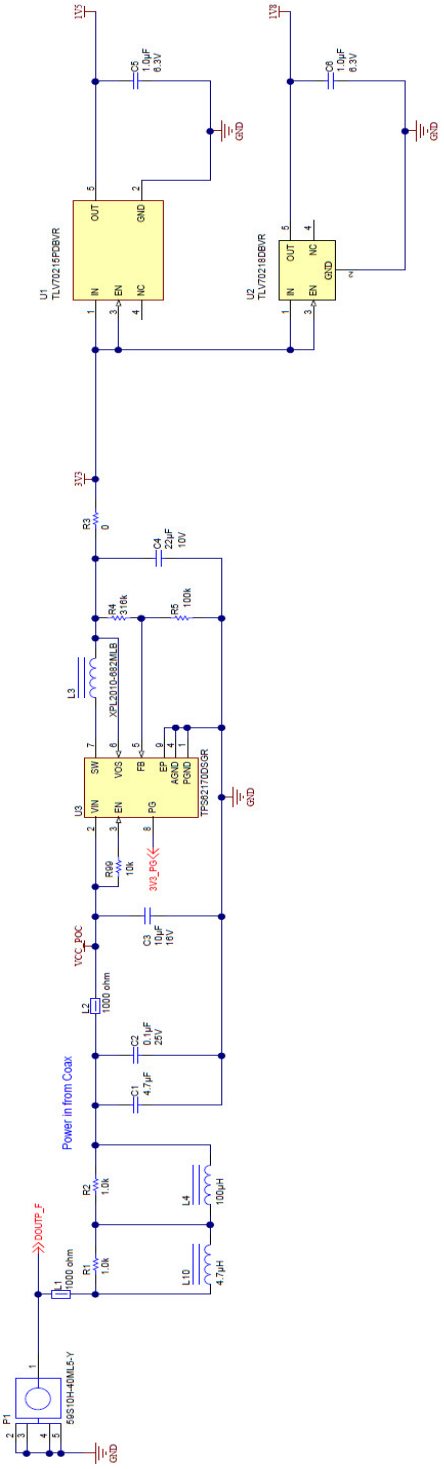


Figure 22: Coax Connection and Power Supplies Schematic

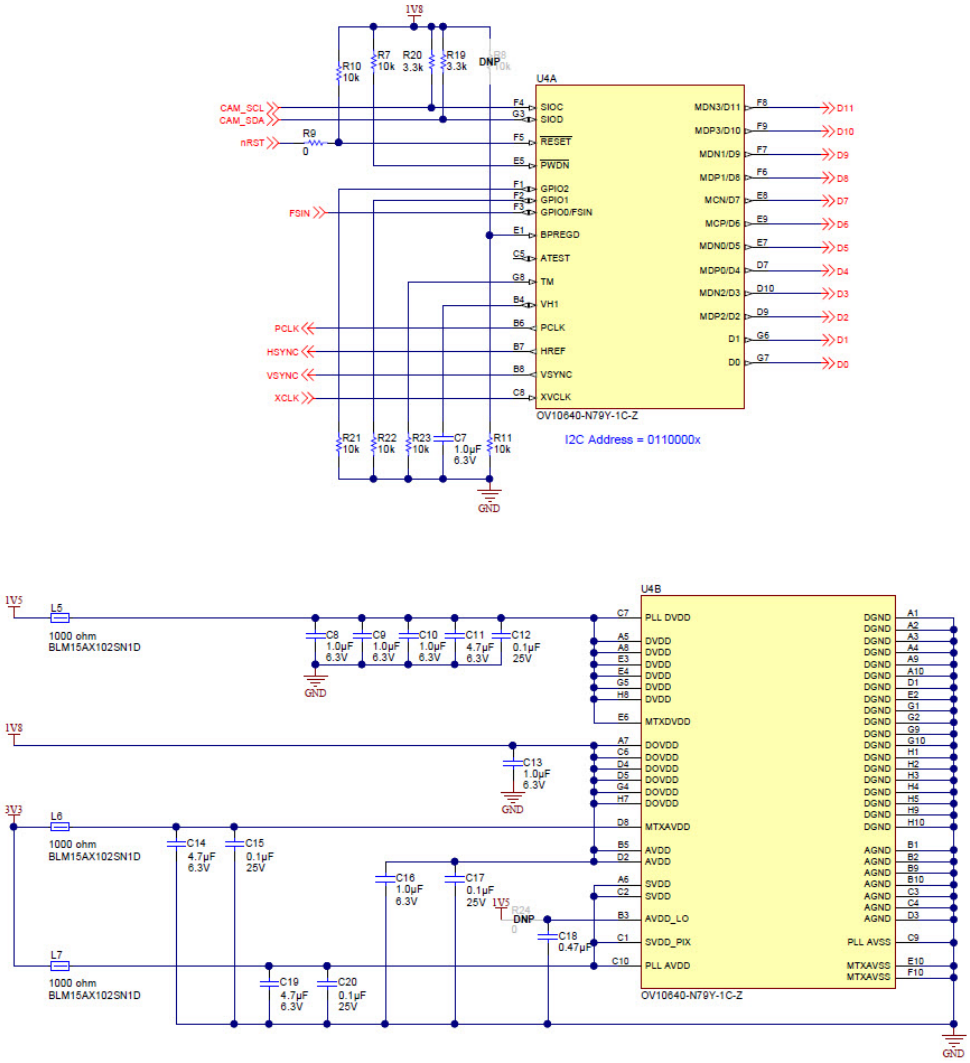


Figure 23: Imager Schematic

8.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at http://www.ti.com/tool/tida-00421

Table 1: TIDA-00421 BOM

Comment	Description	Designator	Footprint	LibRef	Quantity
Printed Circuit Board	Printed Circuit Board	!PCB1		PCB	1
CGA4J1X7R1E475M125AC	CAP, CERM, 4.7uF, 25V, +/-20%, X7R, 0805	C1	0805L	C2012X7R1E474K	1
C1005X7R1E104K050BB	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0402	C2, C12, C15, C17, C20	0402L	C1005X7R1E103K	5
CL21B106KOQNNNE	CAP, CERM, 10 µF, 16 V, +/- 10%, X7R, 0805_140	C3	0805_140	CL21B106KOQNNNE	1
GRM31CR71A226KE15L	CAP, CERM, 22uF, 10V, +/-10%, X7R, 1206	C4, C29	1206L	GRM31CR71A226KE15L	2
CL05B105KQ5NQNC	CAP CER 1UF 6.3V 10% X7R 0402	C5, C6	0402	Capacitor	2
CL05B105KQ5NQNC	CAP CER 1UF 6.3V 10% X7R 0402	C7, C8, C9, C10, C13, C16	0402L	Capacitor	6
CL10B475KQ8NQNC	CAP CER 4.7UF 6.3V 10% X7R 0603	C11, C14, C19, C21, C25	0603L	Capacitor	5
GRM155R60J474KE19D	CAP, CERM, 0.47 µF, 6.3 V, +/- 10%, X5R, 0402	C18	0402	GRM155R60J474KE19D	1
GRM155R71C104KA88D	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0402	C22, C26, C30, C32, C34, C35	0402L	GRM155R71C104KA88D	6
GRM155R71C103KA01D	CAP, CERM, 0.01uF, 16V, +/-10%, X7R, 0402	C23, C27, C31, C33, C36	0402L	GRM155R71C103KA01D	5
C1005X7R1H104K	CAP, CERM, 0.1uF, 50V, +/-10%, C0G/NP0, 0402	C24, C28	0402L	C1005X7R1H104K	2
BLM18AG102SN1D	Ferrite Bead, 1000 ohm @ 100 MHz, 0.4 A, 0603	L1, L2	0603	BLM18AG102SN1D	2
XPL2010-682MLB	Inductor, Shielded, Composite, 6.8 µH, 0.73 A, 0.42 ohm, SMD	L3	XPL2010	XPL2010-682MLB	1
CBC3225T101MR	Inductor, Wirewound, 100 µH, 0.27 A, 1.4 ohm, SMD	L4	CBC3225	CBC3225T101MR	1
BLM15AX102SN1D	Ferrite Bead, 1000 ohm @ 100 MHz, 0.35 A, 0402	L5, L6, L7	0402	BLM15AX102SN1D	3
BLM18KG601SN1D	1.3A Ferrite Bead, 600 ohm @ 100MHz, SMD	L8, L9	0603	BLM18KG601SN1D	2
CBC3225T4R7MR	Inductor, Wirewound, 4.7 µH, 1.01 A, 0.1 ohm, SMD	L10	CBC3225	CBC3225T4R7MR	1
CMT821	Sunex Lens Holder	LH1	CMT821	CMT821	1

59S10H-40ML5-Y	Straight Plug PCB	P1	59S10H-40ML5-Y	59S10H-40ML5-Y	1
CRCW06031K00JNEA	RES, 1.0k ohm, 5%, 0.1W, 0603	R1, R2	0603L	CRCW06031K00JNEA	2
CRCW04020000Z0ED	RES, 0 ohm, 5%, 0.063W, 0402	R3, R9, R17	0402L	CRCW04020000Z0ED	3
CRCW0402316KFKED	RES, 316 k, 1%, 0.063 W, 0402	R4	0402	CRCW0402316KFKED	1
CRCW0402100KFKED	RES, 100k ohm, 1%, 0.063W, 0402	R5	0402L	CRCW0402100KFKED	1
CRCW040210K0JNED	RES, 10k ohm, 5%, 0.063W, 0402	R6, R7, R10, R11, R14, R15, R16, R21, R22, R23, R99	0402L	CRCW040210K0JNED	11
CRCW040249R9FKED	RES, 49.9 ohm, 1%, 0.063W, 0402	R12	0402L	CRCW040249R9FKED	1
CRCW040233R0JNED	RES, 33 ohm, 5%, 0.063W, 0402	R13	0402L	CRCW040233R0JNED	1
	RES, 4.75k ohm, 1%, 0.063W, 0402	R18	0402L	CRCW04024K75FKED	1
CRCW06033K30JNEA	RES, 3.3k ohm, 5%, 0.1W, 0603	R19, R20	0603L	CRCW06033K30JNEA	2
TLV70215PDBVR	300-mA, Low-IQ, Low-Dropout Regulator, DBV0005A	U1	DBV0005A_N	TLV70215PDBVR	1
TLV70218DBVR	Single Output LDO, 300 mA, Fixed 1.8 V Output, 2 to 5.5 V Input, with Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br)	U2	DBV0005A_N	TLV70218DBVR	1
TPS62170DSGR	Buck Step Down Regulator with 3 to 17 V Input and 0.9 to 6 V Output, -40 to 85 degC, 8-Pin WSON (DSG), Green (RoHS & no Sb/Br)	U3	DSG0008A	TPS62170DSGR	1
OV10640-N79Y-1C-Z	1/2.56" color CMOS 1.3 megapixel HDR HD image sensor, BGA78	U4	OVT_10640_aCSP	OV10640-N79Y-1C-Z	1
DS90UB913ATRTVTQ1	DS90UB913A-Q1/DS90UB914A-Q1 25 to 100 MHz 10/20-Bit FPD-Link III Serializer and Deserializer, RTV0032A	U5	RTV0032A	DS90UB913ATRTVTQ1	1
ECS-2018-480-BN	XO, 48.000MHz, 1.8V, SM	Y1	ECS_2018	ECS-2018-480-BN	1

8.3 PCB Layout Recommendations

8.3.1 Switching DC-DC Converter

During part placement and routing, it is helpful to always consider the path the current will be taking through the circuit. The yellow line in figure 24 shows the current path in through the input filter, the switch in the converter, Inductor L3, and then out to R3 across the output capacitor (C4). Any return currents from the input capacitor (C3) or the output capacitor (C4) are joined together on the top side of the board before they are connected to the ground (return) plane. (inside the green circle) This will reduce the amount of return currents, and thereby, voltage gradients in the ground plane. This may not be noticeable in the performance of the converter, but it will reduce its coupled noise into other devices.

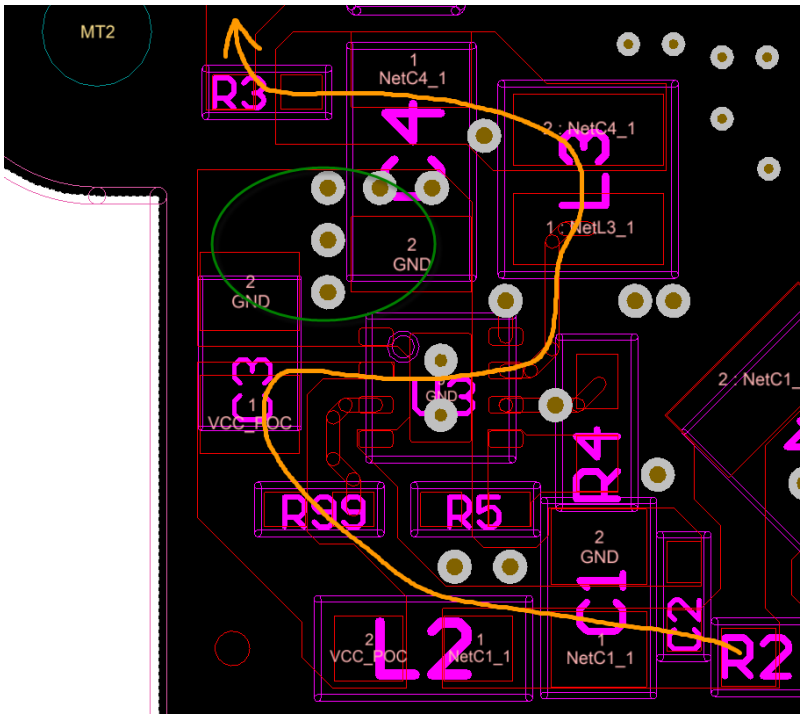
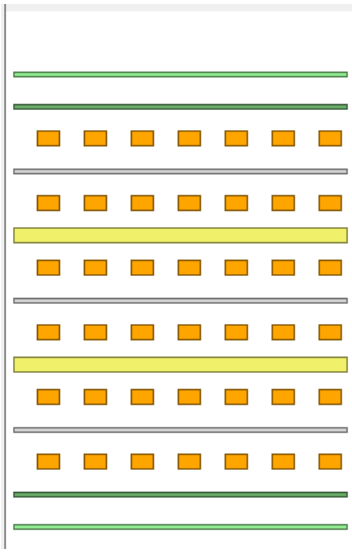


Figure 24: Routing FB traces around SW nodes

Input capacitors should be placed as close to the IC as possible to reduce the parasitic series inductance from the capacitor to the device it is supplying. This is especially important for DCDC converters as the inductance from the capacitor to the high-side switching FET can cause high voltage spikes and ringing on the switch node, which can be damaging to components and cause problems for EMI.

8.3.2 PCB Layer Stackup Recommendations

- Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines
- If using a 4 layer board, layer 2 should be a ground plane. Since most of the components/switching currents are on the top layer, this reduces the inductive effect of the vias when currents are returned through the plane.
- An additional two layers were used in this board to simplify BGA fan out and routing. Here is the stack-up used in this board:



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Layer 1 - Top Lay...	Signal	Copper	1.4		
Dielectric 1	Dielectric	Prepreg	12.6	370HR	4.2
Layer 2 - GND	Signal	Copper	1.4		
Dielectric 2	Dielectric	Core	8	370HR	4.2
Layer 3 - Signal	Signal	Copper	1.417		
Dielectric 3	Dielectric	Prepreg	16.6	370HR	4.2
Layer 4 - Signal	Signal	Copper	1.417		
Dielectric 4	Dielectric	Core	8	370HR	4.2
Layer 5 - PWR	Signal	Copper	1.4		
Dielectric 5	Dielectric	Prepreg	12.6	370HR	4.2
Layer 6 - Bottom...	Signal	Copper	1.4		
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

Figure 25: Layer stack up

8.3.3 Serializer Layout Recommendations

Decoupling capacitors need to be located very close to the supply pin on the serializer. Again, this requires that you consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. Smaller value capacitors that provide higher frequency decoupling should be placed closest to the device.

Figure 26 shows the supply current from C31 in yellow. The green line is the return path. The cross sectional area of this loop is very small. A similar sketch for C29 would show a larger loop.

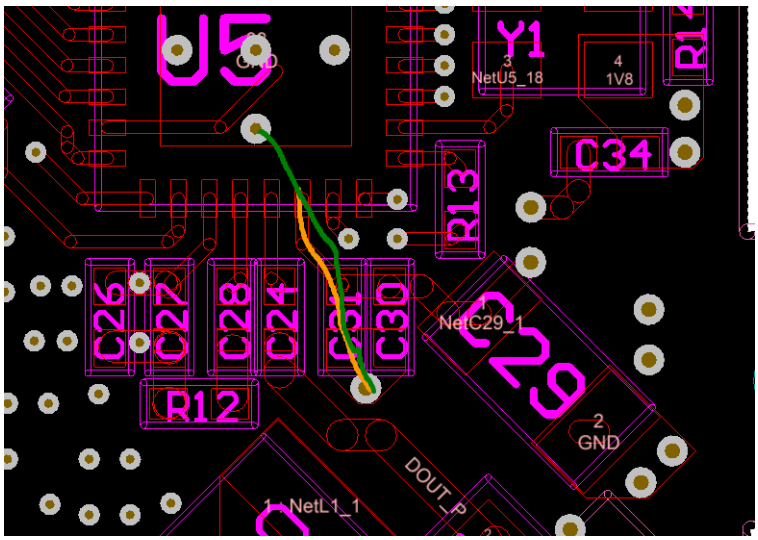


Figure 26: Decoupling Current Loop

For this application, a single-ended impedance of 50Ω is required for the coax interconnect. Whenever possible, this connection should also be kept short. The routing of the high speed serial line is shown in figure 27. It is highlighted in white. The total length between the two yellow arrows is about ½ inch.

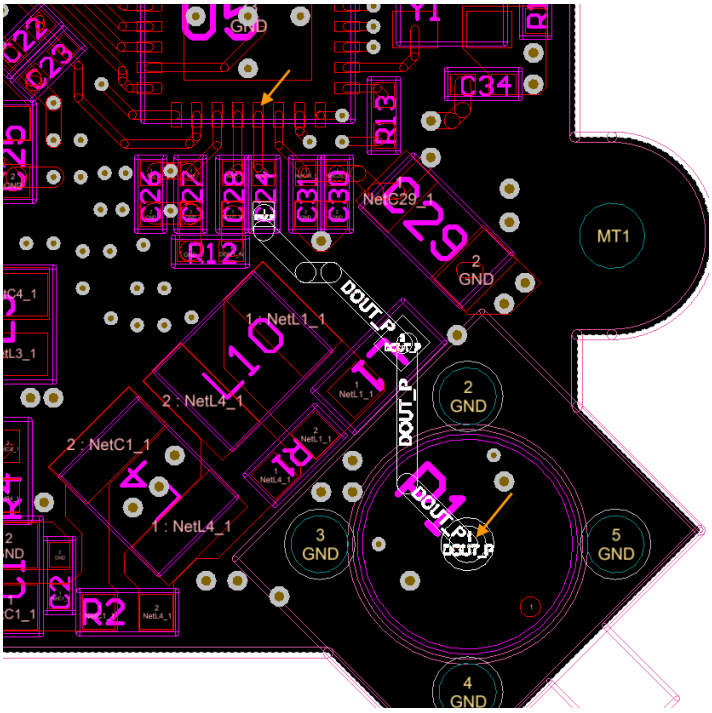


Figure 27: Decoupling Current Loop

8.3.4 TIDA-00421 Layer Artwork

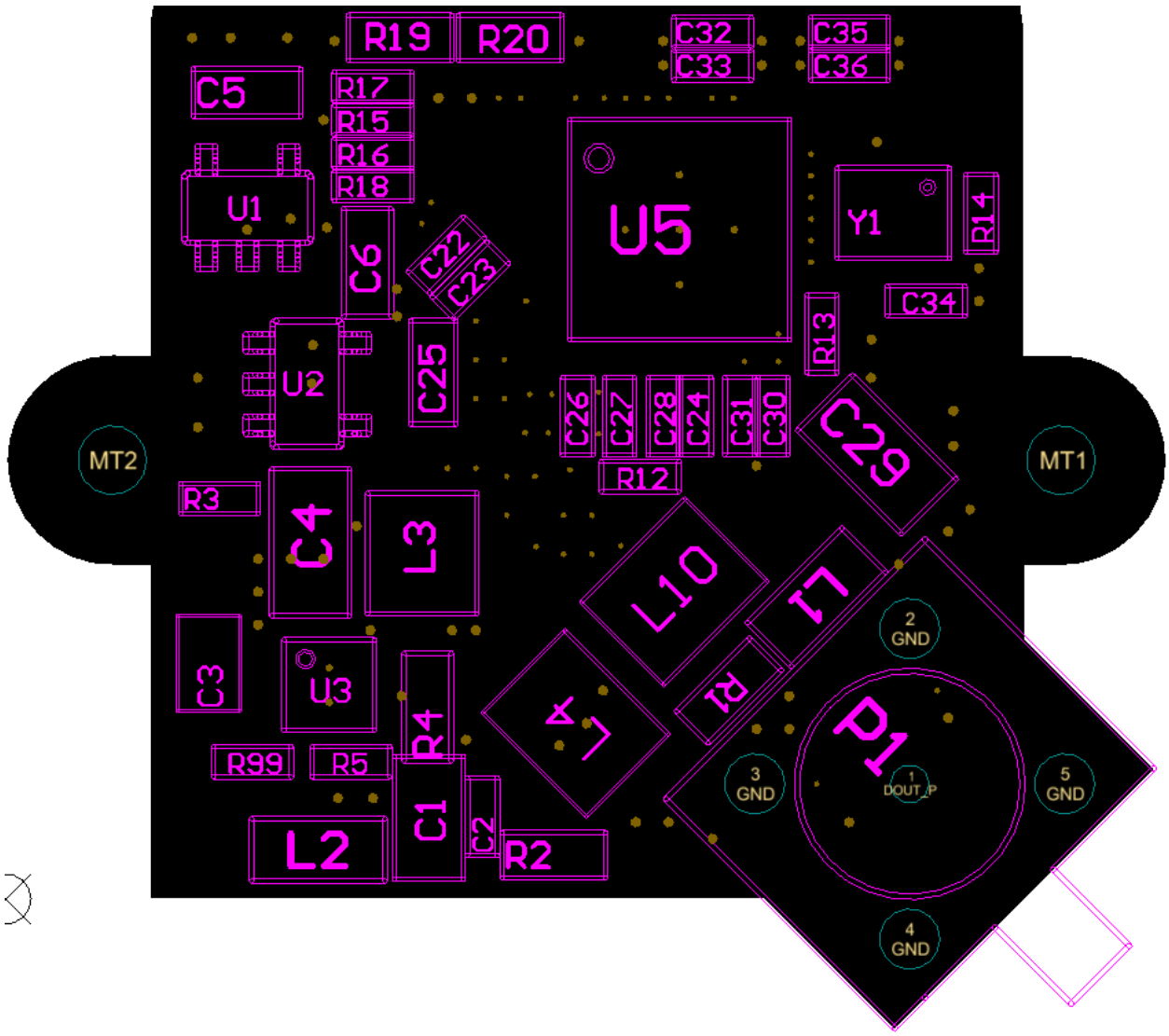


Figure 35: Layer: Assembly Top

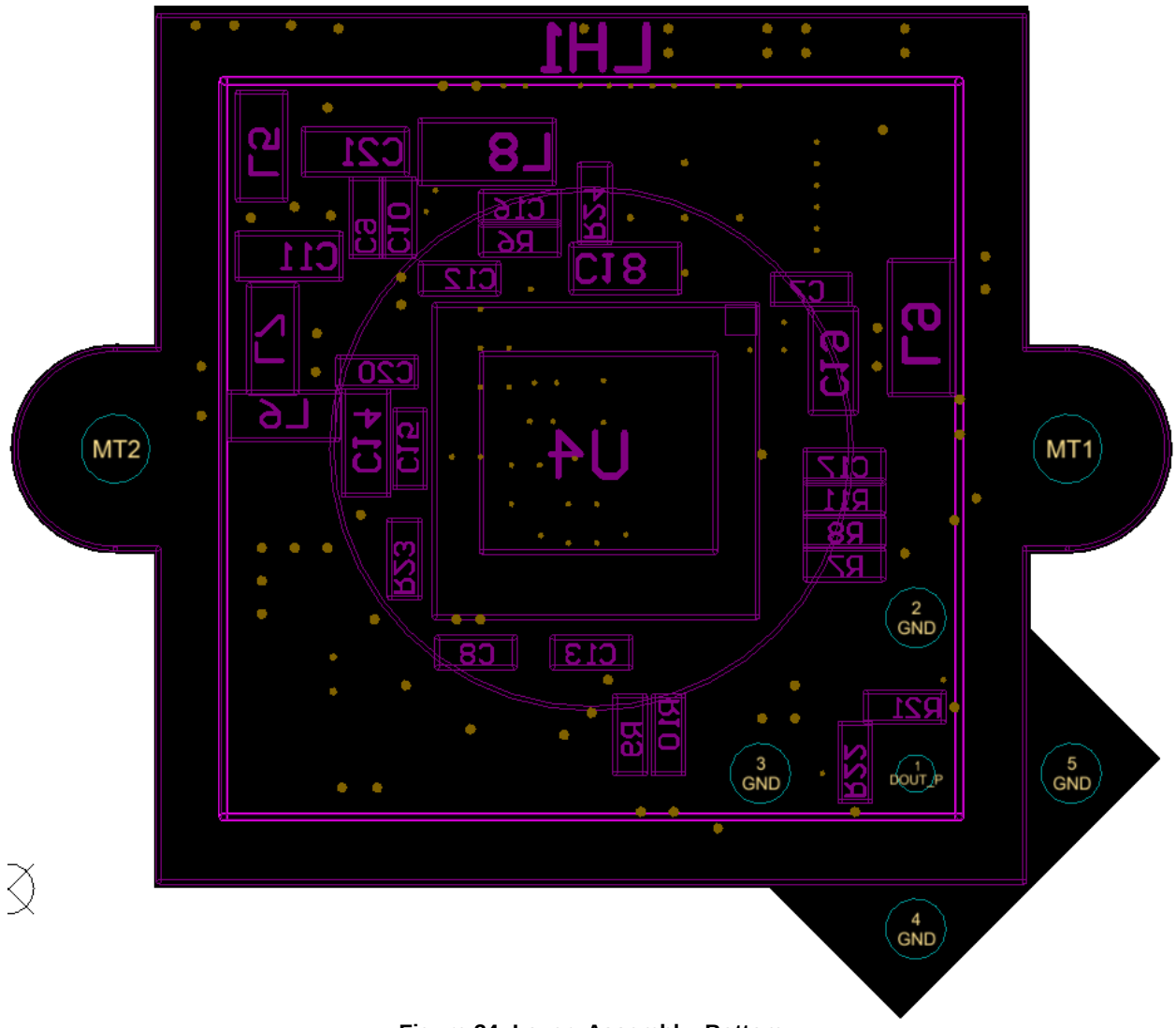


Figure 34: Layer: Assembly, Bottom

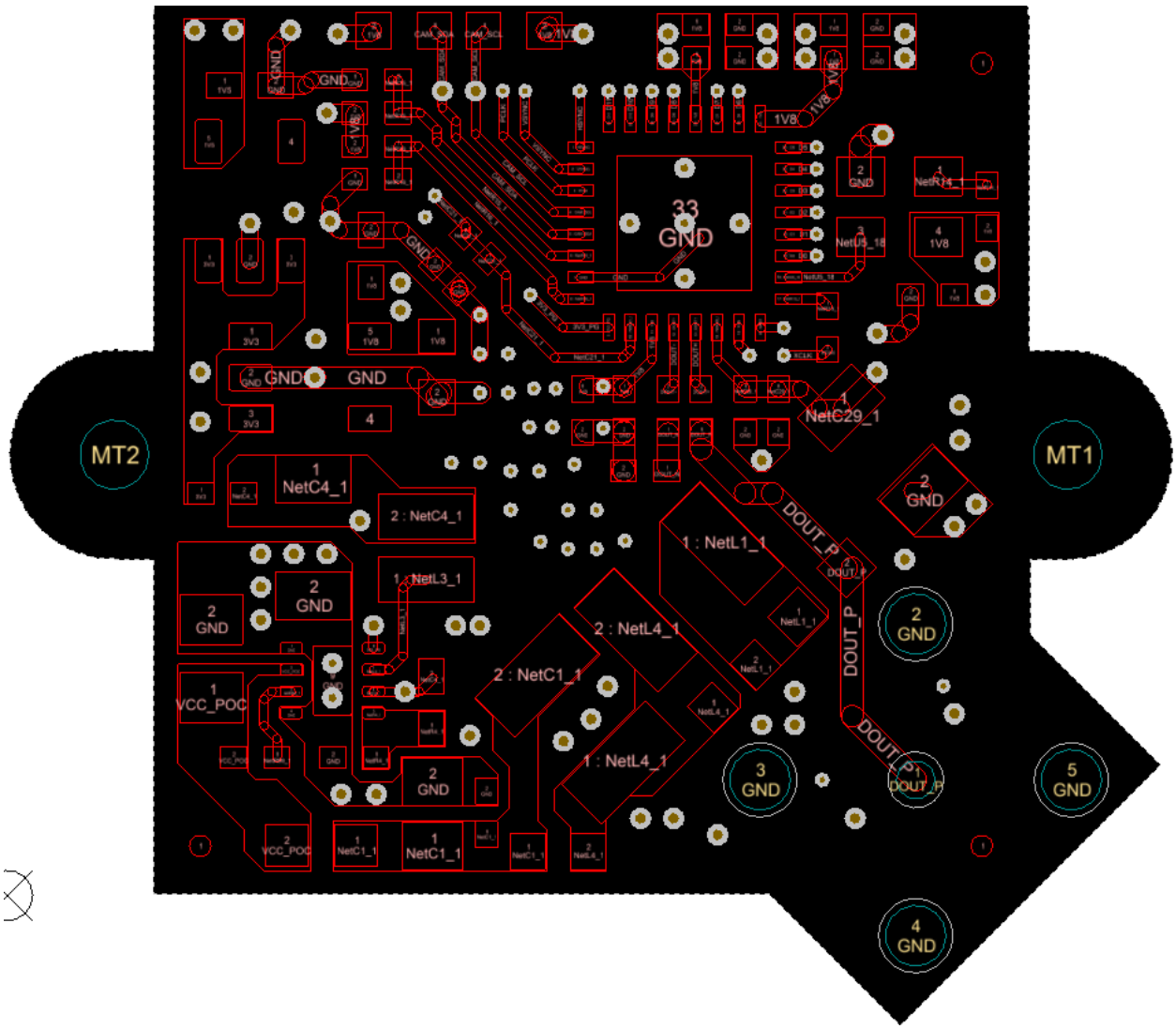


Figure 28: Layer 1: Top

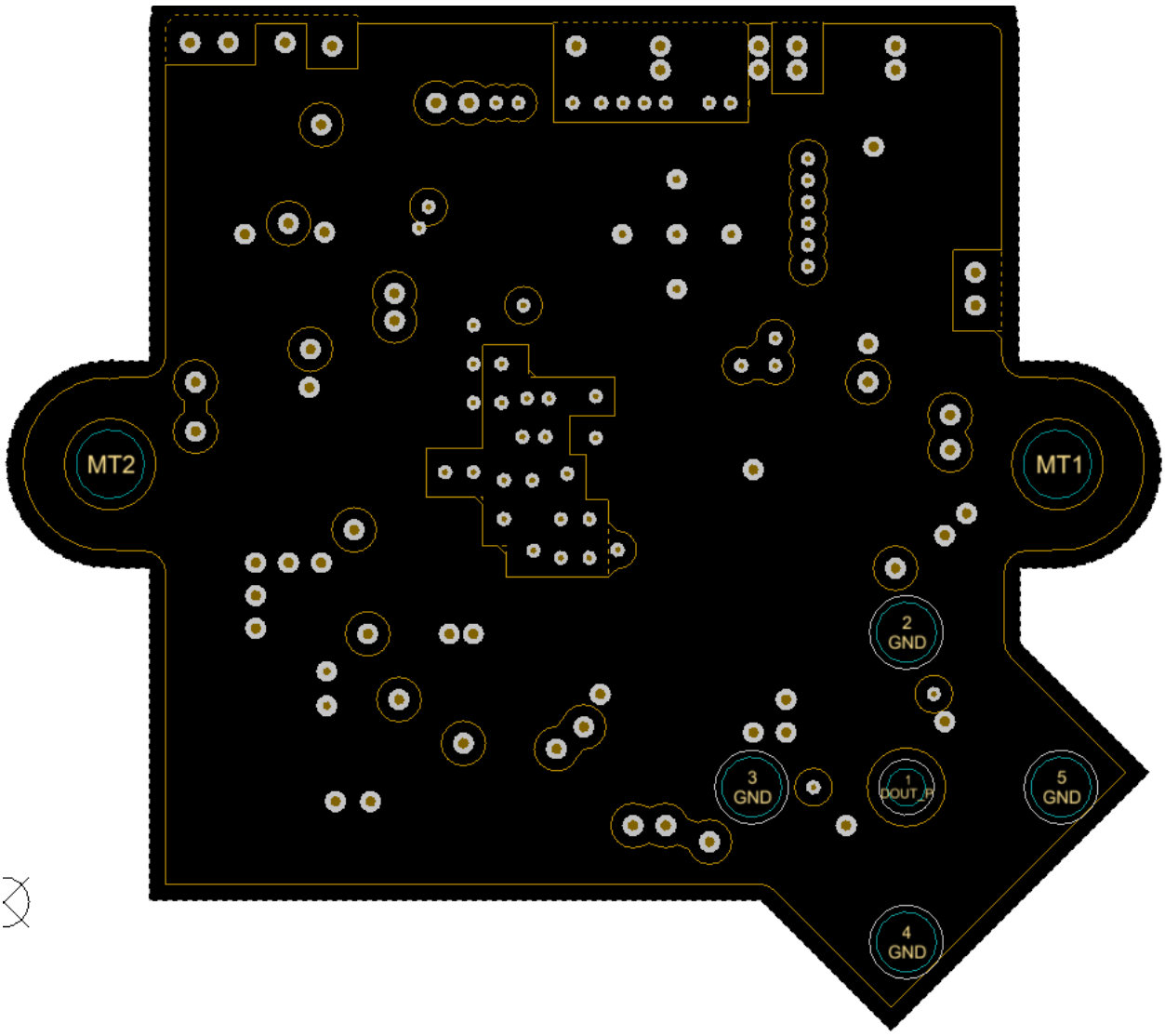


Figure 29: Layer 2: GND

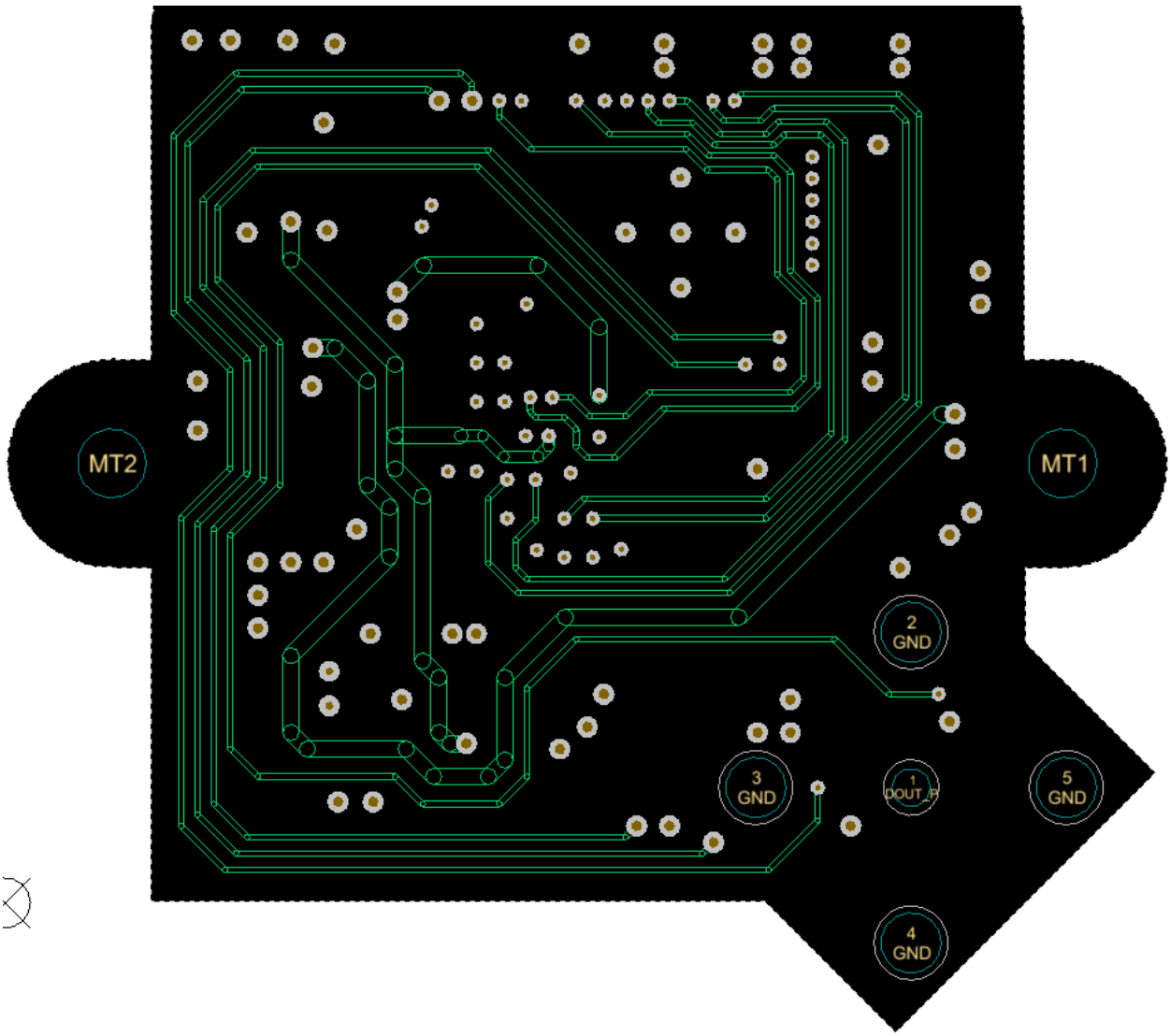


Figure 30: Layer 3: Signal

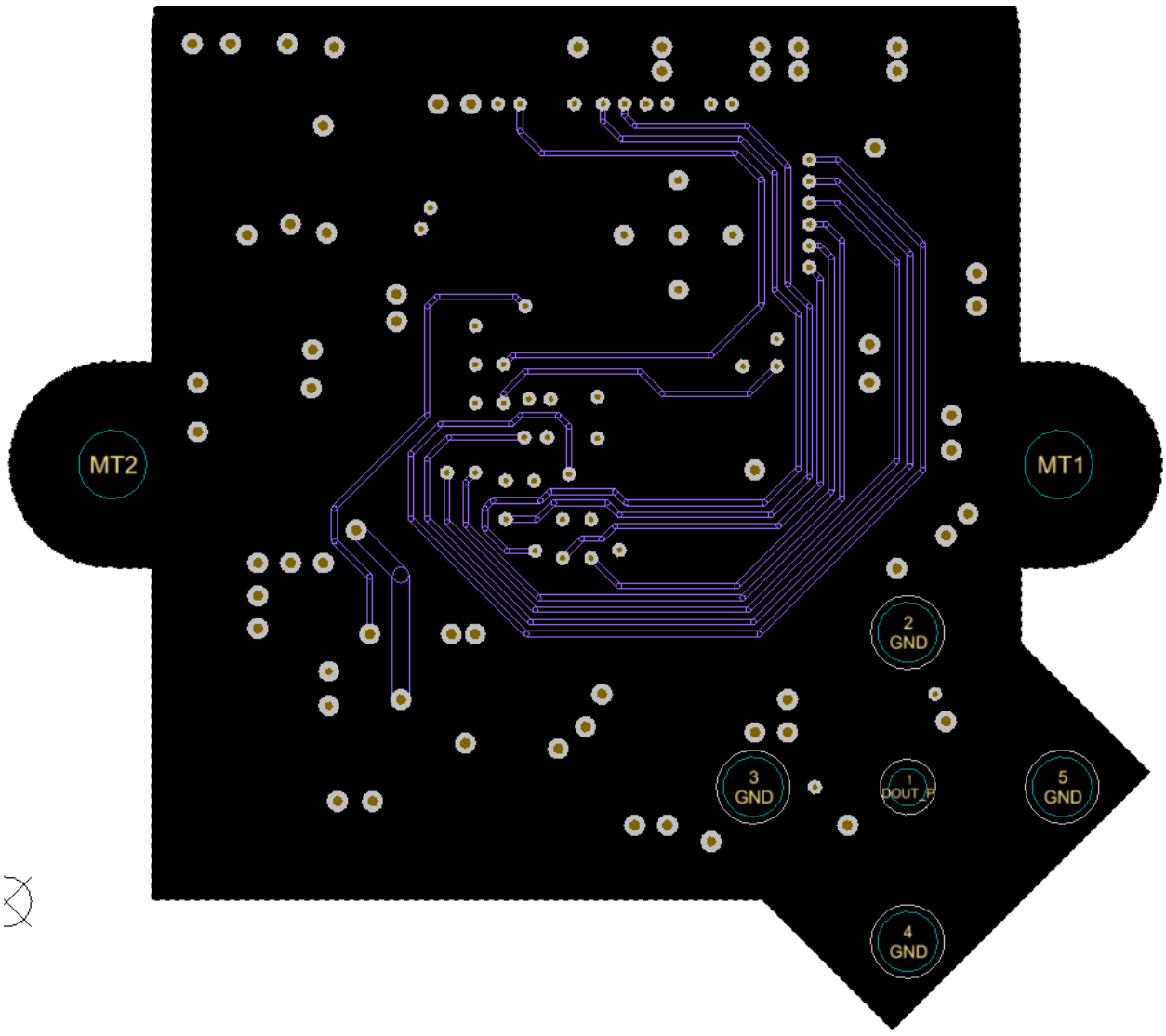


Figure 31: Layer 4: Signal

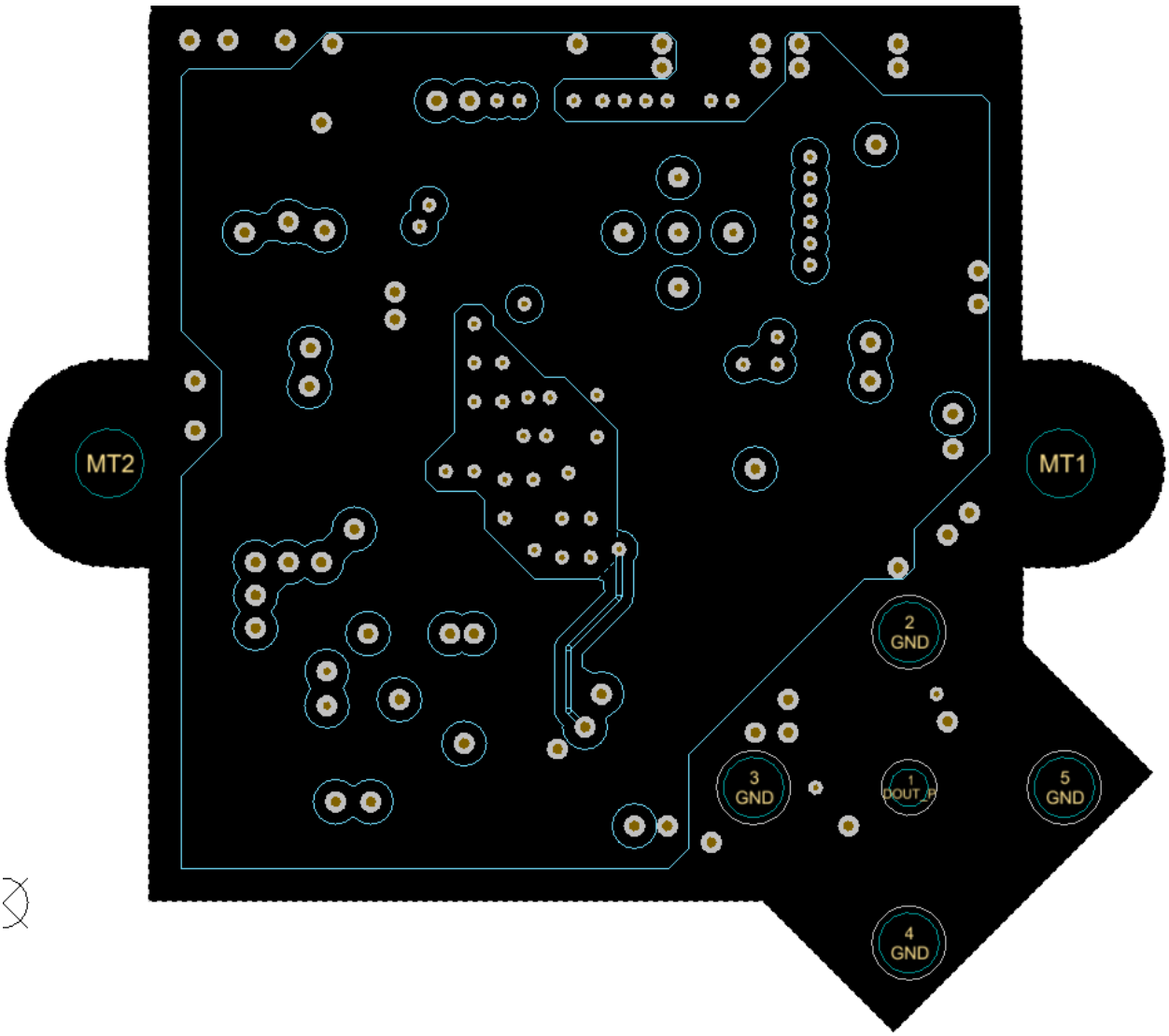


Figure 32: Layer 5: Power

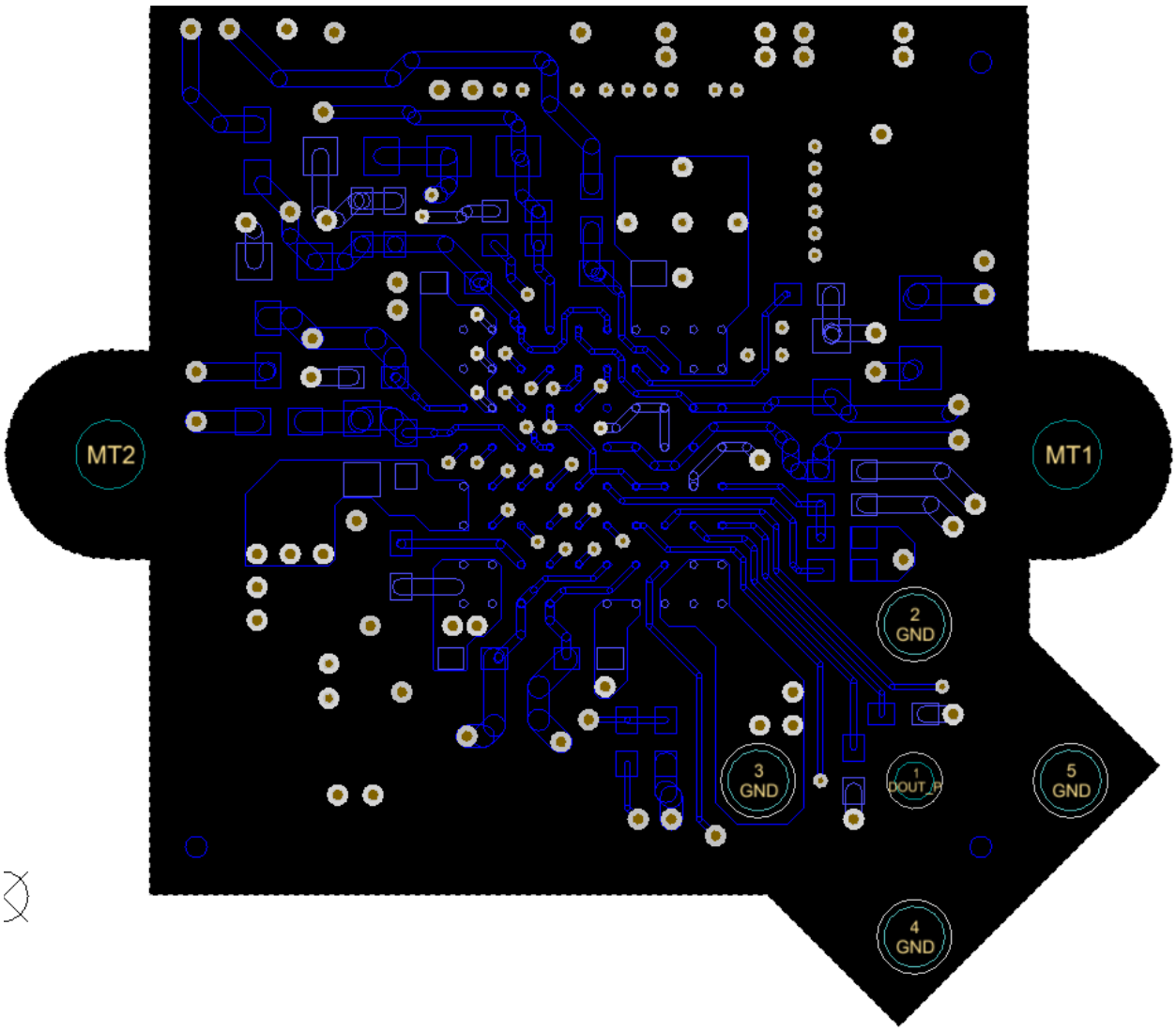


Figure 33: Layer 6: Bottom

To download the Altium project & Gerber files for each board, see the design files at
http://www.ti.com/tool/tida-00421

9 References

1. DS90UB913A-Q1 datasheet (http://www.ti.com/product/DS90UB913A-Q1)
2. TPS62170-Q1 datasheet (http://www.ti.com/product/tps62170-q1)
3. TLV70215-Q1 datasheet (http://www.ti.com/product/TLV702-Q1)
4. TLV70218-Q1 datasheet (http://www.ti.com/product/TLV702-Q1)
5. "Sending Power Over Coax in DS90UB913A Designs", Texas Instruments Application Note, literature number SNLA224. (http://www.ti.com/lit/an/snla224/snla224.pdf)
6. "Cable Requirements for the DS90UB913A & DS90UB914A", Texas Instruments Application Note, literature number SNLA229. (http://www.ti.com/lit/an/snla229/snla229.pdf)
7. "Optimizing the TPS62130/40/50/60/70 Output Filter", Texas Instruments Application Note, literature number SLVA463. (http://www.ti.com/lit/an/slva463a/slva463a.pdf)

10 Terminology

11 About the Author

Brian Shaffer is a Systems Engineer at Texas Instruments. As a member of the Automotive Systems Engineering team, Brian focuses on ADAS (Advanced Driver Assistance Systems) end-equipments, creating reference designs for top automotive OEM and Tier 1 manufacturers. He brings to this role experience in high reliability infrared cameras, power supplies for portable devices, cameras for automotive platforms, and embedded systems design. Brian earned his Bachelor of Science in Electrical Engineering from Kansas State University in Manhattan, KS.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265