TI Designs

Automotive Off-Battery Infotainment Processor Power Reference Design

Design Overview

This reference design is a full off-battery to point-of-load power solution supporting input voltages as low as 2 V. The design uses the Boost plus Buck DC/DC regulator TPS43330A-Q1 supporting an input voltage range of 2 V to 40 V and allowing the design to support not only start-stop, but also crank conditions. The TPS659039-Q1 integrated power management device supplies point-of-load power to an application processor, such as DRA74x/DRA75x. Also included is a 5 V/4 A load switch, the TPS22965-Q1, and a linear regulator, TPS51200-Q1, for double-data-rate (DDR) termination supply.

Design Resources

TIDA-00801	Design Folder
TPS43330A-Q1	Product Folder
TPS659039-Q1	Product Folder
TPS22965-Q1	Product Folder
TPS52100-Q1	Product Folder

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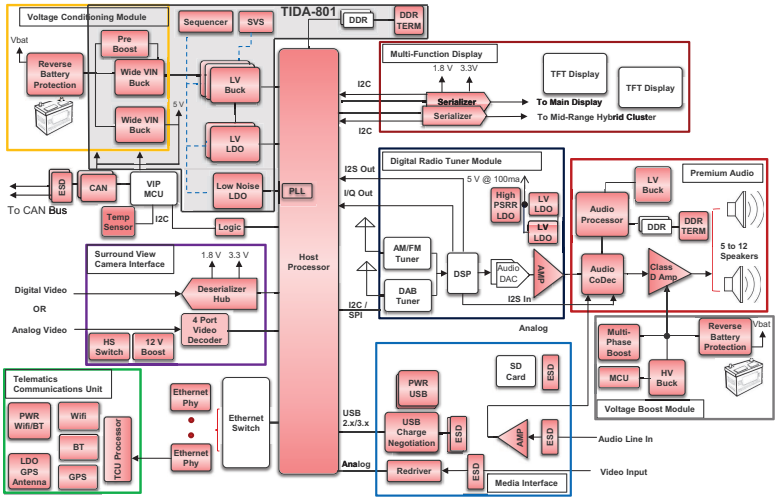
Design Features

- Supports Cold and Warm Cranking
- Supports Modern Processors Sequencing Needs Without Further Logic
- Supports Peripherals
- Small Form Factor
- Low System-Cost Solution

Featured Applications

- Hybrid Clusters
- Head Units with Remote Displays
- Head Units with Integrated Displays
- Advanced Driver Assistant Systems (ADAS) Fusion Systems
- Telematics Communications Units (TCU)
- Head Units
- Automotive Entertainment



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1 Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Pre-Regulator	Provides regulated 3.3 V at 4 A and 5 V at 2 A from a battery-input between 4 V and 40 V	See Section Section 4.1.
Power Management IC (PMIC)	Provides various output voltages and digital signals in the correct order with the correct timing	See Section Section 4.2.
Load-Switch	Turns on to provide I/O voltage upon a signal from the PMIC (up to 2.5 A)	See Section Section 4.3.
DDR-Termination	Provides appropriate termination voltage for the selected DDR-voltage (SMPS3 of PMIC) at 1 A	See Section Section 4.4.

2 System Description

In automotive systems, the entertainment system, information systems (like navigation), and also recently the ADAS are merged. Additionally, with start-stop-systems becoming more common, the availability of the system during (warm-) cranking events is essential.

This reference design is a full power solution for an infotainment system, which takes an input connected to a car battery and provides output supplies to the point of load. The design uses the pre-regulator TPS43330A-Q1 supporting inputs ranging from 2 V to 40 V and as such supports cranking, and the TPS659039-Q1 integrated power management IC to supply the application processor such as TDA2x/DRA7xx and its peripherals. The design also includes the load switch TPS22965-Q1 and linear regulator TPS51200-Q1 for DDR-termination supply.

2.1 TPS43330A-Q1

In order to provide the two high-current rails (3.3 V at 4 A and 5 V at 2 A) for the downstream supplies while maintaining cranking support down to 4 V on the battery supply, the TPS43330A-Q1 was chosen. The device includes two current-mode synchronous-buck controllers and a voltage-mode boost controller. See Figure 1. The device is ideally suited as a pre-regulator stage with low IQ requirements and for applications that must survive supply drops due to cranking events. The integrated boost controller allows the device to operate down to 2 V at the input, without seeing a drop on the buck regulator output stages. For this design, external components were chosen to support a minimum input voltage of 4 V, which is sufficient in most warm-cranking scenarios, at light loads, the buck controllers enable operate automatically in low-power mode, consuming just 30 µA of quiescent current.

Using a controller offers scalability and the combination of a pre-boost and two buck-controllers is ideal for this application. In case of AM-band-usage, the relatively low-switching frequency and harmonics in AM-band can be accounted for with an external clock-synchronization, as to avoid particular frequencies on the fly. Figure 1 shows a simplified schematic of the TPS43330A-Q1 device.

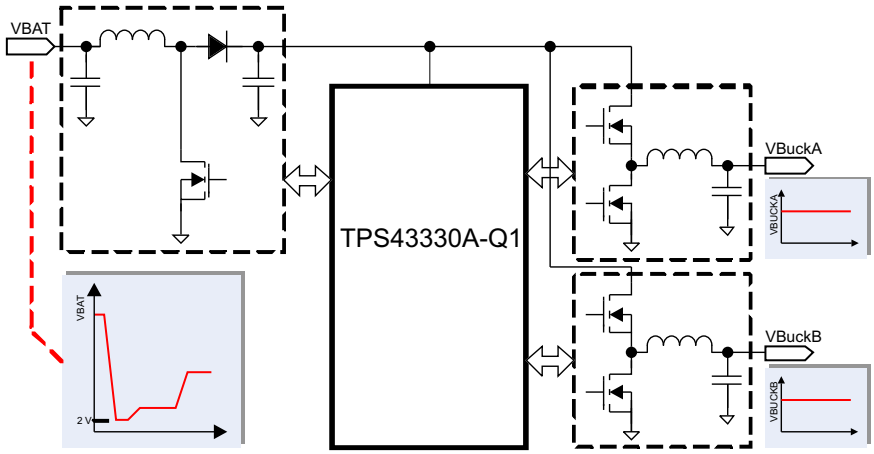


Figure 1. Simplified TPS43330A-Q1 Schematic

2.2 TPS659039-Q1

The TPS659039-Q1 device has integrated power-management integrated circuits (PMICs) for automotive applications, see Figure 2. The device provides seven configurable step-down converters with up to 6 A of output current for memory, processor core, input-output (I/O), or preregulation of LDOs. One of these configurable step-down converters can be combined with another 3-A regulator to allow up to 9 A of output current. All of these step-down converters can synchronize to an external clock source between 1.7 Mhz and 2.7 MHz, or an internal fall back clock at 2.2 MHz. The TPS659039-Q1 device contains six low dropout (LDO) regulators for external use. These LDO regulators can be supplied from either a system supply or a preregulated supply. The power-up and power-down controller is configurable and supports any power-up and power-down sequences (one-time programmable [OTP] based). The TPS659039-Q1 device includes a 32-kHz RC oscillator to sequence all resources during power up and power down. In cases where a fast startup is needed, a 16-MHz crystal oscillator is also included to quickly generate a stable 32-kHz for the system. All LDOs and switched-mode power supply (SMPS) converters can be controlled by the serial peripheral interface (SPI) or I^2C interface, or by power request signals. In addition, voltage scaling registers allow transitioning the SMPS to different voltages by SPI, I^2C, or roof and floor control. One dedicated pin in each package can be configured as part of the power-up sequence to control external resources. General-purpose input-output (GPIO) functionality is available and two GPIOs can be configured as part of the power-up sequence to control external resources. Power request signals enable power mode control for power optimization. The device includes a general-purpose (GP) sigma-delta analog-to-digital converter (ADC) with three external input channels. The TPS659039-Q1 device is available in a 13-ball × 13-ball nFBGA package with a 0.8-mm pitch. Figure 2 shows a simplified schematic of the TPS659039-Q1 device.

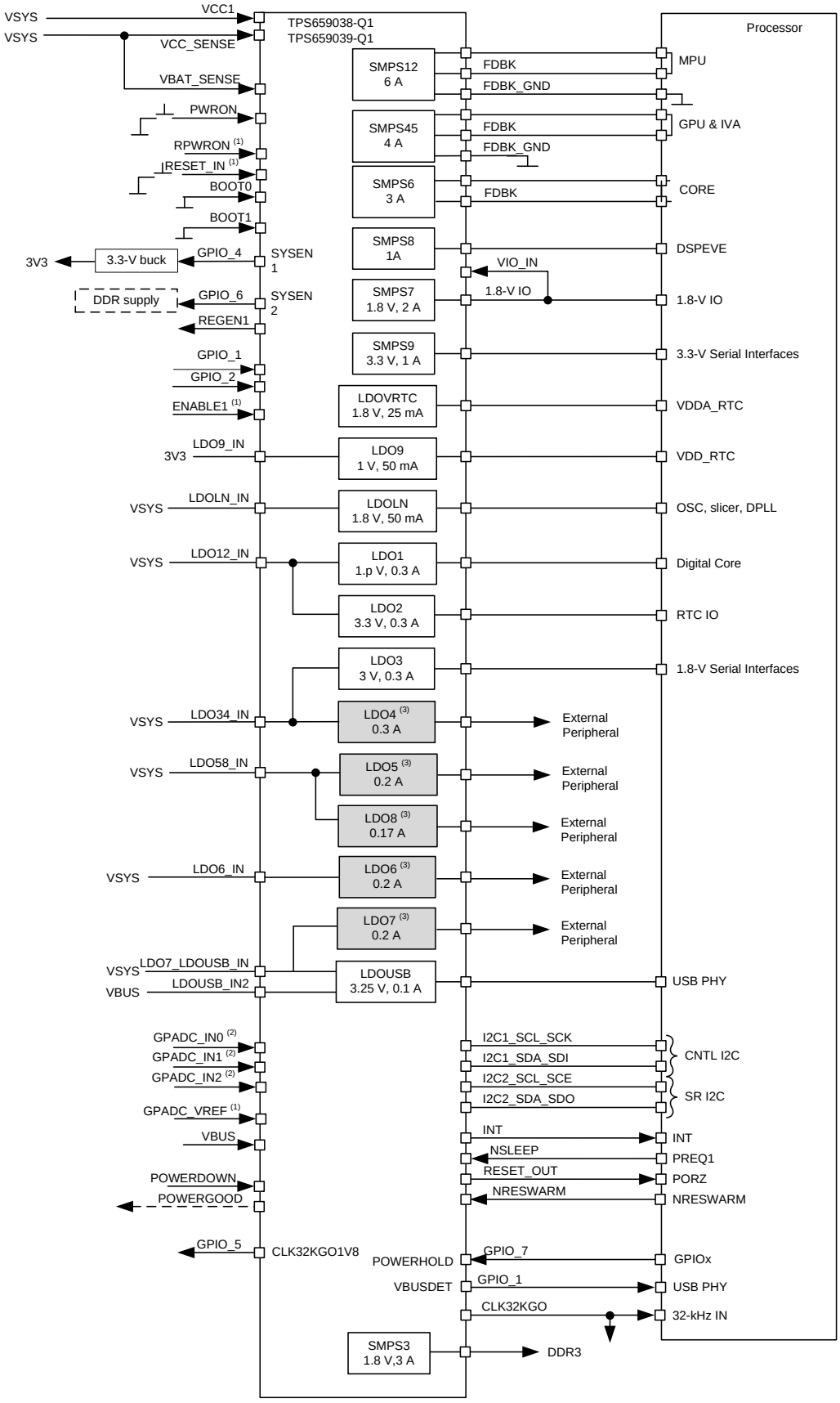


Figure 2. Simplified TPS659039-Q1 Schematic

2.3 TPS22965-Q1

The TPS22965x-Q1 is a small, ultra-low R_{ON}, single channel load switch with controlled turn on. The device contains an N-channel MOSFET that can operate over an input- voltage range of 0.8 V to 5.5 V and can support a maximum continuous current of 4 A. The VOUT rise time is configurable so that inrush current may be reduced. For quick output discharge when the switch is turned off, the TPS22965-Q1 includes a 225-Ω on-chip load resistor. This device has been selected for its size, cost, and performance. Selection of the device is also because it matches the following key criteria:

- Soft-start feature to limit inrush-currents
- Active discharge to maintain the power-down sequence demanded by the controller
- Low RDSon for the highest efficiency and lowest voltage drop

Figure 3 shows a simplified schematic of the TPS22965-Q1 device.

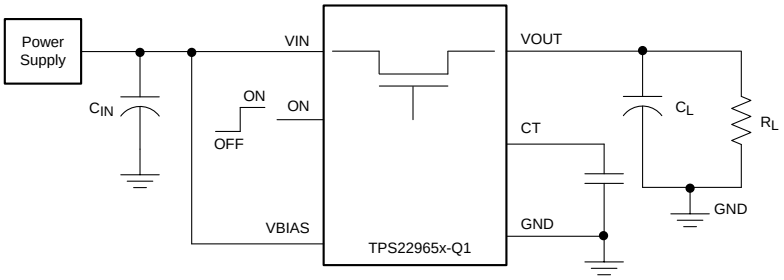


Figure 3. Simplified TPS22965-Q1 Schematic

2.4 TPS51200-Q1

The TPS51200-Q1 device is a sink and source DDR-termination regulator specifically designed for low-input voltage, low-cost, low-noise systems where space is a key consideration. The device supports a remote-sensing function and all power requirements for DDR, DDR2, DDR3, and Low Power DDR3 and DDR4 VTT bus termination. In this design, the Options are predefined by the PMIC, which supports DDR3 and DDR3LV. The part was chosen for cost and space reasons and because it is easy-to-use. Figure 4 shows a simplified schematic of the TPS51200-Q1 device.

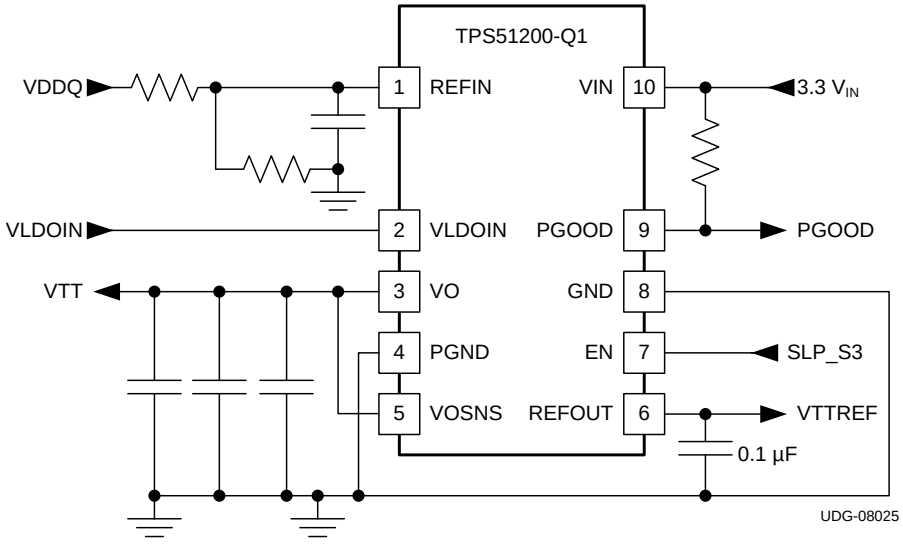
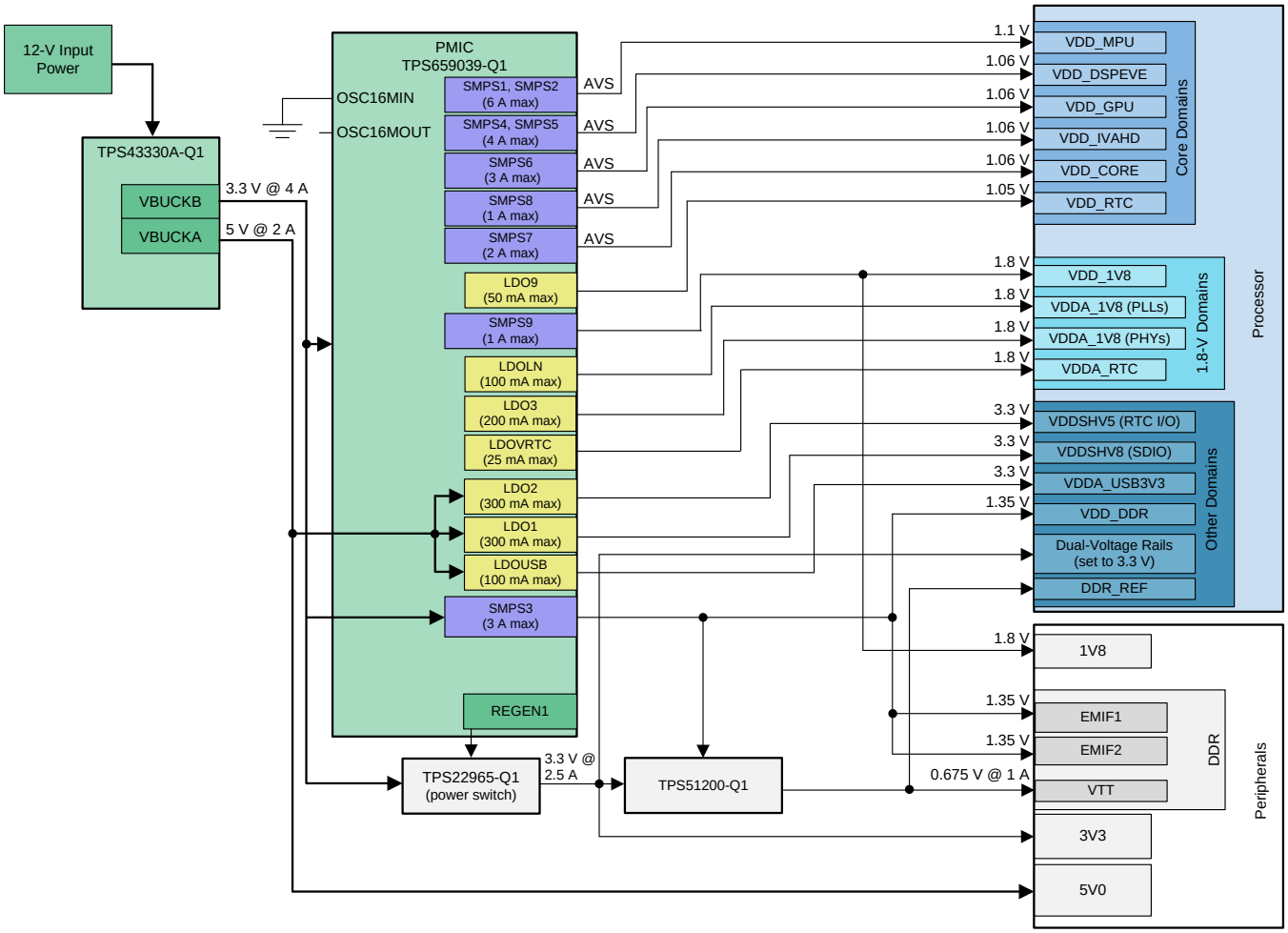


Figure 4. Simplified TPS51200-Q1 Schematic

3 Block Diagram



3.1 Highlighted Products

The reference design features the following devices:

- TPS43330A-Q1
- TPS659039-Q1
- TPS22965-Q1
- TPS51200-Q1

For more information on each of these devices, see the respective product folders at http://www.ti.com.

3.1.1 TPS43330A-Q1 Features

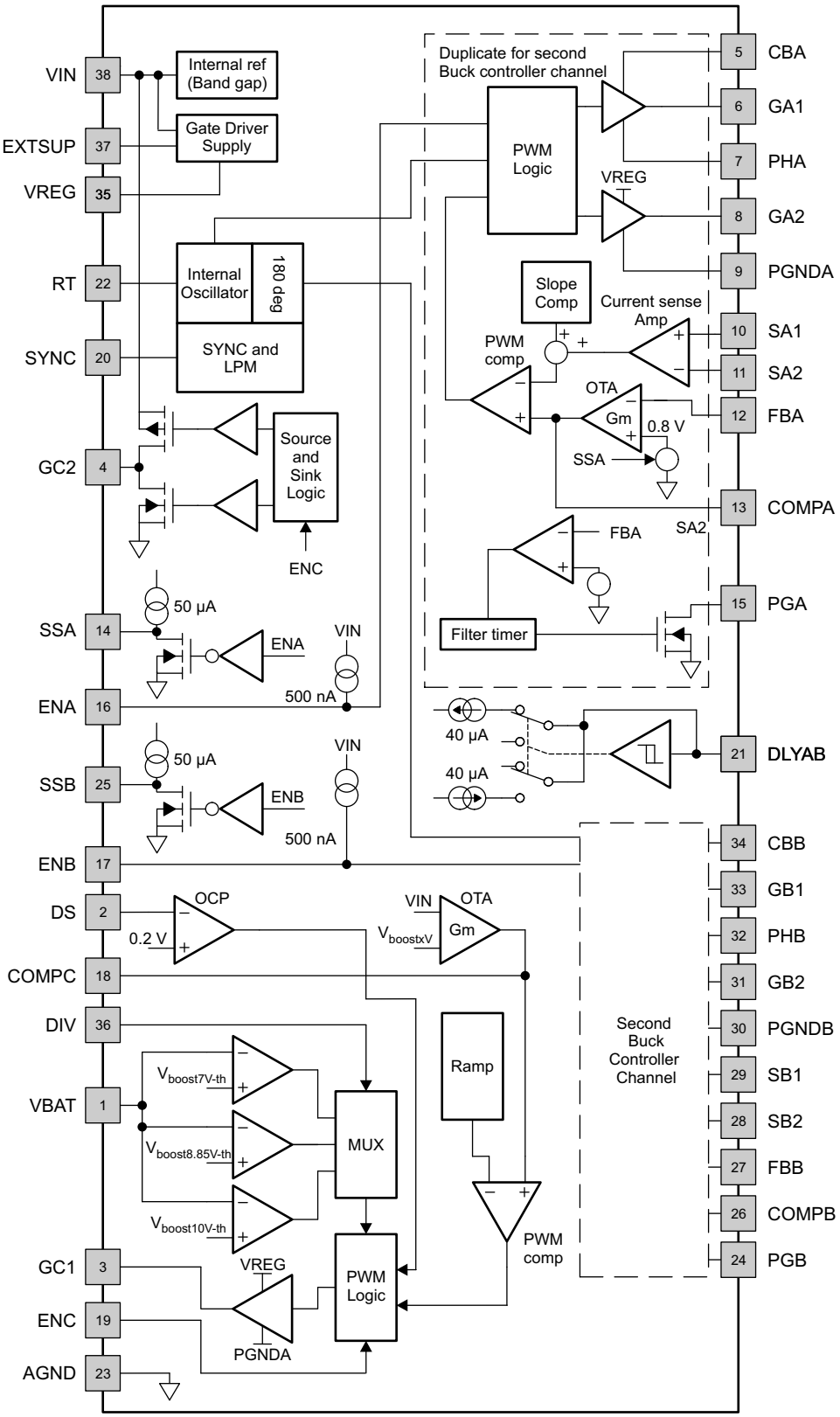


Figure 5. TPS43330A-Q1 Block Diagram

- AEC-Q100 qualified
- Two synchronous buck controller units
- One pre-boost controller
- Input range up to 40 V, down to 2 V
- Low-power-mode IQ: 30 µA (one buck on), 35 µA (two bucks on)
- Programmable frequency and external synchronization range 150 to 600 kHz
- Out-of-phase switching between buck channels

3.1.2 TPS659039-Q1 Features

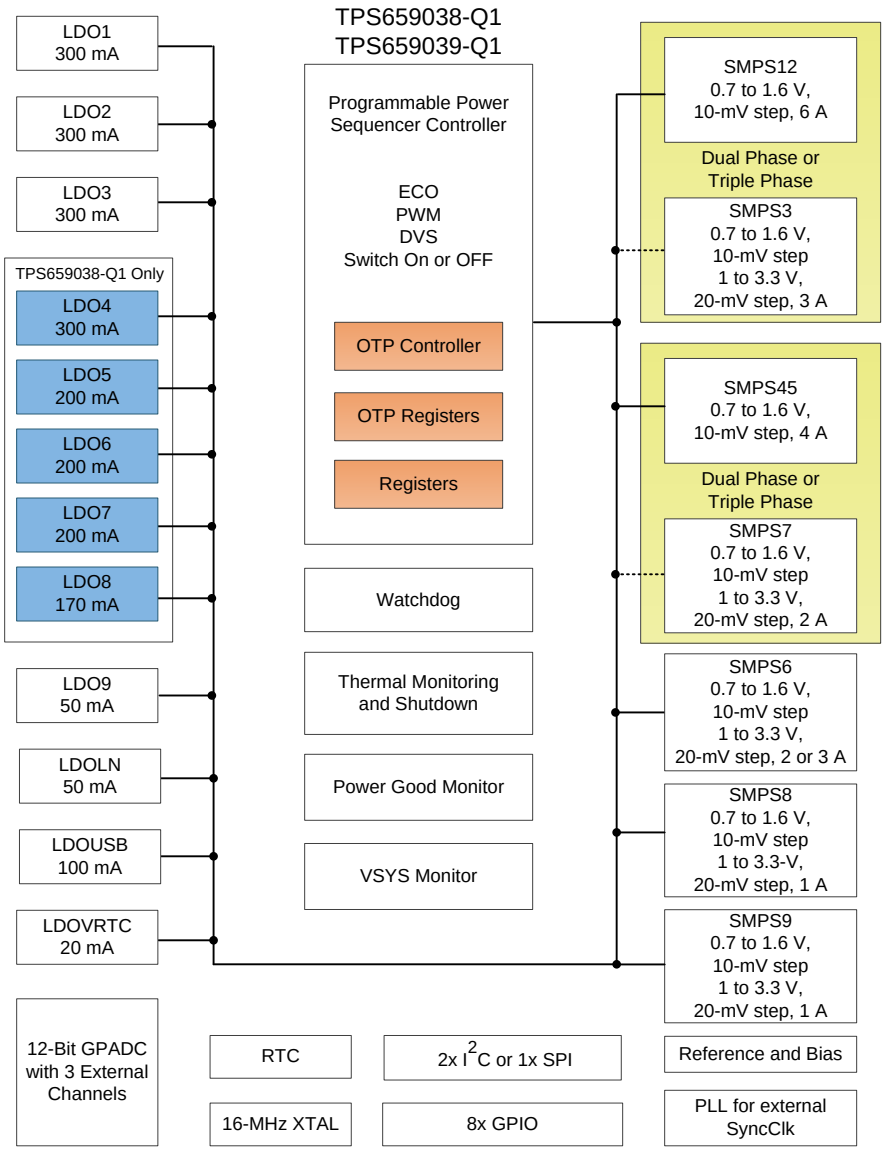


Figure 6. TPS659039-Q1 Block Diagram

- Qualified for automotive
- System voltage range from 3.135 V to 5.25 V
- Seven step-down SMPS regulators:
  - One 0.7 V to 1.65 V at 6 A (10-mV steps)
  - One 0.7 V to 1.65 V at 4 A (10-mV steps)
  - One 0.7 V to 3.3 V at 3 A (10-mV or 20-mV steps)
  - Two 0.7 V to 3.3 V at 2 A (10-mV or 20-mV steps)
  - Two 0.7 V to 3.3 V at 1 A (10-mV or 20-mV steps)
  - Ability to synchronize SMPS to external or internal fallback clock with phase synchronization
  - Short-circuit protection
- Eleven general-purpose LDOs, adjustable in 50-mV steps:
  - Two 0.9 V to 3.3 V at 300 mA with pre-regulated supply
  - Six 0.9 V to 3.3 V at 200 mA with pre-regulated supply
  - One 0.9 V to 3.3 V at 50 mA with pre-regulated supply
  - One 100-mA USB LDO
  - One low-noise LDO 0.9 V to 3.3 V up to 100 mA (low-noise performance up to 50 mA)
  - Short-circuit protection
- Clock management 16-MHz crystal oscillator and 32-kHz RC oscillator
- Real-time clock (RTC) with alarm wake-up mechanism
- Control
  - Configurable power-up and power-down sequences (OTP)
  - Configurable sequences between the SLEEP and ACTIVE states (OTP)
  - One dedicated digital-output signal (REGEN) that can be Included in the start-up sequence
  - Three digital-output signals multiplexed with GPIO that can be Included in the start-up sequence
  - Selectable control interface
    - One SPI for resource configurations and DVS control
    - Two I^2C interfaces, one dedicated for DVS control, and a general-purpose I^2C interface for resource configuration and DVS control

3.1.3 TPS22965-Q1 Features

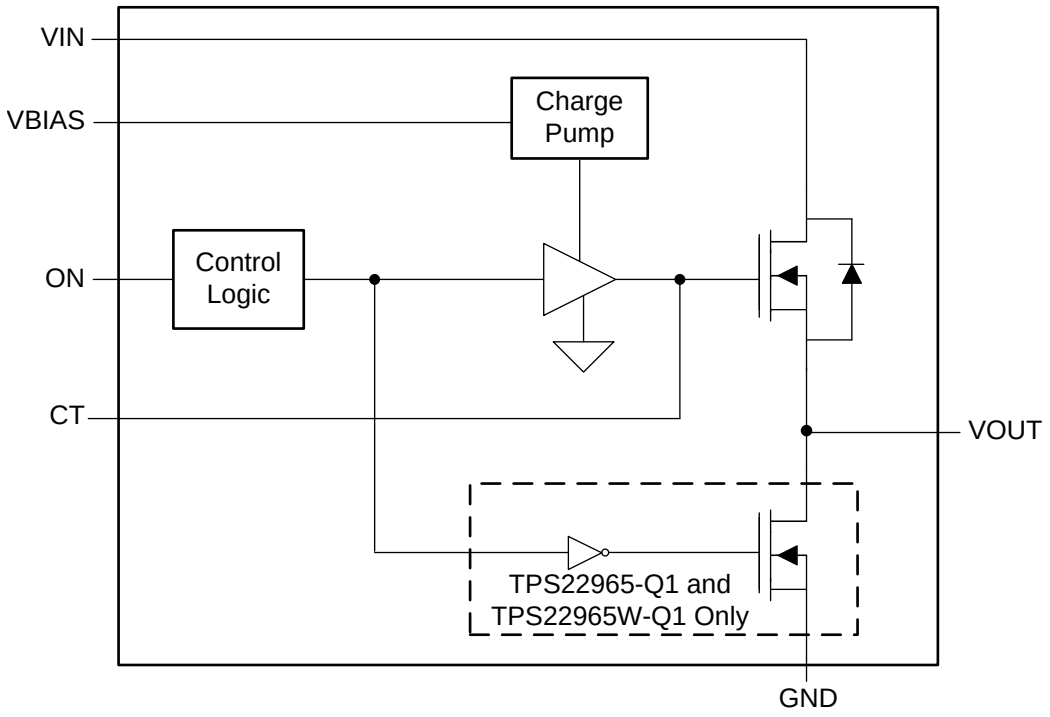


Figure 7. TPS22965-Q1 Block Diagram

- AEC-Q100 qualified
- Integrated single-channel load switch
- Input voltage range: 0.8 V to 5.5 V
- Ultra-low on resistance (R_{ON} = 16 mΩ)
- Maximum continuous switch current
- Low quiescent current (50 µA)
- Configurable rise time
- Quick output discharge (QOD)

3.1.4 TPS51200-Q1 Features

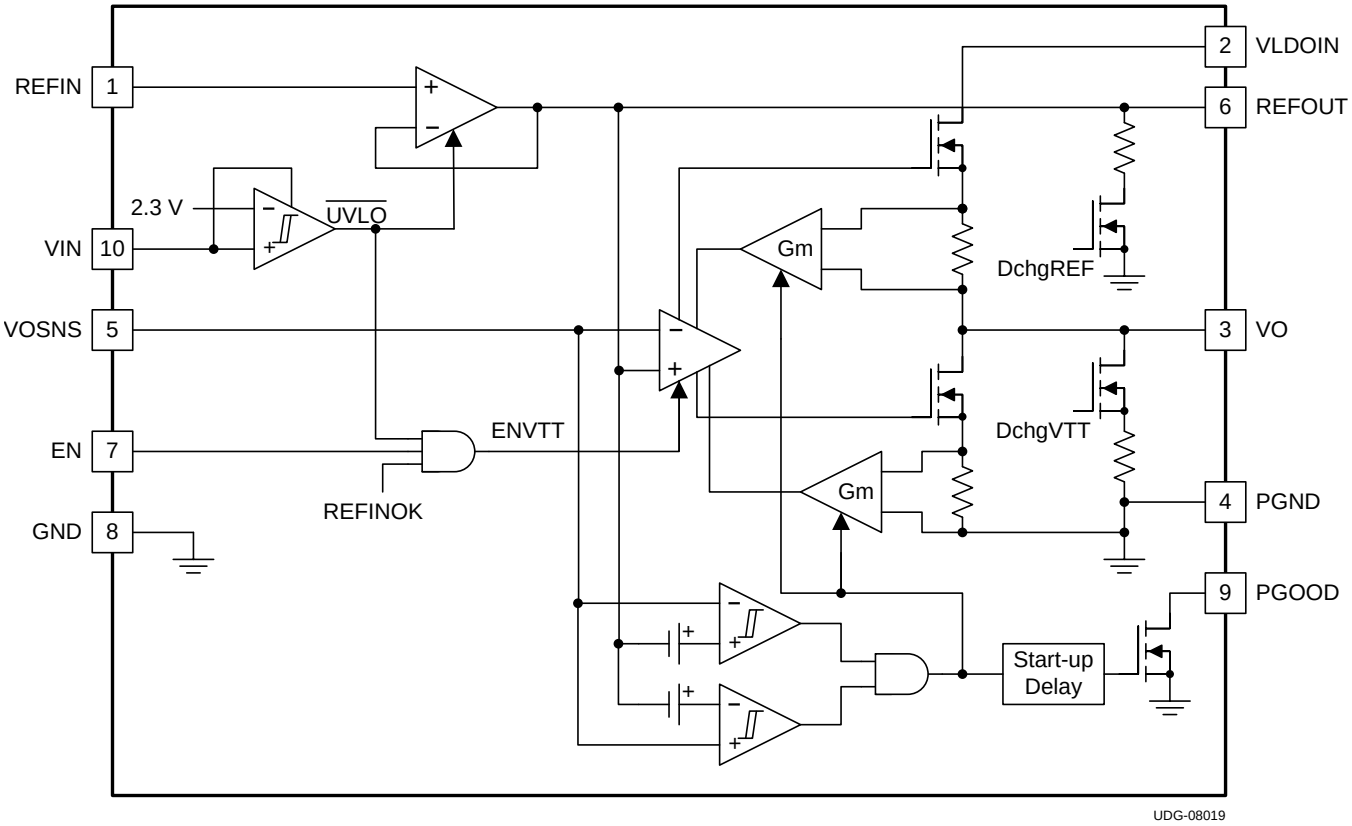


Figure 8. TPS51200-Q1 Block Diagram

- AEC-Q100 qualified
- Input voltage: supports 2.5-V rail and 3.3-V rail
- VLDOIN voltage range: 1.1 V to 3.5 V
- Sink/source termination-regulator droop compensation
- Requires minimum output capacitance of 20-µF (typically 3 × 10-µF MLCCs) for memory termination applications (DDR)

4 System Design Theory

4.1 Pre-Regulation (Battery to 5 V and 3.3 V, Including Cranking Support) With TPS43330A-Q1

Because an infotainment system should not require a reboot after cranking (like during start-stop), the TPS43330A-Q1, which comes with a preboost-controller, will auto-activate in case of a drop in supply-voltage. In the current design, the TPS43330A-Q1 device maintains an output voltage of 7 V, even if the supply drops to as low as 3.2 V.

NOTE: The TPS43330A-Q1 requires to have been supplied a minimum of 8.5 V before activation of the boost.

The device further includes two synchronous buck-controllers, configured for 5 V (2 A) and 3.3 V (4 A), which can deliver all down-stream-supplies. The switching frequency is set to 400 kHz (200 kHz for the boost), which limits the switching losses and keeps the third harmonic below the AM-band.

4.2 Processor-Supply With TPS659039-Q1

The TPS659039-Q1 PMIC has been developed to drive the specific requirements of modern processors with multiple rails, sequencing, and adaptive voltage scaling (AVS). In various applications, the TPS659039-Q1 device powers the TDA3x family of processors from Texas Instruments (TI), but is configurable as suitable to be adopted by a wide range of other processors. The pre-programmed version in this design, O9039A360IZWSRQ1, targets processors of the DRA74x, DRA75x, TDA2x, and AM572x families.

4.3 Switched 3.3-V Rail With TPS22965-Q1

In many designs, a relatively power-hungry 3.3-V rail requires sequencing, while the PMIC requires supplying 3.3 V early. Instead of using another DC-DC-converter to step-down from the 5-V rail, a TPS22965-Q1 Load-switch is being used, which a digital control pin (REGEN1) of the PMIC controls. The TPS22965-Q1 device layout supports 2.5 A output in this design.

4.4 DDR-Termination With TPS51200-Q1

To terminate the DDR-memory, a termination voltage of half the DDR-supply-voltage is required. The current system is configured for LV-DDR3, hence a 1.35-V DDR-supply. The DDR-termination device, TPS51200-Q1, generates a 0.675 reference voltage with up to 1 A on this design. The part itself can source and sink currents in excess of 3 A.

5 Getting Started

5.1 Hardware

See Figure 9 for the respective connections. Additional test points are labeled on the board.

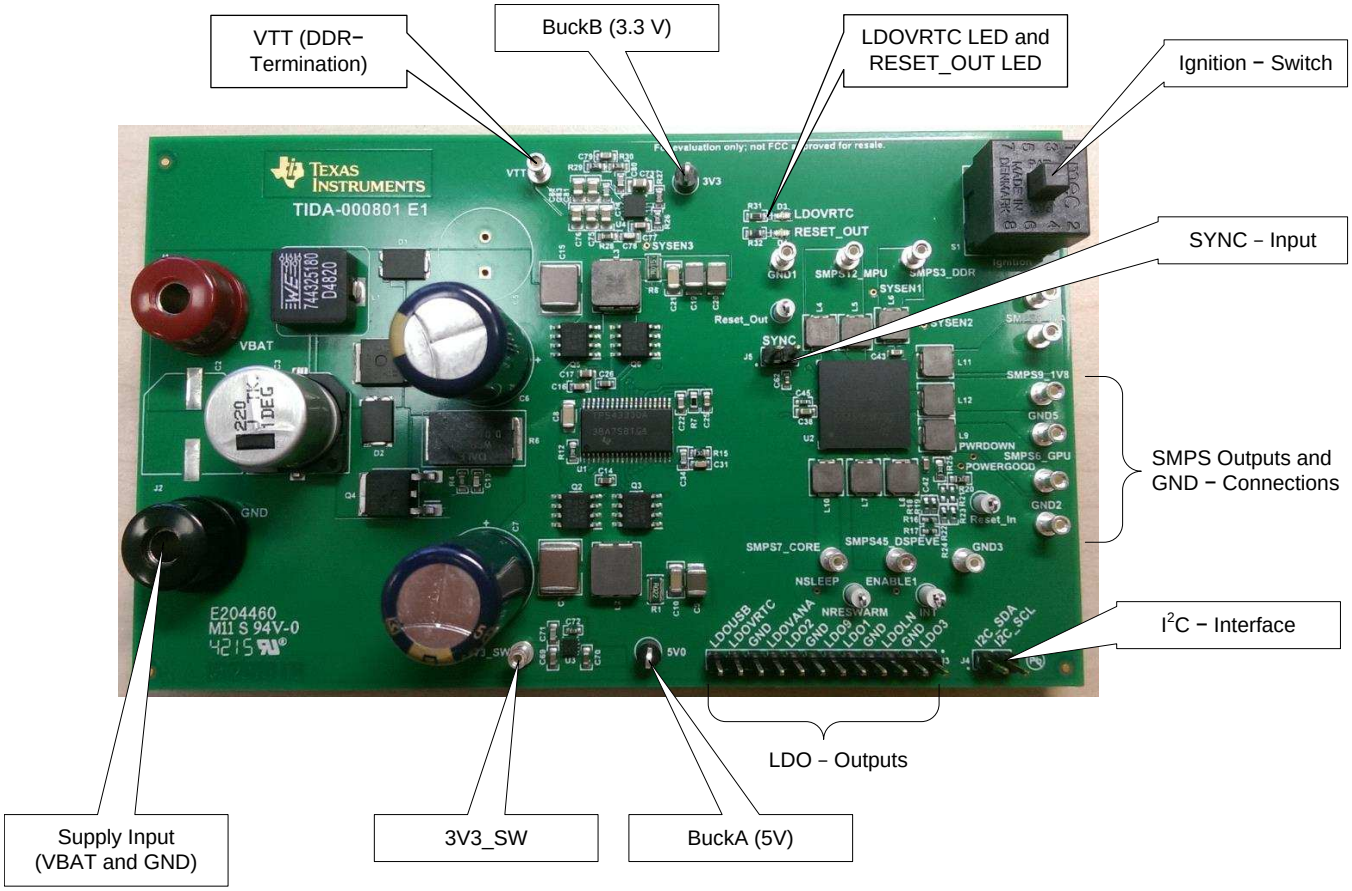


Figure 9. Hardware Connectors and Test Points

5.1.1 Hardware Setup

Before starting, connect a power-supply with sufficient output power (dependant upon intended testing) through banana-jack-cables to J1 (VBAT) and J2 (GND). If desired, apply loads to the outputs. Because some rails are daisy-chained, consider the total current available from the pre-regulator. For example: the load-switch and the PMIC are driven from the BuckB 3.3-V rail, rated for 4 A. If this rail is being loaded already (directly or on the PMIC outputs), the design may not be able to draw the full current. To set up the reference-design hardware, follow the steps listed in this section.

- BuckA is configured for 5-V output and 2 A maximum. Use the 5V0 test-point to apply a load.
- BuckB is configured for 3.3-V output and 4 A maximum. Use the 3V3 test-point to apply a load.

NOTE: Do not use 3V3_SW turret.

- To apply a load to the load-switch, use the 3V3_SW turret, 2.5 A.
- To apply a load to VTT, use the VTT turret, 1 A maximum.
- To apply loads to the SMPSs of the PMICs , use the respective turrets.
- To apply loads to the LDOs, use the header J3.

5.1.1.1 Power-Up

The design configuration powers up the pre-regulator, which supplies the PMIC as soon as the user applies power to the board.

NOTE: Although the pre-regulator contains a boost, there is an unlock threshold, which means that the supply voltage must have once passed above 8.5 V before activating the boost.

For boost operation, apply greater than 8.5 V before reducing the voltage. If the pre-regulator is active, the red LED, D3, LDOVRTC with light. At this point, all PMIC outputs (except LDOVRTC) are off and so are 3V3_SW and VTT.

To start the boot sequence of the PMIC, press the Ignition switch.

NOTE: If RESET_OUT-LED is illuminated, the Ignition switch was pressed already and the PMIC is powered-up. Pressing the switch again will power it down.

All pre-configured rails come up in the correct order and 3V3_SW and VTT are sequenced. At the end of the sequence, which takes about 10 ms, the green LED (D4 or RESET_OUT) illuminates. RESET_OUT is normally the signal that releases the processor.

5.1.1.2 PMIC Switching

The PMIC switches its SMPSs at a default frequency of 2.2 MHz; however, an external clock in the range of 1.7 MHz to 2.7 MHz may be applied. Use the SYNC-jumper for this, where the clock signal with a high-level of 1.8 V is applied to the pin closer to the PMIC-IC and the second pin may be used for GND. If an adequate clock is supplied, the switching frequency will synchronize to the clock signal. If an external clock is not present, the switching frequency defaults back to 2.2 MHz.

J4 provides an interface to the I2C1-interface of the PMIC. Using either a proprietary solution or the USB2ANY-adapter (HPA665-001) and a graphical user interface (GUI), one can read the register of the PMIC and write to the read-write registers. For example, the designer can turn on or off resources, adjust voltages, and so forth. For the default operation and start-up, no interfacing is required.

5.1.1.3 Power Down

An application processor is normally required for a shut-down sequence. This is pre-programmed into the TPS659039-Q1, but can only be executed if input-power is available. Therefore, first turn Ignition switch to off (RESET_OUT-LED should be off) and then turn off the power-supply to the board.

5.1.1.4 Modifying Components

The following unassembled components allow for modifications to the board:

- Increase input capacitance to the boost by adding C2.
- Increase boost output and buck-input capacitance by adding C5.
- Enhance EMI-performance by adding a snubber to the BuckA and/or BuckB outputs by assembling R2 and C11 for BuckA and R9 and C23 for BuckB.
- Change the DDR-Voltage from 1.35 V (for DDR3LV) to 1.5 V for DDR3 by removing R24 and installing R22.
- Some older processor-variants require a double-reset-pulse at boot, configure this by removing R23 and installing R21. RESET_OUT goes high for 2 ms, goes low for 2 ms, and returns to high.

5.2 Firmware

The OTP Memory programs the PMIC, pre-defines all voltages and the sequence.

Refer to the *TPS659039-Q1 EVM User's Guide* (SWCU174) for a detailed description of the GUI for PMIC-control.

NOTE: The TPS659039EVM and corresponding documentation are under NDA-restrictions.

5.2.1 Installing the Firmware

Refer to the *TPS659039-Q1 EVM User's Guide* (SWCU174) for a detailed description of the GUI for PMIC-control.

5.2.2 Running the Firmware

Refer to the *TPS659039-Q1 EVM User's Guide* (SWCU174) for a detailed description of the GUI for PMIC-control.

6 Test Data

During debugging of the design, the following tests were performed:

- Functional test: All rails power up in the correct sequence and to the correct voltages
- Stability tests: All rails have been tested individually to their maximum rated load (static) and with load-steps. For the latter, a FET has been used in order to achieve very fast slew rates. The load-steps were performed in amplitudes that resemble the expected worst-case steps in a real application.
- For the boost, the Cranking Simulator (*Cranking Simulator Reference Design for Automotive Applications*, TIDU143) was used to test the EVM for its response to actual cranking pulses as performed by customers. The Volkswagen Cold-Start Test Pulse, VW80000, was applied.
- Further testing included load-steps on BuckA and BuckB with VBAT low (and boost is active)
- Peripheral testing: Applying an external clock to the SYNC-pin of TPS659039-Q1 and accessing its registers through I^2C.

See the test results in the following sections.

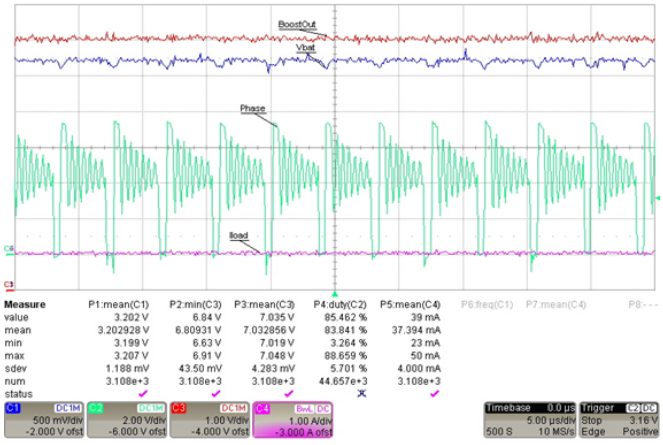
6.1 TPS43330_Boost Test Data

The following plots are the test results for the TPS43330_Boost.

6.1.1 Boost Steady State

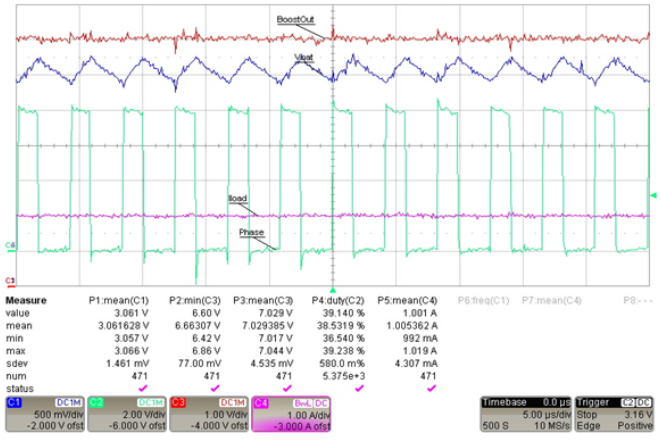
The following plots are the test results in the Boost Steady State using the following parameters.

- Voltage for VBAT = 3.2 V
- Current for Iload is specified for the corresponding figures at 0 A (Figure 10), 1 A (Figure 11), and 2.5 A (Figure 12).



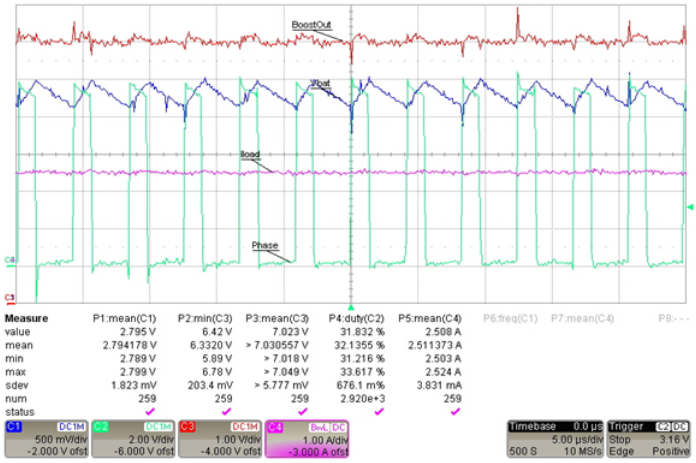
Iload = 0 A VBAT = 3.2 V

Figure 10. Boost Steady State (Iload = 0 A)



Iload = 1 A VBAT = 3.2 V

Figure 11. Boost Steady State (Iload = 1 A)



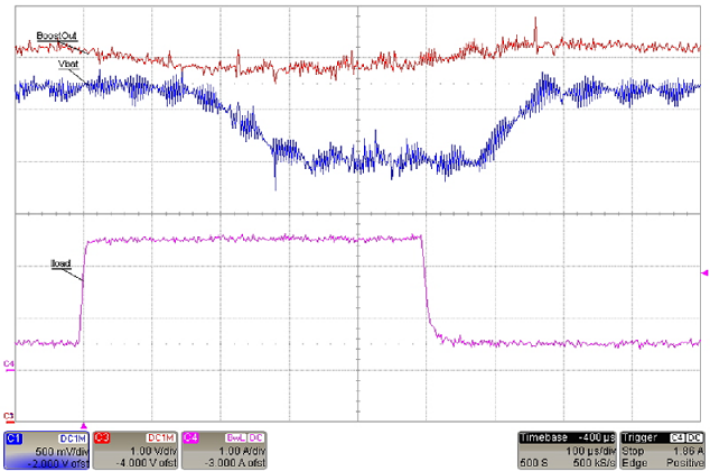
Iload = 2.5 A VBAT = 3.2 V

Figure 12. TPS43330 Boost Steady State (Iload = 2.5 A)

6.1.2 Boost Dynamic

The following plot shows the test results for the Boost Dynamic state using the following parameters.

- Voltage for VBAT = 3.2 V
- Current for Iload starts at 500 mA, goes to 2.5 A, then returns to 500 mA (Figure 13)



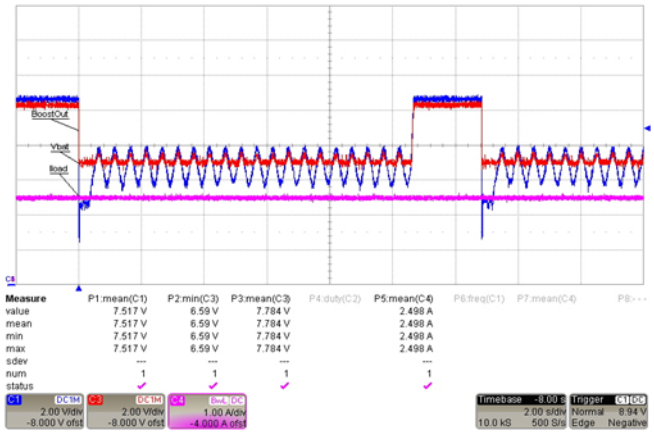
Iload = 500 mA, then goes to 2.5 A, then returns to 500 mA VBAT = 3.2 V

Figure 13. TPS43330 Boost Dynamic

6.1.3 Boost Cranking

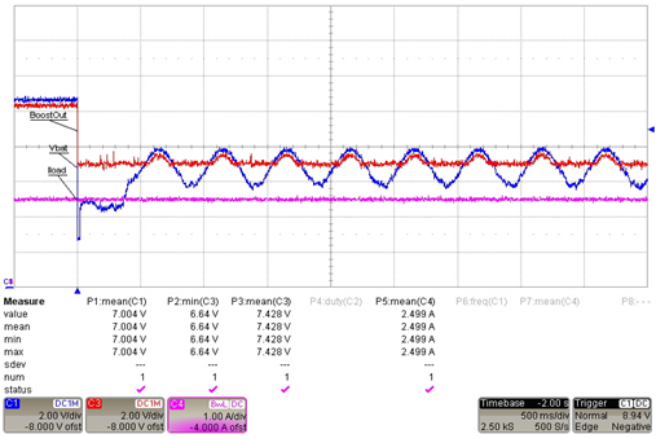
The following plots are the test results for the Boost Cranking state using the following parameters.

- Voltage for VBAT = 3.2 V
- Current for Iload is specified for the corresponding figures at 2.5 A
- BoostOut is measured over cranking time and the following plots correspond to these settings:
  - Timebase 8 s, 2 s/div, 100 kS 200 S/s (Figure 14)
  - Timebase 2 s, 500 ms/div, 2.5 kS 500 S/s (Figure 15)
  - Timebase 400 ms, 100 ms/div, 500 S 500 S/s (Figure 16)
  - Timebase 40 ms, 10 ms/div, 500 S 5 k S/s (Figure 17)



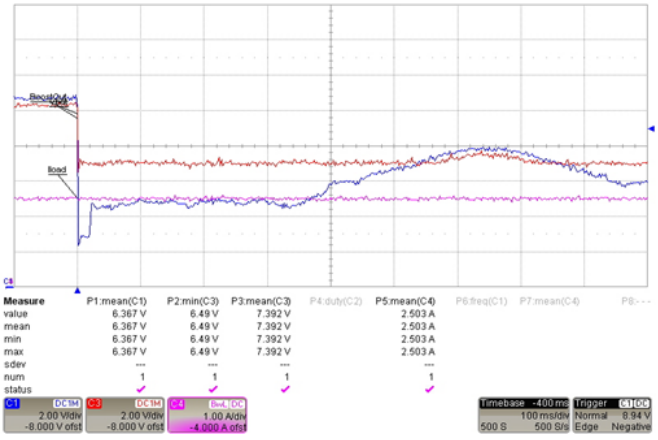
Timebase –8 s, 2 s/div, 100 kS 200 S/s

Figure 14. TPS43330 Boost Cranking (Zoom: 2 s/div)



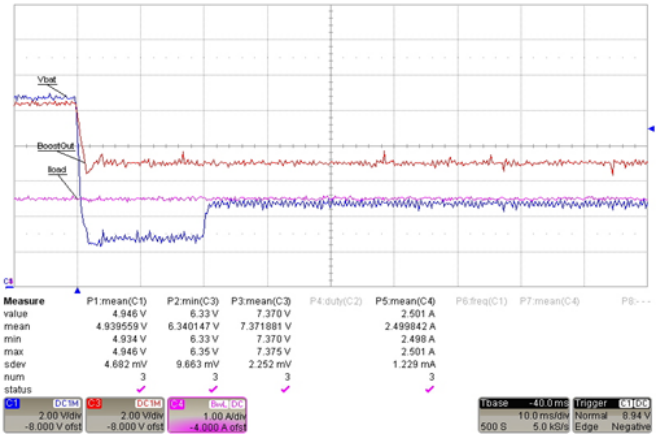
Timebase –2 s, 500 ms/div, 2.5 kS 500 S/s

Figure 15. TPS43330 Boost Cranking (Zoom: 500 ms/div)



Timebase –400 ms, 100 ms/div, 500 S 500 S/s

Figure 16. TPS43330 Boost Cranking (Zoom: 100 ms/div)



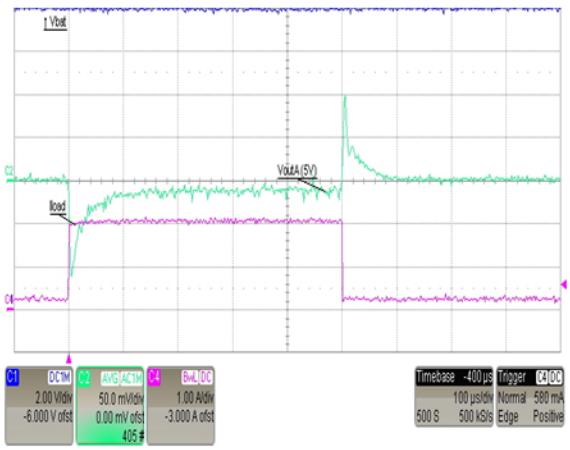
Timebase –40 ms, 10 ms/div, 500 S 5 k S/s

Figure 17. TPS43330 Boost Cranking (Zoom: 10 ms/div)

6.2 TPS43330_BuckA and BuckB Test Data

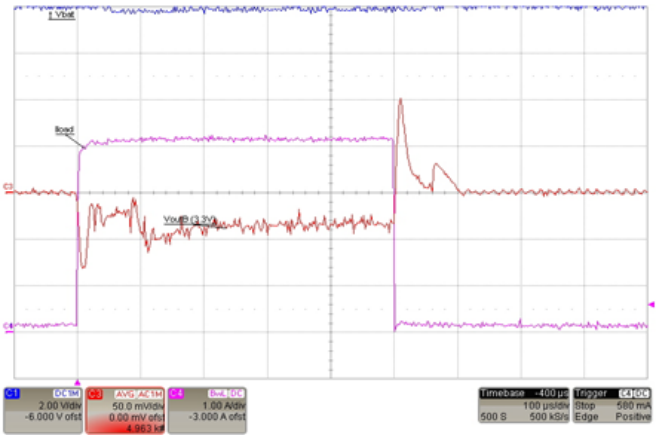
The following are the test plots for the TPS43330 Buck A and Buck B using the following parameters.

- Voltage for VBAT = 14 V
- Voltage for VOUT = 5 V
- BuckA (5 V): Iload goes from 200 mA to 2 A and back to 200 mA (Figure 18)
- BuckB (3.3 V): Iload goes from 200 mA to 4 A and back to 200 mA (Figure 19)



Iload = 200 mA, then goes to 2 A, then returns to 200 mA

Figure 18. TPS43330_BuckA (Iload = 200 mA, Goes to 2 A, Returns to 200 mA)

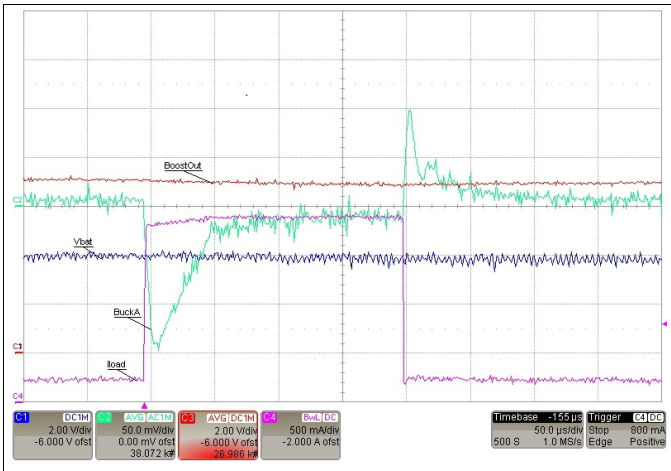


Iload = 200 mA, then goes to 4 A, then returns to 200 mA

Figure 19. TPS43330_BuckB (Iload = 200 mA, Goes to 4 A, Returns to 200 mA)

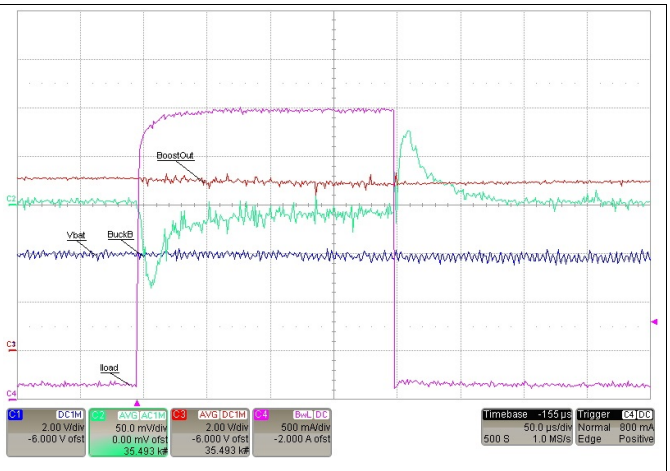
The following are the test plots with load steps applied to BuckA and BuckB with Boost active and VBAT = 4 V.

- Boost active and VBAT = 4 V
- Iload goes from 200 mA to 1.8 A and then returns to 200 mA (Figure 20)
- Iload goes from 200 mA to 3 A and then returns to 200 mA (Figure 21)



Iload = 200 mA, then goes to 1.8 A, then returns to 200 mA

Figure 20. Loadstep VoutA (Iload = 200 mA, Goes to 1.8 A, Returns to 200 mA)



Iload = 200 mA, then goes to 3 A, then returns to 200 mA

Figure 21. Loadstep VoutB (Iload = 200 mA, Goes to 3 A, Returns to 200 mA)

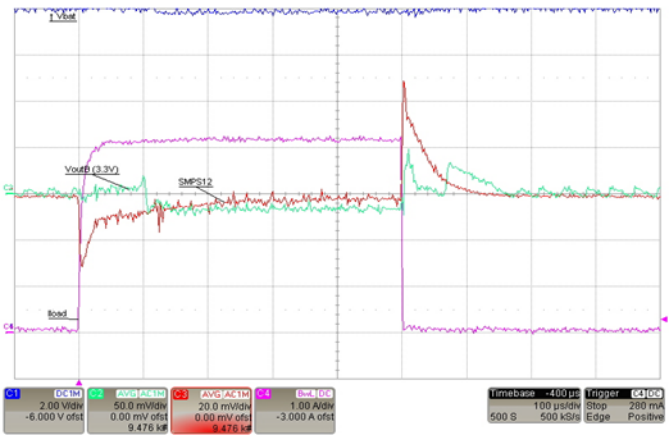
6.3 TPS659039-Q1 Test Data

The following are the test plots for the TPS659039-Q1 using the following parameter.

- Voltage for VSYS = 3.3 V

6.3.1 SMPS12

- Voltage for VOUT = 1.1 V
- Iload goes from 100 mA to 4.2 A and then returns to 100 mA (Figure 22)

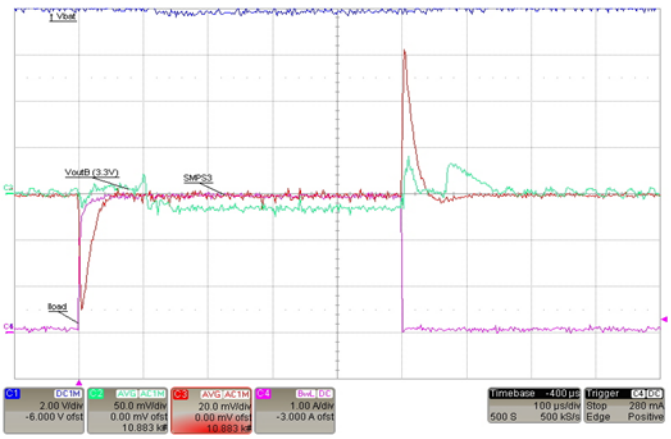


Iload = 100 mA, then goes to 4.2 A, then returns to 100 mA VOUT = 1.1 V

Figure 22. TPS659039-Q1 for SMPS12 (Iload = 100 mA, Goes to 4.2 A, Returns to 100 mA)

6.3.2 SMPS3

- Voltage for VOUT = 1.35 V
- Iload goes from 100 mA to 3 A and the returns to 100 mA (Figure 23)

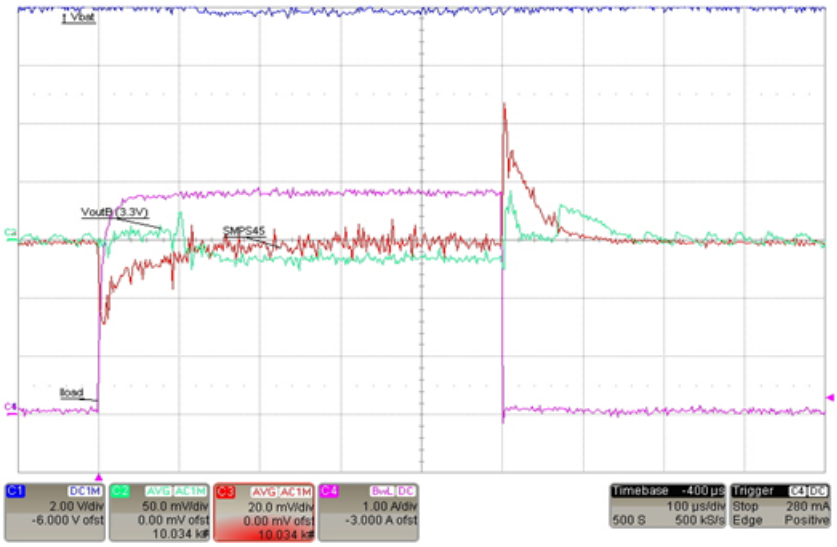


Iload = 100 mA, then goes to 3 A, then returns to 100 mA VOUT = 1.35 V

Figure 23. TPS659039-Q1 for SMPS3 (Iload = 100 mA, Goes to 3 A, Returns to 100 mA)

6.3.3 SMPS45

- Voltage for VOUT = 1.06 V
- Iload goes from 100 mA to 3.8 A and then returns to 100 mA (Figure 24)

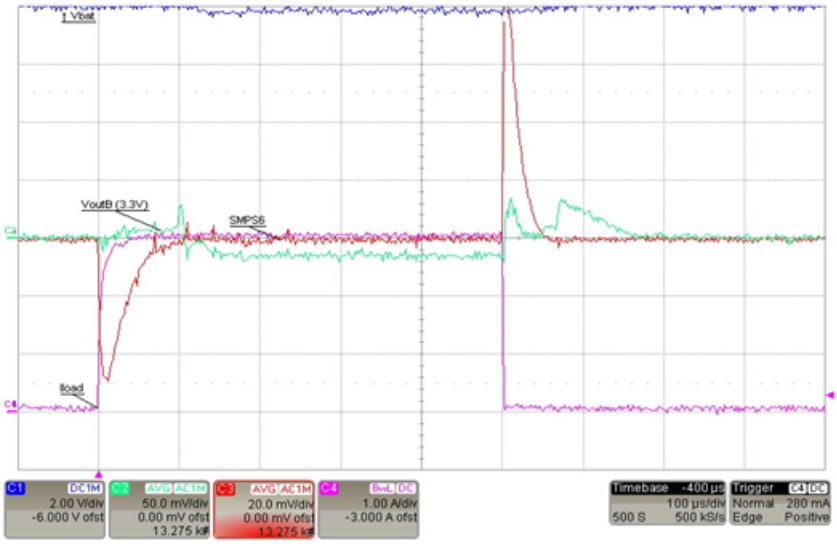


Iload = 100 mA, then goes to 3.8 A, then returns to 100 mA VOUT = 1.06 V

Figure 24. TPS659039-Q1 for SMPS45 (Iload = 100 mA, Goes to 3.8 A, Returns to 100 mA)

6.3.4 SMPS6

- Voltage for VOUT = 1.06 V
- Iload goes from 100 mA to 3 A and then returns to 100 mA (Figure 25)

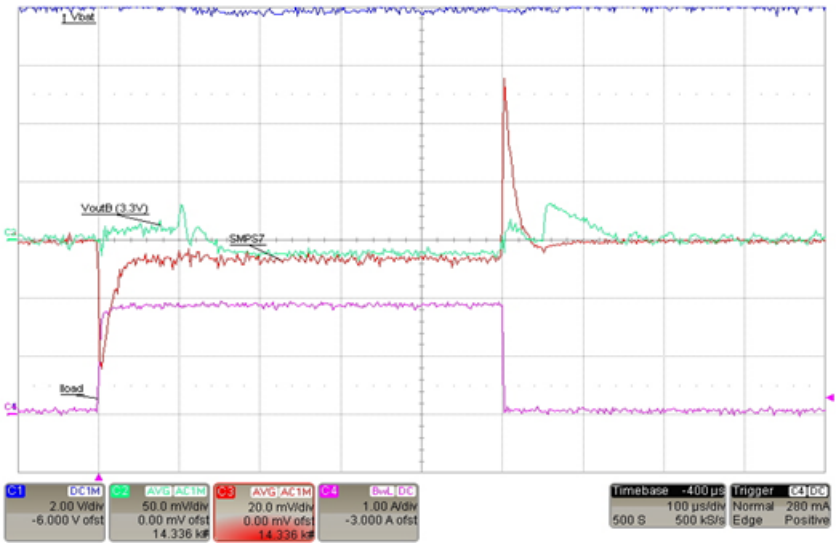


Iload = 100 mA, then goes to 3 A, then returns to 100 mA VOUT = 1.06 V

Figure 25. TPS659039-Q1 for SMPS6 (Iload = 100 mA, Goes to 3 A, Returns to 100 mA)

6.3.5 SMPS7

- Voltage for VOUT = 1.06 V
- Iload goes from 100 mA to 1.9 A and then returns to 100 mA (Figure 26)

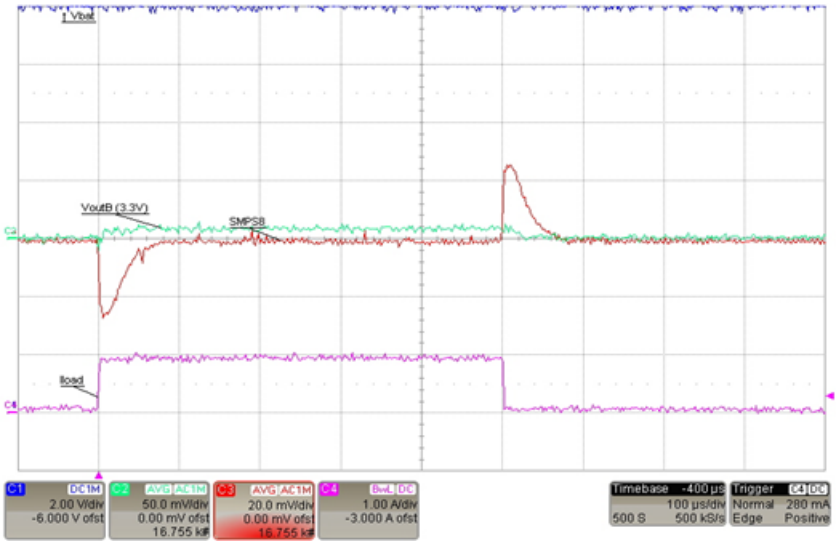


Iload = 100 mA, then goes to 1.9 A, then returns to 100 mA VOUT = 1.06 V

Figure 26. TPS659039-Q1 SMPS7 (Iload = 100 mA, Goes to 1.9 A, Returns to 100 mA)

6.3.6 SMPS8

- Voltage for VOUT = 1.06 V
- Iload goes from 100 mA to 1 A and then returns to 100 mA (Figure 27)

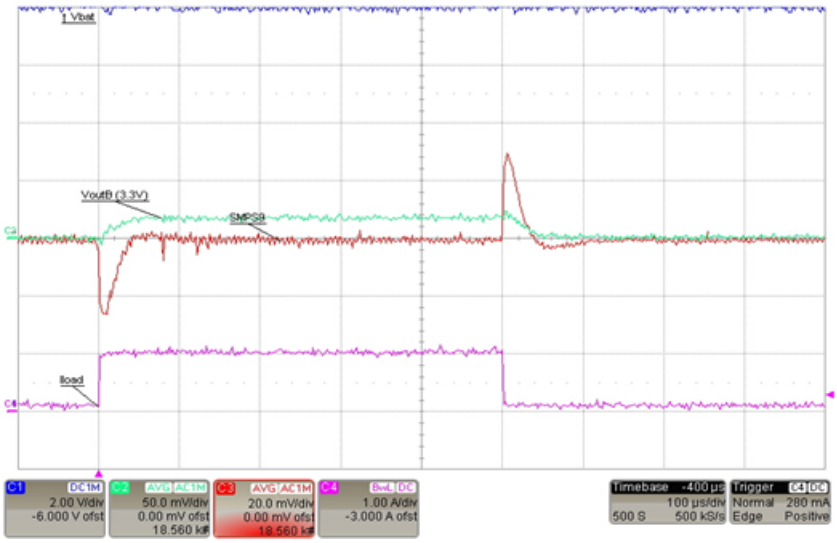


Iload = 100 mA, then goes to 1 A, then returns to 100 mA VOUT = 1.06 V

Figure 27. TPS659039-Q1 SMPS8 (Iload = 100 mA, Goes to 1 A, Returns to 100 mA)

6.3.7 SMPS9

- Voltage for VOUT = 1.8 V
- Iload goes from 100 mA to 1 A and then returns to 100 mA (Figure 28)



Iload = 100 mA, then goes to 1 A, then returns to 100 mA VOUT = 1.8 V

Figure 28. TPS659039-Q1 SMPS9 (Iload = 100 mA, Goes to 1 A, Returns to 100 mA)

6.3.8 Sequencing

Figure 29 plots the test data for the sequencing.

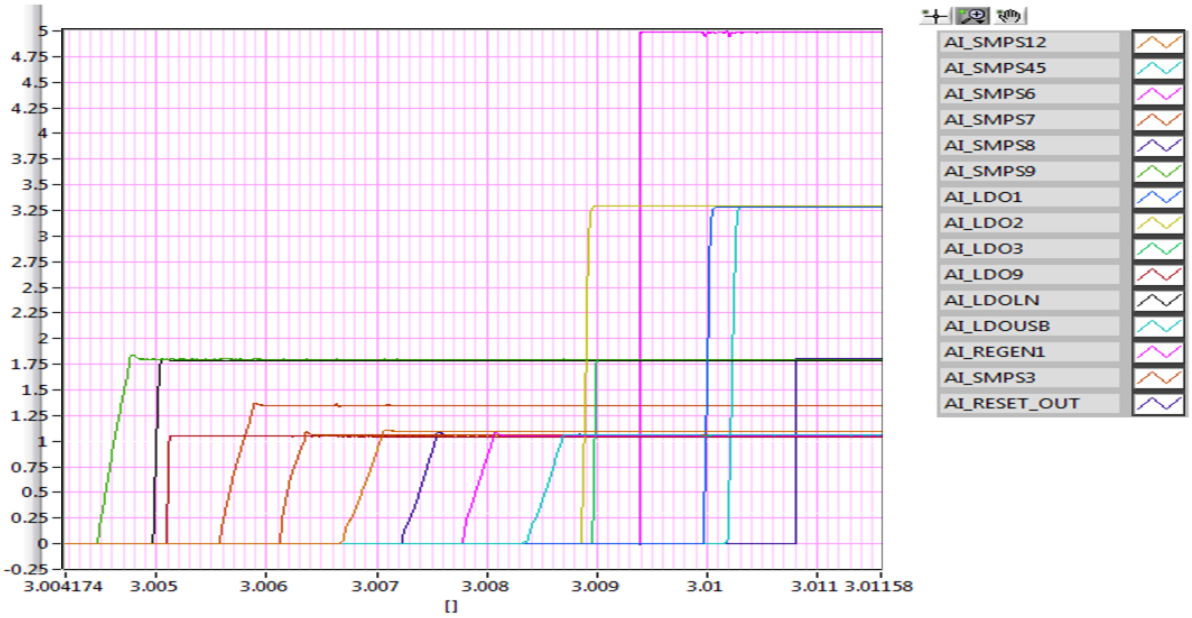
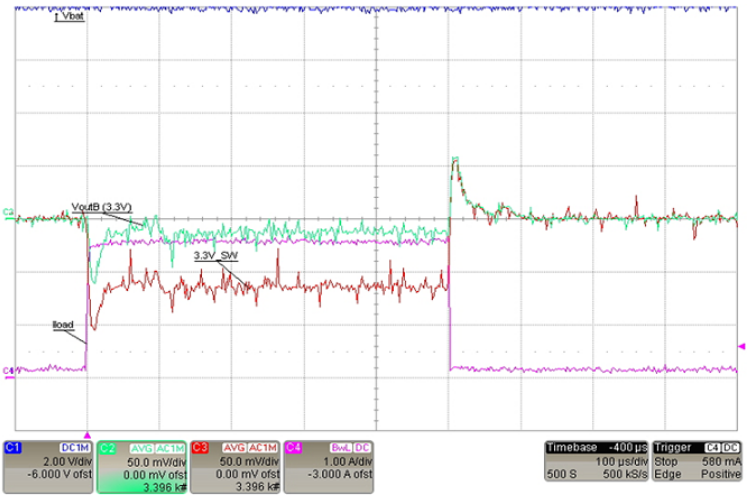


Figure 29. TPS659039-Q1 Sequences 1 Through 5

6.4 TPS22965-Q1 Test Data

The following plot shows the test results for the TPS22965-Q1 device using the following parameters.

- Voltage for VSYS = 3.3 V
- Iload goes from 200 mA to 2.5 A and then returns to 200 mA (Figure 30)



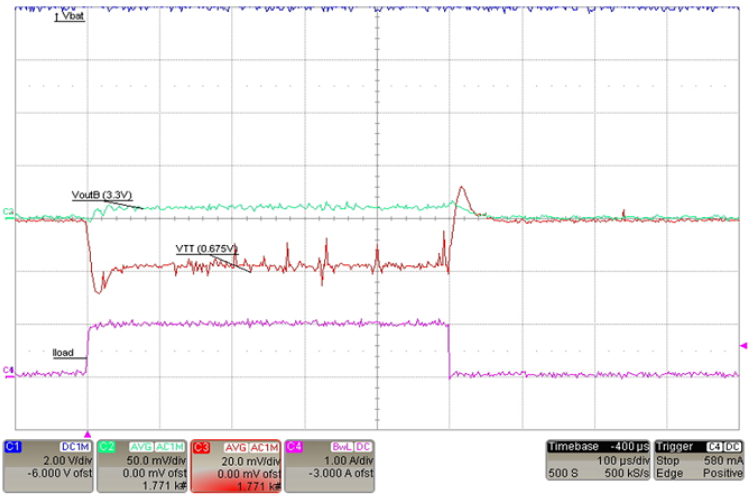
Iload = 200 mA, then goes to 2.5 A, then returns to 200 mA

Figure 30. TPS22965-Q1 Test Plot (Iload = 200 mA, Goes to 2.5 A, Returns to 200 mA)

6.5 TPS51200-Q1 Test Data

The following plot shows the test results for the TPS51200-Q1 device using the following parameters.

- Voltage for VSYS = 3.3 V
- Voltage for VREF = 1.35 V
- Voltage for VOUT = 0.675 V
- Iload goes from 100 mA to 1 A and then returns to 100 mA (Figure 31)



Iload = 200 mA, then goes to 2.5 A, then returns to 200 mA

Figure 31. TPS51200-Q1 Test Plot (Iload = 100 mA, Goes to 1 A, Returns to 100 mA)

7 Design Files

7.1 Schematics

To download the schematics for each board, see the design files at http://www.ti.com/tool/TIDA-00801. The following schematics are available:

1. TPS43330A-Q1 Schematic
2. TPS22965-Q1 Schematic
3. TPS659039-Q1 Schematic
4. TPS51200-Q1 Schematic

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00801.

7.3 Layer Plots

To download the layer plots, see the design files at TIDA-00801.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00801.

7.5 Layout Guidelines

7.5.1 TPS43330-Q1 Layout Guidelines

Use the following guidelines for the design considerations of the grounding and PCB circuit layout.

7.5.1.1 Boost Converter

1. The path formed from the input capacitor to the inductor and BOT_SW3 with the low-side current-sense resistor should have short leads and PC trace lengths. The same applies for the trace from the inductor to Schottky diode D1 to the C_{OUT1} capacitor. Connect the negative terminal of the input capacitor and the negative terminal of the sense resistor together with short trace lengths.
2. The overcurrent-sensing shunt resistor may require noise filtering, and the filter capacitor should be close to the IC pin.

7.5.1.2 Buck Converter

1. Connect the drain of TOP_SW1 and TOP_SW2 together with the positive terminal of input capacitor C_{OUT1}. The trace length between these terminals should be short.
2. Connect a local decoupling capacitor between the drain of TOP_SWx and the source of BOT_SWx.
3. The Kelvin-current sensing for the shunt resistor should have traces with minimum spacing, routed in parallel with each other. Place any filtering capacitors for noise near the IC pins.
4. The resistor divider for sensing the output voltage connects between the positive terminal of its respective output capacitor and C_{OUTA} or C_{OUTB} and the IC signal ground. Do not locate these components and their traces near any switching nodes or high-current traces.

7.5.1.3 Other Considerations

1. Short PGNDx and AGND to the thermal pad. Use a star ground configuration if connecting to a non-ground plane system. Use tie-ins for the EXTSUP capacitor, compensation-network ground, and voltage-sense feedback ground networks to this star ground.
2. Connect a compensation network between the compensation pins and IC signal ground. Connect the oscillator resistor (frequency setting) between the RT pin and IC signal ground. Do not locate these sensitive circuits near the dv/dt nodes; these include the gate-drive outputs, phase pins, and boost circuits (bootstrap).
3. Reduce the surface area of the high-current-carrying loops to a minimum by ensuring optimal component placement. Locate the bypass capacitors as close as possible to their respective power and ground pins.

7.5.2 TPS43330-Q1 Layout Example

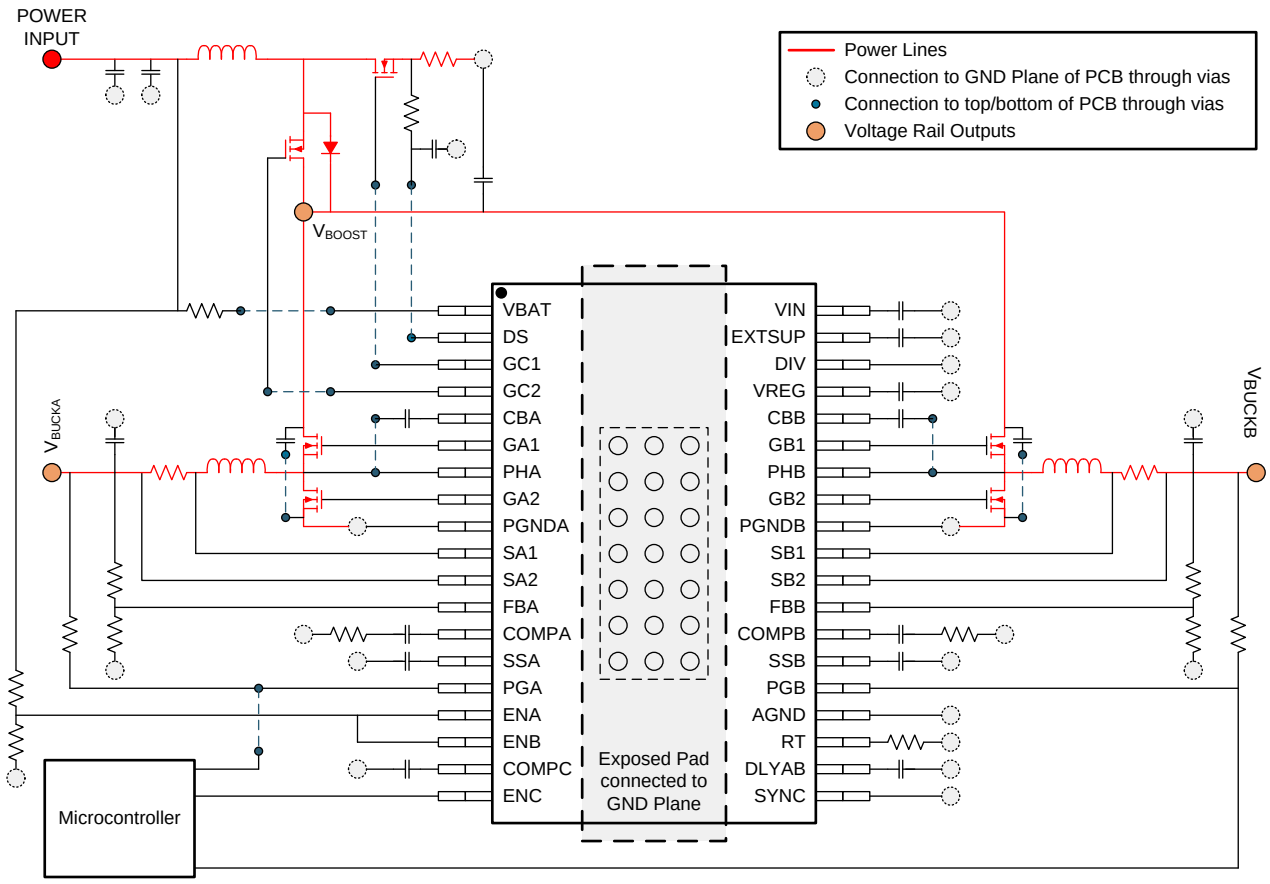


Figure 32. TPS4333x-Q1 Layout Example

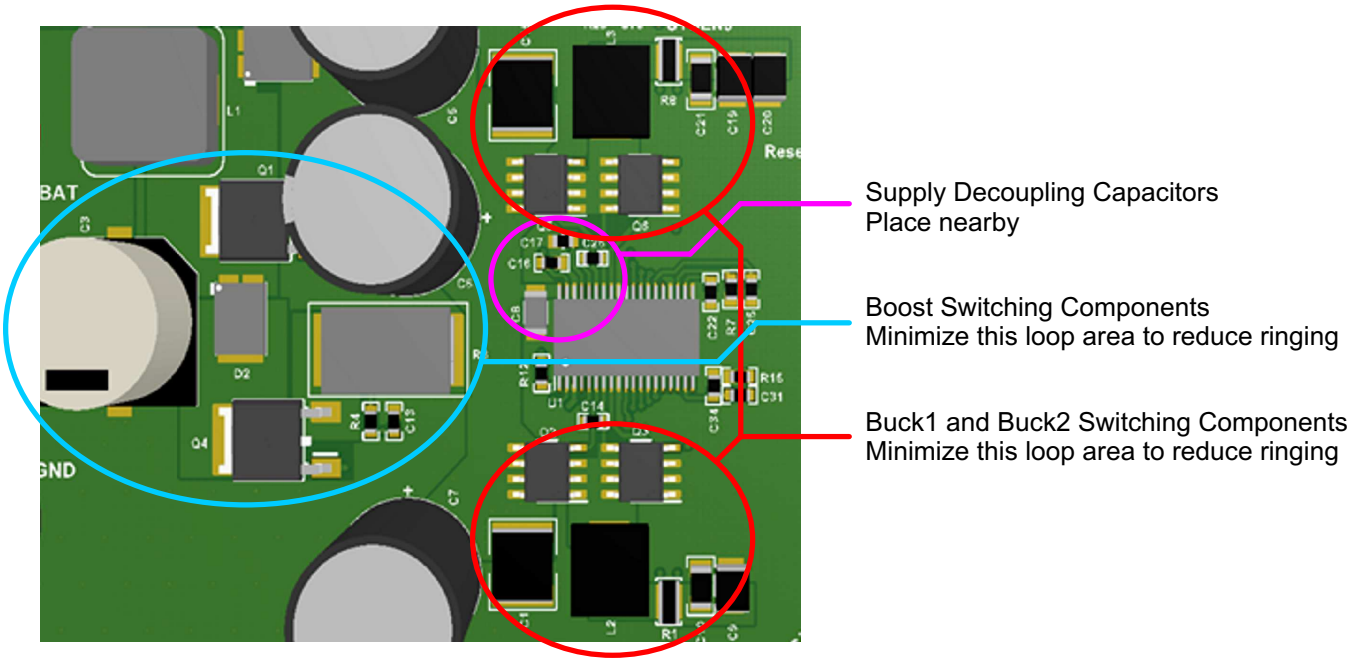


Figure 33. Layout Example (Top)

7.5.3 TPS659039-Q1 Layout Guidelines

As in every switch-mode-supply design, general layout rules apply:

- Use a solid ground-plane for power-ground (PGND)
- Use an independent ground for Logic, LDOs and Analog (AGND)
- Connect those Grounds at a star-point ideally underneath the IC.
- Place input capacitors as close as possible to the input-balls of the IC. This is placement is more important than the output-loop.
- Place the inductor and output capacitor as close as possible to the phase node (or switch-node) of the IC.
- Keep the loop-area formed by phase-node, Inductor, output-capacitor and PGND as small as possible.
- For traces and vias on power-lines, keep inductance and resistance as small as possible by using wide traces, avoid switching layers but if needed, use plenty of vias.

The goal of the previously listed guidelines is a layout that minimizes emissions, maximizes EMI-immunity, and maintains a safe operating area for the IC.

To minimize the spiking at the phase-node for both, high-side (VIN – SWx) as well as low-side (SWx – PGND), the decoupling of VIN is paramount. Appropriate decoupling and thorough layout should ensure that the spikes never exceed 9-V peak-to-peak at the IC.

7.5.4 TPS659039-Q1 Layout Example

Figure 34 and Figure 35 show the actual placement and routing on the EVM.

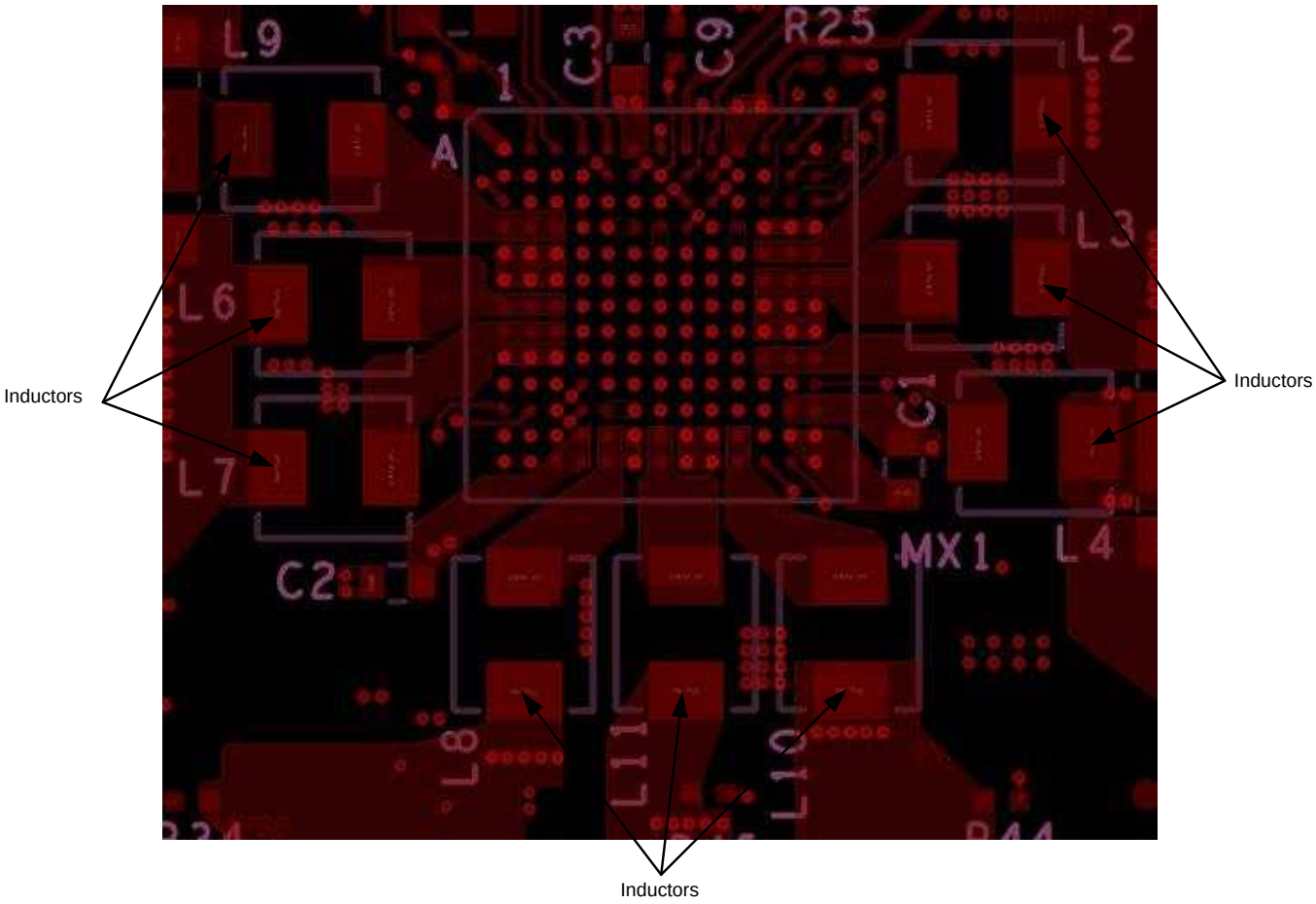


Figure 34. Top Layer Overview of Inductor Placement

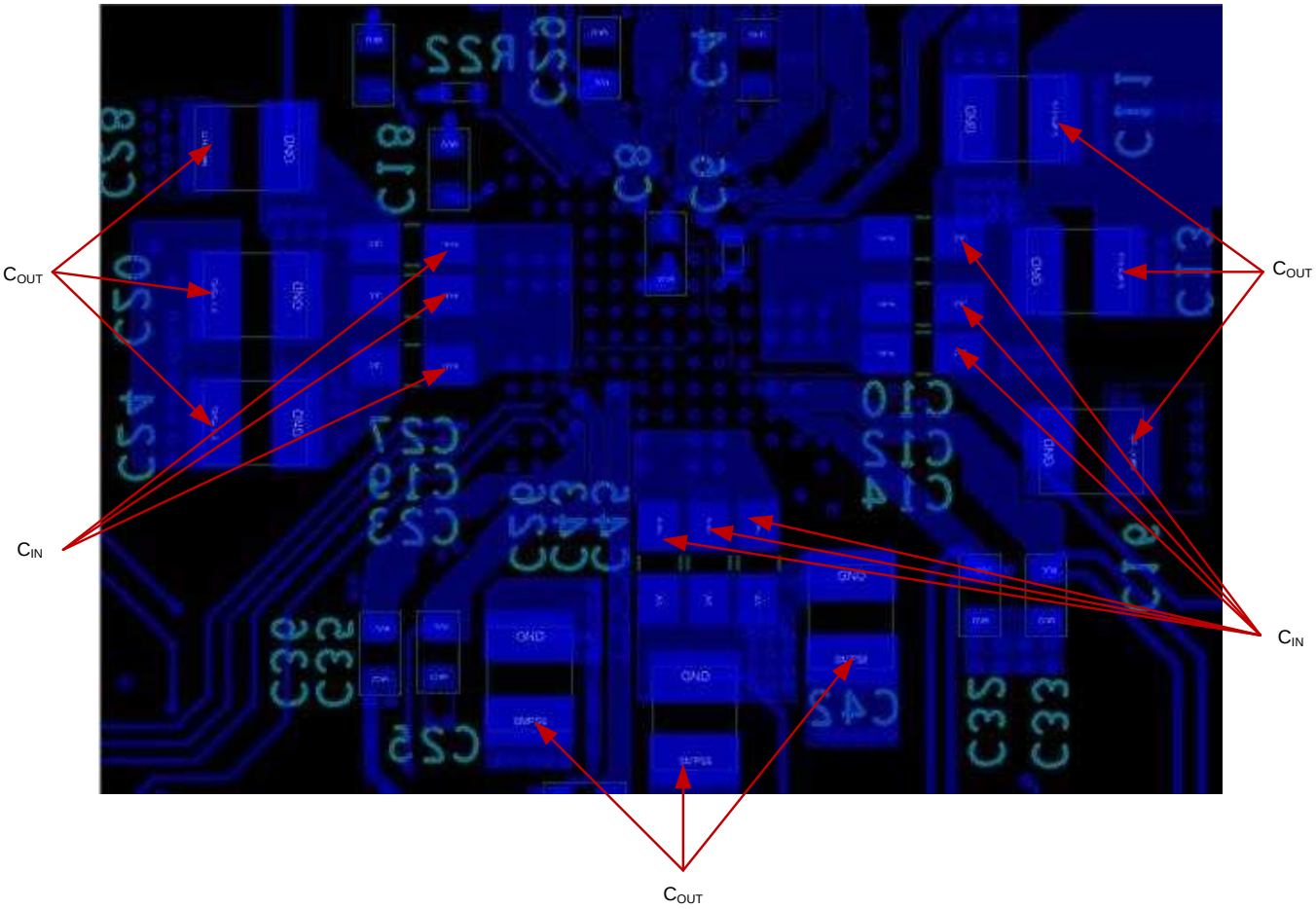
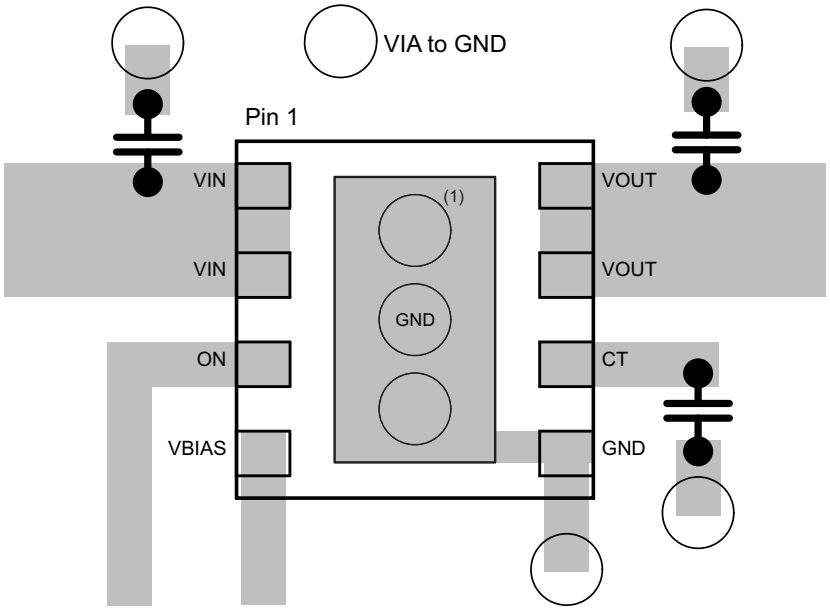


Figure 35. Bottom Layer Overview of Input and Output Capacitor Placement

7.5.5 TPS22965-Q1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace should be as short as possible to avoid parasitic capacitance.

7.5.6 TPS22965-Q1 Layout Example



(1) Thermal relief vias. Thermal relief vias connected to the exposed thermal pad

Figure 36. Layout Recommendation

7.5.7 TPS52100-Q1 Layout Example

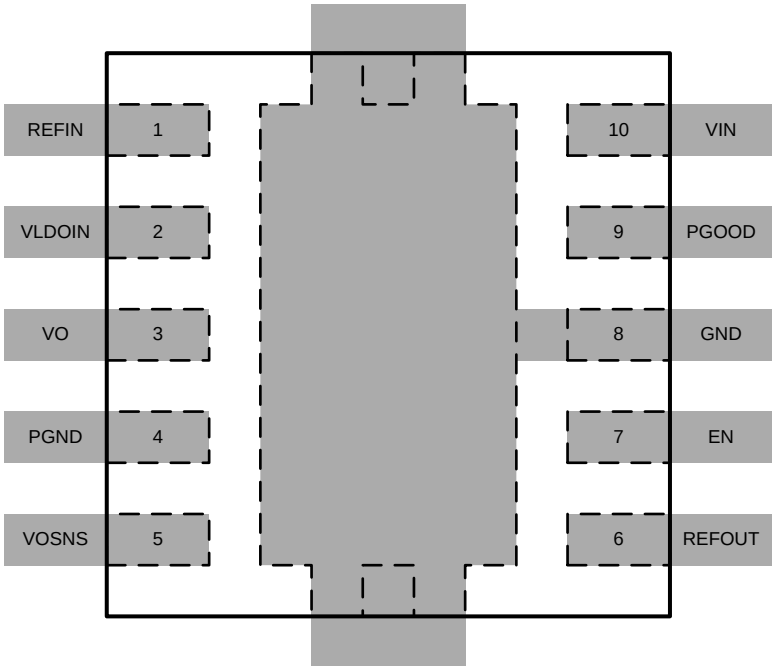


Figure 37. TPS51200-Q1 Layout Example

7.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00801

7.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00801

7.8 Software Files

To download the software files, see the design files at TIDA-00801.

8 References

1. Texas Instruments, *Cranking Simulator Reference Design for Automotive Applications*, Reference Design Guide, TIDU143
2. Texas Instruments, *Noise Analysis in Operational Amplifier Circuits* Application Report, SLVA043
3. Texas Instruments, *TPS65903x-Q1 EVM User's Guide*, SWCU174

9 About the Author

FRANK DEHMELT Frank Dehmelt graduated from Fachhochschule München (Munich Polytech, Germany) as an electrical engineer in 1997 and joined Texas Instruments as a Field Application Engineer (FAE) for interface products for communication infrastructure and industrial. He extended his expertise into Data Converters and Amplifiers when defining products in these domains for the European markets as a Systems engineer. In 2010, Frank changed his focus and joined the Mixed Signal Automotive Team as an Application engineer for Power Management, supporting both battery-connected products and processor-supplies.

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