# TIDA-00530,

## Automotive Power Reference Design for Low Power TDA3x Based Systems

## Test Setup

The following diagrams show how to set up for various tests

### Ripple and Thermal Image Setup

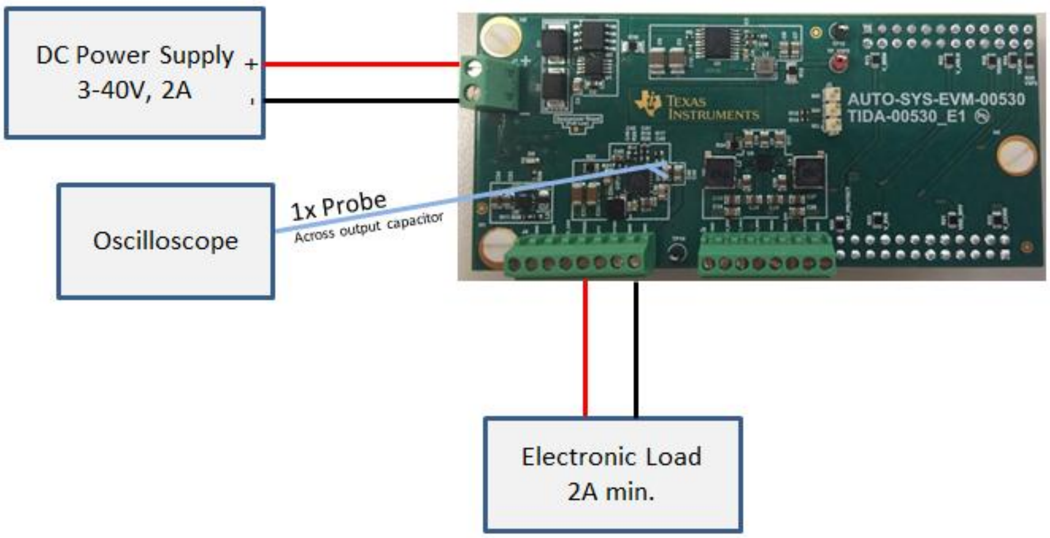


**Figure 1: Setup for measuring output voltage ripple of DCDC converters**

### Load Transient Setup

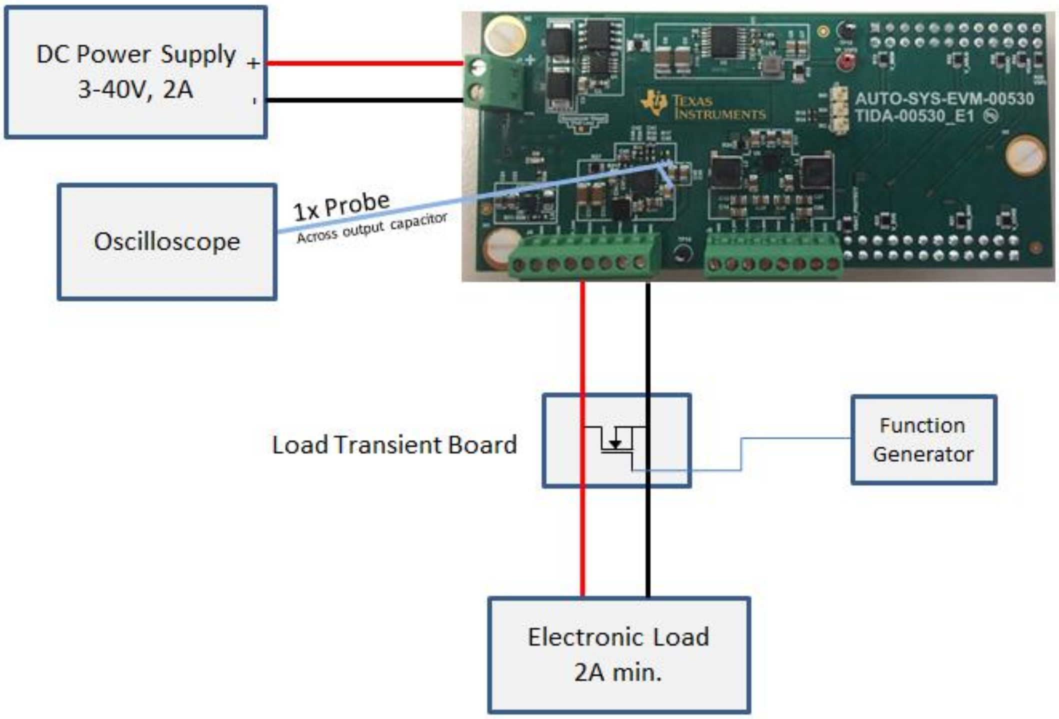


**Figure 2: Setup for conducting Load Transient tests**

## *Efficiency Setup*

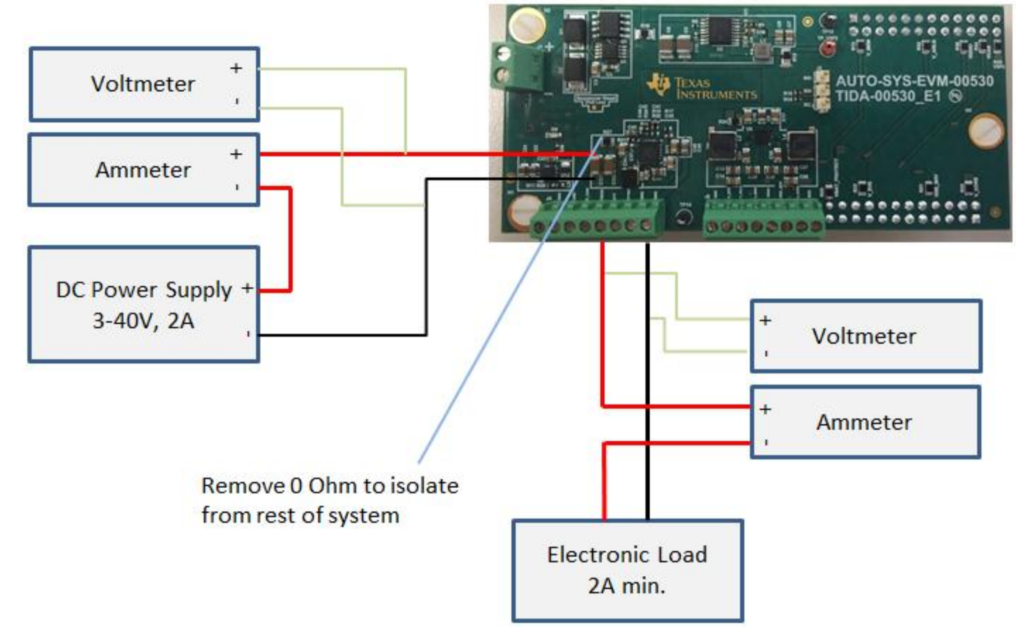


**Figure 3: Setup for measuring DCDC efficiency**

## *Load Regulation Setup*

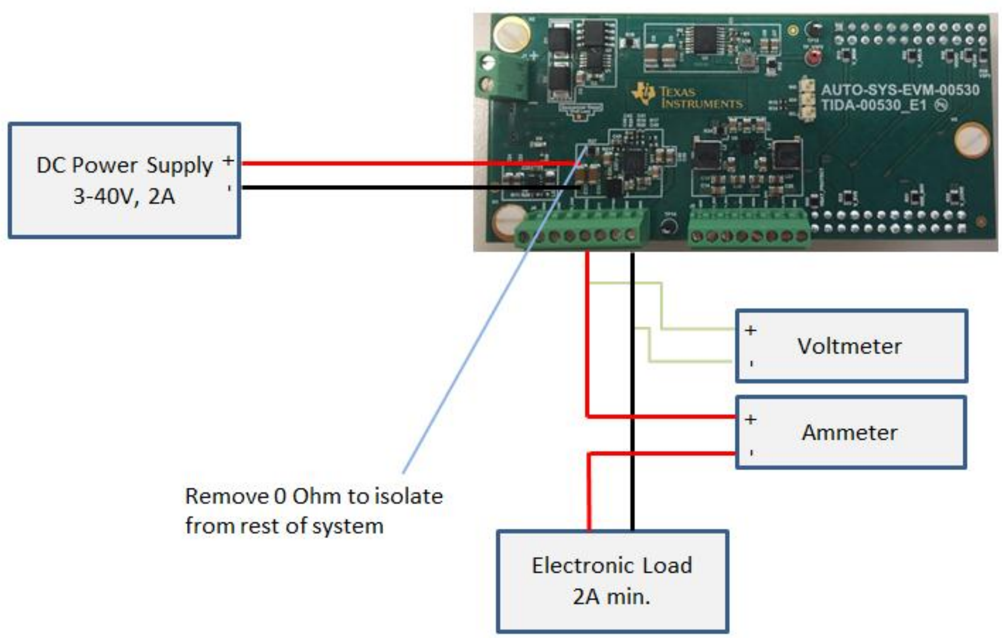


**Figure 4: Setup for measuring Load Regulation**

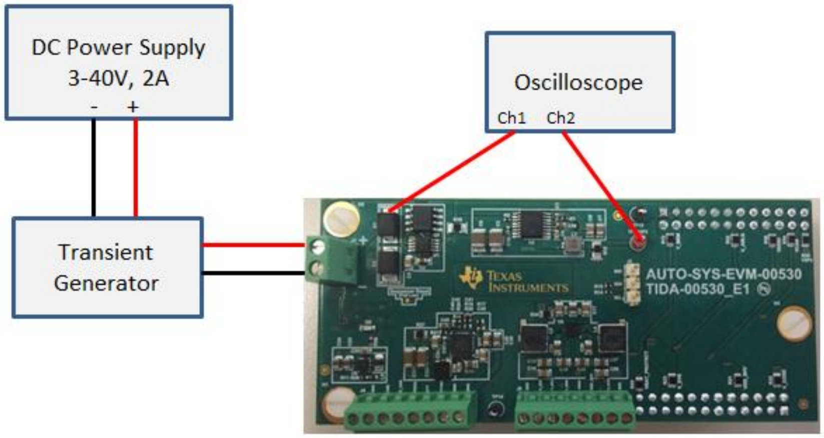


**Figure 5: Electrical Transient Setup (NSG 5500 used for Transient Generator)**

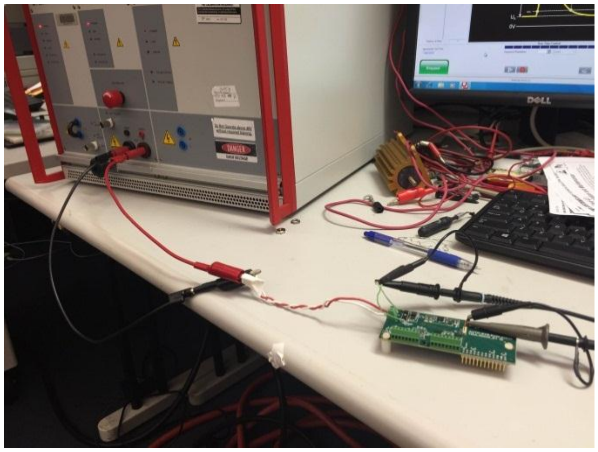

**Figure 6: Picture of setup for transient tests**

To work with the NSG 5500 you will also need the [Teseq AutoStar software](), which has pre-defined pulses which the user can tweak to meet specific requirements. Below is an example:

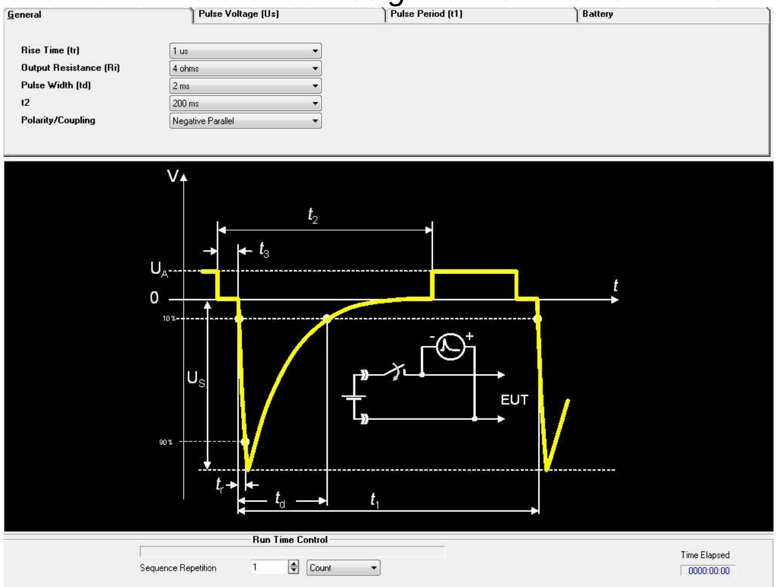


**Figure 7: AutoStar setup for Pulse 1**

# Test Data

The following sections show the test data from characterizing the switching power supplies in the system.

## *DCDC Efficiency*

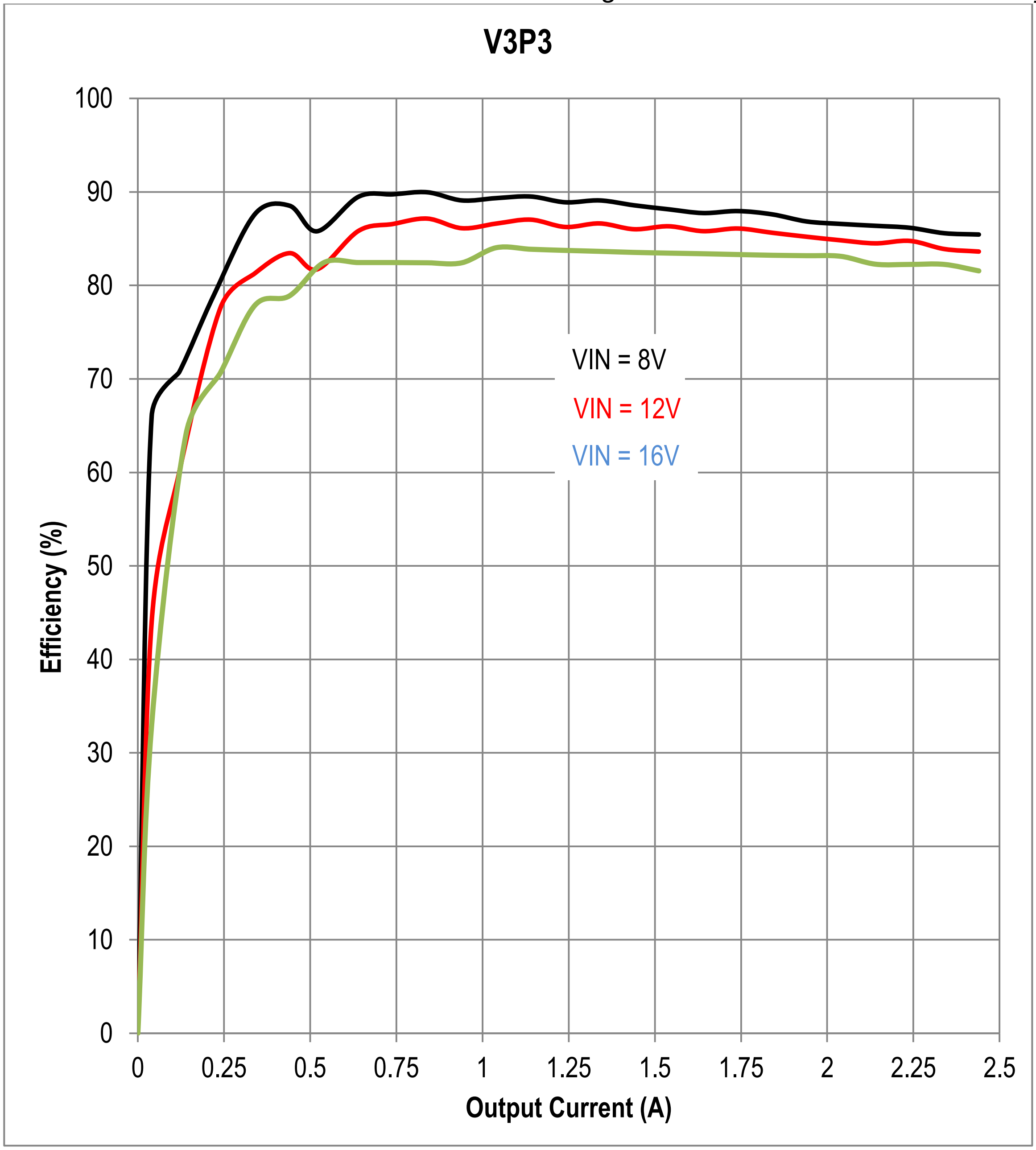


**Figure 8: V3P3 Efficiency**

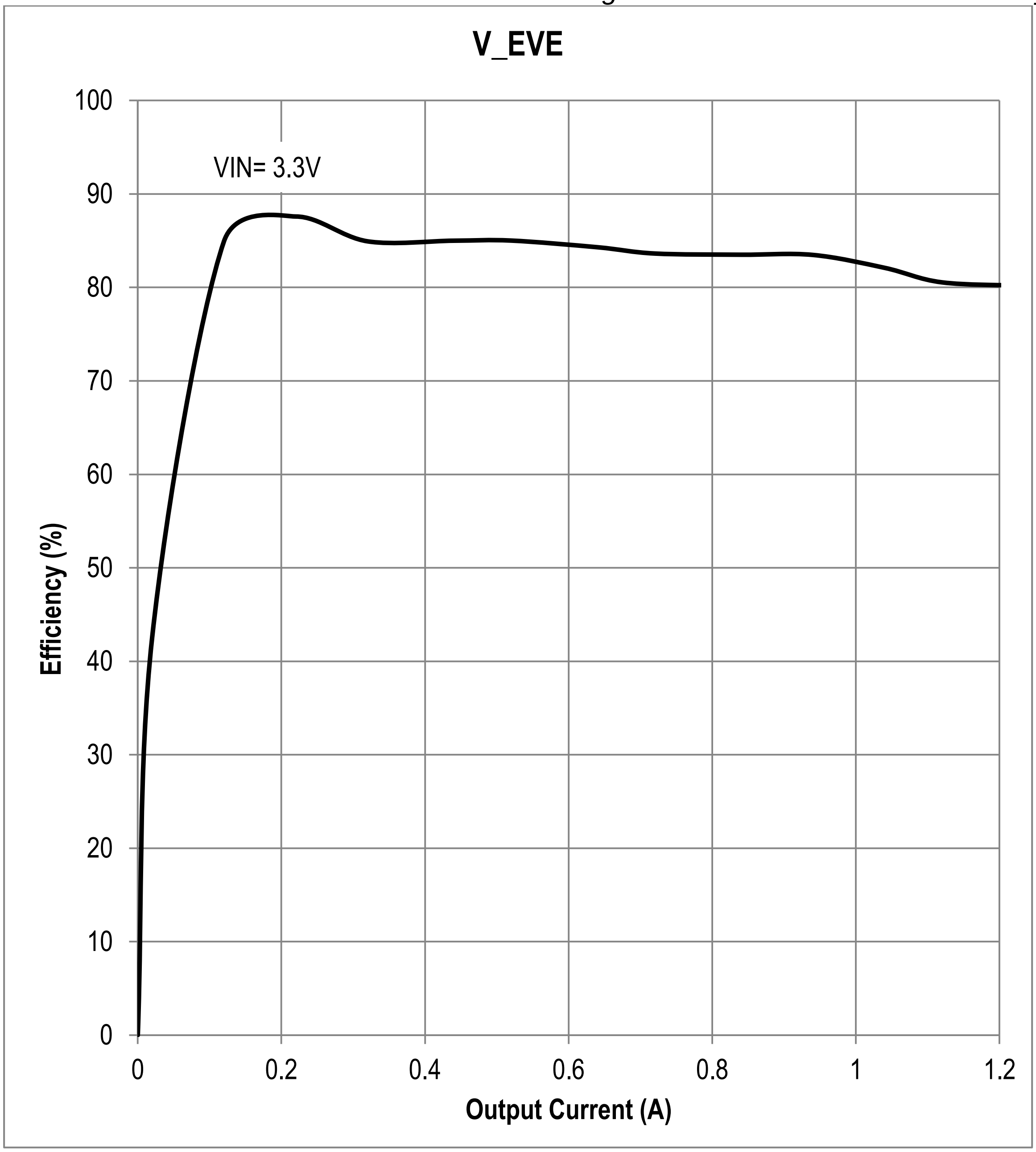


**Figure 9: VEVE Efficiency**

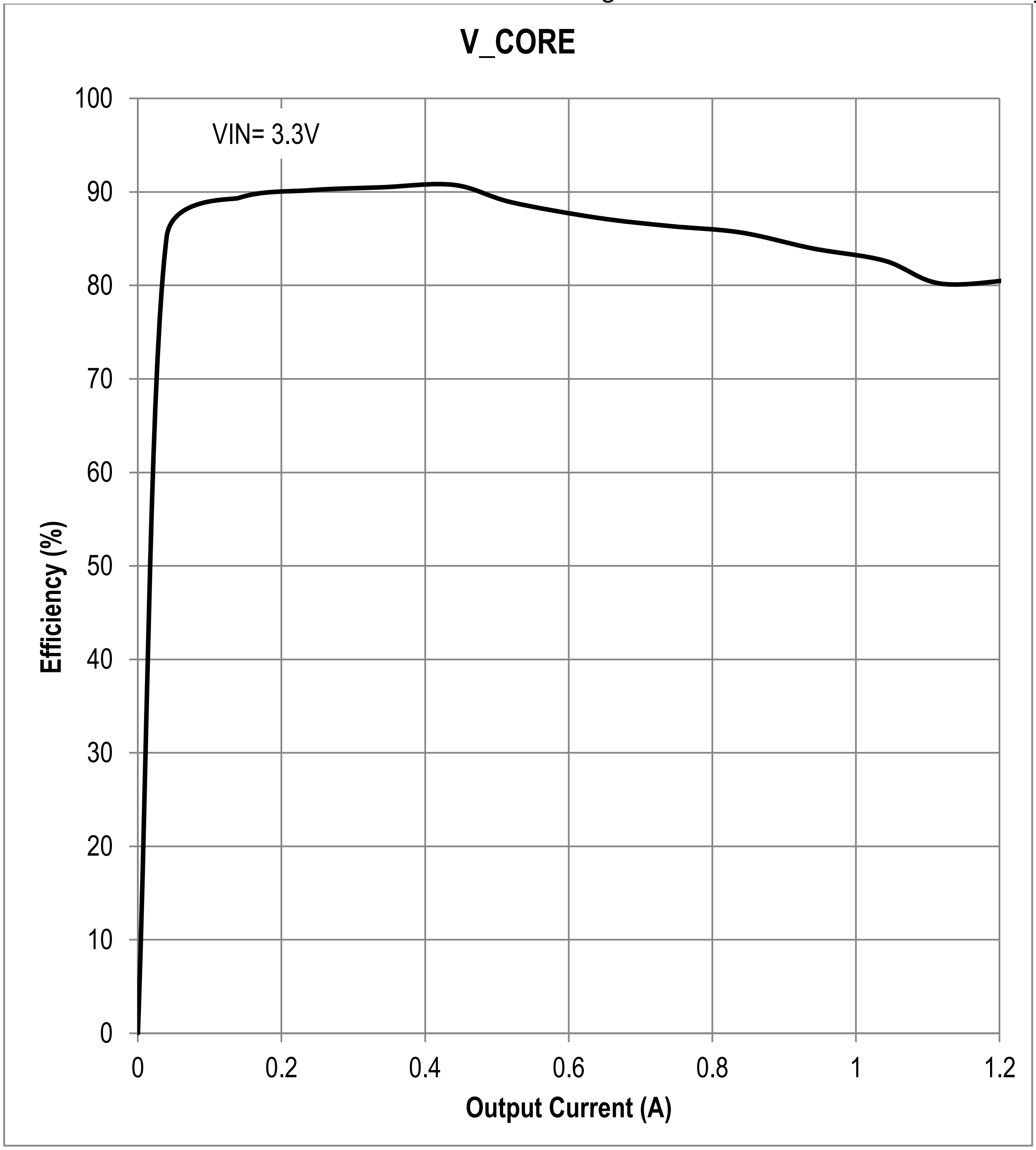


**Figure 10: VCORE Efficiency**

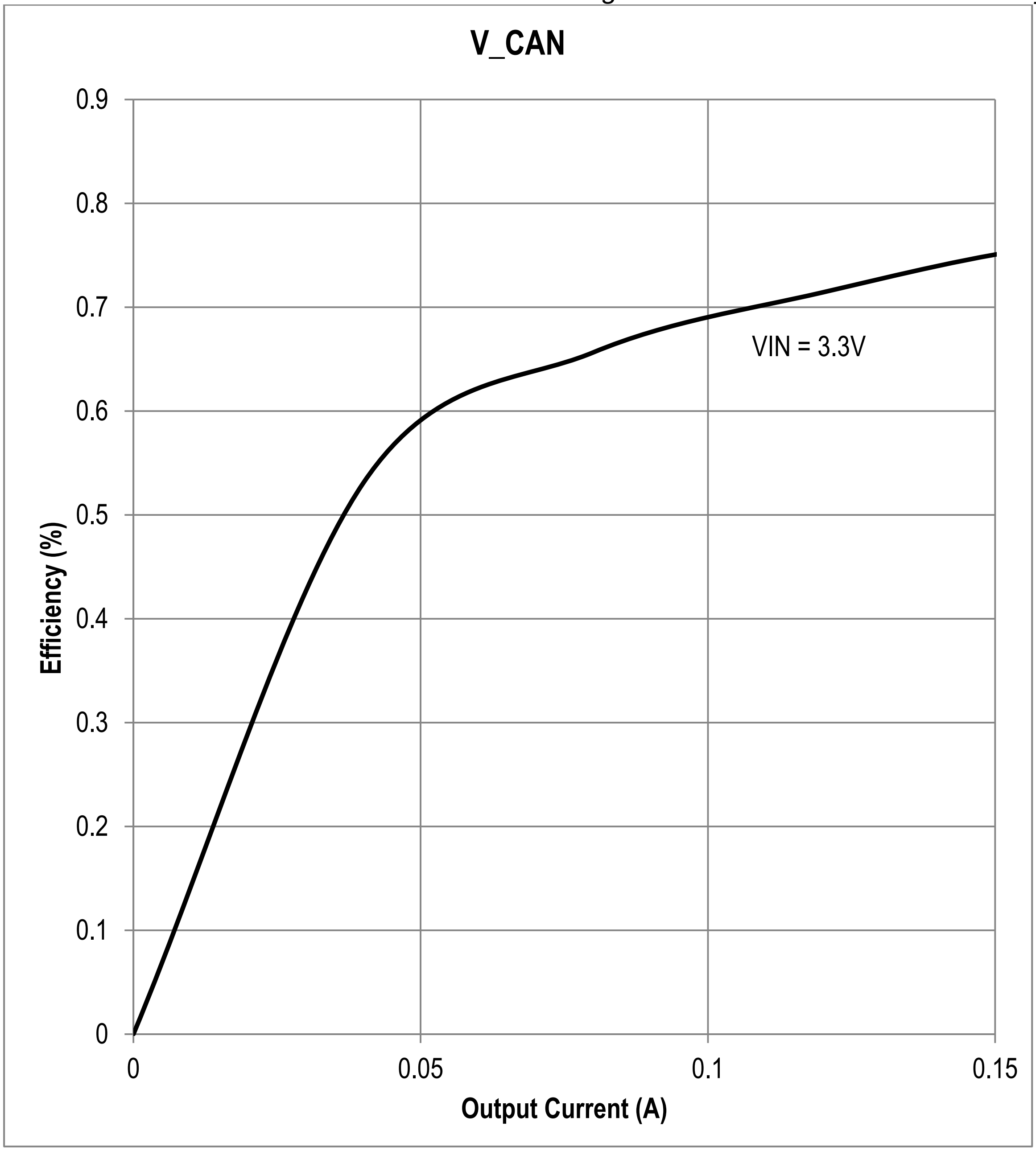


**Figure 11: VCAN Efficiency**

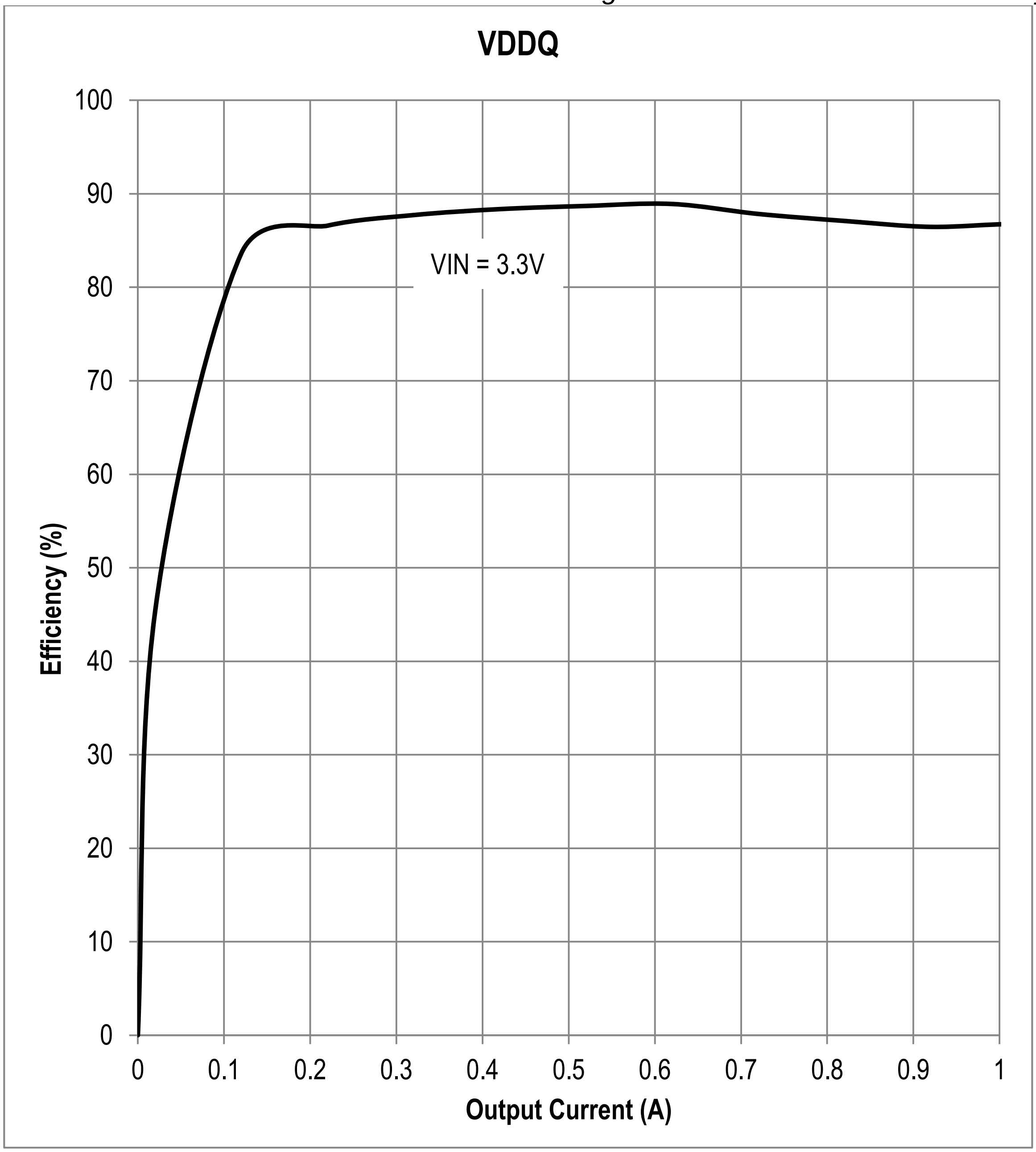


**Figure 12: VDDQ Efficiency**

## *Load Regulation*

The results below show the % deviation from nominal output voltage as a function of output current.

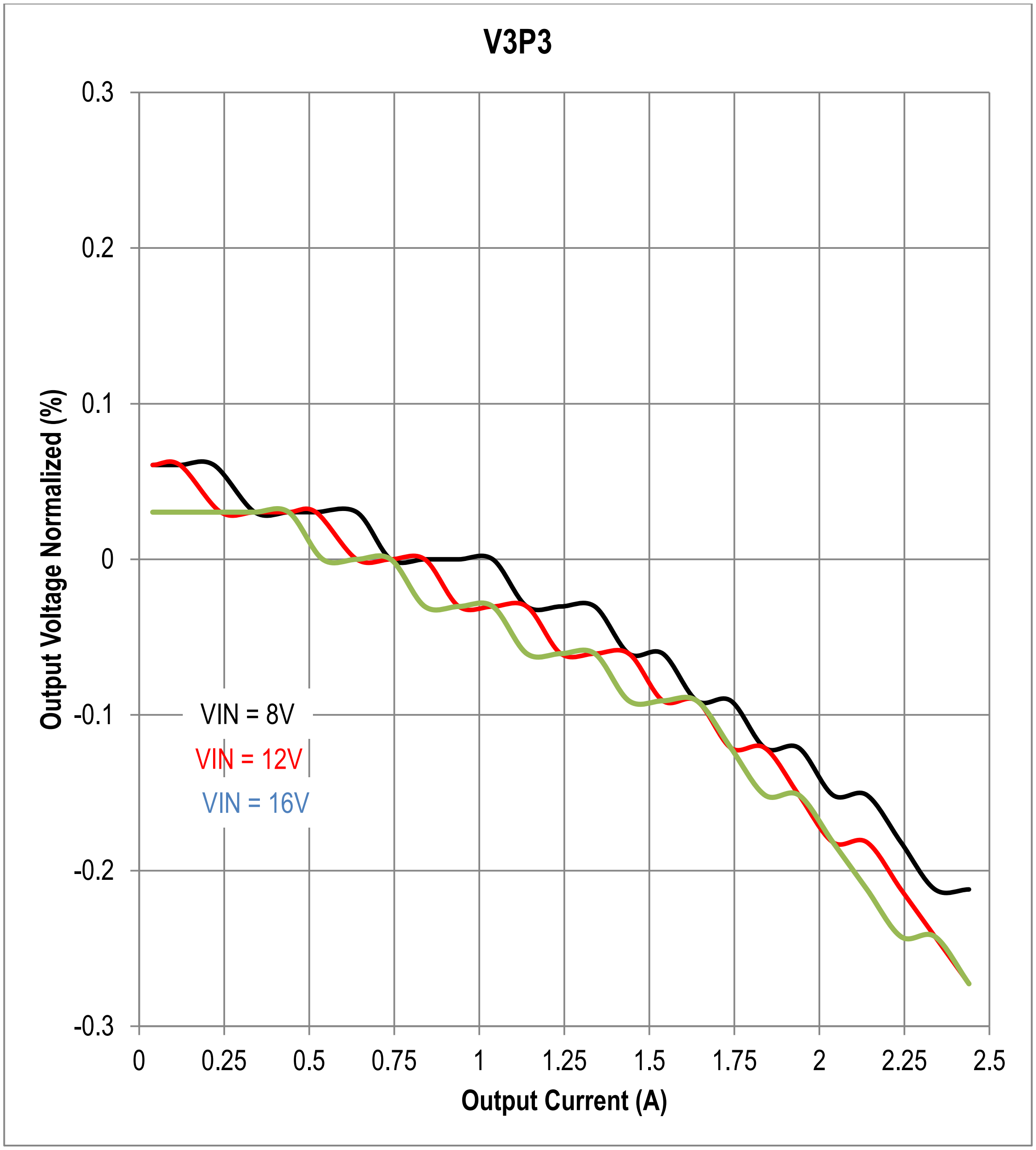


**Figure 13: V3P3 Load Regulation 0-2.5A, 8-16Vin**

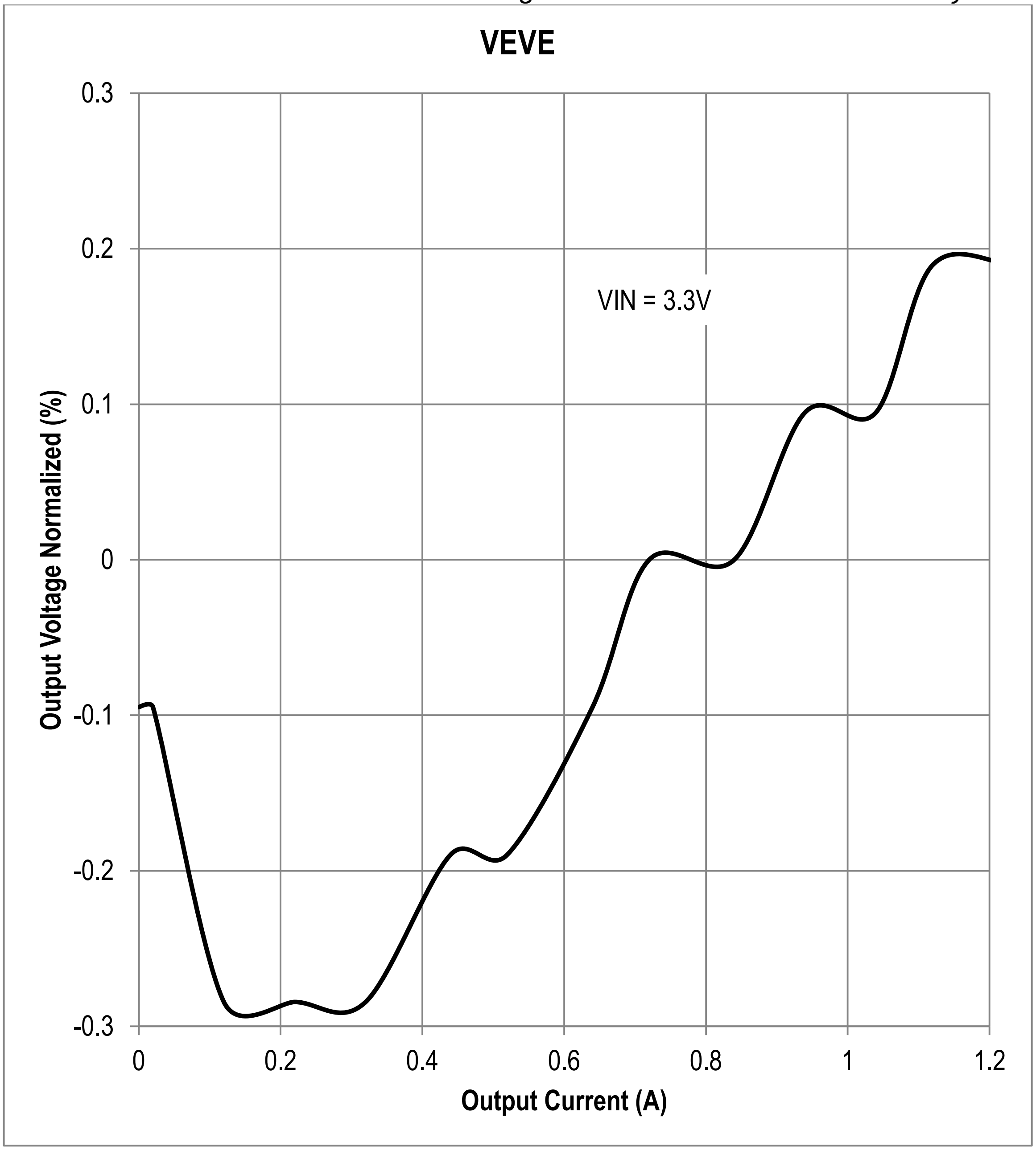


**Figure 14: VEVE Load Regulation 0-1.2A**

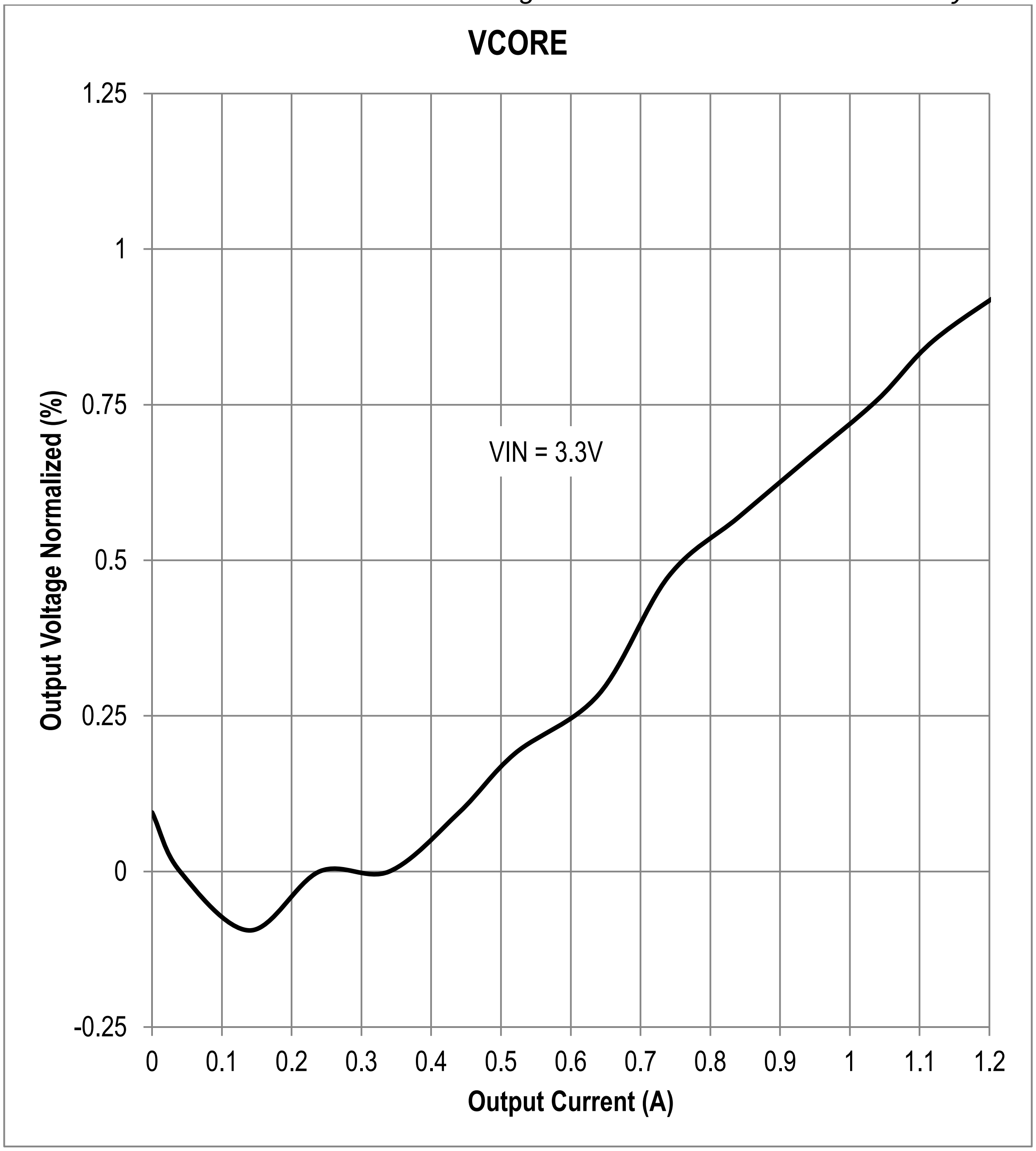


**Figure 15: VCORE Load Regulation 0-1.2A**

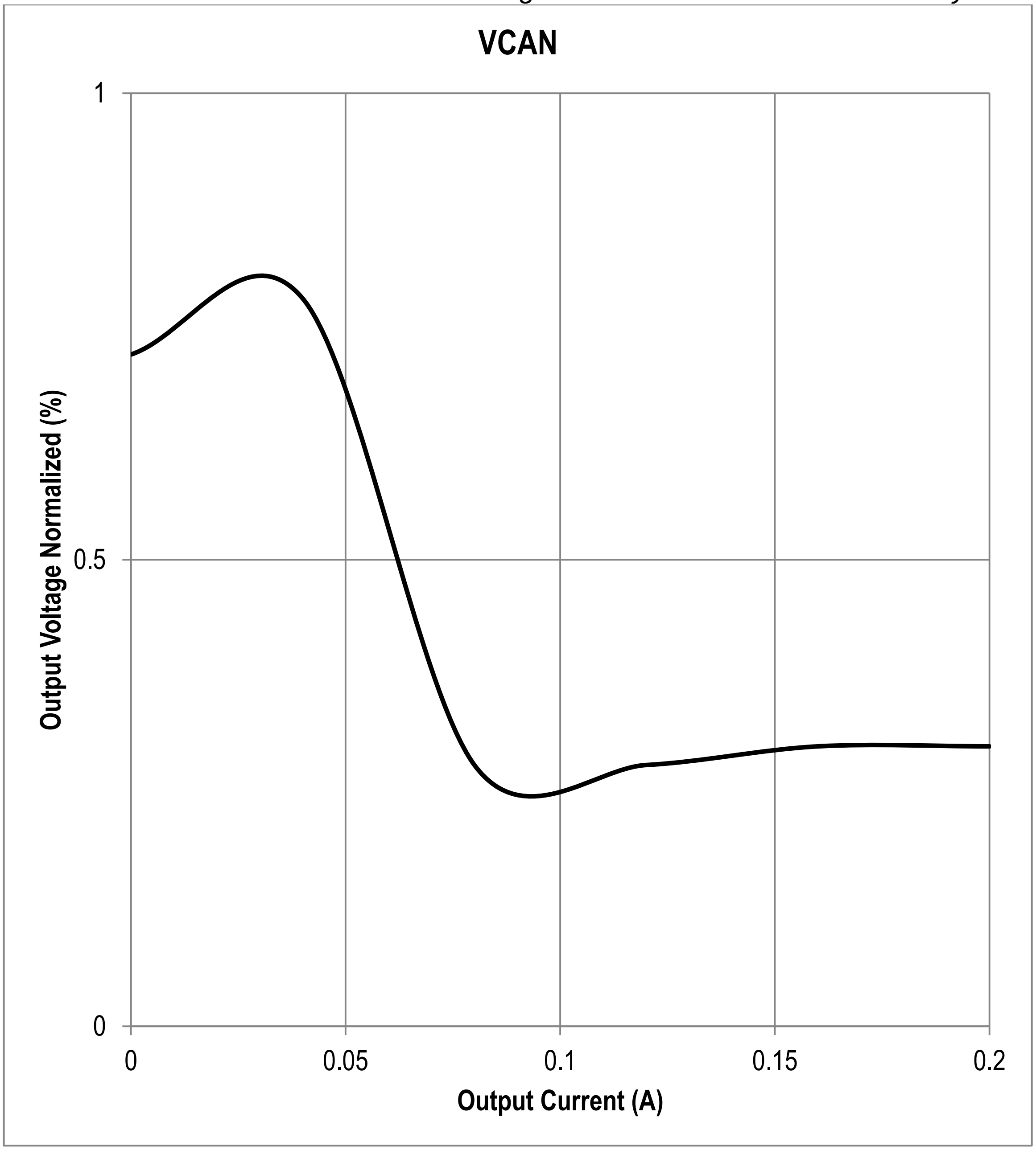


**Figure 16: VCAN Load Regulation 0-0.2A**

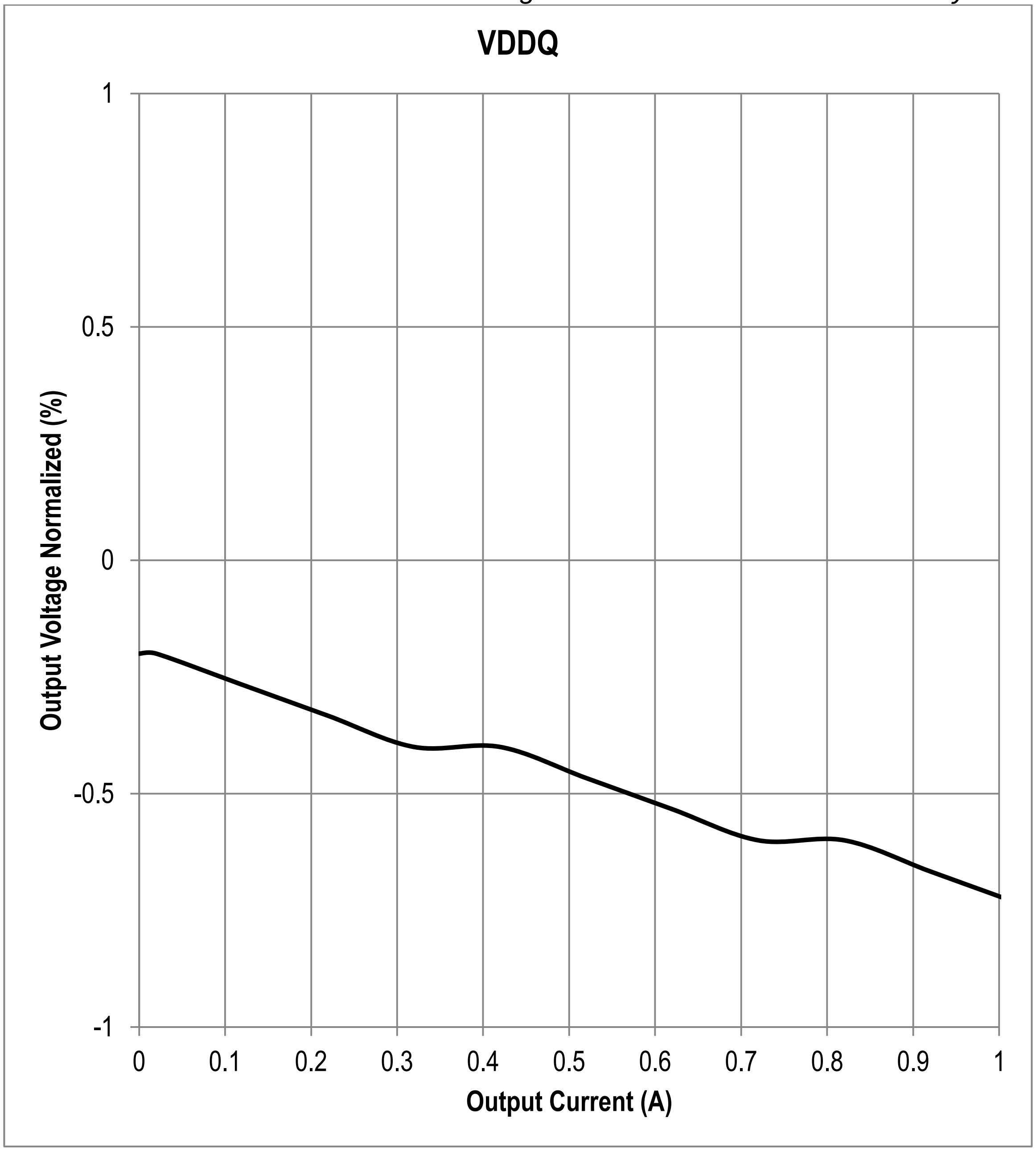


**Figure 17: VDDQ Load Regulation 0-1A**

## ***Start-up sequencing waveforms***

These images show the sequencing of relevant supplies during power-up.

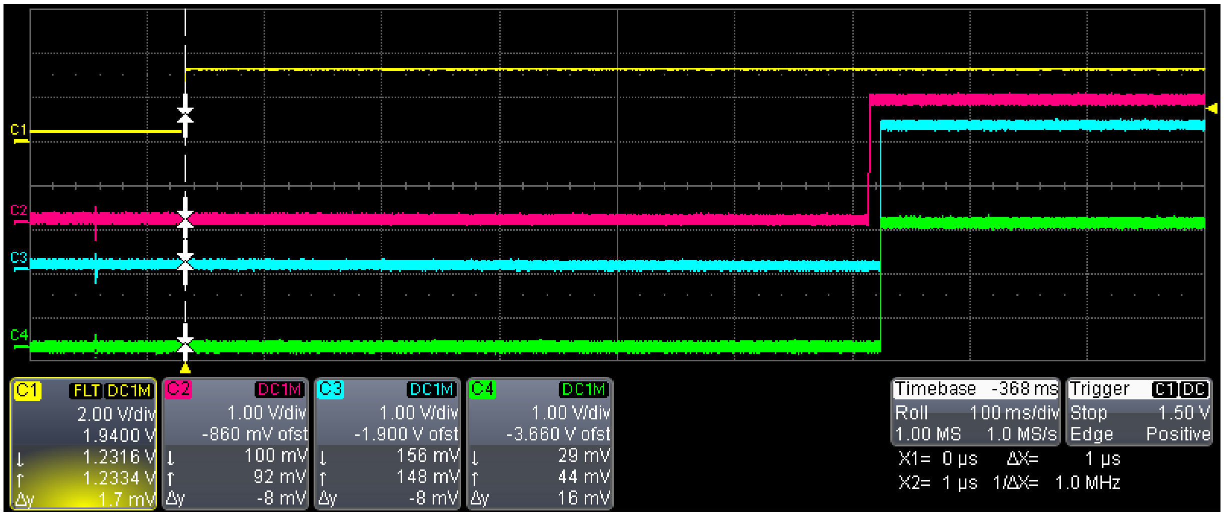


**Figure 18: Startup Waveform 1**

Ch.1: V3P3
Ch.2: VDDIO
Ch.3: V_MEM
Ch.4: V_ANLG

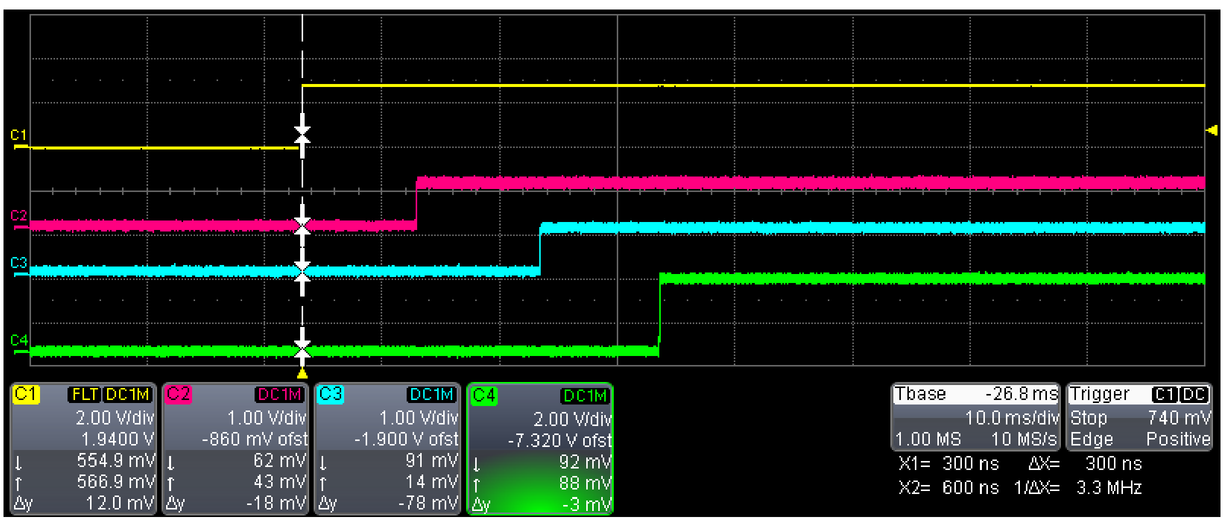


**Figure 19: Startup Waveform 2**

Ch.1: V_ANLG
Ch.2: V_CORE
Ch.3: V_EVE
Ch.4: VDD_SHV

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## ***Power-down sequencing waveforms***

These images show the sequencing of relevant supplies during power-down

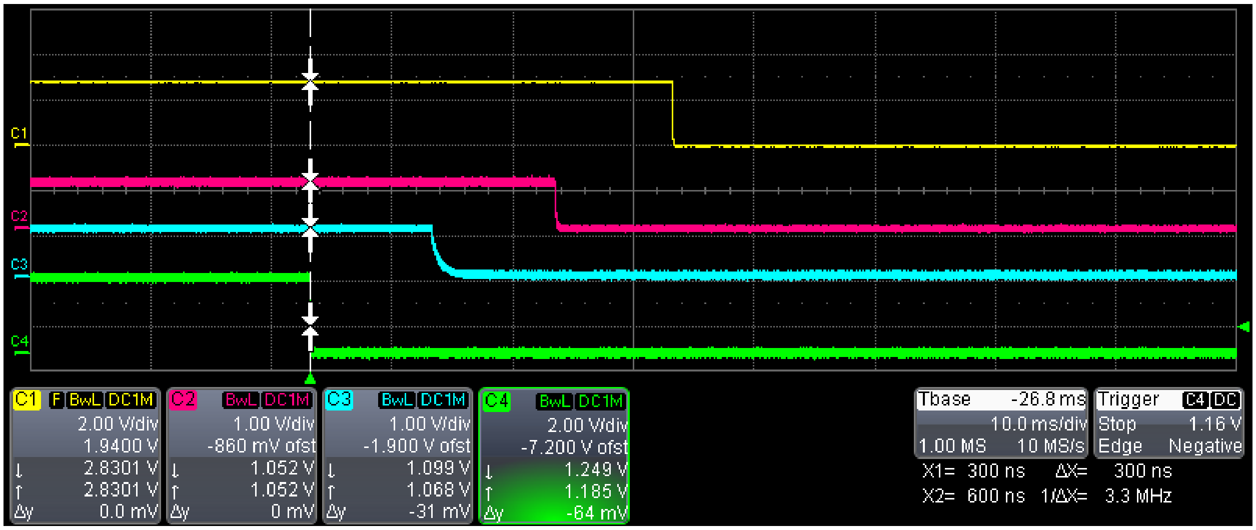


**Figure 20: Shutdown Waveform 1**

Ch.1: VDD_SHV
Ch.2: V_EVE
Ch.3: V_CORE
Ch.4: V_ANLG

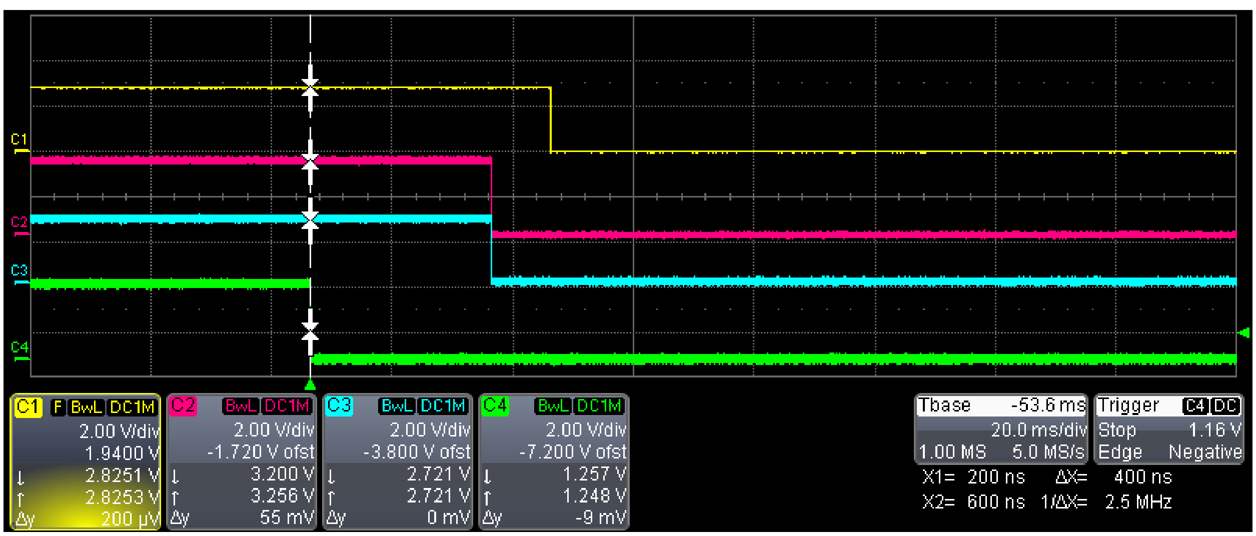


**Figure 21: Shutdown Waveform 2**

Ch.1: V_CORE
Ch.2: V_ANLG
Ch.3: V_MEM
Ch.4: VDDIO

## ***DCDC output voltage ripple***

The images below show the output voltage ripple at full load of each DCDC. Where possible the switch node is also shown. Vin=12V

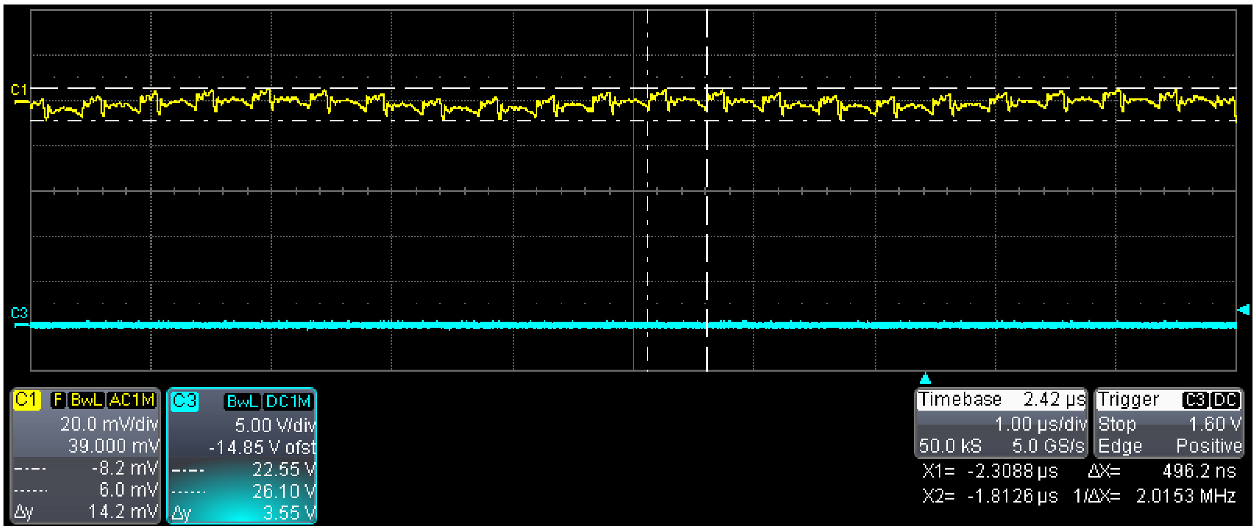


**Figure 22: V3P3, VOUT = 3.3V, IOUT = 2.5A**

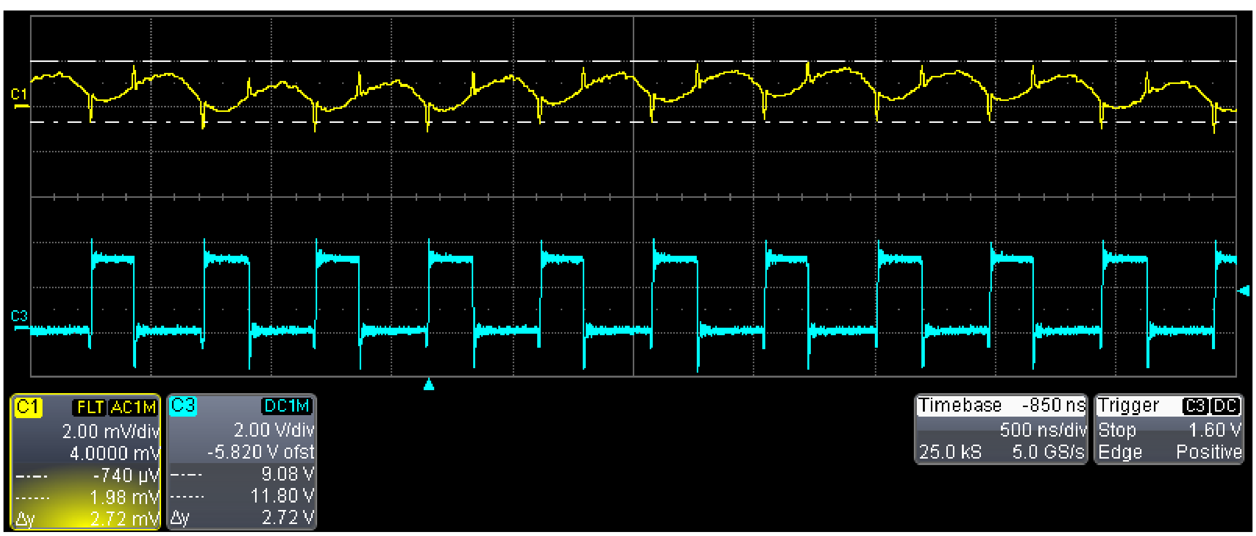


**Figure 23: V_EVE, VOUT = 1.06V, IOUT = 1.2A**

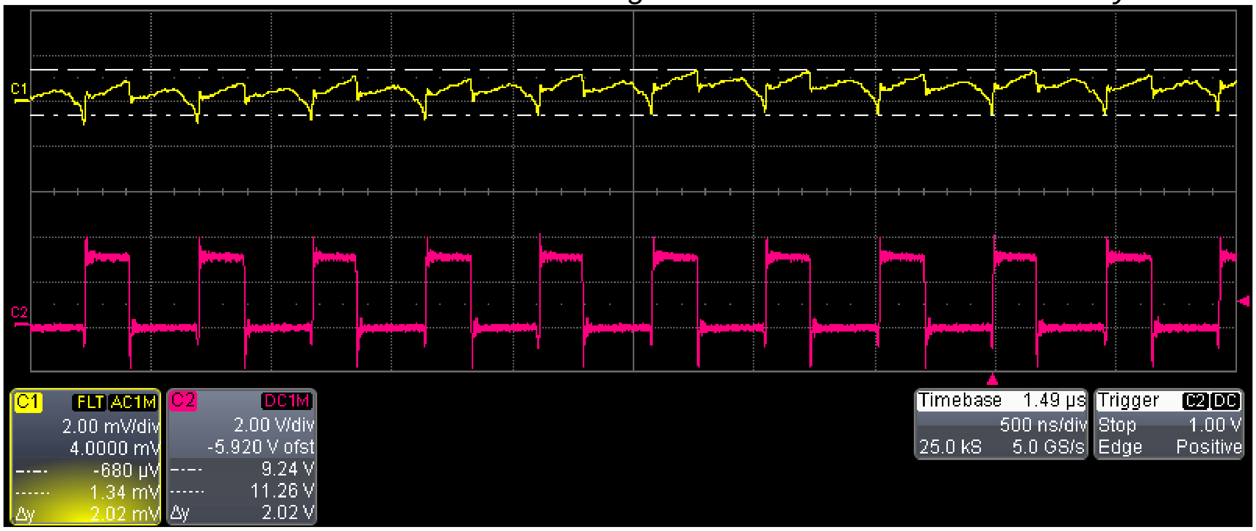


**Figure 24: V_CORE, VOUT = 1.06V, IOUT = 1.2A**

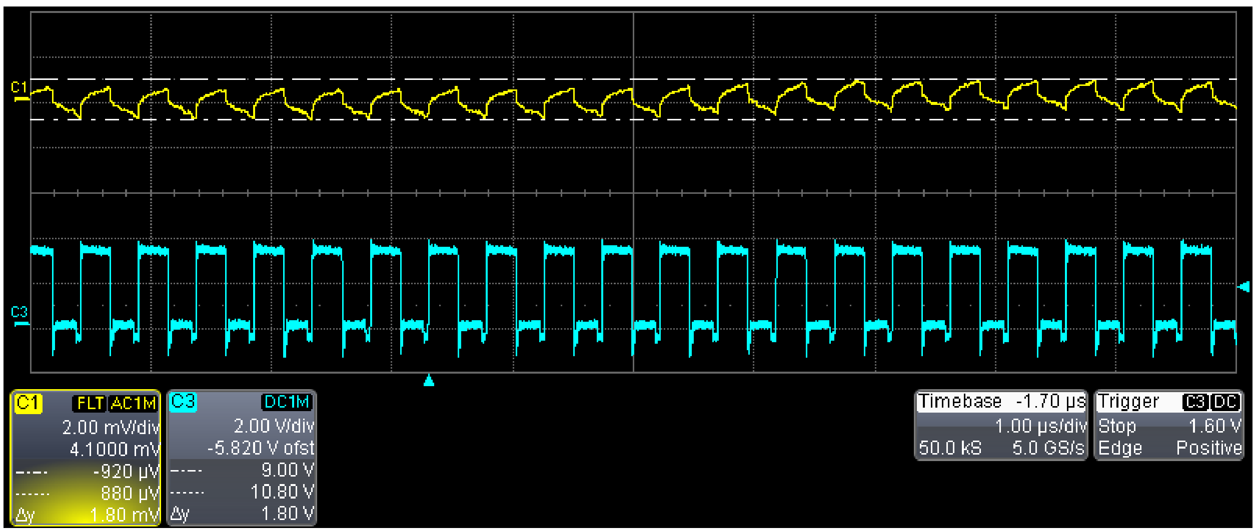


**Figure 25: VDDQ, VOUT = 1.5V, IOUT = 1A**

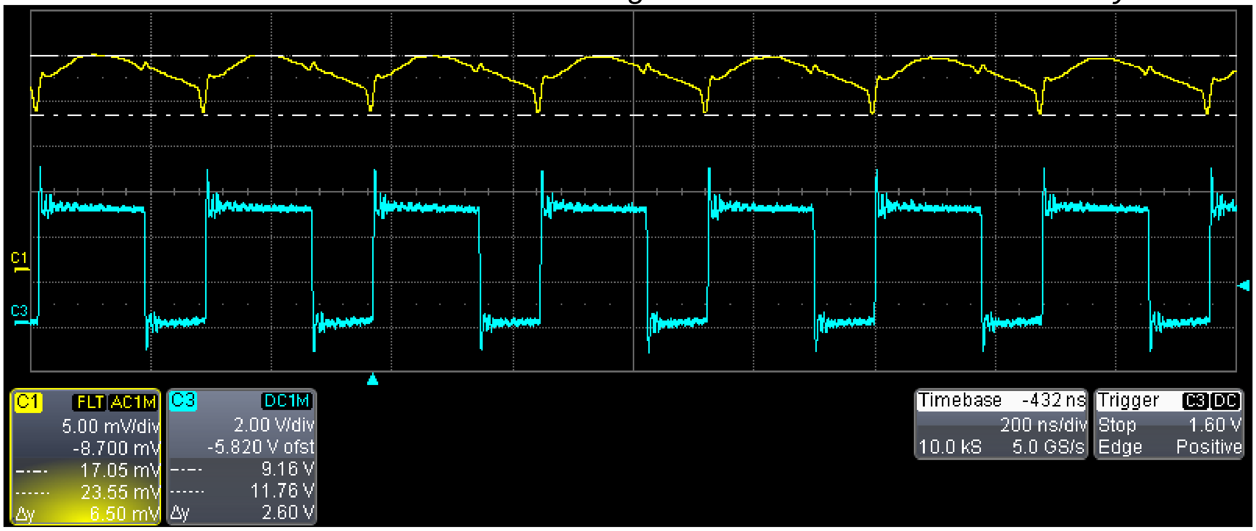


**Figure 26: V_CAN, VOUT = 5V, IOUT = 200mA**

## DCDC Load Transients

The below images show the transient response for load-step and load-release at 25% of full load.

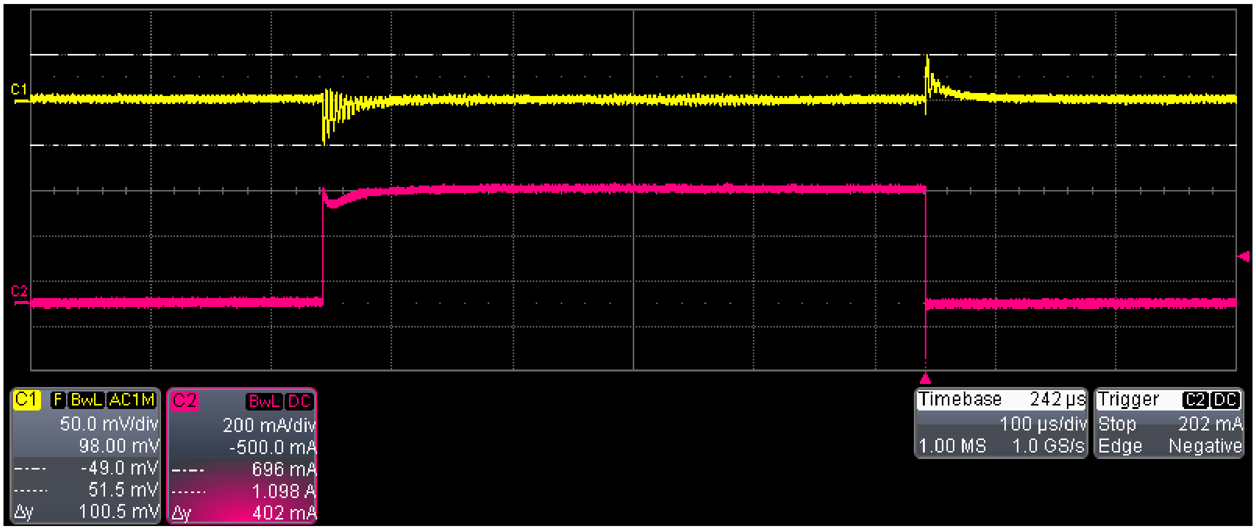


**Figure 27: V3P3, VOUT = 3.3V, IOUT_STEP = 500mA**

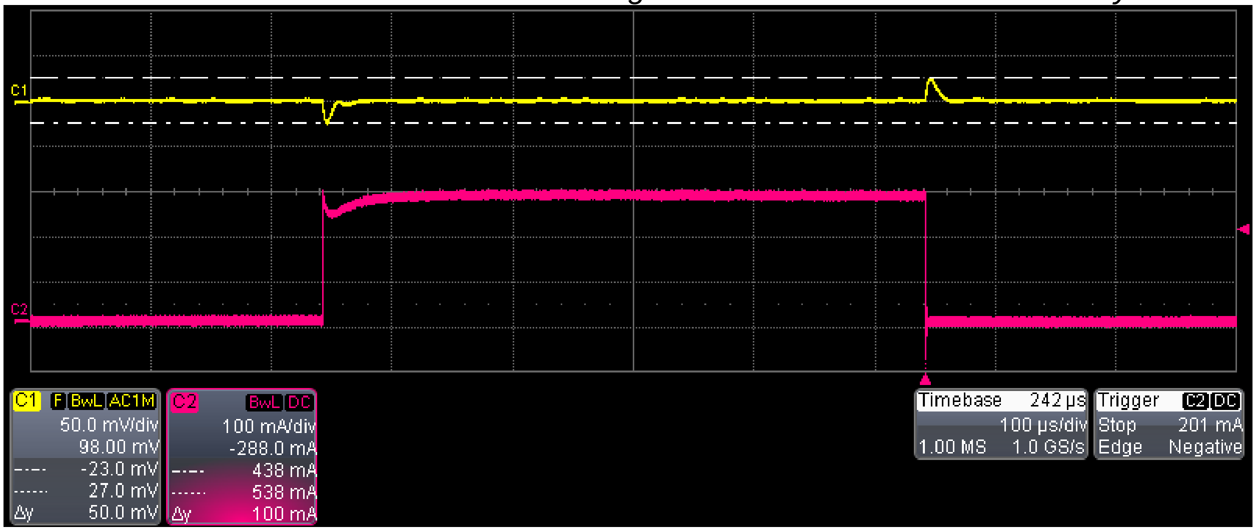


**Figure 28: V_EVE, VOUT = 1.06V, IOUT_STEP = 300mA**

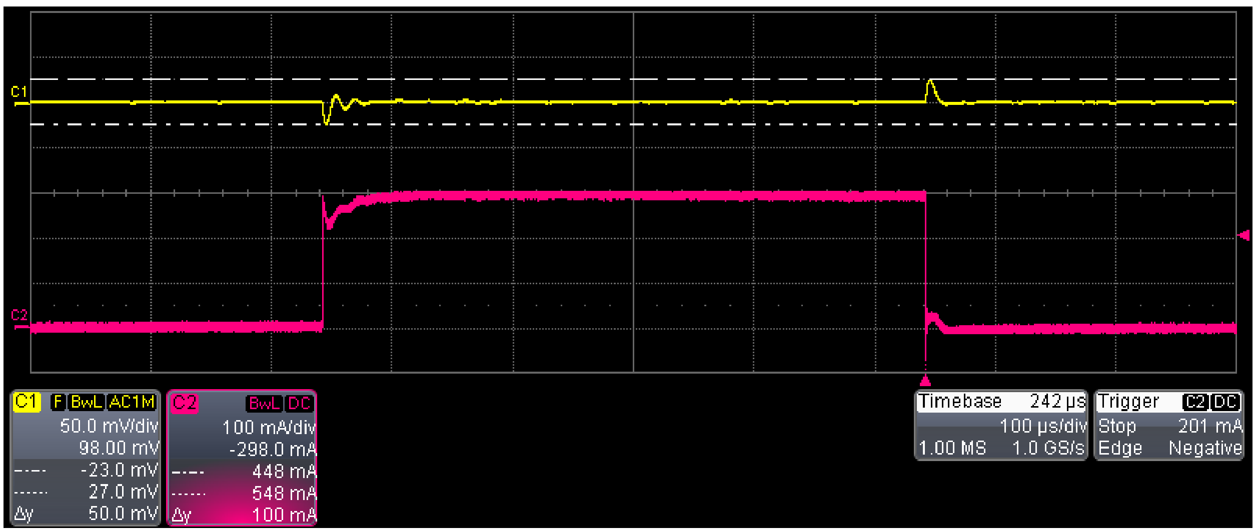


**Figure 29: V_CORE, VOUT = 1.06V, IOUT_STEP = 300mA**

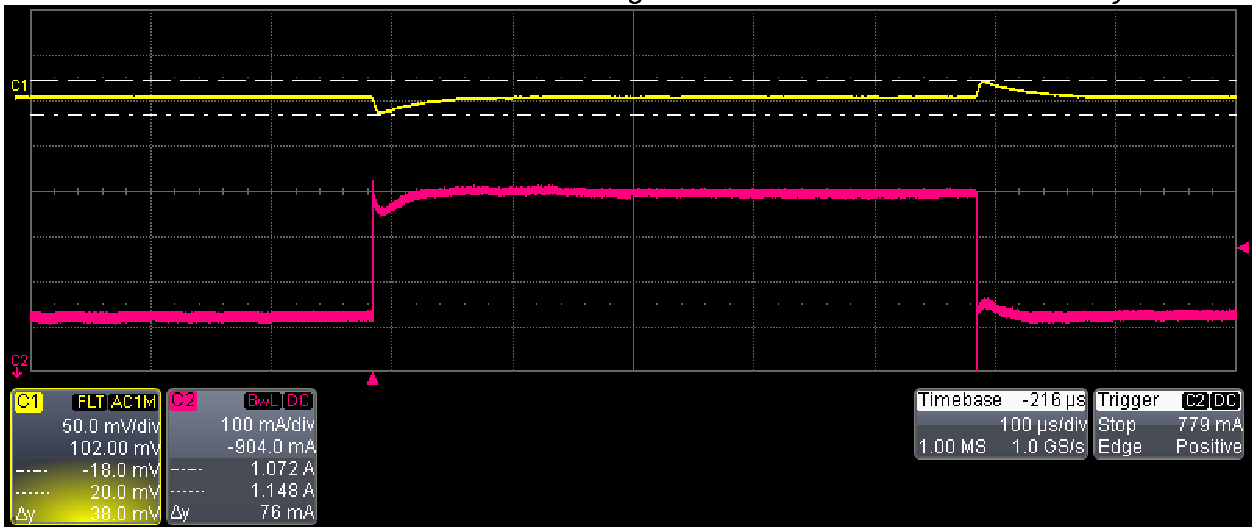


**Figure 30: VDDQ, VOUT = 1.5V, IOUT_STEP = 250mA**

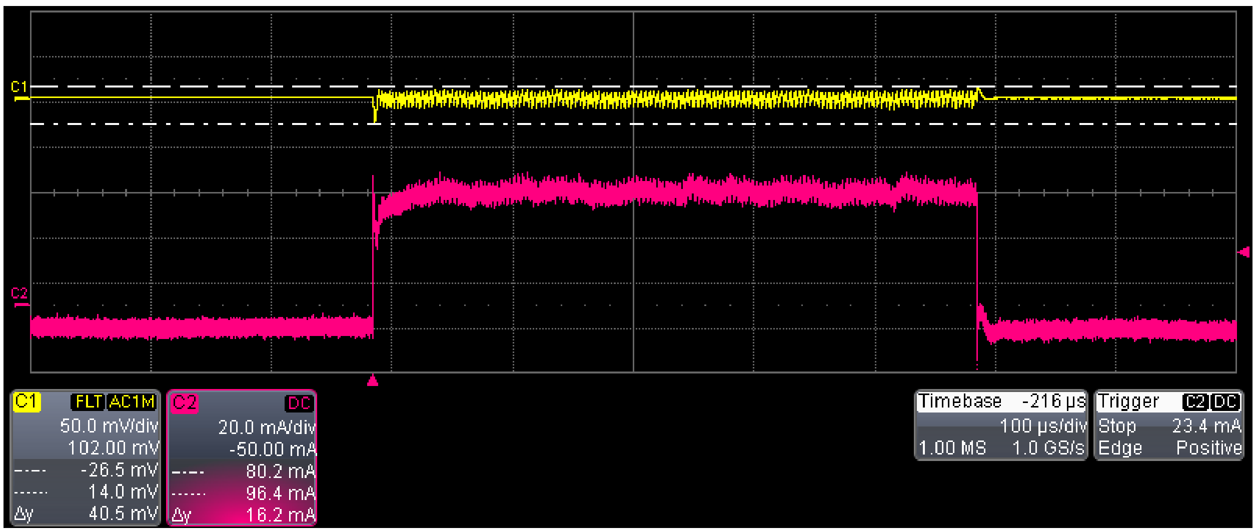


**Figure 31: V_CAN, VOUT = 5V, IOUT_STEP = 50mA**

## *Thermal images*

The below images show the temperature rise of the different components on the board at various load conditions.

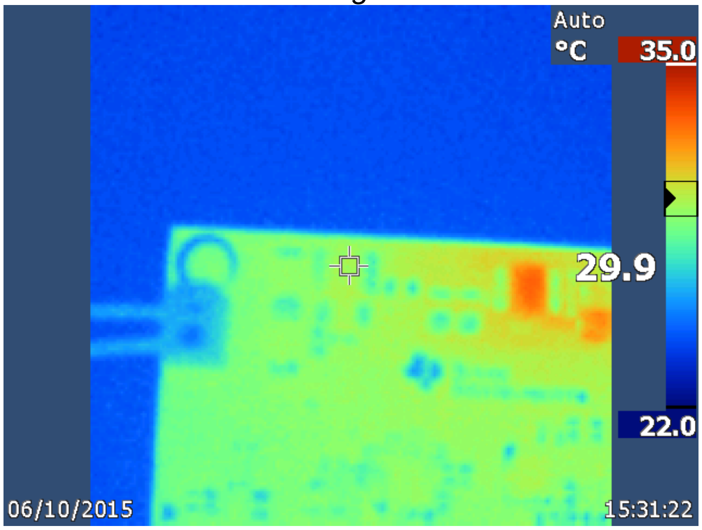


**Figure 32: LM74610 (reverse polarity protection) FET, no load**

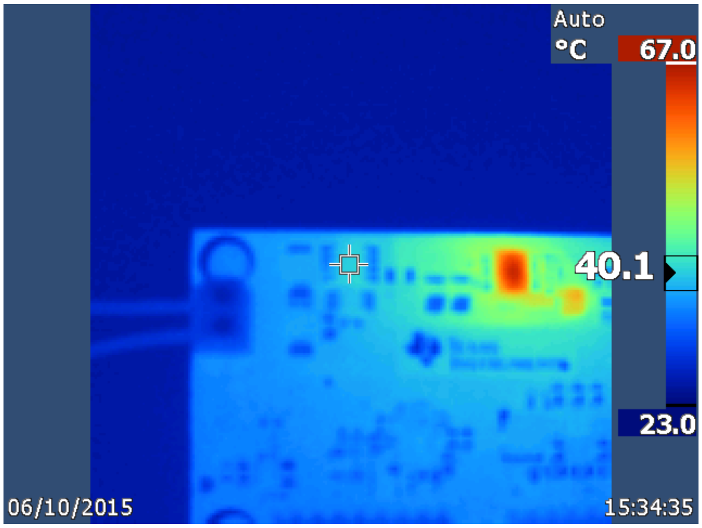


**Figure 33: LM74610 (reverse polarity protection) FET, full board load, steady state**

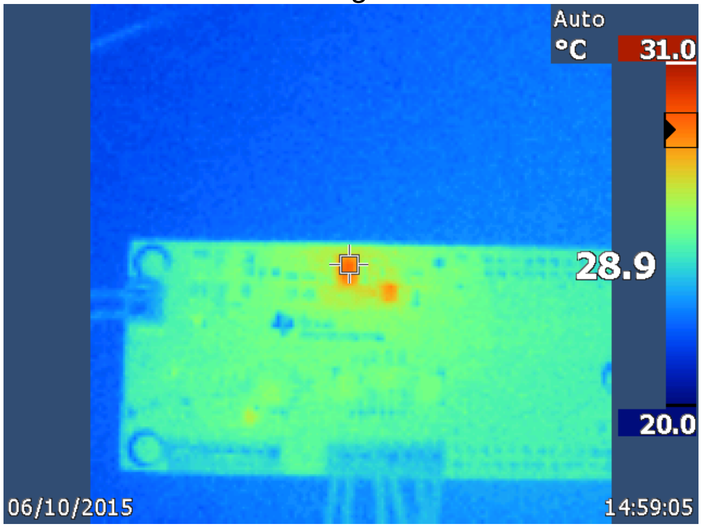


**Figure 34: LM53603 (Wide-VIN Buck) IC, no load, steady state**

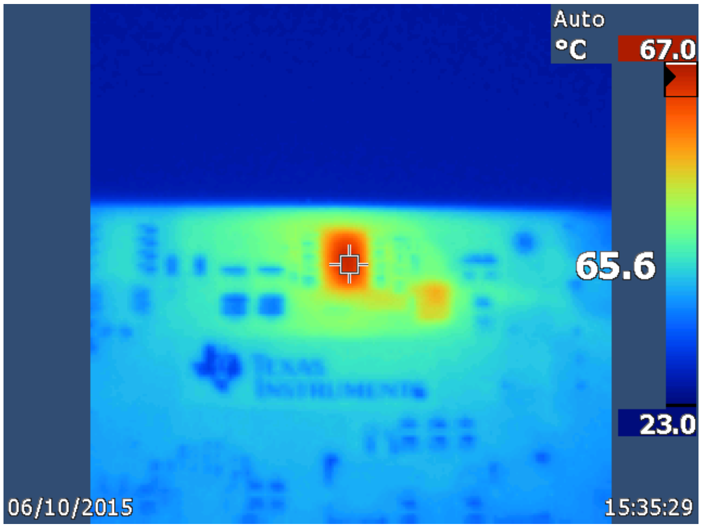


**Figure 35: LM53603 (Wide-VIN Buck) IC, full load, steady state**

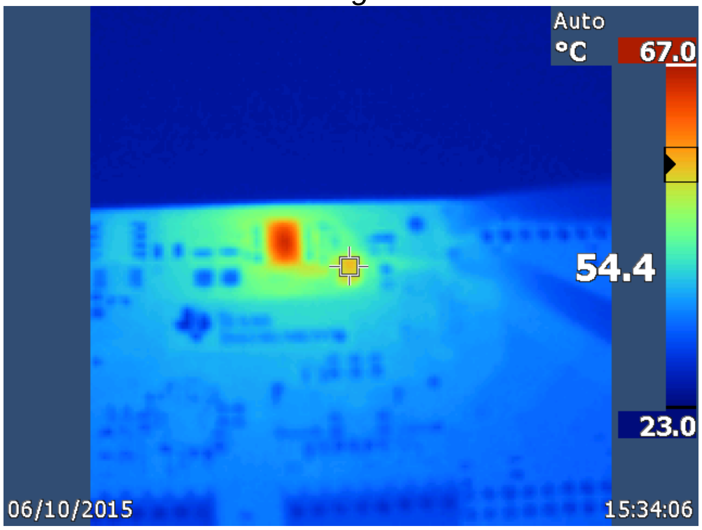


**Figure 36: LM53603 (Wide-VIN Buck) inductor, full load, steady state**

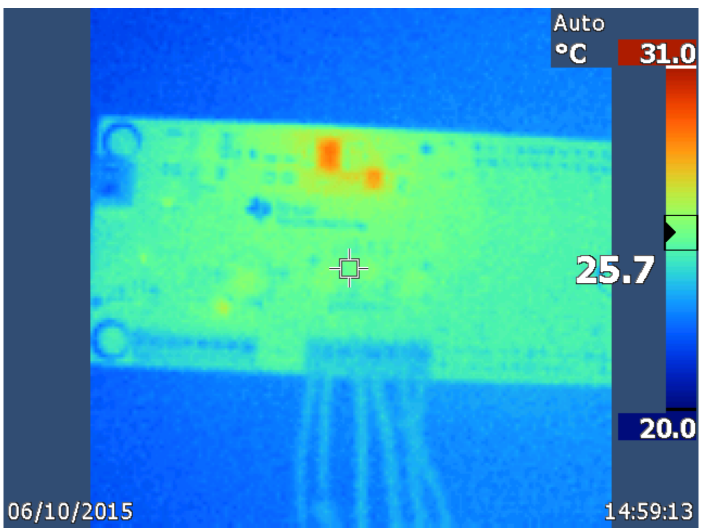


**Figure 37: LP8731 IC, no load, steady state**

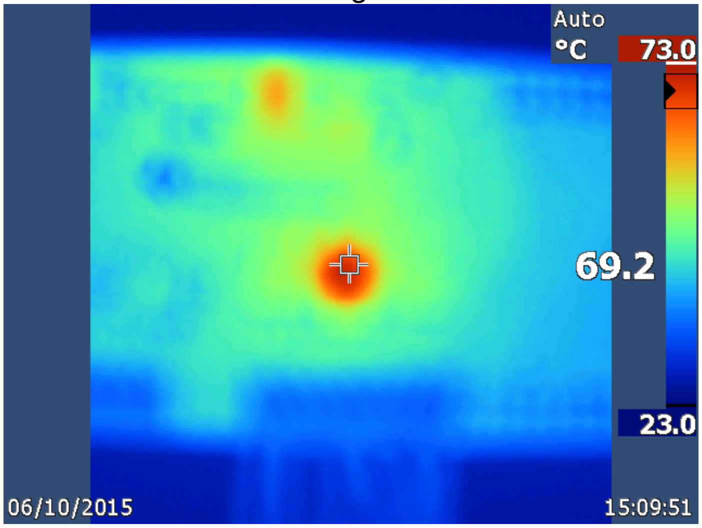


**Figure 38: LP8731 IC, all 4 rails full load, steady state**

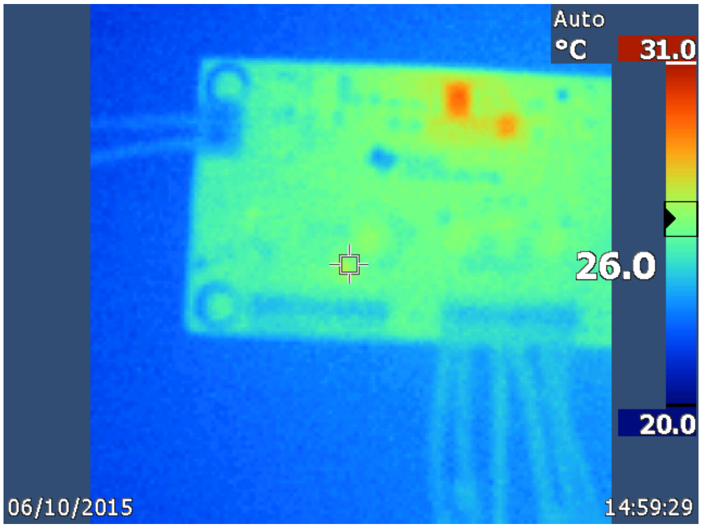


**Figure 39: VDDQ IC, no load, steady state**

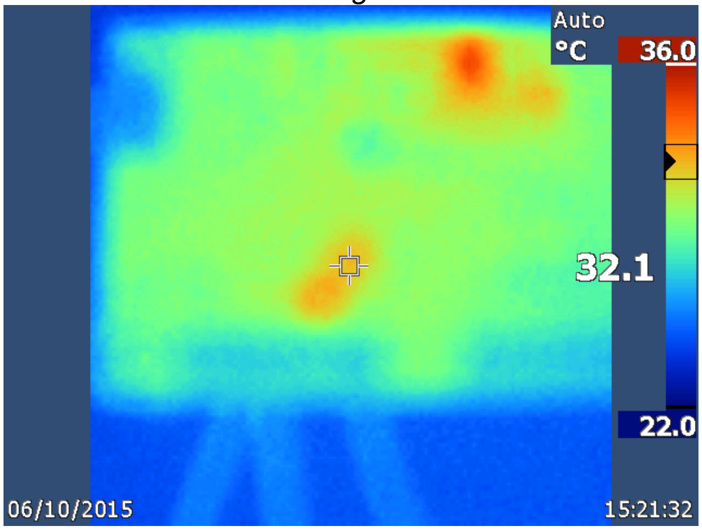


**Figure 40: VDDQ IC, full load, steady state**

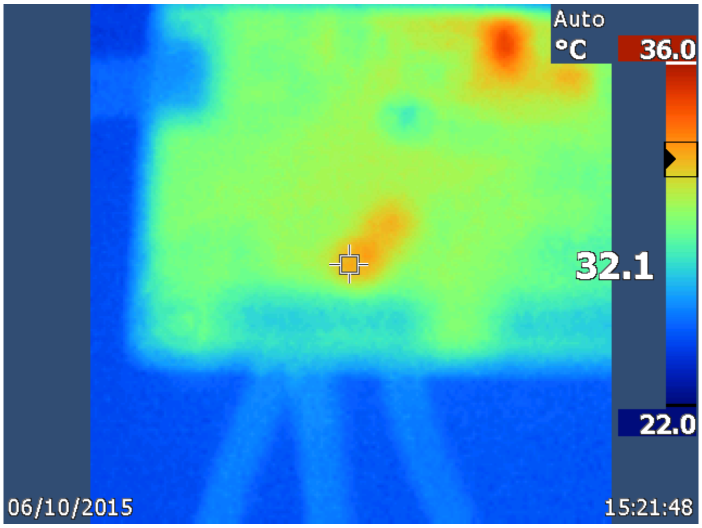


**Figure 41: VDDQ inductor, full load, steady state**

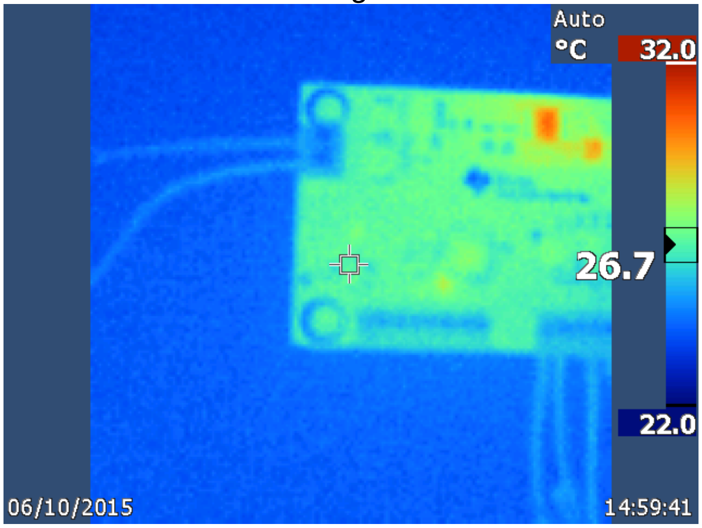


**Figure 42: VCAN IC, no load, steady state**

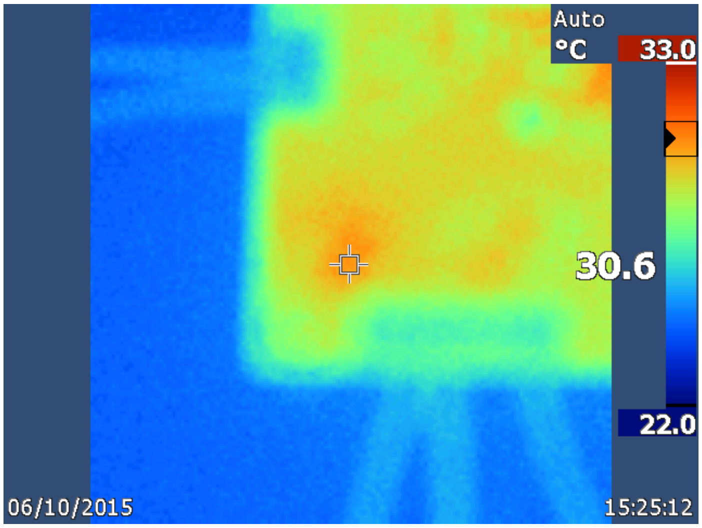


**Figure 43: VCAN IC, full load, steady state**

## *Electrical Transient Testing*

We performed three electrical transient test pulses to verify our transient suppression scheme: ISO 7637-2:2004 Pulse 1, 2a, and 5b (Clamped/Suppressed Load Dump). A battery DC voltage of 13.5V is used for all tests. All yellow traces are pulse inputs, and blue traces are the output of the WVIN buck converter (LM53603).

### 1.1.1 ISO Pulse 1

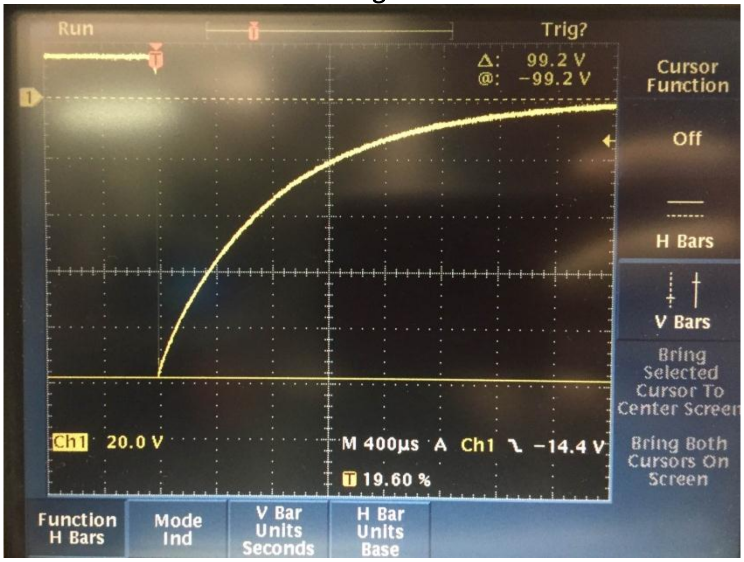


**Figure 44: Pulse 1 test pulse**

The pulse was first verified open-circuit. The following parameters were used:

- $V_{min}$ = -100V (-99.2 achieved)
- $R_{source}$ = 4Ω
- $T_{rise}$ = 1µs
- $T_{duration}$ = 2ms

We then subjected our circuit to the pulse and measured the disturbance to the output of the WVIN buck converter:


**Figure 45: TVS circuit clamps the negative voltage to -20.4V**

Though it is not shown here, the LM74610 disconnects the circuit from the input within a few µs of the pulse, and the output is sustained by the input capacitors until the supply voltage recovers.


**Figure 46: Maximum overshoot is 4.2V which protects downstream circuits**

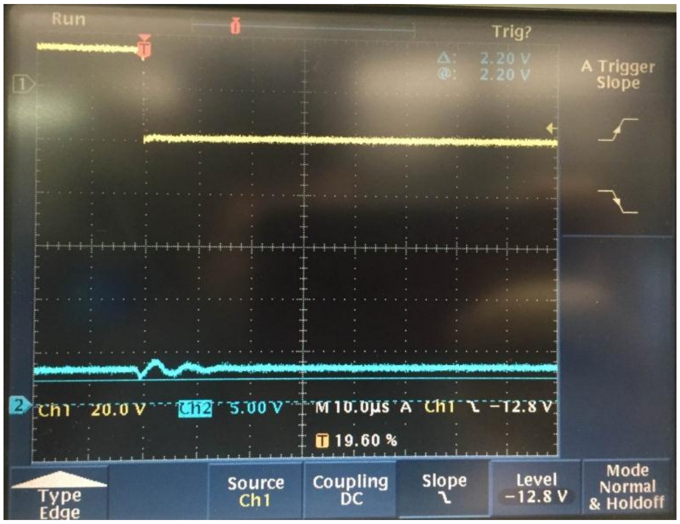


**Figure 47: Maximum undershoot is 2.2V, which may be too low to maintain some downstream converters regulation. Additional hold-up caps can be added to converter inputs to prevent loss of regulation during the pulse**

### 1.1.2 ISO Pulse 2a

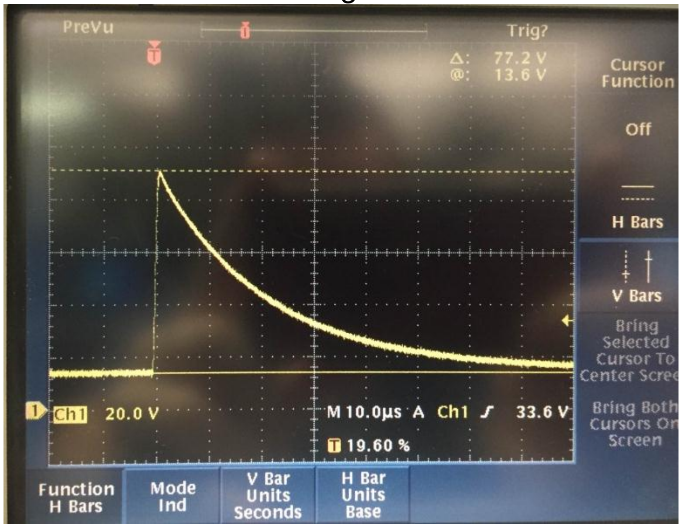


**Figure 48: Pulse 2a test pulse**

The pulse was first verified open-circuit. The following parameters were used:

- $V_{pulse}$ = 75V (77.2V achieved), superimposed on 13.5V DC (so ~90.7V max)
- $R_{source}$ = 4Ω
- $T_{rise}$ = 1µs
- $T_{duration}$ = 50µs

We then subjected our circuit to the pulse and measured the disturbance to the output of the WVIN buck converter:


**Figure 49: TVS circuit clamps voltage to 31.6V**

This is a sufficiently low voltage to protect the downstream WVIN buck converter which has maximum transient voltage standoff of 42V.

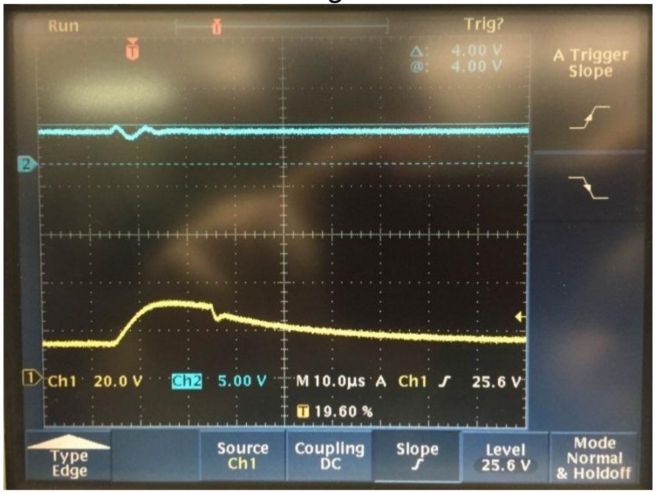


**Figure 50: Maximum overshoot is 4V which is low enough to avoid damage to downstream devices**

Not shown here with markers, but the maximum undershoot is to ~2.5V, which may be too low to maintain some downstream converters regulation. Additional hold-up caps can be added to converter inputs to prevent loss of regulation during the pulse.

### 1.1.3 ISO Pulse 5b (clamped load dump)


**Figure 51: Pulse 5b (clamped load dump) test pulse**

The pulse was first verified open-circuit. The following parameters were used:

- $V_{pulse}$ = 36V (22.5V superimposed on 13.5V DC voltage)
- $R_{source}$ = 0.5Ω
- $T_{rise}$ = 10ms
- $T_{duration}$ = 400ms

We then subjected our circuit to the pulse and measured the disturbance to the output of the WVIN buck converter:

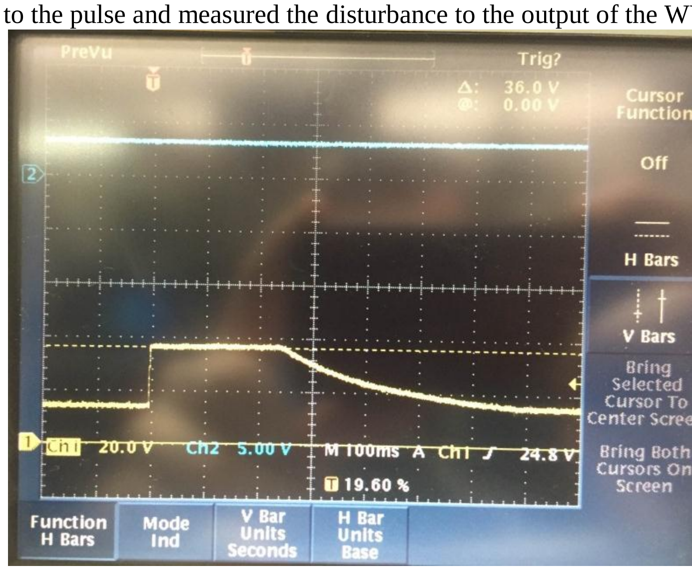


**Figure 52: WVIN output is undisturbed during load dump pulse**

Though the load dump pulse is quite energetic, it is slow enough that it doesn’t cause any significant line transient effects on the output of the LM53603, as the control loop is quick enough to respond to the rising input voltage. The TVS protection circuit also does not need to clamp this pulse as it is low enough in magnitude not to damage downstream devices.

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