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TI Designs – Precision: Verified Design

Headphone Amplifier for Voltage-Output Audio DACs Reference Design

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Design Resources

TIPD189	All Design files
TINA-TI™	SPICE Simulator
OPA1688	Product Folder

Circuit Description

This headphone amplifier circuit converts the output signal from an audio digital-to-analog converter (DAC) into a single-ended signal suitable for headphones. An op amp is configured as a difference amplifier to convert the differential output voltage from a DAC to single-ended. The circuit is designed to operate from 5V bipolar power supplies commonly found in portable devices such as tablets and smartphones.

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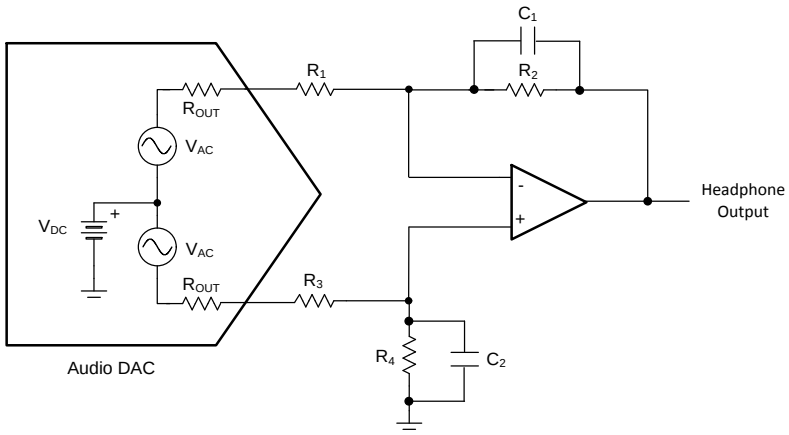

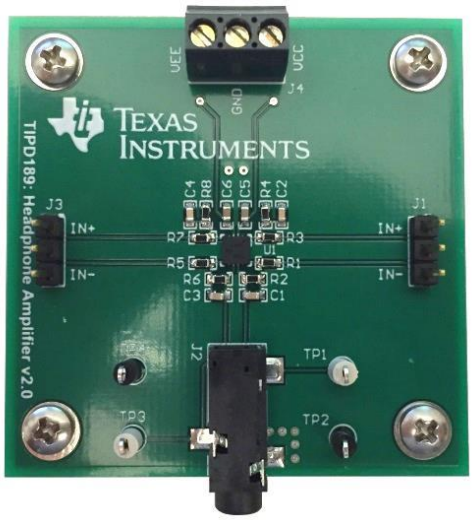

1 Design Summary

The design requirements are as follows:

- Supply Voltage: +/-5 V
- Supply Current: <5mA

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured performance of the design.

Table 1: Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Magnitude Variation (20Hz – 20kHz)	0.01dB	0.009dB	0.003dB
Phase Variation (20Hz – 20kHz)	5.0°	0.927°	-0.563º
THD+N (1kHz, 10mW, 32 Ω load)	-100dB (0.001%)	-104.15dB (0.00062%)	-106.7dB (0.00046%)
Maximum Output Power Before Clipping (32 Ω)	50mW	N/A	55mW
Output Impedance (1kHz)	<0.1Ω	0.00011Ω	0.0317Ω

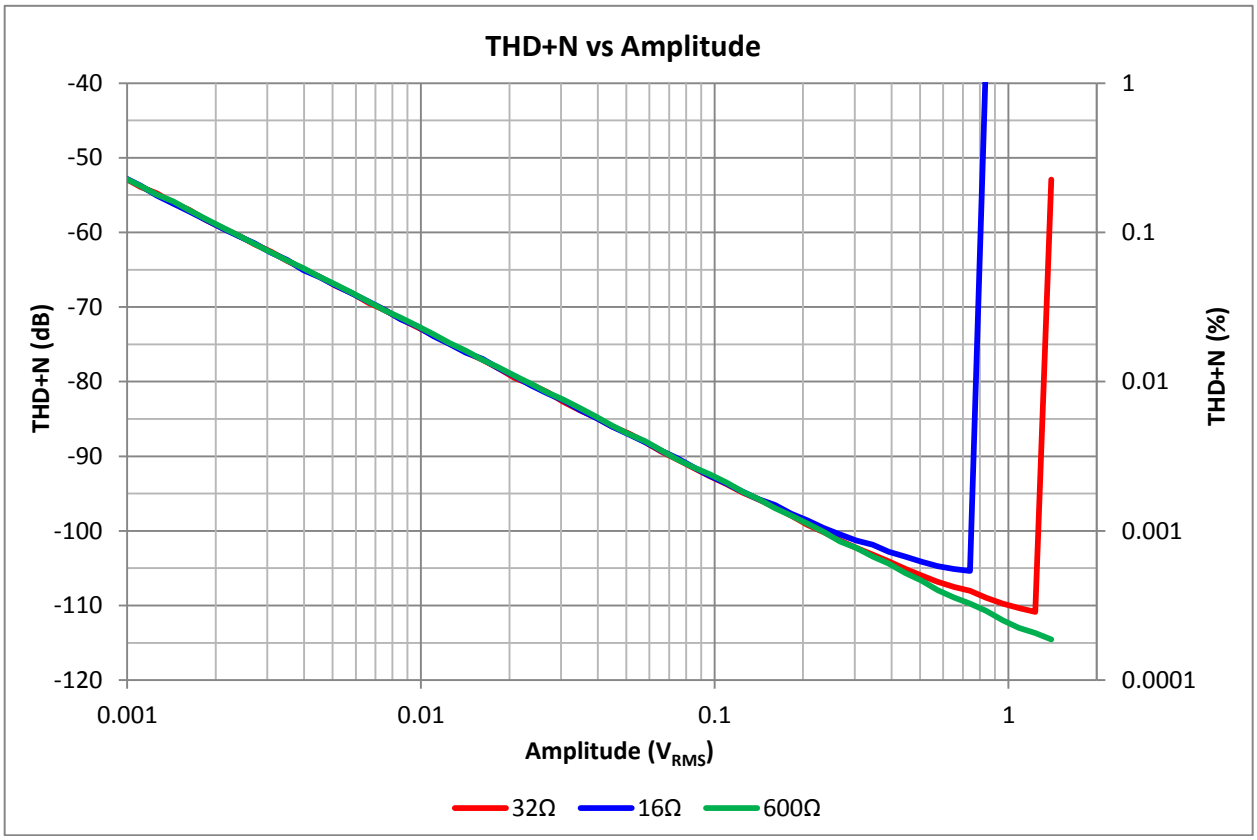

Figure 1: Measured THD+N vs. Output Voltage

2 Theory of Operation

High performance audio DACs may have an output signal which is either a varying current or voltage. Additionally, “current segment” audio DACs may be used as a current output or a voltage output by simply changing the external circuitry used with the DAC. Voltage output configurations require less external circuitry and therefore have advantages in cost, power consumption, and solution size. However, they may offer slightly lower performance than current output configurations. Differential outputs are standard on both types of DACs because it doubles the output signal levels that can be delivered on a single, low-voltage supply, and also allows for even-harmonics common to both outputs to be cancelled by external circuitry. A simplified representation of a voltage-output audio DAC is shown in Figure 2. Two ac voltage sources (V_{AC}) deliver the output signal to the complementary outputs (OUT) through their associated output impedances (R_{OUT}). Both output signals may have a dc component as well, represented by dc voltage source V_{DC}.

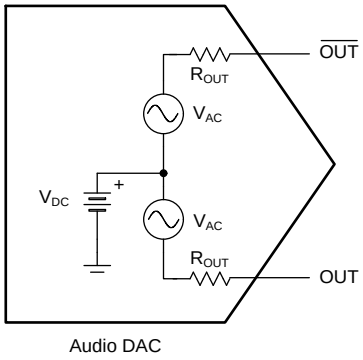

Figure 2: A simplified representation of a voltage output DAC

The headphone amplifier circuit connected to the output of an audio DAC must convert the differential output into a single-ended signal and be capable of producing signals of sufficient amplitude at the headphones to achieve reasonable listening levels. Figure 3 shows a simplified schematic of a circuit which performs this function for voltage output DACs.

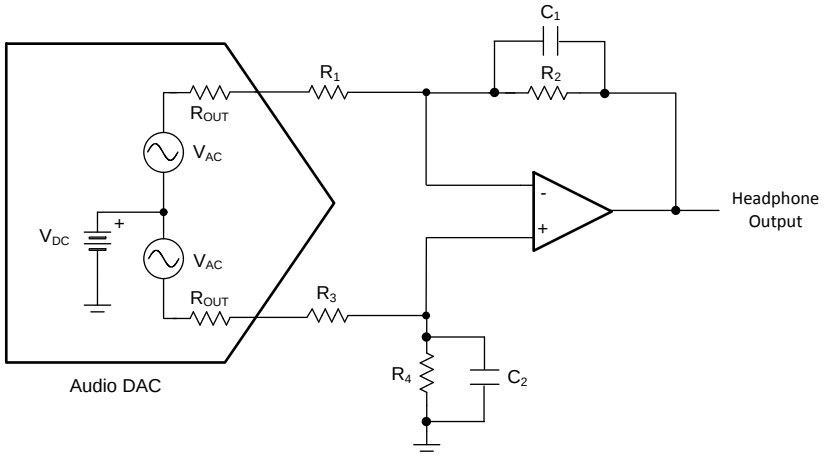

Figure 3: A simplified schematic of a headphone amplifier circuit and audio DAC.

An op amp is configured as a difference amplifier which converts the differential output voltage into a single-ended one. The values of the resistors in the difference amplifier circuit are determined by the specifications of the DAC such as output voltage and output impedance as well as the maximum output voltage desired at the headphone output. The op amp chosen must be capable of delivering the necessary current to the headphones and remain stable into typical headphone loads which may have capacitances as high as 400pF.

2.1 Difference Amplifier Design

The following design process will use a hypothetical DAC with common values of output voltage and impedance for the design process. The specifications of the DAC are shown in Table 2.

Table 2: Audio DAC specifications used for the design process

Parameter	Value
Max. differential output voltage	2 V_{RMS}
Output impedance (R_{OUT})	300 Ω
Output dc offset	1.65V

The gain of the difference amplifier in Figure 3 is determined by the resistor values and includes the output impedance of the DAC. For R2 = R4 and R1 = R3, the output voltage of the headphone amplifier circuit will be:

$$V_{OUT} = V_{DAC} \frac{R_2}{R_1 + R_{OUT}} \quad (1)$$

The output voltage necessary for headphones depends on the headphone impedance as well as the headphone efficiency, which is a measure of the sound pressure level (SPL, measured in dB) for a certain input power level (typically given at 1mW). The headphone SPL at other power levels can be calculated using the efficiency at 1mW:

$$SPL(dB) = \eta + 10\log\left(\frac{P_{IN}}{1mW}\right) \quad (2)$$

Where η is used to denote efficiency, and P_{IN} is the input power to the headphones. Figure 4 shows the input power required to produce certain SPLs for different headphone efficiencies. Typically, over-the-ear style headphones have lower efficiencies than in-ear types with 95dB/mW being a common value.

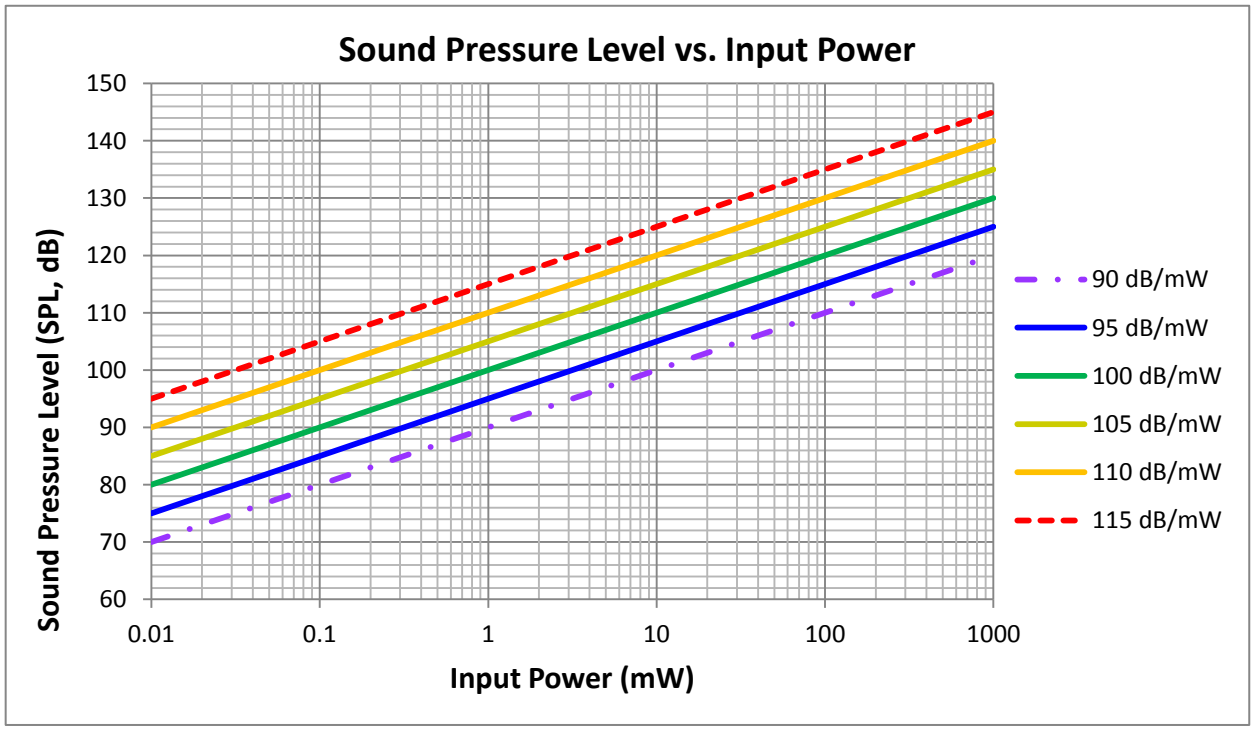

Figure 4: Sound pressure levels vs input power for headphones of varying sensitivity

In-ear headphones may have efficiencies of 115dB/mW or greater and will therefore have much lower power requirements. The output power goal for this design is 50mW which is sufficient power to produce extremely loud sound pressure levels in a wide range of headphones. A 32Ω headphone impedance is used for this requirement because this is a very common value in headphones for portable applications. The voltage required for 32 Ω headphones is therefore:

$$V_O = \sqrt{P \times R} = \sqrt{50mW \times 32\Omega} = 1.265V_{RMS} \quad (3)$$

A tradeoff exists when selecting resistor values for this design. First, high resistor values contribute additional noise to the circuit, degrading the audio performance. However, extremely low resistor values may draw excessive current from the DAC, increasing distortion. A value of 2kΩ was selected for resistors R1 and R3 as a reasonable compromise between these two considerations. Resistor R2 and R4 can then be calculated:

$$V_{OUT} = V_{DAC}\frac{R_2}{R_1 + R_{OUT}} \rightarrow 0.63 = \frac{R_2}{2k\Omega + 300\Omega} \rightarrow R_2 = 1449\Omega \rightarrow 1.47k\Omega \quad (4)$$

The gain of the circuit can be increased to produce greater output voltages in order to accommodate higher impedance headphones. However, this will increase the noise of the circuit, and will also limit the dynamic range of the circuit into lower impedance headphones. For this reason, some designers chose to have the headphone amplifier gain selectable by a switch.

2.2 Capacitor Selection

Capacitors C1 and C2 have a dual role in the headphone amplifier circuit. First, they limit the bandwidth of the circuit to prevent the unnecessary amplification of interfering signals. Second, these capacitors can help to increase the overall stability of the circuit. The maximum value of these capacitors is determined by the limitations on frequency response magnitude and phase deviations detailed in Section 1. C1 and C2 combine with resistors R2 and R4 to form a pole at:

$$f_P = \frac{1}{2\pi(R_2, R_4)(C_1, C_2)} \quad (5)$$

The phase shift at 20 kHz due to this pole should be limited to less than 5°; this allows the pole frequency to be calculated:

$$f_P \geq \frac{f}{\tan(-\theta)} \geq \frac{20kHz}{\tan(5^\circ)} \geq 228.6kHz \quad (6)$$

We must also calculate the minimum pole frequency allowable to meet the magnitude deviation requirements:

$$f_P \geq \frac{f}{\sqrt{\left(\frac{1}{G}\right)^2 - 1}} \geq \frac{20kHz}{\sqrt{\left(\frac{1}{0.999}\right)^2 - 1}} \geq 416.6kHz \quad (7)$$

Where G represents the gain in decimal for a -0.01 dB deviation at 20 kHz, the upper limit for the value of C1 and C2 can be calculated to meet the goals for phase shift and magnitude deviation at 20 kHz.

$$C_1, C_2 \leq \frac{1}{2\pi(R_2, R_4)F_P} \leq \frac{1}{2\pi(1.47k\Omega)(416.6kHz)} \leq 260\,pF \quad (8)$$

This limit defines the value of C1 and C2 in order to meet the goals for magnitude and phase deviation over the passband of the amplifier circuit. However, C1 and C2 also help improve stability of the circuit into capacitive loads such as headphones. Determining the optimum value for these capacitors for stability is best performed in simulation. Please see the stability portion of the simulation section for the final capacitor value.

3 Component Selection

3.1 Resistors

The resistors forming the difference amplifier (R1, R2, R3, and R4) should be precision 0.1% resistors for best performance. Precision resistors maximize the common-mode rejection of the difference amplifier which can reduce dc offset at the headphone output and cancel even harmonic distortion from the DAC. Thin film resistors are also suggested for best audio performance.

3.2 Capacitors

All capacitors that may have a substantial signal voltage across them (C1, C2) must be C0G/NP0 type ceramics. Other types of ceramic capacitors (X7R, X5R, etc.) will produce large amounts of distortion and degrade the performance of the circuit. Please see references [1] and [2] for more information on this effect.

3.3 Amplifier

The basic amplifier requirements are given in Table 3. Additional op amp performance requirements which will impact the audio performance are described in the following sections.

Table 3: Basic op amp requirements

Requirement	Value	Unit
Channels	2	--
Power Supply Voltage	≥10	V
Power Supply Current	≤ 2.5	mA/Ch.

Output Current and Voltage

The most difficult requirement to satisfy in the process of op amp selection is the output current capability. For this design, each op amp channel is required to deliver:

$$P = I^2R \rightarrow I = \sqrt{\frac{50mW}{32\Omega}} = 39.5mA_{RMS} = 55.9mA_P \quad (9)$$

This is a linear output current level, meaning the amplifier is not clipping or limited by its output short circuit current protection. Because short circuit current is often the metric used for sorting op amps by output current capability, an op amp must be selected with a short circuit current much higher than 56mA.

Furthermore the amplifier must be able to deliver this amount of current on the specified power supplies. This gives an output swing requirement of:

$$V_{CC} - V_{OUT(P)} = 5V - \sqrt{2} \times 1.265V_{RMS} = 3.21V \quad (10)$$

This means that the amplifier must be able to produce output voltages within 3.21V of its power supplies while delivering 55.9mAp current.

Noise

The noise of the op amp should be low enough to meet the design goals for total harmonic distortion and noise. To achieve a THD+N of -100dB the total noise of the circuit must be less than:

$$V_{N(RMS)} \le V_f \times 10^{\frac{THD(dB)}{20}} \le 0.566V_{RMS} \times 10^{\frac{-100dB}{20}} \le 5.66\mu V_{RMS} \quad (11)$$

To calculate the input voltage noise of the op amp, the noise gain of the circuit will be calculated as well as the thermal noise contributions of the feedback resistors. Noise gain is always the gain measured from the non-inverting input of the amplifier:

$$G_N = 1 + \frac{R_2}{R_{OUT} + R_1} = 1 + \frac{1.47k\Omega}{300\Omega + 2k\Omega} = 1.639 \quad (12)$$

From a noise perspective, the feedback resistors are in parallel, and the thermal noise contribution is calculated from their equivalent resistance:

$$e_{NR} = \sqrt{4kT_K (R_1, R_3 + R_{OUT}) \,||\, (R_2, R_4)}$$
$$= \sqrt{4(1.381\times10^{-23})(298^\circ K)(2k\Omega + 300\Omega) \,||\, (1.47k\Omega)} = 3.84nV/\sqrt{Hz} \quad (13)$$

Finally, calculating the required input voltage noise of the op amp involves taking the total allowable RMS noise voltage and dividing it by the measurement bandwidth and noise gain. The noise contributions of the feedback resistors are subtracted from that value. These operations are performed in squares and the square root is then taken of the final value because noise sources add as a root sum of squares.

$$e_{N(OA)}{}^2 \le \left(\frac{V_{N(RMS)}}{\sqrt{f_{BW}}\,G_N}\right)^2 - 2e_{NR}{}^2 \le \left(\frac{5.66\mu V_{RMS}}{\sqrt{22kHz}\,(1.639)}\right)^2 - 2\left(3.84nV/\sqrt{Hz}\right)^2 \quad (14)$$
$$e_{N(OA)} \le 22.64nV/\sqrt{Hz}$$

The input voltage noise of the op amp must be less than 22.64nV/√Hz to meet the THD+N goals for this design. This analysis does not include distortion harmonics in the THD+N analysis. Therefore an amplifier should be selected with much lower noise than the calculated value to account for the additional degradation in THD+N caused by the distortion harmonics. Additionally, the current noise of the op amp is not included in this analysis. However, because the source impedance presented to the op amp inputs is fairly low (1.47kΩ || 2.3kΩ = 896.8Ω), current noise was not anticipated to be a significant contributor to the total output noise.

Slew Rate

The slew rate requirements of headphone amplifiers are extremely modest. The slew rate of a sinusoid is given by the equation:

$$SR = 2 \times \pi \times f \times A \quad (15)$$

Where f is the frequency of the waveform and A is the amplitude, the maximum output signal is $1.265V_{RMS}$ or $1.789V_P$. At 20 kHz, the accepted upper end of audibility, the slew rate will be:

$$SR = 2\pi(20kHz)(1.789Vp) = 224.8V/s \rightarrow .2248V/\mu s \quad (16)$$

Consider that for a DAC with a 192 kHz sample rate, the highest output frequency limited by the Nyquist sampling theorem is 96 kHz, which is well above the audio bandwidth. Even at that frequency, the slew rate required is fairly modest:

$$SR = 2\pi(96kHz)(1.789Vp) = 1.08V/\mu s \quad (17)$$

An amplifier with a slew rate 8 to 10 times the maximum signal slew rate is sufficient to assure low distortion.

Amplifier Selection

The OPA1688 was selected for this design because it meets or exceeds all of the calculated performance criteria and is available in an extremely small 8-pin SON package. Table 4 compares the specifications of the OPA1688 to the calculated requirements.

Table 4: Comparison of OPA1688 performance specifications to required values.

Specification	Required Value	OPA1688
Channels	2	2
Power Supply Voltage	≥10V	36V
Power Supply Current	≤ 2.5mA	1.6mA
Output Current	> 56mAp	75mA
Output Voltage (56mA)	3.2V from VCC	2V from VCC
Input Voltage Noise	< 22.6nV/√Hz	8nV/√Hz
Slew Rate	≥8V/µs	8V/µs
Package	N/A	8-SON

4 Simulation

4.1 Stability

The TINA-TI™ schematic used for stability analysis is shown in Figure 5. The feedback loop of the op amp has been broken by inductor LT, and a test signal is injected through capacitor CT. The loop gain of the circuit is measured by the voltage probe labeled: AOLB. The feedback factor is measured by voltage probe B. For the initial stability analysis, capacitors C1 and C2 are removed. A passive component network which closely models the impedance of an actual pair of 32 Ω over-the-ear headphones is connected to the amplifier output.

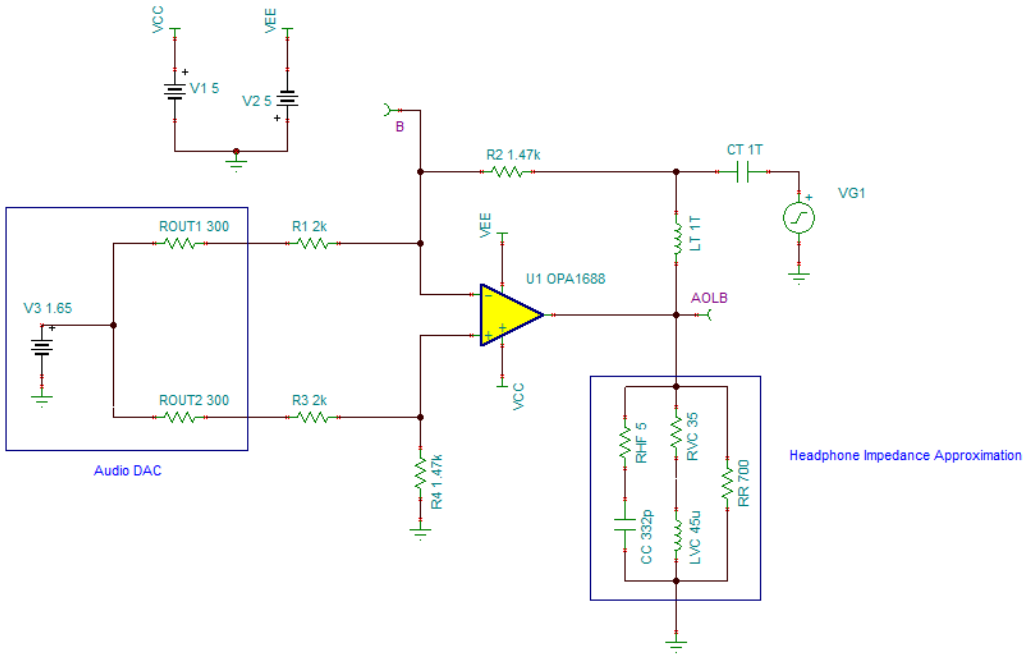

Figure 5: TINA-TI™ simulation schematic to simulate stability. Feedback capacitors are removed for this simulation.

Figure 6 shows the loop gain magnitude and phase response of the circuit. The inverse feedback factor (1/β or noise gain) of the circuit is also plotted by using the post processor in TINA-TI™ to take the inverse of the feedback factor probe. The phase margin of the circuit is measured where the loop gain has decreased to 0dB, in this case at 4.5MHz. Without any feedback capacitors, the circuit has 33° of phase margin with a simulated headphone load connected to the output. A phase margin greater than 45°is a reasonable goal to ensure robust operation of the circuit in all conditions.

From Figure 6 it can be seen that the capacitive loading of the headphones creates a second pole in the loop gain of the amplifier circuit. This second pole degrades the phase margin of the system. The location of the second pole can be determined finding the point in the phase response curve where the phase has decreased from 90° to 45° (about 3MHz). Placing capacitors across the feedback resistors in the difference amplifier circuit produces a pole-zero pair in the 1/β curve. This can help to improve stability because it decreases the rate of closure between the open loop gain and 1/β curves.

The capacitor value will be calculated to produce a pole in the 1/β at the same location as the pole produced in the open loop gain curve: 3 MHz.

$$C_1, C_2 = \frac{1}{2\pi(R_2, R_4)F_P} = \frac{1}{2\pi(1.47k\Omega)(3MHz)} = 36pF \rightarrow 33pF \quad (18)$$

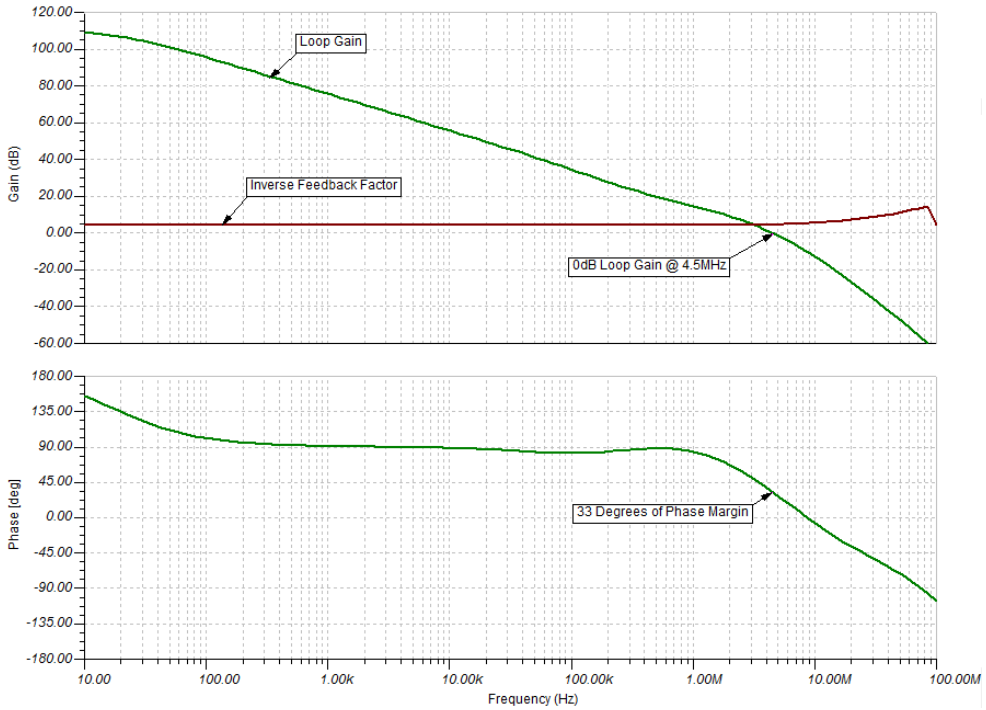

Figure 6: TINA-TI™ simulation result of amplifier circuit without feedback capacitors. The phase margin is 33º

Placing 33pF capacitors across the feedback resistors, as illustrated in Figure 7, gives the simulation results displayed in Figure 8.

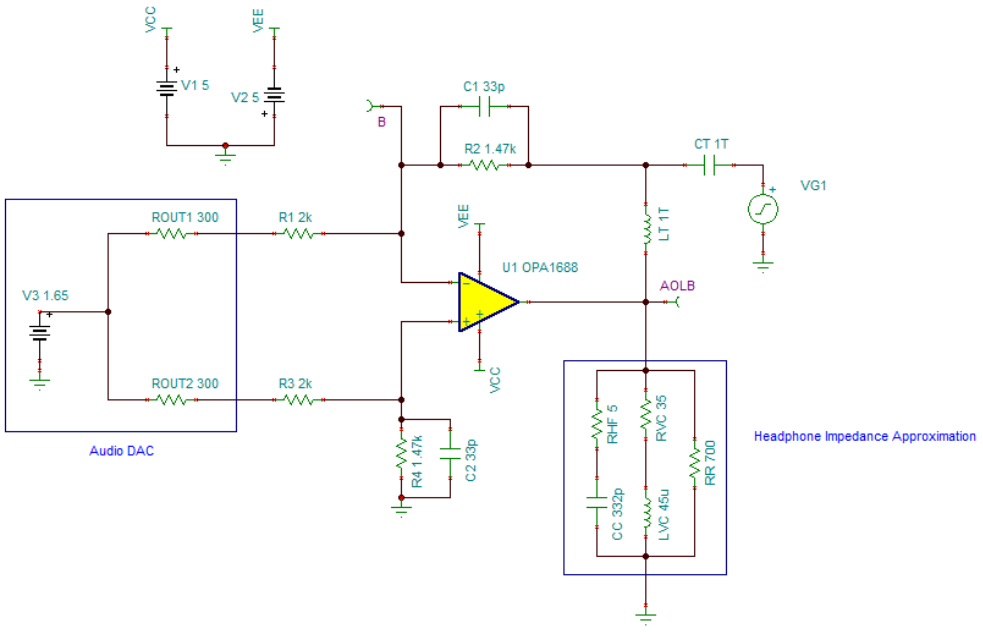

Figure 7: Simulation schematic with 33pF feedback capacitors added.

The effect of the 33pF feedback capacitors can be seen in the slight downward trend of the 1/β curve at high frequencies. The phase margin of the circuit has improved to 51°, indicating a stable design.

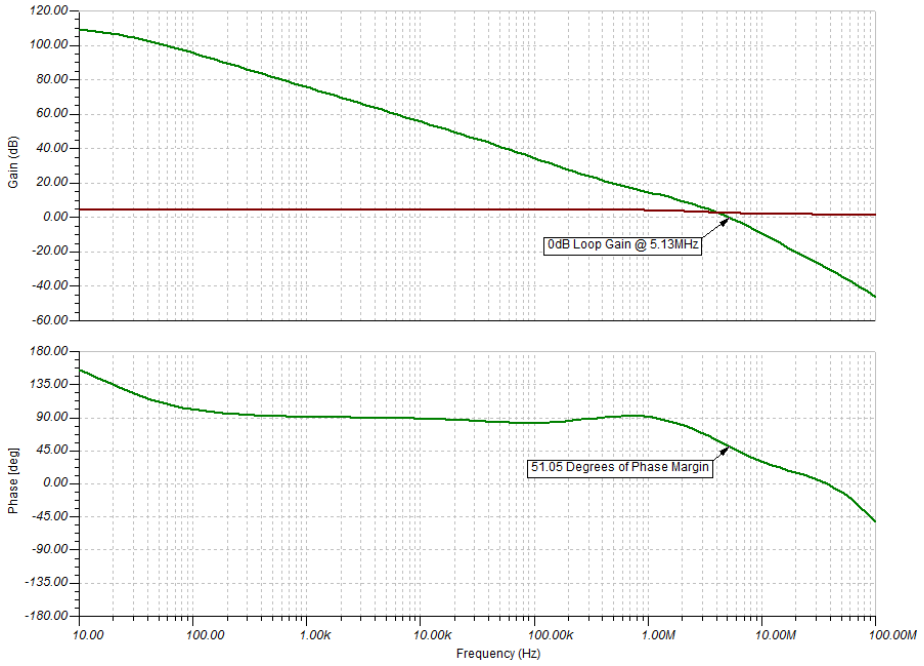

Figure 8: TINA-TI™ simulation results with 33pF feedback capacitors added.

4.2 Transfer Function

The TINA-TI™ schematic used for the transfer function and noise analysis is shown in Figure 9. The audio DAC representation is outlined with a blue box. This model for the audio DAC provides complementary outputs, centered at 1.65V, with the proper output impedance. By using only a single voltage generator, the audio DAC simulation model can be left in-circuit for noise analysis in TINA-TI™.

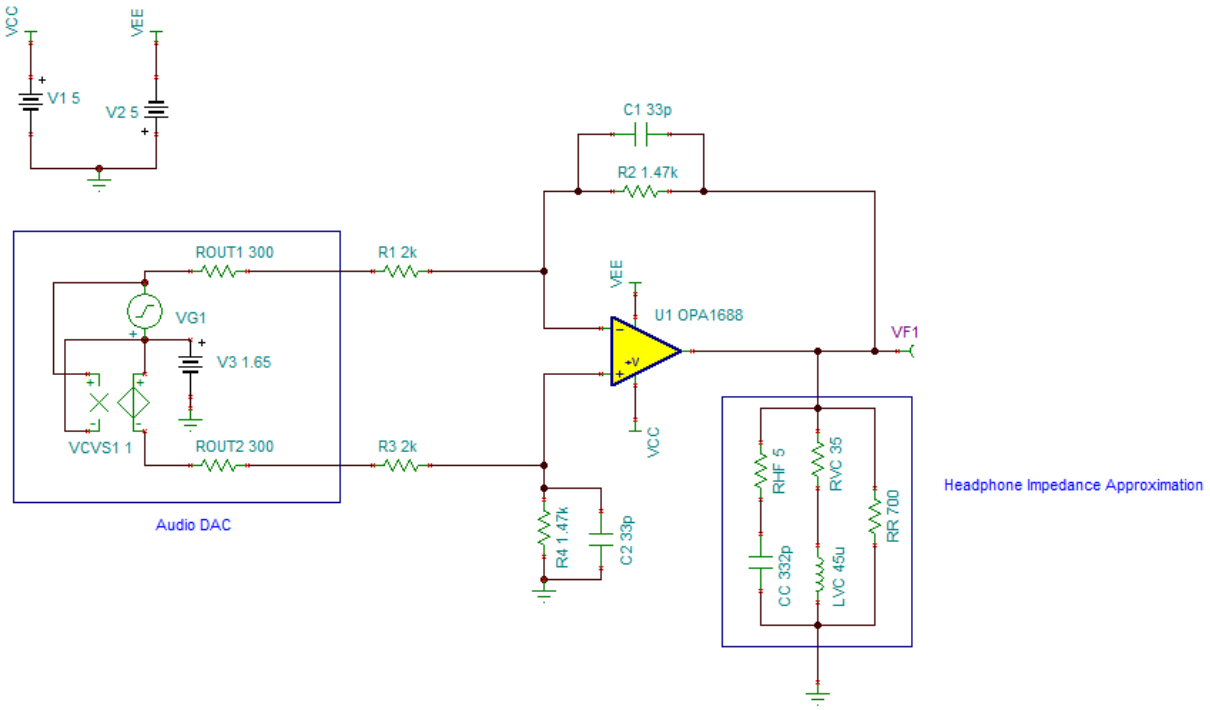

Figure 9: TINA-TI™ simulation schematic for ac transfer characteristic and noise analysis simulations.

Figure 10 shows the magnitude and phase response of the circuit. At 20 kHz, the gain of the circuit has decreased by 0.009dB and the phase has deviated by 0.927°. The absolute value of the gain in this plot is a bit misleading as TINA-TI™ measures gain from the voltage source VG1. The simulated output voltage of the circuit is 1.338 V_{RMS} for a DAC output voltage of $2V_{RMS}$.

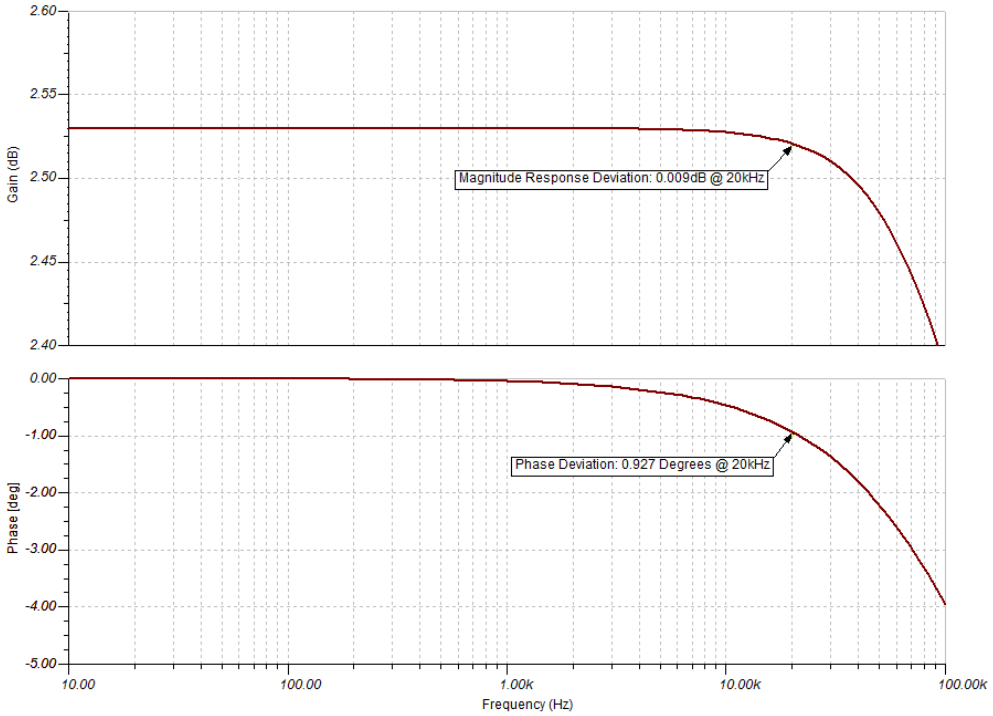

Figure 10: ac Transfer characteristic simulation of the headphone amplifier circuit.

4.3 Noise Analysis

SPICE macromodels do not accurately reflect the distortion performance of most amplifiers. Therefore, the best indication of audio quality offered by simulation is a noise analysis of the circuit. Looking at the equation for total harmonic distortion and noise (THD+N) in decibels shows that this calculation depends heavily on the RMS noise voltage of the circuit (V_N) as well as the amplitude of the fundamental (V_f)

$$THD + N(dB) = 20 \times \log\left(\frac{\sqrt{\sum_{i=2}^{\infty} V_i^{\,2} + V_N^{\,2}}}{V_f^{\,2}}\right) \quad (19)$$

Because the output voltage of headphone amplifiers is typically low, noise is most often the limiting factor in THD+N performance levels. If the contribution of distortion harmonics (V_i) is removed from the THD+N equation, what remains is a simple signal-to-noise (SNR) calculation. Therefore, the signal-to-noise function within the TINA-TI noise analysis can be used to determine the noise limitation to THD+N performance.

Figure 11 plots the SNR of the circuit as the noise bandwidth increases. Taking the value of the curve at 22 kHz (-104.15dB) gives a reasonable approximation of what the measured THD+N will be when measured in that bandwidth.

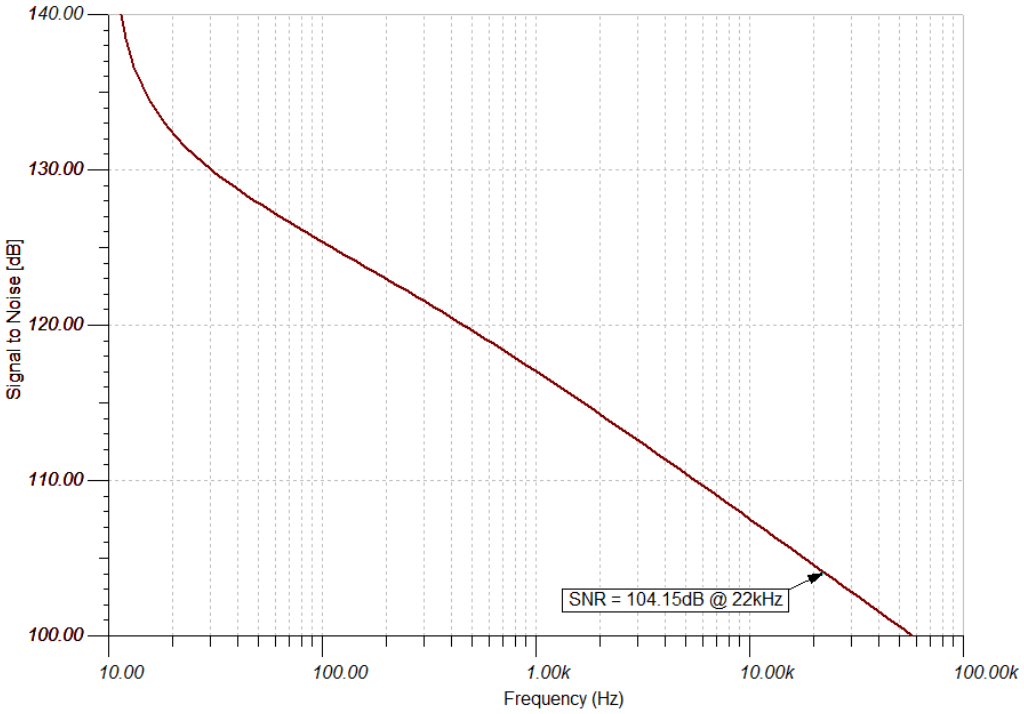

Figure 11: SNR analysis performed in TINA-TI™. The curve shows the SNR as the integration bandwidth increases.

4.4 Output Impedance

The output impedance of a headphone amplifier is a very important parameter because it indicates how the varying impedance of the headphones will affect the frequency response of the amplifier. If the amplifier has a non-zero output impedance, the headphone impedance could cause some frequencies to be artificially attenuated or accentuated [3].

The simulation schematic to measure output impedance is shown in Figure 12. An impedance meter is used for this simulation which is typically only a simulation option in the full licensed version of TINA. However, this circuit will be included in the simulation files of the design document and the impedance meter can be pasted into other schematics.

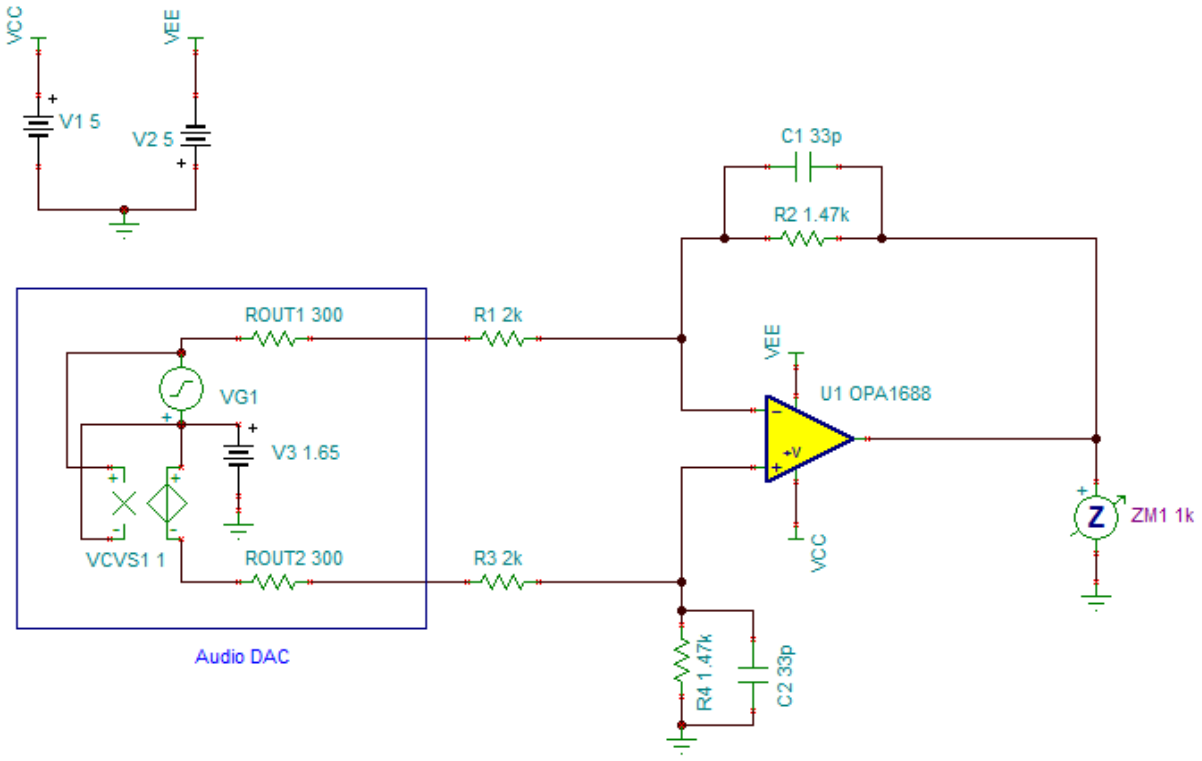

Figure 12: TINA simulation schematic to measure closed-loop output impedance

The simulated closed-loop output impedance is illustrated in Figure 13. At 1 kHz, the output impedance is 110µΩ, but this ignores the effect of parasitic resistances on the PCBs.

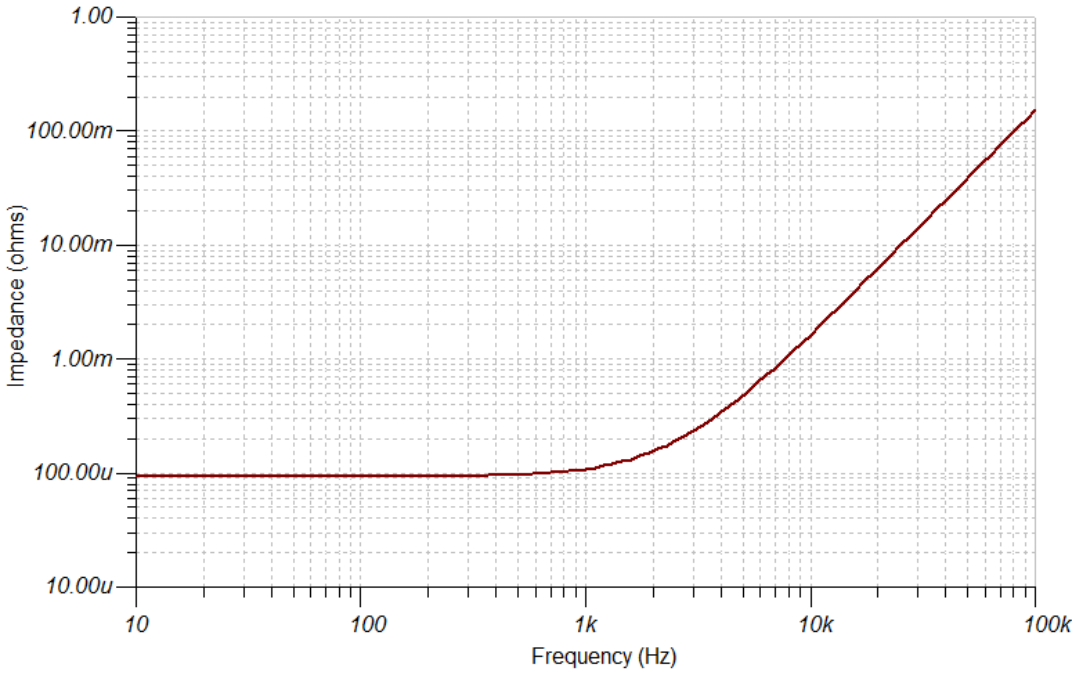

Figure 13: Simulated closed-loop output impedance of the headphone amplifier circuit.

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

The top and bottom layers of the PCB layout are shown in Figure 14. Several aspects of the layout were chosen to ensure optimal audio performance. The unique pinout of the OPA1688 allows for a very efficient placement of all components adjacent to the device. R2 and R6 are placed so that the area of the feedback loop for both channels is as small as possible. The bottom layer of the PCB is almost entirely filled by ground. Vias placed adjacent to the ground terminal on the headphone connector are intended to allow ground currents to return along the bottom of the PCB which is a lower impedance pathway than would be achievable on the top layer. A similar technique is used for the decoupling capacitors C5, and C6 as well as the grounded components in the difference amplifiers (C2, C4, R4, and R8). The input traces for the difference amplifiers are routed as differential signal pairs in an attempt to ensure common-mode noise is rejected by the difference amplifier circuit.

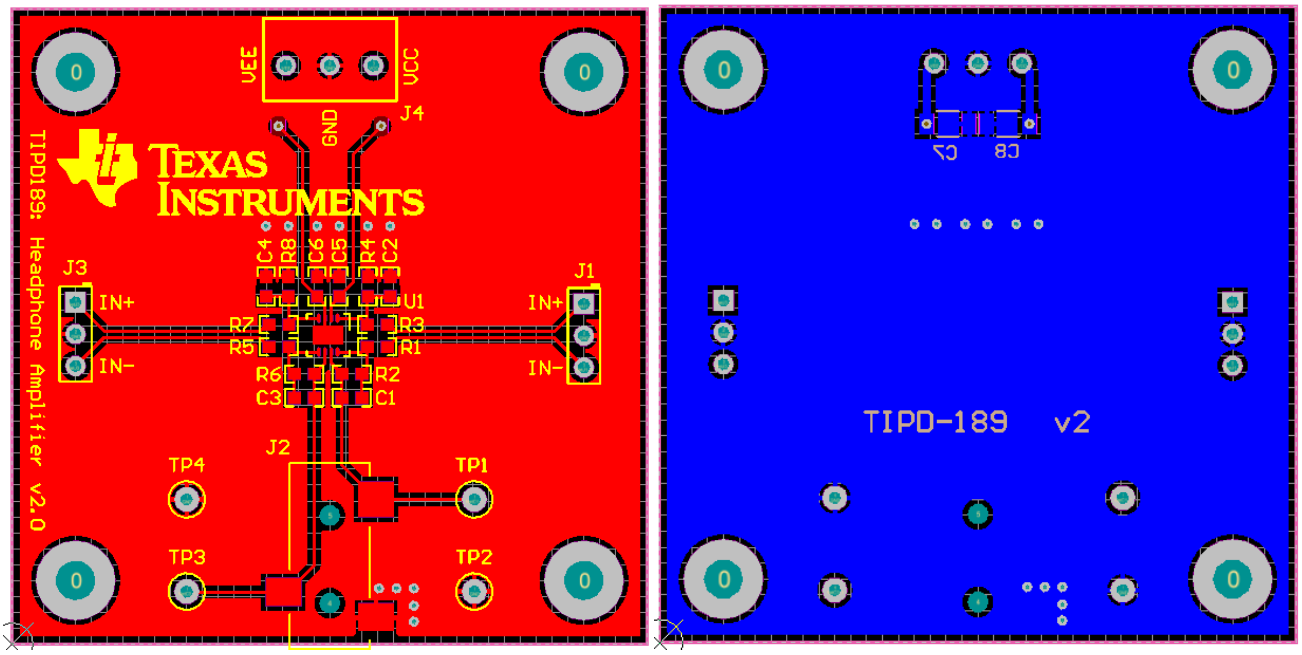

Figure 14: Top layer (red, left) and bottom layer (blue, right) of PCB layout.

6 Verification & Measured Performance

The test setup used to verify the performance of the headphone amplifier is shown in Figure 15. The balanced output of an audio analyzer is used to represent the audio DAC. Because the audio analyzer has an output impedance of 200Ω, the values of R1 and R3 were increased to 2.1kΩ to match the designed value for gain. A load resistor was attached to the output of the amplifier to simulate the headphone loading on the amplifier circuit. Finally, a bench power supply was used to power the circuit during testing. This testing does not include the additional noise and distortion contributed by real-world audio DACs or the switching power supplies commonly used in portable devices.

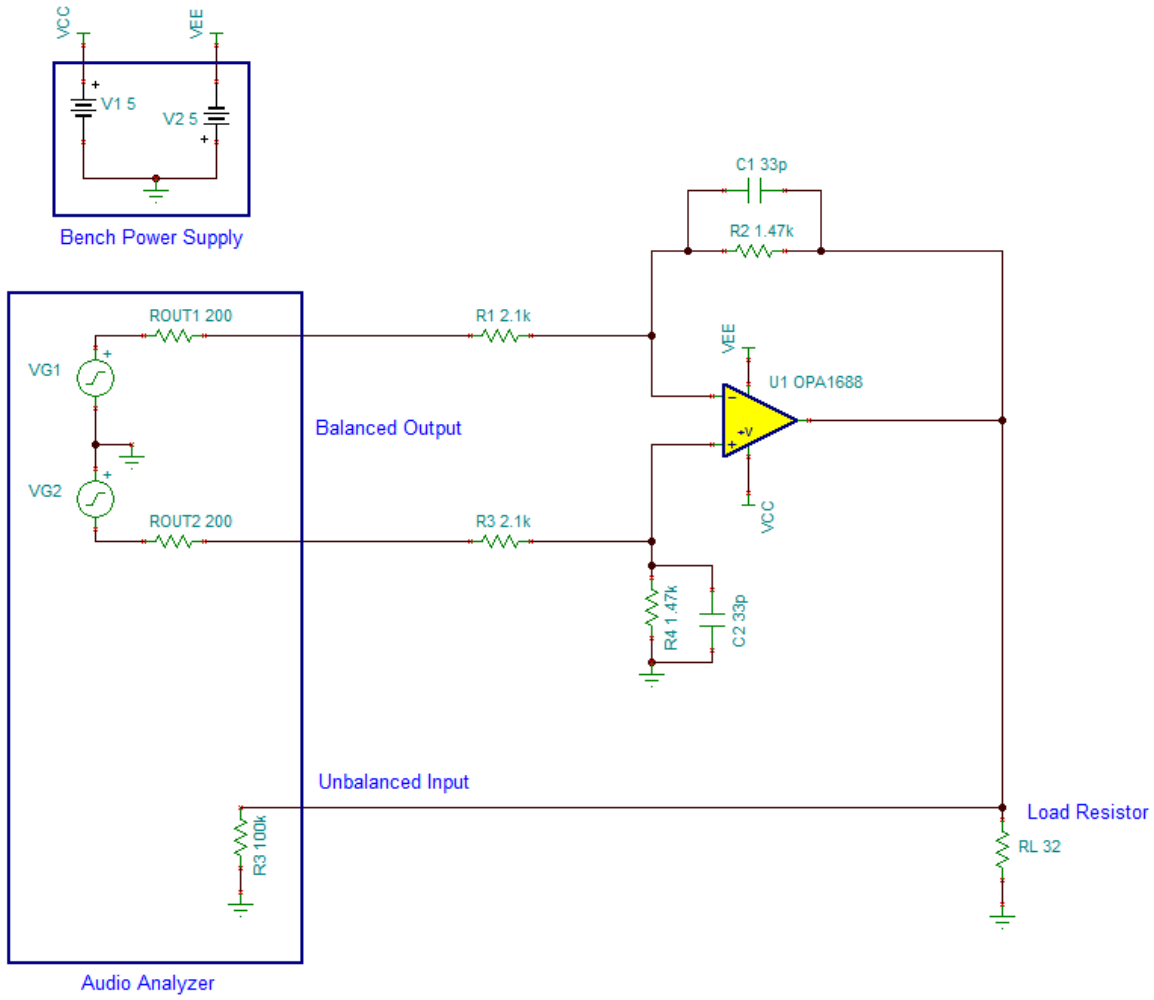

Figure 15: The test setup used to verify the performance of the headphone amplifier circuit.

6.1 Transfer Function

The magnitude response of the headphone amplifier circuit is shown in Figure 16 for two loading conditions. The green curve is an unloaded condition, while the red curve is the frequency response for a 16.2Ω load. The difference in gain for the two loading conditions allows the closed loop output impedance of the circuit to be calculated (displayed by the dashed blue curve). The gain at 1 kHz is selected as the value of nominal gain as this frequency is within the flat passband portion of the circuit and also above low-frequency variations caused by mains interference. The gain at 1 kHz in the unloaded case is -3.502dB, indicating an output of 1.336 V_{RMS} for an input differential voltage of 2 V_{RMS}. At 20 kHz the gain of the circuit has fallen to -3.505dB, for a magnitude deviation of -0.003dB over the passband.

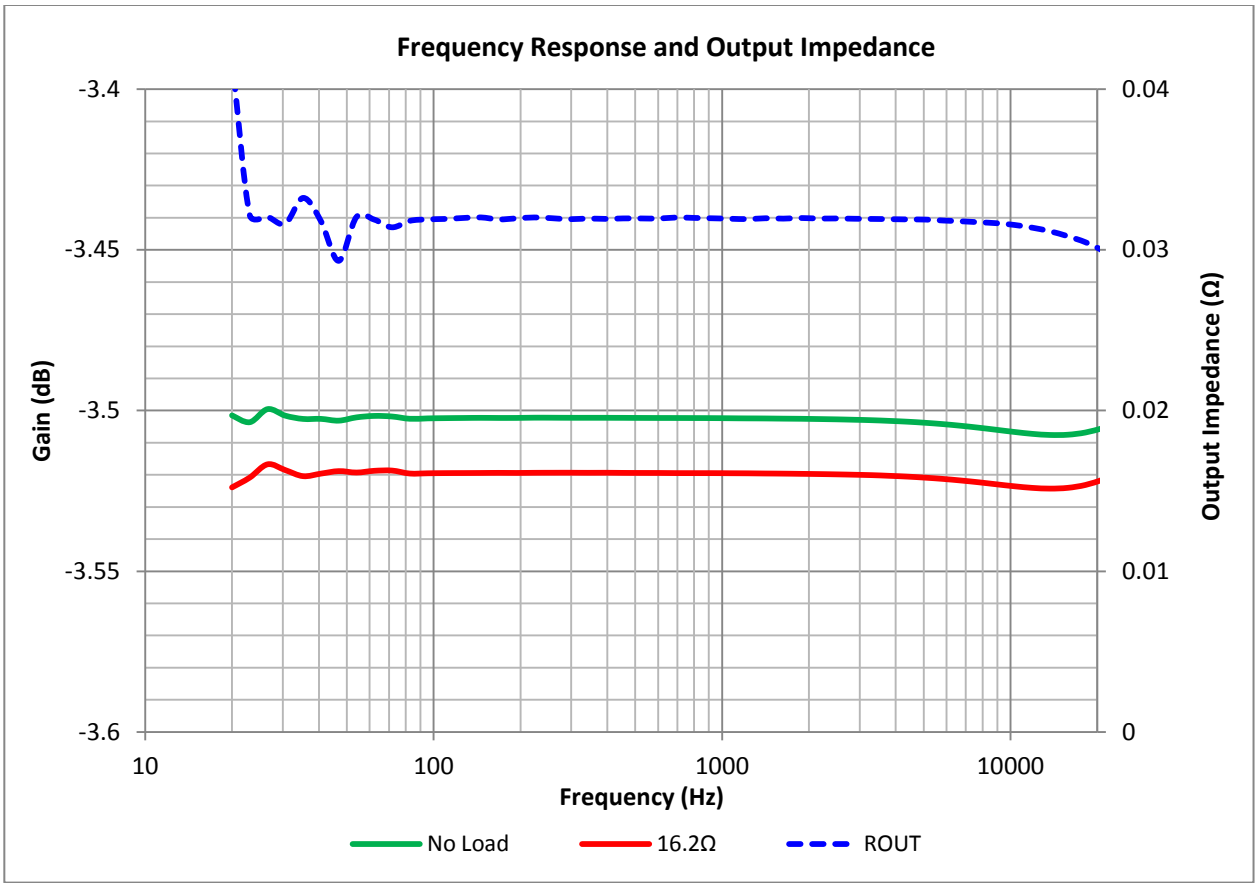

Figure 16: Frequency response of the amplifier circuit in unloaded (green) and loaded (16.2Ω, red) conditions. The calculated closed loop output impedance of the circuit is also shown (blue, dashed).

With a load resistor of 16.2Ω added to the output, the gain at 1 kHz drops to -3.519dB, a decrease of -0.017 dB. The closed loop output impedance forms a voltage divider with the load; therefore the closed loop output impedance can be calculated:

$$\frac{A_{(16.2\Omega)}}{A_{NL}} = 10^{\left(\frac{A_{16.2\Omega(dB)} - A_{NL(dB)}}{20}\right)} = 10^{\left(\frac{-3.519-(-3.502)}{20}\right)} = 0.998$$

$$= \frac{R_L}{R_{OUT} + R_L} \rightarrow R_{OUT} = \left(\frac{16.2\Omega}{0.998}\right) - 16.2\Omega = 0.0317\Omega \quad (20)$$

In the above equation, A denotes the circuit gain (loading condition given in subscript), R_L is the load resistor and R_{OUT} is the closed loop output impedance of the circuit. The calculated output impedance is within the project goals, but above the simulated value due to the contributions of solder joints, PCB traces and contact impedance of the headphone connector.

The phase response of the circuit is shown in Figure 17. The deviation in phase at 20 kHz is -0.563º from the nominal value at 20Hz (0º reference).

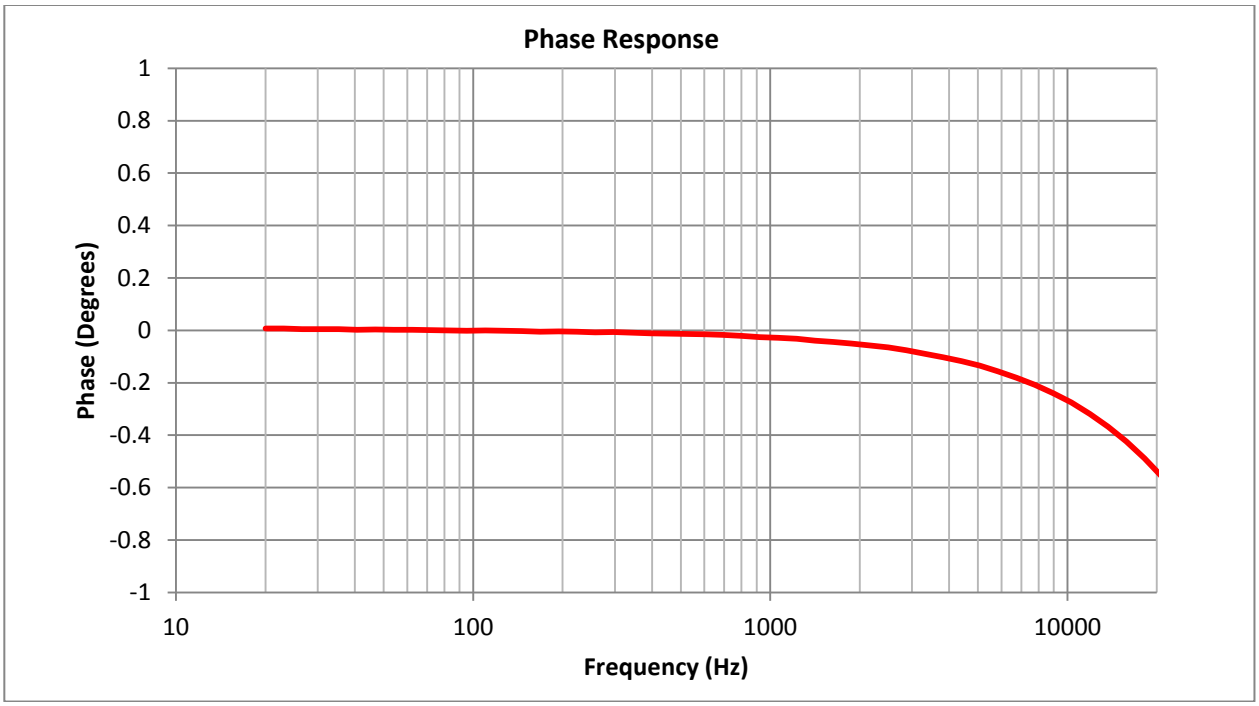

Figure 17: Phase response of the headphone amplifier circuit.

6.2 Audio Performance

Figure 18 through Figure 21 illustrate the excellent audio performance of this headphone amplifier. In Figure 18 the THD+N of the circuit is measured for a 1 kHz signal (22 kHz measurement bandwidth) for increasing output voltages into 3 common headphone loads.

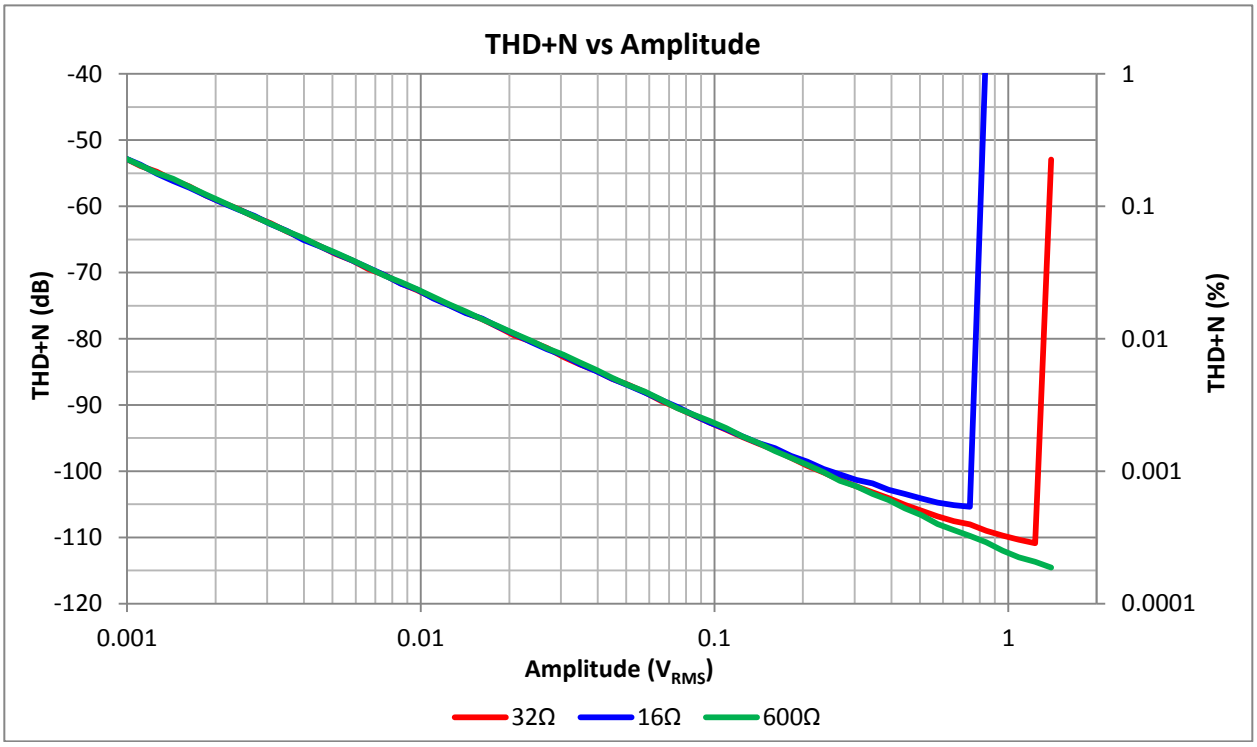

Figure 18: THD+N vs Output Voltage for 3 common headphone loads measured in a 22 kHz bandwidth, 1 kHz fundamental.

The maximum power levels achieved for each load before clipping and the THD+N at that power level is summarized in Table 5. It is important to note that the maximum output voltage level into a 600 Ω load is limited by the maximum output voltage of the hypothetical DAC used (2 V_{RMS}) while the other two loads are limited by the maximum output current the amplifier is able to deliver.

Table 5: Maximum output levels and THD+N before clipping.

Load	Max Output Before Clipping (V_{RMS})	Max Output Before Clipping (mW)	THD+N at Max Output (dB)
16Ω	0.741	33.89	-105.3 (0.00054%)
32Ω	1.34	55.42	-110.2 (0.00031%)
600Ω	1.38	3.17	-114.2 (0.0002%)

Figure 19 shows the THD+N for the same 3 loading conditions measured for frequencies from 20Hz to 20 kHz (500mV_{RMS} amplitude). A 90 kHz measurement bandwidth is used for this measurement to include harmonics of signals above 10 kHz. Increasing the measurement bandwidth also has the effect of increasing the RMS noise voltage included in the THD+N calculation, which will reduce the THD+N values compared to Figure 18.

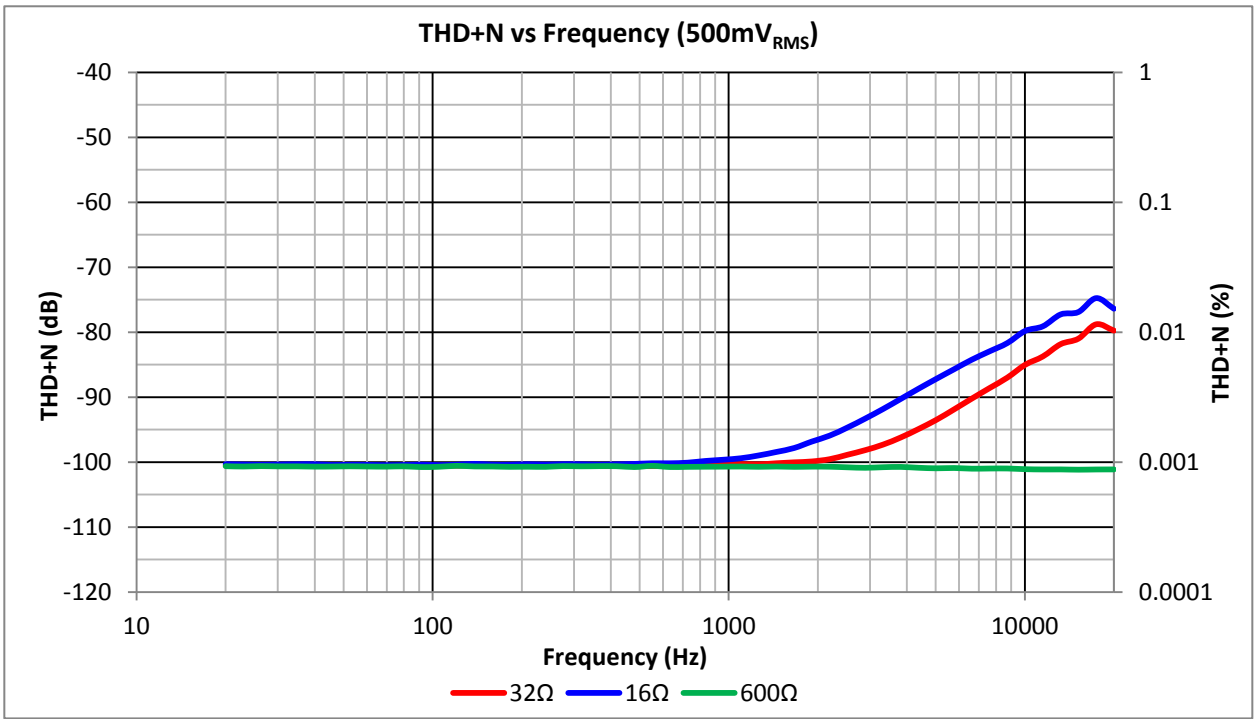

Figure 19: THD+N vs Frequency for a 500mV_{RMS}

Low impedance loads produce additional distortion because the output transistors of the op amp are required to deliver more current and therefore operate in a less linear fashion. At low frequencies this additional distortion is corrected by the loop gain of the op amp, and the THD+N measurement is still dominated by the noise of the circuit. However, as the loop gain of the amplifier decreases at high frequency, the additional distortion rises above the noise. This is why the THD+N progressively degrades at high frequency. The 600Ω load does not draw substantial current at a 500mV_{RMS} signal level, and does not show additional distortion at high frequency.

Figure 20 and Figure 21 are FFTs of the output signal for a 1 kHz fundamental under different output power conditions. In both cases the distortion harmonics are almost 120dB below the fundamental level which is extremely good performance.

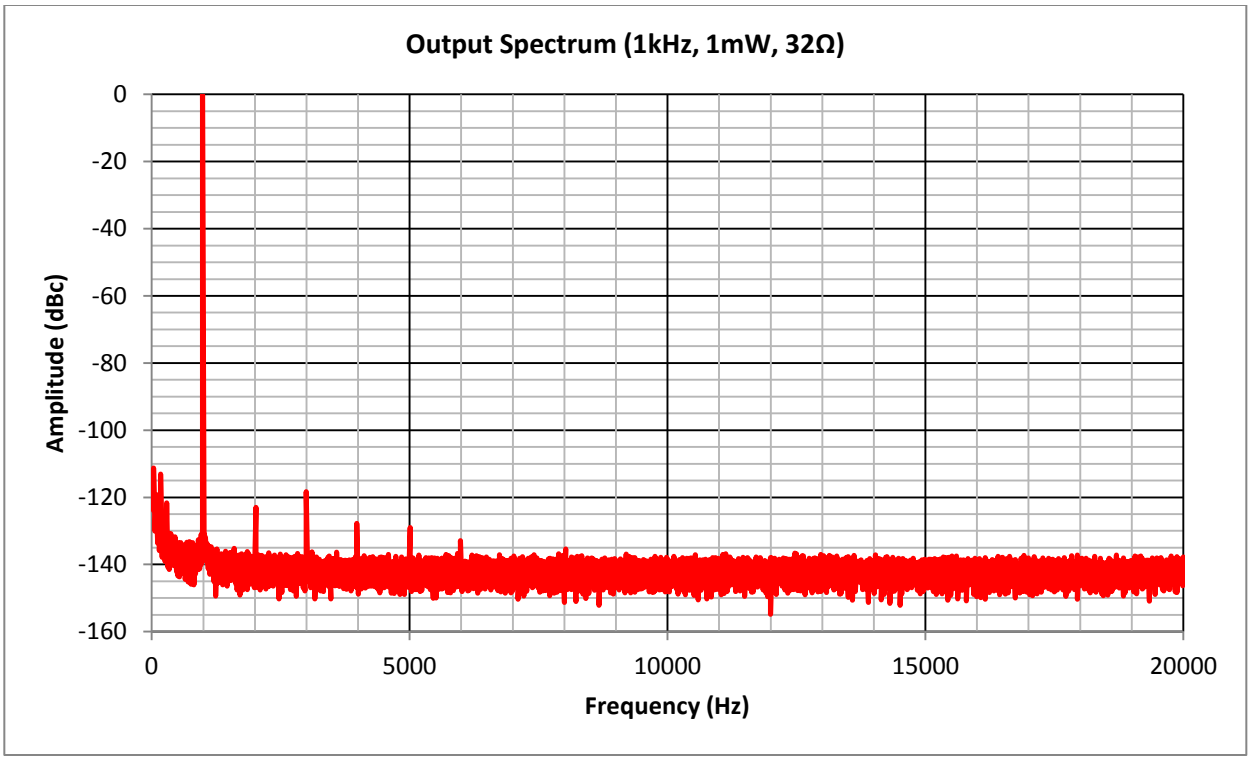

Figure 20: FFT of the amplifier output delivering 1mW into a 32Ω load (1 kHz fundamental). The dominant harmonic is the 3rd at -118.3dBc.

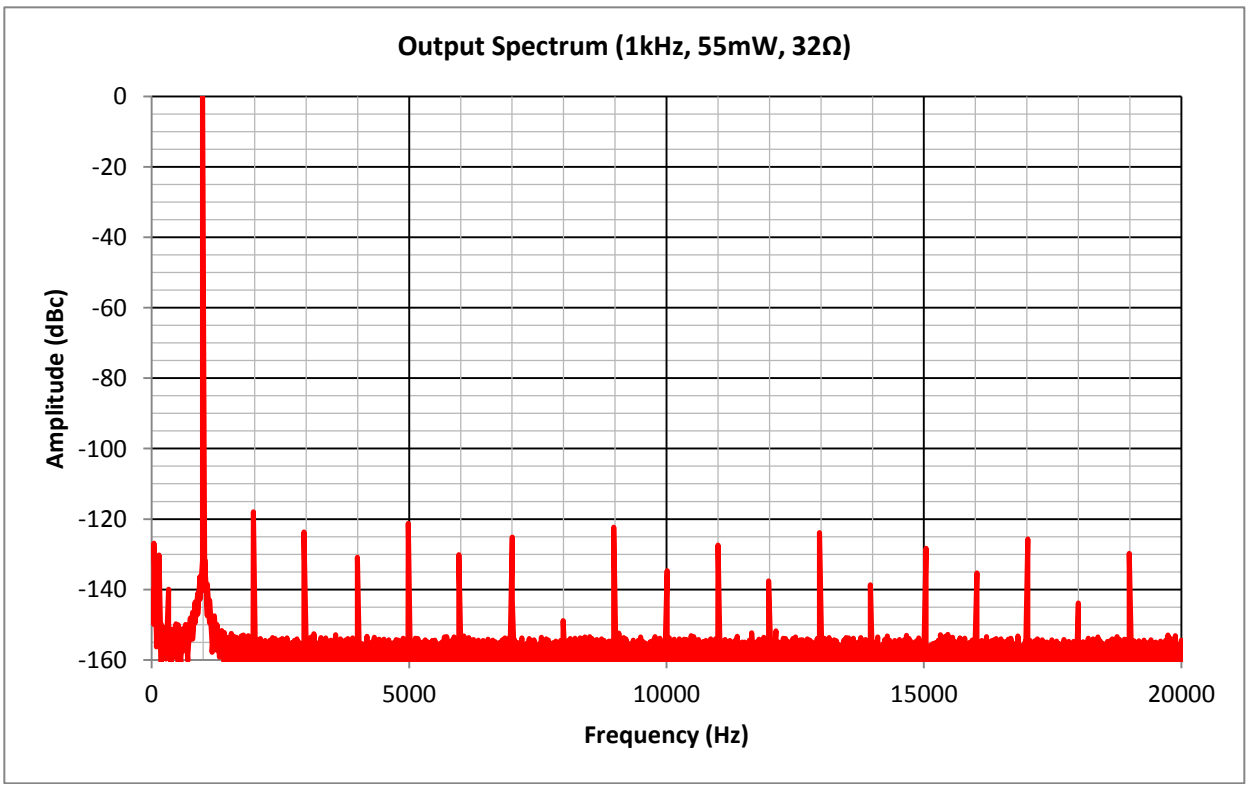

Figure 21: FFT of the amplifier output for a 55mW output level into a 32Ω load (1 kHz fundamental) immediately below the onset of clipping. The dominant harmonic is the 2nd at -118dBc.

7 Modifications

The number of devices which meet the power supply current, output power, and package size requirements for this project are extremely limited. Therefore it is not possible to modify the amplifier selected without making some sort of compromise on performance. For example, the OPA1612 is a low noise audio amplifier available in a DFN package. Although it has lower noise than the OPA1688, which will improve audio quality at lower listening levels, it is not capable of the same amount of output power and consumes more power supply current, potentially decreasing battery life.

An alternative modification would be to increase the gain of the circuit to accommodate 600Ω headphones. The maximum power the circuit is currently able to deliver into 600Ω headphones is limited by the maximum output voltage ($1.38V_{RMS}$). By increasing the gain of the difference amplifier, this would increase the amount of power available for 600Ω headphones, potentially improving the listening experience for those products.

8 About the Author

John Caldwell is a systems engineer with Texas Instruments Precision Analog, supporting audio operational amplifiers. He specializes in low distortion design for analog audio hardware, low-noise design and measurement, and electromagnetic interference issues. He received his MSEE and BSEE from Virginia Tech with a research focus on biomedical electronics and instrumentation. Prior to joining TI in 2010, John worked at Danaher Motion and Ball Aerospace.

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3. *J. Caldwell (2015, April). Stabilizing Difference Amplifiers for Headphone Applications: http://www.ti.com/lit/an/slyt630/slyt630.pdf*

Appendix A.

A.1 Electrical Schematic

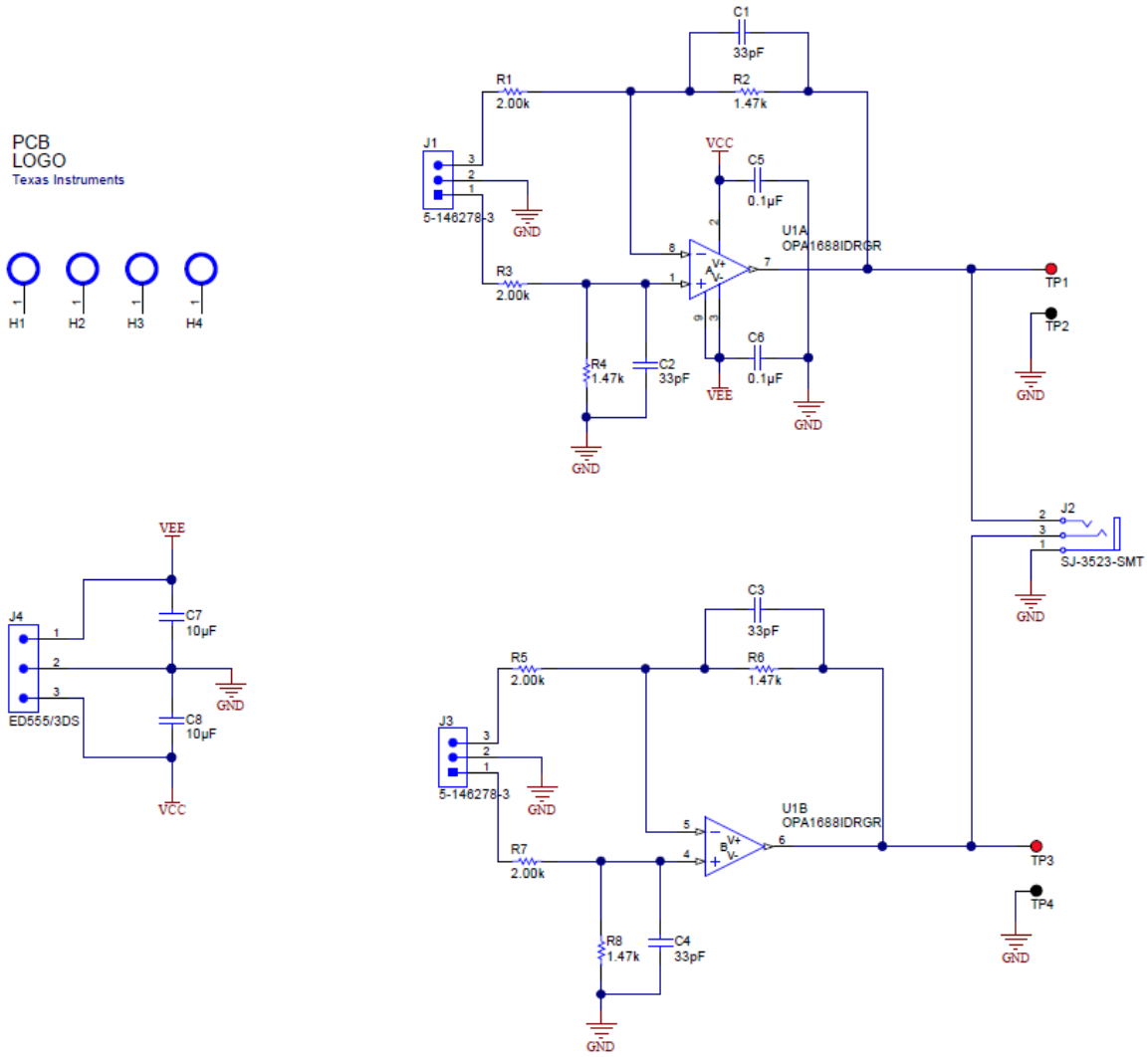

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item	Qty	Value	Designator	Description	Manufacturer	Part Number
1	4	33pF	C1, C2, C3, C4	CAP, CERM, 33pF, 100V, +/-5%, C0G/NP0, 0603	AVX	06031A330JAT2A
2	2	0.1uF	C5, C6	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A
3	2	10uF	C7, C8	CAP, CERM, 10uF, 50V, +/-10%, X5R, 1206_190	TDK	CGA5L3X5R1H106K160AB
4	2		J1, J3	Header, 100mil, 3x1, Tin, TH	TE Connectivity	5-146278-3
5	1		J2	Connector, Audio Jack, 3.5mm, Stereo, SMD	CUI Inc.	SJ-3523-SMT
6	1		J4	ED555/3DS	On Shore Technology Inc	ED555/3DS
7	4	2.00k	R1, R3, R5, R7	RES, 2.00k ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD072KL
8	4	1.47k	R2, R4, R6, R8	RES, 1.47k ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD071K47L
9	2	Red	TP1, TP3	Test Point, Miniature, Red, TH	Keystone	5000
10	2	Black	TP2, TP4	Test Point, Miniature, Black, TH	Keystone	5001
11	1		U1	36V, 10MHz, Low Distortion High Drive Audio Op Amp	Texas Instruments	OPA1688IDRGR

Figure A-2: Bill of Materials

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