TI Designs

EnDat 2.2 System Reference Design

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Design Resources

TIDEP0050	Tool Folder Containing Design Files
Sitara Processors	Product Folder
AM437x ISDK	Product Folder

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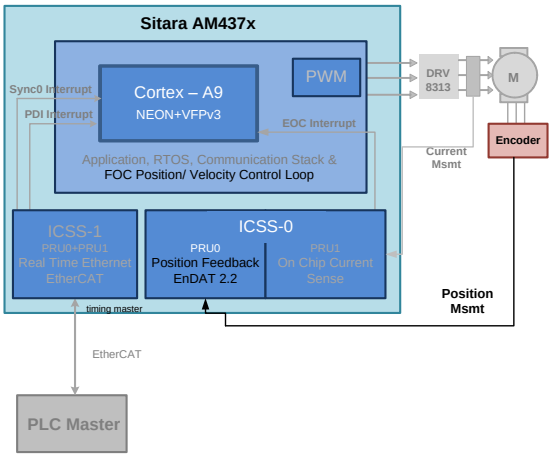
Design Features

- Enables Developers to Use EnDat 2.2 Encoder Interlaces to Implement a Low Foot Print, Low-Power Single-Chip Solutions in Applications Such as Industrial Automation and Factory Automation.
- Provides an Interface That is the Technical Standard for Direct Drive Technology Thanks to its High-Resolution, Short Cycle Times, Commutation Information, Long Line Length Support, and Encoder Diagnostics
- Features Simple Digital Connection Technology, and Simple Voltage-Supply Requirements That Reduces Overall System Cost
- Based on Sitara™ AM437x Processor Which Supports Single-Chip Motor Control Applications and Other Embedded Control and Communications Applications
- Sitara AM437x Supports a Number of Industrial Communications Standards Including EtherCAT®, PROFINET®, PROFIBUS, EtherNet®/IP™, PowerLink, and Sercos

Featured Applications

- EnDat 2.2 Master
- Industrial Drives
- Industrial Sensors and I/O Modules



1 Circuit Description

This TI Design implements the EnDat 2.2 Master protocol stack and hardware interface solution based on the HEIDENHAIN EnDat 2.2 standard for position or rotary encoders. The design is composed of the EnDat 2.2 Master protocol stack, half-duplex communications using RS-485 transceivers and the line termination implemented on the Sitara AM437x Industrial Development Kit (IDK). This design is fully tested to meet the HEIDENHAIN EnDat 2.2 standard. Along with EnDat position feedback, the AM437x IDK also supports industrial communications and motor drive as described in the *AM437x Single-Chip Motor-Control Design Guide* (TIDU800).

2 EnDat 2.2 Overview

EnDat stands for encoder data. To support streamlined factory automation processes, industrial drives with position feedback requires accurate, high-reliability, and low-latency encoder position data. The EnDat 2.2 interface provides all of these capabilities. The HEIDENHAIN EnDat 2.2 interface is a digital, bidirectional interface standard for incremental and absolution position encoders. The EnDat interface supports the transmission of position and auxiliary values from an encoder as well as transmitting or updating information stored in the encoder, or saving new information. Through this interface the EnDat Master, or subsequent electronics, uses mode commands to read encoder position values, additional encoder physical values, parameters, and the internal memory of the encoder, or to write to the memory of the encoder.

The EnDat 2.2 interface supports several encoder types. The encoder type is contained in the encoder's memory area of the encoder. The types are:

- Incremental linear encoder
- Absolute linear encoder
- Rotational incremental single-turn encoder
- Rotational absolute single-turn encoder
- Multiturn rotary encoder
- Multiturn rotary encoder with battery buffer

The EnDat 2.2 interface uses an 8-wire shielded cable, as shown in Figure 1 to connect the position encoder to the subsequent electronics. This interface contains a 4-wire RS-485 digital synchronous serial communications. The serial communications is composed of a differential bidirectional data (DATA+ and DATA–) and a differential clock (CLOCK+ and CLOCK–) that is generated by the subsequent electronics. The bidirectional date is transmitted synchronously with the clock using half-duplex transmission. The transmit data changes on the falling clock edge. Without delay compensation, the received data is latched on the rising clock edge. The clock remains high when data is not being transmitted or received. Two additional wires provide the encoder power supply. The other two wires are used for battery buffering or as parallel power supply lines to reduce IR voltage losses.

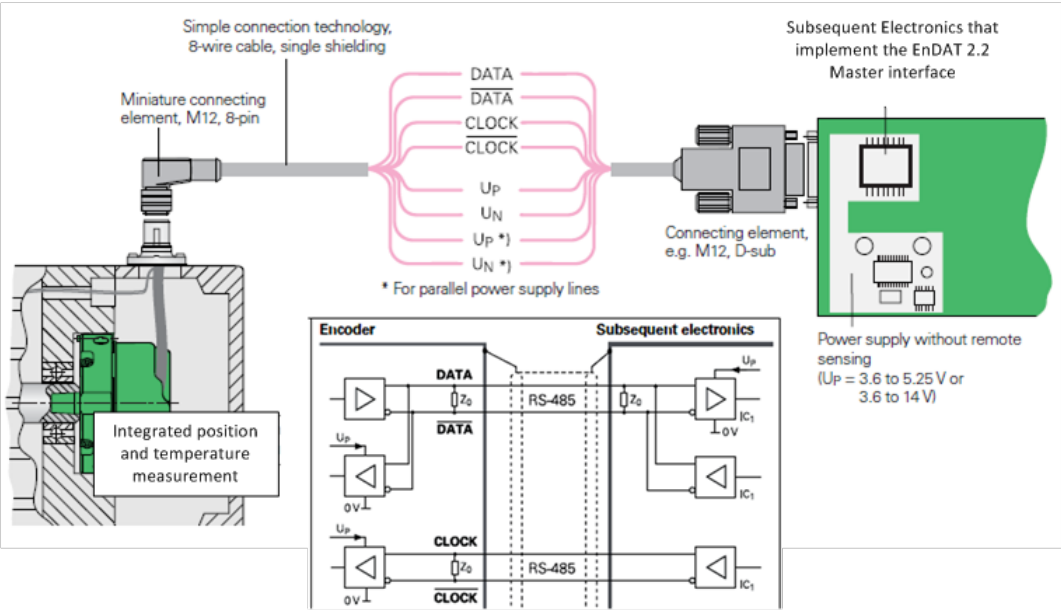


Figure 1. EnDat 2.2 Encoder and Subsequent Electronics

2.1 Without Delay Compensation

The minimum permissible clock pulse frequency is 100 kHz, and the maximum possible clock pulse frequency is 2 MHz. Without delay compensation, the maximum permissible clock pulse frequency depends on the cable length between the encoder and the subsequent electronics. Figure 2 shows the maximum permissible clock pulse frequency, Fc, with respect to the cable length between the encoder and the subsequent electronics when an on-off ratio of 1:1 is used for the clock.

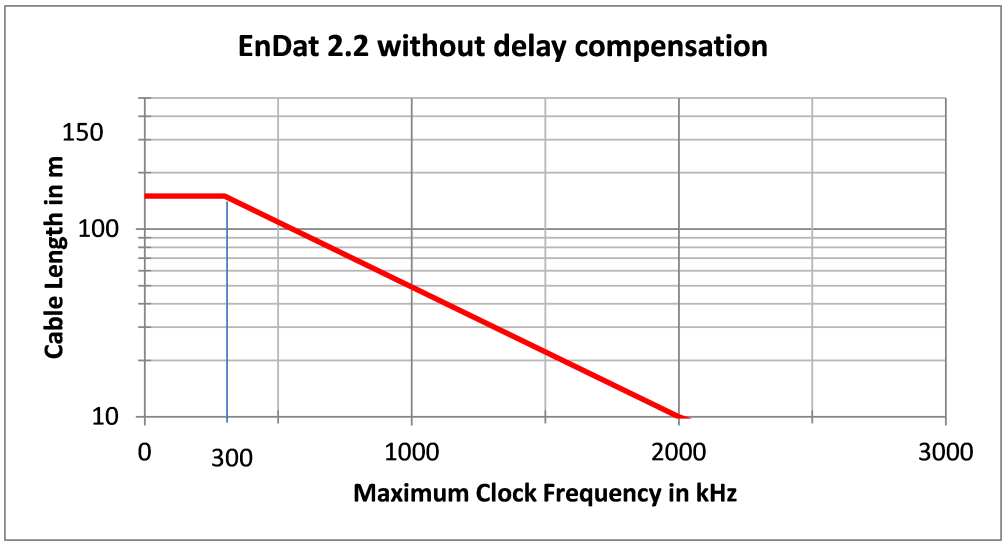
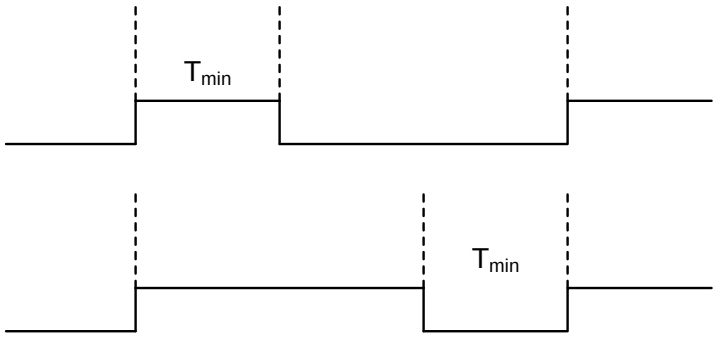


Figure 2. Maximum Clock Frequencies vs Cable Length for the EnDat 2.2 Without Delay Compensation

For all other ratios, the maximum frequencies is determined by the smallest high or low clock pulse period (see Figure 3).



$$\text{Maximum pulse frequency } F_C = \frac{1}{(2 \times t_{min})}$$

Figure 3. Maximum Clock Frequency Determination

2.2 With Propagation Delay Compensation

As the cable length increases with high clock pulse frequencies, the propagation time between the encoder and subsequent electronics becomes large enough that delay compensation must be employed to ensure clear data communications. Delay compensation is performed by the subsequent electronics on the data that is received from the encoder. The compensation is performed by determining the propagation time and compensating for the delay of the received encoder data from the transmitted clock. This compensation is independent from temperature variations. Using delay compensation, a maximum clock pulse frequency of 8 MHz is possible for cable lengths of up to 100 m. Clock frequencies from 8 to 16 MHz are intended for special applications. Figure 4 shows the maximum clock frequencies vs cable length for the EnDat 2.2.

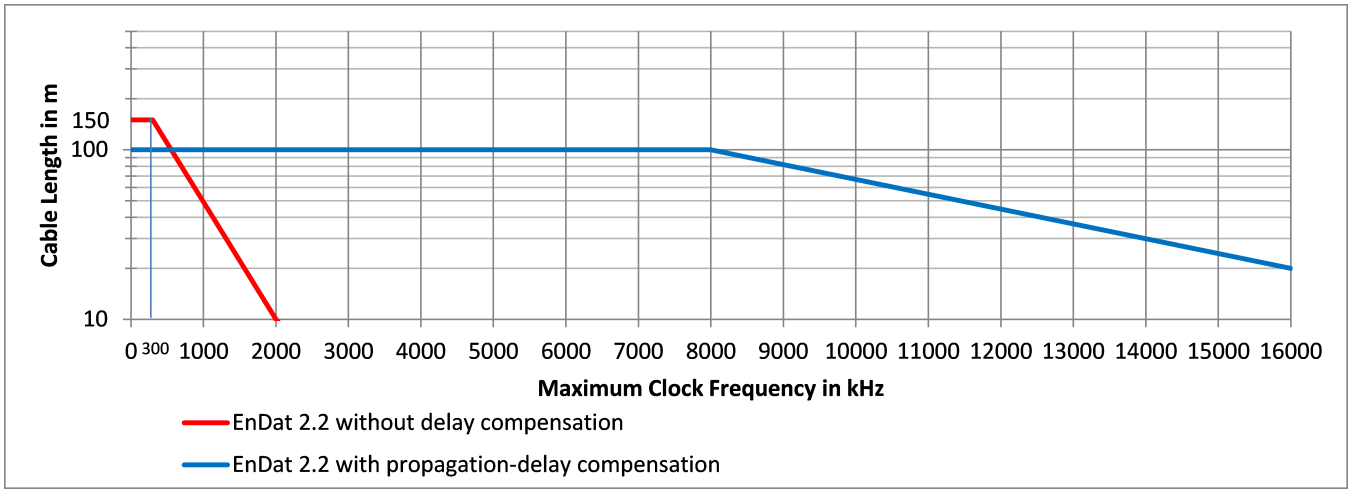


Figure 4. Maximum Clock Frequencies vs Cable Length for the EnDat 2.2

The propagation time is recomputed by the subsequent electronics whenever a hardware change is detected, or immediately after a power interruption. The propagation delay is measured using a 100 to 200-kHz clock. To achieve accuracy, the delay measurement is performed using a sampling frequency that is higher than the intended data transmission maximum intended clock frequency, Fc, with a maximum variation of less than ±10%.

The delay measurement is performed by the subsequent electronics issuing "Encoder send position values" mode command. When the encoder transceiver has switched to sending, after 10 clock pulse periods, the subsequent electronics starts a counter to measure the delay. The delay measurement is captured when the rising edge of the start bit is received. Perform the delay measurement at least three times and compute the mean. A valid measurement occurs when each measured delay value is within 1/8 of the period of the maximum intended clock pulse frequency, Fc. Figure 5 shows the delay measurement.

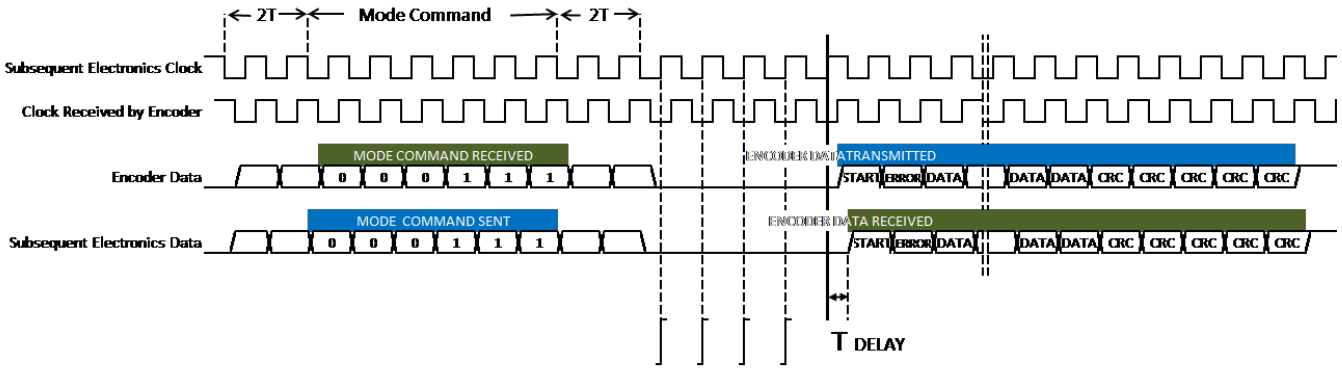


Figure 5. Delay Measurement

Example: If the maximum clock pulse frequency for later data transmission is 4 MHz (Fc = 4 MHz) – choose a sampling frequency of 4 MHz × 8 = 32 MHz or higher. The maximum permissible variation of the sampling frequency is ±10% or ±3.2 MHz. For the delay measurements to be valid, each delay measurement must be within 1 / (4 MHz) / 8 = ±312.5 ns of the mean.

To avoid a collision on the data line when data transmission with delay compensation is active, a low level msut be maintained for t_{ST} for the first clock cycle for each transmission. The value of t_{ST} should be in the range from 2 to 10 µs and is dependent upon line length and maximum clock pulse frequency. Figure 6 shows the EnDat timing.

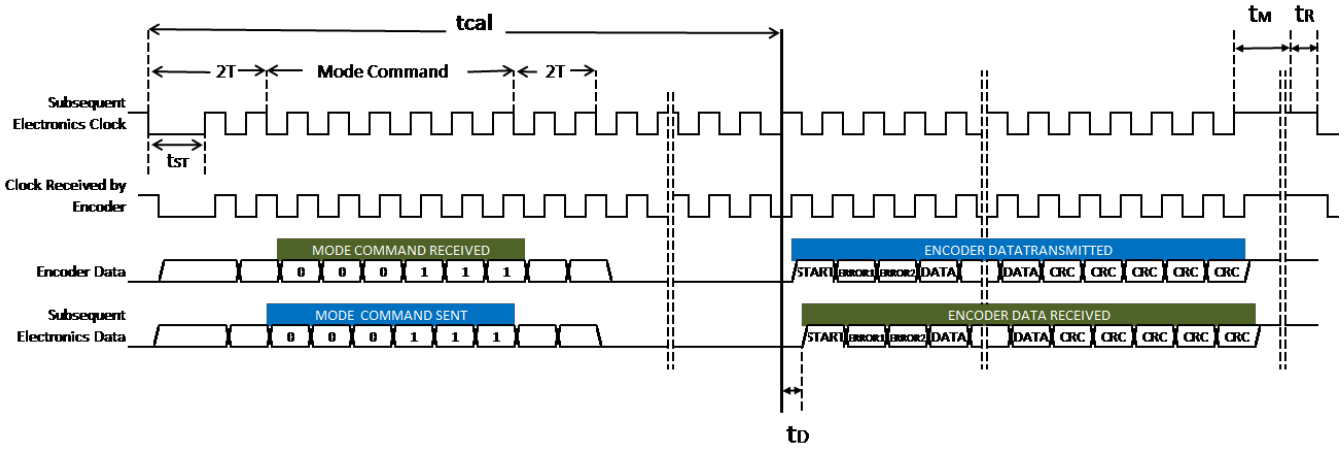


Figure 6. EnDat Timing

At the conclusion of the data transmission, the clock must be set HIGH for the recovery time, t_M. The recovery time is a selectable parameter that can be 10 to 30 µs or 1.25 to 3.75 µs . Then following an additional delay, t_R of up to 500 ns, a new transmission can be initiated. Table 1 shows the EnDat 2.2 timing.

Table 1. EnDat 2.2 Timing

PARAMTER	SYMBOL	WITHOUT DELAY COMPENSATION	WITH DELAY COMPENSATION
Clock Frequency ()	f_c	100 kHz...2 MHz	
Calculation Time for Position Value Paramater	t_{calf}	Typical of EnDat 2.2 encoders: ± µs	
	t_{ac}	Max. 12 ms	
Recovery Time	t_m	10 to 30 µs or 1.25 to 3.75 µs (> 1 MHz) (configurable)	
	t_R	Max. 500 ns	
	t_{ST}		2 µs to 10 µs
Data Delay Time	t_D	0.2 + 0.01 × (cable length in m) µs	

Additional information on the EnDat 2.2 interface is available in the *Technical Information EnDat 2.2 –Bidirectional Interface for Position Encoders* and *EnDat Interface Version 2.2 Bidirectional Synchronous-Serial Interface for Position Encoders* from Heidenhain.

3 Design Physical Implementation

This TI Design implements the EnDat 2.2 Master protocol stack and hardware interface solution based on the HEIDENHAIN EnDat 2.2 standard for position or rotary encoders. The TI design draws upon the TI AM437x Industrial Development Kit (IDK) to provide the physical hardware components and the SYS/BIOS Industrial Software Development Kit (SDK) for Sitara to provide the EnDat 2.2 Master protocol stack and the firmware supporting the EnDat 2.2 signal interface. The AM437x IDK and SDK also support industrial communications and motor drive with current feedback as described in the AM437x Single-Chip Motor-Control Design Guide (TIDU800). Figure 7 shows a simplified block diagram of the AM437x IDK and its EnDat 2.2 interface to a digital encoder along with other functions for industrial communications and motor control. Figure 8 shows the AMX437x Industrial Development Kit.

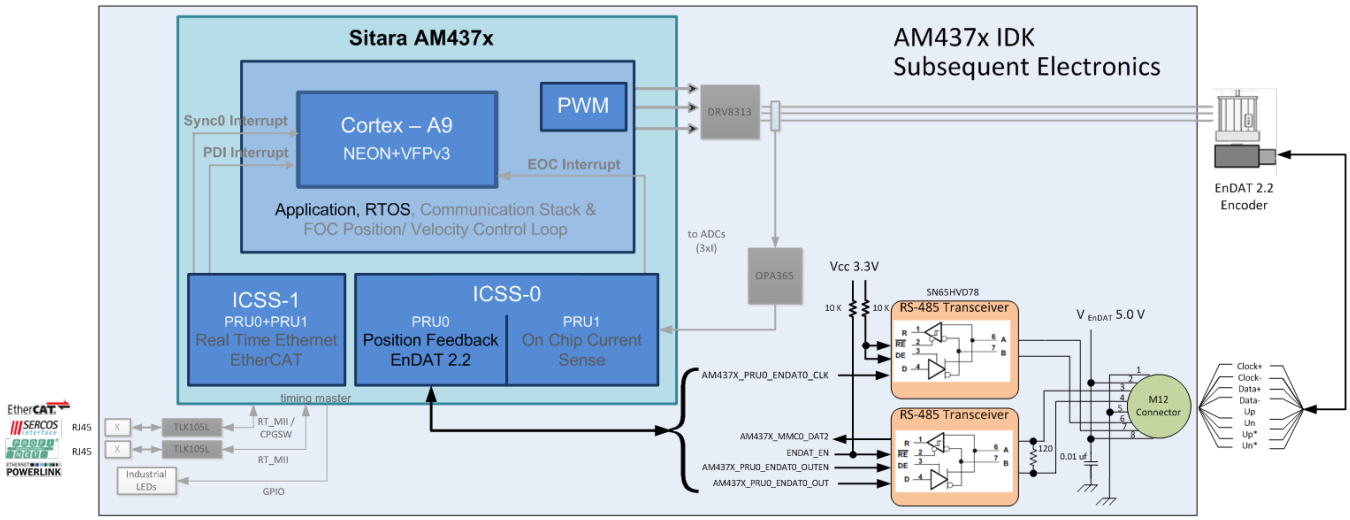


Figure 7. TIDEP0050 System Block Diagram

The major building blocks implementing the EnDat 2.2 Master interface are the AM437x, RS-485 transceivers, the encoder power supply, and the line termination.

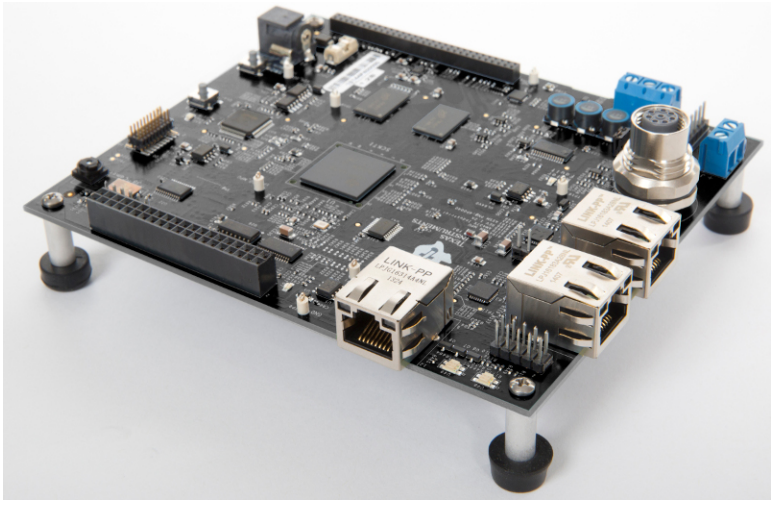


Figure 8. AM437x Industrial Development Kit

3.1 Sitara™ AM437x Architecture

The Sitara AM437x family contains a Cortex®-A9 processor with NEON and VFPv3 plus a powerful set of programmable and fixed-function peripherals for industrial communications, measurement, and control. The peripheral set includes the pulse width modulators (PWMs), analog-to-digital converters (ADCs), real-time clock, quadrature encoder pulse (QEP), a dual-camera interface, dual CANs, dual-gigabit EtherNet interfaces, and other peripheral components, as shown in Figure 9.

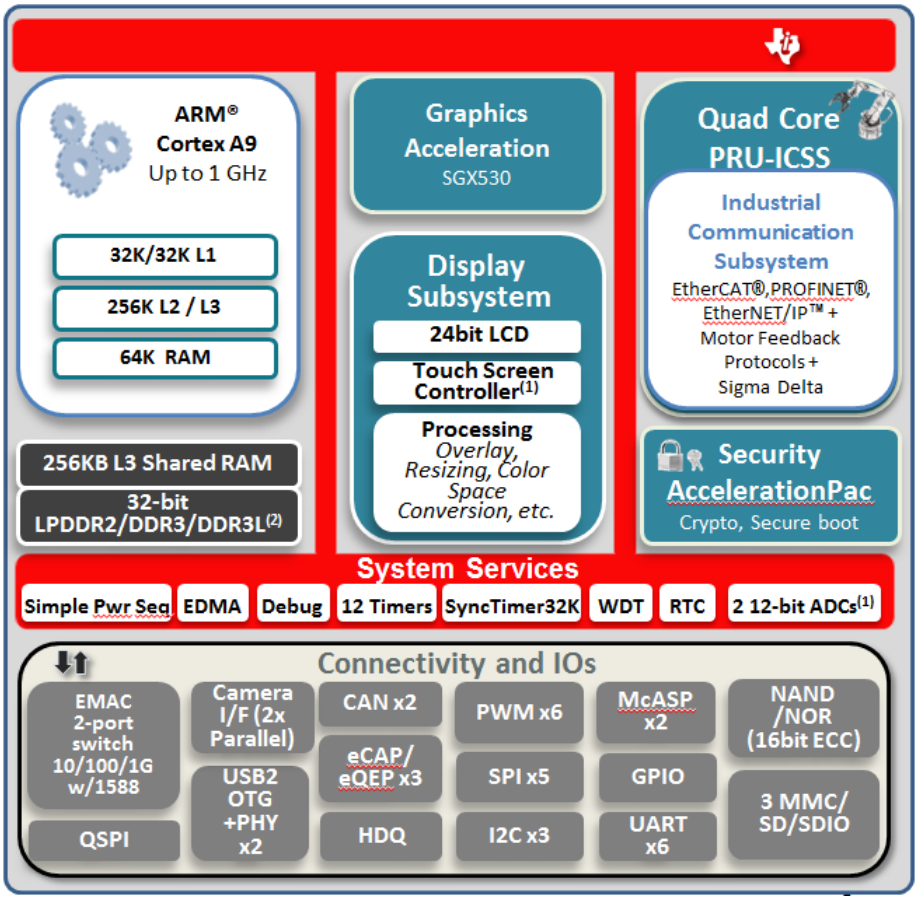


Figure 9. AM437x Device Block Diagram

One of the chief features of the AM437x family is the two Industrial Communication Subsystems (ICSSs) and their combined four programmable real-time units (PRUs). Each PRU is a 200-MHz single-cycle instruction processor with hardware multiplication that has been architected to support deterministic, real-time processing. The PRUs are used to implement industrial communication protocols such as EtherCAT and PROFIBUS®, position encoder interfaces like EnDat2.2 and BiSS, plus sigma delta data conversion. With high-level language and JTAG support on both the ARM® and ICSS cores all of the extensive development and debugging capabilities of Code Composer Studio™ (CCS) are available for support development. In addition, the AM437x family supports a variety of boot options including QSPI and NAND. This full complement of features permits a single AM437x to replace multiple devices with an easy-to-use, compact, low-power, and cost-efficient solution.

3.2 ICSS Subsystem

Figure 10 shows the functional block diagram of an ICSSs and its two PRUs. The two ICSS and their combined four PRUs are separate processing units from the ARM core. Each PRU core runs at 200 MHz with a 5-ns single-cycle instruction execution time. Each PRU core has independent instruction and data memory. Each PRU has access to all of the Sitara SoC, the device pins, memories and IOs – with only a couple of exceptions: The PRUs cannot access the ARM CPU memory; ARM interrupts and ARM receive events.

The PRUs are used to provide a variety of real-time functions in the AM437x. Real-time Ethernet protocols use the MII interface block which includes translation from 4-bit to 16-bit data and crc32 verification. In GPIO mode, the PRU maps external I/O pins directly to register R30 and R31. Serial-based protocols may also use the fast UART which can be clocked for a 12-Mbaud data rate. The EnDat protocol implementation uses direct GPIO mapping to PRU register.

The AM437x has two ICSS subsystems. One subsystem is used for multiprotocol Industrial EtherNet. The second subsystem solves communication and control functions in power and sense applications such as servo drives. The Industrial Ethernet Peripheral (IEP) includes time synchronization unit with many capture and compare registers. On the application side, the IEP is used as application PLL to synchronize PWM generation with current sensing and position sensing.

The EnDat 2.2 master interface performs line delay compensation at the start of position measurement and after any power interruption. This draws upon the compare register in the IEP timer, which triggers an event with 5-ns resolution. The numeric computations that are performed in the PRU are accelerated with PRU single-cycle hardware multiplier. Figure 10 shows the PRU architecture.

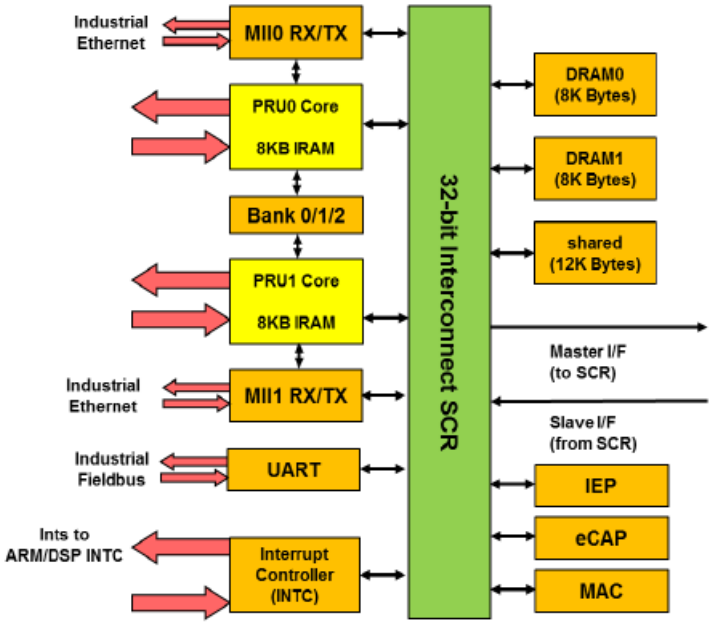


Figure 10. PRU Architecture

For additional details on the ARM9 and the ICSS architecture along with the EnDat PRU interface, see the AM437x Technical Reference Manual (SPRUHL7D).

3.3 RS-485 Transceiver

The AM437x IDK uses the clock, data transmit, data receive, and receive enable signals from PRU0 of ICSS-0 to implement the EnDat master interface. The EnDat channel 0 signal lines connect to the two onboard RS-485 transceivers. The RS485 transceiver differential signals, the termination resistors, and the power lines connect to the M12 connector. All three PRU0 EnDat channel signals are also available through the J16 expansion connector to support an external transceiver connection.

Because the EnDat transmission occurs between the falling and rising clock edges, an EnDat 2.2-compliant RS-485 transceiver must meet a minimum baud rate of 32 Mbps. When EnDat 2.2 is implemented without delay compensation at a maximum clock of 2 MHz, the loop propagation delay (master and encoder) must not exceed 250 ns. The SN65HVD78 was chosen as a transceiver because it met these requirements as summarized in Table 2.

Table 2. RS-485 Parameters of the SN65HVD78 Data Sheet (SLLSE11)

PARAMETER	SN65HVD78
Supply voltage (recommended)	3.3 V
Baud rate (maximum)	50 Mbps
Receiver propagation delay (maximum)	35 ns
Driver propagation delay (maximum)	15 ns
Receiver rise/fall time (maximum)	5 ns
Driver rise/fall time (maximum)	6 ns
Supply current (quiescent) driver and receiver enabled	0.95 mA (max)
IEC61000-4-2 ESD (absolute maximum ratings)	±12 kV (CD)
IEC61000-4-4 EFT (absolute maximum ratings)	±4 kV

The differential bus terminals of the SN65HVD78 transceiver provides on-chip ESD protection against ±15 kV human body model (HBM) and ±12 kV IEC61000-4-2 contact discharge. To meet the SN65HDV78 protection and performance- specific design and layout rules must be followed for the PCM design. For a complete list of layout guidelines, see the SN65HVD78 data sheet.

The design uses one 120-Ω/0.5-W resistor to terminate the differential data signals of the RS-485 transceivers. In the case of the data lines, the termination is applied on both the subsequent equipment and the encoder sides. Because the clock is configured as transmitter only, the termination for the clock is performed on the encoder side. Figure 11 shows the transceivers and EnDat signal termination.

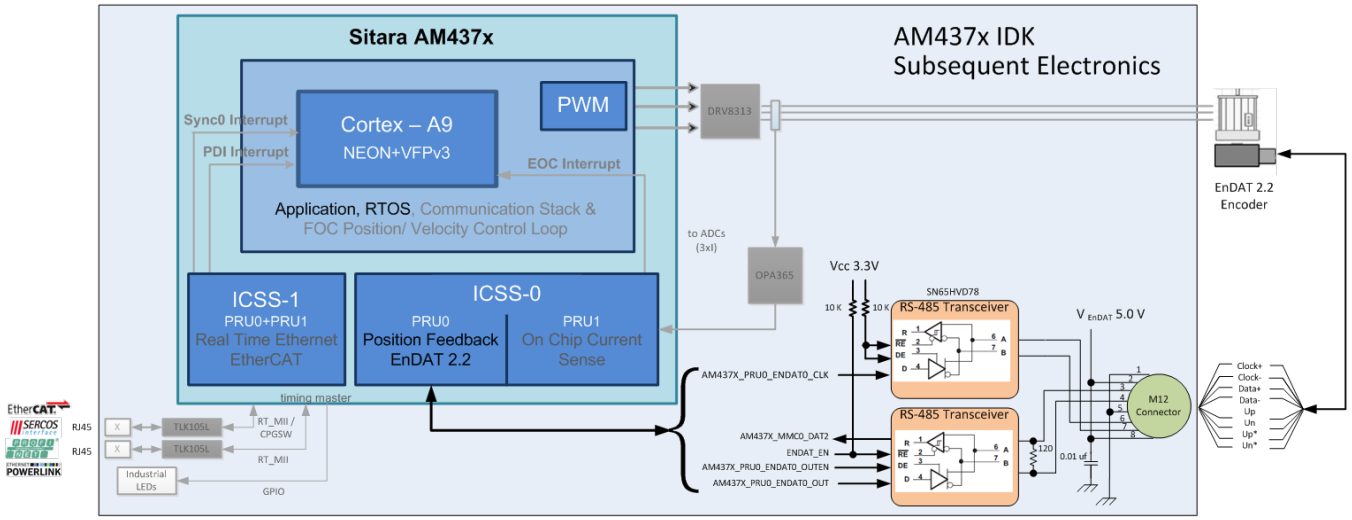


Figure 11. RS-485 Transceivers and EnDat Signal Termination

The communication interface uses a 3.3-V supply for the RS-485 transceivers. This is provided by a TPS5402D DC-DC converter circuit shown in Figure 10. These circuit coverts the 24 volt supply input to the AM437 Industrial Development Kit EVM to a 3.3-V rail that is used to support multiple circuits on the board.

The 5-V EnDat supply voltage is provided by a TPS5402D DC-DC converter circuit shown in Figure 11. This circuit coverts the 24-V supply input to the AM437 Industrial Development Kit EVM to a 5-V rail for the EnDat supply. Figure 12 shows the 3.3-V logic power supply schematic and Figure 13 shows the 5.0-V power supply schematic.

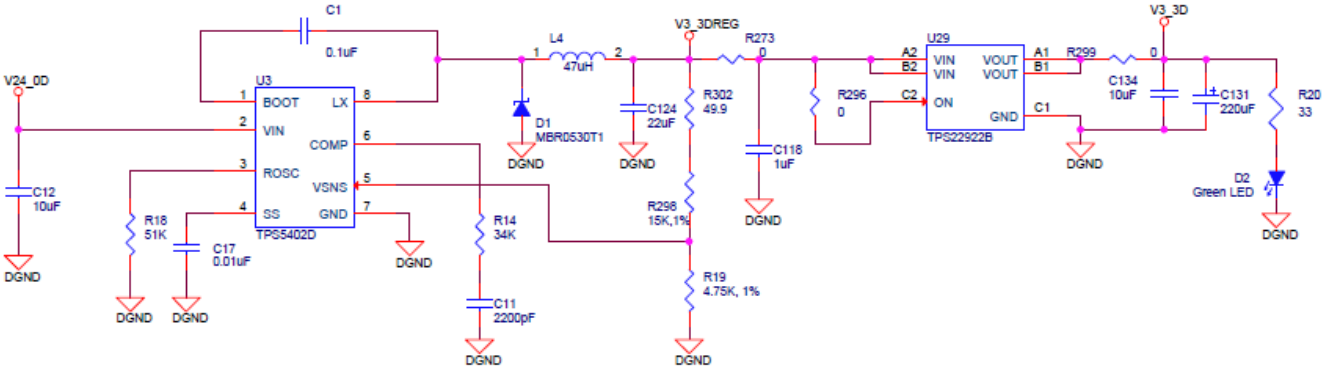


Figure 12. 3.3-V Logic Power Supply Schematic

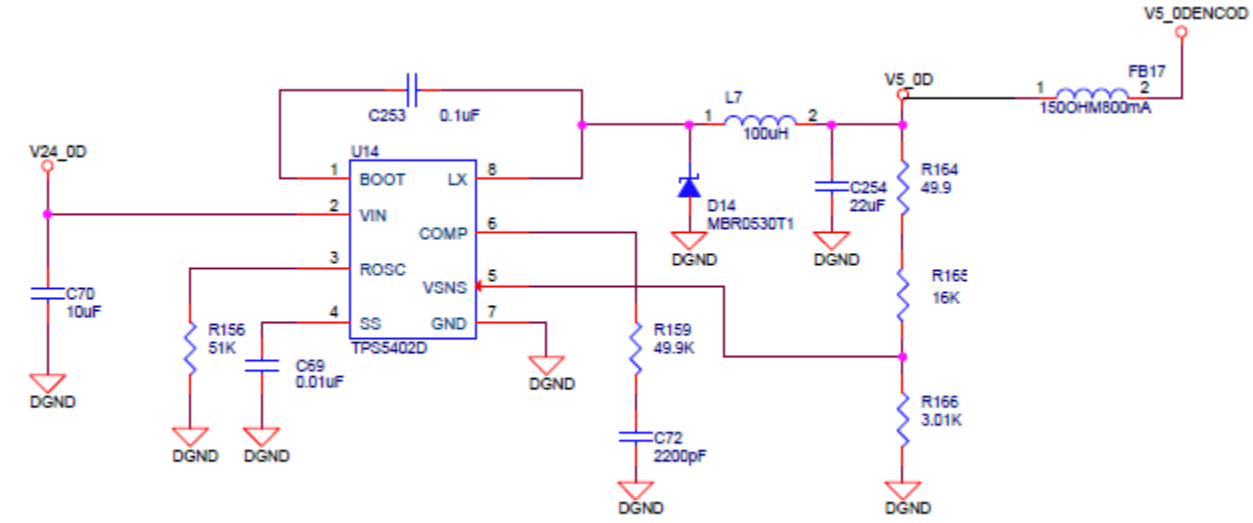


Figure 13. 5.0-V Power Supply Schematic

Table 3 provides the AM437x EnDat pin multiplexing data.

Table 3. AM437x EnDat Pin Multiplexing

PIN NAME	SIGNAL NAME	MODE	OFFSET	FUNCTION
mcasp0_aclkx (pru0_pru0_gpo0)	pru0_EnDat0_clk	5	0x0990	Channel 0 clock
mcasp0_aclkx (pru0_pru0_gpo1)	pru0_EnDat0_out	5	0x0994	Channel 0 trans,it
mcasp0_aclkx (pru0_pru0_gpo2)	pru0_EnDat0_outen	5	0x0998	Channel 0 transmit enable
mmc0_dat2 (pr0_pru0 _gpi9)	pru0_EnDat0_in	6	0x08F4	Channel 0 receive
print_mnb (gpio5[12])	EnDat_en	7	0x0A34	Channel 0, onboard RS485 receive enable
mcasp0_ahclkr (pr0_pru0_gpo3)	pru0_EnDat1_clk	5	0x099C	Channel 1 clock
mcasp0_aclkr (pr0_pru0_gpo4)	pru0_EnDat1_out	5	0x09A0	Channel 1 transmit
mcasp0_fsr (pr0_pru0_gpo5)	pru0_EnDat1_outen	5	0x09A4	Channel 1 transmit enable
mmc0_dat1 (pr0_pru0_gpi10)	pru0_EnDat1_in	6	0x08F8	Channel 1 receive
mcasp0_axr1 (pr0_pru0_gpo6)	pru0_EnDat2_clk	5	0x09A8	Channel 2 clock
mcasp0_ahclkx (pr0_pru0_gpo7)	pru0_EnDat2_out	5	0x09AC	Channel 2 transmit
mmc0_dat3 (pr0_pru0_gpo8)	pru0_EnDat2_outen	5	0x08F0	Channel 2 transmit enable
mmc0_dat0 (pr0_pru0_gpi11)	pru0_EnDat2_in	6	0x08FC	Channel 2 receive

4 Additional Texas Instruments EnDat 2.2 Designs for the AM437x IDK

Texas Instruments also offers a *Reference Design for an Interface to a Position Encoder with EnDat 2.2* (TIDU368). This design is an external EnDat 2.2 design that attaches to the AM437x IDK J16 expansion connector. This TI Design implements a hardware interface solution based on the HEIDENHAIN EnDat 2.2 standard for position or rotary encoders. The design includes building blocks that include the protected power supply, half-duplex RS-485 transceivers, and line termination with EMC protection. An auxiliary power supply and logic level interface with adjustable I/O voltage level is provided to connect to subsequent MCUs and MPUs (such as a Sitara AM437x) that would run the EnDat 2.2 Master protocol stack. This design is fully tested to meet EMC immunity requirements for ESD, Fast Transient Burst and Surge according to IEC61800-3. Figure 14 shows a AM437x Industrial Development Kit and the TI TIDA-00172 EnDat 2.2 Reference design

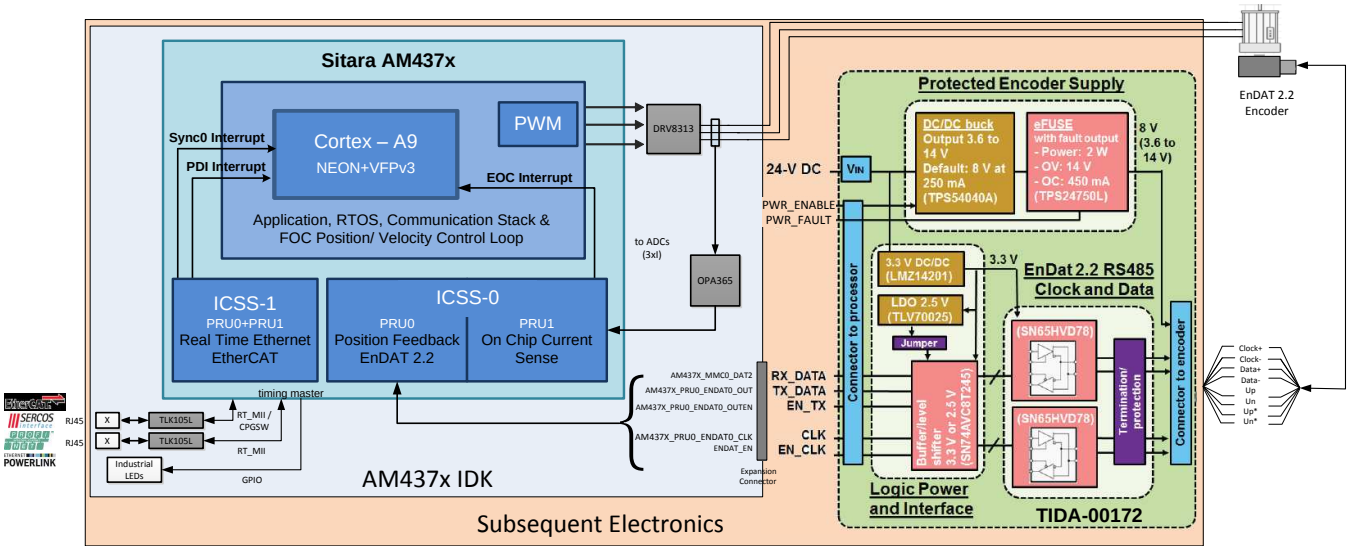


Figure 14. AM437x Industrial Development Kit and the Texas Instruments TIDA-00172 EnDat 2.2 Reference Design

5 EnDat Software Implementation

In this design, the real-time processing for the EnDat master interface, communication and data acquisition functions are performed by the PRU0 that is contained in ICSS-0 Each PRU can support three EnDat channels.

The software architecture for this design is composed of three parts – EnDat hardware support in PRU, the firmware running in PRU, and EnDat driver running in ARM. An industrial application uses the EnDat driver APIs to control EnDat operations. In this design, ICSS-0 PRU0 performs the EnDat real-time control and processing functions. The ARM Cortex-A9 processor driver APIs communicate to the EnDat firmware through a shared memory interface. A command interface in the shared memory is implemented and provides all necessary parameters on data, transmission, status, and errors for the communication. Figure 15 shows the EnDat design.

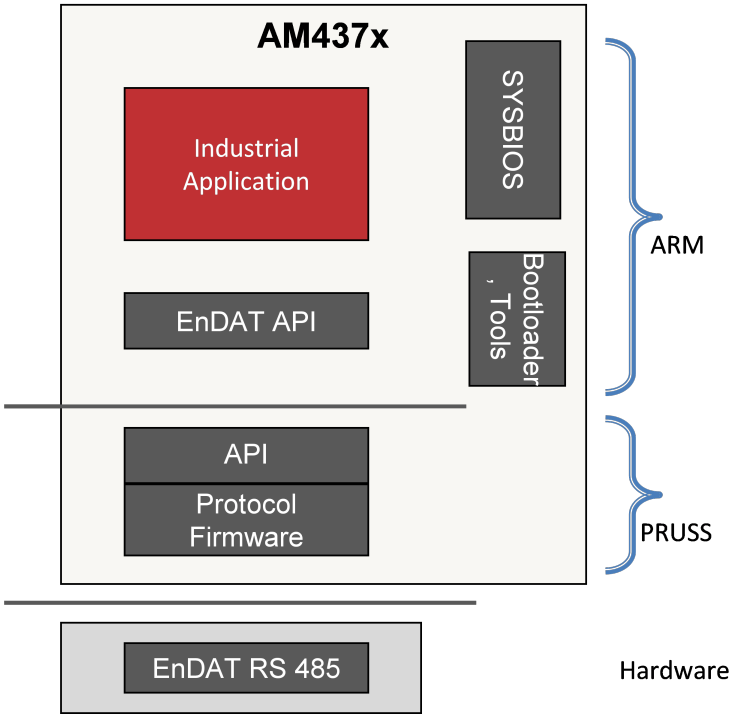


Figure 15. EnDat Design

5.1 EnDat Design Software

The ARM uses 21 EnDat APIs

1. endat_init–Initialize EnDat firmware interface address and get the pointer to EnDat data structure instance.
2. endat_config_host_trigger–Configure EnDat master for host trigger mode.
3. endat_config_channel–Select channel to be used by EnDat Master.
4. endat_wait_initialization–Wait for EnDat master firmware to initialize.
5. endat_command_build–Set up the EnDat command in the PRU interface buffer.
6. endat_command_send–Trigger sending the EnDat command in PRU.
7. endat_command_wait–Wait till PRU finishes EnDat transaction.
8. endat_command_process–Send the EnDat command and wait till firmware acknowledges.
9. endat_recvd_process–Process raw received data and format based on the command.
10. endat_recvd_validate–Validate CRC value.
11. endat_get_encoder_info–Update EnDat data structure with position resolution, ID, serial number, encoder type and supported command set.
12. endat_get_prop_delay–Get propagation delay automatically estimated by the firmware.
13. endat_addinfo_track–Track presence of additional information in EnDat data structure.
14. endat_config_clock–Configure EnDat clock.
15. endat_config_tst_delay–Configure EnDat t_{ST} delay.
16. endat_config_rx_arm_cnt–Configure rx ARM counter.
17. endat_config_rx_clock_disable–Configure clocks to be disabled at the end of rx to account for t_D.
18. endat_start_continuous_mode–Start continuous mode.
19. endat_stop_continuous_mode–Stop continuous mode.
20. endat_config_periodic_trigger–Configure EnDat Master in periodic trigger mode.
21. endat_get_2_2_angle–Read EnDat 2.2 angular position in steps for rotary encoders. This checks the CRC status (updated on-the-fly by firmware), the group alarm errors (F1/F2 bits) and the angle value received.

5.2 EnDat Master Firmware

The majority of the EnDat master functionality is implemented in PRU firmware. Figure 16 shows the EnDat firmware control sequence.

The first step upon system initialization is the initialization of PRU EnDat hardware and the attached EnDat encoder.

1. When the initialization is complete the firmware waits for an EnDat Operation command and for the command trigger bit to be set.
2. When the firmware detects that the trigger has been set, a check is made to determine if the whether the command requested is in continuous mode or is a normal command.

For a normal command:

1. The firmware reads command attributes to determine the transmission and reception parameters.
2. The firmware transmits the mode command to the encoder, waits to the encoder to send a response and then collects the data sent by the encoder.
3. The data that is returned by the encoder is captured at an 8x oversampled rate. As a result, each bit of the data is stored as a byte in the receive buffer.
4. The firmware checks the command attributes to see if a 2.2 command supplement should be transmitted based on attributes. If a command supplement is scheduled, the firmware performs the transmission.
5. The received data is downsampled to extract 2 bits from oversampled 8 bits and the result is written to the defined PRU RAM locations.

For a command requested in continuous mode:

1. The firmware reads command attributes to determine the transmission and reception parameters.
2. The clock is configured to be in free run mode.
3. The firmware transmits the mode command to the encoder.
4. In continuous mode the downsampling is done on-the-fly. In this case the downsampling is done as each bit is received to support the continuous data reception.
5. When data is read, the command trigger interface is checked to see if there has been a command to stop continuous mode.
6. If a stop command has been received then the transmit is reinitialized and the receive is disabled.

At the completion of the transaction requested by the user, the trigger bit that is set is reset. The EnDat driver provides API for the ARM application to poll and test this bit.

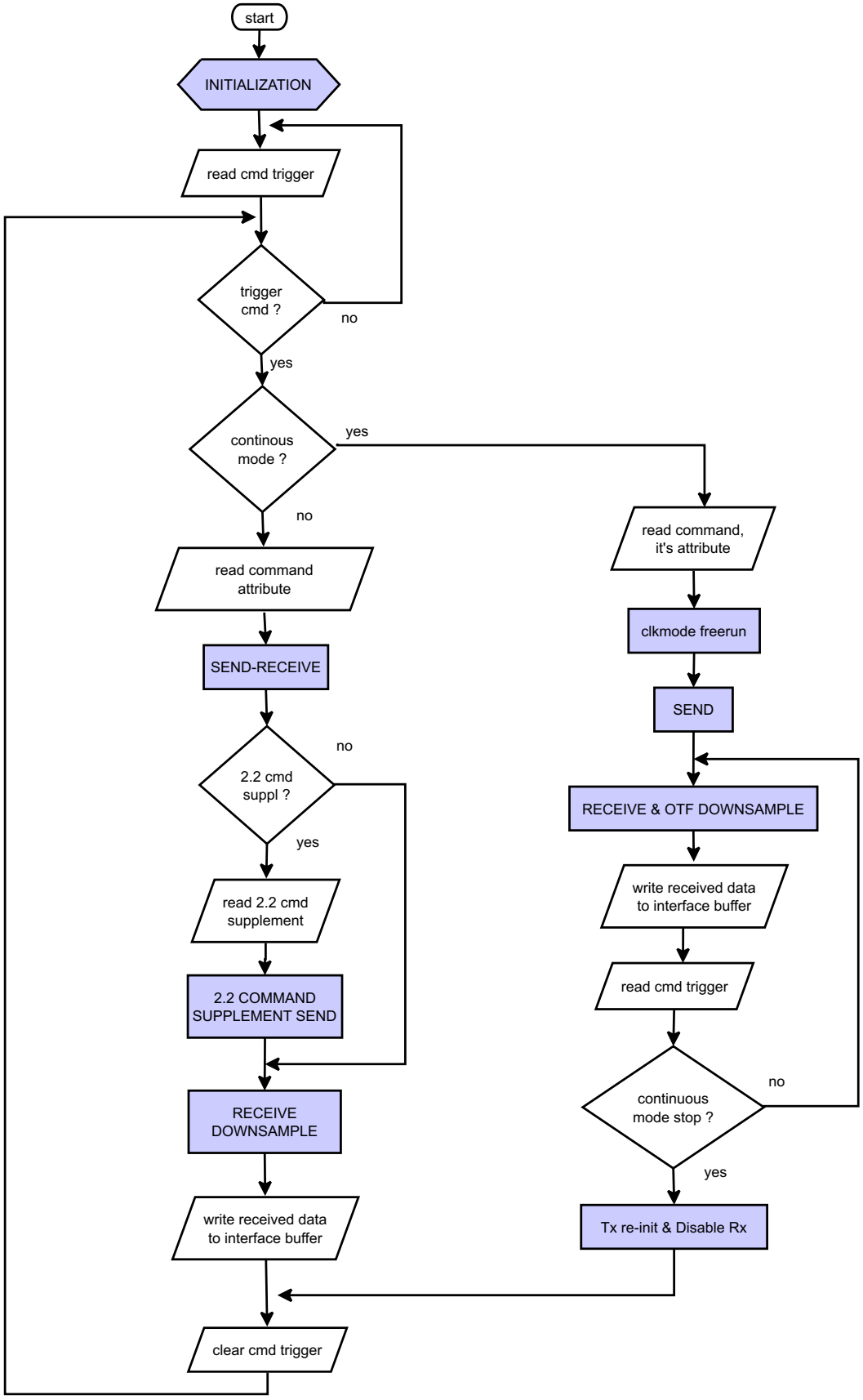


Figure 16. EnDat PRU Firmware

5.3 EnDat Master Processing Resource and Performance

All EnDat Master real-time processing functions are implemented by the ICSS-PRU.

Each PRU can support two EnDat 2.2 Masters operating at 8 MHz or one EnDat 2.2 master operating at 16 MHz. An planned update enables three EnDat 2.2 Masters operating at 8 MHz.

6 EnDat 2.2 Mode Commands

The EnDat mode commands define the exchange of information between the encoder and the subsequent electronics. The EnDat 2.2 command set includes all EnDat 2.1 mode commands. In addition, the EnDat 2.2 mode commands enable the exchange of additional data and memory transfers. The supported command set is stored in the encoder parameters.

To ensure reliable transfer of mode commands, the first 3 mode bits are also transferred in inverted format for redundancy. If the encoder detects a faulty transfer of mode bits, an error is generated. Table 4 lists the EnDat mode commands.

Table 4. EnDat Mode Commands

MODE COMMAND	TYPE	MODE
Encoder send position values	2.1	0
Encoder send position values with additional data	2.2	7
Selection of memory area	2.1	1
Encoder send position values and selection of memory area or of the additional data 2	2.2	1
Encoder send parameter	2.1	4
Encoder send position values and send parameter	2.2	4
Encoder receive parameter	2.1	3
Encoder send position values and receive parameter	2.2	3
Encoder receive reset	2.1	5
Encoder send position values and receive error reset	2.2	5
Encoder receive test command	2.1	6
Encoder send position values and receive test command	2.2	6
Encoder send test values	2.1	2
Encoder receive communication command	2.2	2

The position value can be transmitted with or without additional data. Figure 17 shows the EnDat position command and encoder response.

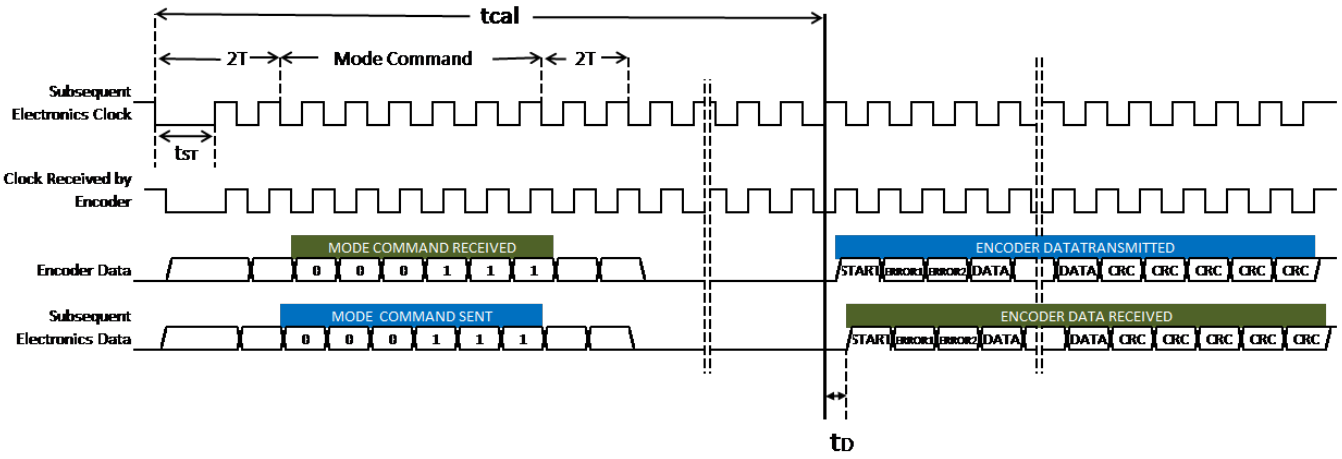


Figure 17. EnDat Position Command and Encoder Response

The encoder transmits the position value, beginning with the LSB. The number of bits transferred is dependent upon the encoder being used. The number of required clock pulses for transmission of a position value is saved in the parameters section of the encoder. After the data, a cyclic redundancy check (CRC) is sent.

The position value can be transmitted with or without additional data. When additional data is requested, this position value is followed by the additional data, and each also concluded with a CRC. This combination is then transmitted with every sample until a new selection is specified. With the end of the data word, the clock must be set to high. After 1.25 to 3.75 µs the data line falls back to low, then a new data transmission can be initiated by starting the clock.

The position information is not transmitted to the subsequent electronics until after the calculation time t_{cal} has passed. The value t_{cal} is the encoder calculation time that is stored in the encoder internal memory. This value is computed for the highest clock frequency permissible supported by the encoder, up to 8 MHz. The encoder transfers only the number of bits needed to support the precision that is specified for the encoder. The number of bits depends on the respective encode. This value is stored in the encoder parameters.

6.1 Error Messages 1 and 2

The EnDat interface provides a comprehensive monitoring of the encoder. An error is transmitted when a malfunction of the encoder results in incorrect position values. There is only one error message that appears and it is transmitted in two fields. One error message will appear in regular format, and the other will appear in bit inverted. The cause of the error is saved in the encoder internal memory. The types of errors that are reported by the encoder include:

- Light unit failure
- Signal amplitude too low
- Error in calculation of position value
- Supply voltage too high or too low
- Current consumption is excessive

The second error message is a bit inverted transmission of the error message for redundancy.

6.2 EnDat Additional Data

One or two items of additional data can be appended to the position value. The description of the additional data supported by the encoder is saved in the encoder parameters. When additional data is sent by the encoder, it immediately follows the CRC and the last bit of the previous transmission with the following format, as shown in Figure 18.

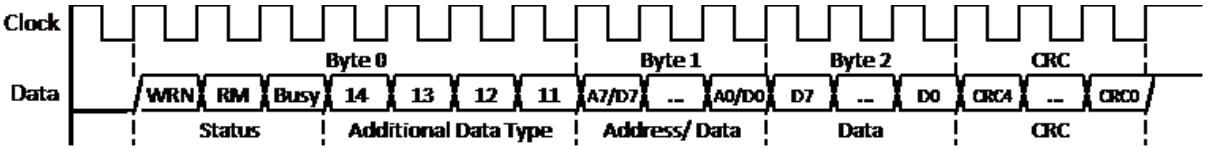


Figure 18. Additional Data Format

The content of the additional data is defined by the mode command for selection of a memory area. This content, updated with each clock pulse, is transmitted until there is a new request. A unique number is assigned to each additional datum. This unique number is 5 bits long and is transmitted for inspection purposes.

6.3 Status Information

Table 5 provides the status that is reported by the slave device .

Table 5. Status Bits

STATUS BIT	VALUE	DESCRIPTION
WRN	0	No warning
	1	Indicates that a warning occurred (group alarm). The cause of the warning can be read from the encoder memory.
Busy	0	Ready for internal data processing (read/write); parameter request possible.
	1	Internal data processing (read/write) active.
RM	0	Reference run not finished.
	1	Reference run complete, absolute position value available. Already available at switch-on for absolute encoders.

6.4 Additional Datum 1

- **Diagnostics**—Cyclic information on the encoder function and additional diagnostic values, such as mounting information
- **Position Value 2**—For incremental encoders: Relative position information (the counter starts at zero at switch-on). The absolute position value is only available after the reference marks are traversed (RM bit HIGH). For absolute encoders: Second absolute position value for safety-related applications.
- **Memory Parameters**—Parameters saved in the encoder may also be transmitted with the position values. The request is defined through memory range selection, followed by the output of the parameters with the associated address.
- **MRS Code–acknowledgment**—Acknowledgment of the requested memory area selection
- **Test Values**—Test values serve for inspection purposes (for example, in service diagnostics).
- **Temperature**—Transmission of temperature in the encoders with integrated evaluation of internal or external temperature sensors
- **Additional Sensors**—The EnDat 2.2 protocol enables the connection of 16 additional sensors (using the 4-bit address).

6.5 Additional Datum 2

- **Communication**—Some incremental encoders provide "rough" position information for communication in electric motors.
- **Acceleration**—If the encoder has additional sensor systems for acceleration measurement, the sensor transmits the results.
- **Limit Position Signals**—Limit position signals and homing information.
- **Asynchronous Position Value**—Position formed by oversampling between two "regular" requests.
- **Operating Status Error Sources**—Detailed information about the cause of the present error message.
- **Timestamp**—Reserved for touch probes.

6.6 Memory Areas

The encoder provides several memory areas for parameters. These memory areas can be read from the subsequent electronics. Some of the values are written by the encoder manufacturer, the OEM, or the end user. The parameter data is stored in a permanent memory. The memory permits only a limited number of write access events and is not designed for cyclic data storage. Certain memory areas can be write-protected (this can only be reset by the encoder manufacturer can be reset).

The parameters that are saved in various memory areas include:

- **Parameters of the encoder manufacturer**—This write-protected memory area contains all the information specific to the encoder, such as encoder type (linear, angular, single-turn, muliturn, and so forth), signal periods, the number of position values per revolution, the transmission format of absolute position values, direction of rotation, maximum permissible speed, accuracy dependent on shaft speeds, support of error and warning messages, part number, and serial number. The information provides what is needed for automatic configuration.
- **Parameters of the OEM**—This area is reserved for the OEM information which includes the motor ID, maximum current rating, and so forth.
- **Operating Parameters**—This area is available for the user.
- **Operating Status**—This memory area provides detailed error messages or warnings for diagnostic purposes. In the operating status, the user can initialize encoder functions, activate write protection for the OEM parameters and operating parameter memory areas, and interrogate the status of these parameters and memory areas.

7 EnDAT Performance Tests

7.1 Test Description

This test covers the operation of the EnDat Master interface that performs the EnDat 2.1 and 2.2 operations with propagation delay compensation.

7.2 Hardware Configurations

The tested hardware configuration was a AM4379 Industrial Development Kit connected to one of three EnDAT encoders. The encoders that were tested were the Heidenhain ROQ437, ROQ1037 (iirc), and LC 415 (iirc). The tests were performed at 8 MHz operation using 100 m of EnDat cable, and at 16 MHz operation with 20 m of cable with delay compensation enabled. The tests were also performed at 300 kHz operation with 150 m of EnDat cable and at 2 MHz with 10 m of cable without delay compensation.

7.3 Software Configurations

The software test configuration is:

- SYSBIOS Industrial Software Development Kit 02.01.00.01
- Code Composer Studio version CCS 6.1.0.00104
- SYS/BIOS 6.41.4.54 Real-Time Operating System
- XDC Tool 3.31.2.28_core
- NDK 2.24.2.31
- Compiler GNU v4.8.4 (Linaro)
- Teraterm Serial console terminal application

7.4 Test Reults

Testing of the EnDAT master showed good performance for all modes and cable lengths as listed in Table 6.

Table 6. Test Results

MODE COMMAND	TYPE	PASS/FAIL	FUNCTION
Encoder send position values	2.1	Pass	Request a position value.
Encoder send position values with additional data	2.2	Pass	Request a position value and additional data, such as diagnostic, commutating, and acceleration in the same cycle.
Selection of memory area	2.1	Pass	Select the memory area.
Encoder send position values and selection of memory area of the additional data 2	2.2	Pass	Request a position value and select the memory area or block address in the same cycle.
Encoder send parameter	2.1	Pass	Send parameters necessary for read access.
Encoder send position values and send parameter	2.2	Pass	Request a position value and in the same cycle send parameters necessary for read access.
Encoder receive parameter	2.1	Pass	Write parameters.
Encoder send position values and receive parameter	2.2	Pass	Request a position value and write parameters in the same cycle.
Encoder receive reset	2.1	Pass	Execute a reset.
Encoder send position values and receive error reset	2.2	Pass	Request position values and reset errors in the same cycle.
Encoder receive test command	2.1	Pass	Write a test command.
Encoder send position values and receive test command	2.2	Pass	Request position values and write a test command in the same cycle.

8 Summary

This TI Design implements the EnDat 2.2 Master protocol stack and hardware interface solution based on the HEIDENHAIN EnDat 2.2 standard for position or rotary encoders. This TI Design enables developers to use EnDat 2.2 encoder interlaces to implement low footprint, low-power single-chip solutions in applications such as industrial automation and factory automation. This design is fully tested to meet the HEIDENHAIN EnDat 2.2 standard. Along with EnDat position feedback, the AM437x IDK can also support industrial communications and motor drive as described in the *AM437x Single-Chip Motor-Control Design Guide* (TIDU800).

8.1 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP0050.

9 References

1. *Sensored Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors* (SPRABP8)
2. AM335x and AM437x EtherCAT firmware API guide

10 About the Authors

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