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TIDA-00392
October 2015

TI Designs: Reference Design

Monitoring Voltage Rails on Delfino™ with TPS3702

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Circuit Description

The C2000™ Delfino™ microcontroller demands a tight tolerance on both of its supply rails; this TI Design monitors the two voltage rails and asserts a reset when either rail is not within its specified supply voltage range. The TPS3702 window comparators monitor for both undervoltage and overvoltage faults on each voltage rail and incorporate glitch immunity and hysteresis to ensure proper resets.

Design Resources

TI Design Number	Design Folder
Design Archive	All Design files
TPS3702	Product Folder
TPS62420	Product Folder
TMS320F28377D	Product Folder
Other EVMs / TI Designs	Tools Folder

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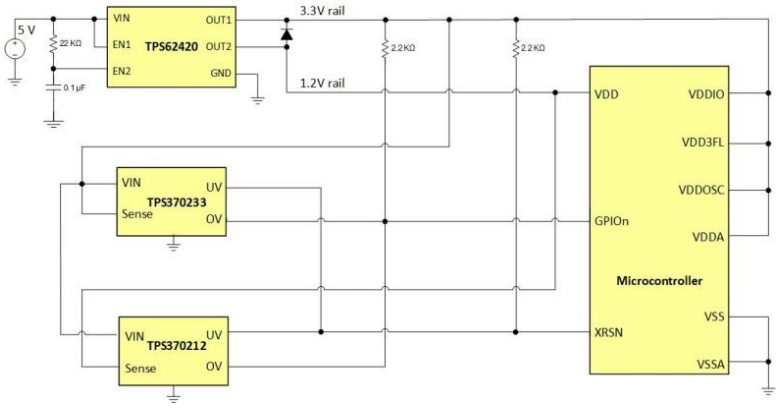

1 Design Parameters

Table 1: TMS320F28377D Electrical Specifications

Device	Parameter	Description	Specification	Tolerance	Max Current Consumption
Delfino Microntroller	VDD3VFL	Flash power pins	3.3 V	± 5 %	40 mA *
	VDDOSC	On-chip crystal oscillator	3.3 V	± 5 %	-
	VDDIO	Digital I/O power pins	3.3 V	± 5 %	55 mA *
	VDDA	Analog power pins	3.3 V	± 5 %	25 mA *
	VDD	Digital logic power pins	1.2 V	± 5 %	480 mA *

* All I/O pins are left unconnected.

Table 2: TPS62420 Electrical Specifications

Device	Parameter	Description	Specification	Tolerance	Max Current Output
TPS62420	VIN	Input voltage	5 V		
	Vout1	First channel output voltage	3.3 V	± 1%	600 mA
	Vout2	Second channel output voltage	1.2 V	± 1%	1000 mA

2 Theory of Operation

The Delfino™ microcontroller, TMS320F28377D, requires two supply voltage rails for operation: 3.3 V and 1.2 V. There is a ±5% tolerance associated with each rail, as shown in Table 1. An adjustable dual DC/DC converter, TPS62420, was selected to generate both rails. To ensure that each rail is within its specified range, both are monitored by a window voltage detector, TPS3702, which features undervoltage (UV) and overvoltage (OV) detection. Any deviation from the specified supply voltage range will trigger a reset signal that will be read by the microcontroller.

In order to power up the microcontroller properly, the 3.3 V rail needs to be powered on first, followed by the 1.2 V rail, as shown in Figure 2. To do this, a resistor and capacitor were placed on the second channel enable pin, EN2, of the TPS62420, creating an RC delay between the start of each rail's ramp, as shown in Figure 3. A diode was also added between the two output rails to ensure that the 3.3 V rail is always higher than the 1.2 V rail per specification.

In order to monitor both rails simultaneously, both window comparators' OV outputs are wire-OR'ed to a general purpose input/output (GPIO) pin of the microcontroller. When the microcontroller reads a low output signal (OV is active-low), it will run an interrupt to hold the microcontroller in reset until normal operating conditions resume. The UV outputs of each TPS3702 are also wire-OR'ed and connected directly to the microcontroller's reset pin, asserting a system reset when an undervoltage condition is detected on either rail.

2.1 Design

2.1.1 Sense Accuracy

The TMS320F28377D specifies a ±5% tolerance for both of its supply rails. A ±5% tolerance for the 3.3 V rail specifies a range from 3.13 V to 3.46 V. The TPS3702 monitors various voltages including 3.3 V. It also features two built-in window threshold options that can be chosen by setting the SET pin high or low. The TPS3702CX33 was selected with the SET pin pulled high to enable the ±4% window threshold option. This yields a nominal overvoltage threshold of 3.17 V and a nominal undervoltage threshold of 3.43 V. However, once the ±0.9% tolerance for each of the thresholds is factored in, the overvoltage threshold voltage may vary from 3.40 V to 3.46 V depending on system conditions. The undervoltage threshold can vary from 3.14 V to 3.19 V. This is depicted in Figure 1. Setting the thresholds in this manner prevents the voltage rail from deviating outside the specified ±5% without triggering a reset.

The same approach was used when selecting TPS3702CX12 to monitor the 1.2 V rail.

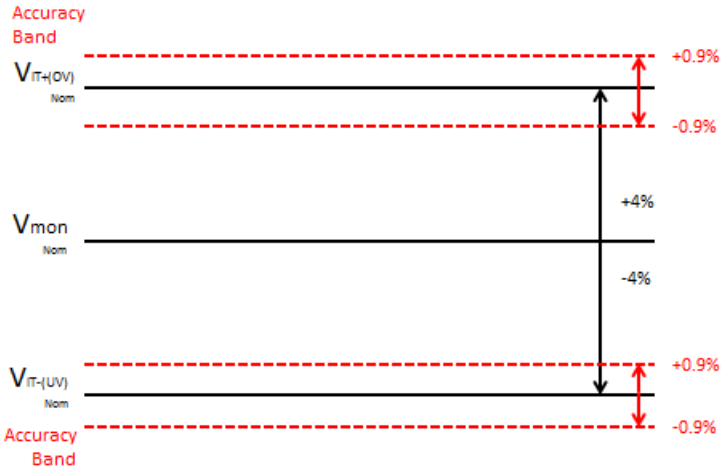

Figure 1: TPS3702 voltage thresholds

For more information on TPS3702 device selection, please refer to the Device Nomenclature section of the TPS3702 datasheet.

2.1.2 Pull Up Resistor Sizing for Current Consumption

The TPS3702 features open drain outputs that require a pull-up resistor from their output pins to the desired pull-up voltage. The pull-up resistance is typically in the range of 10 kΩ – 1 MΩ. Higher resistance keeps current consumption low. Take, for example, a resistor of 10k Ω pulled up to 3.3 V; when the signal is active there will be a current draw of 0.33 mA.

In this design, however, it is not expected that the signal will be active for long periods of time. Therefore, current consumption is not a pressing concern. Instead, 2.2 kΩ resistors were used resulting in a current draw of 1.5mA. This was done deliberately to boost immunity to noise. Due to concerns of electromagnetic interference, the current was increased to limit the chances of a false signal being read by the microcontroller.

2.1.3 Enabling an Interrupt

Both fault conditions, undervoltage and overvoltage, are monitored by the microcontroller. The undervoltage output signal is directly connected to the microcontroller's reset pin. The overvoltage output signal, on the other hand, is connected to a GPIO set up as an external interrupt. Another option is to launch a non-maskable interrupt when an overvoltage condition occurs. This can commence shutdown routines and hold the microcontroller in an internally initialized reset.

A sample code to initialize an external interrupt can be found in the appendix.

3 Component Selection

3.1 TPS3702

The TPS3702 is an integrated overvoltage and undervoltage window detector. It has high threshold accuracy (0.9% max) which facilitates proper resets. A SET pin, which can be pulled high or low, allows the user to change the width of the window, i.e. the overvoltage and undervoltage thresholds. It is also equipped with a built-in hysteresis to prevent oscillatory behavior on the rail from affecting the reset signal. Built-in glitch immunity prevents transient voltage spikes from triggering an unnecessary reset signal.

The TPS3702CX33 is used to monitor the 3.3 V rail. The SET pin is pulled high so the undervoltage and overvoltage thresholds correlate to a ±4% window. There is a 0.55% nominal hysteresis associated with both the undervoltage and overvoltage thresholds.

The TPS3702CX12 is used to monitor the 1.2 V rail. The SET pin is pulled high so the undervoltage and overvoltage thresholds correlate to a ±4% window. There is a 0.55% nominal hysteresis associated with both the undervoltage and overvoltage thresholds.

For more information on TPS3702 device selection, please refer to the Device Nomenclature section of the TPS3702 datasheet.

3.2 TMS320F28377D Delfino™ Microcontroller

The Delfino™ TMS320F2837xD is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications such as industrial drives and servo motor control; solar inverters and converters; digital power; transportation; and power line communications.

3.3 TPS62420

The TPS62420 is DC/DC converter that generates two voltage rails. It has independent enable pins for each channel which are necessary to achieve the required power up sequence for the microcontroller. It also features a power save mode at light current loads and an easy scale interface function which can change the output voltage of either rail through a serial interface. It operates at 95% peak efficiency.

4 Simulation

No TINA simulations were generated for this project.

4.1 Timing Diagram

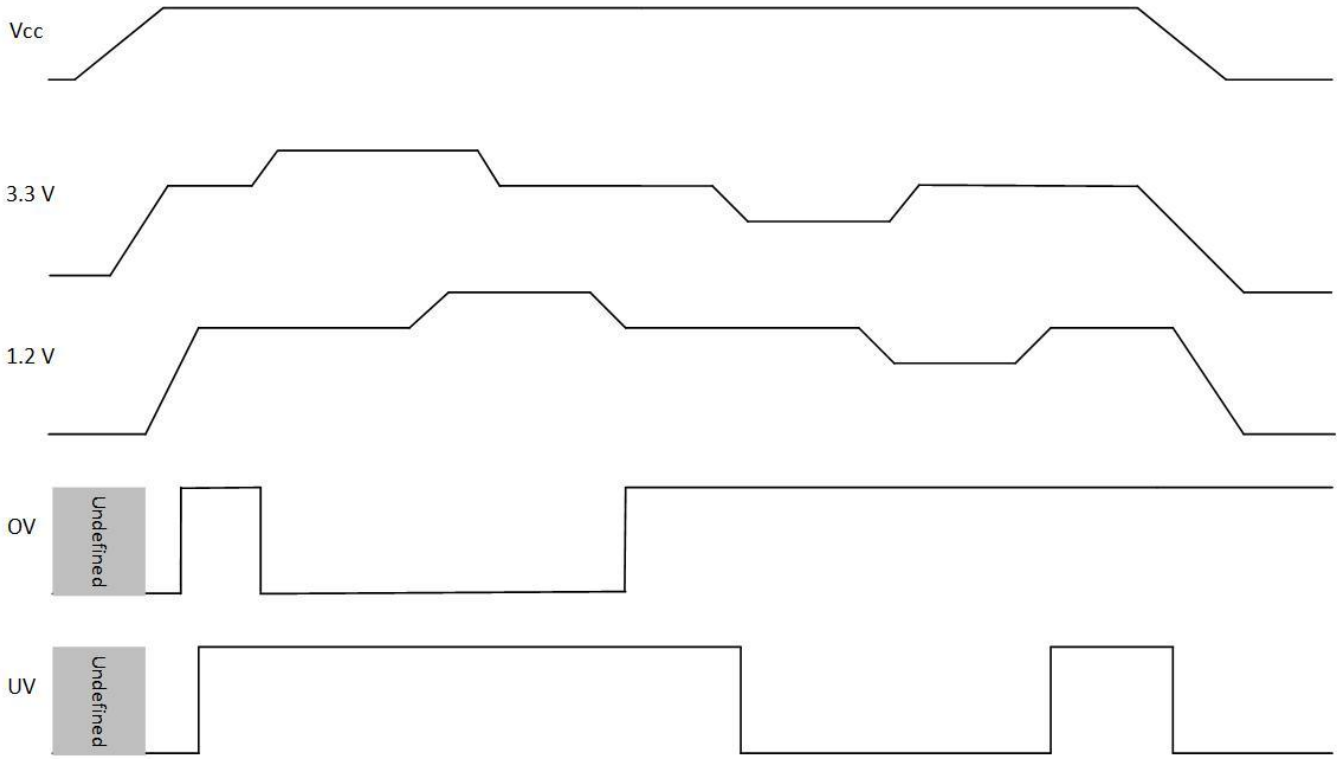

Figure 2: System timing diagram

4.2 Block Diagram

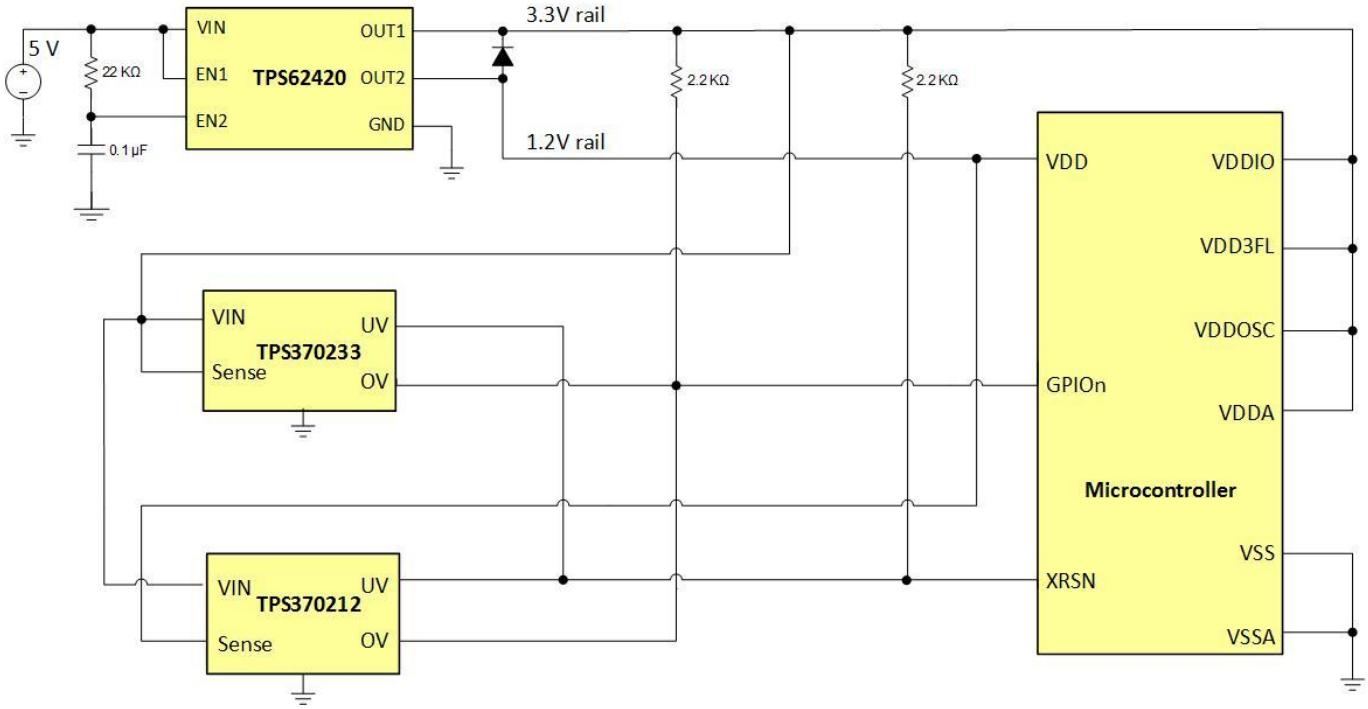

Figure 3: Block diagram showing UV and OV detection

5 Measurements and Verification

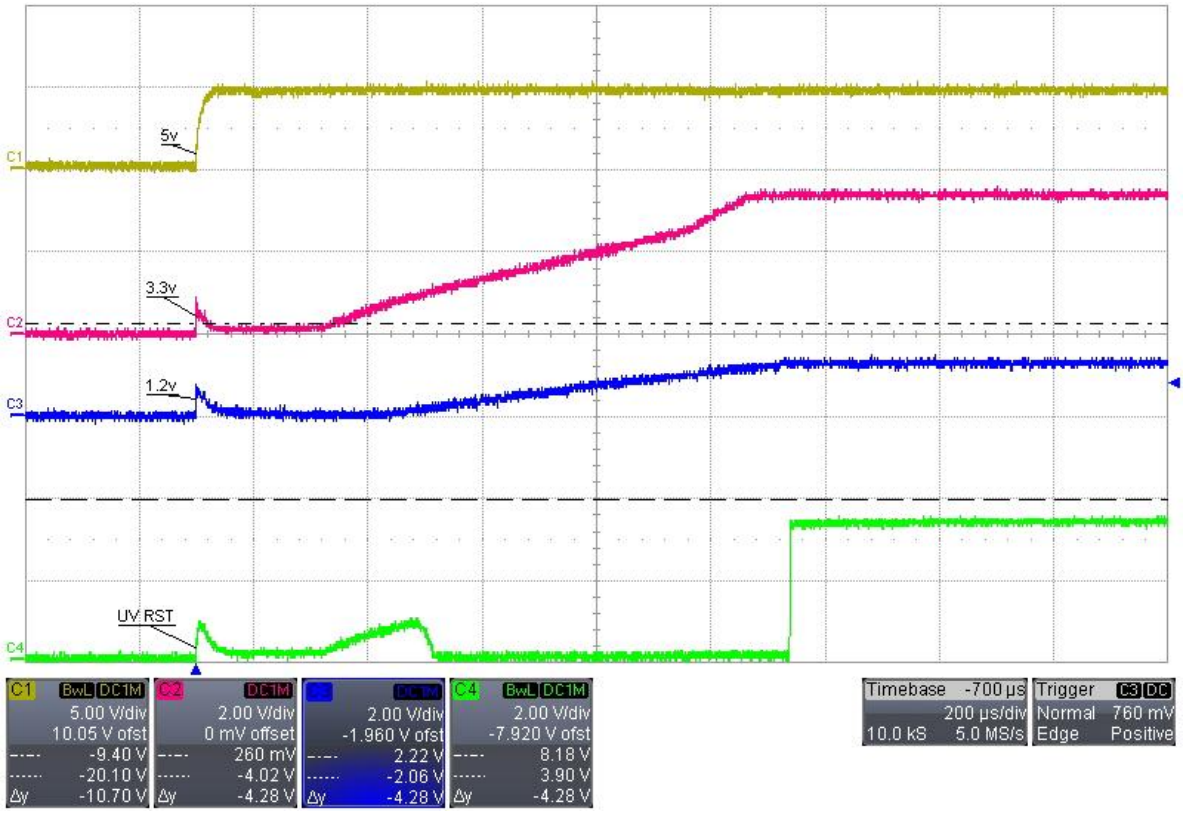

Figure 4: Start-Up

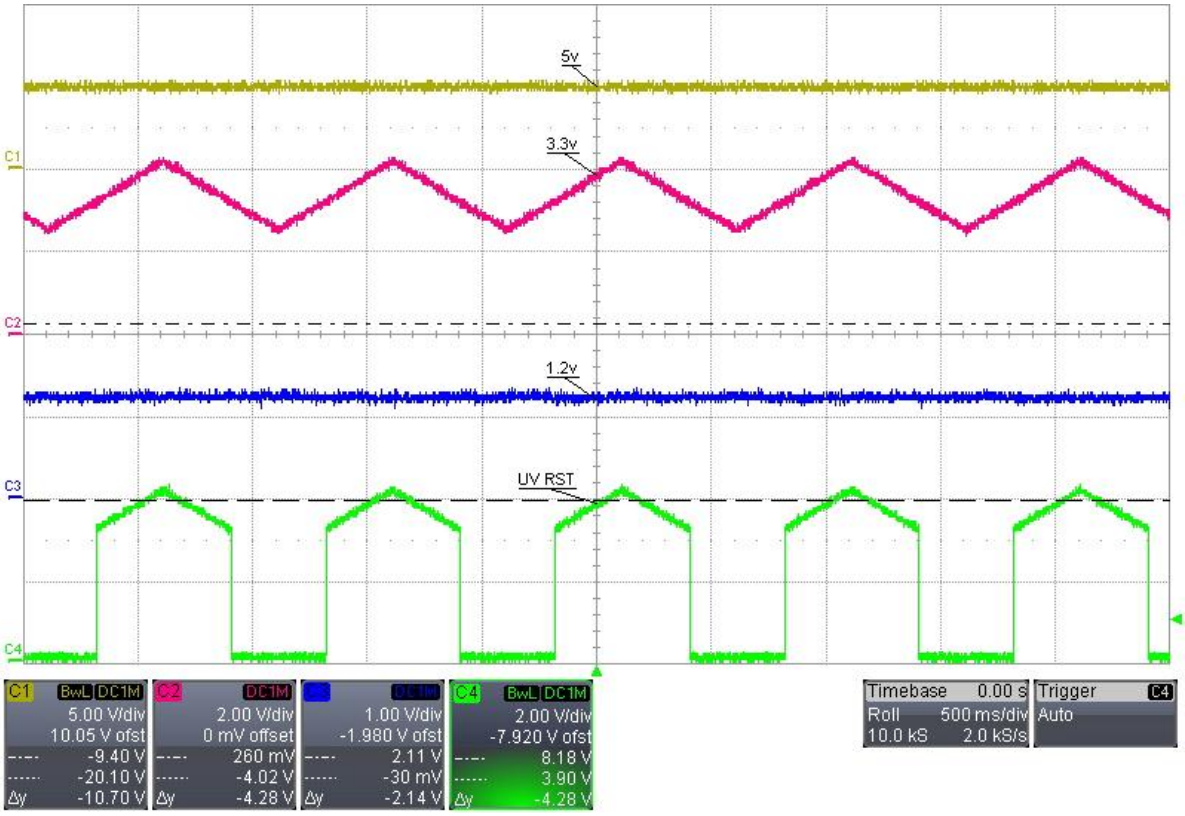

Figure 5: Reset asserted for an undervoltage fault on the 3.3 V rail

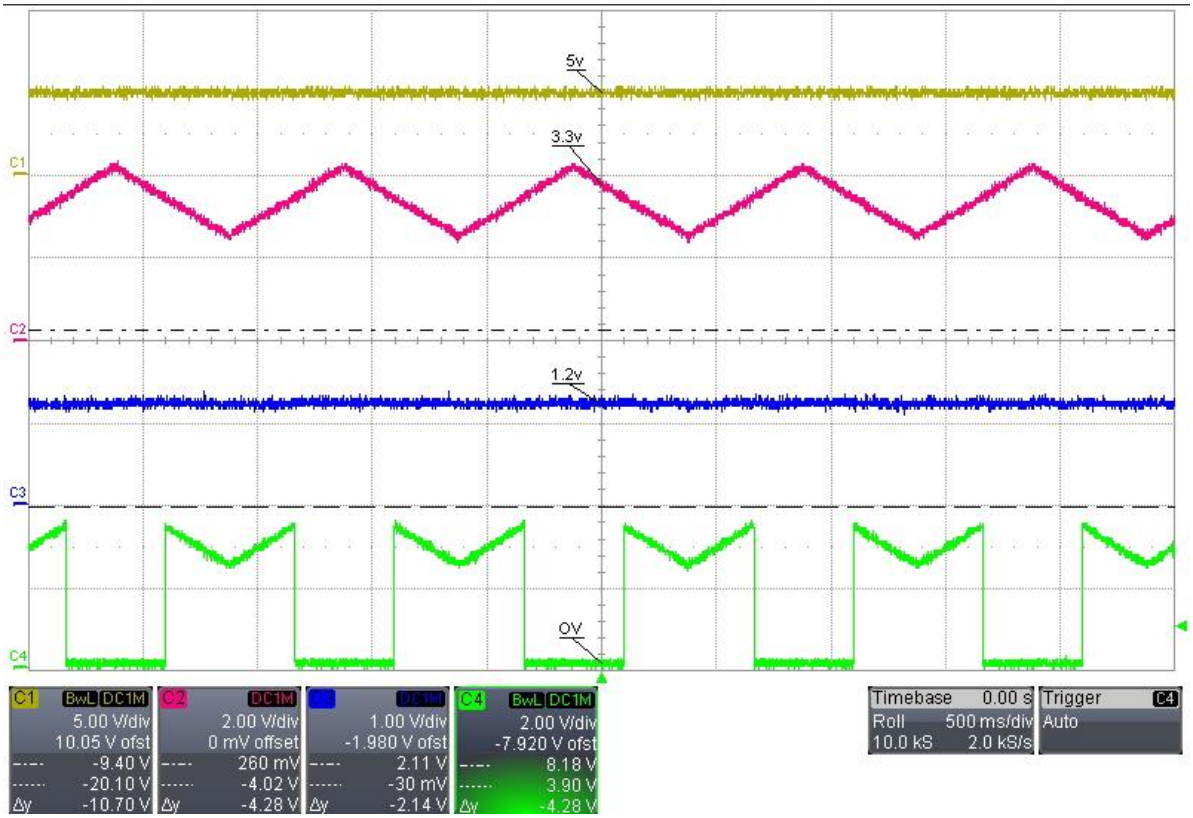

Figure 6: Reset asserted for an overvoltage fault on the 3.3 V rail

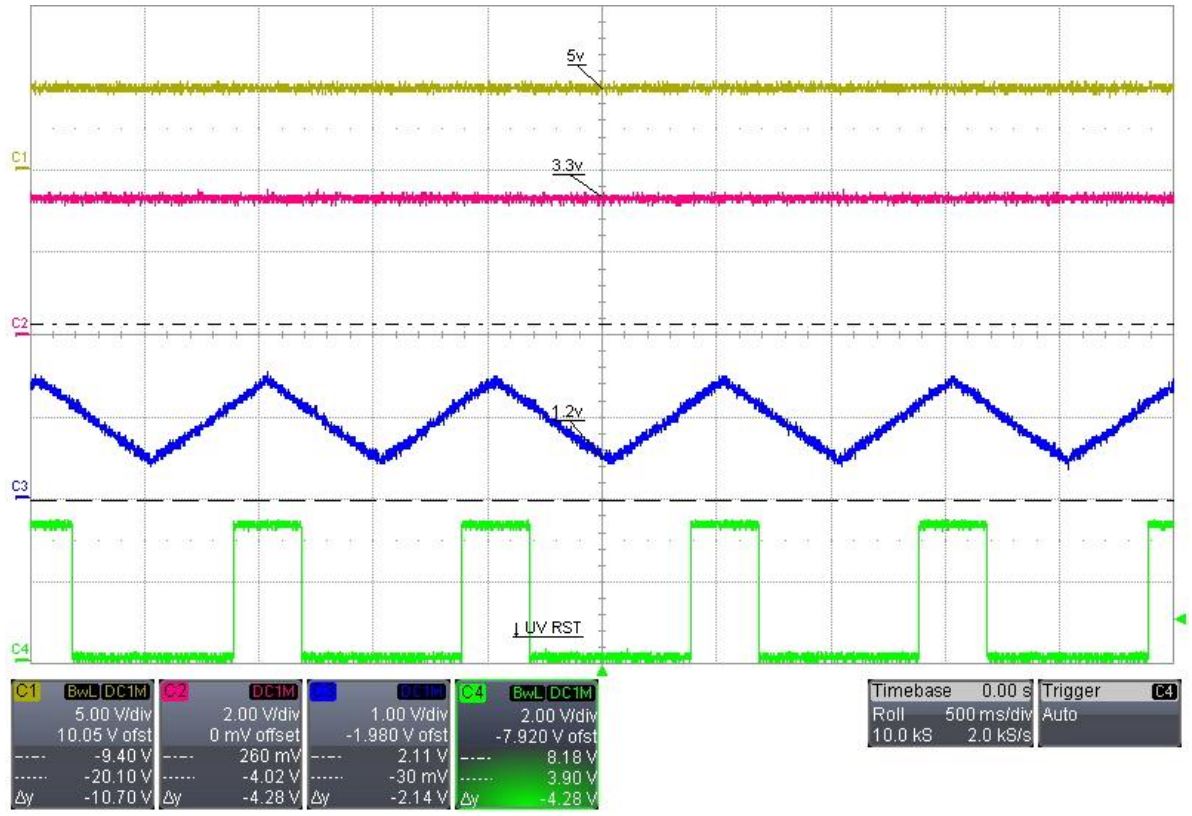

Figure 7: Reset asserted for an undervoltage fault on the 1.2 V rail

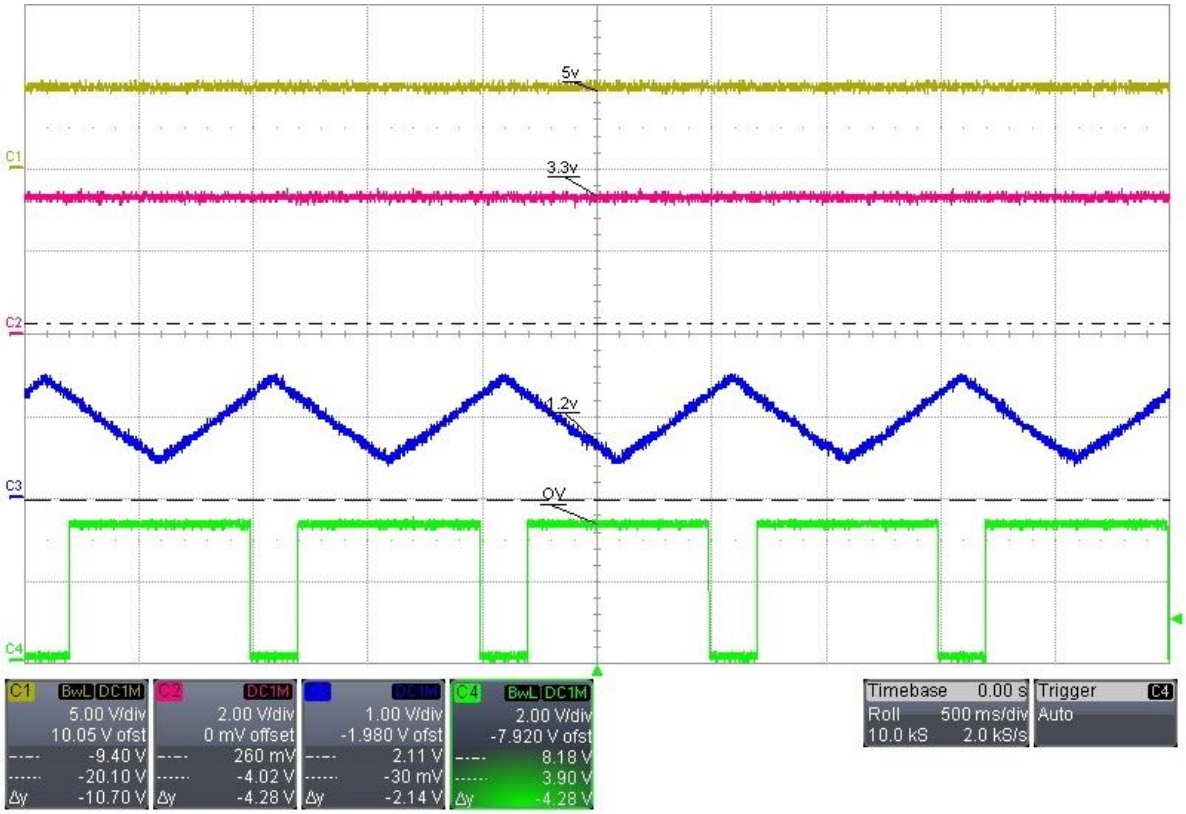

Figure 8: Reset asserted for an overvoltage fault on the 1.2 V rail

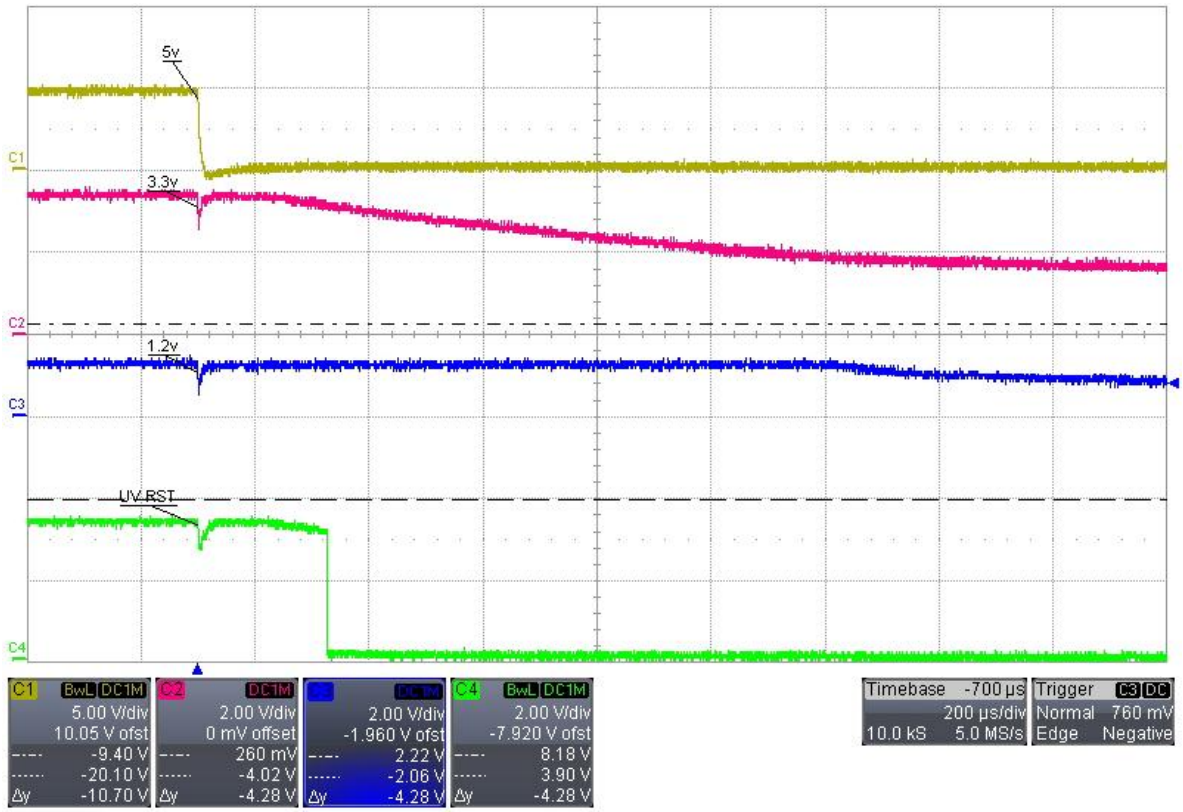

Figure 9: Shut-down

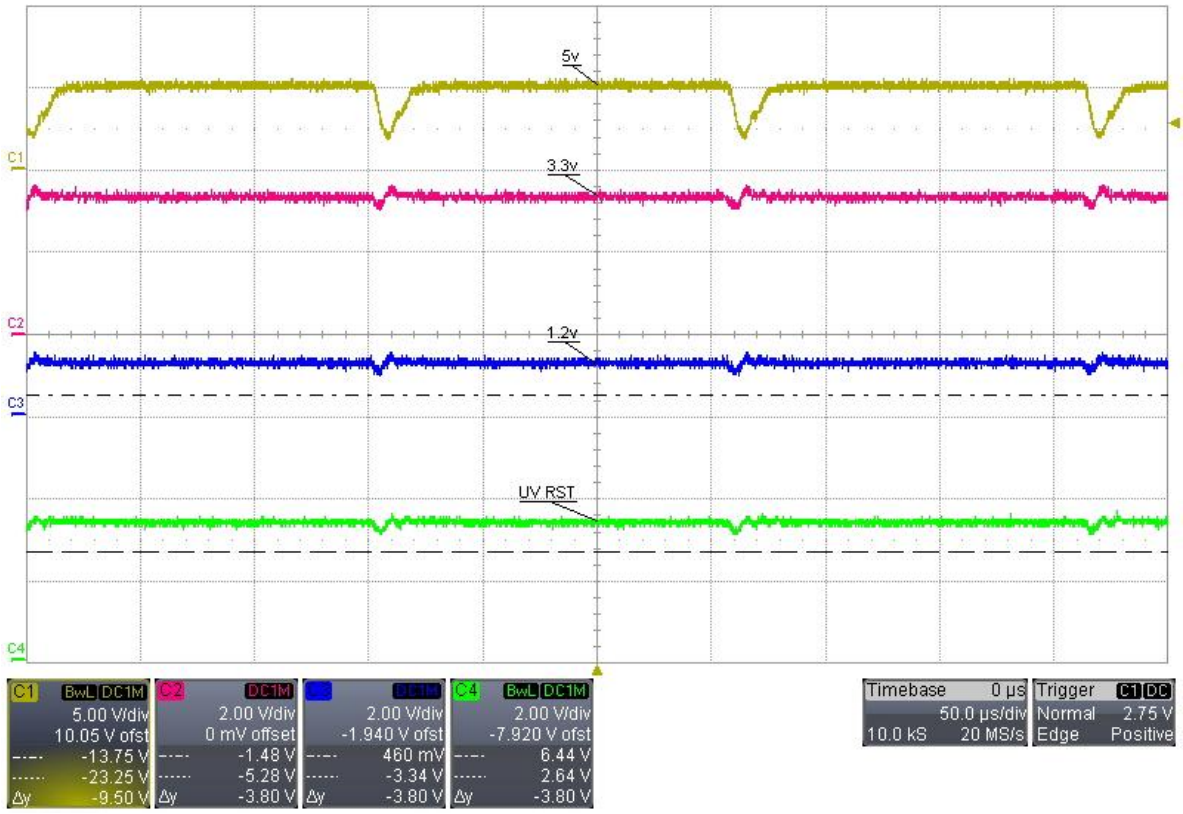

Figure 10: Brownout condition – 5 V input voltage dropping to 2.4 V for 10 µs

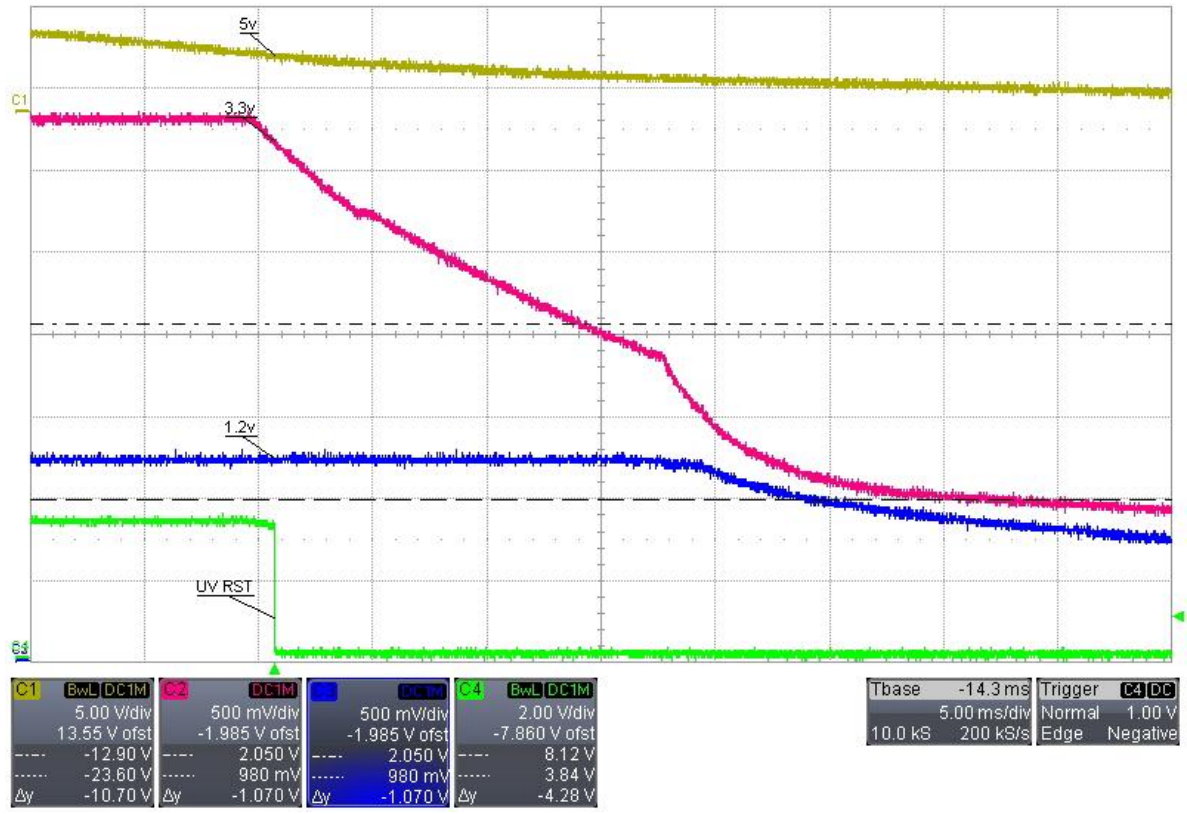

Figure 11: Slow shut down with diode maintaining bias between 3.3 V and 1.2 V rails

6 About the Author

Cynthia Sosa is an Applications Engineer in the Linear Power business unit since she joined TI. She received her BSEE from the University of Texas at El Paso.

7 Acknowledgements & References

1. TPS3702 Datasheet
2. TMS320F28377D Datasheet
3. TMS320F2837xD Technical Reference Manual
4. TPS62420 Datasheet

I would like to thank Brett Larimore and his team for their immense knowledge and William Stevers for his immense support. Also to my own team members, especially Kyle Van Renterghem for being so willing to take on this project and all that came with it.

Appendix A.

A.1 Schematic

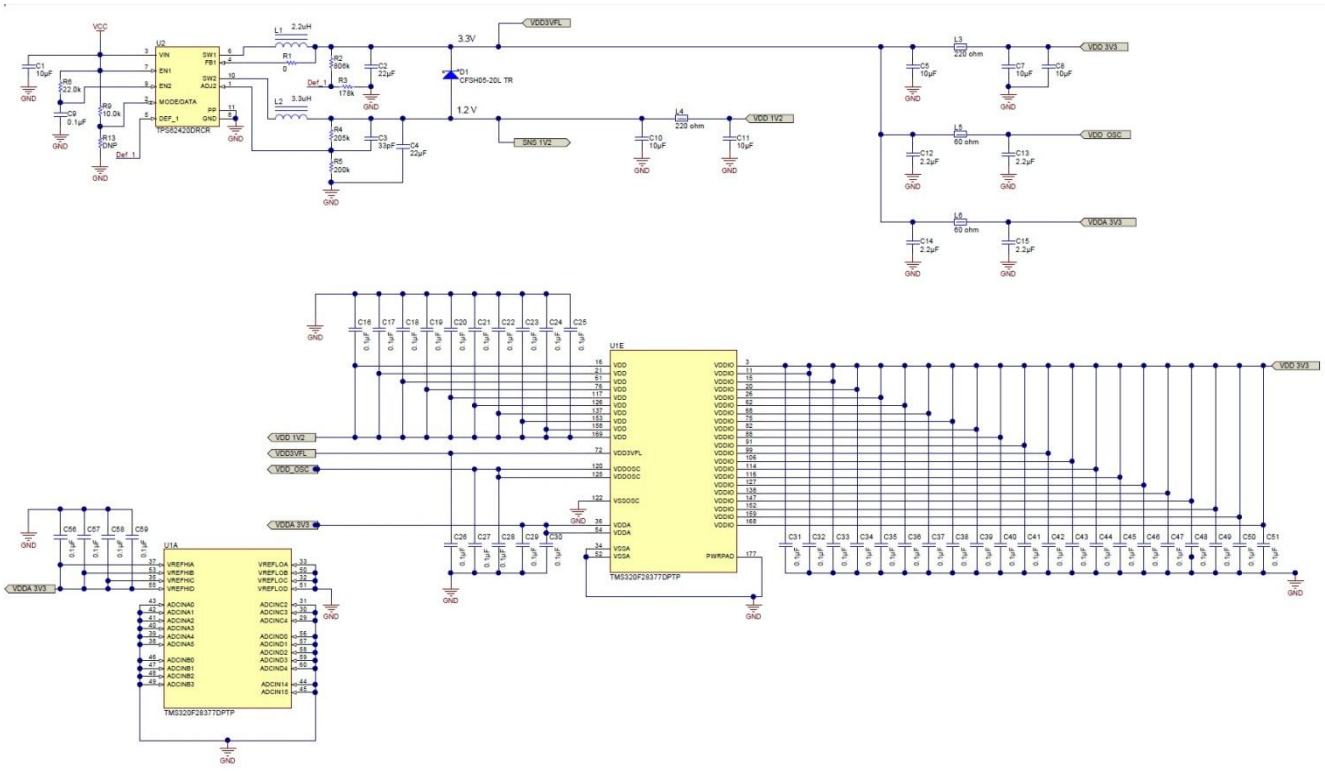

Figure A-1: Page 1 of electrical schematic

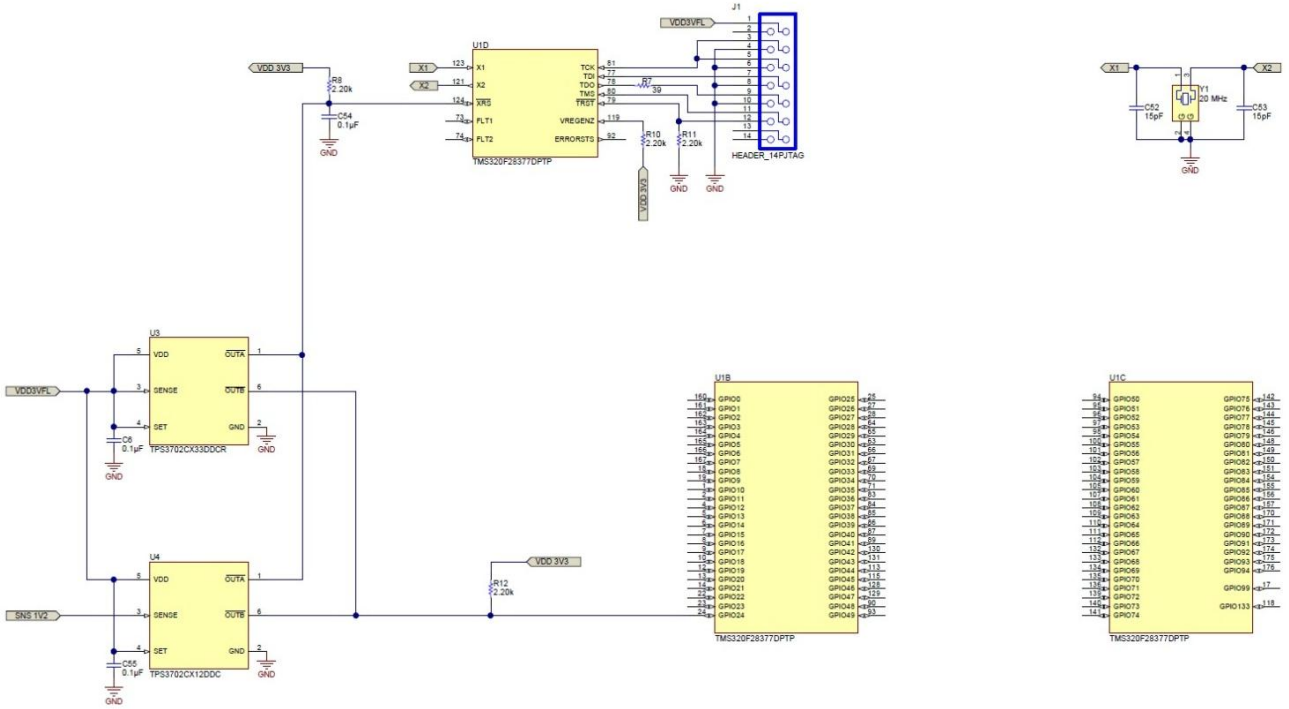

Figure A-2: Page 2 of electrical schematic

A.2 Sample Test Code

```
// FILE:   OverVoltageInterrupt.c

// TITLE:  Soprano Example External Interrupt Test Program.

// This program sets up GPIO0 as XINT1.  A GPIO signal is used to trigger the interrupt

// GPIO30 triggers XINT1, jumper this two pins together

// User needs to externally connect these pins for the program to work properly.

// XINT1 input is synced to SYSCLKOUT.

// When the ISR is triggered, it will flag OverVoltageFlag to 1 (default is 0)

// The interrupt is only fired once -- if ResetOverVoltageISR is set to 1 in the // watch window (the default), // the OverVoltageFlag will clear and the ISR will // be reenabled.

// ResetOverVoltageISR (default 1) activates the ISR if set to 0, resets ISR when set to 1.  0 simulates the desired fail condition.

//////////////////////////////////////////////////////////

#include "F28x_Project.h"     // Device Headerfile and Examples Include File

interrupt void xint1_isr(void);  // Prototype statements for functions found // // within this file.

// Global variables for this example

volatile Uint32 Xint1Count;

Uint32 LoopCount,OverVoltageFlag,ResetOverVoltageISR;


void main(void)

{

  InitSysCtrl()              // Initialize System Control:

  DINT;                      // Disable CPU interrupts

// Initialize PIE control registers to their default state, all PIE interrupts disabled and flags  are cleared.

  InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:

  IER = 0x0000;

  IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell Interrupt

// Service Routines (ISR).

  InitPieVectTable();
```

```
// Interrupts that are used in this example are re-mapped to ISR functions found within this file.
   EALLOW;                          // This is needed to write to EALLOW protected registers
   PieVectTable.XINT1_INT = &xint1_isr;
   EDIS;                            // This is needed to disable write to EALLOW protected registers

// User specific code, enable interrupts:
// Clear the variables
   Xint1Count = 0;          // Count XINT1 interrupts, used with resetISR to limit the number of ISR calls to     //
one per "over-voltage" event
   OverVoltageFlag = 0;     // ISR flag (default is 0)
   ResetOverVoltageISR = 1;

// Enable XINT1 in the PIE: Group 1 interrupt 4
// Enable INT1 which is connected to WAKEINT:
   PieCtrlRegs.PIECTRL.bit.ENPIE = 1;          // Enable the PIE block
   PieCtrlRegs.PIEIER1.bit.INTx4 = 1;          // Enable PIE Group 1 INT4
   IER |= M_INT1;                       // Enable CPU INT1
   EINT;                               // Enable Global Interrupts

// GPIO0 is an input
   EALLOW;
   GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 0;         // GPIO
   GpioCtrlRegs.GPADIR.bit.GPIO0 = 0;          // input
   GpioCtrlRegs.GPAQSEL1.bit.GPIO0 = 0;        // XINT1 Synch to SYSCLKOUT only
   EDIS;

// GPIO30 is an output, starts high
   EALLOW;
   GpioDataRegs.GPASET.bit.GPIO30 = 1;         // Load the output latch (high)
   GpioCtrlRegs.GPAMUX2.bit.GPIO30 = 0;        // GPIO
   GpioCtrlRegs.GPADIR.bit.GPIO30 = 1;         // output
   EDIS;
```

```
// GPIO0 is XINT1
   GPIO_SetupXINT1Gpio(0);

// Configure XINT1
   XintRegs.XINT1CR.bit.POLARITY = 0;          // Falling edge interrupt

// Enable XINT1
   XintRegs.XINT1CR.bit.ENABLE = 1;

   while(1)
   {
  LoopCount++;
 // ResetOverVoltageISR can be set in the watch window
  if(OverVoltageFlag == 1 && ResetOverVoltageISR == 1)
  {
            OverVoltageFlag = 0;
            GpioDataRegs.GPASET.bit.GPIO30 = 1;                    // raise GPIO30 (disabling ISR)
       PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;                    // reenable interrupt
  }
  else if(ResetOverVoltageISR == 0)
  {
            GpioDataRegs.GPACLEAR.bit.GPIO30 = 1;
            // take GPIO0 low, triggers ISR (this simulates the "over-voltage" condition)
  }
   }
}

// Insert all local Interrupt Service Routines (ISRs) and functions here:
// If local ISRs are used, reassign vector addresses in vector table
interrupt void xint1_isr(void)
{
  Xint1Count++;          // counts the number of ISR triggers-- the ISR should ONLY be triggered when an   //
"over-voltage" is detected
```

```
 OverVoltageFlag = 1;    // flags the "over-voltage" condition
 // User specific requirements to correct the condition would be placed here
}
```

A.3 Test and Measurements

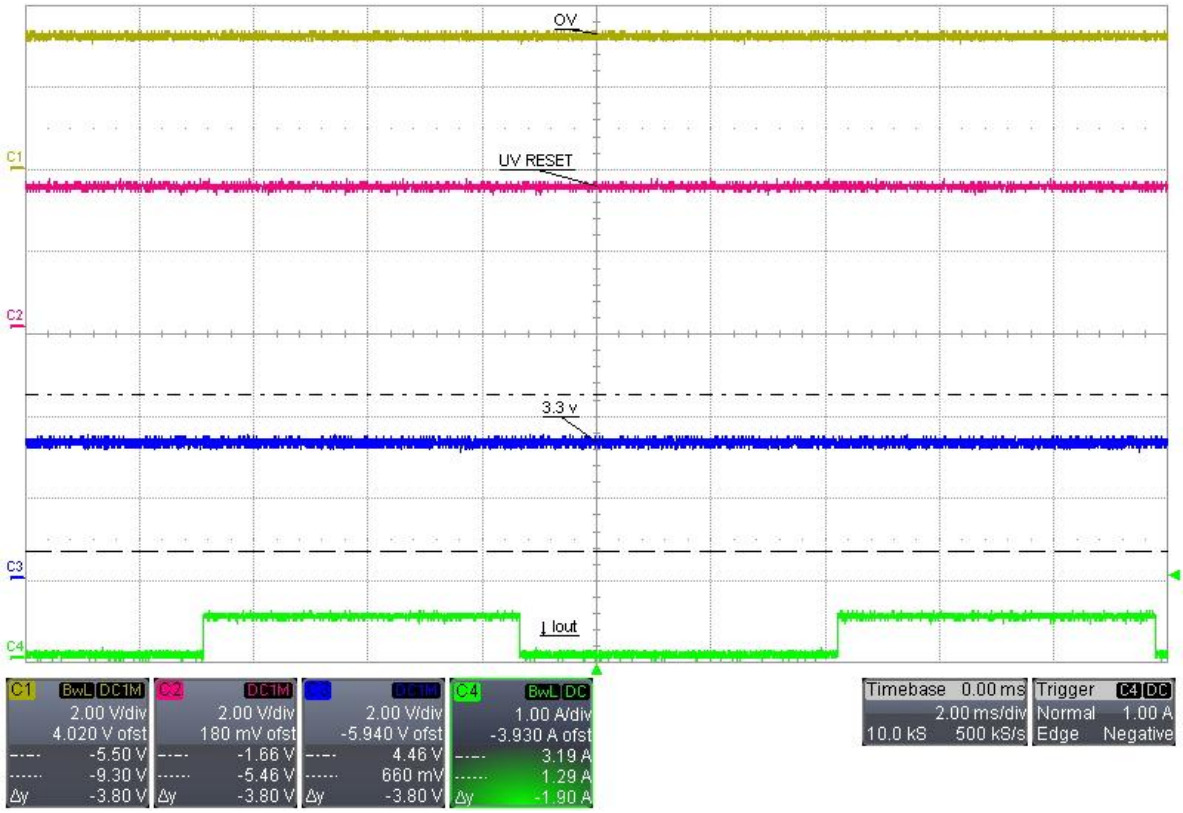

Figure A-3: Load Transient Response – 0 mA to 500 mA on 3.3 V rail

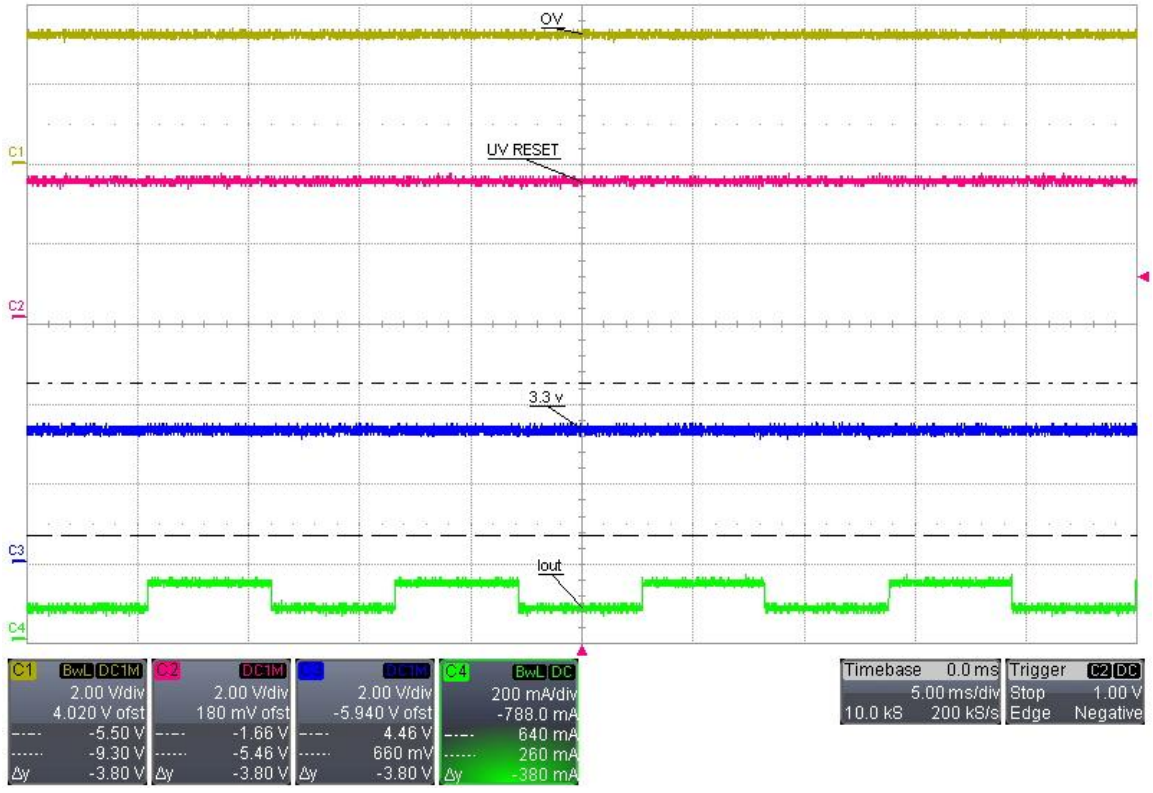

Figure A-4: Load Transient Response – 77 mA to 140 mA on 3.3 V rail

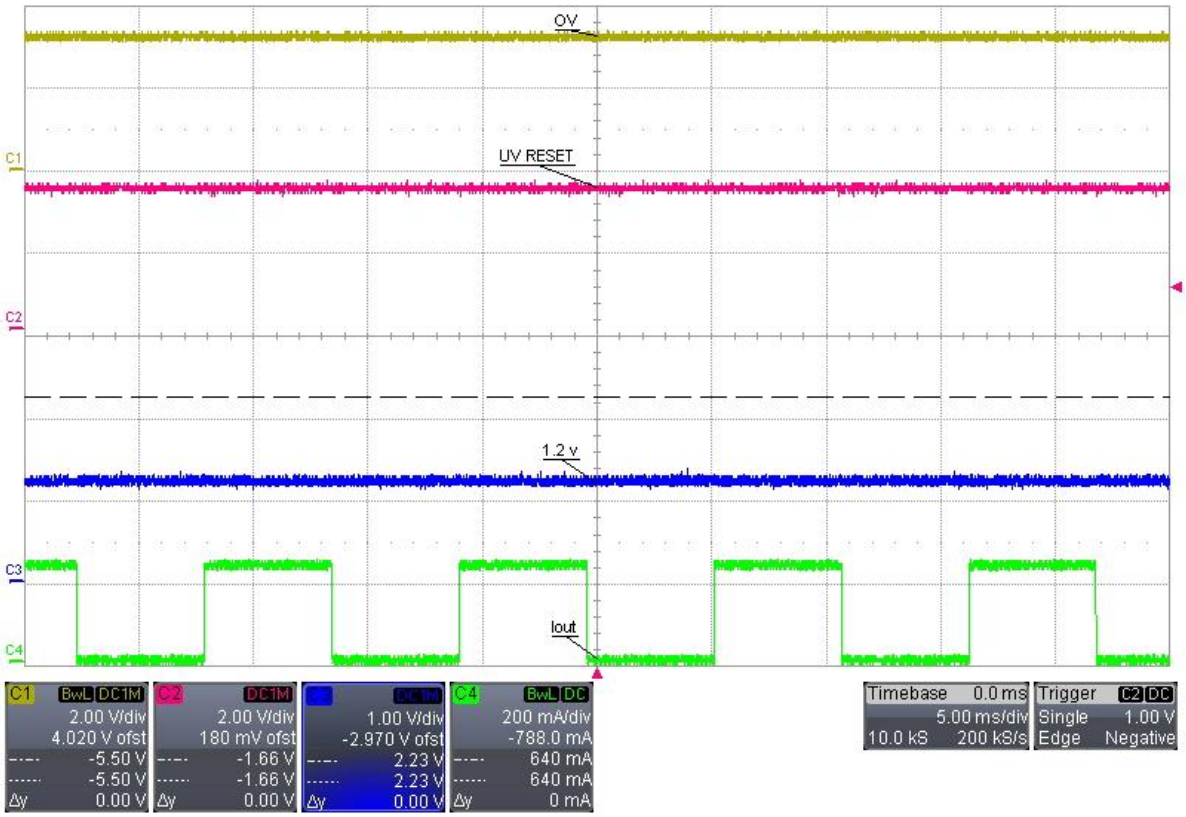

Figure A-5: Load Transient Response – 0 mA to 250 mA on 1.2 V rail

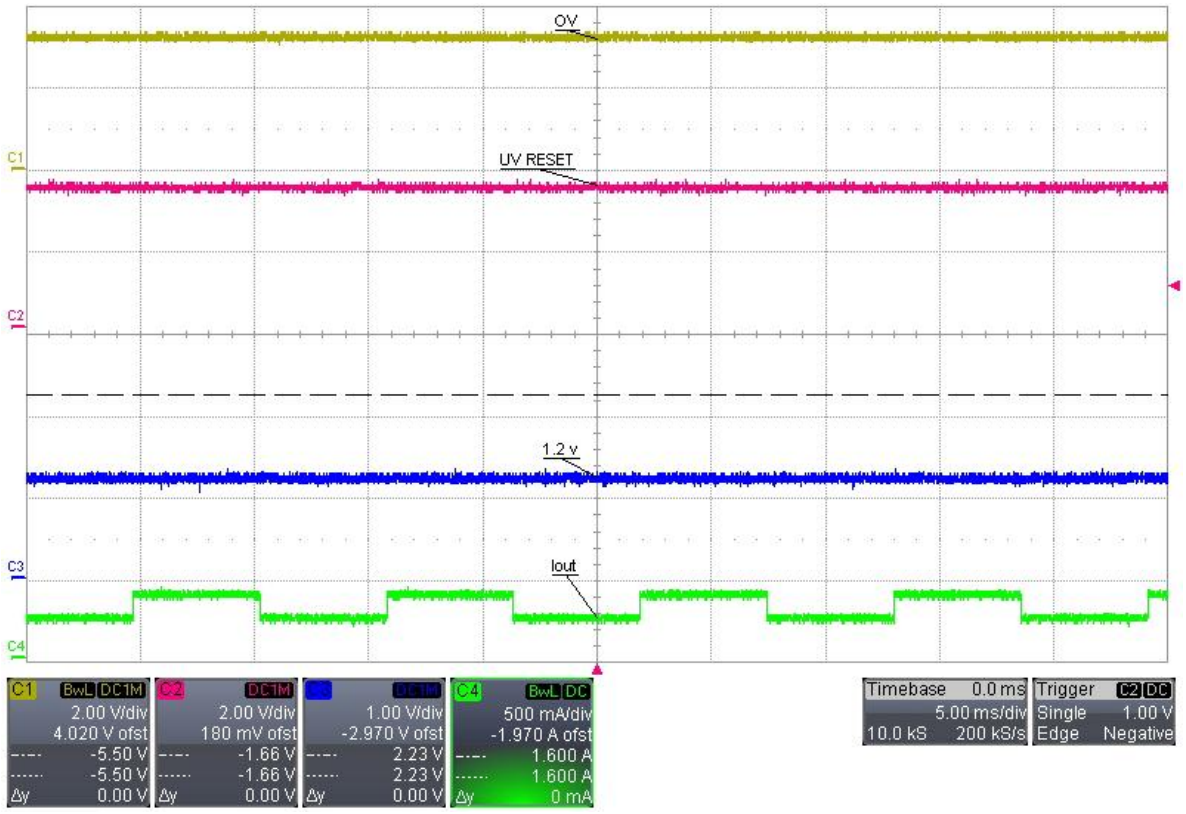

Figure A-6: Load Transient Response – 250 mA to 400 mA on 1.2 V rail.

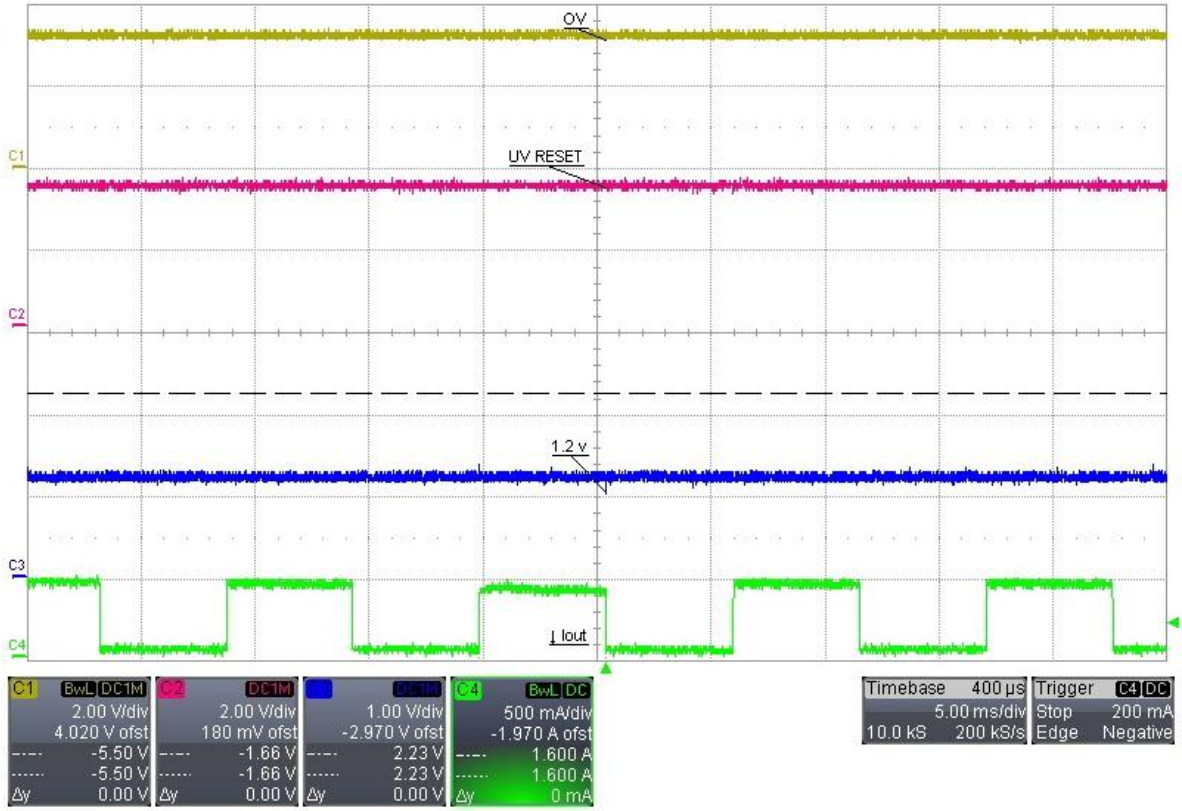

Figure A-7: Load Transient Response – 30 mA to 480 mA on 1.2 V rail

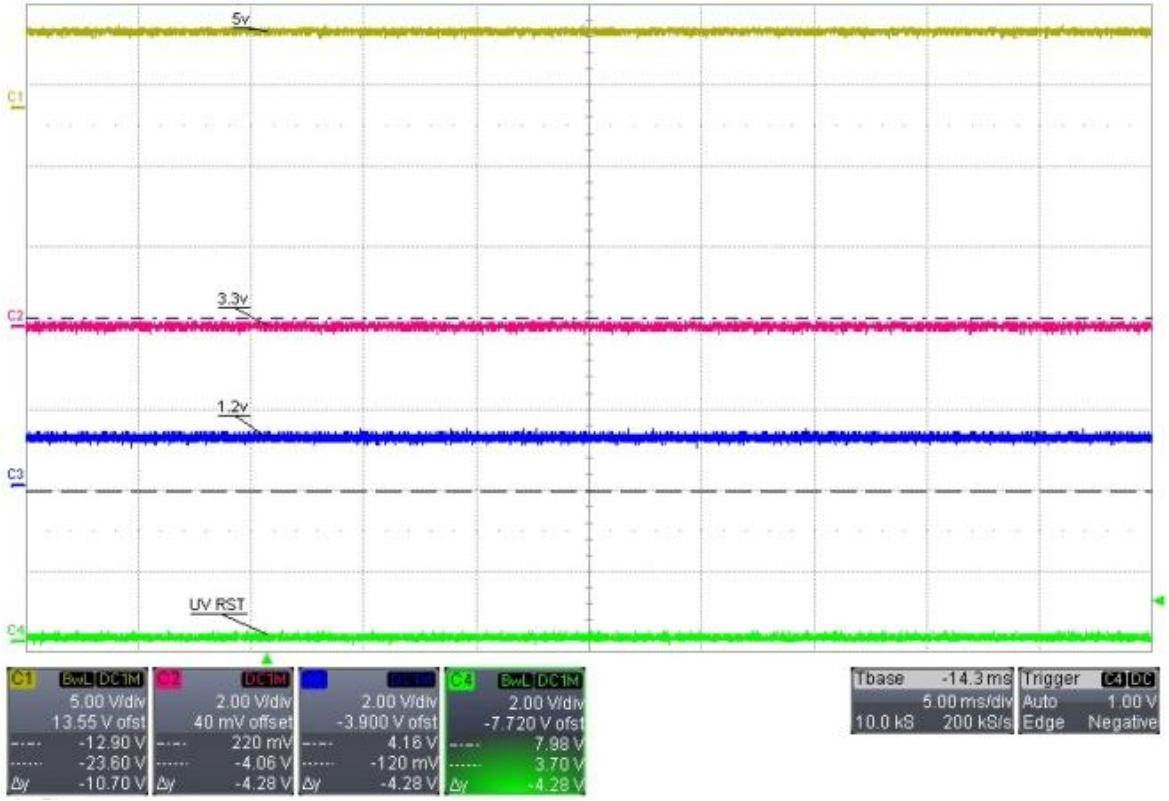

Figure A-8: Reset asserted while 3.3V rail is low and 1.2V rail is high

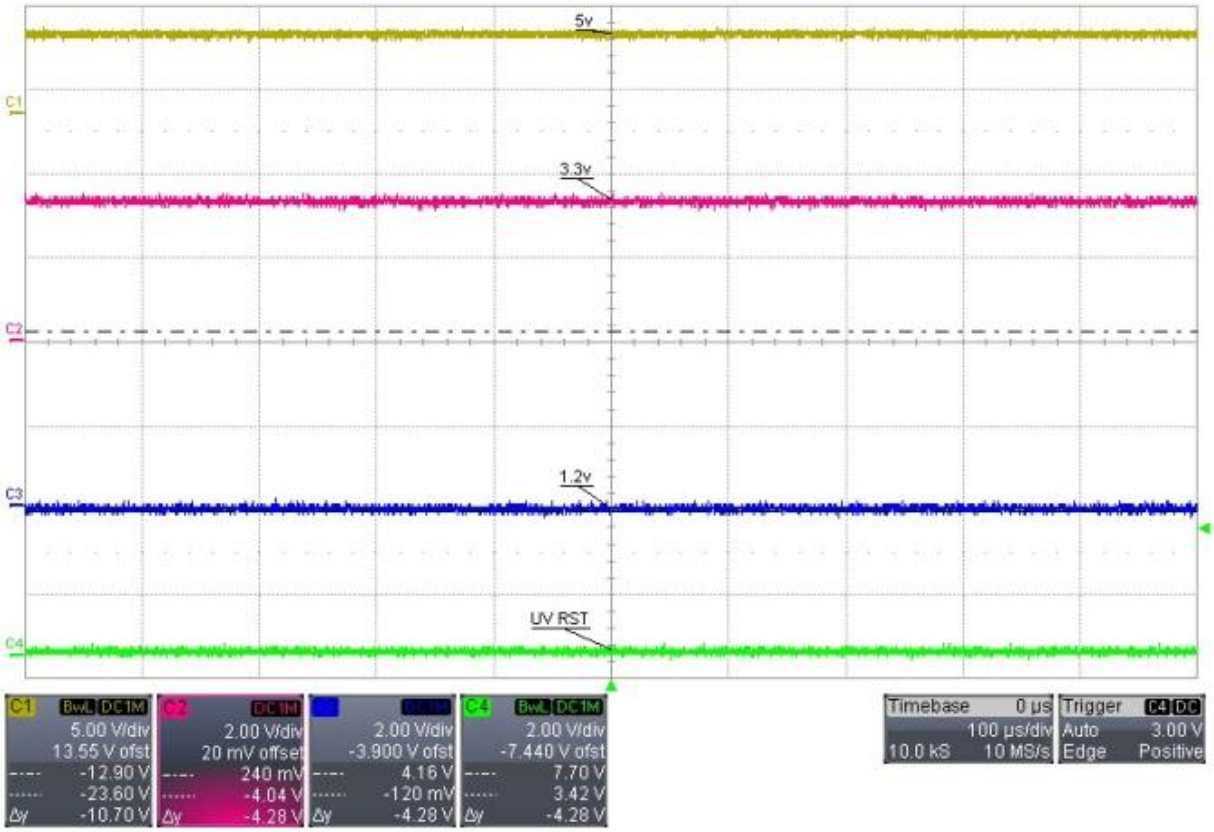

Figure A-9: Reset asserted while 3.3V rail is high and 1.2V rail is low

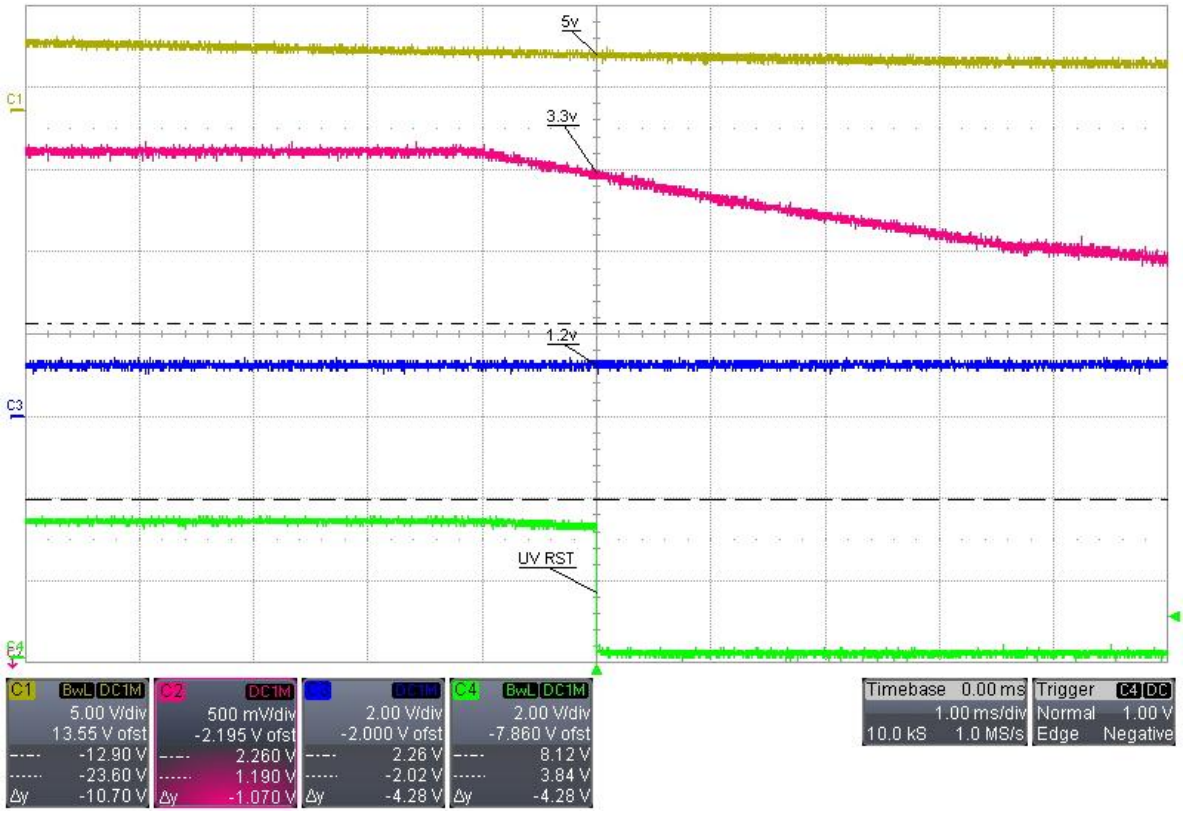

Figure A-10: Displaying how low 3.3V rail reaches until reset is asserted.

Appendix B.

B.1 Bill of Materials

Texas Instruments

Bill of Materials

TI DESIGNS

TIDA-00392

Item	Qty	Reference	Value	Part Description	Manufacturer	Manufacturer Part Number	Alternate Part	PCB Footprint
1	6	C1, C5, C7, C8, C10, C11	10 µF	CAP, CERM, 10 µF, 25 V, +/- 20%, X5R, 0603	TDK	C1608X5R1E106M080AC		C1608X5R1E106M080AC
2	2	C2, C4	22 µF	CAP, CERM, 22 µF, 10 V, +/- 20%, X5R, 0603	TDK			
3	1	C3	33 pF	CAP, CERM, 33 pF, 100 V, +/- 5%, C0G/NP0, 0603	AVX	06031A330JAT2A		06031A330JAT2A
9	44	C6, C9, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C54, C55, C56, C57, C58, C59	0.1 µF	CAP, CERM, 0.1 µF, 16 V, +/- 20%, X7R, 0603	Kemet	C0603C104M4RACTU		C0603C104M4RACTU
10	4	C12, C13, C14, C15	2.2 µF	CAP, CERM, 2.2 µF, 25 V, +/- 10%, X5R, 0402	TDK	C1005X5R1E225K050BC		C1005X5R1E225K050BC
11	2	C52, C53	15 pF	CAP, CERM, 15 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H150JA01D		GRM1555C1H150JA01D
12	1	D1		Diode, Schottky, 20 V, 0.5 A, 1.0x0.35x0.6mm	Central Semiconductor	CFSH05-20L CT-ND		CFSH05-20L TR
13	1	J1		Header, 2x7 pin, 100mil spacing, Straight, 4 Wall	3M	2514-6002UB		HEADER_14PJTAG
14	1	L1	2.2 µH	Inductor, Drum Core, Ferrite, 2.2 µH, 1 A, 0.11 ohm, SMD	Bourns	SRU2016-2R2Y		SRU2016-2R2Y
15	1	L2	3.3 µH	Inductor, Drum Core, Ferrite, 3.3 µH, 0.6 A, 0.32 ohm, SMD	Bourns	SRU2009-3R3Y		SRU2009-3R3Y
16	2	L3, L4	220 ohm	Ferrite Bead, 220 ohm @ 100 MHz, 0.2 A, 0402	MuRata	BLM15BB221SN1D		BLM15BB221SN1D
17	2	L5, L6	60 ohm	Ferrite Bead, 60 ohm @ 100 MHz, 3.5 A, 0603	TDK	MPZ1608S600A		MPZ1608S600A
18	1	R1	0	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED		CRCW04020000Z0ED
19	1	R2	806 k	RES, 806 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805806KFKEA		CRCW0805806KFKEA
20	1	R3	178 k	RES, 178 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805178KFKEA		CRCW0805178KFKEA
21	1	R4	205 k	RES, 205 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805205KFKEA		CRCW0805205KFKEA
22	1	R5	200 k	RES, 200 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805200KFKEA		CRCW0805200KFKEA
23	1	R6	22.0 k	RES, 22.0 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0722KL		RC0603FR-0722KL
24	1	R7	39	RES, 39, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040239R0JNED		CRCW040239R0JNED
25	4	R8, R10, R11, R12	2.20 k	RES, 2.20 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-072K2L		RC0603FR-072K2L
26	1	R9	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040210K0FKED		CRCW040210K0FKED
27	0	R13	DNP	RES, 5%, 0.063 W, 0402		CRCW040210K0FKED		CRCW040210K0FKED
28	1	U1		Dual-Core Delfino Microcontroller, PTP0176F	Texas Instruments	TMS320F28377DPTP		TMS320F28377DPTP
29	1	U2		Buck Adjustable Regulator with 2.5 to 6 V Input and 0.6 to 6 V Output	Texas Instruments	TPS62420DRCR		TPS62420DRCR
30	1	U3		High-Accuracy, Fixed-Threshold OV/UV Monitor, DDC0006A	Texas Instruments	TPS3702CX33DDCR		TPS3702CX33DDCR
31	1	U4		High Accuracy Fixed Threshold OV/UV Monitor, DDC0006A	Texas Instruments	TPS3702CX12DDC		TPS3702CX10DDC
32	1	Y2		Crystal, 20 MHz, 10 pF, SMD	Abracon Corportation	ABM3B-20.000MHZ-10-1-U-T		ABM3B-20.000MHZ-10-1-U-T

Figure B-1: Bill of Materials

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