TI Designs

Power Sequencing for the 66AK2E0x and AM5K2E0x Using the UCD9090 Design Guide

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

K2EVM	K2 EVM Information
66AK2E05	Product Folder
66AK2E02	Product Folder
AM5K2E04	Product Folder
AM5K2E02	Product Folder
UCD9090	Product Folder

Circuit Description

The UCD9090 10-Channel Sequencer and System Health Monitor can sequence power-supply rails for the 66AK2E0x and AM5K2E0x SoCs. The UCD9090 also monitors the voltage levels of the power supplies. If a power supply fails, the remaining power supplies can be shut down.

TI E2E™ Community

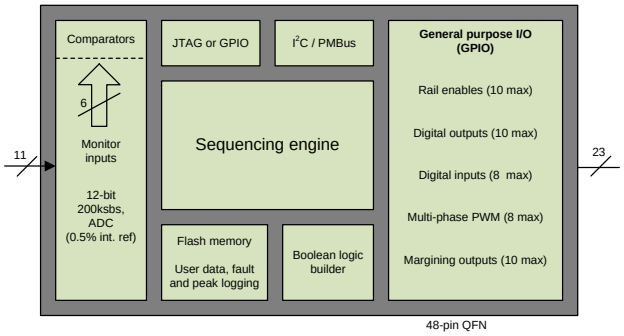
ASK Our E2E Experts
WEBENCH® Calculator Tools

Design Features

- Sequences 10 Individual Power Supplies

Featured Applications

- Compatible With Any KeyStone or KeyStone II Design



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 Design Summary

The 66AK2E0x and AM5K2E0x SoCs require that the supply voltages be sequenced for initialization. For details on the voltages and the sequence order, see *66AK2E0x Multicore DSP+ARM KeyStone II System-on-Chip (SoC)* (SPRS865D) and *AM5K2E0x Multicore ARM KeyStone II System-on-Chip (SoC)* (SPRS864D). The UCD9090 device sequences and monitors up to 10 power supplies. This design shows sequencing control using the UCD9090 device. For the full power tree for the XEVMK2EX design, see Figure 1.

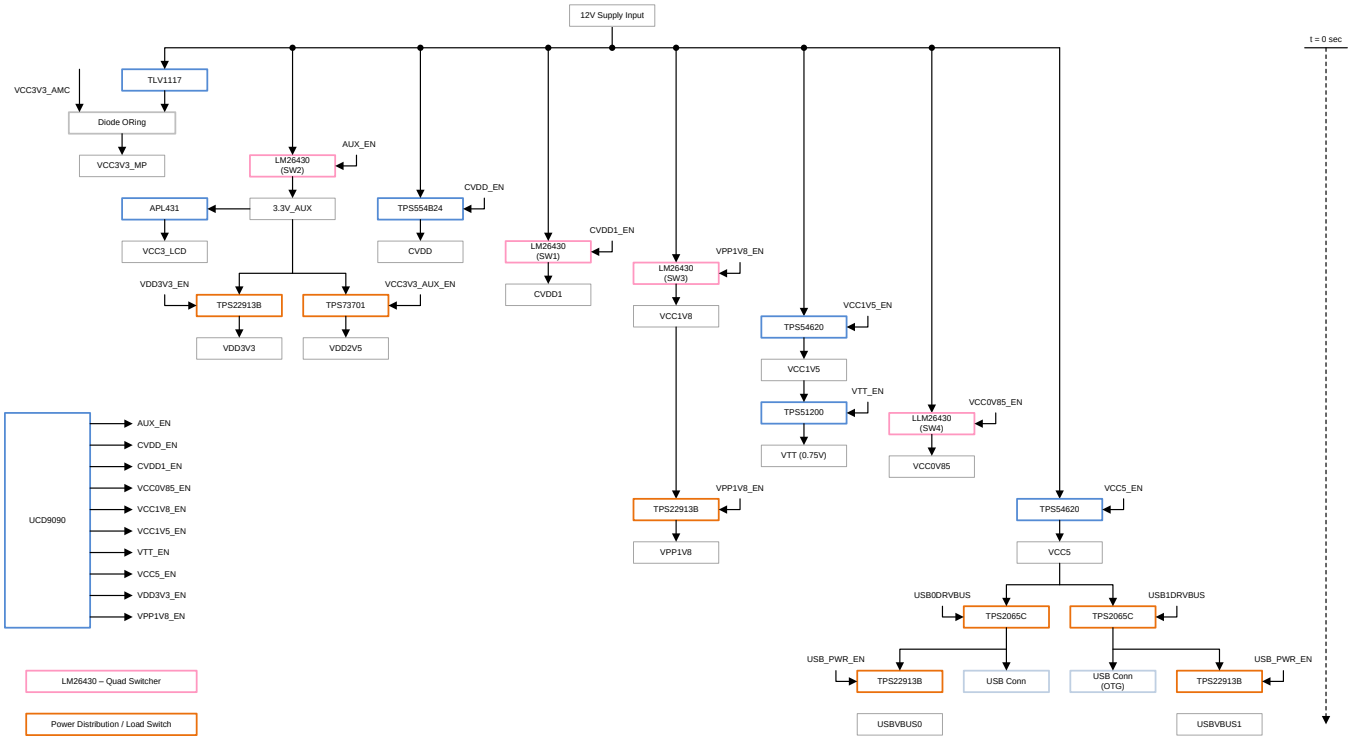


Figure 1. Power Tree for the XEVMK2EX Design

1.1 Introduction to the UCD9090

The UCD9090 device can monitor and enable up to 10 power supplies in a programmed sequence. The device includes 10 analog inputs connected to ADCs that monitor the voltage levels of power supply. The analog inputs provide 12 bits of accuracy from 0 to 2.5 V. The device has twenty-one GPIOs which are programable as inputs or outputs. These GPIOs can perform stem-level functions such as external interrupts, power-good, resets, or rail enables. When configured as a rail enable, you can sequence GPIOs up or down and program them as active-high, active-low, or open-drain. The sequencing engine can generate a user-defined sequence of rail enables. You can use the Fusion Digital Power Designer software to program the conditions for the sequence and store that configuration into the internal flash memory.

2 Block Diagram

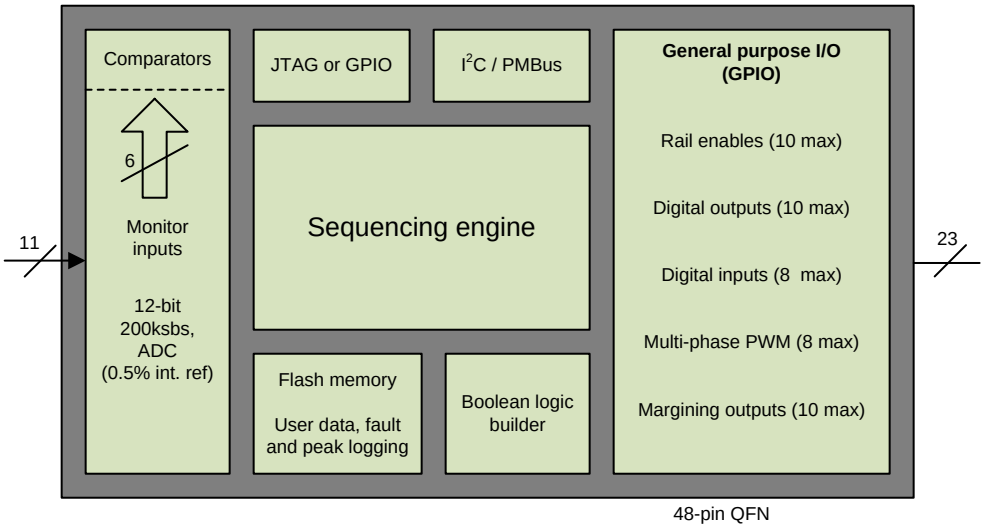


Figure 2. Block Diagram

2.1 Implementation

The UCD9090 device sequences and monitors the power outputs of the XEVMK2EX design. If an output fails, the UCD9090 disables the power supplies in the programmed sequence. For a list of the power supplies for the XEVMK2EX design, see Table 1.

Table 1. XEVMK2EX Power Supplies Controlled by the UCD9090

Sequence	Power Supply	Voltage	Rail Enable	Description
1	TPS65400	3.3 V	VCC3V3_AUX_EN	Local system 3.3 V isolated from K2E
2	TPS544C25	Core AVS	CVDD_EN	K2E core AVS power supply
3	TPS65400	1.0 V	CVDD1_EN	K2E 1.0-V fixed core supply (0.95 V in EVM design)
4	TPS65400	1.8 V	VCC1V8_EN	K2E 1.8-V I/O voltage supply
5	TPS54620	1.5 V	VCC1V5_EN	K2E 1.5-V DDR3 I/O voltage supply
6	TPS51200	0.75 V	VTT_EN	K2E 0.75-V DDR3 VTT I/O voltage supply
7	TPS65400	0.85 V	VCC0V85_EN	K2E 0.85-V Serdes low-voltage supply
8	TPS22913B	3.3 V	VCC3V3_EN	SoC side 3.3-V supply (Not connected to K2E directly)
9	TPS54620	5.0 V	VCC5_EN	K2E USB 5.0-V supply
10	TPS22913B	5.0 V	USB_VBUS_EN	K2E VBUS pin voltage isolator

For more information on each of these devices, see the respective product folders at www.TI.com.

2.2 Voltage Monitoring

The UCD9090 device monitors the voltage levels for the power supplies on the XEVMK2EX design. The internal ADC inputs are limited to 2.5 V. To accommodate this limit, a voltage divider connects the 3.3-V and 5-V supply inputs. For the voltage monitor inputs, see Figure 3.

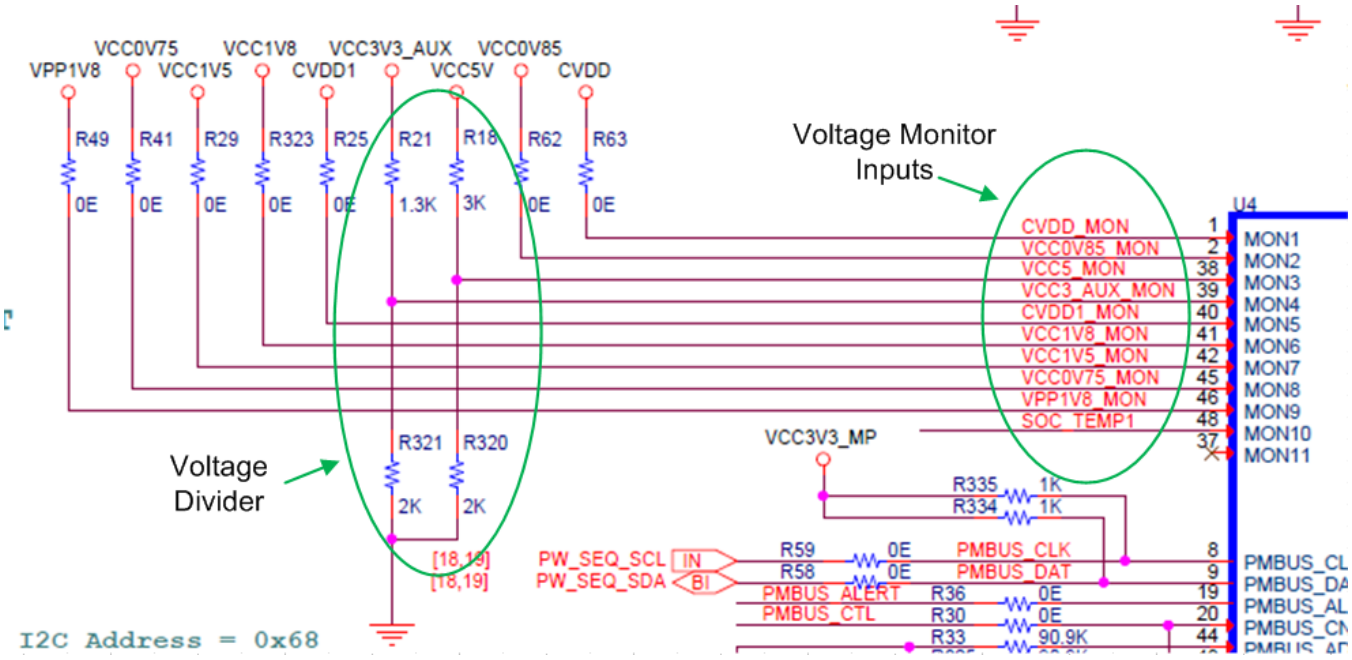


Figure 3. Voltage Monitor Inputs

Each monitor input generates a power-good signal for that rail. The power-good signals can then sequence and define the GPIO logic in the UCD9090 device. The Vout Config tab of the Fusion Digital Power Designer software defines the power-good condition for each monitor input. For an overview of the voltage monitor definition, see Figure 4.

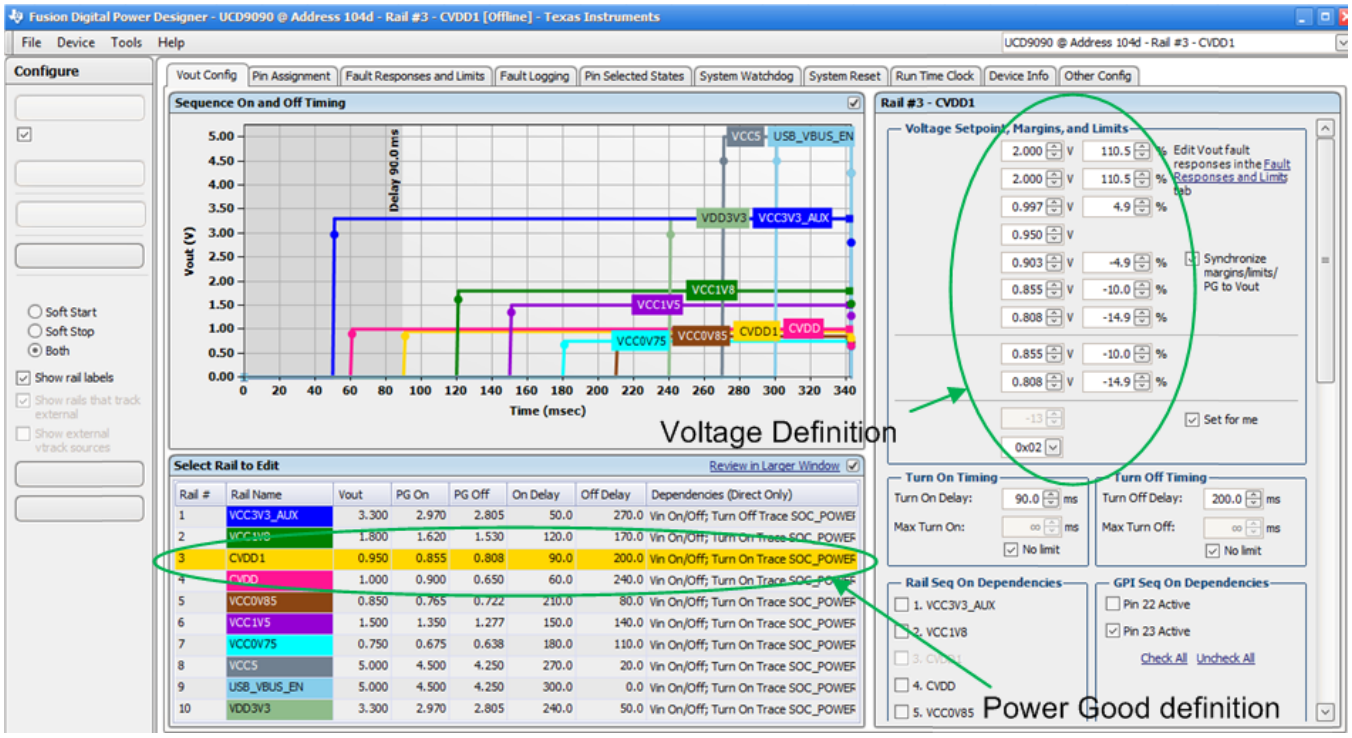


Figure 4. Voltage Monitor Definition

2.3 Rail Enables

The UCD9090 device provides the 10 rail-enable signals to the power supplies on the XEVMK2EX design. For the voltage rail enables, see Figure 5.

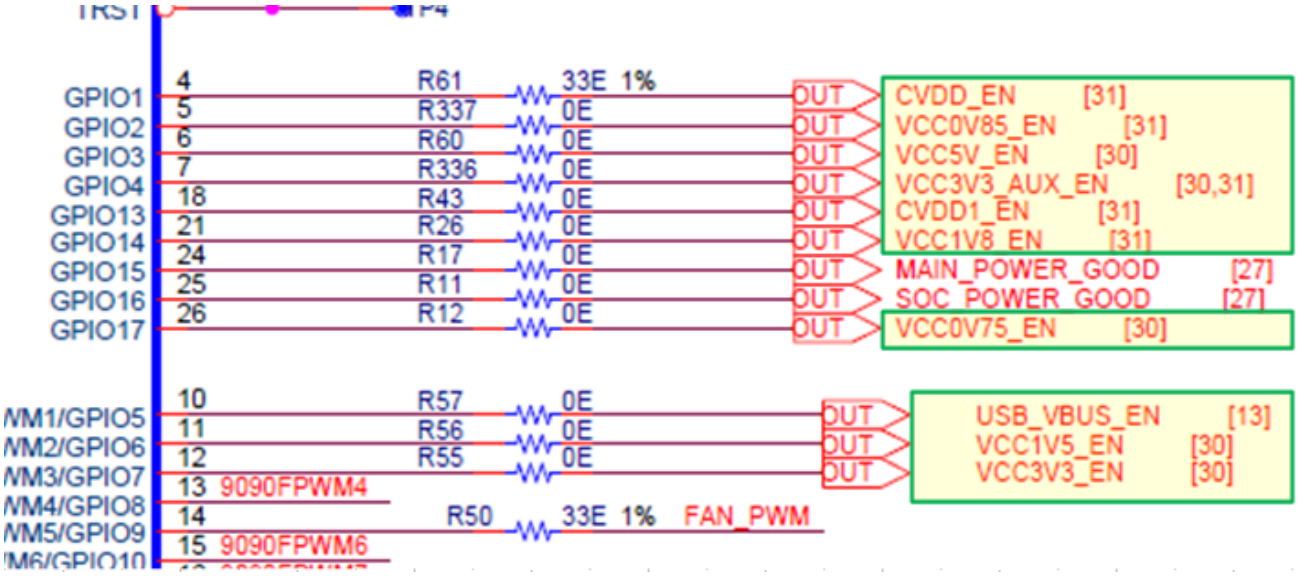


Figure 5. Voltage Rail Enables

The Pin Assignment tab of the Fusion Digital Power Designer software assigns the rail-enable signals and selects the signal type. For the voltage rail enable selection, see Figure 6.

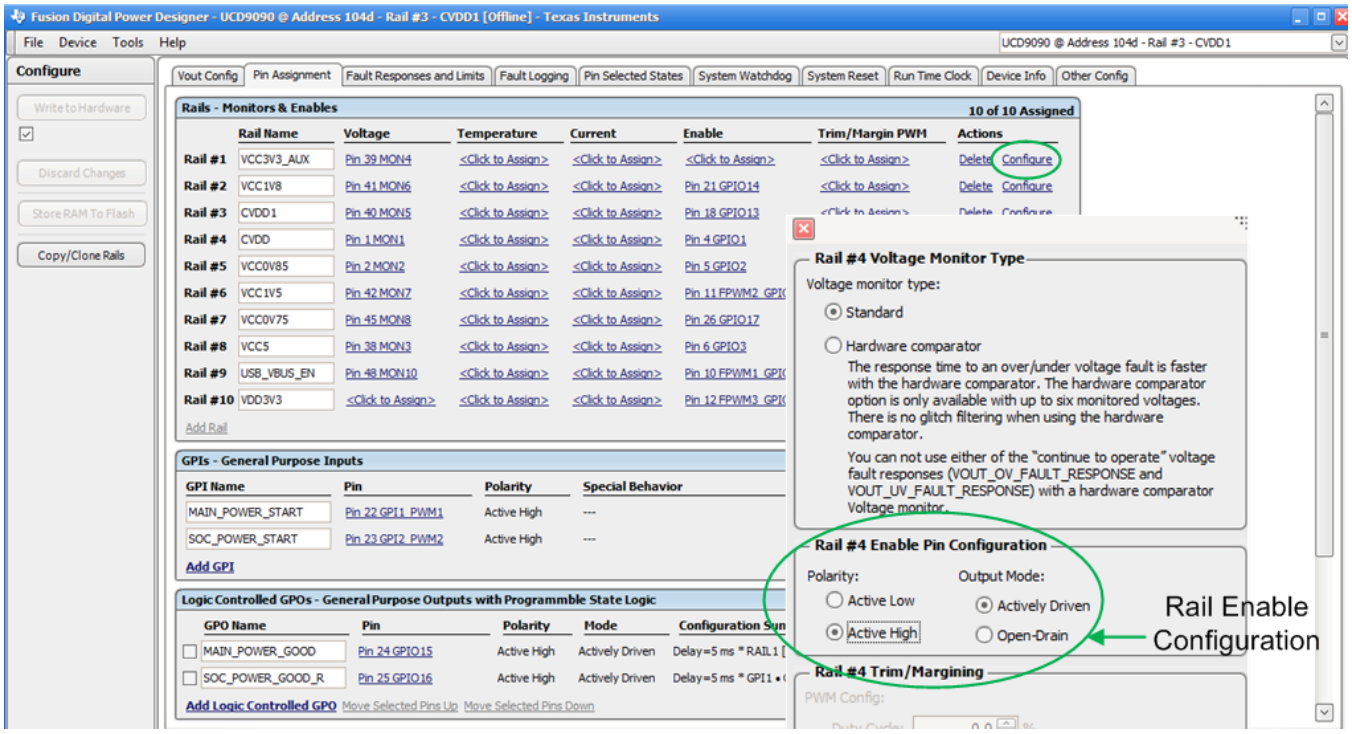


Figure 6. Voltage Rail-Enable Selection

In the power sequence for the XEVMK2EX design, the Vout Config tab of the Fusion Digital Power Designer software defines the rail enable for each power supply. The EVM uses a time-based sequence for the power supplies initiated by a control input from the BMC processor. When the processor enables the sequence, the rail enables are activated as defined in Figure 7. You can use the turn-on timing setting to set the delay for the rail and to specify the turn-off delay for a sequenced shutdown. For an overview of the definition of the voltage rail-enable sequence, see Figure 7.

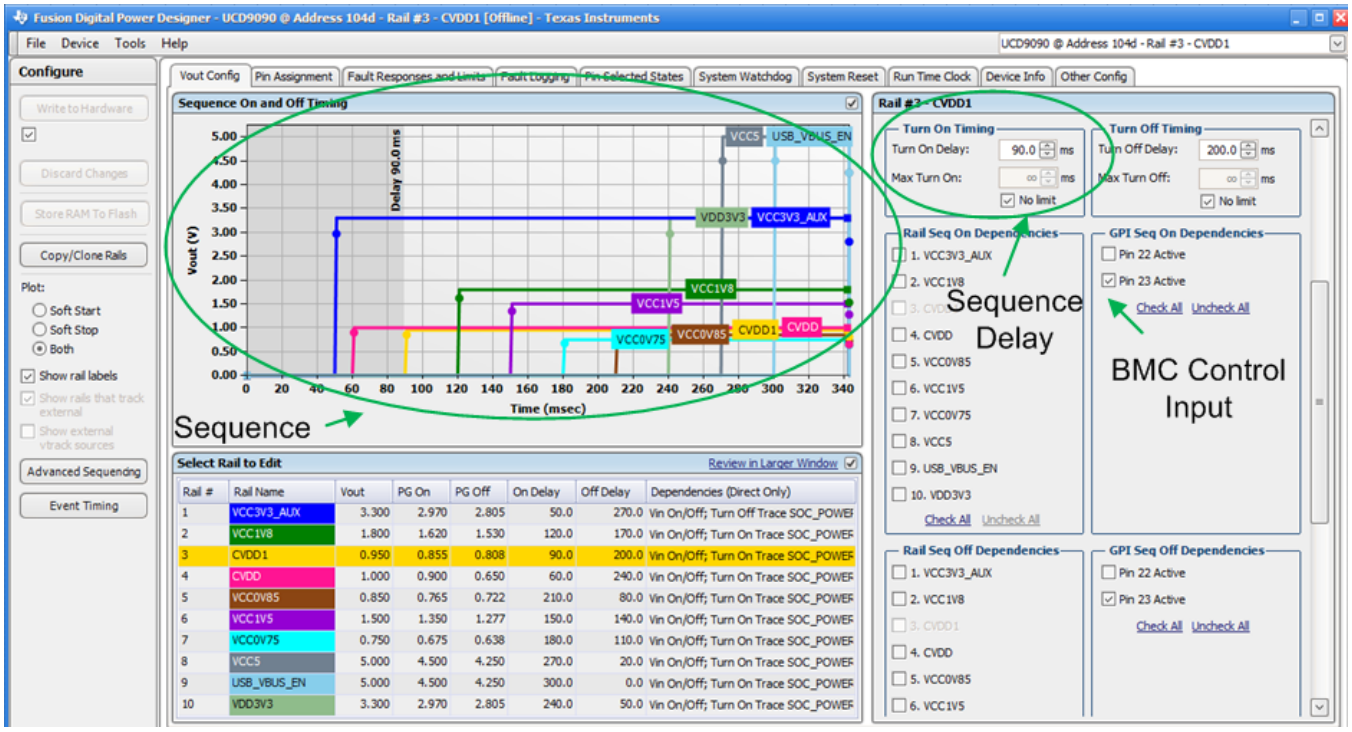


Figure 7. Voltage Rail-Enable Sequence Definition

When the power sequence completes, the K2E SoC requires all voltage rails be present. If a voltage rail fails during operation, the UCD9090 device shuts down the rest of the rails. If the power supply fails, the fault shutdown slave window defines which additional power supplies are disabled. For an overview of the fault shutdown condition of the voltage rail-enable sequence, see Figure 8.

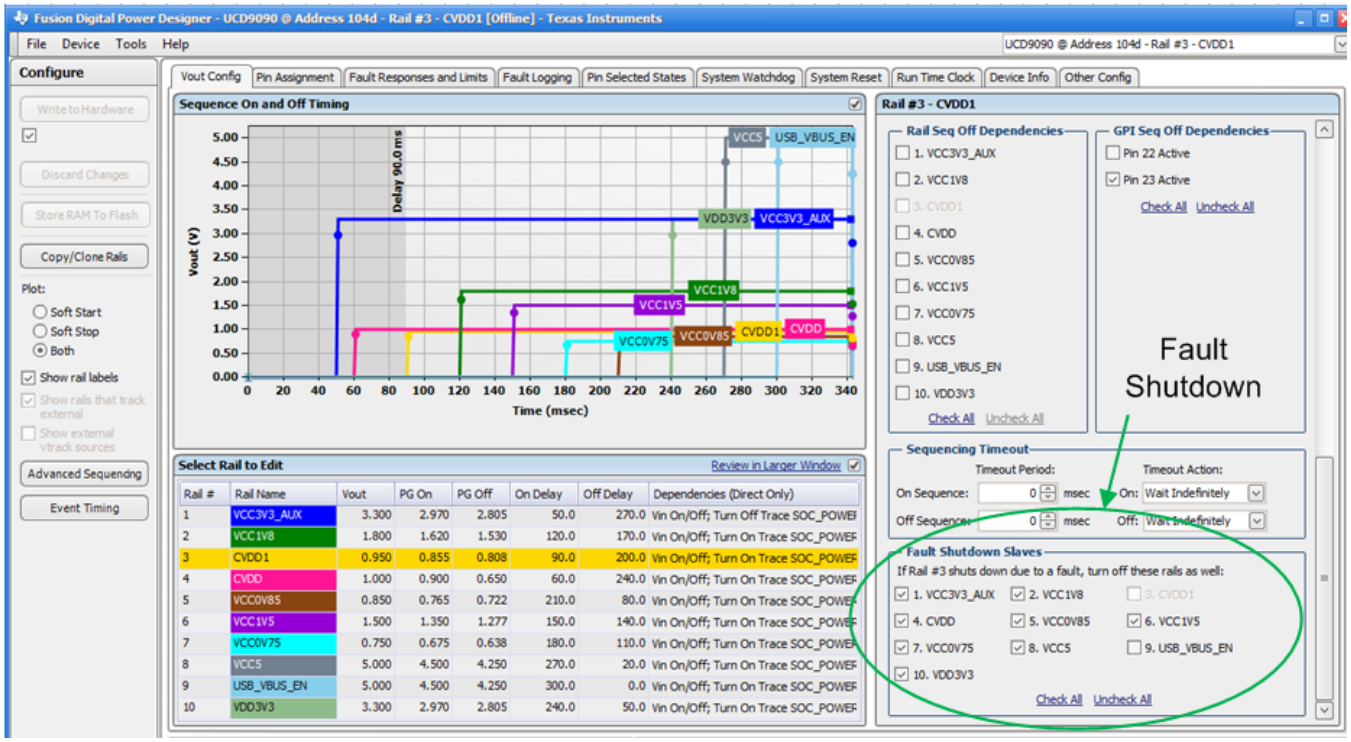


Figure 8. Voltage Rail-Enable Fault Shutdown Condition

2.4 BMC Processor Control Signals

The XEVMK2EX design uses the BMC processor to control the state of the K2E, including initiating the sequencing of the power supplies. The processor provides two control inputs and two monitor outputs. We intended the MAIN_POWER_START input to enable the VCC3V3_AUX supply and the SOC_POWER_START input to initiate the sequence of the rest of the rails. The released version of the configuration does not use the MAIN_POWER_START input. When the SOC_POWER_START is set at the beginning of the sequence, the UCD9090 enables the VCC3V3_AUX supply. For the BMC sequencing control signals, see Figure 9.

To configure the power supply sequence, do the following:

1. Use the window in the Vout Config tab to select the on and off dependencies for the GPI sequence.
2. Use the Pin Assignment tab to define the pins for GPI and GPO (see Figure 10).
3. Select Configure, listed under Actions, to define the GPO (a window with two conditions to be assigned to an OR function opens [see Figure 11]).
4. Select the login function that controls the GPO (see Figure 12).

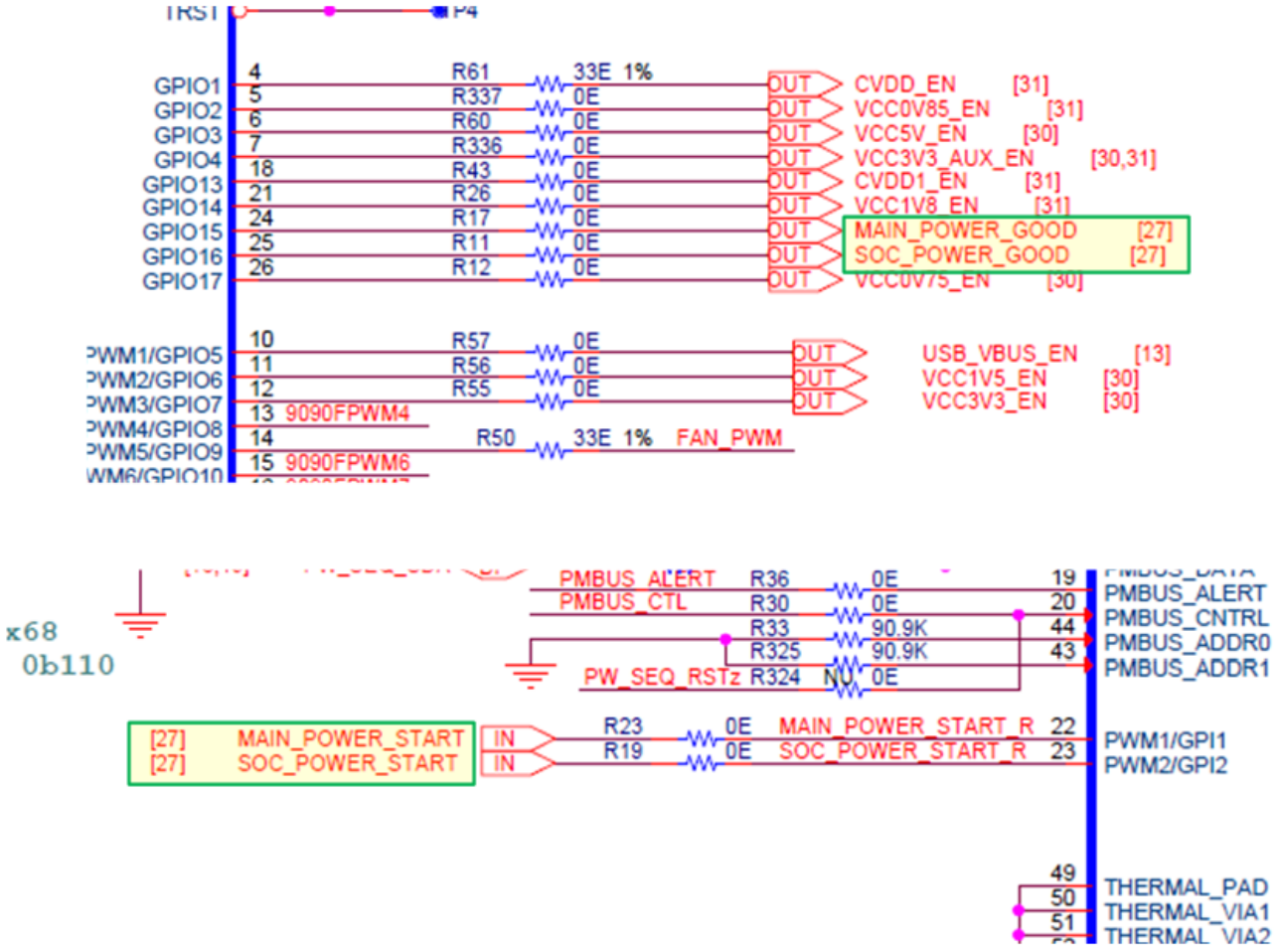


Figure 9. BMC Sequencing Control Signals

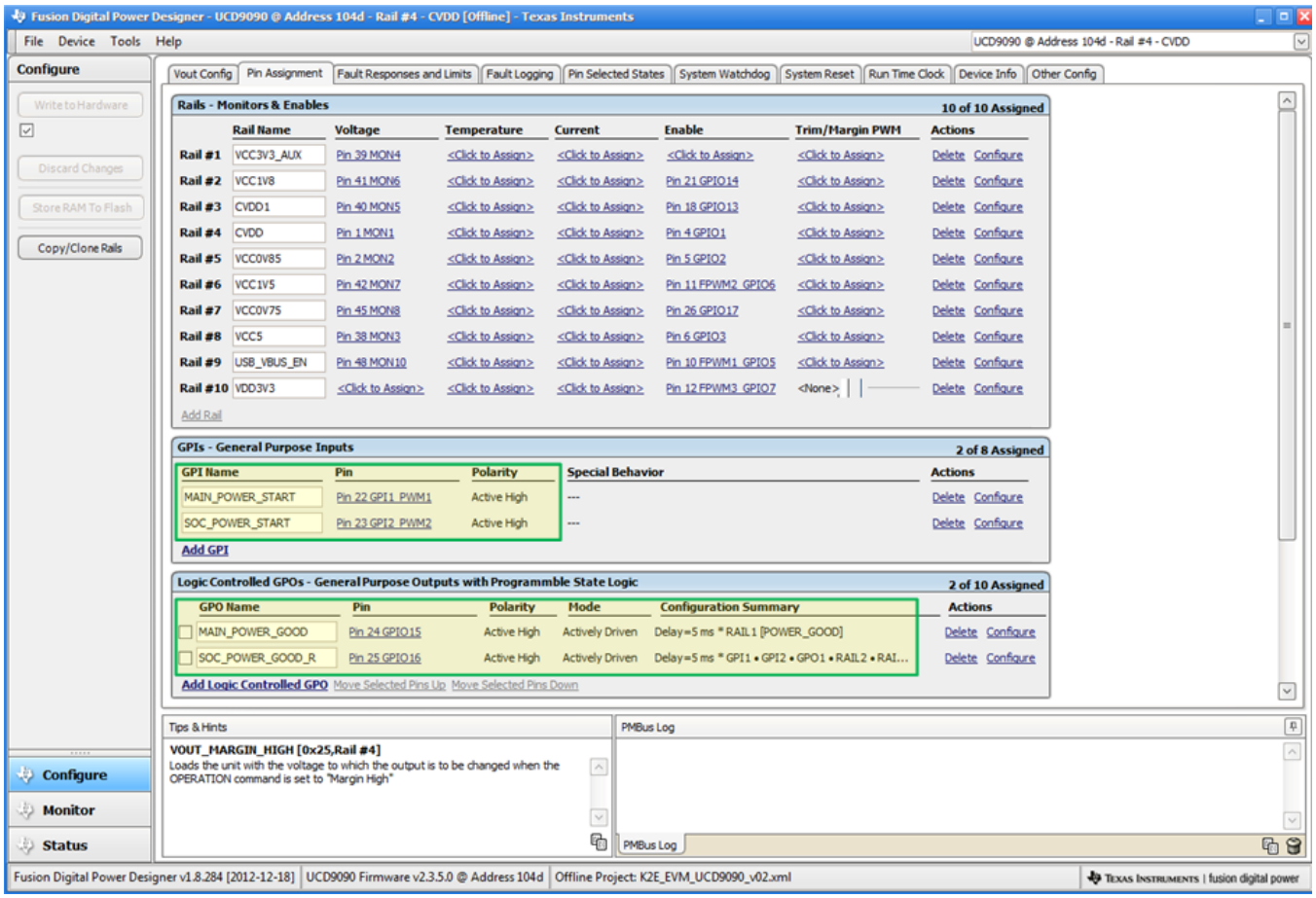


Figure 10. GPI and GPO Pin Assignment

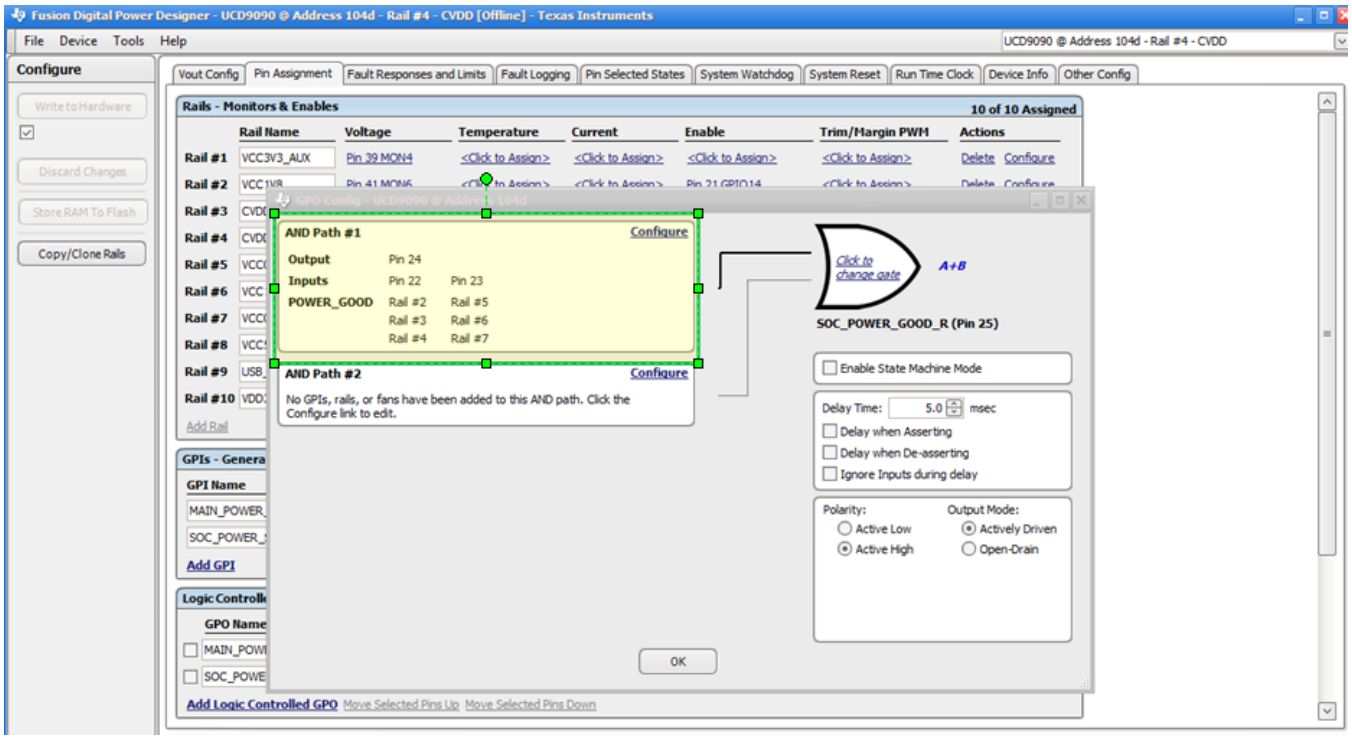


Figure 11. GPO Pin Configuration

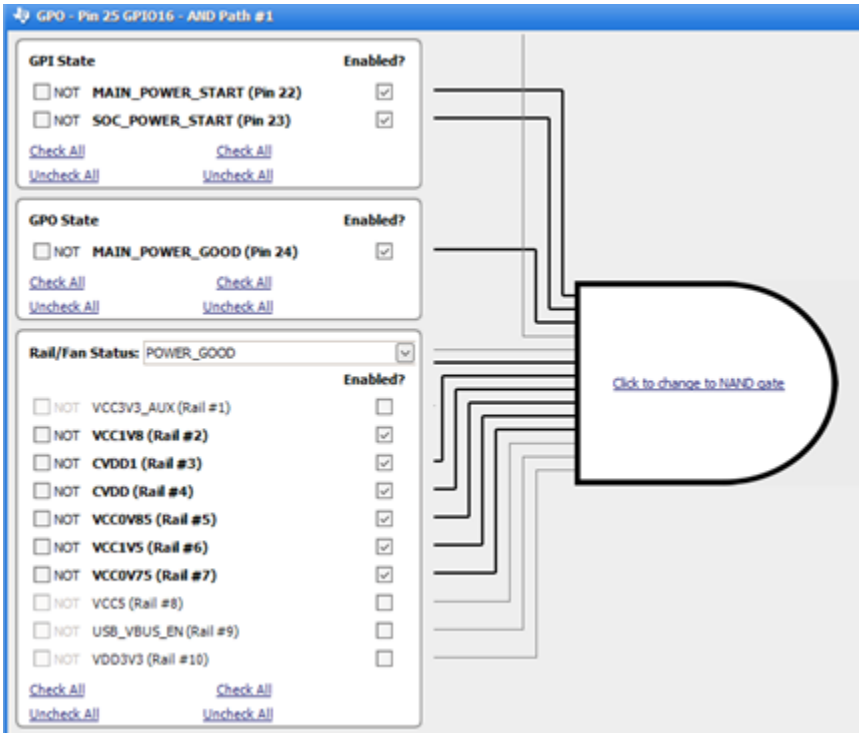


Figure 12. GPO Pin Output Criteria

3 Configuration of the UCD9090

Use the Fusion Digital Power Designer software and the PMB interface to generate the register values and to program the UCD9090 device. The Fusion Digital Power Designer software uses the TI USB-TO-GPIO USB Interface Adapter EVM to connect a PC running the Fusion software to the XEVMK2EX design. Only the PMBUS_DAT, PMBUS_CLK and GND signal must be connected to program the UCD9090 device. When you have configured the UCD9090, click *Write to Hardware* on the tab labeled Configure to store the configuration to the UCD9090 device.

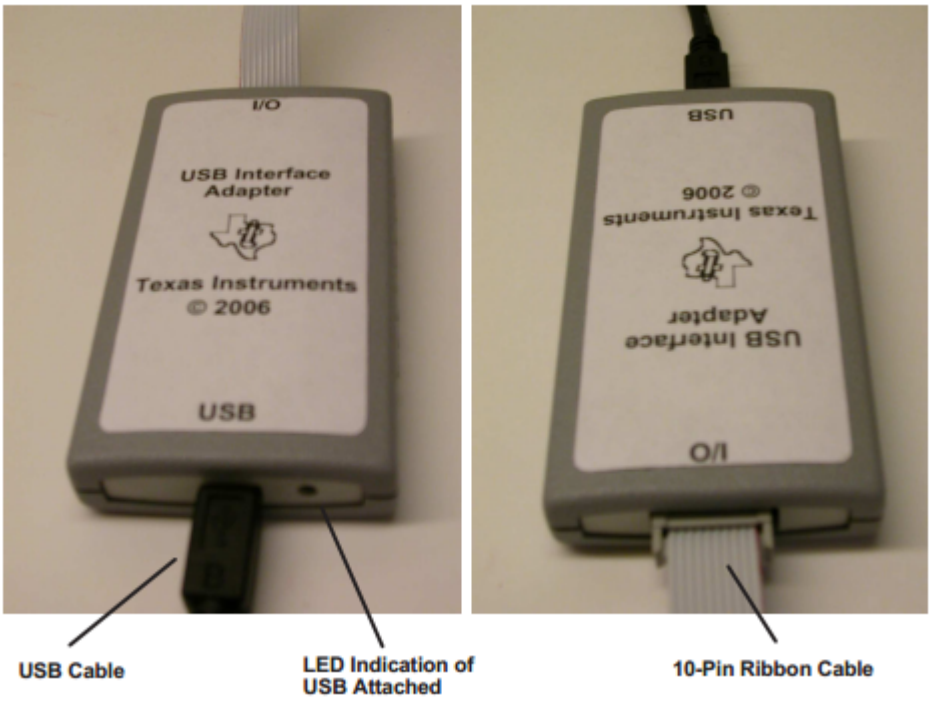
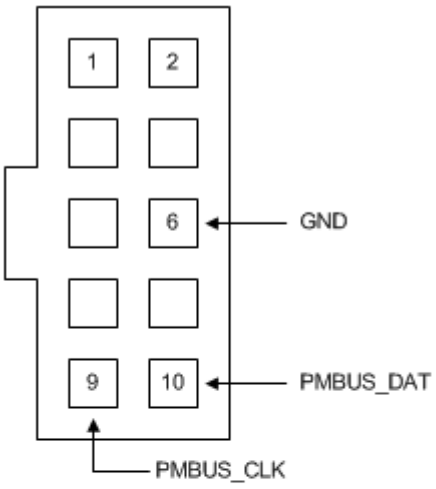


Figure 13. USB Interface Adapter Pod



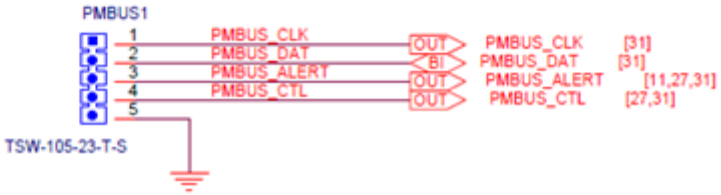


Figure 14. USB Pod to PMBus Header Connection

3.1 Configuration File

You can use the Fusion Digital Power Designer to open an XML file as a project. The XML configuration file for the EVMK2E is in the product folder for this design. When you open the configuration file with the software, it displays the Vout Config tab. This tab shows the power supply rail enable and the sequence order.

4 PCB Design

You can find the PCB, schematic, and bill of materials in the product folder for this design. For details on the placement and layout of the PCB, refer to *10-Rail Power Supply Sequencer and Monitor with ACPI Support* (SLVSA30A). This design was implemented as part of the XEVMK2EX design. The PCB file includes all parts associated with the 66AK2E0x EVM device.

5 Modifications

The XEVMK2EX design includes a few power supplies that are not used by the K2E SoC. The XEVMK2EX design includes the board monitor controller (BMC) that acts as a master to set the boot mode and initiate the power supply sequence for the K2E SoC. These power supplies are unnecessary for customer designs and can be removed. The UCD9090 device includes other features unused by the XEVMK2EX design. For more information on capabilities that might be useful in your design, see *10-Rail Power Supply Sequencer and Monitor with ACPI Support* (SLVSA30A).

5.1 Power Supply Removal

In the XEVMK2EX design, the VCC3V3_AUX and the VDD3V3 voltages are not used by the K2E SoC. Your design may not require these supplies.

5.2 BMC Initialization

The current design requires the external control of the BMC to initiate the sequence using the SOC_POWER_START input. You can modify the programming of the UCD9090 device to initiate the sequence when power is available to the device. You can include monitor input for the source voltage used by the SoC power supplies and change the sequence to initiate when the source voltage power good condition exists. The supplies shut downs if one of the voltage rails fails. You can use the SOC_POWER_GOOD signal as a test point or drive an LED to indicate when the supplies are stable.

6 References

- *UCD9090 10-Rail Power Supply Sequencer and Monitor with ACPI Support* (SLVSA30)
- *66AK2E05, 66AK2E02 Multicore DSP+ARM KeyStone II System-on-Chip (SoC)* (SPRS865)
- *AM5K2E04, AM5K2E02 Multicore ARM KeyStone II System-on-Chip (SoC)* (SPRS864)

7 About the Author

WILLIAM TABOADA is an application engineer at TI, where he supports the KeyStone I and KeyStone II multicore processor families. William brings to this role his extensive experience designing processor based systems utilizing DDR3 memory architecture and high-speed serial interfaces. William earned a Bachelor of Science (BS) from Lehigh University and a Master of Science (MS) from The George Washington University.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265