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36-V, 1-kW Brushless DC Motor Drive With Stall Current Limit of < 1-µs Response Time Reference Design

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Design Resources

TIDA-00436	Design Folder
TIDA-00285	Design Folder
CSD18540Q5B	Product Folder
DRV8303	Product Folder
TPS54061	Product Folder
OPA2374	Product Folder
TPD4S009	Product Folder
LMT84	Product Folder
TMS320F28027	Product Folder
LAUNCHXL-F28027	EVM Folder

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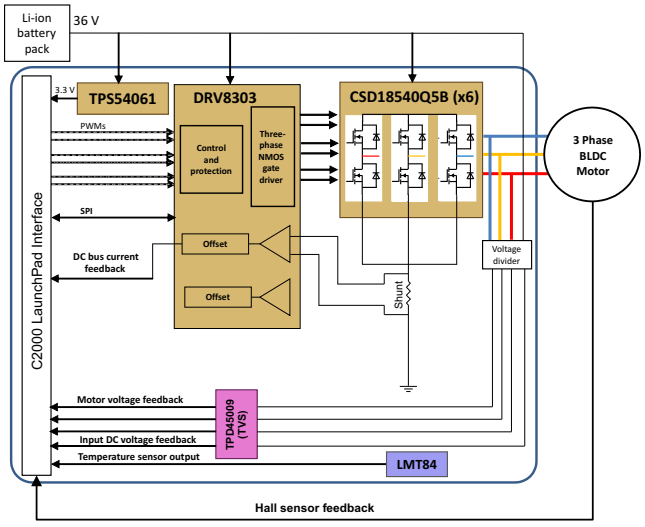
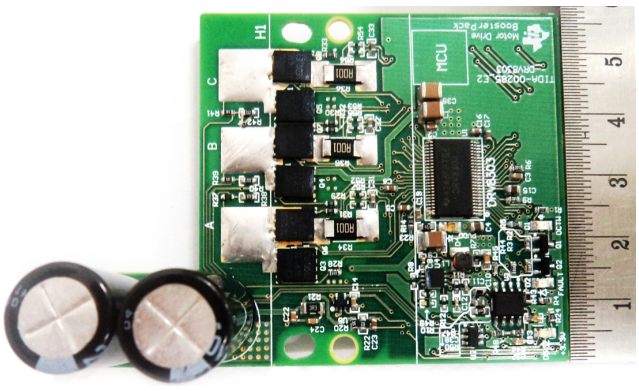
Design Features

- 1-kW Power Stage With Hall Sensor-Based Trapezoidal Control for Brushless DC Motor Implemented on TMS320F28027 C2000™ MCU
- Designed to Operate from 10-Cell Li-Ion Battery Voltage Ranging from 30 to 42 V
- Delivers up to 30-A Continuous Motor Current With an Airflow of 400 LFM
- Small PCB Form Factor of 57 × 59 mm Using CSD18540Q5B 60-V/400-A_{peak}, 1.8-mΩ R_{DS_ON}, SON5x6 package MOSFETs for Power Stage
- Uses DRV8303 Three-Phase Gate Driver, Which Can Operate from 6 to 60-V Input, Supporting Programmable Gate Current of 2.3-A Sink / 1.7-A Source V_{DS} Sensing of External MOSFETs and Two PGAs for Current Measurement
- Cycle-by-Cycle Overcurrent Limit With Configurable Threshold for Motor Stall Protection
- DC Bus Return Current Measurement Using Shunt to Enable Torque Control Implementation and DC Bus Voltage Measurement Using Built-In 12-Bit ADC of MCU
- TPS54061-Based 3.3-V/0.15-A Step-Down Buck Converter for Powering MCU
- Designed to Operate at an Ambient Temperature of –20°C to 55°C

Featured Applications

- Power Tools
- Garden Tools
- Lawn Mover Robots
- Vacuum Cleaning Robots





1 Introduction

This reference design is a power stage for brushless motors in battery-powered garden and power tools rated up to 1 kW. The power stage operates from a 10-cell lithium-ion battery with a voltage range from 36 to 42 V. The design uses CSD18540Q5B NexFET™ MOSFET featuring a very low drain-to-source resistance (R_{DS_ON}) of 1.8 mΩ in a SON5x6 SMD package, which results in a very small PCB form factor of 57 × 59 mm. The three-phase gate-driver DRV8303 is used to drive the three-phase MOSFET bridge, which can operate from 6 to 60 V and support programmable gate current with maximum setting of 2.3-A sink / 1.7-A source. The C2000 Piccolo™ LaunchPad™ LAUNCHXL-F28027 is used along with this design. Software for 120° trapezoidal control of the BLDC motor with digital output Hall sensors for position feedback is implemented on a C2000 LaunchPad. The corresponding test report evaluates the cycle-by-cycle overcurrent protection feature of the DRV8303, for protecting the power stage during motor stalls. The cycle-by-cycle current limit feature protects the board from excessive current that is caused during motor stalls by limiting the maximum current allowed in the power stage to a safe level.

Power tools are used in various industrial and household applications such as drilling, grinding, cutting, polishing, driving fasteners, various garden tools, and so on. The most common types of power tools use electric motors while some use internal combustion engines, steam engines, or compressed air. Power tools can be either corded or cordless (battery-powered). Corded power tools use the mains power (the grid power) to power up the AC or DC motors. The cordless tools use battery power to drive DC motors. Most of the cordless tools use lithium-ion batteries, the most advanced in the industry. Lithium-ion batteries have high energy density, low weight, and greater life. These batteries have relatively low self-discharge (less than half that of nickel-based batteries) and can provide a very high current for applications like power tools. Cordless tools use brushed or BLDC motors. The brushless motors are more efficient and have less maintenance, low noise, and longer life. Power tools have requirements on form factor and thermal performance. Therefore, high-efficient power stages with a compact size are required to drive the power tool motor. Small form factor of the power stage enables design flexibility for optimal cooling method and placement of the power stage close to the battery pack to minimize impedance on connections carrying high current. High efficiency provides maximum battery duration and reduces cooling efforts. High efficiency requirement in turn asks for switching devices with low R_{DS_ON}. The power stage should also take care of protections like motor stall or any other chance of high current.

The objective of this reference design is to provide a 1-kW/36-V power stage for brushless motors used in battery powered applications (like power tools, garden tools, and so on). This design demonstrates the power stage in a small form factor (57 × 59 mm) operating from a 36-V DC input (using a 10-cell Li-ion battery) and delivers up to a 30-A continuous current output to motor. The design also provides scalability for lower voltage and current levels. At higher power levels, the cooling is provided by forced air, which allows for the small form factor. The cycle-by-cycle feature of the DRV8303 is used for protecting the power stage against damage due to stall currents. In applications like cordless power tools, during the normal usage, the motor very often faces stall situations. In such situations, the stall current level is too high compared to the normal operation of the motor and it needs to be limited to protect the power stage and the motor. Having such kind of overcurrent protection in hardware is always safer. The cycle-by-cycle current limit feature helps achieving the same and in turn helps rightly size the power MOSFETs rather than over designing the power section.

2 Key System Specifications

Table 1. Key System Specifications of Power Stage

PARAMETER	SPECIFICATION
DC input voltage	36-V nominal (42-V maximum)
Maximum input DC current	30 A with 400 LFM airflow
Rated power capacity	1 kW
Inverter switching frequency	20 kHz
Operating ambient temperature	–20°C to 55°C
Inverter efficiency	≥ 97% (theoretical) at rated load
Power supply specification for MCU	3.3 V ±5%
Feedbacks	Hall sensors, DC bus current sense, DC bus voltage
Protections	Overcurrent (cycle-by-cycle/latch), over temperature, input undervoltage
PCB	57 × 59 mm / 4-Layer, 2-Oz copper

3 System Description

Compared to their brushed motor counterpart, permanent magnet brushless DC (BLDC) motors are gaining importance because of their high efficiency, low maintenance, high reliability, low rotor inertia, low noise, and so on. A brushless motor has a wound stator and a permanent magnet rotor assembly. These motors generally use internal or external devices to sense rotor position. The sensing devices provide logic signals for electronically switching the stator winding currents in a proper sequence to maintain rotation of the rotor with magnet assembly. The Hall sensors typically embedded as a part of the motor assembly and gives information on rotor position.

The electronic drive is required to control the stator currents to generate rotating magnetic field in a BLDC motor. The electronic drive consists of:

- A power stage with three-phase inverter having the required power capability
- MCU to implement the motor control algorithm
- DC-Link current and position feedback from Hall sensors
- Gate driver for driving the three-phase inverter
- Power supply for the MCU

3.1 Brushless Permanent Magnet Motors

Permanent magnet motors can be classified based on Back-EMF (BEMF) profiles: BLDC motor and permanent magnet synchronous motor (PMSM). Both BLDC motors and PMSMs have permanent magnets on the rotor but differ in the flux distributions and BEMF profiles. In a BLDC motor, the BEMF induced in the stator is trapezoidal, and in a PMSM, the BEMF induced in the stator is sinusoidal. Implementation of an appropriate control strategy is required to obtain the maximum performance from each type of motor.

3.1.1 BLDC Motor – Trapezoidal Control

The BLDC motor or the trapezoidal BEMF motor has the ampere conductor distribution of the stator, which ideally remains constant and fixed in space for a fixed interval known as the commutation interval. For a three-phase winding, the commutation interval is 60° electrical. At the end of each commutation interval, the ampere conductors are commutated to the next position. These motors use a two-phase ON control, where two phases of the motor will be energized at a time and the third winding will be open, The principle of the BLDC motor is, at all times, to energize the phase pair, which can produce the highest torque. The combination of a direct current with a trapezoidal BEMF makes it theoretically possible to produce a constant torque. In practice, the current cannot be established instantaneously in a motor phase as a consequence the torque ripple is present at each 60° phase commutation. Figure 1 describes the electrical waveforms in the BLDC motor in the two phases ON operation.

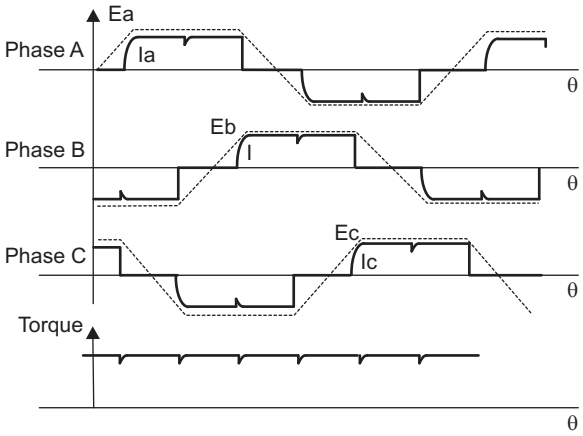


Figure 1. Electrical Waveforms in Two-Phase ON Control of BLDC Motor and Torque Ripple

A trapezoidal control has following advantages:

- Only one current at a time needs to be controlled
- Only one current sensor is necessary (or none for speed loop only)
- The positioning of the current sensor allows the use of low cost sensors as a shunt

For more details about trapezoidal control, see the application report *Sensorless Trapezoidal Control of BLDC Motors* (SPRABQ7). For Hall-sensored control, refer to the application note *Trapezoidal Control of BLDC Motors Using Hall Effect Sensors* (SPRABQ6)

3.2 Stall Current in BLDC Motor

A stall current is the current in the motor when rotor is stuck or at zero speed. Figure 2 shows electrical model of the BLDC, showing the three phases of the motor: phase resistance R, phase inductance L, and BEMF Ea, Eb, and Ec. The motor terminal voltages are Va, Vb, and Vc. I_a is the phase current in when Phase A and B is energized. The line voltage Vab is given as

$$Vab = 2R \times I_a + 2L\frac{d(I_a)}{dt} + Ea - Eb \quad (1)$$

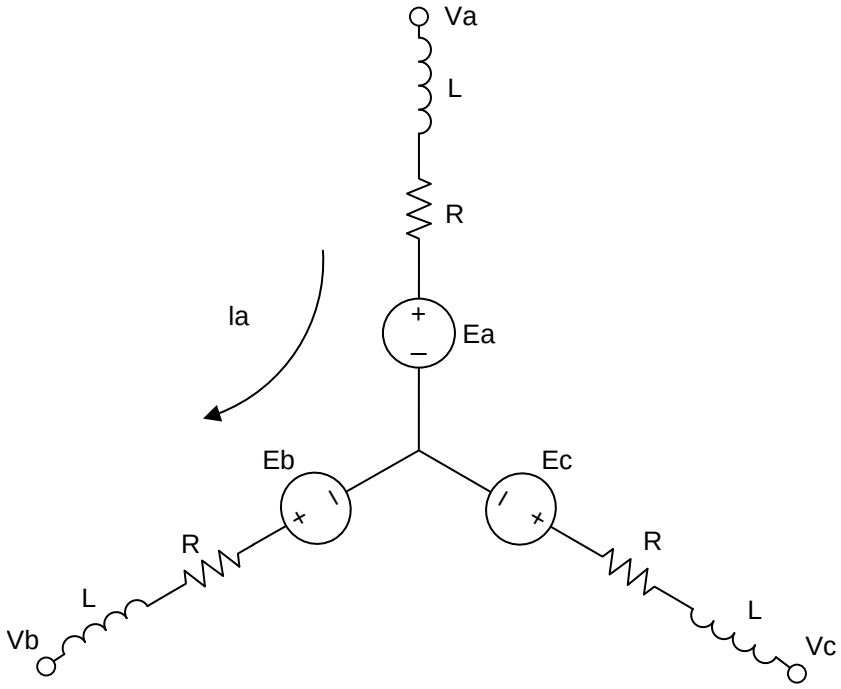


Figure 2. Electrical Model of BLDC Motor

The Motor BEMF, E ∝ NlrBω where N is the motor winding turns per phase, l length of the motor, r is radius of motor, B is magnetic field density, and ω is the angular velocity.

At zero angular velocity, the BEMF does not exist in the motor. Also, the BLDC motor has low inductance due to permanent magnet construction, ignoring this term for calculating the stall current. Therefore, from Equation 1 the stall current is $I_{stall} = \frac{Vab}{2R}$.

Vab is the terminal voltage. When the phase are energized during the on time of the PWM, the terminal voltage is equal to the DC bus voltage. The resistance R of the motor is typical very small in order of mΩ. Considering practical values of 36-V DC bus and motor resistance of 20 mΩ, the current can be $\frac{36}{2 \times 0.02} = 900$ A.

The stall current value at an overall system level will be lesser due to the ON resistance contribution from the MOSFETs, internal resistance of the battery, motor connecting wires, PCB track resistance, and so on.

Designing a power stage for power tools overrated to handle such high currents is cost prohibited. The DRV8303 cycle-by-cycle protection mechanism implemented in hardware will turn off MOSFETs when the current exceeds a set threshold. Therefore, the MOSFETs in the power stage can be selected with a current rating lower than the peak stall current of the motor.

3.3 Power Stage for the Motor Drive

The reference design provides a 1-kW/36-V power stage for brushless motor control in battery powered garden and power tools. The reference design uses the MCU TMS320F28027 that is part of the LAUNCHXL-F28027 LaunchPad. The power stage is mounted as the booster pack. Figure 3 shows the assembled power stage mounted with the LaunchPad.

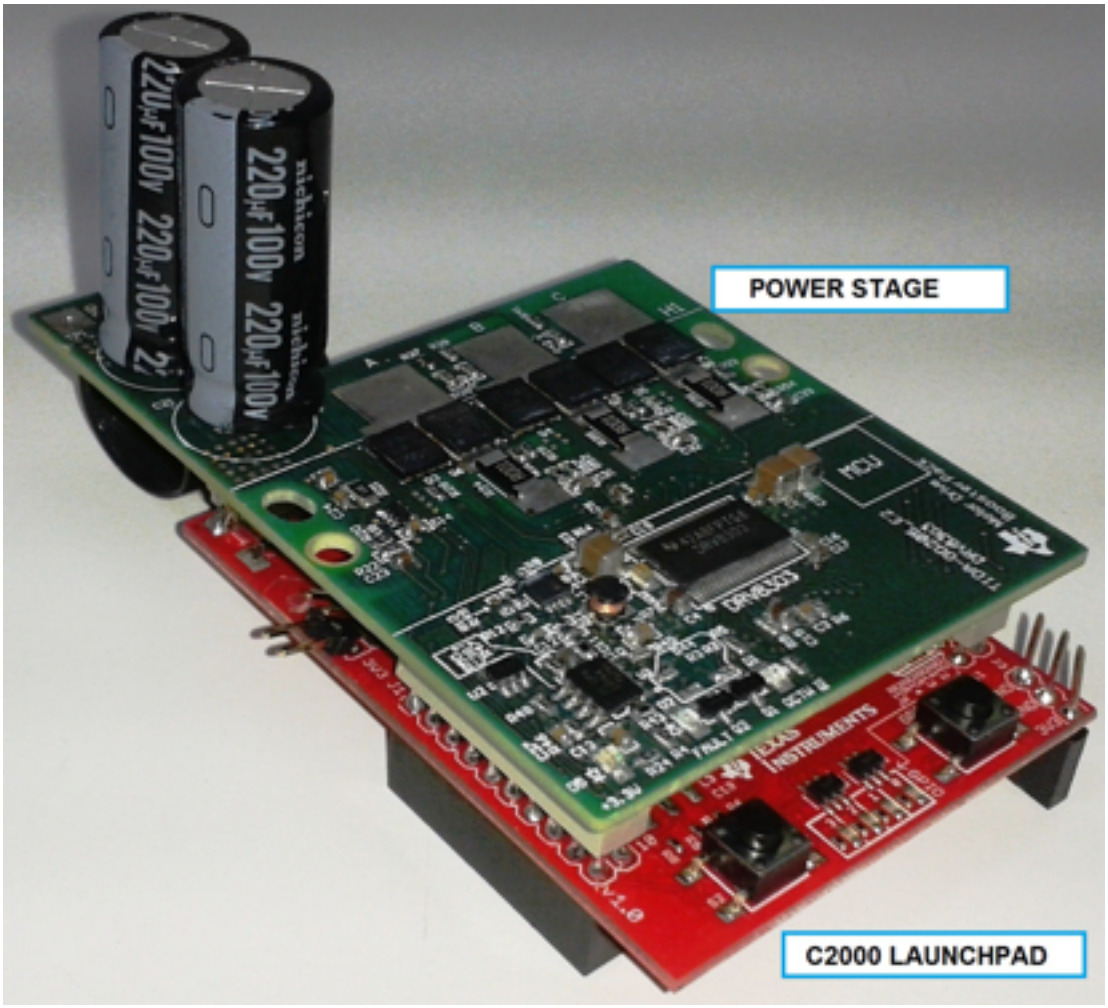


Figure 3. Assembled Power Stage Mounted With LaunchPad

The power stage is designed to operate from a 10-cell Li-ion battery. For a Li-ion battery, the maximum volt per cell is 4.2 V and nominal voltage is 3.6 V per cell. The power stage is designed to operate up to 42 V. The booster pack power stage consists of the high efficient, six miniature NexFET CSD18540Q5B to form the three-phase inverter bridge. The SON5x6 miniature package of the NexFET enables to make the power stage in a small form factor. The power stage is designed to handle the nominal power with a forced air cooling of 400 LFM. The low R_{DS_ON} of 1.8 mΩ of the FETs helps to reduce the power loss. which lessens heat dissipation in the FETs and makes the power stage thermally stable.

The FETs are driven by the three-phase gate driver DRV8303. The DRV8303 can operate from a 6- to 60-V power supply, which is suitable to work in the application voltage range. The DRV8303 has two internal current shunt amplifiers for accurate current measurements and provides overcurrent protection by sensing the drain-to-source voltage of the external power MOSFETs. These features make the DRV8303 apt for motor control. The different references and features of the DRV8303 can be configured through SPI programming. The DRV8303 driver also has shoot-through, and undervoltage protection.

The 3.3-V power supply for the MCU is generated in the power stage board using the TPS54061.

4 Block Diagram

Figure 4 depicts the block diagram of the power stage. The main parts of the power stage consists of the three-phase MOSFET bridge, the gate driver DRV8303, interface to C2000 MCU LaunchPad, 3.3-V step-down DC-DC converter, ESD protection, over temperature protection, and the sense feedback circuits.

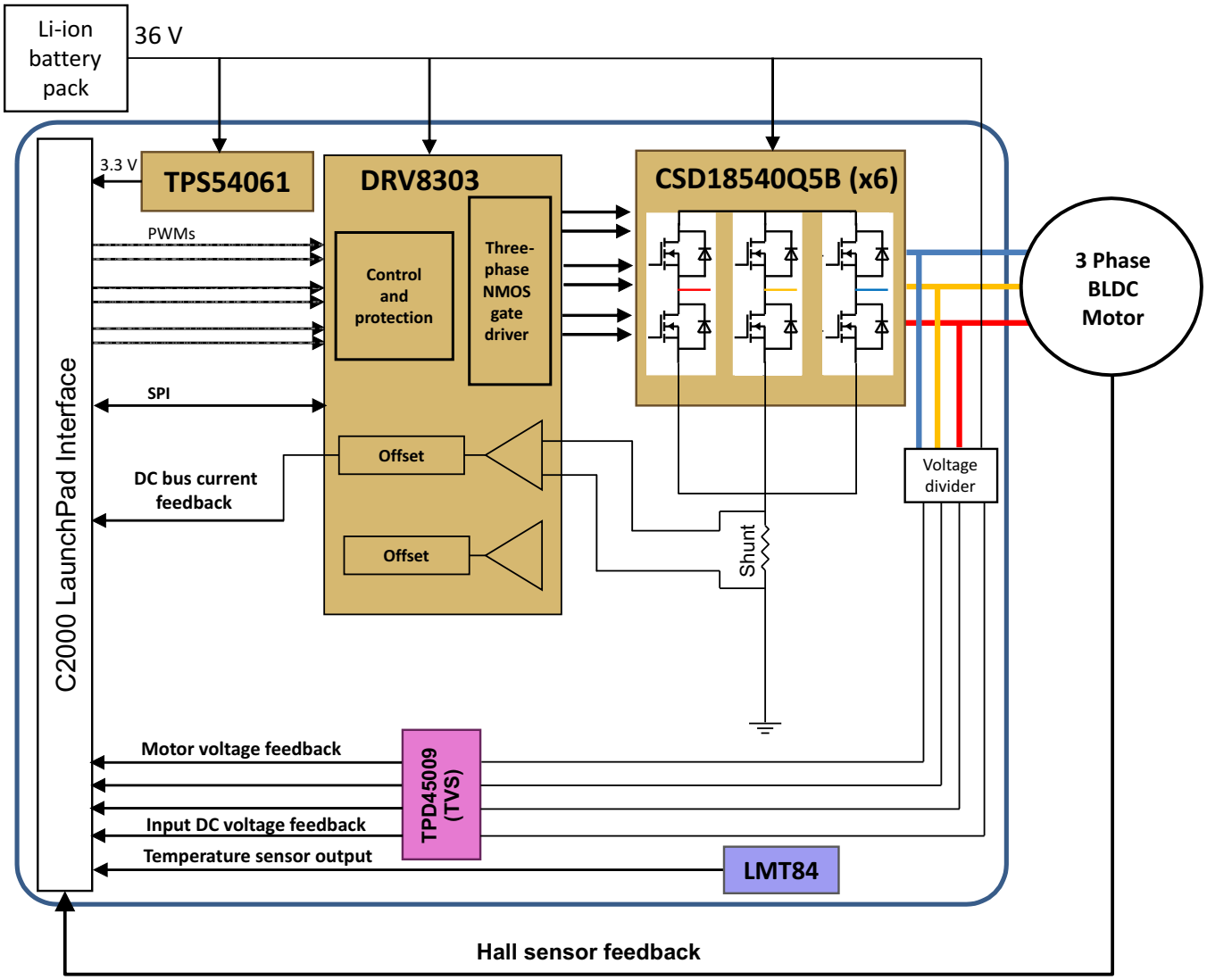


Figure 4. Block Diagram of the Power Stage

The inverter is powered from a 36-V, 10-cell lithium-ion battery. The 3.3-V supply required for the MCU in the LaunchPad is generated using the step-down DC-DC converter TPS54061. The C2000 LAUNCHXL-F28027 LaunchPad is used as the control unit. The DRV8303 is the gate driver IC, which is used to drive the three-phase MOSFETs based on the PWM signals generated by the C2000 controller from the LaunchPad. The LaunchPad configures the gate driver DRV8303 using SPI. The temperature sensor LMT84 is used to sense the heat sink temperature and is interfaced to the LaunchPad. Three Hall sensors embedded in the motor are connected to the LaunchPad connector directly.

The BEMF voltage feedback from the motor windings are attenuated and then are ESD protected by the transient voltage suppressor (TVS) diode array TPD4S009 before feeding to the C2000 LaunchPad. The software implementation on this design does not use the BEMF voltages and only uses the Hall sensors for rotor position sensing.

5 Highlighted Products

Key features of the highlighted devices are taken from product datasheets. The following are the highlighted products used in this reference design.

5.1 DRV8303

The DRV8303 is a gate driver IC for three-phase motor drive applications. The device provides three half-bridge drivers, each capable of driving two N-type MOSFETs (one for the high-side and one for the low-side). The DRV8303 supports up to a 2.3-A sink and a 1.7-A source peak current capability, and it only needs a single power supply with a wide range from 6 to 60 V. The DRV8303 uses bootstrap gate drivers with trickle charge circuitry to support 100% duty cycle. The gate driver uses automatic hand shaking when high-side FET or low-side FET is switching to prevent current shoot through. The V_{DS} of FETs is sensed to protect external power stage during overcurrent conditions. The DRV8303 includes two current shunt amplifiers for accurate current measurement. The current amplifiers support bi-directional current sensing and provide an adjustable output offset of up to 3 V. The SPI provides detailed fault reporting and flexible parameter settings such as gain options for current shunt amplifier and slew rate control of the gate driver.

5.2 CSD18540Q5B

The CSD18540Q5B is a 60-V N-Channel NexFET Power MOSFET with ultra-low Q_g and Q_{gd} and a very low R_{DS_ON} of 1.8 mΩ and features very low total gate charge requirement. The CSD18540Q5B is available in very small package, SON5×6 mm with a peak current rating of 400 A and continuous drain current (package limited) of 100 A.

5.3 TPD4S009

The TPD4S009 provide system level ESD solution for high-speed differential lines. These devices offer four ESD clamp circuits for dual pair differential lines. The TPD4S009 offers an optional V_{CC} supply pin, which can be connected to system supply plane. A blocking diode at the V_{CC} pin enables the I_{off} feature for the TPD4S009. The TPD4S009 can handle live signal at the D+, D– pins when the V_{CC} pin is connected to 0 V. The V_{CC} pin allows all the internal circuit nodes of the TPD4S009 to be at known potential during start up time. However, connecting the optional V_{CC} pin to board supply plane does not affect the system level ESD performance of the TPD4S009. The TPD4S009 is offered in DBV, DCK, DGS, and DRY packages. The TPD4S009 comply with IEC 61000-4-2 (Level 4) ESD. The TPD4S009 is characterized for operation over the ambient air temperature range of –40°C to 85°C.

5.4 TPS54061

The TPS54061 device is a 60-V, 200-mA, synchronous step-down DC-DC converter with integrated high-side and low-side MOSFETs. Current mode control provides simple external compensation and flexible component selection. The non-switching supply current is 90 µA. Using the enable pin, shutdown supply current is reduced to 1.4 µA. To increase light load efficiency, the low-side MOSFET emulates a diode when the inductor current reaches zero. Undervoltage lockout (UVLO) is internally set at 4.5 V but can be increased using two resistors on the enable pin. The output voltage startup ramp is controlled by the internal slow start time. The adjustable switching frequency range allows efficiency and external component size to be optimized. Frequency fold back and thermal shutdown protects the part during an overload condition. The TPS54061 enables small designs by integrating the MOSFETs, boot recharge diode, and minimizing the IC footprint with a small 3×3-mm thermally enhanced VSON package.

5.5 LMT84

The LMT84 is precision CMOS integrated-circuit temperature sensors with an analog output voltage that is linearly and inversely proportional to temperature. Its features make it suitable for many general temperature sensing applications. The LMT84 can operate down to a 1.5-V supply with a 5.4-µA power consumption, making the device ideal for battery-powered devices. Multiple package options, including through-hole TO-92 and TO-126 packages, also allow the LMT84 to be mounted on board, off board, to a heat sink, or on multiple unique locations in the same application. Class-AB output structures gives the LMT84 strong output source and sink current capability that can directly drive up to 1.1-nF capacitive loads. This capability means the device is well suited to drive an analog-to-digital converter sample-and-hold input with its transient load requirements. The LMT84 has accuracy capability specified in the operating range of −50°C to 150°C. The accuracy, three-lead package options, and other features also make the LMT84 an alternative to thermistors.

6 System Design Theory

6.1 Main Power Input

The main power input section is shown in Figure 5. The input bulk aluminum electrolytic capacitors C20 and C21 provide the ripple current and its voltage rating is de-rated by 50% for better life. These capacitors are rated to carry a high ripple current of 2.8 A. C22 and C24 are used as bypass capacitors to GND. D3 is the TVS having a breakdown voltage of 53.2 V and a stand-off voltage of 47.8 V.

The input supply voltage +PVDD is scaled using the resistive divider network, which consists of R20, R22, and C23, and fed to the MCU. Considering the maximum voltage for the MCU ADC input as 3.3 V, the maximum DC input voltage measurable by the MCU is calculated as in Equation 2.

$$V_{DC}^{max} = V_{ADC\_DC}^{max} \times \frac{(2.20\ k\Omega + 34.8\ k\Omega)}{2.20\ k\Omega} = 3.3 \times \frac{(2.20\ k\Omega + 34.8\ k\Omega)}{2.20\ k\Omega} = 55.5\ V \quad (2)$$

Considering a 20% headroom for this value, the maximum recommended voltage input to the system is 55.5 × 0.8 = 44.4, so for a power stage with maximum operating voltage of 42 V, this voltage feedback resistor divider is ideal. Also, this choice gives optimal ADC resolution for a system operating from 36 to 42 V.

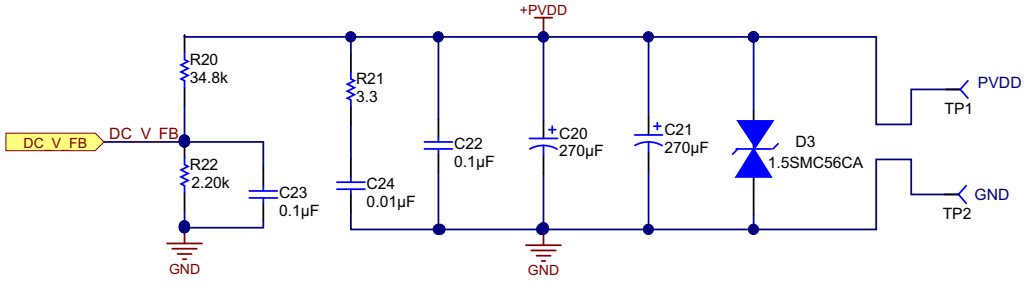


Figure 5. Main Power Input

6.2 Inverter Stage

The power circuit shown in Figure 6 consists of a three-leg MOSFET bridge. The DC bus return current is measured using the current sense resistors R51 and R61 that are in parallel. The sensed currents are fed to the MCU through the current shunt amplifiers. A gate resistance of 10 Ω is used at the input of all MOSFET gates. C28, C29, and C30 are the decoupling capacitors connected across each inverter leg.

NOTE: Connect these decoupling capacitors very near to the corresponding MOSFET legs for better decoupling (see Section 9.3). An improper layout or position of the decoupling capacitors can cause undesired V_{DS} switching voltage spikes and unintentional fault detection by the V_{DS} sensing overcurrent operation of the DRV8303.

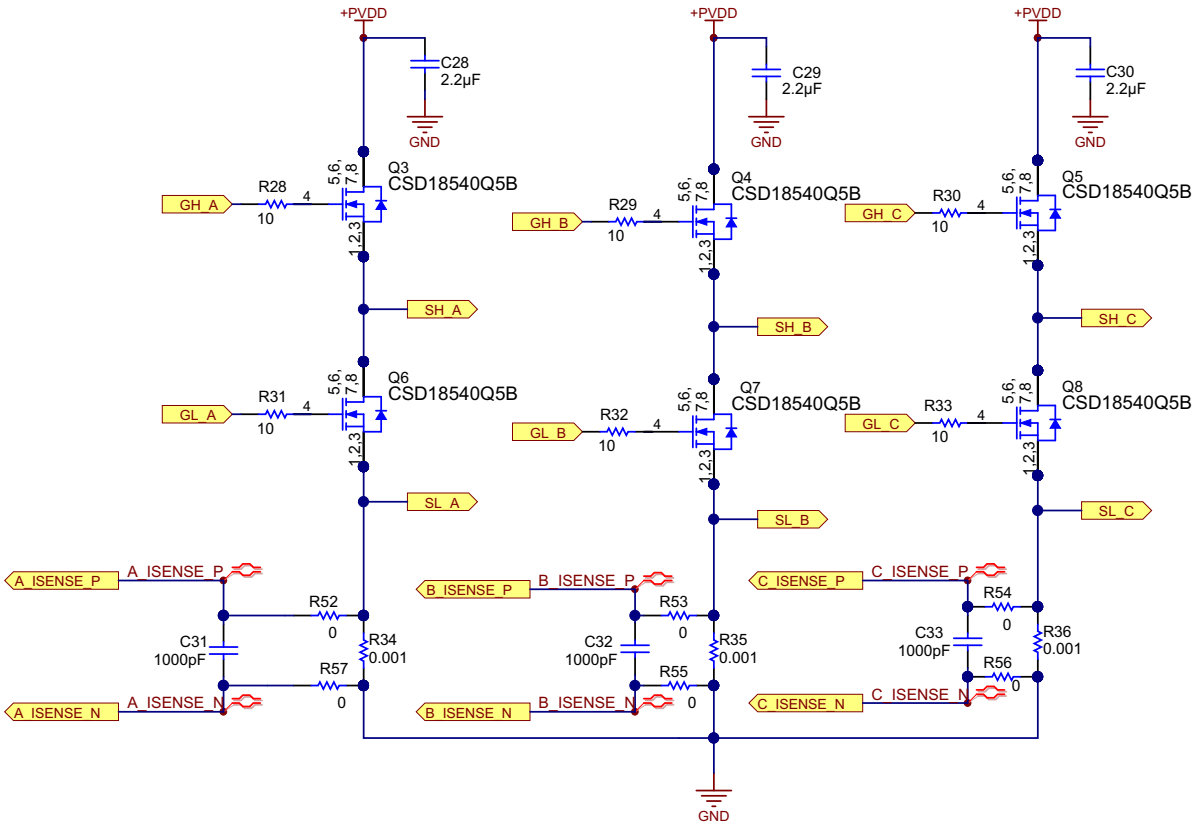


Figure 6. Three-Phase Inverter of Power Stage

6.2.1 Selection of the MOSFET

The board is designed to operate from a 10-cell lithium-ion battery voltage ranging from 30 to 42 V, meaning the maximum input DC voltage in the application is 42 V. Considering the safety factor and switching spikes, the MOSFET with a voltage rating of 1.5 times the maximum input voltage can be selected. A MOSFET with voltage rating greater than or equal to 60 V will be suitable for this application.

The current rating of the MOSFET depends on the peak winding current. The power stage has to provide a 30-A nominal current to the motor winding. Considering an overloading 120%, the peak winding current will be 36 A.

For better thermal performance, select the MOSFETs with very low R_{DS_ON}. In the reference design, the MOSFET CSD18540Q5B is selected, which is a 60-V N-Channel NexFET power MOSFET with a very low R_{DS_ON} of 1.8 mΩ and features very low total gate charge requirement. It has continuous drain current capacity (package limited) of 100 A and a peak current capacity of 400 A.

6.2.2 Selection of the Sense Resistor

Power dissipation in sense resistors and the input offset error voltage of the op-amps are important in selecting the sense resistance values. The rated motor winding current is 30 A; in a single commutation, a phase pair is energized where current path enters one phase and exits from the second phase with the third phase floating. Therefore, the sense resistors in the DC-Link minus will be carrying a current equal to the motor winding current of 30 A. The resistance value of a high current sense increases the power loss in the resistors; therefore, a lower value of resistance is preferable.

Selecting a 0.5-mΩ resistor as the sense resistor, the power loss in the resistor at 30 A is given by Equation 3:

$$\text{Power loss in the resistor} = I^2 \times R_{SENSE} = 30^2 \times 0.0005 = 0.45\ \text{W} \quad (3)$$

Therefore, a standard 2-W, 2512-package resistor can be used. For the 30-A current, the sense voltage across the resistor has a peak value of 15 mV, and with the proper gain setting for PGA of the DRV8303, the MCU can measure the current precisely.

6.3 DRV8303 — Three-Phase Gate Driver

The DRV8303 is used as the gate driver IC for the three-phase motor drive. The device provides three half-bridge drivers, each capable of driving two N-type MOSFETs, one for the high-side and one for the low-side. Figure 7 shows the schematic of the gate driver section.

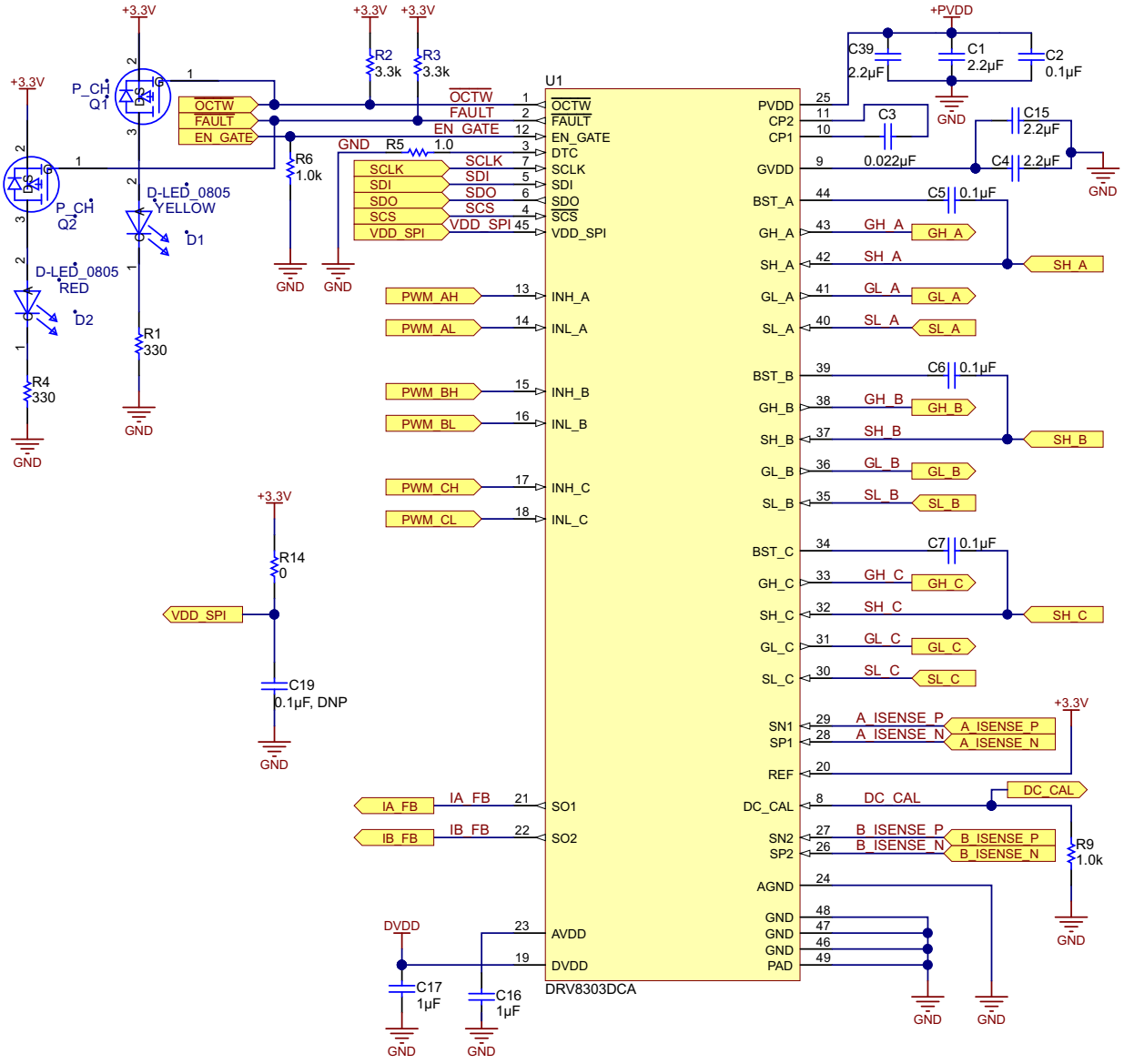


Figure 7. DRV8303 Schematic

The gate driver has following features:

- Internal handshake between high-side and low-side FETs during switching transition to prevent current shoot through
- Programmable slew rate or current driving capability through SPI
- Supports up to 200-kHz switching frequency with Q_g(TOT) = 25 nC or total 30-mA gate drive average current
- Provide cycle-by-cycle current limiting and latch overcurrent shut down of external FETs. Current is sensed through FET V_{DS} and the overcurrent level is programmable through SPI. V_{DS} sensing range is programmable from 0.060 to 2.4 V with 5-bit resolution
- High-side gate drive will survive negative output from half bridge up to –10 V for 10 ns
- During EN_GATE pin low and fault conditions, the gate driver keeps external FETs in high impedance mode
- Programmable dead time through DTC pin. Dead time control range: 50 to 500 ns. Shorting DTC pin to ground will provide minimum dead time of 50 ns. External dead time will override internal dead time as long as the time is longer than the dead time setting
- Bootstraps circuits are used to drive high-side FETs of three-phase inverter. Trickle charge circuitry is used to replenish current leakage from bootstrap cap and support 100% duty cycle operation

In Figure 7, C1, C2, and C39 are the PVDD decoupling capacitors. PVDD decoupling capacitors should be placed close to their corresponding pins with a low impedance path to device GND (PowerPAD; see Section 9.3 for more details). PVDD is the power supply pin for gate driver. The DRV8303 provides power stage undervoltage protection by driving its outputs low whenever PVDD is below 6 V (PVDD_UV). The PVDD undervoltage will be reported through $\overline{\text{FAULT}}$ pin and SPI status register. C5, C6, and C7 are the bootstrap capacitors. The detailed design and features of the DRV8303 are explained in the following sections.

6.3.1 Internal Regulator Voltages of DRV8303

AVDD
AVDD is the internal 6-V supply voltage. Connect the AVDD capacitor to the AGND. AVDD is an output, but not specified to drive external circuitry. In the schematic, C16 is used as the AVDD capacitor with a recommended value of 1 µF. Typical AVDD voltage is 6.5 V. The minimum specified value is 6 V and a maximum of 7 V.

DVDD
Internal 3.3-V supply voltage. Connect the DVDD capacitor to the AGND. DVDD is an output, but not specified to drive external circuitry. In the schematic, C17 is used as the DVDD capacitor with a recommended value of 1 µF. Place AVDD and DVDD capacitors close to their corresponding pins with a low impedance path to the AGND pin (see Section 9.3 for more details). Make this connection on the same layer. Tie AGND to the device GND (PowerPAD) through a low-impedance trace or copper fill. Typical DVDD voltage is 3.3 V. The minimum specified value is 3 V and maximum is 3.6 V. If DVDD goes to undervoltage, the external FETs go to high-impedance state by means of weak pull down of all gate driver output. On recovering from undervoltage, the DRV8303 resets the SPI registers. The DVDD undervoltage will be reported through $\overline{\text{FAULT}}$ pin.

GVDD
GVDD is the voltage output from internal gate driver voltage regulator. The capacitor C15 is connected to the GVDD pin. Connect the GVDD capacitor to GND. Typically, use a 2.2-µF ceramic capacitor as the GVDD capacitor. Place the GVDD capacitor close to its corresponding pin with a low-impedance path to device GND (PowerPAD; see Section 9.3 for more details). GVDD pin is protected from undervoltage and overvoltage. The undervoltage protection limit is 7.5 V and overvoltage protection limit is 16 V. When undervoltage protection is triggered, the DRV8303 outputs are driven low and the external MOSFETs will go to a high-impedance state. The GVDD undervoltage will be reported through $\overline{\text{FAULT}}$ pin and SPI status register. The GVDD overvoltage fault is a latched fault and can only be reset through a transition on EN_GATE pin. The GVDD overvoltage will be reported through $\overline{\text{FAULT}}$ pin and SPI status register.

6.3.2 Current Shunt Amplifiers in DRV8303

The DRV8303 includes two high performance current shunt amplifiers for accurate current measurement. The current amplifiers provide output offset up to 3 V to support bidirectional current sensing. The current shunt amplifier has following features:

- Programmable gain: Four gain settings (10, 20, 40, 80) are possible through SPI command
- Programmable output offset through reference pin (half of the V_{ref})
- Minimize DC offset and drift over temperature with DC calibration through SPI command or DC_CAL pin. When DC calibration is enabled, the device will short input of current shunt amplifier and disconnect the load. DC calibrating can be done at any time even when FET is switching because the load is disconnected. For best results, perform the DC calibrating during the switching off period when no load is present to reduce the potential noise impact to the amplifier

The output of current shunt amplifier can be calculated as:

$$V_O = \frac{V_{ref}}{2} - G \times (SN_X - SP_X) \quad (4)$$

where

- V_{ref} is the reference voltage
- G is the gain of the amplifier
- SN_X and SP_X are the inputs of channel X

Connect SP_X to the resistor ground for the best common mode rejection.

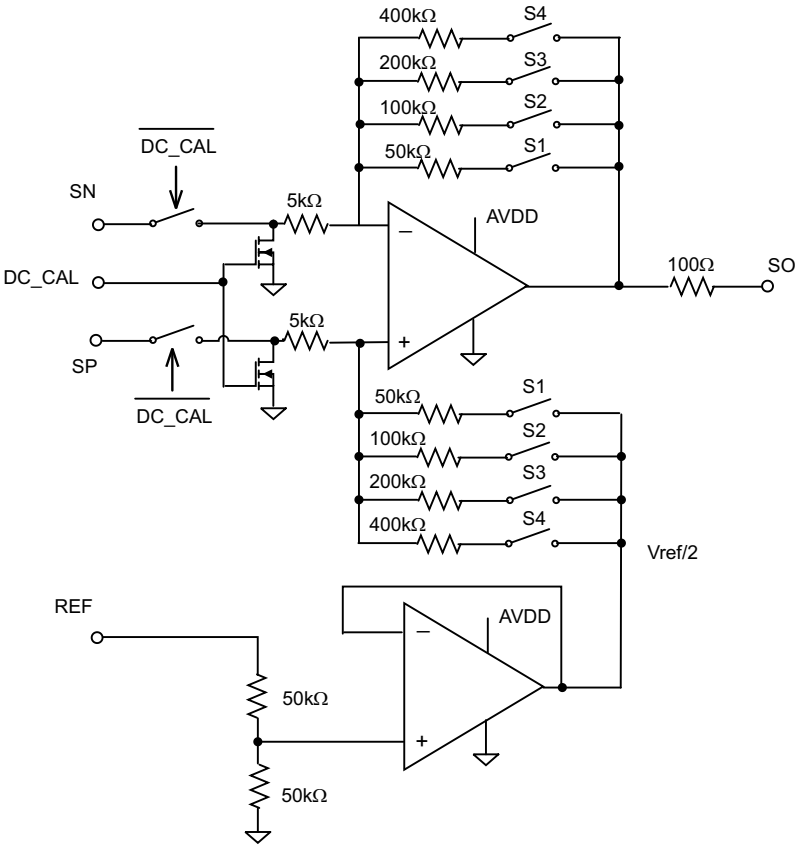


Figure 8. Simplified Block Diagram of Current Shunt Amplifier in DRV8303

6.3.3 Protection Features in DRV8303

Overcurrent Protection and Reporting

To protect the power stage from damage due to high currents, a V_{DS} sensing circuitry is implemented in the DRV8303. Based on the R_{DS_ON} of the power MOSFETs and the maximum allowed drain current, a voltage threshold can be calculated, which, when exceeded, triggers the overcurrent protection feature. This voltage threshold level is programmable through SPI command.

There are total four OC_MODE settings in SPI:

1. Current limit mode
   When current limit mode is enabled, the DRV8303 limits the MOSFET current instead of shutting down during the overcurrent event. The overcurrent event is reported through the overcurrent temperature warning ($\overline{\text{OCTW}}$) pin. $\overline{\text{OCTW}}$ reporting will hold low during same PWM cycle or for a max 64-µs period (internal timer) so that the external controller has enough time to sample the warning signal. If in the middle of reporting other FETs get overcurrent, then $\overline{\text{OCTW}}$ reporting will hold low and recount another 64 µs unless PWM cycles on both FETs are ended.

   There are two current control settings in current limit mode (selected by one bit in SPI and default is CBC mode):

   - Setting 1 (CBC mode): During an overcurrent event, the FET that detected the overcurrent will turn off until next PWM cycle.
   - Setting 2 (off-time control mode):
     - During an overcurrent event, the FET that detected the overcurrent will turn off for 64 µs as off time and back to normal after that (so the same FET will be on again) if PWM signal is still holding high. Since all three phases or six FETs share a single timer, if more than one FET get overcurrent, the FETs will not be back to normal until the all FETs that have the overcurrent event pass 64 µs.
     - If PWM signal is toggled for this FET during timer running period, the device will resume normal operation for this toggled FET. In this case, the real off time could be less than 64 µs.
     - If two FETs get overcurrent and one FET's PWM signal gets toggled during the timer running period, this FET will be back to normal, and the other FET will be off until the timer ends (unless its PWM is also toggled).
2. Overcurrent latch shutdown mode
   When overcurrent occurs, the device will turn off both high-side and low-side FETs in the same phase if any of the FETs in that phase have overcurrent.
3. Report only mode
   No protection action will be performed in this mode. Overcurrent detection will be reported through the $\overline{\text{OCTW}}$ pin and SPI status register. External MCU takes actions based on its own control algorithm. A pulse stretching of 64 µs will be implemented on $\overline{\text{OCTW}}$ pin so the controller can have enough time to sense the overcurrent signal.
4. Overcurrent disable mode
   The device will ignore all the overcurrent detections and will not report them either.

Undervoltage Protection

To protect the power stage during undervoltage conditions, the DRV8303 provides power stage undervoltage protection by driving its outputs low whenever PVDD is below 6 V (PVDD_UV) or GVDD is below 7.5 V (GVDD_UV). When undervoltage protection is triggered, the DRV8303 outputs are driven low and the external MOSFETs will go to a high impedance state.

Overvoltage Protection (GVDD_OV)

The DRV8303 will shut down both the gate driver and charge pump if GVDD voltage exceeds 16 V to prevent potential issue related to the GVDD or charge pump (for example, short of external GVDD cap or charge pump). The fault is a latched fault and can only be reset through a transition on EN_GATE pin.

Over Temperature Protection

A two-level over temperature detection circuit is implemented in the DRV8303:

- Level 1: over temperature warning (OTW). OTW is reported through $\overline{\text{OCTW}}$ pin for default setting. The $\overline{\text{OCTW}}$ pin can be set to report OTW or overcurrent warning only through SPI command.
- Level 2: over temperature latched shut down of gate driver and charge pump (OTSD_GATE). The fault will be reported to the $\overline{\text{FAULT}}$ pin. This pin is a latched shut down, so the gate driver will not be recovered automatically—even over temperature condition is not present anymore. An EN_GATE reset through pin or SPI (RESET_GATE) is required to recover gate driver to normal operation after temperature goes below a preset value, t_{OTSD_CLR}. SPI operation is still available and register settings will be remaining in the device during OTSD operation as long as PVDD is still within defined operation range.

Junction temperature for resetting over temperature warning (OTW_CLR) is 115°C. Junction temperature for the over temperature warning and resetting over temperature shutdown (OTW_SET/OTSD_CLR) is 130°C.

Fault and Protection Handling

The $\overline{\text{FAULT}}$ pin indicates an error event (with shutdown) has occurred such as overcurrent, over temperature, overvoltage, or undervoltage. Note that $\overline{\text{FAULT}}$ is an open-drain signal. $\overline{\text{FAULT}}$ will go high when gate driver is ready for PWM signal (internal EN_GATE goes high) during start up. The $\overline{\text{OCTW}}$ pin indicates overcurrent event and over temperature event that not necessary related to shut down. $\overline{\text{OCTW}}$ is an open-drain signal.

EN_GATE

EN_GATE low is used to put the gate driver, charge pump, current shunt amplifier, and internal regulator blocks into a low-power consumption mode to save energy. SPI communication is not supported during this state. The device will put the MOSFET output stage to a high-impedance mode as long as PVDD is still present. When EN_GATE pin goes high, it will go through a power-up sequence, and enable gate driver, current amplifiers, charge pump, internal regulator, and so on and reset all latched faults related to the gate driver block. The pin will also reset status registers in the SPI table. All latched faults can be reset when EN_GATE is toggled after an error event unless the fault is still present. When EN_GATE goes from high to low, it will shut down gate driver block immediately, so the gate output can put external FETs in high impedance mode. It will then wait for 10 µs before completely shutting down the rest of the blocks.

A quick fault reset mode can be done by toggling EN_GATE pin for a very short period (less than 10 µs). This will prevent device to shut down other function blocks such as charge pump and internal regulators and bring a quicker and simple fault recovery. SPI will still function with such a quick EN_GATE reset mode. The other way to reset all the faults is to use SPI command (RESET_GATE), which will only reset gate driver block and all the SPI status registers without shutting down other function blocks. One exception is to reset a GVDD_OV fault. A quick EN_GATE quick fault reset or SPI command reset will not work with GVDD_OV fault. A complete EN_GATE with low level holding longer than 10 µs is required to reset GVDD_OV fault. Inspect the system and board when GVDD_OV occurs.

DTC

Dead time can be programmed through DTC pin. Connect a resistor from DTC to ground to control the dead time. Dead time control range is from 50 to 500 ns. A short DTC pin to ground will provide the minimum dead time (50 ns). The resistor range is 0 to 150 kΩ. Dead time is linearly set over this resistor range. Current shoot through prevention protection is constantly enabled in the device, independent of dead time setting and input mode setting. In the reference design, a 1-Ω resistor is connected to the DTC pin.

6.3.4 SPI Communication

VDD_SPI
VDD_SPI is the power supply to power SDO pin. It has to be connected to the same power supply (3.3 V or 5 V) that the MCU uses for its SPI operation. During power up or down transient, VDD_SPI pin could be zero voltage shortly. During this period, no SDO signal should be present at the SDO pin from any other devices in the system because it causes a parasitic diode in the DRV8303 conducting from SDO to VDD_SPI pin as a short. This should be considered and prevented from system power sequence design.

DC_CAL
When DC_CAL is enabled, the device will short inputs of the shunt amplifier and disconnect from the load, so the external microcontroller (or SPI command) can calibrate the DC offset. Using the SPI exclusively for DC calibration, the DC_CAL pin can be connected to GND.

SPI Pins
The SDO pin has to be 3-state, so a data bus line can be connected to multiple SPI slave devices. The SCS pin is active low. When SCS is high, SDO is at high impendence mode.

SPI
SPI is used to set device configuration, operating parameters and read out diagnostic information. The DRV8303 SPI operates in the slave mode. The SPI input data (SDI) word consists of 16-bit word, with 11-bit data and 5-bit (MSB) command. The SPI output data (SDO) word consists of 16-bit word, with 11-bit register data and 4-bit MSB address data and one frame fault bit (active 1). When a frame is not valid, frame fault bit will set to 1, and the rest of SDO bits will shift out zeroes.

A valid frame has to meet following conditions:

1. The clock must be low when /SCS goes low.
2. The clock must have 16 full cycles.
3. The clock must be low when /SCS goes high.

When SCS is asserted high, any signals at the SCLK and SDI pins are ignored, and SDO is forced into a high impedance state. When SCS transitions from high to low, SDO is enabled and the SPI response word loads into the shift register based on 5-bit command in SPI at the previous clock cycle. The SCLK pin must be low when SCS transitions low. While SCS is low, at each rising edge of the clock, the response bit is serially shifted out on the SDO pin with MSB shifted out first. While SCS is low, at each falling edge of the clock, the new control bit is sampled on the SDI pin. The SPI command bits are decoded to determine the register address and access type (read or write). The MSB will be shifted in first. If the word sent to SDI is less than 16 bits or more than 16 bits, it is considered a frame error. If it is a write command, the data will be ignored. The fault bit in SDO (MSB) will report 1 at the next 16-bit word cycle. After the 16^{th} clock cycle or when SCS transitions from low to high, in case of write access type, the SPI receive shift register data is transferred into the latch where address matches decoded SPI command address value. Any amount of time may pass between bits as long as SCS stays active low, which allows two 8-bit words to be used.

For a read command (N^{th} cycle) in SPI, SPO will send out data in the register with address in read command in next cycle (N+1). For a write command in SPI, SPO will send out data in the status register 0x00h in next 16-bit word cycle (N+1). For most of the time, this feature will maximize SPI communication efficiency when having a write command, but still get fault status values back without sending extra read command.

SPI Format
An SPI input data control word is 16 bits long, consisting of:

- 1 read or write bit W [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

An SPI output data response word is 16 bits long, and its content depends on the given SPI command (SPI Control Word) in the previous cycle. When an SPI Control Word is shifted in, the SPI Response Word (that is, shifted out during the same transition time) is the response to the previous SPI Command (shift in SPI Control Word 'N' and shift out SPI Response Word "N-1"). Therefore, each SPI Control and Response pair requires two full 16-bit shift cycles to complete. The definitions of all SPI registers are given in the DRV8303 datasheet (SLOS846).

6.4 Motor Current Sensing — Settings

The motor current sensing amplifier gain has to be designed to get maximum resolution from the ADC of the MCU. Considering the external shunt amplifier, the output of the current shunt amplifier can be written as in Equation 5:

$$\text{Output of the current shunt amplifier} = 1.65 + \left(I_C \times R_{SENSE} \times \text{AMPLIFIER\_GAIN}\right) \quad (5)$$

Here, I_C is the phase C leg current. Equation 5 is also valid for the current shunt amplifiers in the DRV8303 used for phase A and phase B leg current sensing. The maximum leg current feedback measurable by the MCU can be calculated as follows, considering the maximum voltage for the ADC input is 3.3 V:

If I_a^{max} is the peak value of the DC-Link return current measurable by the ADC, then

$$1.65 + (I_a^{max} \times R_{SENSE} \times \text{AMPLIFIER\_GAIN}) = V_{ADC\_Ia}^{max} \quad (6)$$

$$I_a^{max} = \frac{\left(V_{ADC_{Ia}}^{max} - 1.65\right)}{R_{SENSE} \times \text{AMPLIFIER\_GAIN}} = \frac{(3.3 - 1.65)}{0.0005 \times 40} = 82.5 \quad (7)$$

Therefore, the maximum current measurable by the ADC is 82.5 A. As the PGA output is offset by 1.65 V, both directions of the current can be measured ±82.5 A.

6.5 Motor Winding Voltage Sensing

The voltage divider circuit shown in the Figure 9 is used to measure the BEMF of the un-energized winding. BEMF feedback is needed for sensorless control to estimate the position of the rotor for accurate commutation.

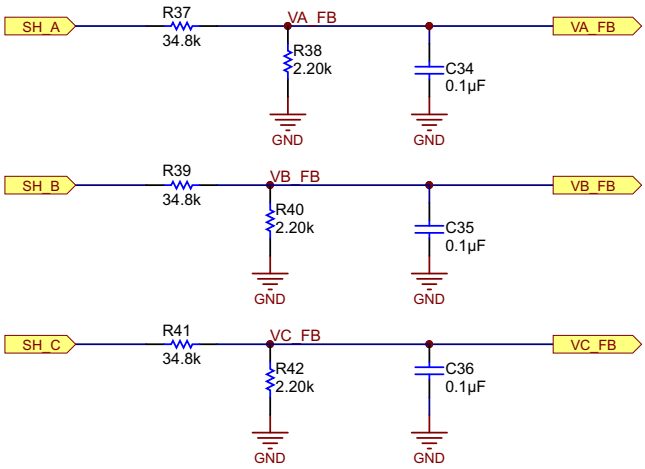


Figure 9. Motor Winding Voltage Sense Circuit

In Figure 9, SH_A, SH_B, and SH_C are the phase voltages. These voltages are properly scaled and fed to the MCU through VA_FB, VB_FB, and VC_FB. The maximum phase voltage feedback measurable by the MCU can be calculated as follows, considering the maximum voltage for the ADC input is 3.3 V:

$$V_a^{max} = V_{ADC\_a}^{max} \times \frac{(2.20\ k\Omega + 34.8\ k\Omega)}{2.20\ k\Omega} = 3.3 \times \frac{(2.20\ k\Omega + 34.8\ k\Omega)}{2.20\ k\Omega} = 55.5\ V \quad (8)$$

Considering a 20% headroom for this value, the maximum voltage input to the system is recommended to be 55.5 × 0.8 = 44.4; for a motor with maximum operating voltage of 42 V, this voltage feedback resistor divider is ideal. This divider makes sure that the ADC resolution is maximum for a motor working from 36 to 42 V.

6.6 Design of 36-V to 3.3-V Step-Down DC-DC Converter

The 3.3-V regulated power supply for the board is derived using the switching converter TPS54061. The TPS54061 device is a 60-V, 200-mA, step-down (buck) regulator with an integrated high-side and low-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant frequency, current mode control, which reduces output capacitance and simplifies external frequency compensation design. The design specifications of the step-down converter are given in Table 2. The schematic of the step-down converter is shown in Figure 10.

Table 2. Design Specifications of Step-Down Converter

PARAMETER	VALUE
Conduction mode	Continuous conduction mode (CCM)
Output voltage	3.3 V
Maximum output current	150 mA
Input voltage	36 V nominal (36 to 42 V)
Output voltage ripple	0.5% of V_{OUT}
Start input voltage (rising V_{IN})	36 V
Stop input voltage (falling V_{IN})	30 V

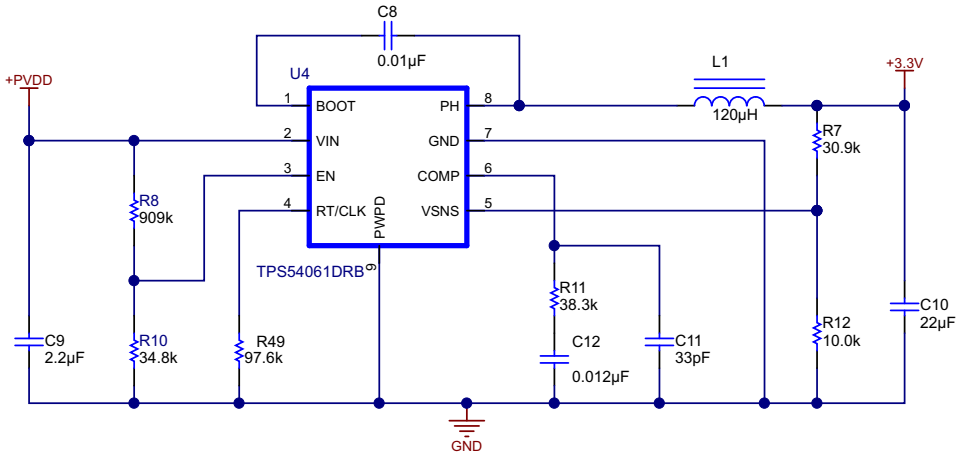


Figure 10. 36-V to 3.3-V Step-Down Converter

The following parameters symbols are used for the further analysis of the buck converter:

- $L_{O,min}$ — Minimum value of output inductor
- L_O — Output inductor
- $V_{IN,max}$ — Maximum value of input voltage
- $V_{IN,min}$ — Minimum value of input voltage
- V_{OUT} — Output voltage
- I_{OUT} — Average output current
- f_{sw} — Switching frequency

6.6.1 Selecting the Switching Frequency

The switching frequency of the TPS54061 is adjustable over a wide range, from 50 to 1100 kHz, by varying the resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.53 V and must have a resistor to ground to set the switching frequency. To reduce the solution size, set the switching frequency as high as possible; however, consider the tradeoffs of the supply efficiency, maximum input voltage, and minimum controllable on time. The minimum controllable on time is typically 120 ns and limits the operating frequency for high input voltages. To determine the timing resistance (R_T) for a given switching frequency, use Equation 9.

$$R_T\,(k\Omega) = \frac{71657}{f_{sw}\,(kHz)^{1.039}} \tag{9}$$

The switching frequency is set by resistor R49 shown in Figure 10. The reference design uses a switching frequency of 573 kHz.

6.6.2 Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use Equation 10:

$$L_{O,min} \geq \frac{V_{IN,max} - V_{OUT}}{K_{IND} \times I_O} \times \frac{V_{OUT}}{V_{IN,max} \times f_{sw}} = \frac{42 - 3.3}{0.4 \times 0.15} \times \frac{3.3}{42 \times 573 \times 10^3} = 89\,\mu H \tag{10}$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. This design uses a K_{IND} of 0.4. The minimum inductor value is calculated to be greater than 89 µH. For this design, a standard 120-µH value was chosen as the L_O. The inductor current ripple (I_{RIPPLE}), RMS inductor current ($I_L$rms), and peak inductor current ($I_L$peak) can be calculated using Equation 11 through Equation 13.

$$I_{RIPPLE} \geq \frac{V_{OUT} \times (V_{IN}\,max - V_{OUT})}{V_{IN}\,max \times L_O \times f_{sw}} = \frac{3.3 \times (42 - 3.3)}{42 \times 120 \times 10^{-6} \times 573 \times 10^3} = 44.22\,mA \tag{11}$$

$$I_L rms = \sqrt{I_O{}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN}\,max - V_{OUT})}{V_{IN}\,max \times L_O \times f_{SW}} \right)^2}$$

$$I_L rms = \sqrt{0.15^2 + \frac{1}{12} \times \left(\frac{3.3 \times (42 - 3.3)}{42 \times 120 \times 10^{-6} \times 573 \times 10^3} \right)^2} = 150\,mA \tag{12}$$

$$I_L peak = I_{OUT} + \frac{I_{RIPPLE}}{2} = 0.15 + \frac{0.04422}{2} = 0.172\,A \tag{13}$$

For this design, the RMS inductor current is 150 mA and the peak inductor current is 172 mA. The chosen inductor has a saturation current rating of 250 mA and an RMS current rating of 220 mA. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the calculated peak inductor current.

6.6.3 Output Capacitor

Consider these three aspects when selecting the value of the output capacitor: the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria. Equation 14 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where f_{sw} is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current.

$$C_{out} \geq \frac{I_{RIPPLE}}{V_{RIPPLE}} \times \left(\frac{1}{8 \times f_{sw}} \right) \tag{14}$$

Refer to the datasheet of TPS54061 for the detailed description of the capacitor selection (SLVSBB7). The reference design uses a 22-µF, 4-V X5R ceramic capacitor.

6.6.4 Bootstrap Capacitor Selection

Connect a 0.01-µF ceramic capacitor between the BOOT and PH pins for proper operation. Use a ceramic capacitor with X5R or better grade dielectric with a voltage rating of 10 V or higher.

6.6.5 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the V_{SENSE} pin. Use 1% tolerance or better divider resistors. Start with 10 kΩ for the R_{LS} resistor and use the Equation 15 to calculate R_{HS}.

$$R_{HS} = R_{LS} \times \left(\frac{V_{OUT} - 0.8\ V}{0.8\ V} \right) \tag{15}$$

Selecting R_{LS} = R12 = 10 k; To get V_{OUT} = 3.3 V

R_{HS} = R7 = 30.9 k (Selecting the standard value)

6.6.6 UVLO Set Point

The UVLO can be adjusted using an external voltage divider on the EN pin of the TPS54061. The UVLO has two thresholds: one for power up when the input voltage is rising, and one for power down or brown outs when the input voltage is falling. The programmable UVLO and enable voltages are set by connecting the resistor divider between +PVDD and ground to the EN pin. Equation 16 and Equation 17 can be used to calculate the resistance values necessary.

$$R8 = R_{UVLO}1 = \frac{V_{START}\left(\frac{V_{ENAFALLING}}{V_{ENARISING}} \right) - V_{STOP}}{I_1 \times \left(1 - \frac{V_{ENAFALLING}}{V_{ENARISING}} \right) + I_{HYS}} \tag{16}$$

$$R10 = R_{UVLO}2 = \frac{R_{UVLO}1 \times V_{ENAFALLING}}{V_{STOP} - V_{ENAFALLING} + R_{UVLO}1 \times \left(I_1 + I_{HYS} \right)} \tag{17}$$

From the datasheet of TPS54061:

- The EN pin rising threshold, $V_{ENARISING}$ = 1.23 V
- The EN pin falling threshold, $V_{ENAFALLING}$ = 1.18 V
- The EN pin internal pull up current, I_1 = 1.2 µA
- The hysteresis current, I_{HYS} = 3.5 µA

The UVLO feature can be used to protect the lithium-ion batteries from discharging below the safe voltage level. Generally, 3.6 V per cell is considered a safe voltage to operate the batteries safely. General standard of discharge protection voltage is 2.75 V. Sometimes, 3.0 V is a safer setting. Considering 3.0 V per cell as the protection voltage on discharge for the 10-cell unit, disconnect the battery when the battery unit voltage reaches 30 V to avoid further discharge. Considering these values, the UVLO thresholds for the reference design are:

- The power up threshold, V_{START} = 33 V
- The power down threshold, V_{STOP} = 30 V

Using the above design vales, a 909-kΩ resistor between +PVDD and EN and a 34.8-kΩ resistor between EN and ground are required to produce the 33-V and 30-V start and stop voltages, respectively.

6.7 Heat Sink Temperature Sensor

Figure 11 shows the temperature sensor circuit used to measure the heat sink temperature. The LMT84 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage, thus providing a low-impedance output source. The average output sensor gain is –5.5 mV/°C.

Although the LMT84 is very linear, its response does have a slight parabolic shape. The output voltages at different temperatures are given in the datasheet of LMT84 in tabular form (SNIS167). For an even less accurate linear approximation, a line can easily be calculated over the desired temperature range using the two-point equation of a line. Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

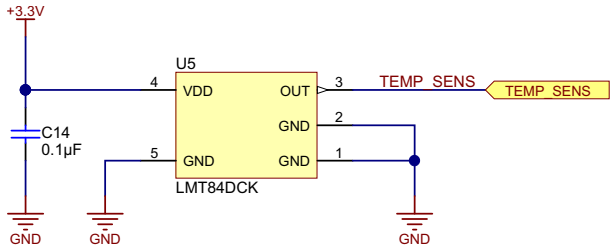


Figure 11. Heat Sink Temperature Sensor

6.8 LaunchPad Connections

Figure 12 shows the LaunchPad connections. The C2000 LAUNCHXL-F28027 LaunchPad is used in the testing. The TPD4S009 provides system level ESD protection in the voltage feedback signal lines. The current sense feedback signals from the current shunt amplifiers are filtered and fed to the LaunchPad. The TEMP_SENS is the signal from the temperature sensor, $\overline{\text{FAULT}}$ and $\overline{\text{OCTW}}$ signals from the DRV8303 are also connected to the LaunchPad so that the MCU can be programmed to take necessary action during these fault events. The signal connections SCLK, SCS, SDI, and SDO are required for the SPI programming of the DRV8303. The DC offset calibration of the shunt amplifiers in the DRV8303 are controlled through DC_CAL signal. EN_GATE is used to enable gate driver and current shunt amplifiers of the DRV8303.

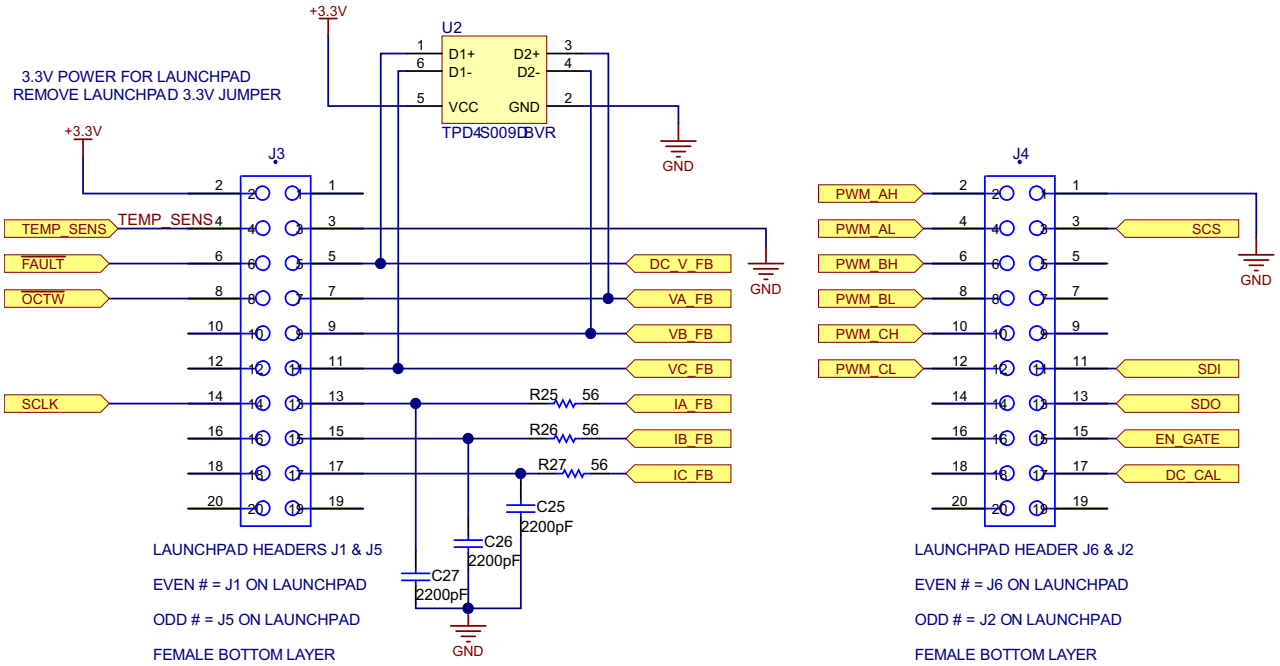


Figure 12. LaunchPad Connections for C2000 LAUNCHXL-F28027 LaunchPad

6.9 Fault Indications

The DRV8303 fault indication outputs $\overline{\text{OCTW}}$ and $\overline{\text{FAULT}}$ are pulled up and connected to two LED indications as shown in Figure 13. Table 3 shows the faults in the DRV8303 indicated through the two fault reporting output pins.

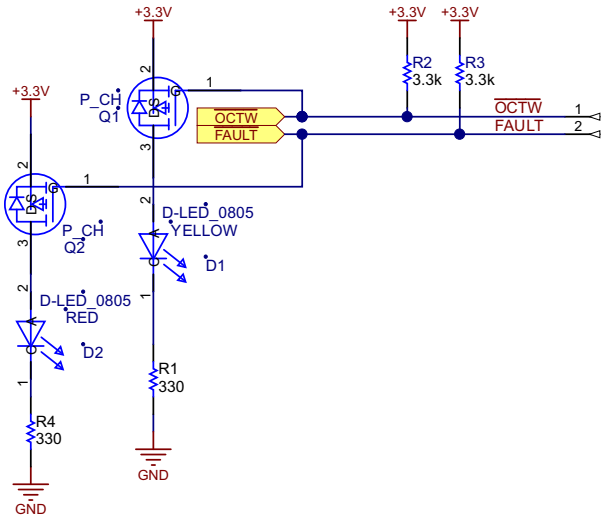


Figure 13. Fault Indication Through LED

Table 3. Fault Events Reporting from DRV8303

REPORTING PIN	FAULT EVENTS
$\overline{\text{FAULT}}$	PVDD Undervoltage
	DVDD undervoltage
	GVDD undervoltage
	GVDD overvoltage
	OTSD_GATE — Gate driver latched shut down
	External FET Overload — Latch mode
$\overline{\text{OCTW}}$	OTW — Over temperature
	OTSD_GATE — Gate driver latched shut down
	External FET Overload — Current limit mode
	External FET Overload — Latch mode
	External FET Overload — Reporting only mode

6.10 Hall Sensor Feedback

This design uses Hall sensor feedback for commutation. Figure 14 shows the connection of the Hall sensor from motor to the C2000 LaunchPad. The Hall sensors are typically open drain outputs and require pull-ups as shown in Figure 14. The Hall interface is not given on the power stage and is connected directly to C2000 LaunchPad.

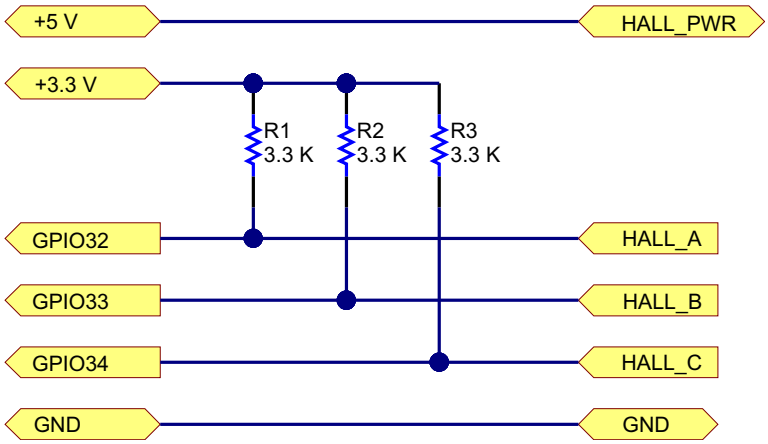


Figure 14. Hall Sensor Interface to LAUNCHXL-F28027 LaunchPad

7 Getting Started — Firmware

The firmware is developed using Code Composer Studio™ (CCS). Firmware uses files from controlSUITE™, which include TMS320F2027 Device specific C source, and header files the motor control application libraries. The CCS project can be downloaded from TIDA-00436.

The firmware is based on the DRV8312-C2-KIT, which is a motor control kit using the DRV8312. The reference firmware for Hall-sensored trapezoidal control can be found in DRV8312-C2-KIT project folder in controlSUITE. Refer to *Trapezoidal Control of BLDC Motors Using Hall Effect Sensors* for the firmware documentations. This document explains the project is built in steps called build levels. The build levels allow the testing of the code systematically with each higher build level adding more features.

The testing of the cycle-by-cycle current limit feature of the DRV8303 uses build level 4. Figure 15 shows the block diagram of build level 4. The build level 4 of the firmware has a closed loop Hall commutation with no current control.

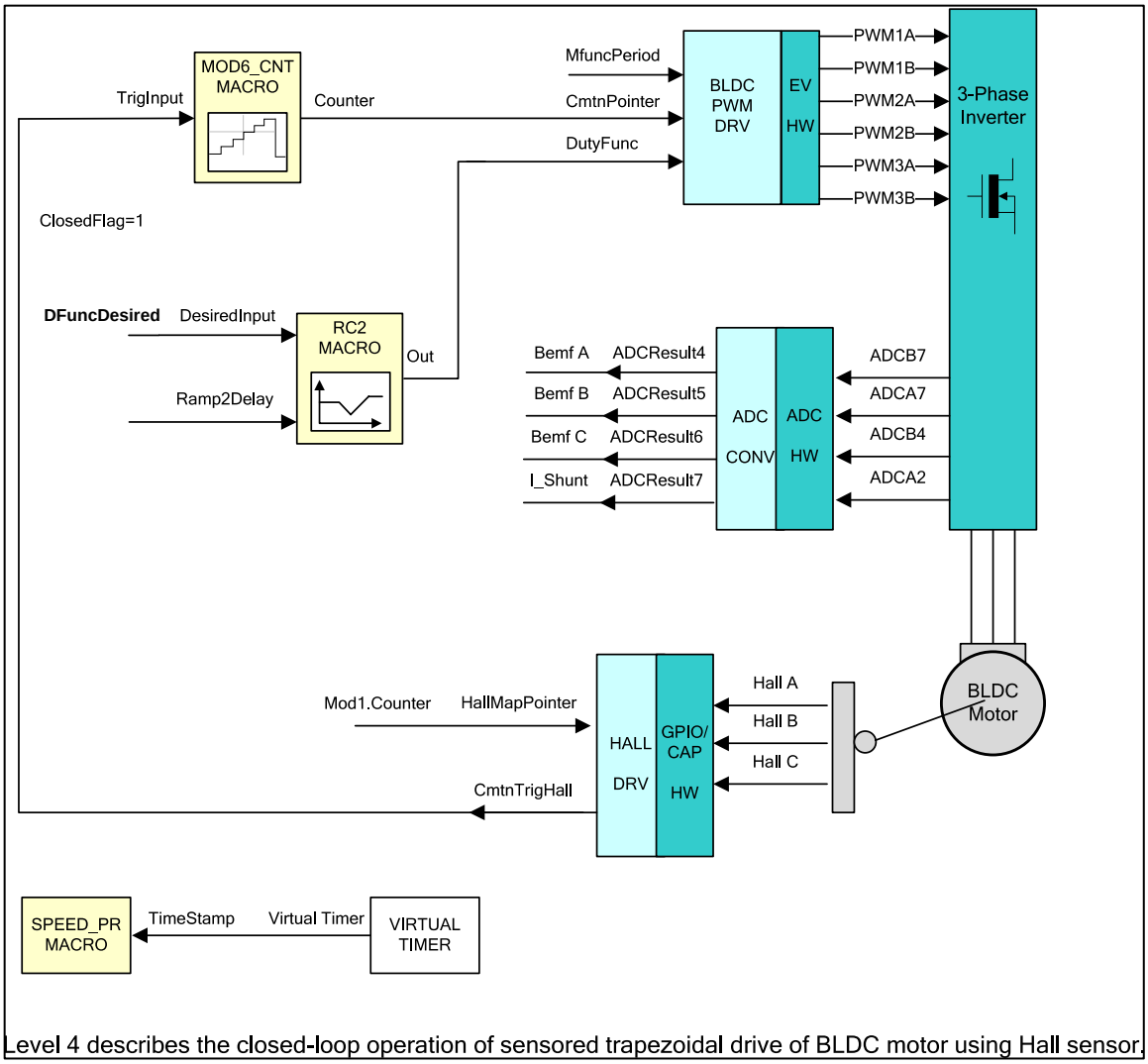


Figure 15. Level 4 Incremental System Build Block Diagram

The firmware block diagram in Figure 15 execute in the PWM interrupt routine. The entire block has to be calculated with the time for one PWM period, the Hall macro reads the Hall input every PWM cycle (20-kHz PWM) and does a software polling to de-glitch the Hall input to reject noise. CmtnTrigHall is an output form the HALL3_READ_MACRO, this is a trigger to change the commutation state. A hard-coded commutation table is used for 120° apart placement of three Hall sensors for clockwise rotation. MOD6_CNT_MACRO is used to generate pointer value for look up from the commutation table. BLDCPWM_MACRO outputs the required PWM sequence using the commutation table. DutyFunc is an input to the BLDCPWM_MACRO, which sets the duty of the PWM output. The required PWM duty is entered into the DFuncDesired variable, using the watch variables window of CCS IDE. The RC2_MACRO ramps up or ramps down the DutyFunc output variable to match the value of the DFuncDesired input variable. DFuncDesired is used to change the speed of the motor.

Input and Output Ports

Table 4 displays the inputs and outputs used for implementing Hall-sensored trapezoidal control. Except for the Hall feedback signals that are connected from motor to LaunchPad directly, the remaining signal are available on the header interfacing the power stage to the LaunchPad.

Table 4. Signals Used for Hall-Sensored Trapezoidal Control

HEADER, POSITION	SIGNAL NAME ON POWER STAGE	SIGNAL NAME ON C2000 LAUNCHPAD	COMMENT
J1.2	TEMP-FB	AIO6 ADCINA6	Temperature sensor
J5.7	IA-FB	ADCINB1	DC-Link current
J6.1	PWM-AH	GPIO0	Phase A high-side PWM
J6.2	PWM-AL	GPIO1	Phase A low-side PWM
J6.3	PWM-BH	GPIO2	Phase B high-side PWM
J6.4	PWM-BL	GPIO3	Phase B low-side PWM
J6.5	PWM-CH	GPIO4	Phase C high-side PWM
J6.6	PWM-CL	GPIO5	Phase C low-side PWM
J6.7		GPIO32	HALL_A; connect to LaunchPad
J6.8		GPIO33	HALL_B; connect to LaunchPad
J1.5		GPIO34	HALL_C; connect to LaunchPad
J2.2	SCS	GPIO19	DRV8303 SPI chip select
J2.6	SDI	GPIO16	DRV8303 SPI SIMO
J2.7	SDO	GPIO17	DRV8303 SPI SOMI
J1.7	SCLK	GPIO18	DRV8303 SPI clock
J2.8	EN-GATE	GPIO6	DRV8303 Enable
J2.9	DC-CAL	GPIO7	DRV8303 DC-CAL

Table 5 lists the additional signals that have not been used but are available for implementing sensorless trapezoidal control. Implement sensorless control by removing the Hall sensor feedback and replacing it with voltage feedbacks given in Table 5.

Table 5. Signals Available for Implementing Sensorless Control

HEADER, POSITION	SIGNAL NAME ON POWER STAGE	SIGNAL NAME ON C2000 LAUNCHPAD	COMMENT
J5.3	DC-V-FB	ADCINA7	DC-Link voltage feedback (not used)
J5.4	VA-FB	ADCINA3	Phase A motor BEMF feedback (not used)
J5.5	VB-FB	ADCINA1	Phase B motor BEMF feedback (not used)
J5.6	VC-FB	ADCINA0	Phase C motor BEMF feedback (not used)
J1.3	FAULT	GPIO28	DRV8303 fault signal (not used)
J1.4	OCTW	GPIO29	DRV8303 overcurrent and temperature warning (not used)

Required Modification on C2000 LaunchPad

1. Remove resistor R8, this resistor pulls down GPIO34, as GPIO34 is used for the Hall input.
2. Remove shorting jumpers on JP3 and JP5, which provide 3.3 V and 5 V respectively to the MCU on the LaunchPad. The power to the MCU will be provided from the BoosterPack. During testing, always power up the BoosterPack first and then connect the USB cable for emulation.
3. Open connections JP5, JP7, JP8, and JP10 while the shorts on JP4, JP6, JP9, and JP11 should be present. These jumpers are used to multiplex GPIO16, GPIO17, GPIO32, and GPIO33 to different location on the LaunchPad interface headers.

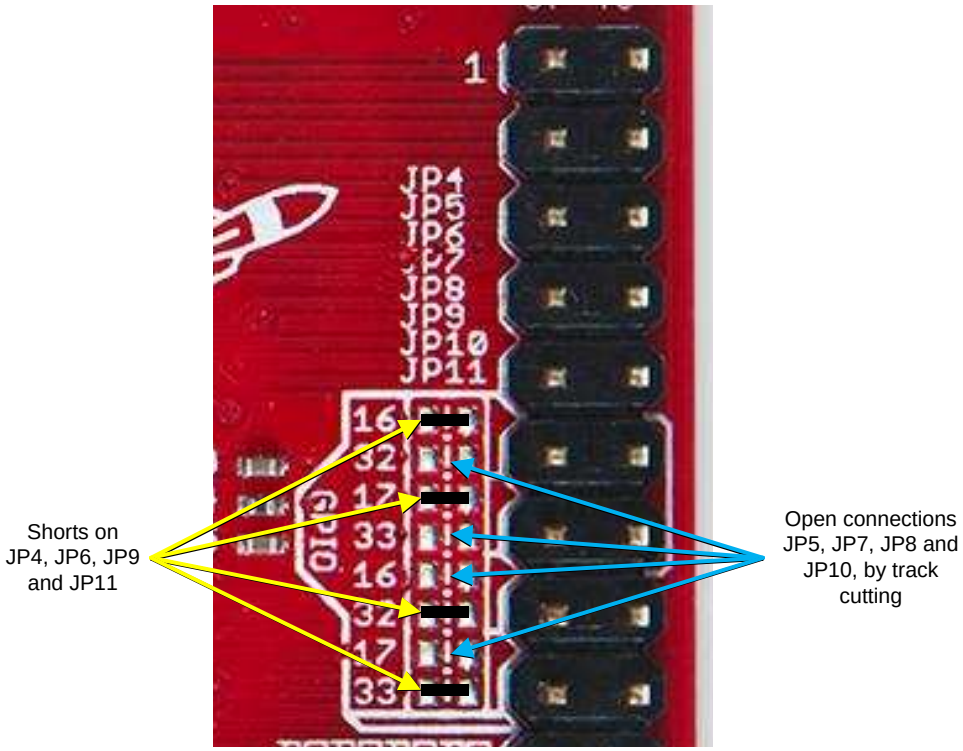


Figure 16. Jumper Modification on C2000 LaunchPad

Project Dependencies

Table 6 gives a list the resource folders used in the project. If the folder location is controlSUITE, they are linked to the project using include options from controlSUITE. All other project specific files are given in the TIDA-00436 software folder available from www.ti.com/tool/TIDA-00436.

Table 6. Project Resources

RESOURCE FOLDER	LOCATION
\device_support\f2802x\v220	controlSUITE
\libs\app_libs\motor_control\math_blocks\v3.1	controlSUITE
\device_support\f2802x\v220\f2802x_headers\include	controlSUITE
\device_support\f2802x\v220\f2802x_common\include	controlSUITE
\libs\app_libs\motor_control\drivers\f2802x_v2.0	TIDA00436_firmware
\development_kits\~SupportFiles\F2802x_headers_v2	TIDA00436_firmware

The project runs in CCS version 6, which can be installed from www.ti.com/tool/ccstudio. The project is imported into CCS using the *Project → Import CCS Eclipse* project feature. Browse to the downloaded TIDA-00436 software folder and import into CCS workspace. the project should build in CCS without error. The following steps are for operating the power stage from CCS.

1. Open BLDC_Sensored-Settings.h and select level 4 incremental build option by setting the BUILDLEVEL to LEVEL4 (#define BUILDLEVEL LEVEL4). Right click on the project name and click *Rebuild Project*. Once the build is complete click on debug button, reset CPU, restart, enable real time mode, and run. The required variable in the expression window can be loaded automatically by opening "AddWatchWindowVars_F2802x.js" in the scripting console. The expression window once populate is shown in Figure 17. The continuous refresh option should be enable to see the values while CPU is running.
2. Set "EnableFlag" to 1 in the watch window start motor rotation. The variable named "IsrTicker" will be incrementally increased as seen in watch windows to confirm the interrupt working properly. Now the motor is running with default DFuncTesting value.
3. Vary the motor speed by changing the PWM duty ratio represented by DFuncDesired. Double-click on DFuncDesired in the watch window, and enter the new value. This is a Q15 parameter; therefore, the max value is 0x7FFF.
4. Verify the motor speed (both pu and RPM) calculated by SPEED_PR.
5. Bring the system to a safe stop as described in Figure 17 by setting EnableFlag to '0', taking the controller out of real-time mode and reset.

Expressions

Expression	Value	Type	Address
(x)= EnableFlag	0	unsigned int	0x00008B51@Data
(x)= IsrTicker	0	unsigned long	0x00008B62@Data
(x)= SpeedRef	0.3000000119 (Q-Value(24))	long	0x00008B64@Data
(x)= dlog.prescalar	1	int	0x00008C1D@Data
(x)= SpeedLoopFlag	0	unsigned int	0x00008B4F@Data
(x)= ILoopFlag	0	unsigned int	0x00008B4E@Data
(x)= CmtnPeriodTarget	848	unsigned long	0x00008B74@Data
(x)= DFuncDesired	0.0999756 (Q-Value(15))	int	0x00008B4C@Data
(x)= ClosedFlag	0	unsigned int	0x00008B49@Data
(x)= speed1.Speed	0.0 (Q-Value(24))	long	0x00008BF4@Data
(x)= speed1.SpeedRpm	0	long	0x00008BF8@Data
(x)= CurrentSet	0.09999996424 (Q-Value(2...	long	0x00008B6A@Data
(x)= pid1_idc.term.Fbk	0.0 (Q-Value(24))	long	0x00008C82@Data
(x)= DCbus_current	0.0 (Q-Value(24))	long	0x00008B76@Data
(x)= DfuncTesting	0.119995 (Q-Value(15))	int	0x00008B4D@Data
(x)= IDC_offset	0.5 (Q-Value(15))	long	0x00008B5E@Data
Add new expression			

Figure 17. CCS Expression Window Used With Level 4 Build

8 Test Results

Figure 18 and Figure 19 show the top and bottom view of the assembled board. Note from the bottom view that copper wire is soldered into the mask opening to carry the high current. The board is assembled with the input DC connection leads and screw terminals for three-phase motor connections. To enable the PCB to carry currents of up to 40 A, follow these PCB fabrication and assembly processes:

- The power stage is made of a four-layer PCB with 2-oz copper thickness in all layers. There is wide power and ground return tracks provided in all layers (Refer the PCB fabrication images in Section 9.3).
- The power tracks on the bottom side of the PCB have external copper filling to enable high current carrying capacity.

Figure 20 shows the heat sink mounting on the PCB. The heat sink is mounted on the top side of the MOSFETs. The thermally conductive pad is used between the PCB and the heat sink flat surface to provide electrical insulation. Select a thermal pad with high thermal conductivity. The selected heat sink has a thermal resistance of 1.74°C/W thermal resistivity at airflow of 2 m/s.

The test results are divided in three sections that cover the functional test results, load test results, and stall current test results.

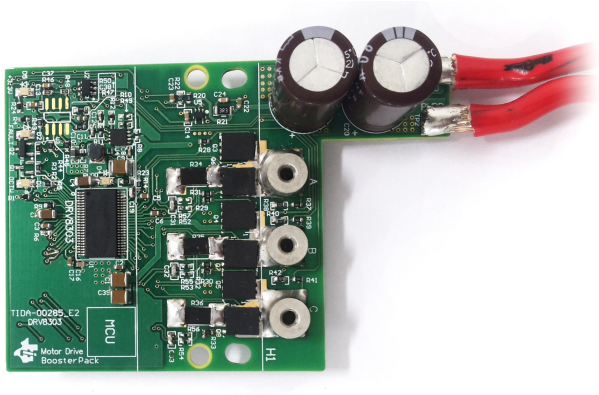


Figure 18. Assembled Power Stage — Top View

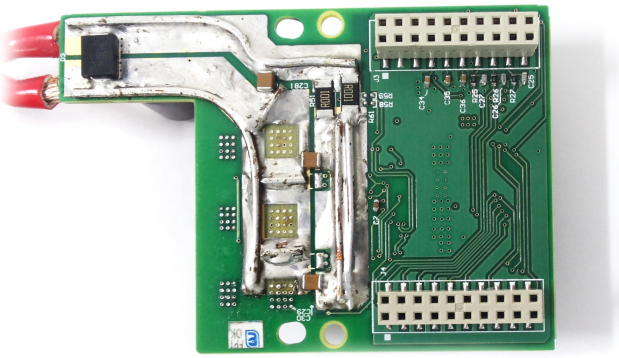


Figure 19. Assembled Power Stage — Bottom View

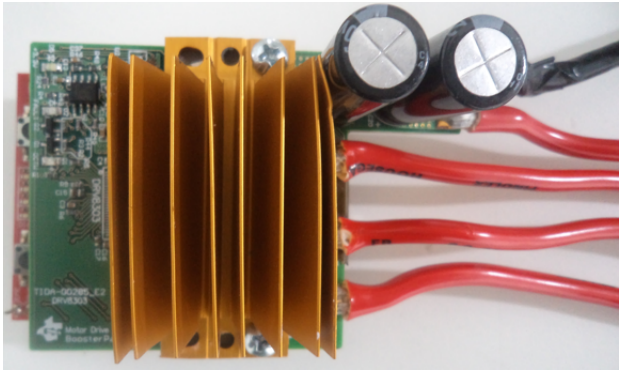


Figure 20. Assembled Power Stage With Heat Sink Mounting

8.1 Functional Tests

Figure 21 shows the 3.3 V generated from the TPS54061 step-down converter. The ripple in the 3.3-V rail is shown in Figure 22.

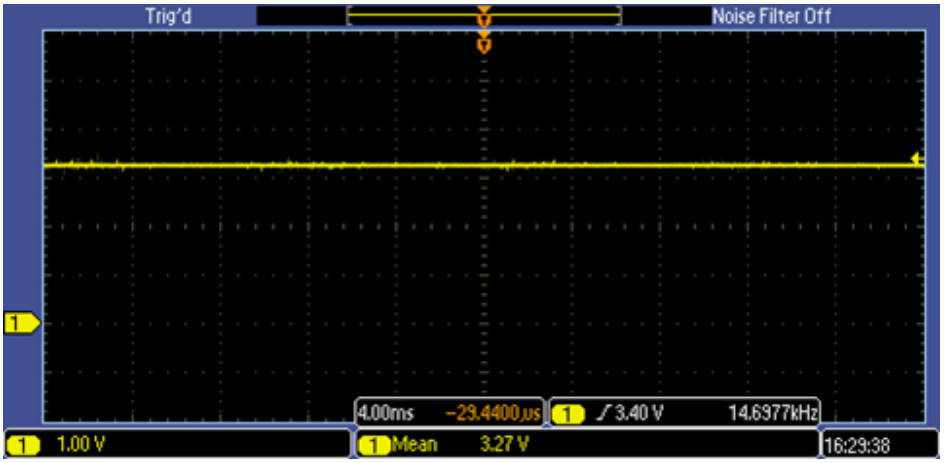


Figure 21. Output Voltage of 3.3 V from Step-Down Converter

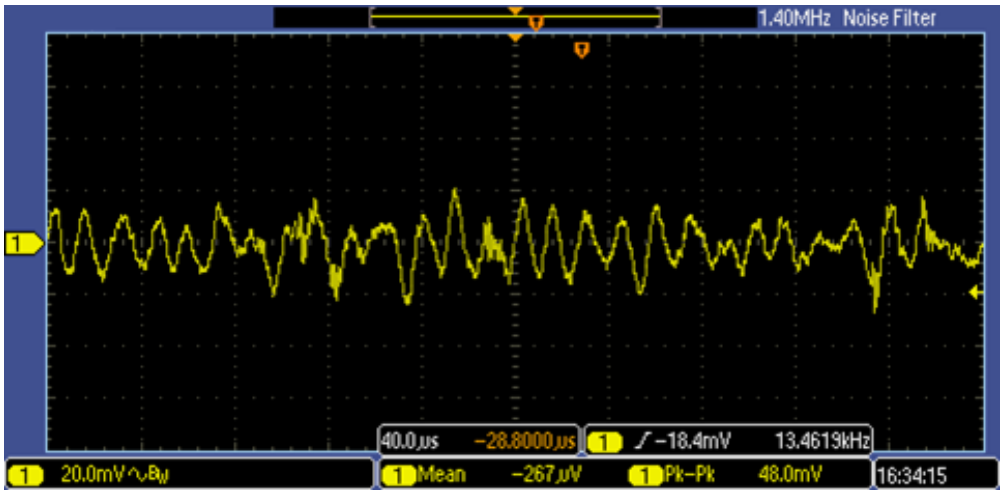


Figure 22. Ripple in 3.3-V Output from Step-Down Converter

The internal voltage regulator of the DRV8303 produces different regulated voltages. The DRV8303 generates GVDD, AVDD, and DVDD for the operation of the internal circuits of the DRV8303. Figure 23 shows the GVDD voltage of the DRV8303 and the voltage ripple in GVDD is shown in Figure 24. The mean voltage at the GVDD is observed to be 10.8 V, well above the undervoltage rating (7.5 V). The GVDD ripple is like a saw tooth wave. This ripple waveform is expected as GVDD supplies the bootstrap capacitor for high side and also gate charge for bottom side.

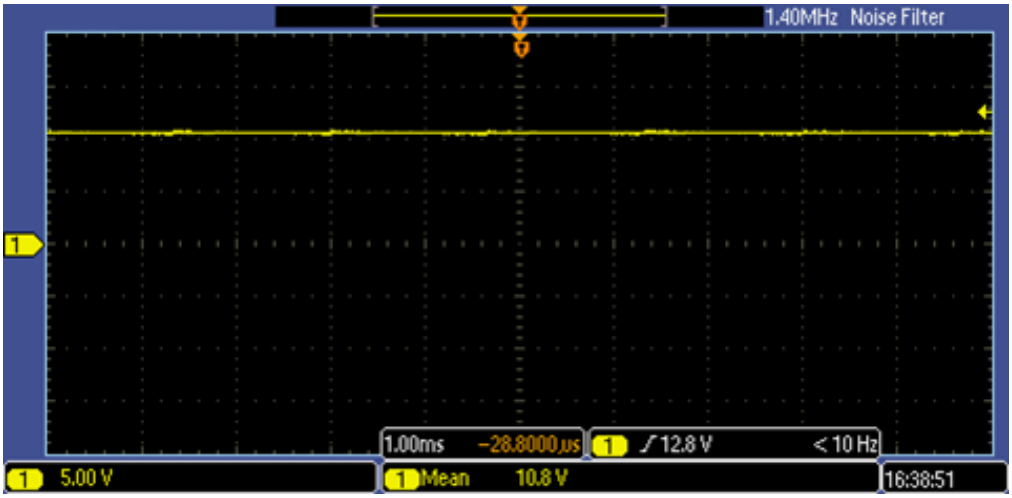


Figure 23. Voltage at GVDD Pin of DRV8303

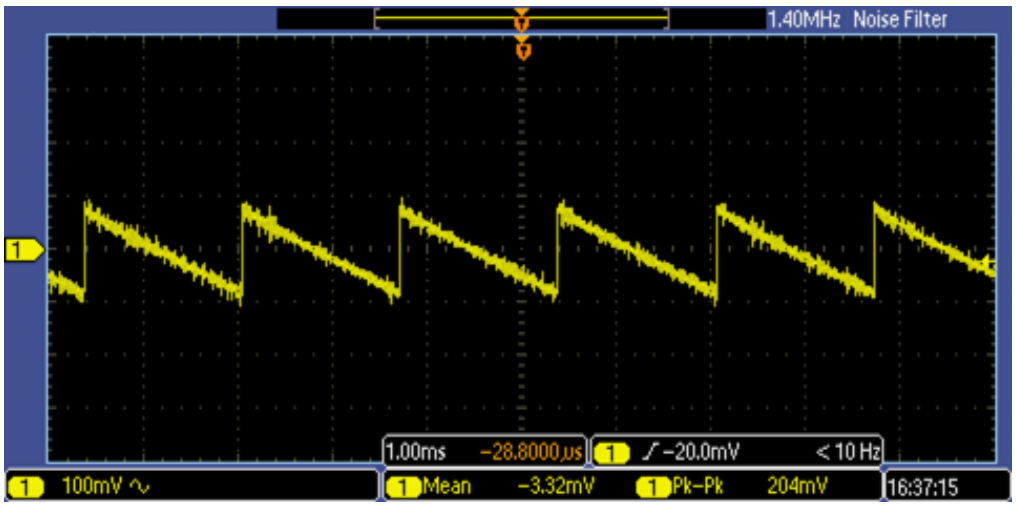


Figure 24. Ripple at GVDD Pin Voltage of DRV8303

Figure 25 shows the voltage output at the DVDD pin of the DRV8303, and the ripple in DVDD rail is shown in Figure 26.

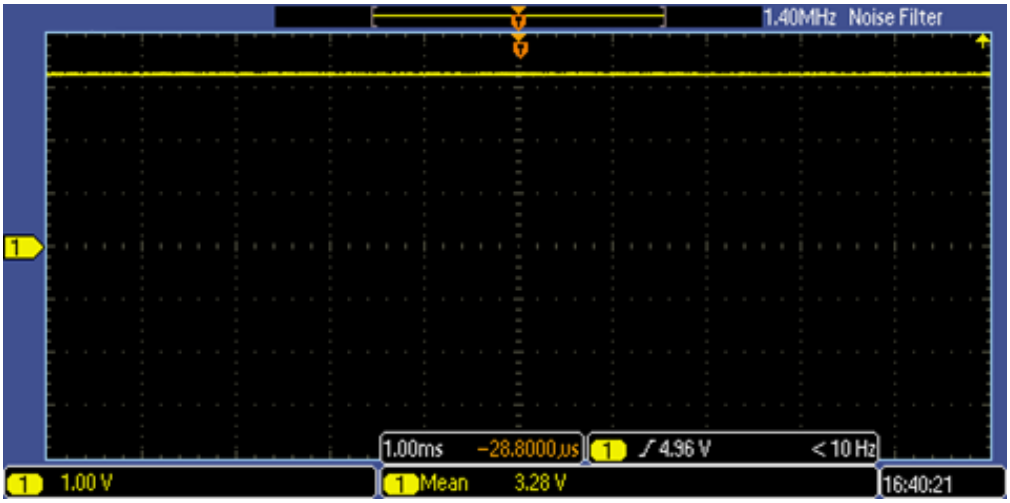


Figure 25. Voltage at DVDD Pin of DRV8303

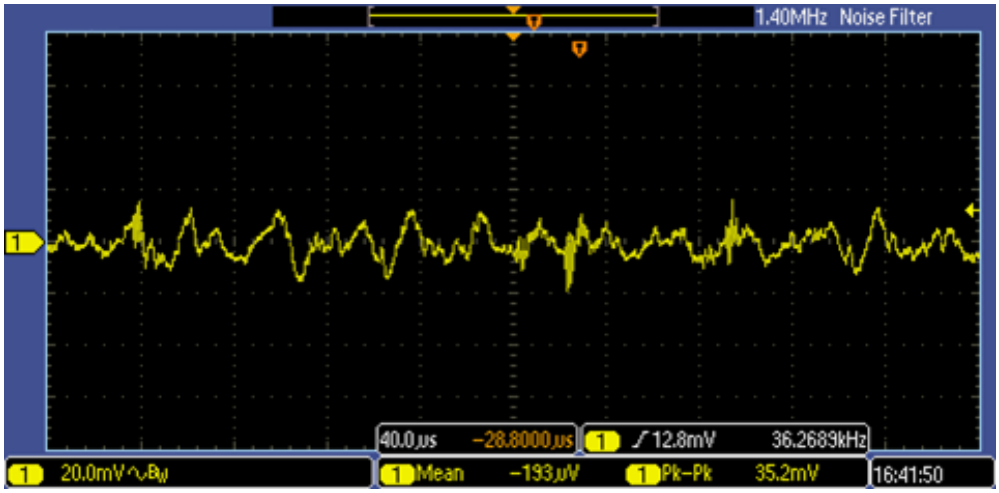


Figure 26. Ripple at DVDD Pin Voltage of DRV8303

Figure 27 shows the voltage output at the AVDD pin of DRV8303, and Figure 28 shows the ripple in AVDD voltage rail. The mean voltage available at the AVDD pin is 6.64 V.

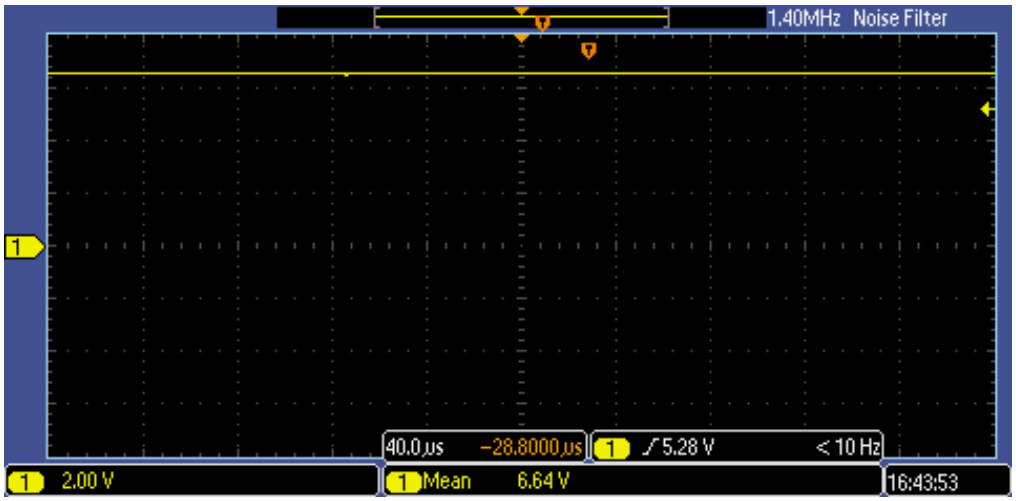


Figure 27. Voltage at AVDD Pin of DRV8303

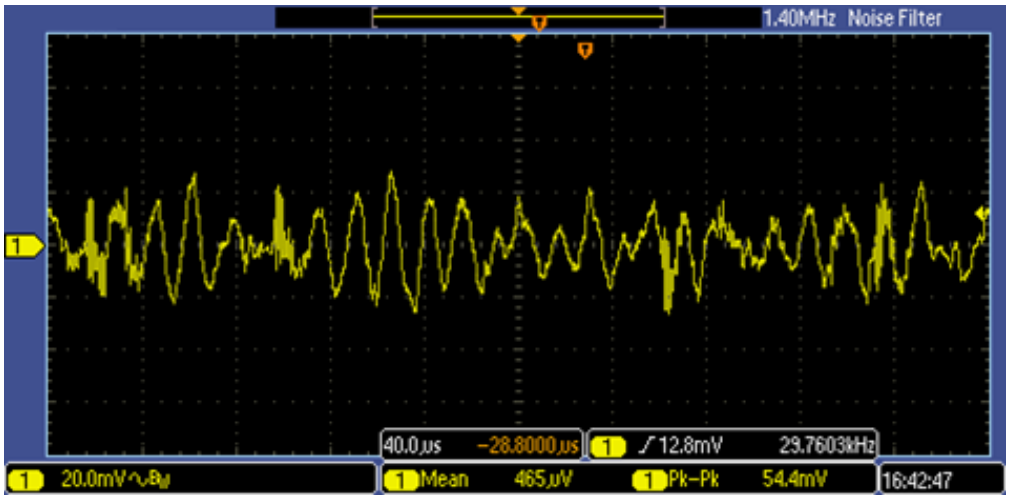


Figure 28. Ripple at AVDD Pin Voltage of DRV8303

The PWM signals generated from the C2000 controller LaunchPad are fed to the DRV8303 gate driver. A switching frequency of 20 kHz is used in the power stage inverter. Figure 29 shows the gate-source voltage for one of the lower MOSFET from the output of the DRV8303 and the corresponding input of DRV8303 coming from the C2000 LaunchPad.

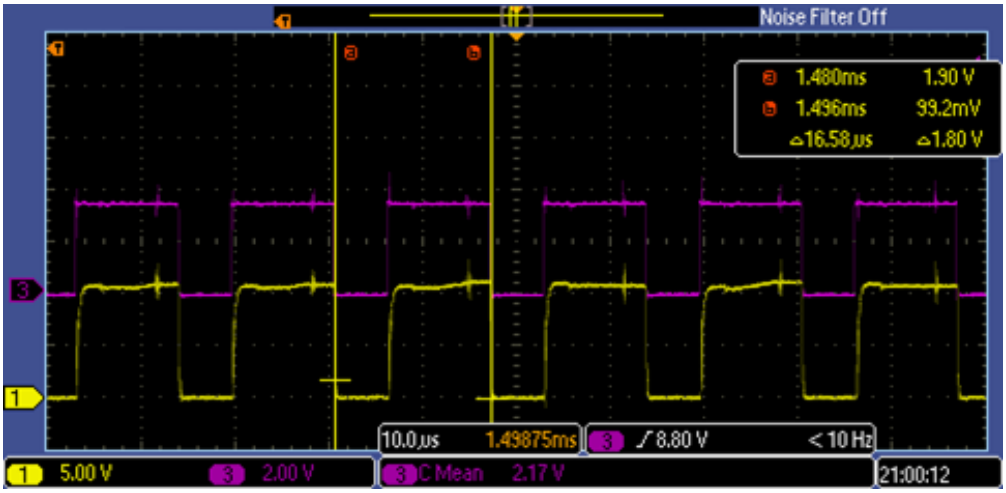


Figure 29. Low-Side PWM Input and Output of DRV8303

Figure 30 shows the complimentary PWM gate signal from the DRV8303 for one leg of the inverter (Both the top side bottom side waveforms are measured with same ground reference). Figure 31 and Figure 32 show the dead time inserted by the DRV8303 at the falling edge and rising edge of the PWMs.

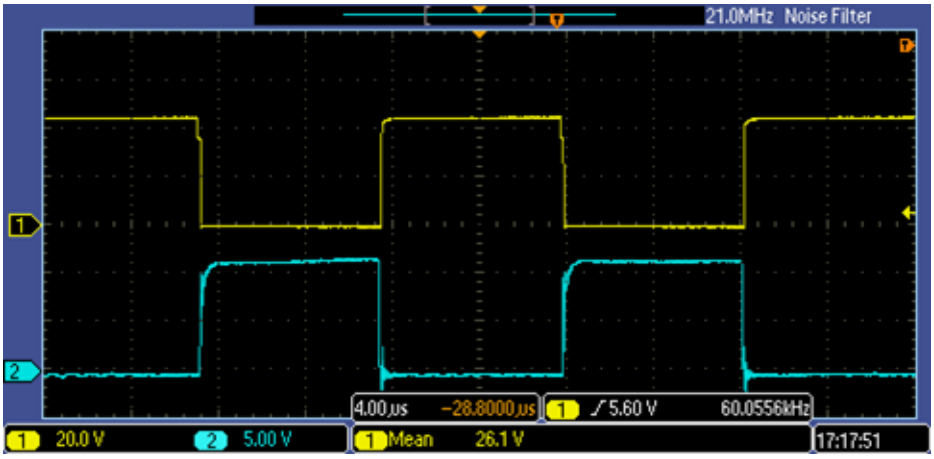


Figure 30. Complimentary PWM Gate Signal From DRV8303

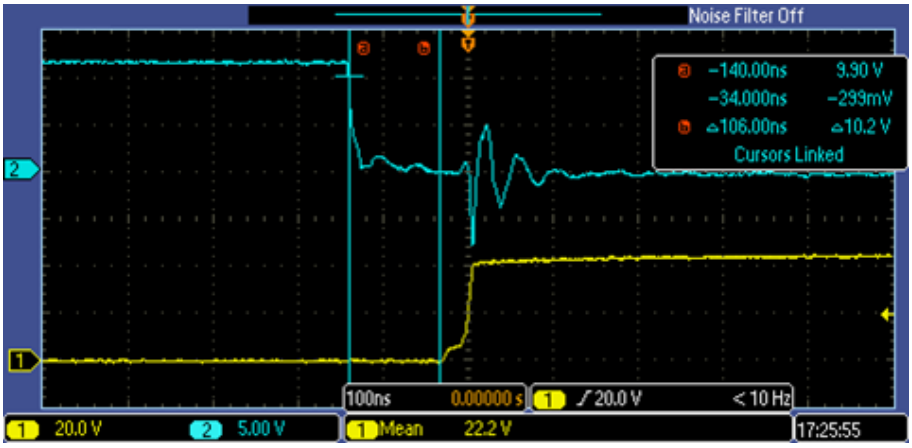


Figure 31. Dead Time Inserted by DRV8303 Measured at Falling Edge of Lower FET PWM

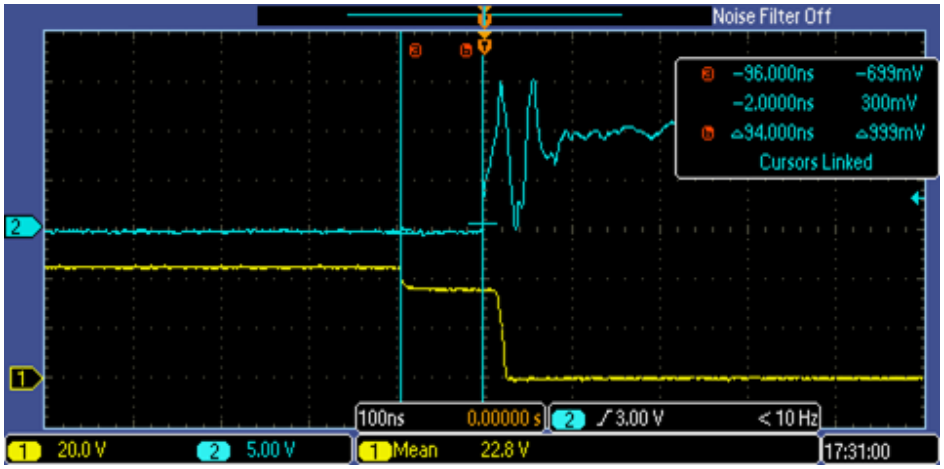


Figure 32. Dead Time Inserted by DRV8303 Measured at Rising Edge of Lower FET PWM

Figure 33 shows the phase-to-phase voltage at motor winding terminals, which is the switching voltage as per the trapezoidal control from the C2000 LaunchPad. Figure 33 shows the phase-to-DC-Link minus voltage.

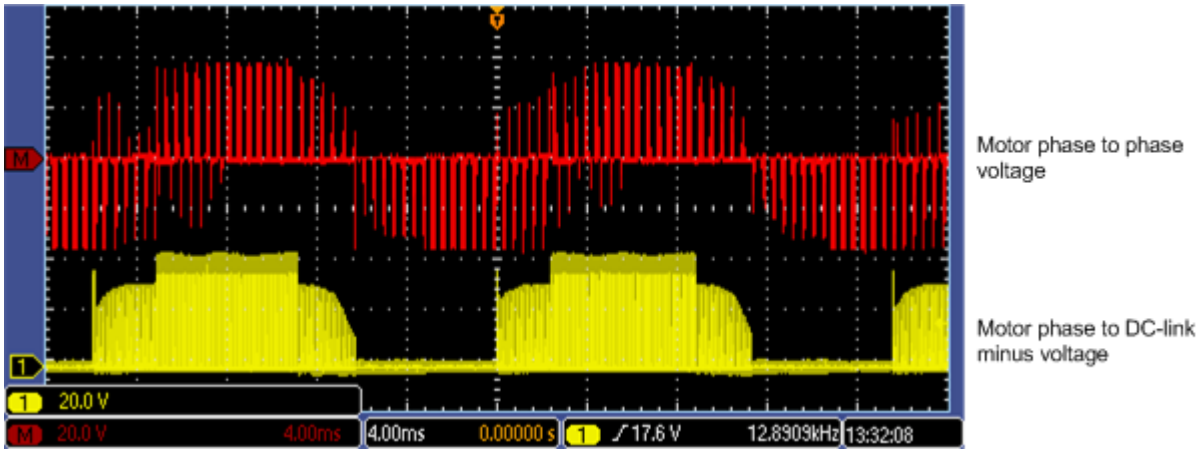


Figure 33. Phase-to-Phase Voltage at Motor Winding Terminals

8.2 Load Tests

The thermal performance of the power stage has been tested and test results have been given in TIDA-00285. TIDA-00285 uses the same board and gives board temperature versus sinusoidal motor winding RMS currents. The board temperature is same for the equivalent DC current with trapezoidal control.

The load test is used to determine the performance of the cycle-by-cycle control features of the DRV8303 while the motor is loaded. The DRV8303 is setup with a V_{DS} threshold to trigger the cycle-by-cycle feature, when the motor is overloaded. Behavior of the system is noted during this condition. Figure 34 shows the block diagram of the test setup used for load testing.

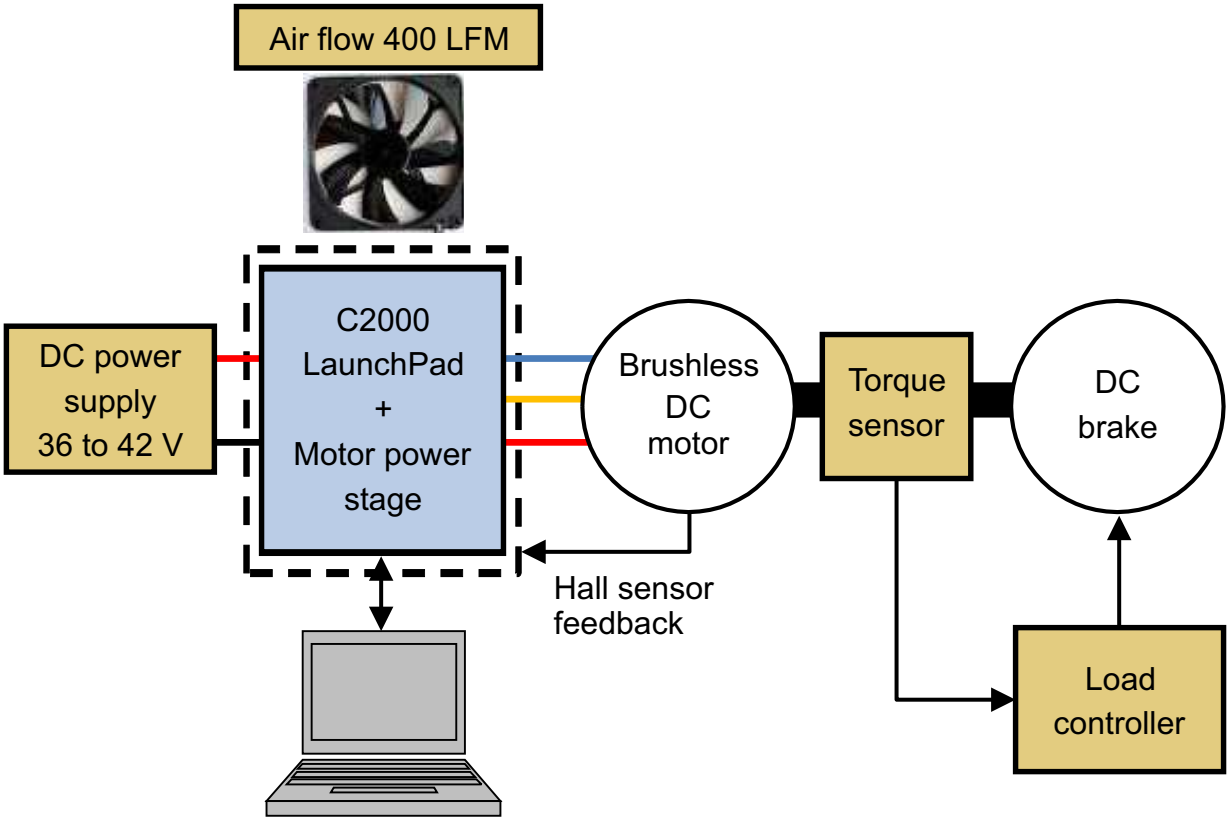


Figure 34. Block Diagram of Load Test Setup

The motor shaft is connected to a DC brake. A 3000-RPM/3-Nm motor is used for testing. The loading on the brushless motor is done by means of the DC brake controlled by the load controller. The torque sensor provides the shaft torque feedback to the load controller so that the shaft torque can be adjusted by the torque controller. The load setup measures torque and speed of the motor. The load testing was done by running the motor using the hall sensor for commutation. The firmware on the C2000 LaunchPad is running firmware described in Section 7. The speed can be commanded while CCS is connected to the C2000 LaunchPad. A constant torque is applied on the motor shaft using the load controller. The waveforms taken are the $\overline{\text{OCTW}}$ signal from the DRV8303, motor winding current in a single phase, corresponding motor windings high side gate input to the DRV8303 and output PWM from the DRV8303.

Figure 35 shows the enclosure setup to provide airflow to the power stage. The cooling fan is selected to provide a 400-LFM airflow to the board. The airflow is measured using an anemometer.

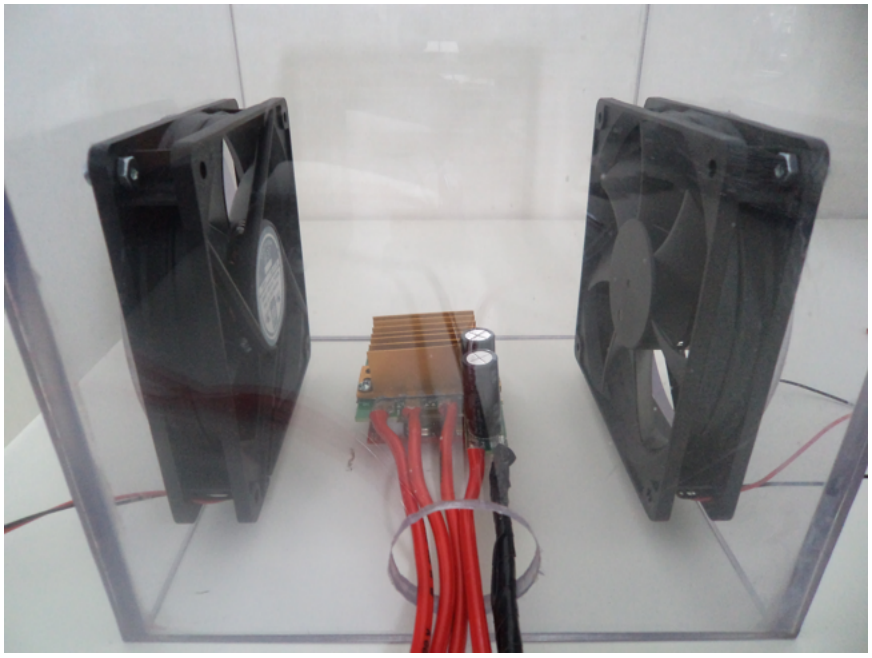


Figure 35. Test Setup to Provide Airflow to Power Stage

Figure 36 shows the motor winding current when the motor is loaded up to 3 Nm at 1200 RPM; the peak current can reach 40 A. The V_{DS} sensing threshold is set to a value such that the cycle-by-cycle current limiting triggers below 40 A to observe the CBC.

The V_{DS} threshold is set to 86 mV; however, the V_{DS} setting can have a 20% variations. The R_{DS_ON} of the MOSFET is taken as 2.6 mΩ, considering the R_{DS_ON} has risen due to heating of the board and the temperature rise by 60°C. The corresponding current is calculated as

$$I_{th} = \frac{V_{DS}}{R_{DS\_ON}} = \frac{0.8 \times 86\ mV}{2.6\ mV} = 26.5\ A \quad (18)$$

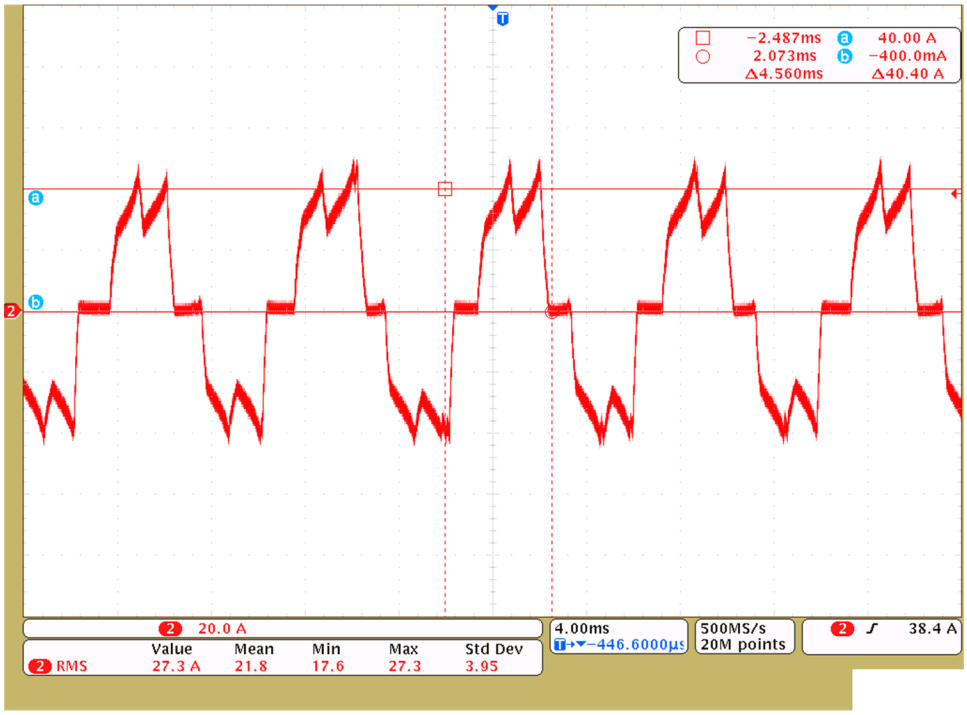


Figure 36. Motor Winding Current Loaded on Test Setup

Figure 37 shows the waveform while loaded just before the motor cycle-by-cycle is triggered. Figure 38 shows the first instant the cycle-by-cycle is triggered when motor is lightly overloaded, which happens at the peak of the current waveforms.

The instance of cycle-by-cycle is when the $\overline{\text{OCTW}}$ signal is pulled low. Notice at the instance cycle-by-cycle has triggered, the output PWM turns off. The current at this point is 23.6 A.

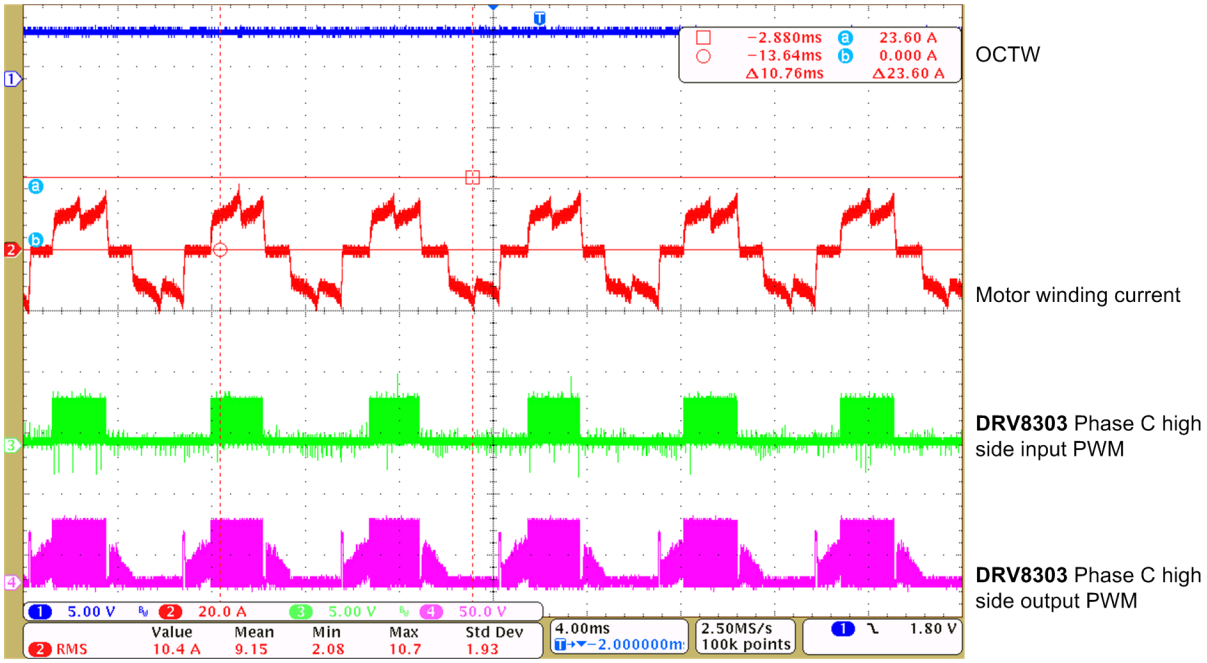


Figure 37. Motor Current Before Cycle-by-Cycle

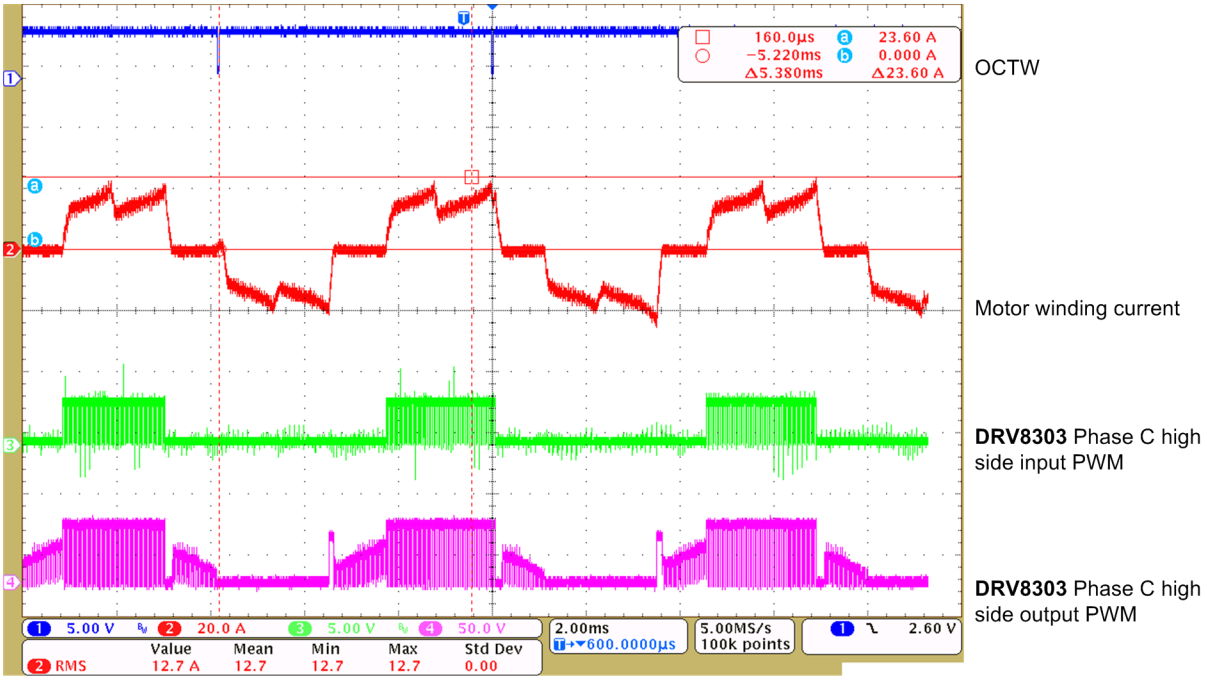


Figure 38. Cycle-by-Cycle Current Limiting When Motor Lightly Overloaded

Figure 39 shows the zoomed in view, shows the input PWM, and the output PWM is turns of when $\overline{\text{OCTW}}$ is pulled low this is the point at which cycle-by-cycle has acted.

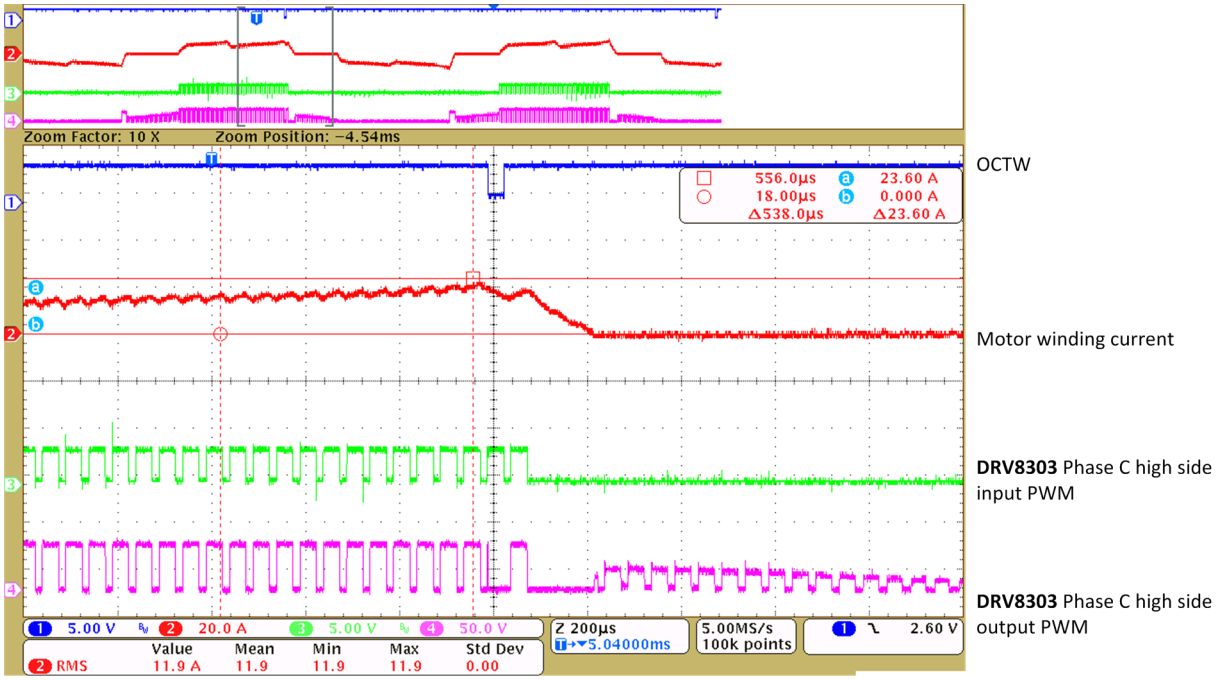


Figure 39. Cycle-by-Cycle Current Limiting When Motor is Lightly Overloaded (Zoomed View)

Figure 40 shows the motor is further overloaded; the cycle-by-cycle is triggered more in each commutation period.

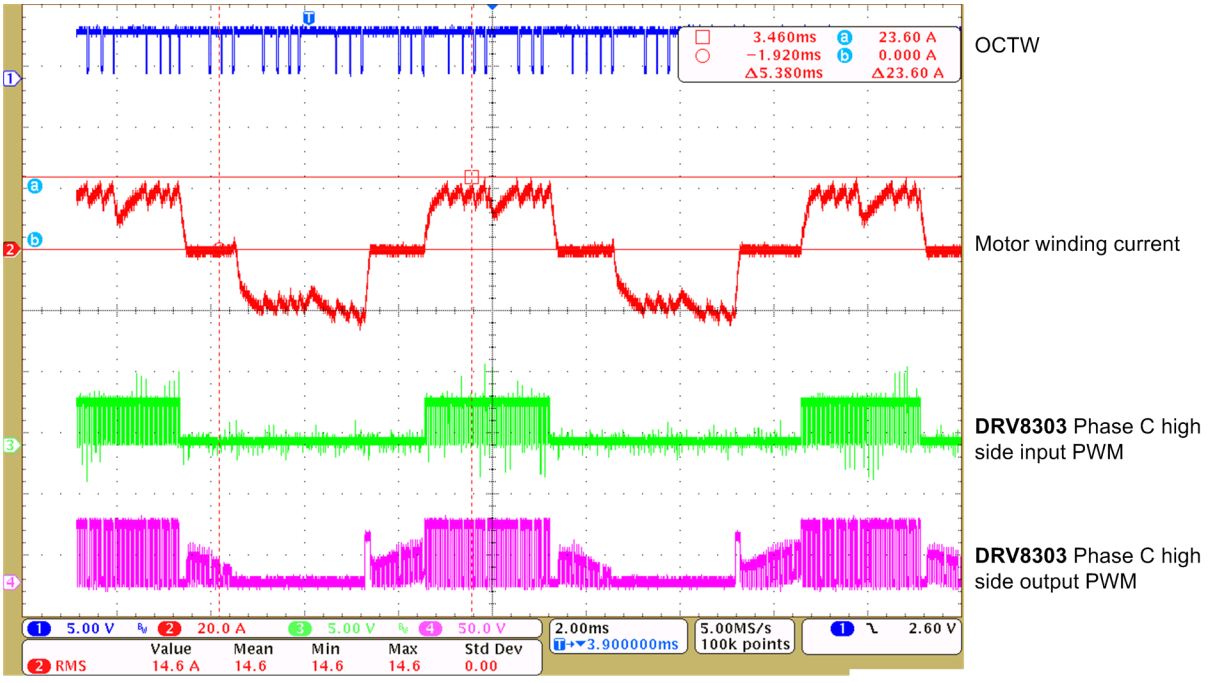


Figure 40. Cycle-by-Cycle Current Limiting When Motor is Medium Overloaded

Figure 41 shows the motor heavily overloaded and the cycle-by-cycle is triggered almost every PWM cycle.

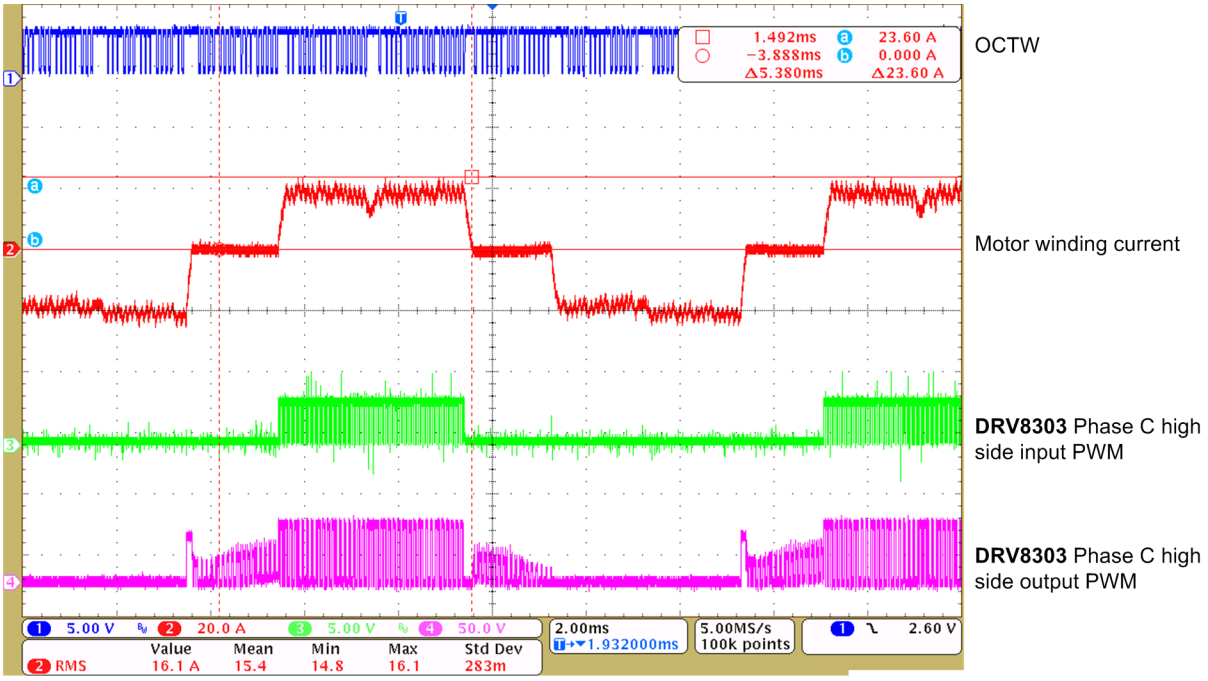


Figure 41. Cycle-by-Cycle Current Limiting When Motor is Heavily Overloaded

Figure 42 shows a zoomed view where the input PWM, and the output PWM is shown. The output PWM is shown to turn-off when cycle-by-cycle is triggered.

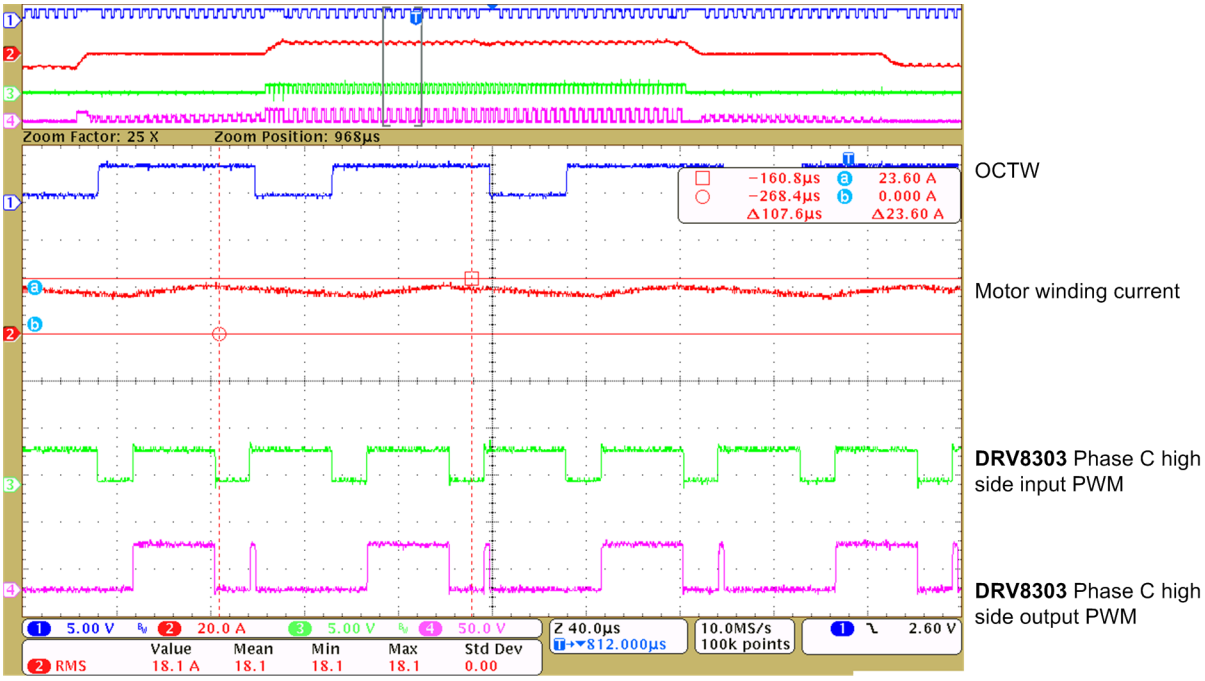


Figure 42. Cycle-by-Cycle Current Limiting When Motor is Heavily Overloaded (Zoomed View)

In all of the above cases of the motor winding current, the MOSFET current is never allowed to go beyond the set point. However, the motor continues to rotate providing the torque with a reduced speed. In a stall condition where the motor stops, even though the cycle-by-cycle is triggered then motor continues to get energized. This provides motor with a limited amount of torque. It is required to provide some torque, in case the stall condition can be removed and the motor can regain rotation. This is required in case of a power tool application where the stall may be temporary and the tool can regain rotation.

8.3 Stall Current Protection Test

Figure 43 shows the test setup to simulate a stall currents. S1 is a single-throw, double-pole switch connect between the motor terminals. This is used to create a motor winding to a winding short. Shorting the motor terminals would cause a high current to be generated in the power stage. The high current is seen in the top side MOSFET of a single leg and the bottom side MOSFET of another leg. This situation would be similar to a stall condition where high current is would exist in the motor limited only by the motor resistance.

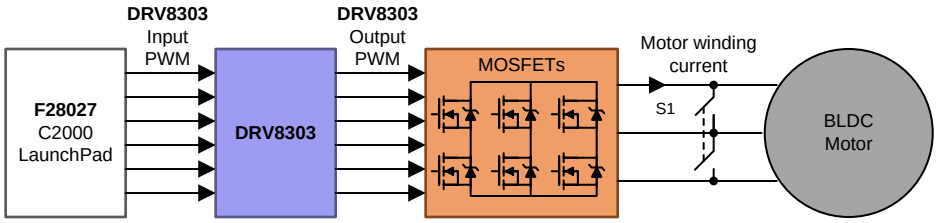


Figure 43. Test Setup to Simulate Stall Currents

Before S1 is closed, the motor was rotating at a steady speed with no load. Figure 44 shows the waveforms obtained when the S1 is closed. When S1 is closed, S1 carries the short circuit current; the maximum value of the short circuit current is 30.4 A. During this condition the motor stops, which causes the Hall state to be stuck at the current commutation state; therefore, the controller continues to generate the PWM corresponding to this commutation state.

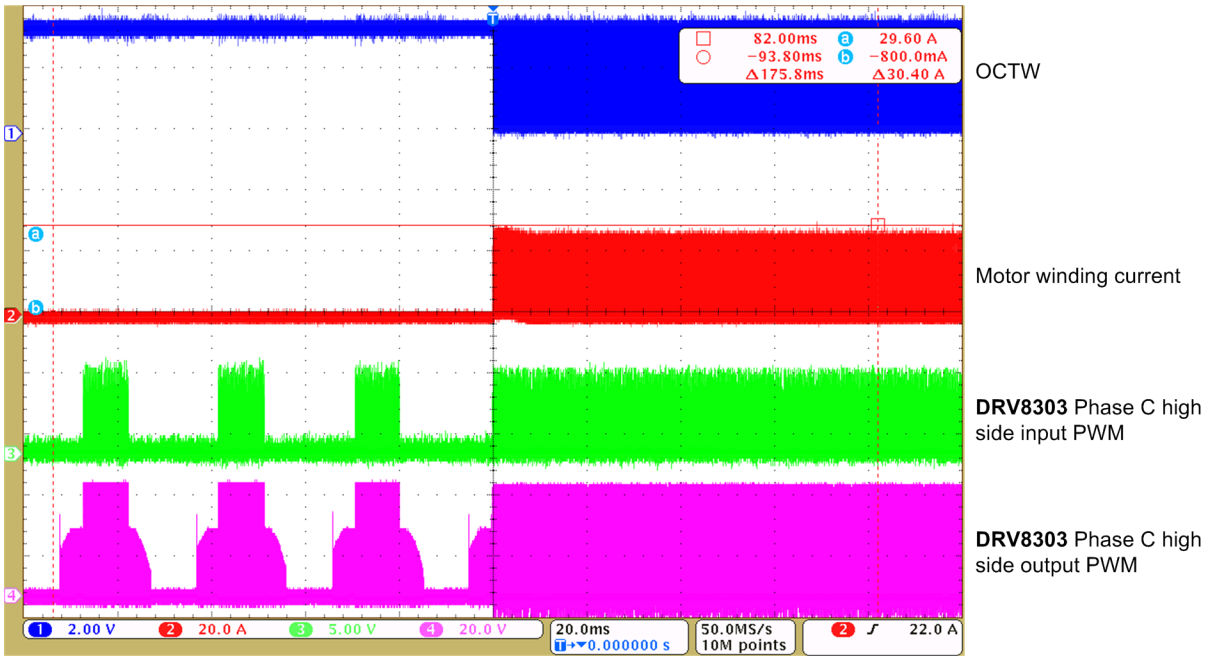


Figure 44. Motor Terminals Short Circuit Waveforms

Figure 45 shows a zoomed-in view of this state.

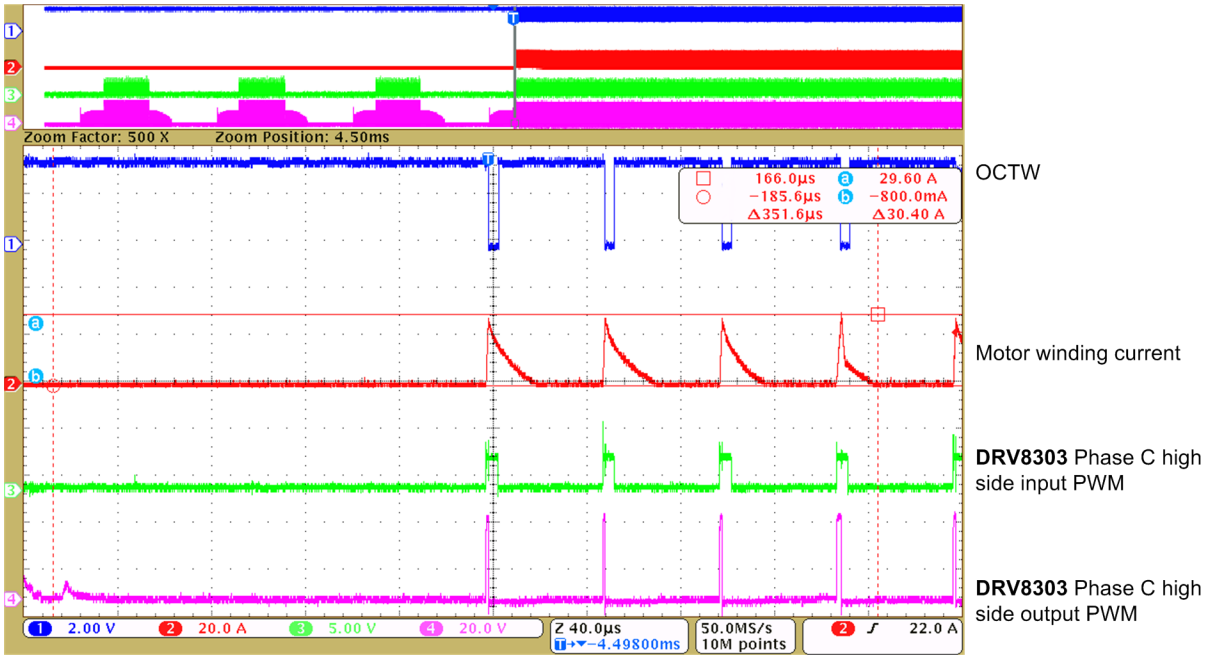


Figure 45. Motor Terminals Short Circuit Waveforms (Zoomed View)

S1 is applied for a short duration of about one second. When short due to S1 being removed, the motor starts to rotate again.

Figure 46 shows the waveform zoomed into one PWM cycle. The output PWM has stayed on for a period of 2 µs during the stall condition. This time includes the time for the current to ramp up V_{DS} sensing and time for cycle-by-cycle to trigger. The exact time for taken for cycle-by-cycle to respond to from the time the current crossed the threshold cannot be determined. However, the cycle-by-cycle inferred to acts within less than 2 µs, with actual response time in order of 100 ns. This quick response is due to the V_{DS} sensing implemented in the hardware of the DV8303, which is always active during the on period of the MOSFET. This is an advantage of having the V_{DS} sensing in hardware over software technique for protection, where the controller response can be delayed by a couple of PWM cycles.

Figure 46. Cycle-by-Cycle Response Time

9 Design Files

9.1 Schematics

To download the schematics, see the design files at TIDA-00436.

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00436.

9.3 PCB Layout Recommendations

Consider the following points during the PCB layout design and assembly:

1. The DRV8303 makes an electrical connection to GND through the PowerPAD. Always check to ensure that the PowerPAD has been properly soldered. See the PowerPAD application report (SLMA002).
2. C1/C2/C39: Place PVDD decoupling capacitors close to their corresponding pins with a low impedance path to device GND (PowerPAD).
3. C4/C15: Place GVDD capacitor close its corresponding pin with a low-impedance path-to-device GND (PowerPAD).
4. C16/C17: Place AVDD and DVDD capacitors close to their corresponding pins with a low-impedance path to the AGND pin. If possible, make this connection on the same layer.
5. Tie AGND to GND (PowerPAD) through a low-impedance trace/copper fill.
6. Add stitching vias to reduce the impedance of the GND path from the top to bottom side.

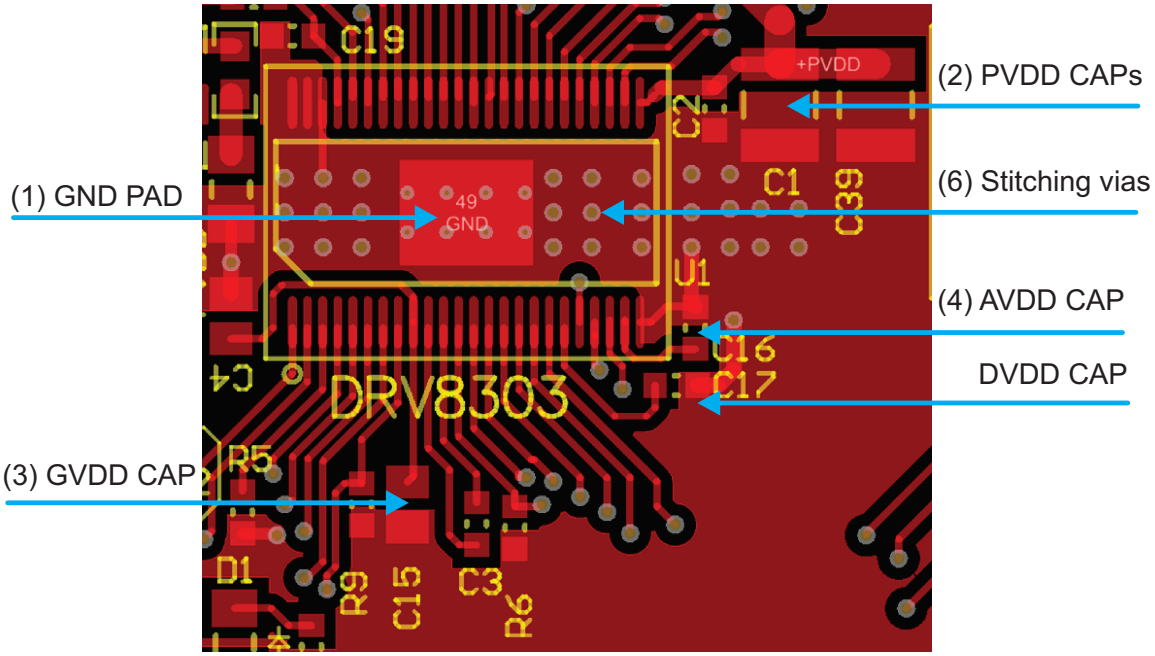


Figure 47. Layout Consideration for DRV8303

7. Clear the space around and underneath the DRV8303 to allow for better heat spreading from the PowerPAD.

8. Route the track for sensing the V_{DS} of the MOSFET as a differential track as shown in Figure 48.

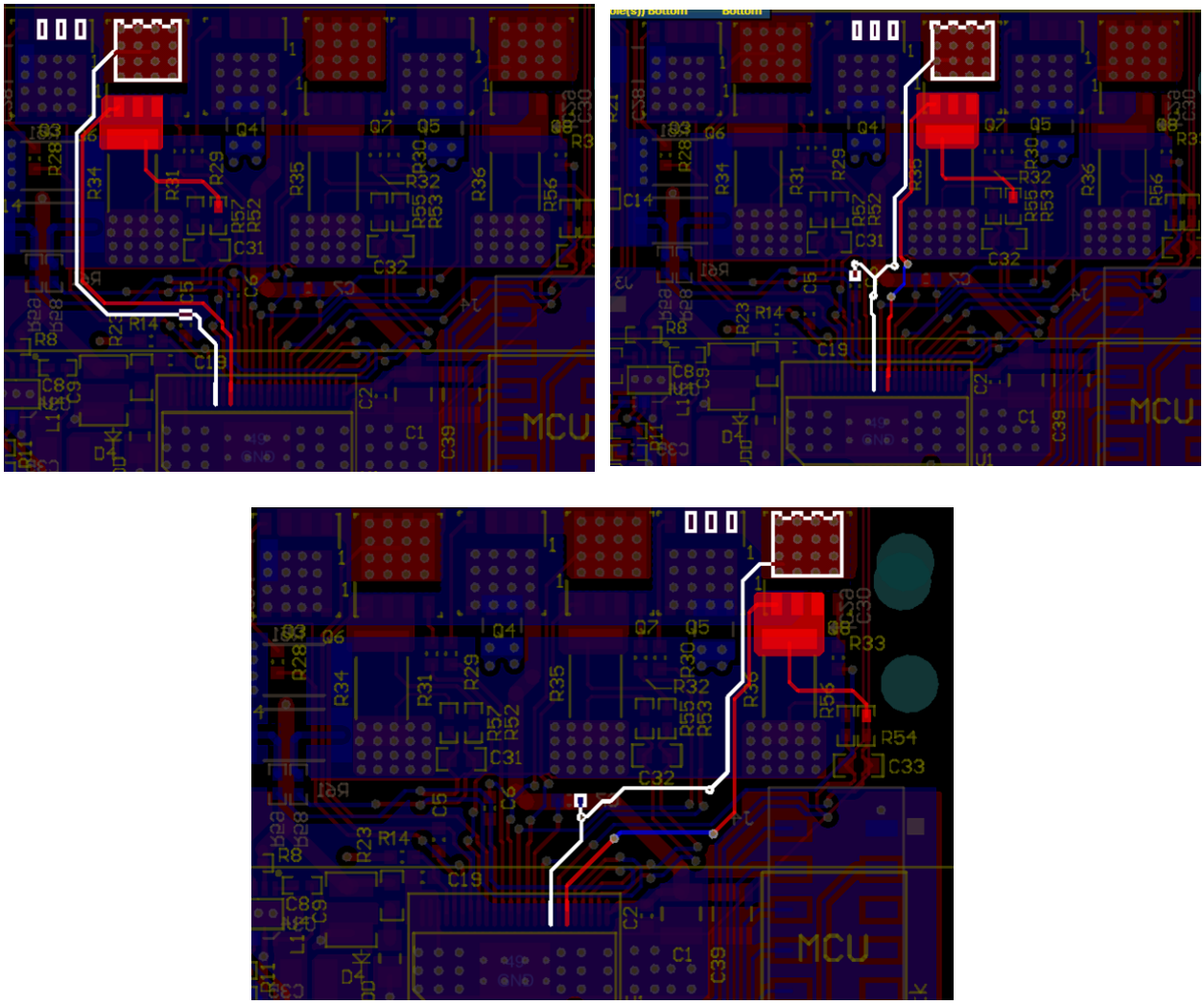


Figure 48. Differential Line for V_{DS} Sensing of MOSFETs

9. In the reference design, the PCB is made in four layer with 2-oz (70 micron) copper thickness in every layer. The power tracks are made wide to carry a high current. Figure 49 shows the current carrying track from the power input point. The tracks in different layers are connected by arrays of stitching vias.

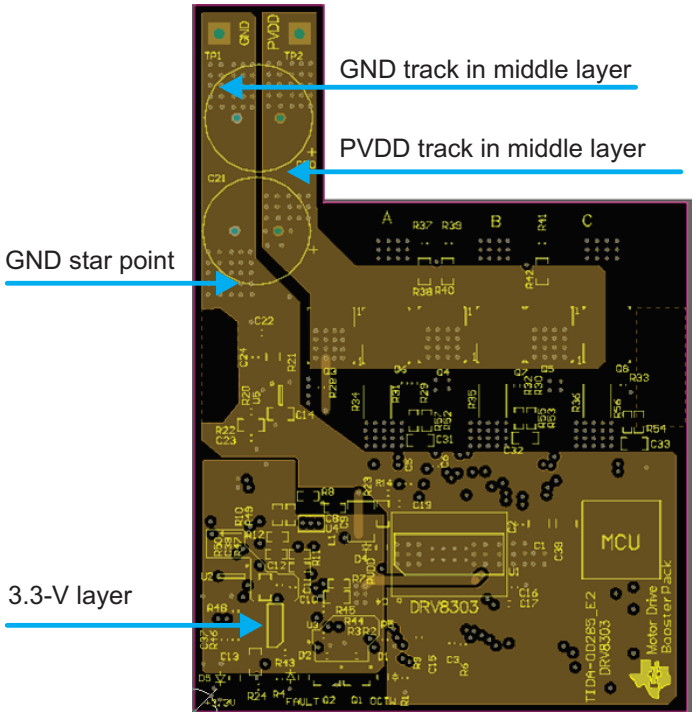


Figure 49. Layout Considerations for Power Handling and GND Tracks

10. A GND star point is defined in the PCB from where the GND path for the DRV8303 and other signal circuits in the board is tapped.
11. For better thermal dissipation from the MOSFET to the PCB, increase the copper area around the MOSFET pad as much as possible. Use arrays of vias under the drain pad of the MOSFET, which will help in better heat dissipation through the bottom surface copper area. Add a small heat sink or copper bars to the bottom surface of PCB to aid heat dissipation.

12. The placement of the decoupling capacitors is important for the proper functioning of the V_{DS} sensing protection of the DRV8303. Place these capacitors near to each MOSFET leg. The return path of the decoupling capacitors should be through a thick track, and the return path length should be as short as possible to improve the decoupling.

NOTE: The mounting of the decoupling capacitors deviates from what is shown in the schematic and layout. This is done to satisfy the layout guideline 12 to make the shortest return path for the decoupling capacitor current. Figure 50 shows the decoupling capacitor placement used for testing.

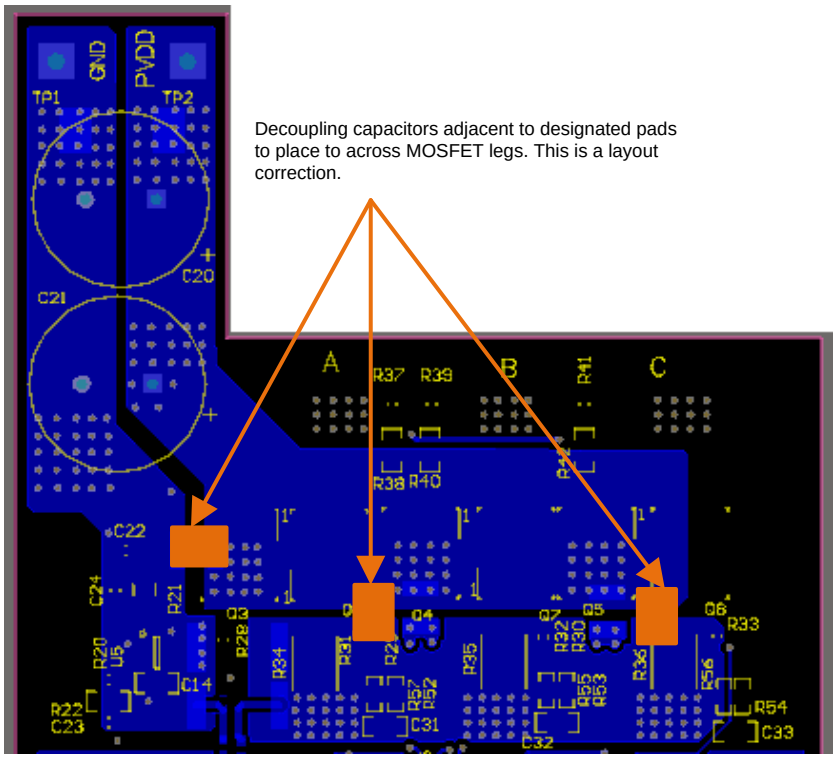


Figure 50. Mounting of Decoupling Capacitors for Inverter Legs

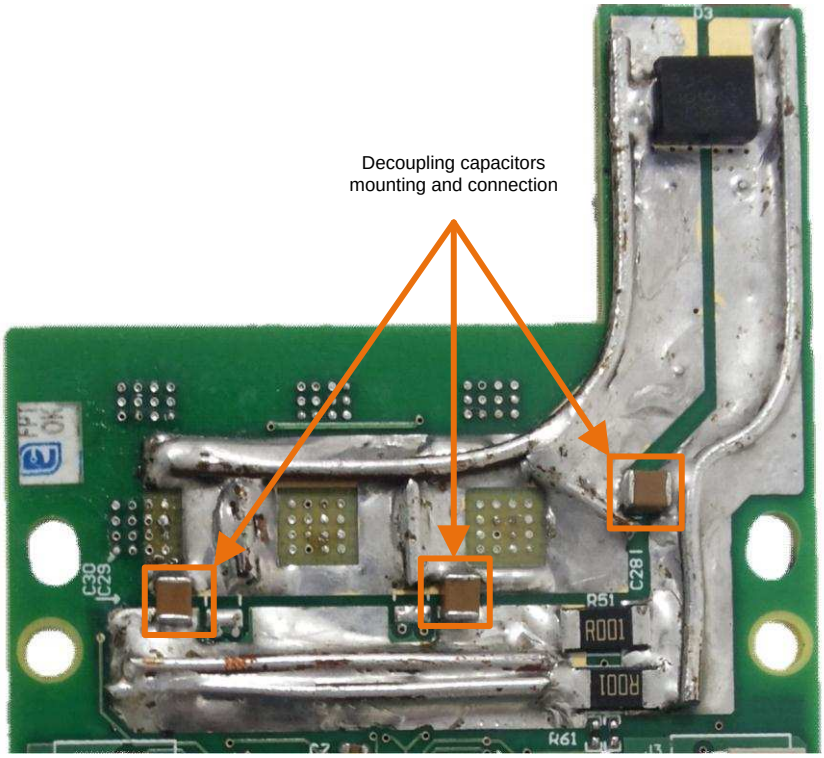


Figure 51. Mounting of Decoupling Capacitors for Inverter Legs

9.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00436.

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00436.

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00436.

9.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00436.

10 References

1. Texas Instruments Datasheet, *Three Phase Pre-Driver with Dual Current Shunt Amplifiers*, DRV8303 (SLOS846)
2. Texas Instruments Application Report, *Trapezoidal Control of BLDC Motors Using Hall Effect Sensor*, (SPRABQ6)
3. Texas Instruments Application Report, *PowerPAD™ Thermally Enhanced Package*, (SLMA002)
4. Texas Instruments Application Report, *Semiconductor and IC Package Thermal Metrics*, (SPRA953)
5. Texas Instruments Application Report, *AN-2026 The Effect of PCB Design on the Thermal Performance of SIMPLE SWITCHER® Power Modules*, (SNVA424)
6. Texas Instruments Application Report, *PCB Layout Guidelines for Power Controllers*, (SLUA366)

11 Terminology

BLDC— Brushless DC motor

ESD— Electrostatic discharge

FETs, MOSFETs—The metal-oxide-semiconductor field-effect transistor

FOC— Field oriented control

LaunchPad— All reference to LaunchPad refers to C2000 LaunchPads

LFM— Linear feet per minute; 1 LFM = 0.005 m/s

MCU— Microcontroller unit

PMSM— Permanent magnet synchronous motor

PWM— Pulse width modulation

RMS— Root mean square

RPM— Rotation per minute

SPI— Serial peripheral interface

TVS— Transient voltage suppressors

12 About the Author

NELSON ALEXANDER is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Nelson has been with TI since 2011 and has been involved in designing products related to smart grid and embedded systems based on microcontrollers. Nelson earned his bachelor of technology in electrical engineering at MSRIT, Bangalore.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2015) to B Revision	Page
• Changed title from *36-V, 32-A Power Stage for BLDC Motor With Cycle-by-Cycle Stall Current Limiter* to *36-V, 1-kW Brushless DC Motor Drive With Stall Current Limit of < 1-µs Response Time Reference Design*	1

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