Peter Semig, Tim Claycomb

TI Designs – Precision: Verified Design

±1A Single-Supply Low-Side Current Sensing Solution Reference Design

TI Designs – Precision

TI Designs – Precision are analog solutions created by TI's analog experts. Verified Designs offer the theory, component selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

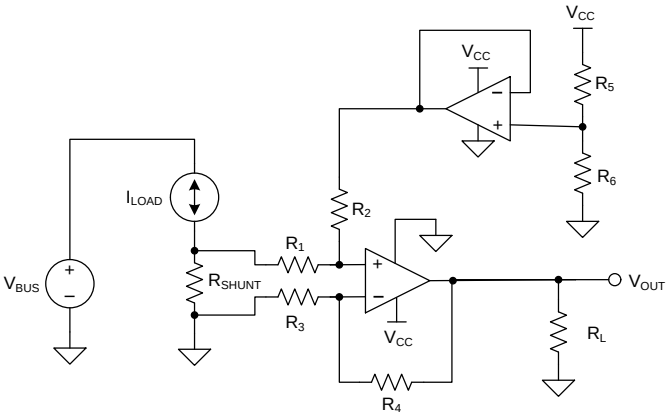
Design Archive	All Design files
TINA-TI™	SPICE Simulator
OPA2313	Product Folder

Circuit Description

This single-supply low-side, bidirectional current sensing solution can accurately detect load currents from -1 A to 1 A. The linear range of the output is from 110 mV to 3.19 V. The design utilizes the OPA2313 configured as a difference amplifier and reference voltage buffer.

TI E2E™ Community

Ask The Analog Experts
WEBENCH® Design Center
TI Designs – Precision Library



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

TINA-TI is a trademark of Texas Instruments
WEBENCH is a registered trademark of Texas Instruments

1 Design Summary

The design requirements are as follows:

- Supply Voltage: 3.3 V
- Input: -1 A to + 1 A
- Output: 110 mV to 3.19 V
- Maximum Shunt Voltage: ±100 mV

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated (typ)	Calculated (typ)	Measured
Total Unadjusted Error (%)	±1.0%	±0.893%	±0.53%	±0.621%

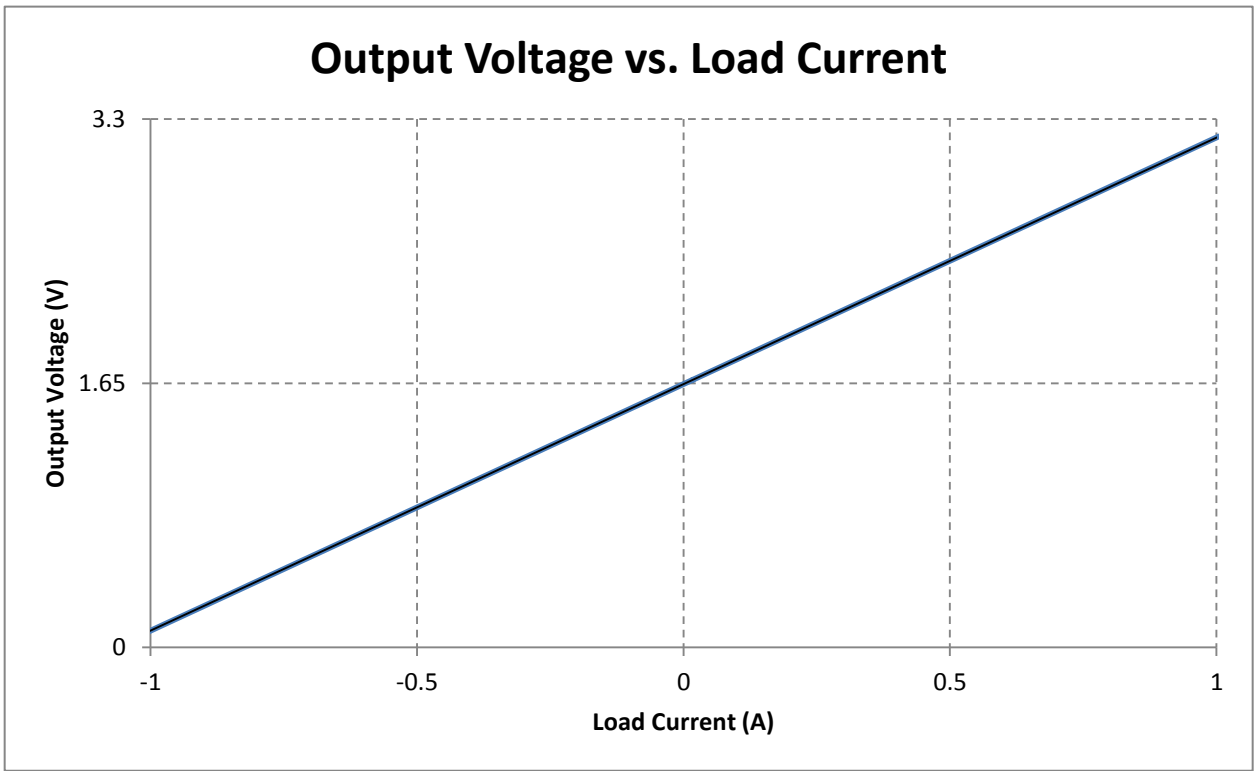


Figure 1: Measured Transfer Function

2 Theory of Operation

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore the current sensing solution is independent of the bus voltage, V_{BUS}. When sensing bidirectional currents, a reference voltage must be added to differentiate between positive and negative currents. Figure 2 depicts a general circuit topology for a low side, bidirectional current sensing solution. This topology is particularly useful when cost is a priority at the expense of accuracy and printed circuit board (PCB) space.

The shunt voltage (V_{SHUNT}) is created by the load current (I_{LOAD}) flowing through the shunt resistor (R_{SHUNT}). V_{SHUNT} is amplified by an op amp (U1A) according to the gain set by the ratio of R_4 to R_3. To achieve the transfer function in Equation (1) and to minimize errors as described in Table 2, set R_4=R_2 and R_3=R_1.

To provide the reference voltage in this design, divide down the supply voltage (V_{CC}) using R_5 and R_6. The reference voltage is then buffered using an op amp (U1B).

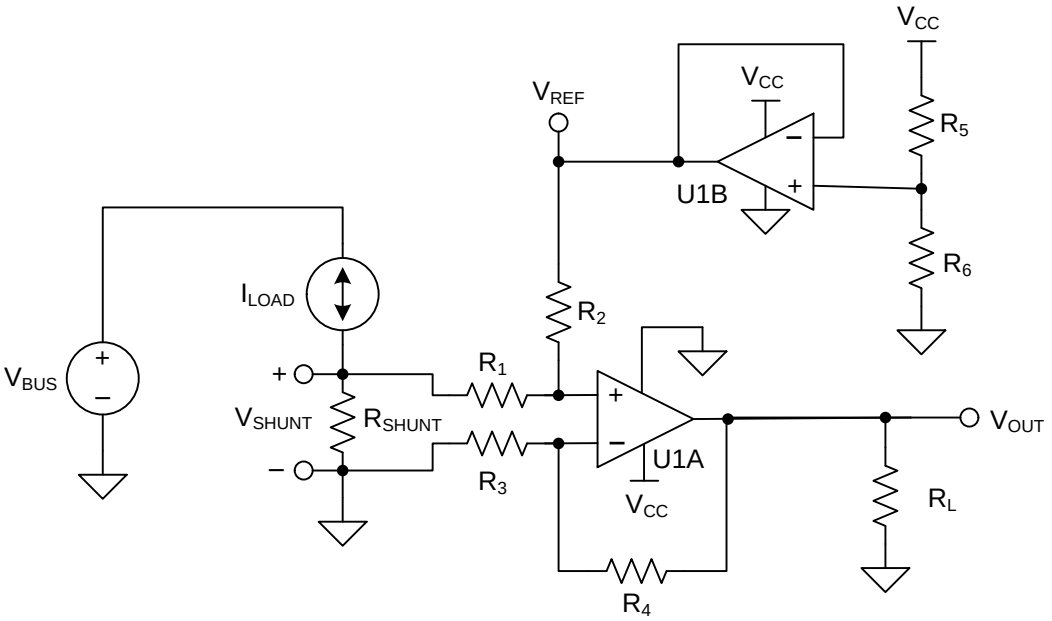


Figure 2: Design Schematic

Equation (1) depicts the ideal transfer function for the schematic shown in Figure 2.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF} \quad (1)$$

Where

$$V_{SHUNT} = I_{LOAD} \times R_{SHUNT} \quad (2)$$

$$Gain_{Diff\_Amp} = \frac{R_4}{R_3} \quad (3)$$

$$V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right) \quad (4)$$

2.1 Error Analysis

There are two types of errors introduced by the circuit in Figure 2: offset and gain. To obtain more information about these types of errors, please refer to TIPD129. Table 2 lists the error sources and their respective type(s).

Table 2. Design Error Sources

Error Source	Description	Error Type
Shunt resistor	Shunt resistor tolerance	Gain
Difference Amplifier	U1A and R_1-R_4 create a difference amplifier. The ratios of R_2/R_1 and R_4/R_3 introduce a gain error. The absolute value of the ratios introduce a gain error and the matching of the ratios determine the CMRR performance, which translates to an offset error.	Offset & Gain
Reference Voltage	The accuracy of the voltage divider created by R_5 and R_6 yields an offset error.	Offset

These errors ultimately combine and are measured at the output as gain and offset errors. It is common to combine them using the root sum squared (RSS) method. This method is used when combining errors with a normal distribution, thereby yielding typical total error. For a worst-case total error, simply add all error terms directly.

3 Component Selection

3.1 Shunt Resistor (R_{SHUNT})

As shown in Figure 2, the value of V_{SHUNT} is the ground potential for the system load. If the value of V_{SHUNT} is too large, it may cause issues when interfacing with systems whose ground potential is truly 0 V. If the value of V_{SHUNT} is too negative, it may violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore it is important to limit the voltage across the shunt resistor. Equation (**5**) calculates the maximum value of R_{SHUNT} given a maximum shunt voltage of 100 mV.

$$R_{SHUNT(MAX)} = \frac{\left|V_{SHUNT(MAX)}\right|}{\left|I_{LOAD(MAX)}\right|} = \frac{100mV}{1A} = 100m\Omega \tag{5}$$

Since cost is a priority in this design, a shunt resistor with 0.5% tolerance was selected.

3.2 Operational Amplifiers

The shunt voltage in this design can range from -100 mV to +100 mV. It is divided down by R_1 and R_2. The op amp configured as a difference amplifier (U1A) must have an input common-mode that includes this voltage range. Therefore an op amp with rail-to-rail input (RRI) that extends below GND is recommended. The output swing of the amplifier should also be rail-to-rail output (RRO) to maximize the dynamic range of the system. A CMOS op amp is suggested because the supply voltage is 3.3 V. The supply-splitter op amp (U1B) should have low offset voltage. Since there are 2 op amps in this design, a dual package minimizes the required area.

This design utilizes the OPA2313 because it is a RRI/O CMOS device. In addition, the cost vs. performance of the device is excellent.

3.3 Reference Voltage Resistors (R5-R6)

Since the load current range is symmetric (-1 A to 1 A), the resistors that divide down the supply voltage should be equal so that the reference voltage is mid supply (1.65 V). Since cost is a priority in this design, the tolerance should be consistent with the shunt resistor tolerance (0.5%). Finally, select resistors that are large enough to meet the system's power consumption requirement. For this design, 10 kΩ resistors were chosen.

3.4 Difference Amplifier Gain Setting Resistors (R1-R4)

Equations (6) and (7) show the input common-mode and output voltage range of the OPA2313 given a 3.3V supply.

$$-200mV < V_{CM} < 3.5V \tag{6}$$

$$100mV < V_{OUT} < 3.2V \tag{7}$$

The gain is calculated as shown in Equation (8).

$$Gain_{Diff\_Amp} = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{R_{SHUNT} \times \left(I_{MAX} - I_{MIN}\right)} = \frac{3.2V - 100mV}{100m\Omega \times \left(1A - \left(-1A\right)\right)} = 15.5\frac{V}{V} \tag{8}$$

The resistor value selected for R_1 and R_3 was 1 kΩ. The resistor value selected for R_2 and R_4 was 15.4 kΩ, which is the nearest 0.1% value to the ideal value of 15.5 kΩ. Therefore the ideal gain of the difference amplifier is 15.4 V/V.

4 Simulation

4.1 Transfer Function

Figure 3 shows the TINA-TI™ schematic used to simulate the dc transfer function.

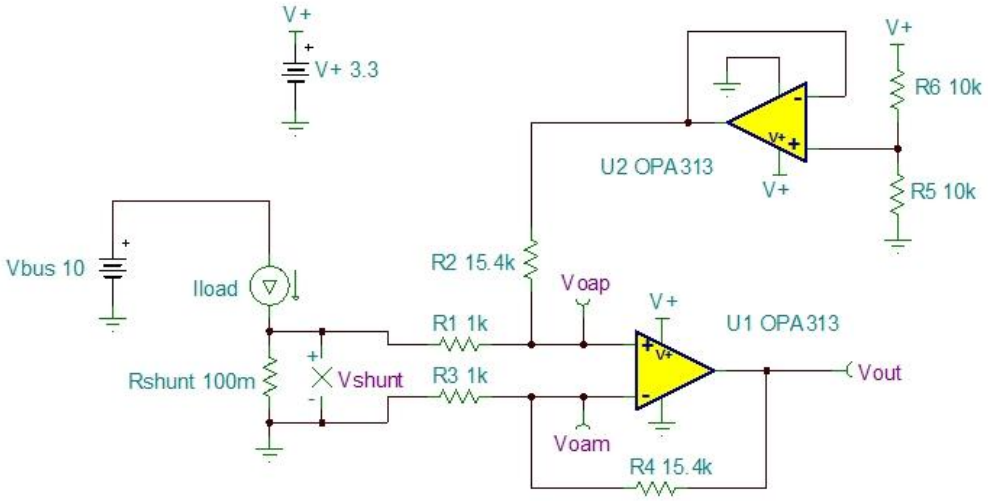


Figure 3: TINA-TI™ Transfer Function Schematic

Figure 4 depicts the simulated dc transfer function results using nominal component values.

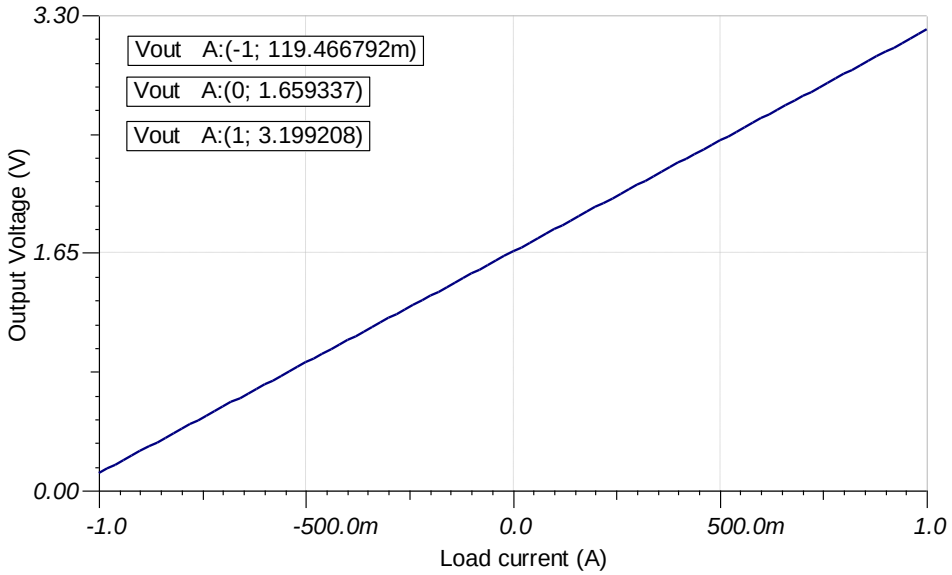


Figure 4: Simulated Nominal Output Voltage vs. Load Current

These results correlate with the ideal minimum and maximum output voltages as calculated in Equations (9) and (10).

$$V_{OUT\_MIN} = -100mV \times 15.4\frac{V}{V} + 1.65V = 110mV \quad (9)$$

$$V_{OUT\_MAX} = 100mV \times 15.4\frac{V}{V} + 1.65V = 3.19V \quad (10)$$

4.2 Monte Carlo Simulation Error Analysis

To analyze error due to the op amps, tolerance of R_{SHUNT}, the difference amplifier resistors R_1-R_4, and the reference voltage divider resistors R_5-R_6, a 1,000 point Monte-Carlo simulation was run at -1 A and 1 A input currents. The results of the Monte-Carlo simulation are shown in Table 3.

Table 3. DC Transfer Results from Calibrated Monte-Carlo Analysis

	Average (μ)	Std. Dev. (σ)
V_{OUT} (V) at -1A	119.481035m	3.424383m
V_{OUT} (V) at 0A	1.659374	2.215354m
V_{OUT} (V) at 1A	3.199267	3.608592m

Using the mean (μ) and standard deviation (σ) from the Monte-Carlo simulation, a prediction of the typical (±1σ) offset error is calculated using Equation (12).

$$OffsetError(\%)_{TYP\_SIM} = \frac{(\mu \pm 1\sigma) - 1.65}{1.65} \times 100 = 0.7\% \quad (11)$$

Similarly, a prediction of the typical gain error is calculated below.

$$GE(\%)_{TYP\_SIM} = \left[\frac{(\mu_{1A} + \sigma_{1A}) - (\mu_{-1A} - \sigma_{-1A})}{2 \times 1.54} - 1\right] \times 100 = 0.22\% \quad (12)$$

4.3 DC Sweep Error Analysis

In addition to the Monte Carlo simulation, worst-case dc sweeps of the circuit in Figure 3 were simulated while varying the resistors within their typical values (±1σ), which is 1/3 of their given tolerance. For example, resistors with a tolerance of 0.1% were change to 0.033%. The typical offset error was simulated to be 0.86% and the gain error was 0.24%. These results correlate well with the Monte Carlo simulation.

4.4 Simulated Results Summary

Table 4 compares the simulation results with the design goals.

Table 4. Design Goals with Simulated Performance

	Goal	Simulated-MC	Simulated-DC Sweep
Offset Error		0.7%	0.86%
Gain Error		0.22%	0.24%
Total Error	±1%	0.734% (RSS)	0.893% (RSS)

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

Figure 5 depicts the printed circuit board (PCB) layout. The traces for the shunt voltage are balanced and short. Wide, short traces were used for the load current path to minimize impedance. All other standard PCB layout practices were observed.

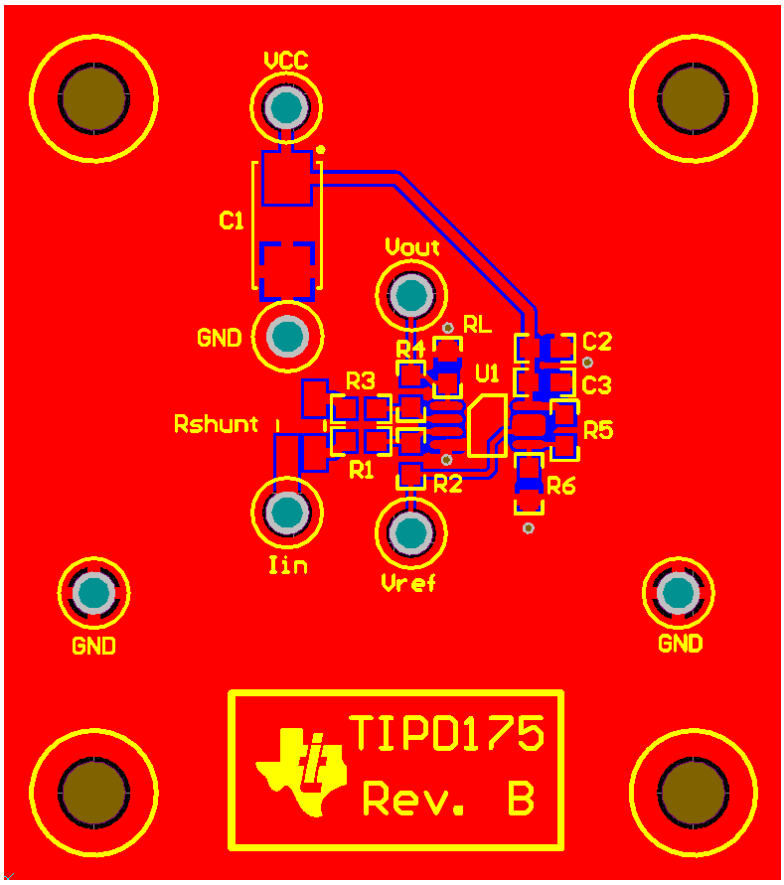


Figure 5: PCB Layout

6 Verification & Measured Performance

6.1 Transfer Function

The output voltage was measured while sweeping the input current from -1 A to 1 A. Five boards were assembled and measured. The transfer function measurement for Board 1 is shown in Figure 6 while the remaining results can be found in Appendix C.

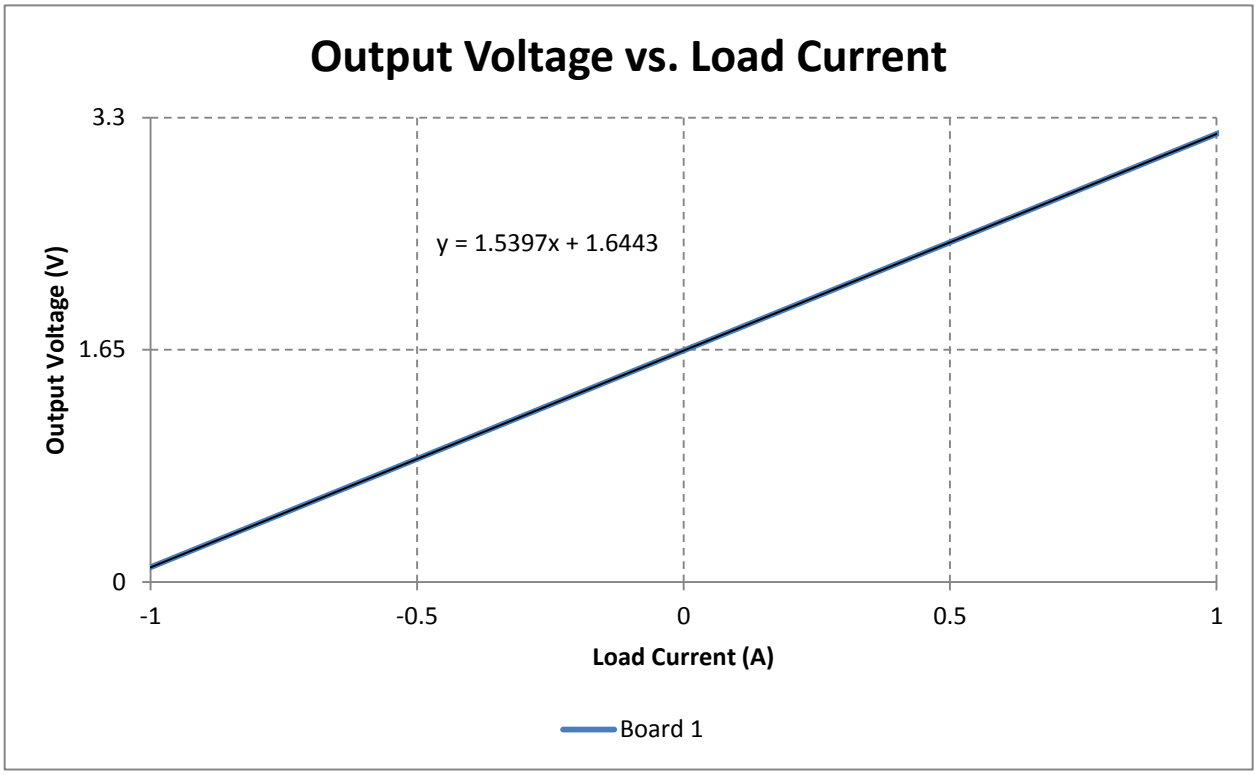


Figure 6: Measured Output Voltage vs. Load Current (Board #1)

The ideal circuit gain (which is the product of the shunt gain, 0.1, and difference amplifier gain, 15.4) is 1.54V/V. The ideal offset voltage is equal to the reference voltage, or 1.65V. Using a straight-line approximation for the results yields the measured gain and offset as shown in Figure 6. The gain and offset error for board #1 is calculated below.

$$\mathrm{OffsetError}(\%)_{\mathrm{MEAS\_BOARD1}} = \frac{1.6443 - 1.65}{1.65} \times 100 = -0.343\% \tag{13}$$

$$\mathrm{GE}(\%)_{\mathrm{MEAS\_BOARD1}} = \frac{1.5397 - 1.54}{1.54} \times 100 = -0.022\% \tag{14}$$

6.2 Measured Results Summary

The measured results are summarized in Table 5.

Table 5. Measured Performance Summary

	GE(%)	Offset Error (%)	RSS Total Error (%)
Board 1	-0.022	-0.343	0.344
Board 2	-0.011	-0.146	0.146
Board 3	-0.084	0.026	0.088
Board 4	0.029	0.448	0.449
Board 5	-0.010	0.621	0.621

7 Modifications

The most significant error contribution is the offset error due to the reference voltage divider accuracy and op amp offset voltage. In order to minimize this error, consider using resistors with a tighter tolerance. Alternate op amps with less offset voltage are listed below. Note that the input common-mode range for the alternate op amps is less than the OPA2313. Therefore it is suggested to limit the shunt voltage to no more than 50 mV below the negative rail for design margin.

Table 6: Alternate Op Amps

Op Amp	V_{OS} @ 25ºC (max, µV)	Vcm(min)	Vcm(max)	Output Swing to Supply (mV)	BW (typ, MHz)
OPA2313	2500	(V-)-0.2	(V+)+0.2	100	1
OPA2317	90	(V-)-0.1	(V+)+0.1	100	0.3
OPA2320	150	(V-)-0.1	(V+)+0.1	35	20
OPA2330	50	(V-)-0.1	(V+)+0.1	100	0.35
OPA2333	10	(V-)-0.1	(V+)+0.1	50	0.35
OPA2365	200	(V-)-0.1	(V+)+0.1	20	50
OPA2376	25	(V-)-0.1	(V+)+0.1	30	5.5

In order to decrease gain error, consider either resistors with a tighter tolerance or a RRI/O instrumentation amplifier (e.g. INA326). For solutions that require low-drift, consider using a current shunt monitor and dual-output reference (e.g. TIPD156) because all resistors are integrated in the package and will drift together.

8 About the Authors

Pete Semig is an Analog Applications Engineer in the Precision Linear group at Texas Instruments. He supports Texas Instruments' difference amplifiers & instrumentation amplifiers. Prior to joining Texas Instruments in 2007, he earned his B.S.E.E. and M.S.E.E. from Michigan State University in 1998 & 2001, respectively. From 2001-2007 he was a faculty member in Michigan State University's Department of Electrical & Computer Engineering where he taught a variety of courses and laboratories.

Timothy Claycomb is an Analog Applications Engineer in the Precision Linear group at Texas Instruments. He earned his B.S. in Electrical Engineering from Michigan State University in 2013.

9 Acknowledgements & References

The authors would like to thank Collin Wells for his technical contributions.

[1] S. Franco, "Circuits with Resistive Feedback," in *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd ed. New York: McGraw-Hill, 2002, ch. 2, pp.75-76.

Appendix A.

A.1 Electrical Schematic

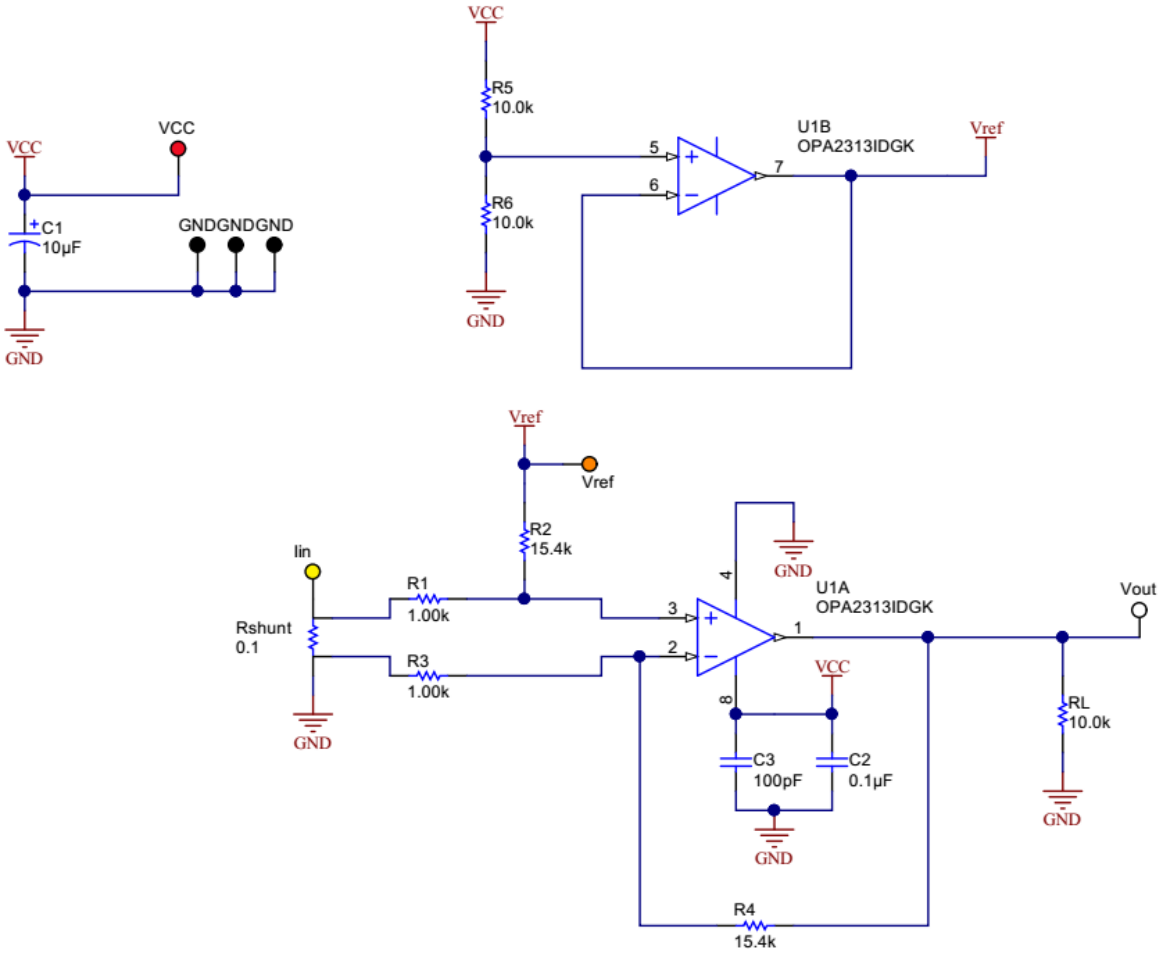


Figure A-1: Electrical Schematic

A.2 Bill of Materials

Quantity	Designator	Value	Description	Manufacturer	Manufacturer Part Number	DigiKey Part Number
1	VCC	Red	Test Point, TH, Compact, Red	Keystone	5005	5005K-ND
3	GND	Black	Test Point, TH, Compact, Black	Keystone	5006	5006K-ND
1	Vout	White	Test Point, Compact, White, TH	Keystone	5007	5007K-ND
1	Vref	Orange	Test Point, Compact, Orange, TH	Keystone	5008	5008K-ND
1	Iin	Yellow	Test Point, Compact, Yellow, TH	Keystone	5009	5009K-ND
1	C2	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	AVX	06033C104KAT2A	478-3714-1-ND
1	C3	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A101JAT2A	478-1175-1-ND
2	R1, R3	1.00k	RES 1K OHM 1/16W .1% 0603 SMD	Bourns	CRT0603-BY-1001ELF	CRT0603-BY-1001ELFCT-ND
1	RL	10.0k	RES 10K OHM 1/10W 1% 0603	Stackpole Electronics Inc	RMCF0603FT10K0	RMCF0603FT10K0CT-ND
1	Rshunt	0.1	RES 0.1 OHM 1/2W 0.5% 1206	Ohmite	LVK12R100DER	LVK12R100DERCT-ND
4	U94, U95, U96, U97		MACHINE SCREW PAN PHILLIPS 4-40	B&F Fastener Supply	PMSSS 440 0025 PH	H703-ND
1	U1		IC OPAMP GP 1MHZ RRO 8VSSOP	Texas Instruments	OPA2313IDGK	296-35004-ND
2	R5, R6	10.0k	RES 10.0K OHM 1/16W .5% 0603 SMD	Susumu Co Ltd	RR0816P-103-D	RR08P10.0KDCT-ND
2	R2, R4	15.4k	RES 15.4K OHM 1/10W .1% 0603 SMD	Susumu Co Ltd	RG1608P-1542-B-T5	RG16P15.4KBCT-ND
4	U90, U91, U92, U93		STANDOFF HEX 4-40THR ALUM 1L"	Keystone	2205	2205K-ND
1	C1	10uF	CAP, TA, 10uF, 25V, +/-10%, 0.5 ohm, SMD	AVX	TPSC106K025R0500	478-1762-1-ND

Figure A-2: Bill of Materials

Appendix B.

B.1 Error Analysis

The transfer function for this design is given in Equation (15).

$$V_{OUT} = V_{SHUNT} \times Gain + V_{REF} \tag{15}$$

Equation (16) is the transfer function in terms of circuit voltages, currents, and components. This equation aids in understanding the error analysis.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \frac{R_4}{R_3} + \left(V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right) \right) \tag{16}$$

B.1.1 Offset Errors

The reference voltage supplied by the resistor divider (R_5 and R_6) and U1B will introduce an offset error. Given a tolerance of ±0.5% for the resistors, supply voltage (V_{CC}) of 3.3V, and ideal dividing ratio of ½, the maximum offset voltage due to R_5 and R_6 is calculated in Equation (17).

$$V_{OS\_R5R6\_MAX} = V_{CC} \times \left(IdealRatio - \frac{1 \mp 0.5\%}{(1 \mp 0.5\%) + (1 \pm 0.5\%)} \right) = \pm 8.25mV \tag{17}$$

This error calculation represents the worst-case scenario. Assuming the resistor values observe a Gaussian 6σ (±3σ) distribution, dividing the tolerance by 3 will yield a typical error analysis (±1σ). This result is calculated in Equation (18).

$$V_{OS\_R5R6\_TYP} = V_{CC} \times \left(IdealRatio - \frac{1 \mp 0.167\%}{(1 \mp 0.167\%) + (1 \pm 0.167\%)} \right) = \pm 2.76mV \tag{18}$$

In addition to the offset due to R_5 and R_6, the op amps U1A and U1B have typical offset voltages of ±0.5mV (±2.5mV maximum).

$$V_{OS\_U1\_TYP} = \pm 0.5mV \tag{19}$$

$$V_{OS\_U1\_MAX} = \pm 2.5mV \tag{20}$$

The CMRR performance of the op amp U1A also introduces an offset error. Equations (21) and (22) calculate the typical and maximum offset errors introduced by the OPA313 given a common-mode voltage near zero. For more information on this calculation, please refer to Part III of the Current Sensing Fundamentals article series.

$$V_{OS\_U1A\_CMRR\_TYP} = 1.65V \times \left(\frac{1}{10^{\frac{85dB}{20dB}}} \right) = \pm 97.8\mu V \quad (21)$$

$$V_{OS\_U1A\_CMRR\_MAX} = 1.65V \times \left(\frac{1}{10^{\frac{70dB}{20dB}}} \right) = \pm 0.52mV \quad (22)$$

Finally, the CMRR performance of the difference amplifier also introduces an offset error. The CMRR performance of a discrete difference amplifier can be calculated using Equation (23). [1]

$$CMRR_{dB} \cong 20\log_{10} \left| \frac{1 + Gain}{4 \times \frac{R_{tolerance}(\%)}{100}} \right| \quad (23)$$

The worst-case CMRR performance of the difference amplifier in a gain of 15.4 V/V using 0.1% resistors is 72.25 dB. The typical CMRR is 81.8 dB (calculated using 0.033% resistors).

The common-mode voltage of the difference amplifier (defined as the average voltage at the input pins) can range from -50 mV to 50 mV. Therefore, the offset voltage due to the difference amplifier CMRR is calculated in Equations (24) and (25).

$$V_{OS\_DA\_TYP} = \pm 50mV \times \left(\frac{1}{10^{\frac{81.8dB}{20dB}}} \right) = \pm 4.1\mu V \quad (24)$$

$$V_{OS\_DA\_MAX} = \pm 50mV \times \left(\frac{1}{10^{\frac{72.25dB}{20dB}}} \right) = \pm 12.2\mu V \quad (25)$$

Table 7 summarizes the offset voltage errors.

Table 7. Summary of Calculated Offset Errors

	Typical	Maximum
Resistor Divider	±2.76mV	±8.25mV
U1A & U1B	±0.5mV	±2.5mV
U1A CMRR	±97.8µV	±0.52mV
Difference Amp CMRR	±4.1µV	±12.2µV

The offset voltages due to the resistor divider (R5 and R6) and the offset voltage of U1B add directly to the output of U1A. The remaining offset voltages are referred to the output of the circuit (RTO) by multiplying by the gain of the difference amplifier (15.4V/V). Therefore we can calculate the total offset error referred to the output as shown in Equation (26). The typical and maximum offset voltages referred to the output are depicted in Equations (27) and (28).

$$V_{OS\_Total\_RTO} = \sqrt{V_{OS\_R5R6}^{2} + V_{OS\_U1B}^{2} + \left(Gain \times V_{OS\_U1A}\right)^{2} + \left(Gain \times V_{OS\_U1A\_CMRR}\right)^{2} + \left(Gain \times V_{OS\_DA}\right)^{2}} \quad (26)$$

$$V_{OS\_Total\_RTO\_TYP} = \pm 8.33mV \quad (27)$$

$$V_{OS\_Total\_RTO\_MAX} = \pm 40.23mV \quad (28)$$

Given an ideal offset voltage of 1.65V, the offset typical and maximum offset errors are calculated below.

$$OffsetError(\%)_{TYP\_CALC} = \frac{\pm 8.33mV}{1.65} \times 100 = 0.5\% \quad (29)$$

$$OffsetError(\%)_{MAX\_CALC} = \frac{\pm 40.23mV}{1.65} \times 100 = 2.44\% \quad (30)$$

The calculated typical offset error correlates well with the simulated results (0.7% and 0.86%). The calculated maximum offset error is larger than the simulated results because the amplifier simulation models only model the typical offset error.

B.1.2 Gain Errors

The shunt resistor, R_{SHUNT}, introduces a gain error. In this design, the tolerance of R_{SHUNT} is 0.5%. Also, any mismatch in the gain setting resistors of the difference amplifier (R_4 and R_3) introduce gain error. Since they each have a tolerance of 0.1% (ε=0.001), the worst-case gain error introduced by the gain-setting resistors of the difference amplifier is approximately 0.2% as calculated in Equation (31).

$$GE_{Diff\_Amp}(\%) = \left[1 - \left(\frac{1+\varepsilon}{1-\varepsilon}\right)\right] \times 100 = 0.2002...\% \approx 0.2\% \tag{31}$$

The following equations calculate the typical (using 1/3 of the resistor tolerance) and maximum gain error expected for this design.

$$GE_{TYP} = \sqrt{0.167^2 + 0.07^2} = 0.18\% \tag{32}$$

$$GE_{MAX} = \sqrt{0.5^2 + 0.2^2} = 0.54\% \tag{33}$$

B.1.3 Total Error

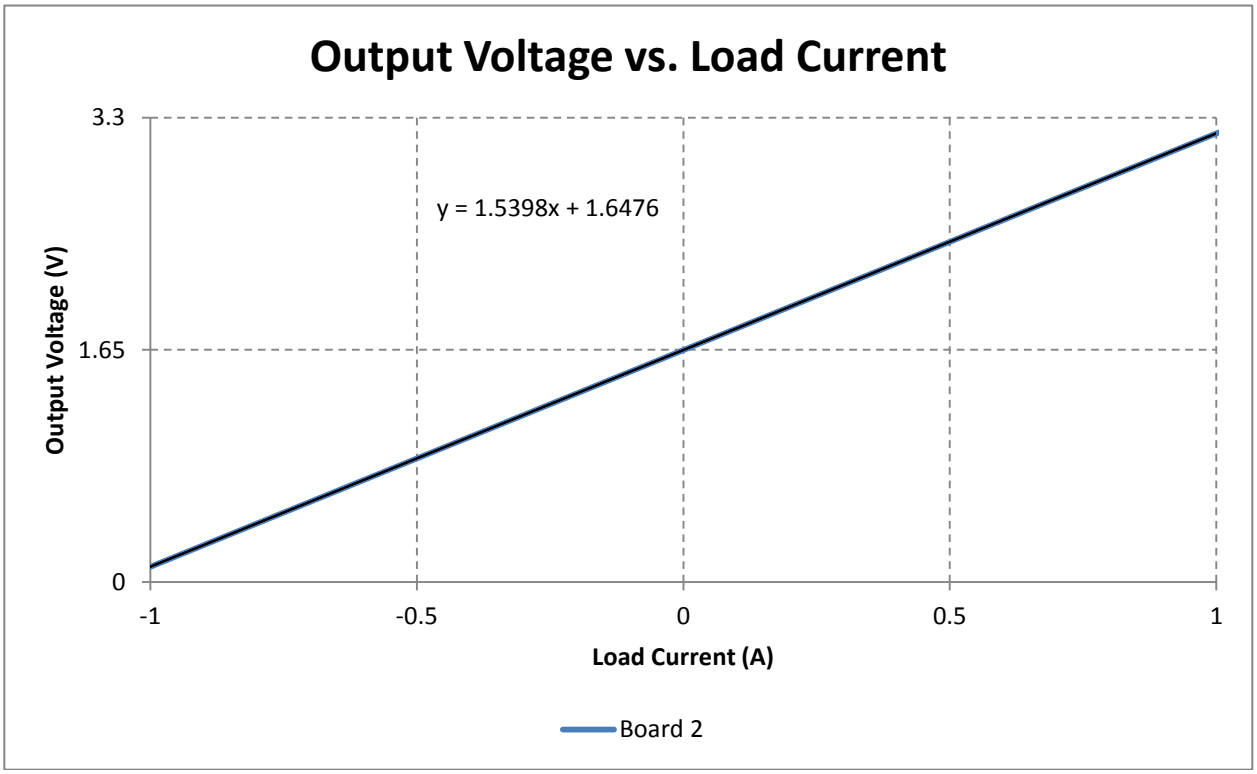
The total error, including both offset and gain errors, is calculated in Equations (34) and (35).

$$Error_{Total\_TYP} = \sqrt{OffsetError_{TYP}{}^2 + GE_{TYP}{}^2} = 0.53\% \tag{34}$$

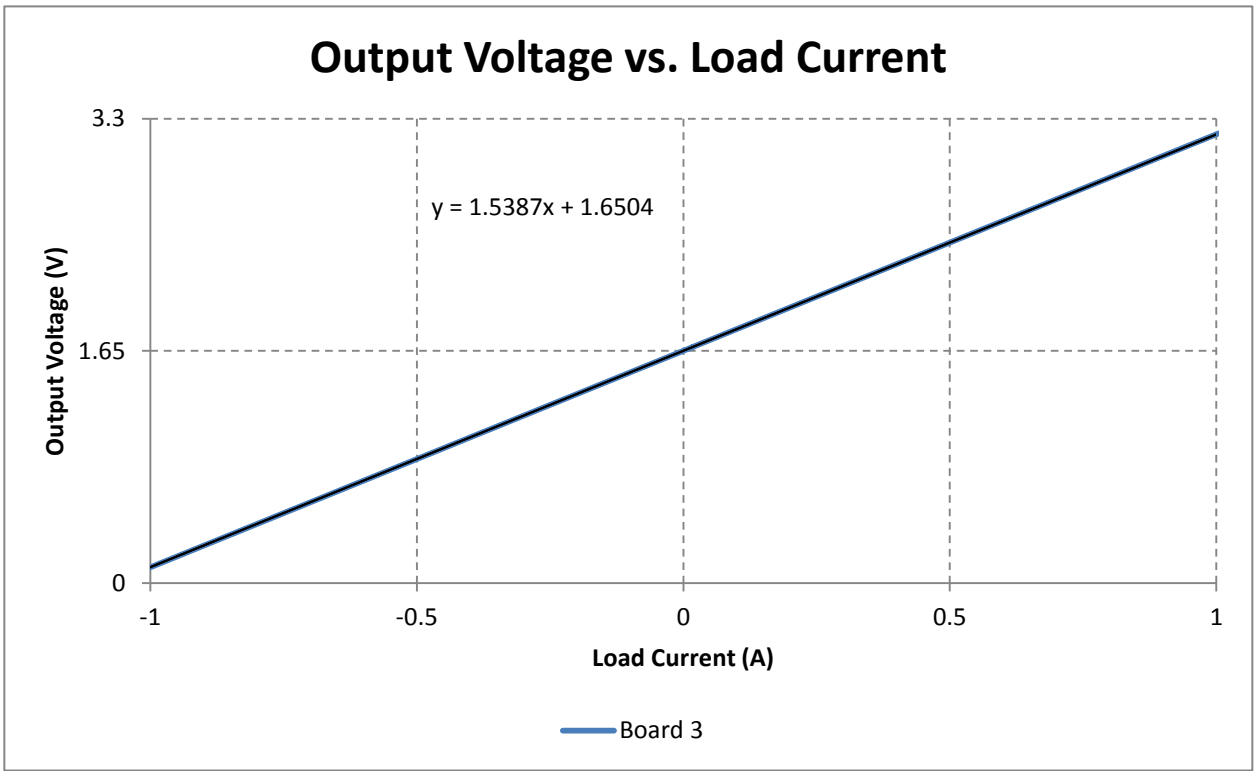
$$Error_{Total\_MAX} = \sqrt{OffsetError_{MAX}{}^2 + GE_{MAX}{}^2} = 2.5\% \tag{35}$$

Appendix C.

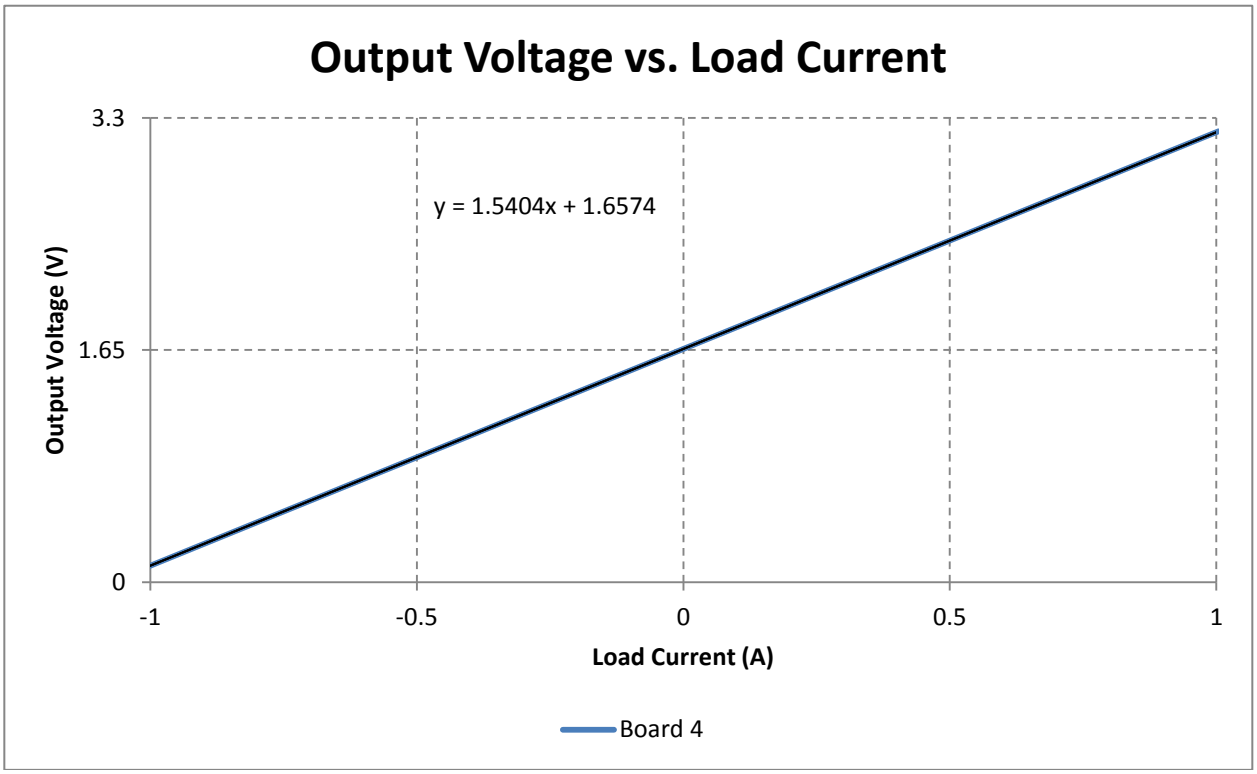
C.1 Board #2



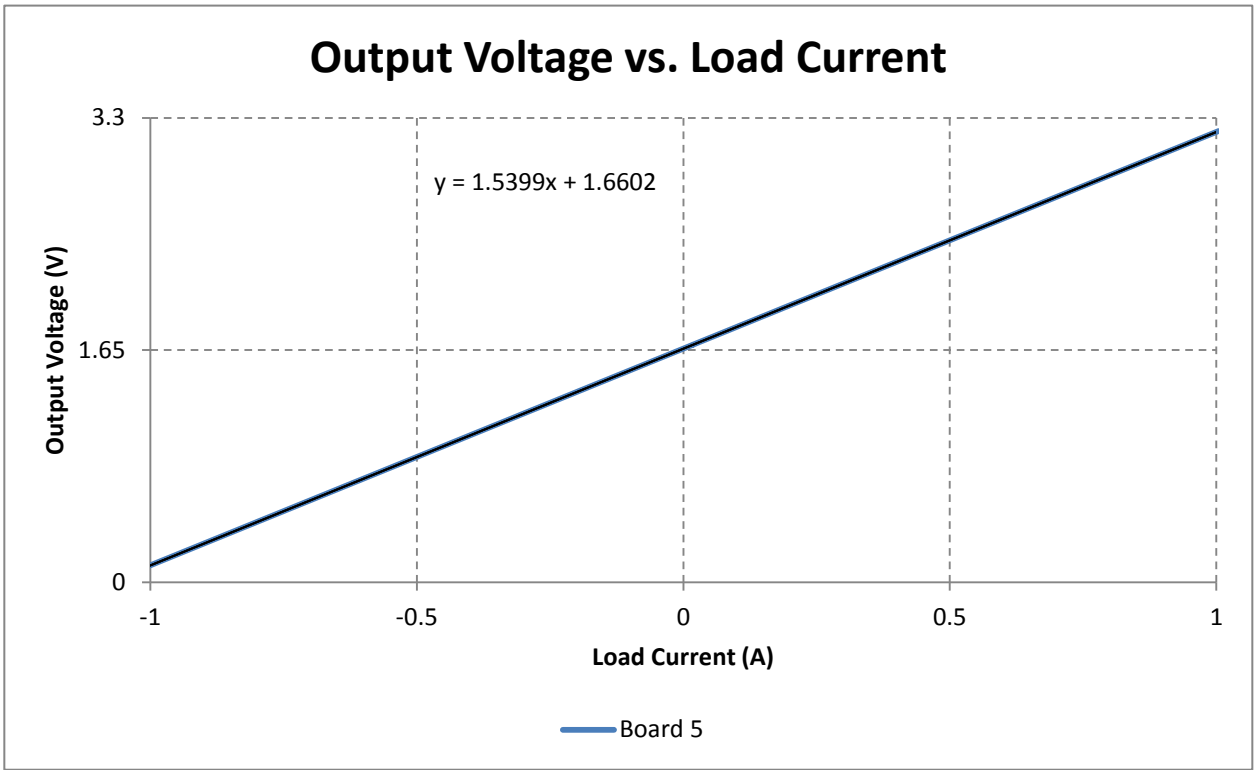
C.2 Board #3



C.3 Board #4



C.4 Board #5



IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265