

# TI High Speed Designs

## High Bandwidth, High Frequency Transmitter Solution



### TI High Speed Designs

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### Circuit Description

The TSW38J84EVM reference design provides a platform to test the 2.5 GSPS DAC38J84 device with the high performance modulators: TRF3722 (including integrated PLL/VCO) and TRF3705. The high sampling rate of the DAC is specifically suited to handle high bandwidth signals. When the RF frequency of operation exceeds the max allocated frequency of the TRF3705 modulator, the TRF3704 device can be substituted. The TRF3704 operates up to 6 GHz and has a large input baseband (BB) bandwidth. The translation network required to properly interface the DAC38J84 to the TRF3704 is described along with some circuit techniques to mitigate issues with high bandwidth signals. Measurement data of the combination of these devices is shown to illustrate the bandwidth performance, output third order intercept performance, and modulator sideband suppression performance.

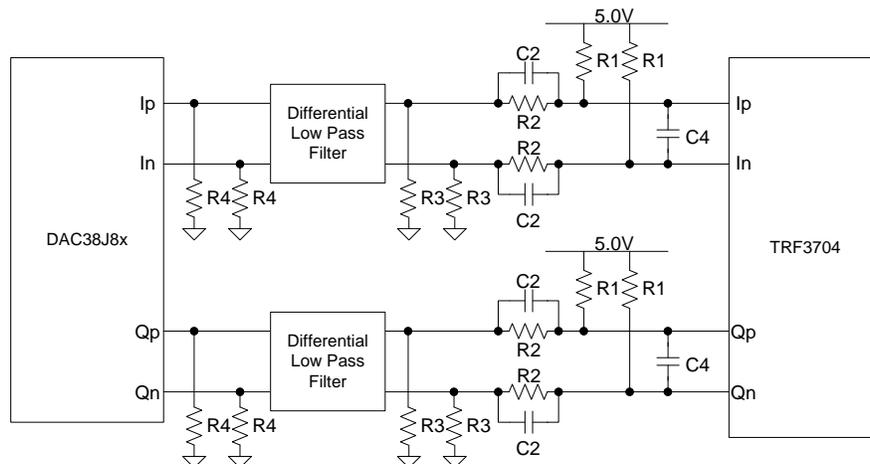
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## 1 TSW38J84 Reference Design

The TSW38J84 reference design demonstrates a high performance RF transmitter. The reference design includes the 2.5 GSPS Quad DAC38J84 which is a JESD204B compliant DAC (Digital to Analog Converter). The Quad DAC supports two separate I/Q channels to drive two outputs. One I/Q pair interfaces to the TRF3722 modulator with integrated PLL/VCO. The other pair interfaces with the TRF3705 modulator. The output frequency of the '22/'05 is limited to 4 GHz. For applications that need to operate up to 6 GHz the TRF3704 modulator can be substituted for the TRF3705. The '04 and '05 are pin compatible though not pin-for-pin replacements. The modifications required to change over the design to the TRF3704 are discussed in the next section.

## 2 Modifications for TRF370417 Operation

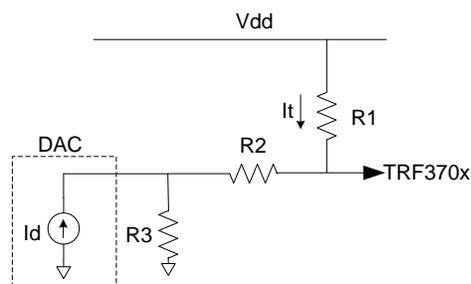
### 2.1 Power Requirement

The TRF3704 modulator operates from a 5.0 V supply. In addition, the translation network is referenced to a 5V supply as well. The board must be modified to operate on this rail.

### 2.2 Translation Network

The DAC38J84 operates at a common mode voltage ( $V_{cm}$ ) of around 0.25V or a bit higher. The TRF3704 operates at a  $V_{cm}$  of 1.7V; hence, a translation network is required to shift the common mode voltage to the proper level.

The DAC38J8x family is a current source DAC. The three resistor translation network is shown in Figure 1.



**Figure 1: Translation Network Model**

With this model the circuit equations are defined where  $I_d$  is the average DAC current and  $V_{dd}$  is the supply rail of 5.0V. The goal is to establish the DAC common mode at around 0.25V and the modulator common mode at 1.7V. The choice of resistors  $R_1$ - $R_3$  is arbitrary to some degree, but it is generally desirable to keep the series resistor  $R_2$  as small as possible to reduce insertion loss through the network.

The design equations and calculations are shown in the MathCAD worksheet in the appendix. The solver function was used to simultaneously solve the equations to derive the resistor values. The resistor values rounded to the closest available 1% tolerance component are listed in table 1.

**Table 1. Translation Network Resistor Values**

Ref Designator	Value
R1	2.21 kohm
R2	953 ohm
R3	25 ohm

### 2.3 *Pseudo-AC Interface*

This network is satisfactory for translating the DC operating point of the DAC to the modulator; however, if left as is there would be some significant impact to the AC signal performance. The introduction of the series resistor introduces insertion loss. According to the calculations the insertion loss is just above 3 dB. In itself, this can be overcome in the system. The other ramification of the series resistance is that it operates with the internal capacitance of the modulator inputs to create an RC low pass filter. This LPF effect will severely limit the BB bandwidth of operation.

To mitigate the problem a large capacitor is added across the series resistor to provide an AC short. This will eliminate the signal insertion loss and eliminate the LPF effect while still maintaining the proper common mode voltages. A value of 1  $\mu$ F was chosen. Note that this capacitor will introduce some gain variation and phase variation at very low frequencies below a 10 kHz. In most applications that are utilizing high signal bandwidths this very small distortion is negligible.

### 2.4 *BB Gain Flatness Adjustment*

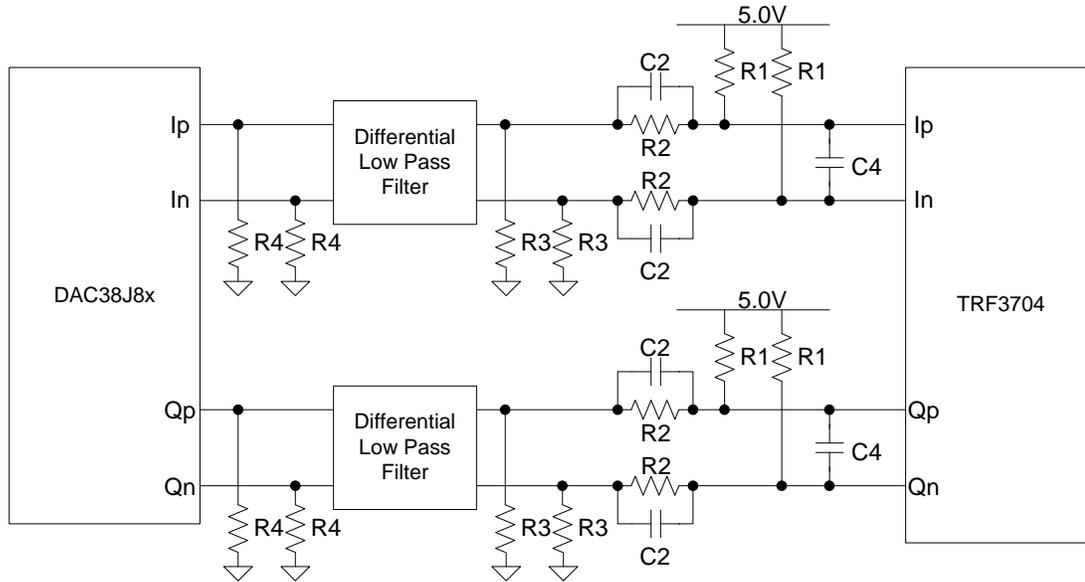
One additional modification for high bandwidth operation is to introduce a small amount of filtering close to the BB input ports of the modulator to help with flattening out the BB gain response. This addition is not absolutely required, but can help to eliminate the BB peaking at high frequency offsets. Note the performance response of the device across BB bandwidth is actually a sum of the BB frequency offset performance and the RF output over frequency performance. In an actual system, it is not possible to decouple the two mechanisms. Gain performance of the modulator over BB frequency offset will then be impacted by the RF frequency variation; hence, any filtering to flatten out the gain response will be dependent on the LO frequency of operation. For this application with an LO of 2.14 GHz the filtering cap of 2.2 pF was chosen to provide a bit flatter gain response.

### 2.5 *Baseband LPF Considerations*

In an actual system it will be desirable to include some amount of BB filtering to eliminate unwanted images from the DAC. The translation shunt resistor,  $R_3$ , is 25 ohms. This resistor can be separated into two 50 ohm resistors in parallel. The LPF can be placed between the two resistors to have a convenient 50 ohm source and load termination without impacting the translation operation. For the measurements in this design the filter was eliminated so that there would be no limitation on the bandwidth performance.

### 2.6 *Interface Schematic*

The interface schematic is shown in Figure 2 between two DAC channels connecting to the I/Q inputs of the TRF3704. Table 2 shows the component values that are represented in the schematic.



**Figure 2: DAC38J8x to TRF3704 Interface Schematic**

**Table 2. Schematic Component Values**

Ref Designator	Value
R1	2.21 kohm
R2	953 ohm
R3, R4	49.9 ohm
C2	1 uF
C4	2.2 pF

### 3 Measured Performance

The DAC38J84 is clocked at 2.456 GSPS which is near its max sampling rate. The interpolation is set to x2. This sets the input data rate to 1.2288 GSPS which is near the maximum rate. In this configuration the DAC can support its maximum bandwidth. The front panel of the DAC's GUI is shown in Figure 3 for reference.

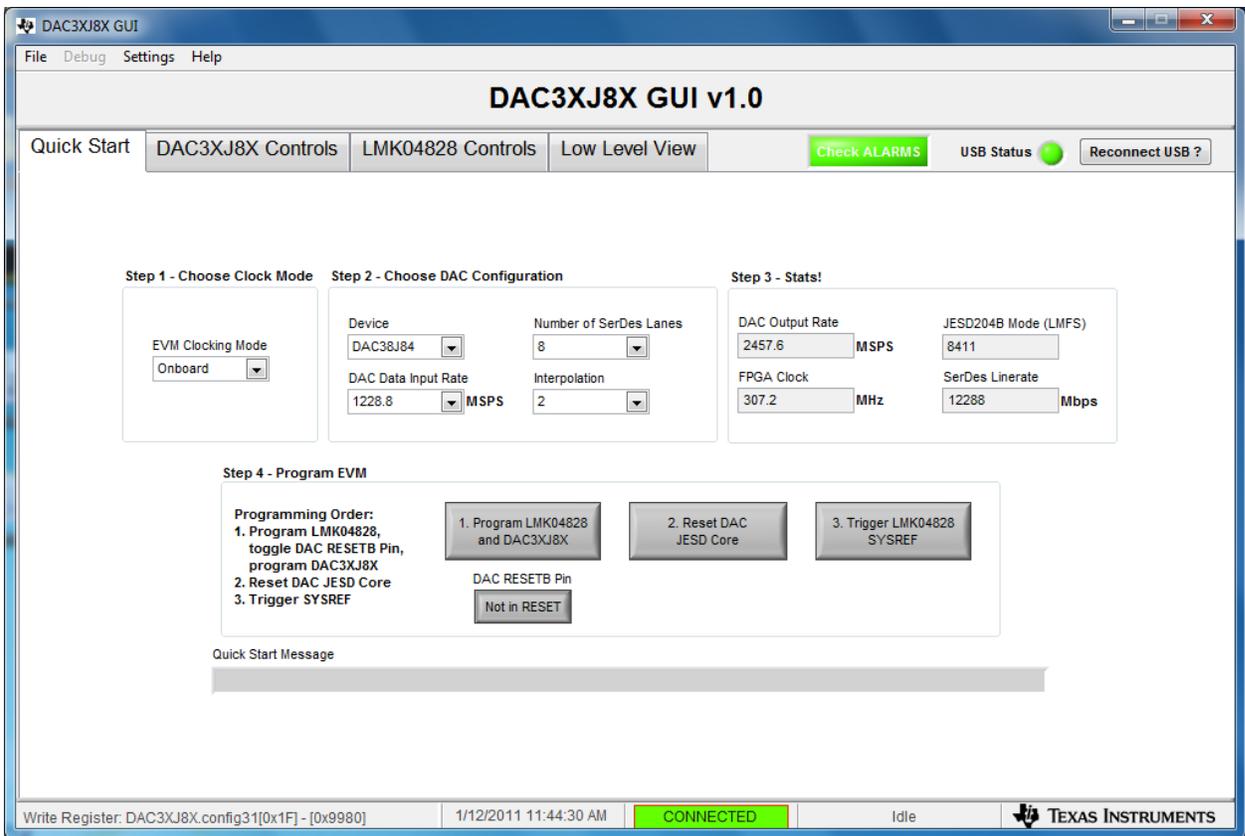
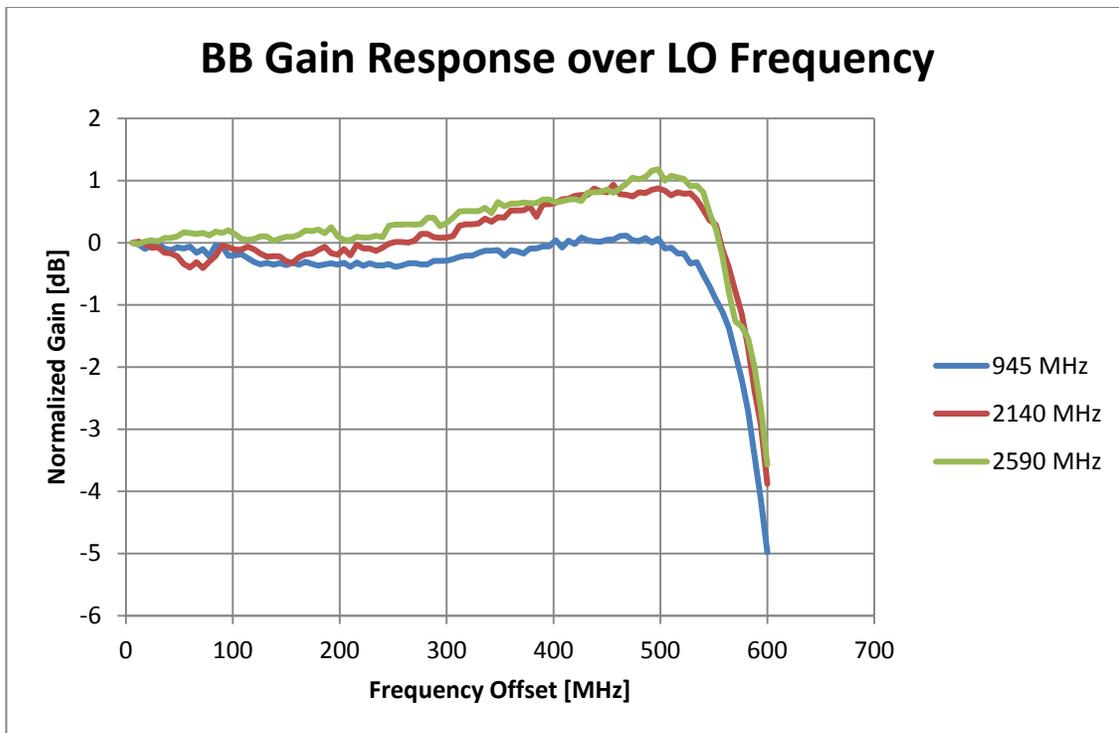


Figure 3: DAC38J84 GUI Configuration

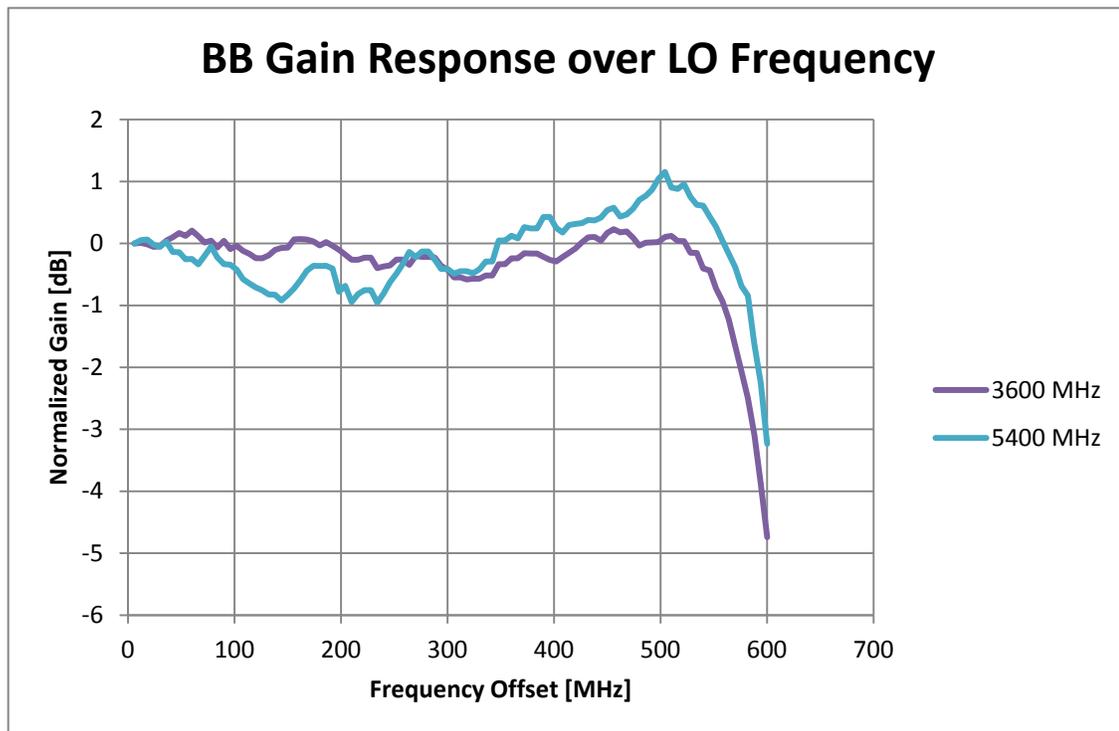
### 3.1 Baseband Bandwidth Response

The baseband bandwidth is measured at several different frequencies across the operational band of the TRF3704 and is shown in Figure 4. Recall that the output response is a combination of the BB bandwidth response plus the RF output response; hence, there are differences when operating at difference LO frequencies. At the higher frequencies the ripple in the response is due to RF mismatch on the output and not the BB input.

The BB 3 dB gain bandwidth response is just under 600 MHz. The 1 dB corner is roughly around 550 MHz or higher depending on the LO frequency.



(a) LO Frequency below 3 GHz



(b) LO Frequency above 3 GHz

**Figure 4: BB Gain Response vs. BB Frequency Offset over LO Frequency**

### 3.2 OIP3 Response over BB Frequency

The OIP3 performance over frequency is measured with two tones separated by 10 MHz that is moved across the BB bandwidth. In order to differentiate variation due to RF output versus BB output the same output frequencies are measured with a low frequency offset (50 MHz) by shifting the LO frequency. The initial LO is set to 2450 MHz. Figure 5 shows the OIP3 response by varying the BB versus varying the LO while keeping the RF output frequency constant. Figure 6 illustrates the OIP3 degradation with respect to BB frequency offset.

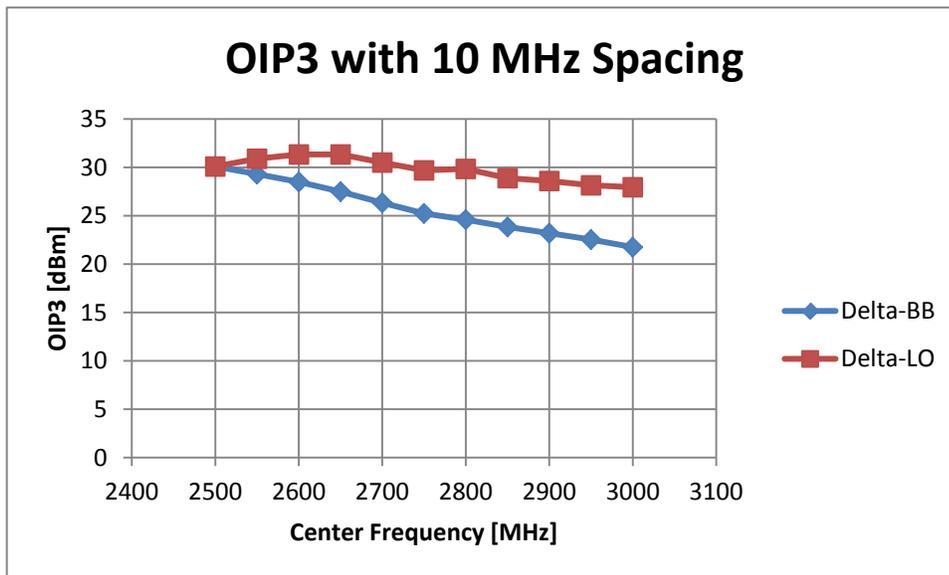


Figure 5: OIP3 Performance with varying BB Frequency Offset and varying LO

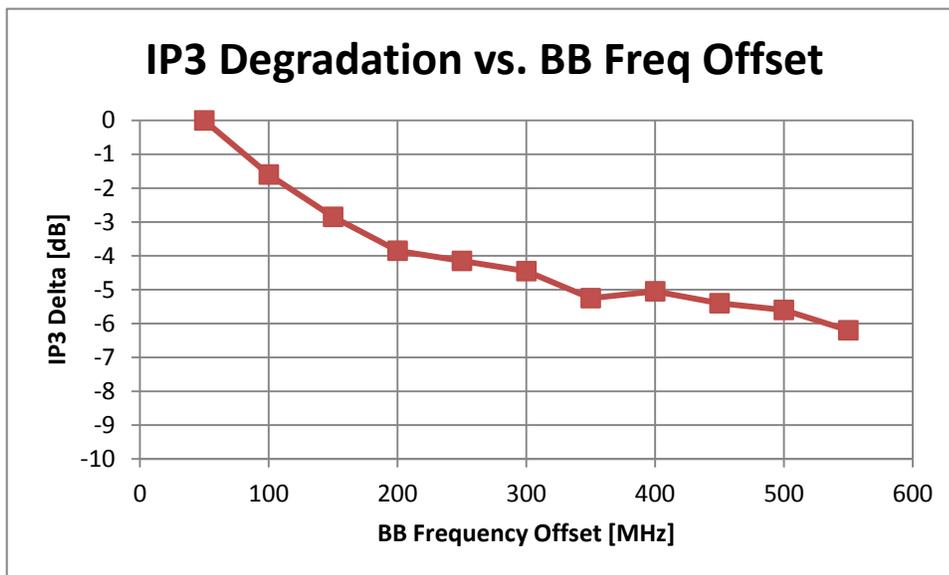


Figure 6: Normalized IP3 Degradation vs. BB Frequency Offset

### 3.3 SBS Response over BB Frequency

Another key concern related to high bandwidth signals in the modulator is the sideband suppression (SBS) performance versus baseband frequency offset. The SBS performance over BB frequency offset at several LO frequencies is shown in Figure 7.

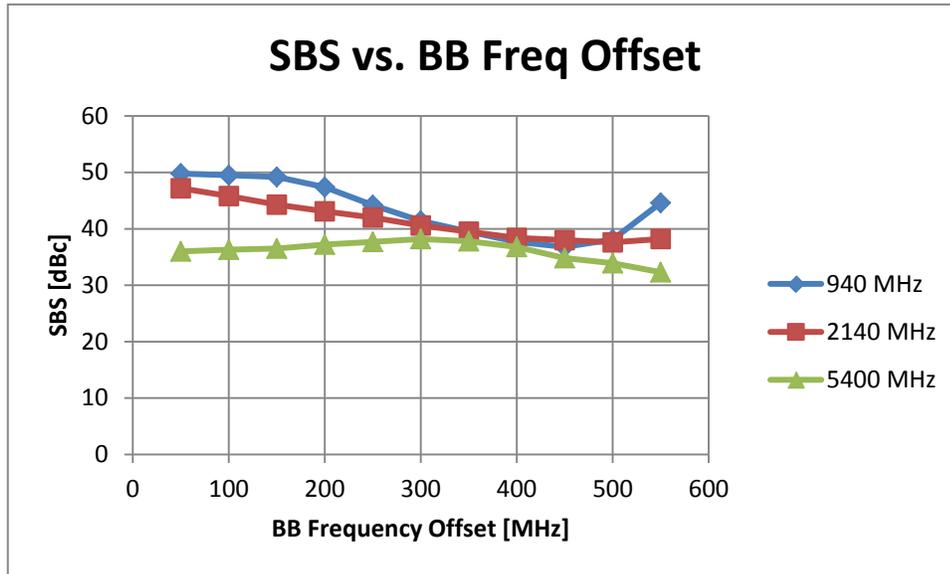


Figure 7: SBS vs. BB Frequency Offset over LO Frequency

## 4 Conclusion

The DAC38J8x in conjunction with the TRF3704 is a suitable platform to operate at output frequencies up to 6 GHz with BB signal bandwidths up to around 550 MHz. This supports RF signal bandwidths of 1 GHz or beyond. The network required to interface the two devices is provided to translate the DAC common mode voltage to 1.7V suitable for the TRF3704 modulator.



### Verify Solution:

$$I_t(I_d) := \frac{V_{dd} - I_d \cdot (R_3)}{R_1 + R_2 + R_3}$$

$$V_d(I_d) := V_{dd} - I_t(I_d) \cdot (R_1 + R_2)$$

$$V_m(I_d) := V_{dd} - I_t(I_d) \cdot R_1$$

$$V_{dmax} := V_d(2 \cdot I_d)$$

$$V_{dmin} := V_d(0)$$

$$\Delta := V_{dmax} - V_{dmin}$$

$$Z_L := \text{pll}(R_3, R_1 + R_2)$$

$$IL := A \left( \Delta, \Delta \cdot \frac{R_1}{R_1 + R_2} \right)$$

$$V_d(I_d) = 0.289 \quad \text{Verify DAC operating point}$$

$$V_m(I_d) = 1.727 \quad \text{Verify modulator common mode voltage}$$

$$V_{dmax} = 0.539$$

$$V_{dmin} = 0.039$$

$$\Delta = 0.5 \quad \text{Verify DAC output swing}$$

$$Z_L = 25 \quad \text{Verify DAC Load}$$

$$IL = 3.164 \quad \text{Insertion loss of the network}$$

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