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Differential Signal Conditioning Circuit for Current and Voltage Measurement Using Fluxgate Sensors

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Design Resources

TIDA-00201	Tool Folder Containing Design Files
THS4531	Product Folder
ADS7254	Product Folder
ADS7854	Product Folder
TPS7A4700	Product Folder
TLV70033	Product Folder
REF5025	Product Folder
REF2025	Product Folder
TLC372	Product Folder
OPA322	Product Folder
F3837x Control Card	Tool Folder

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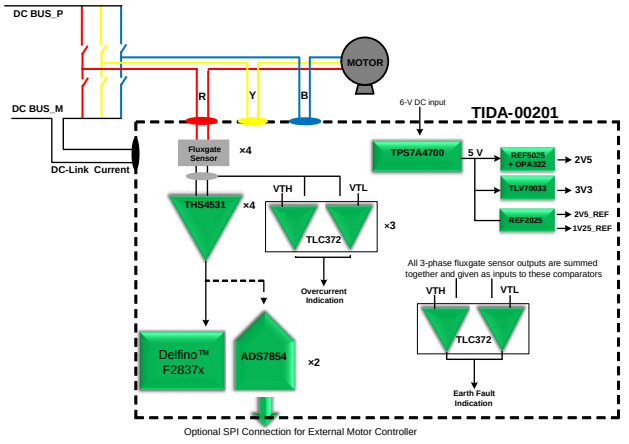
Design Features

- Designed to Measure All 3-Phase Motor Currents Along With DC-Link Current through 6-A Fluxgate Sensor (Scalable up to 50 A)
- Differential Signal Conditioning Circuit to Interface Fluxgate Sensors With Differential ADCs
- Two Onboard 14-Bit Dual-Channel Simultaneous Sampling SAR ADCs With 4-Wire SPI to Interface With External Motor Controllers
- Provision to Measure Current and Voltage Through Internal ADCs of TI Delfino™ Controller F2837x
- <0.1% DC Accuracy of Signal Conditioning Circuit
- Overcurrent and Earth Fault Protections for Each Channel With <100-ns Sensing Delays
- Provision to Interface the Signal Conditioning Circuit With External ADC

Featured Applications

- AC Variable Speed and Servo Motor Drives
- Static Converters
- DC Motor Drives
- UPS Systems
- Solar Inverters
- Power Supplies for Welding Applications



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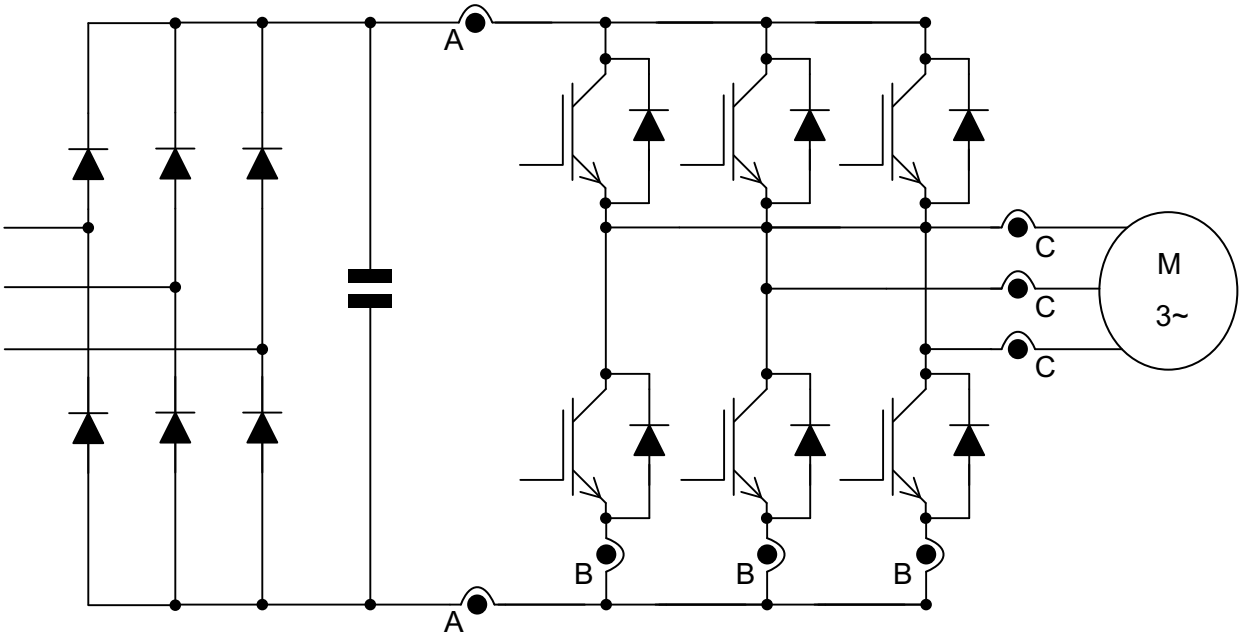
1 System Description

Current measurement is an inherent part of any inverter-driven application. One important reason for measuring the motor current is to control algorithm. Vector control and direct torque control require current sensing for control purposes. Approaches for sensorless control require the motor current measurement to provide accurate control with low cost and complexity. Information of motor parameters is important for several control schemes. Stator current measurement is used for the estimation of these parameters. Motor current information is also required to detect the motor's insulation condition. Electrical insulation is the most critical component for operating electrical motors. Stator insulation failure during motor operation can lead to motor failure, resulting in a costly outage.

Another important phenomenon is protection from hardware overload and earth fault conditions. Typically, these conditions occur when the current exceeds the limit of 200% or 300% of its nominal current. Derating must be taken into account when using the drive in different conditions. Ambient temperature or other environmental conditions such as dust or humidity are unknown, especially when a drive is not installed by the end-user but the machine manufacturer. The end user must identify all derating factors to reach a reliable solution.

Above the drive-designed ambient temperature, drives can usually operate when the maximum output current is derated according to the user's manual of the drive. The switching frequency also plays important role. The higher the switching frequency of the drive is, the more the power semiconductors generate heat losses. Therefore, the drive output current is derated when increasing the switching frequency, which applies to nominal current, overload current, and maximum instantaneous current.

The motor current can be measured at different points in the inverter. Figure 1 shows the overview of usual measurement locations, considering a 3-phase inverter for a motor control application:



A) Current measurement in the DC- and DC+ link
B) Current measurement in the bottom side emitter path of each half-bridge
C) Current measurement in the output phases

Figure 1. Typical Measuring Locations for Current Measurement in Motor Drives

From Figure 1, the least expensive variant of current measurement (*A*) is often used for applications in the lower power range. Typically, the current measurement is done on DC-MINUS bus, because this may be the reference potential of the microcontroller and is therefore not necessary to isolate the signal. Another alternative location of current measurement, found particularly in the low-to-medium power range is variant *B*. In this case, the current is measured at the emitter of the bottom IGBT of each arm in a 3-phase inverter. The end user can also dispense with third current measurement as this can be derived by calculation based on the two measured current signals. The advantage of this measurement method is similar to that of variant *a*, in that the negative section of the DC-bus can be taken as the common reference potential. However, the disadvantage is the increased stray inductance. In high dynamic drives and high-power applications, current is usually measured in the output phases of the inverter (variant *C* in Figure 1). The third current sensor is not necessary in this case either.

The design TIDA-00201 is predominantly meant for current measurement using fluxgate sensors in AC motor drives, but the design can also be used for DC drives. The objective of this design is to provide a solution for differential signal conditioning circuit along with ADC to measure motor current using fluxgate sensors, typically available from companies like LEM Technologies and VACUUMSCHMELZE. It is very common to use single-ended ADCs integrated into the controller for current measurement. Single-ended measurements are more prone to noise in a larger drive system, which can lead to inaccuracies in the measurement. Differential measurement would help to overcome the noise issues. With the Delfino series of controllers (consisting of differential input ADCs) from Texas Instruments (TI), it is possible to do measure differentials overcoming noise issues.

The signal conditioning circuit for fluxgate current sensors is required for the following reasons:

- Fluxgate sensors have inherent noise at 450 kHz / 900kHz because of the internal oscillator and switching, so proper filtering is required.
- Typical fluxgate sensors have a reference signal on REF pin (always at 2.5 V) and signal output available on the OUT pin (±0.625 V riding on a 2.5-V reference). The output voltage of fluxgate sensors may not match the input range of analog-to-digital converters, or ADCs (external or internal to the controller). In this scenario, level shifting may be required.
- Fluxgate sensors can measure up to 300% of their nominal rating. It is important to detect the overload condition and protect the drive.
- For a fluxgate sensor with nominal current (In) of 6 A with 300% of nominal current rating, the signal strength can vary from 0.625 V [2.5 – (3 × 0.625)] to 4.375 V [2.5 + (3 × 0.625)]. However, the ADCs integrated into microcontrollers can take 0 to 3.3 V, so level shifting is required.
- If using differential ADC inside Delfino controllers, the common-mode voltage needs to be shifted from 2.5 V to 1.25 V, unlike the external ADCs.

2 Design Requirements

- To measure a 3-phase motor current and DC-Link current in a variable speed drive using fluxgate sensor (up to 6 A)
- Signal conditioning circuit with 0.1% accuracy to interface with a differential ADC
- Simultaneous sampling of all current channels
- Hardware overload detection within < 100 ns
- Hardware earth fault detection within < 100 ns

3 Block Diagram

The system block diagram is shown in Figure 2. There are four fluxgate current sensors used in the design: three for the motor phase currents and one for measuring the current flowing through the DC-Link. Each of the sensors is interfaced with a fully-differential amplifier (FDA), THS4531. The outputs of each THS4531 are:

1. Connected to onboard 14-bit SAR ADCs (ADS7854), the digital output of which is taken out on a connector to interface with external motor controllers or processors
2. Connected to 180-pin connector to interface with Internal ADC of Delfino F2837x

To provide protection against overcurrent fault condition, each of the phases is provided with two fast responding comparators TLC372 (one for detection of overcurrent in a positive half-cycle and one for detection of overcurrent in a negative half-cycle). For ground fault detection, the output signals coming from each of the phases are combined together and compared against references using two comparators TLC372s. Both the protection circuits have a response time of less than 100 nanoseconds.

The entire board is powered using the 6-V DC power supply available on most of the industrial motor drives. 6-V DC input is step-downed by a high-precision, low-noise low-dropout regulator (LDO) TPS7A4700 to generate 5 V. (TPS7A4700 has an input voltage range up to 36 V, so it can also be used in case a 15-V or 24-V supply is available). The 5 V is used to power fully-differential amplifiers, onboard ADCs, and the fluxgate current sensors. For a digital supply, the low-cost LDO TLV70033 is used for 5-V to 3.3-V conversion. The output common-mode voltage (VOCM) for THS4531 can be set at 2.5 V when used with 5-V ADCs or 1.25-V when used with the internal ADC of the Delfino F2837x controller. The 2.5-V reference is generated using REF5025 and OPA322 (used as a buffer for reference). The REF2025 is used to generate reference voltage of 1.25 V and 2.5 V.

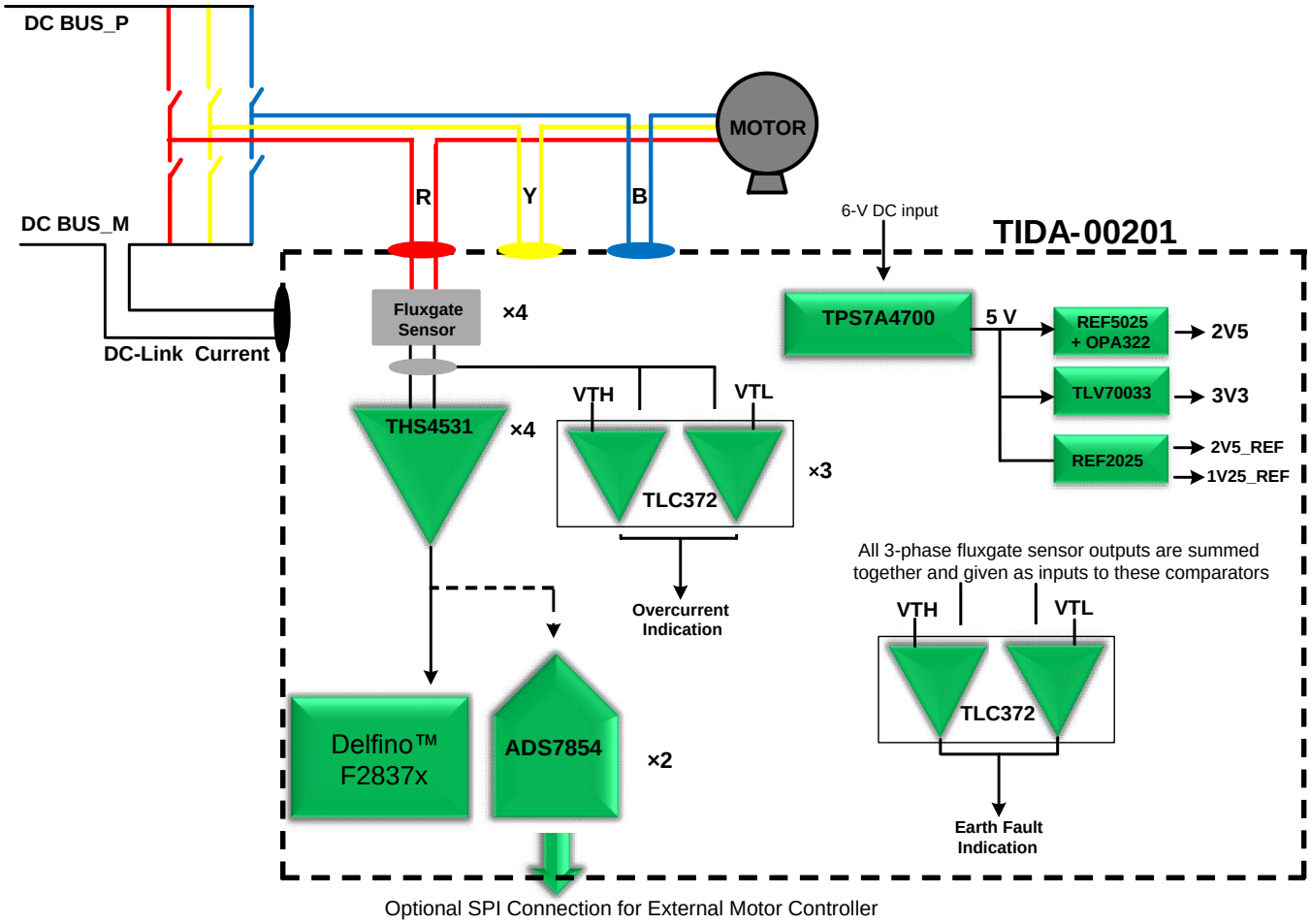


Figure 2. System Block Diagram

4 Highlighted Products

The reference design features the following devices:

- THS4531: Ultra-low power, rail-to-rail output, fully-differential amplifier
- ADS7254 and ADS7854: Dual, high-speed, 12-bit and 14-bit, simultaneous-sampling, SAR ADCs
- TPS7A4700: 1-A, low noise (4.17 μV_{RMS}), high-voltage, LDO
- TLV70033: 200-mA, low IQ, LDO
- REF5025: Low-noise, very low-drift, precision voltage reference
- OPA322: Low-noise, 1.8-V RRIO, CMOS operational amplifier with shutdown
- REF2025: Low-drift, low-power, dual-output VREF, and VREF / 2 voltage reference
- TLC372: Dual general purpose LinCMOS™ differential comparator

For more information on each of these devices, see their respective product folders at www.ti.com or click on the links for the product folders in Design Resources.

5 Fluxgate Technology

5.1 Open-Loop and Close-Loop Fluxgate Sensors

The operating principle of open-loop current transducers is shown in Figure 3 (taken from LEM Technologies' voltage transducer catalogue).[8] The magnetic flux created by the primary current IP is concentrated in a magnetic circuit and measured in the air gap using a fluxgate device. The output from the fluxgate device is then signal conditioned to provide an exact representation of the primary current at the output.

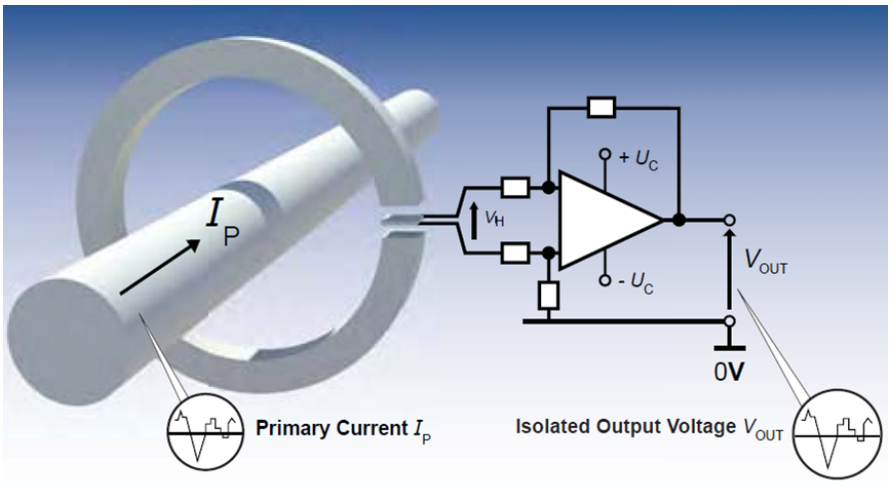


Figure 3. Open-Loop Fluxgate Sensor

On the other hand, the operating principle of a close-loop fluxgate sensor is that of a current transformer equipped with a magnetic sensing element, which senses the flux density in the core. As shown in Figure 4, the output of the field sensing element is used as the error signal in a control loop driving a compensating current through the secondary winding of the transformer.[8] At low frequencies, the control loop maintains the flux through the core near zero. As the frequency rises, an increasingly large fraction of the compensating current is due to the operation in transformer mode. The secondary current is therefore the image of the primary current. In a voltage output transducer, the compensating current is converted to a voltage through a precision resistor and made available at the output of a buffer amplifier.

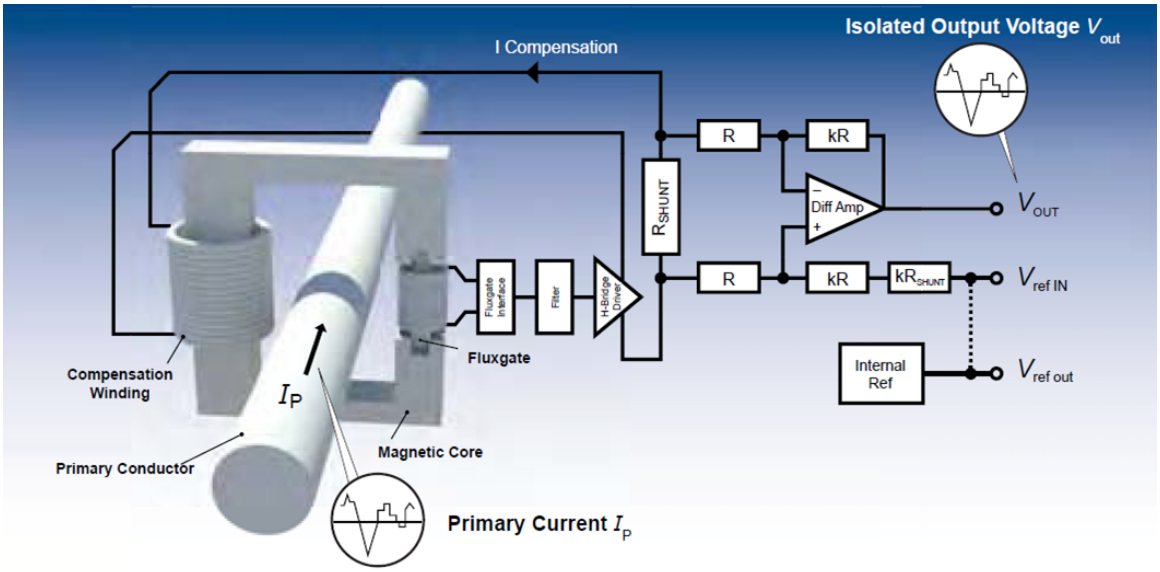


Figure 4. Close-Loop Fluxgate Sensor

5.2 Details of Fluxgate Sensor CKSR 6-NP

Selecting the right transducer is often a trade-off between several parameters: accuracy, frequency response, weight, size, costs, and so on. The CKSR 6-NP is a close-loop fluxgate sensor from LEM Technologies. The CKSR 6-NP typically measures current (DC, AC, or pulsed) with galvanic separation between the primary and secondary circuit. The internal structure of CKSR 6-NP is shown in Figure 5.

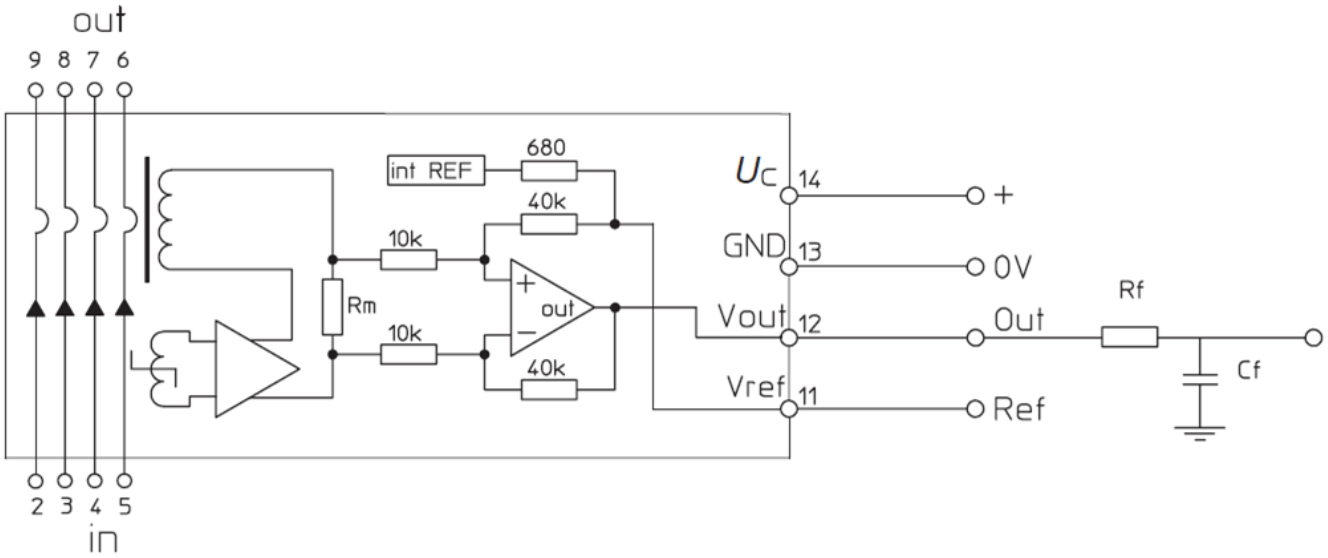


Figure 5. Internal Structure of CKSR 6-NP

The CKSR 6-NP can do bipolar measurements with a single unipolar 5-V power supply. The device can provide its internal voltage reference on an external pin (VREF) or receive an external voltage reference to share **it** with microcontrollers or ADCs. The output signal is available on the OUT pin, which is an amplified voltage signal proportional to the primary current. In a single supply voltage, the output signal varies around a non-zero reference. In CKSR 6-NP, the output signal rides over a 2.5-V reference. The output voltage is proportional to the nominal primary current as shown in Equation 1.

$$VOUT = VREF \pm 0.625 \times \frac{I}{In} \quad (1)$$

where

- VOUT is output voltage
- I is the primary current
- In is nominal primary current (for example, In = 6 A for CKSR 6-NP)

Close-loop fluxgate transducers provide excellent accuracy at 25°C, generally below 1% of the nominal range, and a reduced error over the specified temperature range (–40°C to 105°C). Table 1 shows the accuracy data for CKSR 6-NP (taken from its datasheet).[7]

Table 1. Accuracy of CKSR 6-NP

PARAMETER	SYMBOL	UNIT	MIN	TYP	MAX
Overall accuracy	X_G	% of I_{PN}			1.7
Overall accuracy at T_A = 85°C (105°C)	X_G	% of I_{PN}			2.2 (2.4)
Accuracy	X	% of I_{PN}			0.8
Accuracy at T_A = 85°C (105°C)	X	% of I_{PN}			1.4 (1.6)

6 Overcurrent and Earth Fault Protection

Contemporary state-of-the-art inverters are equipped with full IGBT protection, including overcurrent and ground fault protection. An overcurrent condition is one of the fatal drive faults that could destroy IGBT devices in a motor drive system. IGBT overcurrent conditions fall into three categories: ground fault, line-to-line short, and shoot-through.

Table 2. Overcurrent Conditions and Possible Causes

OVERCURRENT CONDITION	POTENTIAL CAUSE
Ground fault	Motor insulation breakdown to ground
Line-to-line short	Mis-wiring, motor leads short, motor phase-to-phase insulation breakdown
Shoot-through	False IGBT turn-on

Table 2 lists overcurrent conditions and their potential causes. When considering an IGBT overcurrent protection scheme, evaluate two important factors. The first factor is what type of overcurrent protection the system must provide and how the system can shut down. The second factor is the control architecture. Control architecture significantly influences the method and implementation of the overcurrent protection. Protection of IGBT devices is normally implemented in the hardware circuit. However, the circuit implementation and the type of overcurrent-sensing device varies depending on which overcurrent condition is being addressed.

This design implements the overcurrent protection using two comparators for each phase. The two thresholds are derived based on the output voltage coming from fluxgate sensors (one for the positive cycle and one for the negative cycle). On the other hand, the earth fault protection is implemented by adding the three signals coming from current sensors connected in each phase and compared against two thresholds (one for the positive cycle and one for the negative cycle).

The total propagation delay of shutdown also is important. The current sensor itself has some delay, which includes delay for the sensing mechanism and its own response time. Therefore, no matter how the protection circuit is implemented, this delay time must be added to the circuit delay to meet the IGBT short-circuit duration time.

7 Component Selection and Circuit Design

7.1 Selection of Differential ADC

- Input voltage range: CKSR 6-NP fluxgate sensor provides a 2.5-V reference output and an output voltage proportional to primary current riding on a 2.5-V reference signal. The output voltage corresponding to the measured current is given by VREF – VOUT. This differential signal can go up to 300% of its nominal output (that is, ±0.625 × 3 = ±1.875 V).
- Number of channels: For three phases (R, Y, and B) and DC-Link current measurement, the total number of channels required is four. It is better to have four ADCs that can be simultaneously sampled.
- Simultaneous sampling: For optimal 3-phase motor control, it is important to take simultaneous current measurements for each of the phases.
- Sampling speed: Typical industrial motor drive application uses sampling frequency of 100 to 250 kSPS, so the minimum sampling frequency required for the selected ADC is 300 kSPS.
- Number of bits (resolution): Generally, 12 to 14 bits of resolution is enough for an industrial motor drive using fluxgate sensors.
- Supply voltage: Since the CKSR 6-NP has an operating voltage range from 4.75 to 5.25 V, use an ADC with a supply voltage of 5 V.
- Reference requirement: Internal as well external reference options are good to have.

ADS7254 and ADS7854 are the suitable devices for the mentioned criteria. The features of ADS7254 and ADS7854 are as follows:

- Pin compatible family: 12 to 14 bits
- Simultaneous sampling of two channels (If the /CS signal of two ADS7x54 devices combine, all four ADCs — two in each ADS7x54 — can be sampled simultaneously).
- Sampling speed: 1 MSPS
- Fully differential inputs
- Excellent DC/AC performance
- Dual, programmable, buffered 2.5-V internal reference for gain calibration
- Extended temperature range: –40°C to 125°C

7.2 Selection of Differential Amplifier

The differential amplifier is a critical piece of the analog signal chain and can often have a dramatic impact on the performance of the entire signal chain. The primary functions of this FDA are:

1. To buffer the inputs coming from the sensor
2. To amplify the low level input signals coming from the sensor
3. To provide the desired common-mode voltage at the output

Table 3 gives a comprehensive list of the factors that need to be considered in determining the choice of the differential amplifier.

Table 3. Selection Considerations for the FDA

REQUIREMENT	BENEFIT
High input impedance	Minimizing the impedance reduces the input loading on sensor and the input current offsets on input resistors.
Input current noise	Minimizing the current noise reduces the amount of current noise that becomes converted to voltage noise on input resistors.
Voltage noise	Minimizing the voltage noise improves the overall signal-to-noise ratio
CMRR versus frequency	Maximizing this comparison reduces the amount of input offset changes due to high dv/dt at the inverter output.
Resistive gain matching	Maximizing this matching improves the total unadjusted system error.
Voltage offset drift	Minimizing this drift reduces the amount that the total unadjusted error changes at the output of the FDA.
Single-supply operation	Designing a single-supply amplifier simplifies the system supply requirements. The operation usually correlates with a lower power architecture.
Low power	This requirement enables use in power-sensitive or battery monitoring applications.
Input type	Using differential input structure can improve common-mode noise rejection.
Output type	Using differential output structure can improve common-mode noise rejection at ADC inputs as well as potentially reduce or relax the signal conditioning circuitry.

This reference design uses THS4531 as a front-end amplifier for the ADC. The THS4531 is a fully differential op-amp and can amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 6 (VOCM and PD inputs not shown). The gain of the circuit is set by R_F divided by R_G.

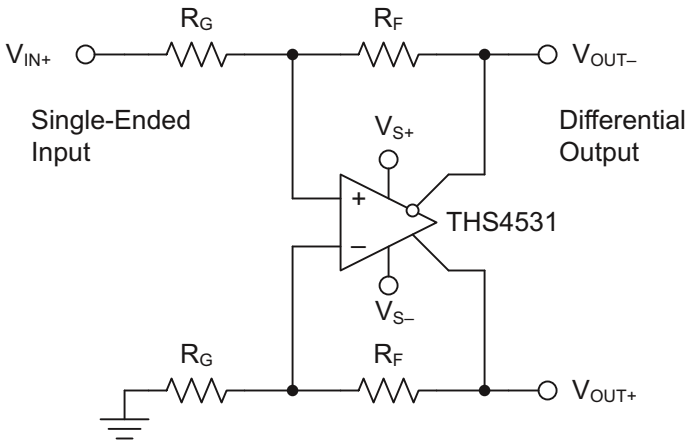


Figure 6. Differential Input Differential Output Amplifier

The output common-model voltage for THS4531 is set by the voltage at the VOCM pin, and the internal circuit works to maintain the output common-mode voltage as close as possible to this voltage. If left unconnected, the output common-mode is set to mid-supply by internal circuitry, which may be over-driven from an external reference source.

7.3 Selection of External Voltage References

TIDA-00201 uses the ADS7254, which has an external reference voltage range from 2.4 V to AVDD (or 5 V) as shown in Table 4 (taken from the ADS7254 datasheet).[9]

Table 4. Voltage Reference Input Limits

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREF Reference voltage (input)	±VREF range	2.4	2.5	AVDD	V
	2 × VREF range	2.4	2.5	AVDD / 2	V

The design needs an external reference IC that can provide 2.5 V. The REF5025, selected for this reference, is a low-noise, low-drift, very high-precision voltage reference.

On the other hand, the internal ADC of a controller can take a maximum voltage of 2.5 V on the analog input pins. For signals coming to the inputs of internal ADCs, the common-mode voltages should be at mid-scale to bias the input bipolar signals. REF2025 can provide two voltages: 1.25 V and 2.5 V.

7.4 Selection of Comparator

A typical industrial drive needs to have overcurrent and earth fault protection to operate within 300 nanoseconds. To reach this goal, the following comparators are compared and TLC372 is selected. The TLC372 has a 100-nanosecond response time. Table 5 shows the comparison chart.

Table 5. Comparator Comparison

PARAMETER	LM293	LM293A	TLC372	TLV1702	LMV7235	LM6511	TLV1391
No. of Channels	2	2	2	2	1	1	1
Supply voltage (min) in Volts	2	2	3	2.2	2.7	2.5	2
Supply voltage (max) in Volts	36	36	16	36	5.5	30	7
T(RESP) low to high (in µS)	1.3	1.3	0.2	0.78	0.075	0.18	0.7
Output type	Open collector, open drain	Open collector, open drain	Open collector, open drain	Open collector	Open drain, push-pull	Open collector	Open collector, open drain
Input offset voltage (in mV) - Max	5	2	5	0.3	6	8	9
Input offset current (in nA) - Max	50	50	0.001	0.5	200	200	150
Input bias current (in nA) - Max	250	250	0.03	20	400	50	400
Supply current (in mA) - Max	1	1	0.3	??	0.1	5	0.175
Packages available	SOIC-8, VSSOP-8, PDIP-8	SOIC-8, VSSOP-8, PDIP-8	SOIC-8, TSSOP-8, PDIP-8, SO-8	MSOP8-, QFN-8	SOT-23, SC-70	SOIC-8	SOT-23
Temperature (in °C)	–25 to 85	–25 to 85	–40 to 125	–40 to 125	–40 to 85	–40 to 85	–40 to 85

7.5 Selection of Power Devices: Voltage Regulators

The entire board is powered using the 6-V DC power supply available on most of the industrial motor drives. The drive can also have 24-V or 15-V supplies available. To step down the 6-V DC input to generate 5 V, the board requires a high-precision, low-noise LDO. The 5-V is used to power fully differential amplifiers, onboard ADCs as well as the fluxgate current sensors, so the total current output requirement from the LDO is at least 500 mA.

The TPS7A47 is a family of positive voltage (36 V), ultra low-noise (4 μV_{RMS}) LDOs capable of sourcing a 1-A load. The TPS7A4700 output voltages are user-programmable (up to 20.5 V) using a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, which reduces the overall component count. The TPS7A47 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, ADCs, digital-to-analog converters (DACs), and other high-performance analog circuitry. (TPS7A4700 has an input voltage range up to 36 V, so the device can also be used in case a 15-V or 24-V supply is available). The digital supply requires a low-cost LDO to convert the 5 V to 3.3 V with a <200-mA output current capability. TLV70033 is a 3-pin, low-cost LDO that can provide the 200-mA current to convert the 5 V to 3.3 V.

8 Circuit Design

8.1 Decoupling for Fluxgate Current Sensor

As per the CKSR 6-NP datasheet, the internal fluxgate oscillator draws current pulses of up to 30 mA at a rate of 900 kHz.[7] A significant 900-kHz voltage ripple on the supply pin (Vc) can indicate a power supply with high impedance. At these frequencies, the power supply rejection ratio is low, and the ripple may appear on the transducer output Vout and reference Vref. The transducer has internal decoupling capacitors, but in the case of a power supply with high impedance, it is better to use local decoupling (100 nF or more, located close to the transducer).

In this design, the fluxgate sensor is decoupled using the 1-µF ceramic capacitor (as shown in Figure 7). The capacitor is placed very close to the sensor in the layout.

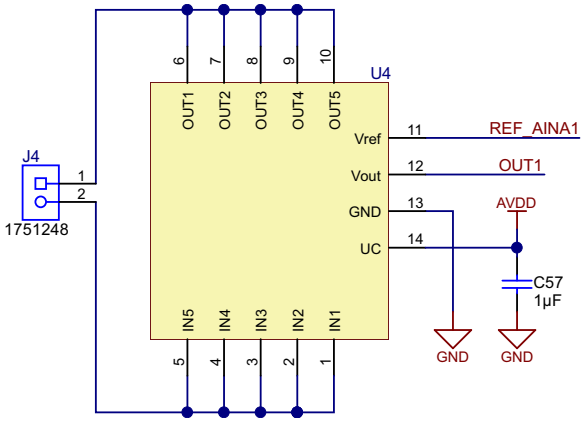


Figure 7. CKSR 6-NP With Capacitor Decoupling on Supply Pin

8.2 Designing the ADC Input Stage

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called aliasing. Therefore, an analog anti-aliasing filter must remove the harmonic content from the input signal before being sampled by the ADC. An anti-aliasing filter is designed as a low-pass RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. A high-bandwidth filter is required to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For AC signals, the filter bandwidth should be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system. The datasheet of ADS7254 suggests the component values for anti-aliasing filter as shown in Figure 8:

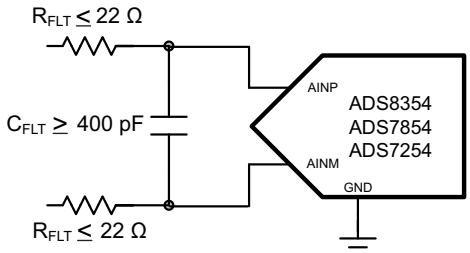


Figure 8. Anti-Aliasing Filter for ADS7x54

The cut-off frequency of anti-aliasing filter is calculated using Equation 2:

$$f_{-3db} = \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \quad (2)$$

Designing the input stage is a two-step optimization process:

1. Select a noise rejection input capacitor that charges the sample-hold capacitor (C_{SH}).
2. Identify an op-amp that can consume low power and recharge the input capacitor.

A filter capacitor, C_{FLT}, which connects across the ADC inputs and filters the noise from the front-end drive circuitry, reduces the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. The noise reduction filter block consists of a differential capacitor, C_{FLT}, which is added between the two input pins as shown in Figure 9. This block helps minimize noise by attenuating the kick-back noise from the ADC and also by band-limiting the broadband noise of the op-amp.

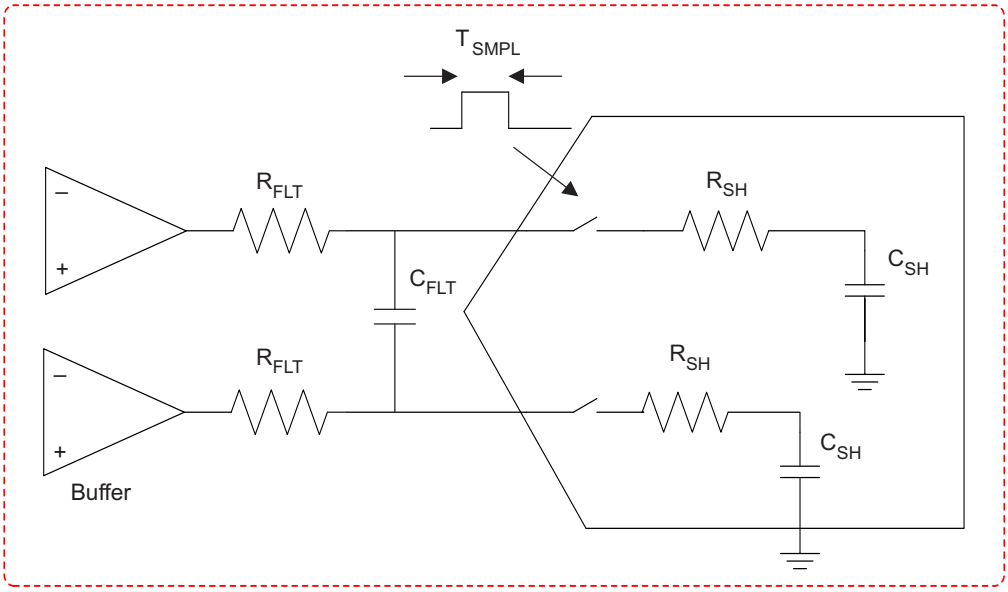


Figure 9. Input Capacitor C_{FLT} for Attenuating Noise

This filter capacitor acts as a charge reservoir by providing the charges to C_{SH} during acquisition time. The op-amp delivers charges to the capacitor to bring it up to the input voltage *V* as shown in Figure 10. This capacitor must be large enough to charge or discharge the sample-hold capacitor during acquisition time and retain 95% of its initial voltage.

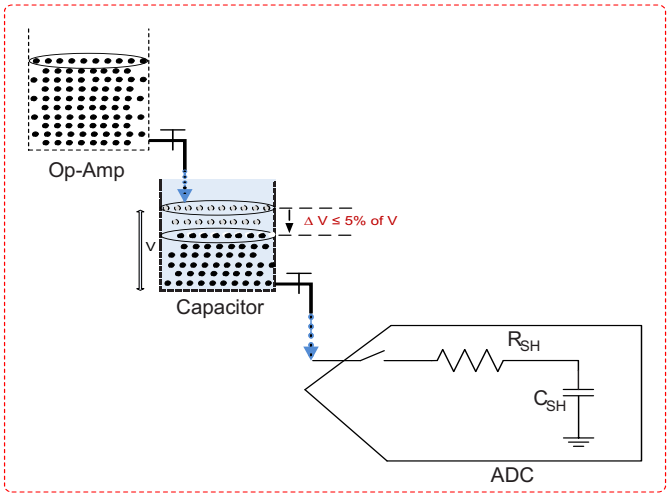


Figure 10. Filter Capacitor Delivering Charges to C_{SH}

The sampling capacitor inside ADS7x54 has a typical value of 40 pF. When the input is at its maximum, C_{SH} has to be charged to 2xVREF during the sampling time. The corresponding charge needed is approximately 200 pC (40 pF × 5 V). While delivering 200 pC to C_{SH}, the voltage across this capacitor should not drop below 5% of its initial voltage, which is VREF to keep the op-amp in its linear operating region (no slew).

As a rule of thumb, the value of this capacitor should be at least 20 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Therefore, the value of C_{FLT} should be greater than 800 pF. Note that driving capacitive loads can degrade the phase margin of the input amplifiers, which makes the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For these devices, TI recommends limiting the value of R_{FLT} to a maximum of 22 Ω to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1%.

TIDA-00201 uses C_{FLT} = 0.01 µF and R_{FLT} = 10 Ω, with the cut-off frequency of 795.77 kHz.

The flicker and broadband noise introduced by the op-amp (or FDA) can be verified using Equation 3:

$$OPA_{Broadband\_RMS\_Noise} = OPA_{Broadband\_RMS\_Density} \times \sqrt{\frac{\pi}{2} \times \left(\frac{1}{2\pi R_{FLT} C_{FLT}} - 10\,Hz \right)} \quad (3)$$

8.3 Designing the FDA Stage

Figure 11 shows the THS4531 section. As mentioned earlier, TIDA-00201 has four sensors on board, which means four THS4531 devices are used for each of the sensors.

Important observations from Figure 11 include:

1. Single supply operation: THS4531 is powered through 5 V coming out of TPS7A4700 (as explained in Section 8.6). One bypass capacitor with a value of 0.1 µF is placed very close to the AVDD pin of THS4531.
2. VOCM pin: This pin is supplied with 2.5 V (coming from VREF_BUF or Sensor REF output) in case the pin interfaces with the external ADC. But when the internal ADC of the Delfino control card is used, the common-mode voltage needs to be 1.25 V. In that case, the VOCM pin of THS4531 is supplied through the 1.25 V coming from REF2025 REF/2.
3. Input signal filtering: The fluxgate sensors have an inherent noise due to their internal structure. Both inputs of THS4531 use a low-pass filter. The design of filters is explained in Section 8.4.
4. Selection of gain:
   - When used with the external ADC, the output can have a common-mode voltage of 2.5 V and the full-scale range of the ADC can be 5 V. The fluxgate sensors can work up to 300% of their nominal current range, which means the signal must have a gain to go from 1.875 to 2.5 V at 300% of the operating current. This signal gives a gain of 1.33.
   - When used with internal ADC of controller, the output can have a common-mode voltage of 1.25 V and the full-scale range of the ADC can be 3.3 V. The fluxgate sensors can work up to 300% of their nominal current range, which means the signal must have a gain to go from 1.875 to 1.65 V at 300% of the operating current. This signal gives a gain of 0.88. If the current measurement requirement is only up to 200% or 250%, a gain of 1 can be used.
5. Selection of components: The 1-nF caps in the dual feedback helps in reducing overall noise of the system. Note that the resistors on both inverting and non-inverting inputs must match tightly so as not to unbalance the current. The components used in this design have a 0.5% tolerance. The effect of passive component mismatch can be simulated to estimate the statistical error incurred from the offset and gain mismatch between channels using the Monte Carlo simulation method.

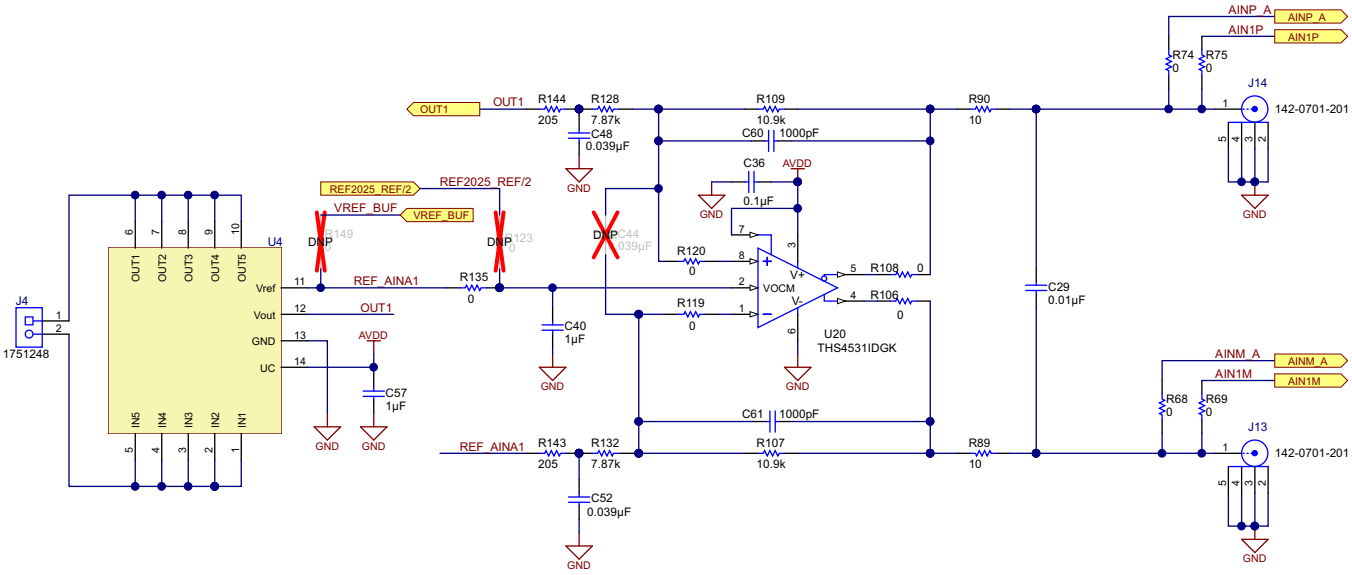


Figure 11. THS4531 FDA Interface Between Sensor and ADC

8.4 Noise Filtering for Fluxgate Current Sensors

Fluxgates have an inherent noise (450 kHz / 900 kHz) at their output that needs filtering. A low-pass filter is designed with a cut-off frequency of 20 kHz using TI's FilterPro™ software as shown in Figure 12.

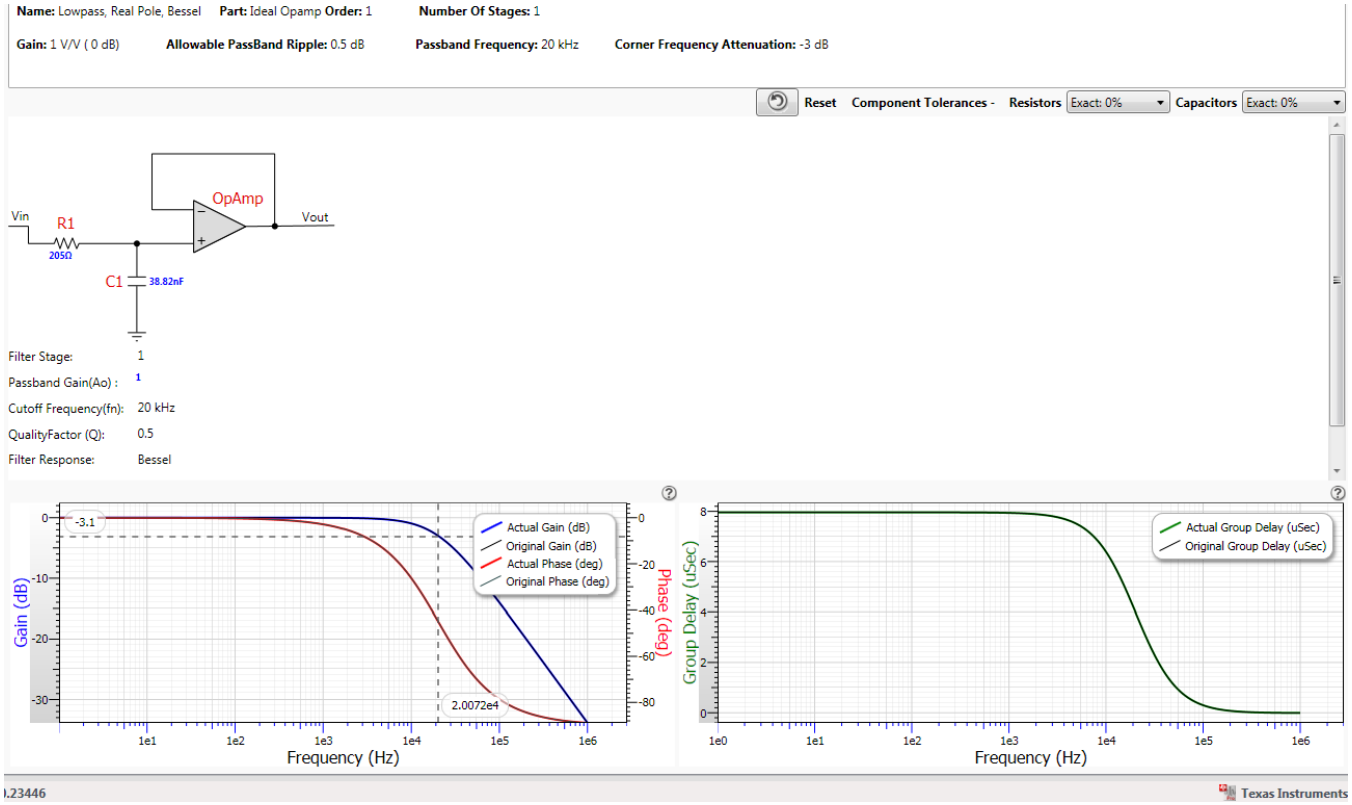


Figure 12. Low-Pass Filter Design Simulation Using FilterPro

8.5 Designing the Reference Circuit for ADC

An ADC is as good as its reference because ADCs compare an input to a known reference and its binary scaled weights to estimate an equivalent digital code. An accurate digital conversion of the input signal requires a highly accurate, low-drift, low-noise reference. The reference should also support the dynamic charge requirements without affecting the noise and linearity performance of the device. An ideal ADC is one that gives the same digital code for a given input. For a capacitor-based ADC reference input, the load at the reference pin spikes out every time a bit value is estimated. Not only does reference current transient multiple times within a conversion cycle, but also the magnitude of the transient current vary between the conversions. A noisy reference shows up as a variation of code out at the output of the ADC for a fixed input. A noisy reference also degrades the linearity, THD, and SNR.

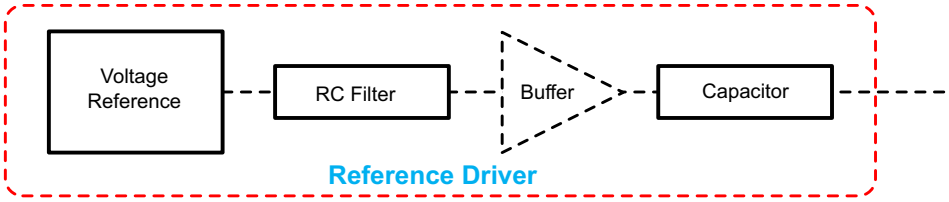


Figure 13. Reference Driver Circuit

As shown in Figure 13, designing the reference drive circuitry is a four-step optimization process that involves

1. identifying a reference that is suitable for the application
2. designing a filter that limits the broadband noise from the reference
3. estimating the capacitor value needed to provide the reference drive current
4. identifying an op-amp that is suitable for low power that can recharge the capacitor

There are two types of noise that a reference can introduce: flicker noise and broadband noise. Flicker noise is the noise dominant at low frequencies and broadband noise dominates at high frequencies. The broadband noise, in particular, can be of the order of hundreds of microvolts and can easily exceed the tens of microvolts of RMS noise of the converter. Typically, flicker noise is specified on the datasheet as peak-to-peak noise up to 10 Hz. This noise has to be scaled down by a factor of 6.6 to convert it into RMS noise. On the other hand, the density of broadband spectral noise may not be specified on the datasheet. For a band-gap reference, the density is 0.1 $\mu V_{RMS}/\sqrt{Hz}$ to 10 $\mu V_{RMS}/\sqrt{Hz}$ in magnitude and is inversely proportional to the square root of the quiescent current of the reference. If the reference is not specified, Equation 4 gives a good approximation:

$$REF_{Broadband\_Noise\_Density} = \frac{10{,}000\ nV}{\sqrt{Hz}} \times \frac{\sqrt{\mu A}}{\sqrt{2 \times IQ\_REF\,(in\ \mu A)}} \quad (4)$$

As seen from Figure 14, noise and power are inversely related. A reference with low IQ inherently comes with higher noise.

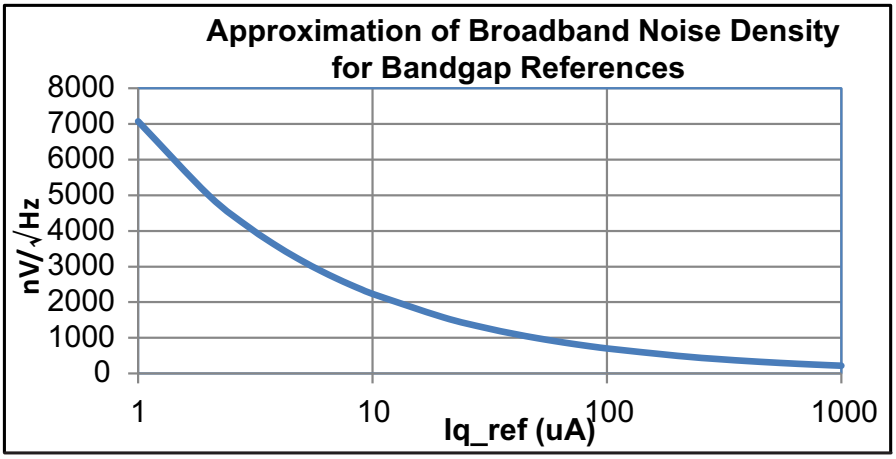


Figure 14. Broadband Noise versus Reference Quiescent Current

For REF5025, I_{Q_REF} = 800 µA, which gives the broadband noise a density equal to 250 nV/√Hz using Figure 14.

Buffer

An op-amp is needed to recharge the capacitor above. Additional noise introduced by the buffer should be minimized while selecting this op-amp. However, this selection is less of a concern because unlike references where output noise density is a few μV/√Hz, the same will be in the range of 10 nV/√Hz to 100 nV/√Hz for op-amps. The broadband noise gets further band-limited by the isolation resistor and the capacitor following the buffer. Flicker and broadband noise introduced by the op-amp should be verified for it to be significantly smaller (less than one-third) than the reference noise before finalizing on the op-amp. Reducing the buffer noise to less than a third of the reference noise makes the op-amp noise term insignificant when it gets added to the reference noise (square root of summation of squares). Flicker noise is specified on the datasheet as peak-to-peak noise up to 10 Hz. This noise has to be scaled down by a factor of 6.6 to convert it into RMS noise. The total noise introduced by the op-amp is the square root of the sum of the squares of the flicker noise and broadband RMS noise. Equation 3 can be used to verify the same.

Note that high resolution converters cause the size of the capacitor in the charge bucket to become too large, causing stability issues in most of the op-amps. This issue can be addressed with a series isolation resistor at the cost of the bandwidth of the op-amp. Choosing the right capacitor, op-amp, and isolation resistor is an iterative process that has to be verified by simulation. During this process the capacitance might require minimal adjustments from the starting value taking stability, voltage drop, and cutoff frequency into consideration.

Reference for External ADC: REF5025 + OPA322

The REF5025 is used as a 2.5-V voltage reference device. Use a supply bypass capacitor ranging between 1 to 10 μF. The REF5025 allows access to the band-gap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND in combination with the internal resistors creates a low-pass filter. A capacitance of 1 μF creates a low-pass filter with the corner frequency between 10 and 20 Hz. This filter decreases the overall noise measured on the V_{OUT} pin by half. A higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Note that use of this capacitor increases startup time. Figure 15 shows schematic capture of REF5025 and the OPA322-based buffer connected at the output of the REF5025 so as to recharge the capacitor at the output.

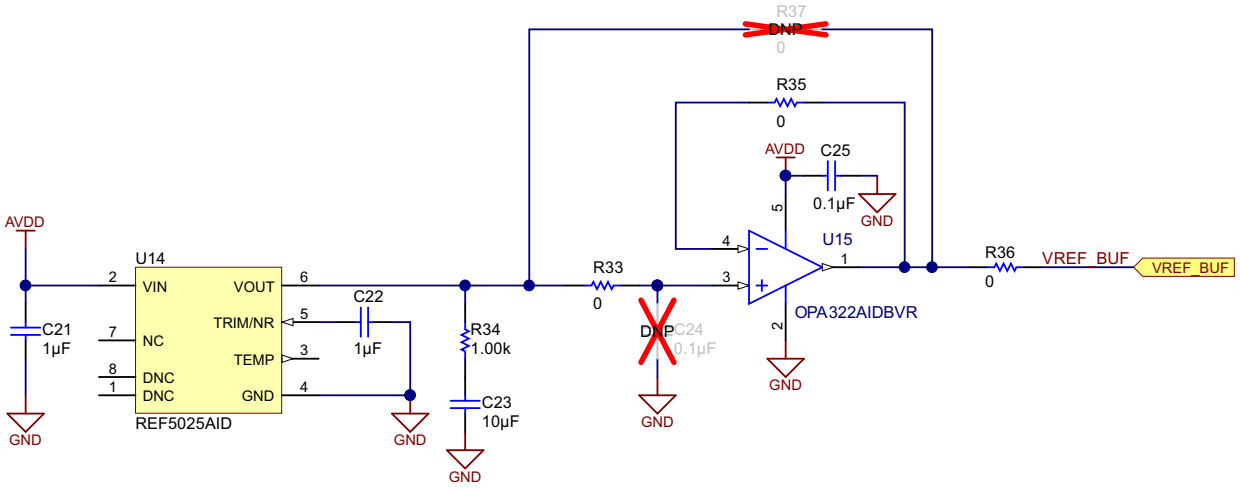


Figure 15. REF5025 + OPA322 Circuit

Reference for Internal ADC of Delfino F2837x: REF2025

The REF2025 can provide two reference voltages, 1.25 V and 2.5 V. The 2.5 V is given as reference to the integrated ADC, and 1.25 V is used as output common-mode voltage for the THS4531. Figure 16 shows the reference circuit using the REF2025.

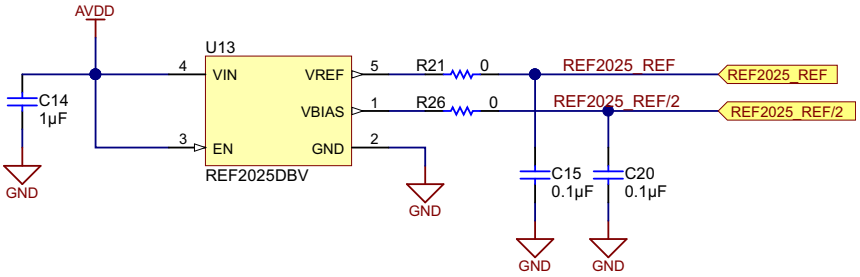


Figure 16. REF2025 Circuit to Provide 1.25 V and 2.5 V as Reference

8.6 Power Supply: 5-V and 3.3-V Generation

The TIDA-00201 board can be powered through connector J6. The input voltage can be 6 V, 15 V, or 24 V based on the availability in the industrial drive. The output voltage for the TPS7A4700 is set by grounding the appropriate control pins. When grounded, all control pins add a specific voltage on top of the internal reference voltage (V_{REF} = 1.4 V). For example, when grounding pins 0P4V and 3P2V, the voltage values 0.4 V and 3.2 V are added to the 1.4-V internal reference voltage for $V_{OUT(NOM)}$ equal to 5.0 V. Figure 17 shows the TPS7A4700 section of the design. One green LED (LD1) is provided to indicate availability of the 5-V output.

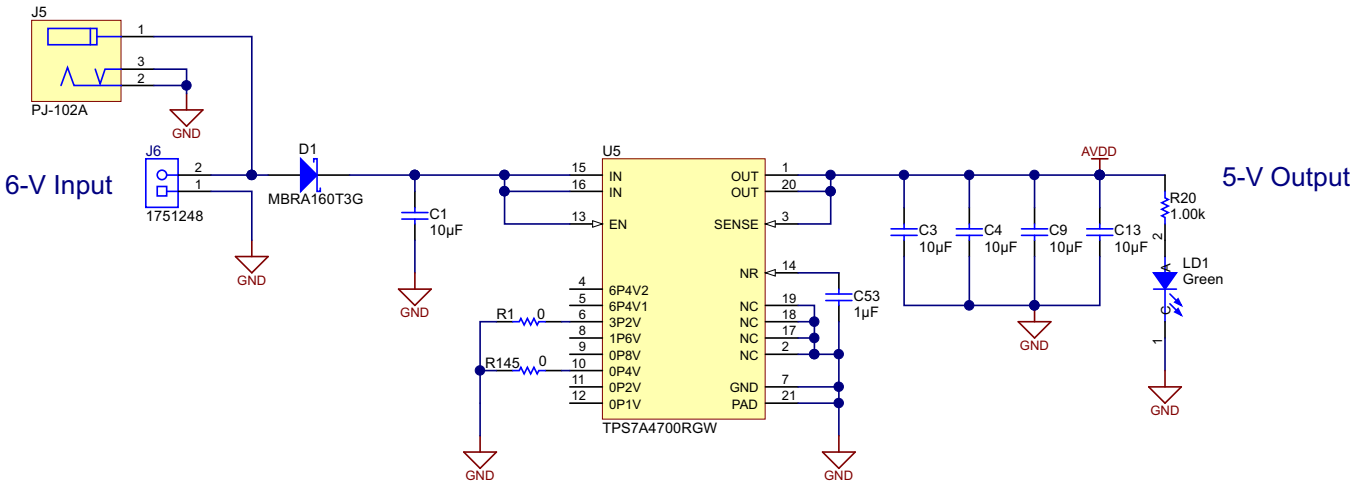


Figure 17. 6-V to 5-V Conversion Using TPS7A4700

TLV70033 converts the 5 V to 3.3 V. Figure 18 shows the schematic for the same.

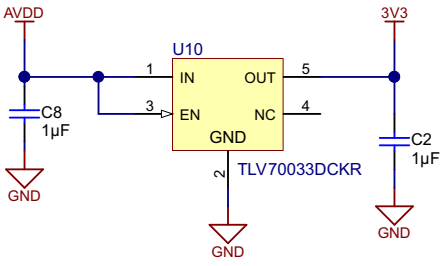


Figure 18. 5-V to 3.3-V Conversion Using TLV70033

8.7 Design for Overcurrent and Earth Fault Detection Circuits

Generally, the fluxgate sensors can be operated up to 300% of their nominal current ratings for a shorter duration. If the current goes beyond 300%, enable the protection mechanism. For example, in this design, the thresholds are calculated as follows:

- Nominal current rating (In) = 6 Amperes
  Corresponding fluxgate sensor output voltage = 0.625 Volts
- 300% of the nominal rating = 18 Amperes
  Corresponding fluxgate sensor output voltage at 300% current = 0.625 × 3 = 1.875 Volts

The output of fluxgate sensor always rides on 2.5 V, so the positive and negative values can go up to 4.375 V and 0.625 V, respectively. Considering 50 mV as a buffer, the thresholds are calculated as:

- Threshold for positive cycle = VTH (pos) = 2.5 V + 1.875 V + 0.05 V = 4.38 Volts
- Threshold for negative cycle = VTH (neg) = 2.5 V – 1.875 V – 0.05 V = 0.62 Volts

8.7.1 Overcurrent Protection

The overcurrent protection is implemented as shown in Figure 19. The resistor dividers are calculated for VTH (pos) = 4.38 V and VTH (neg) = 0.62 V. Each channel has individual overcurrent protection. The indication of the overcurrent's condition is shown with an LED at the output.

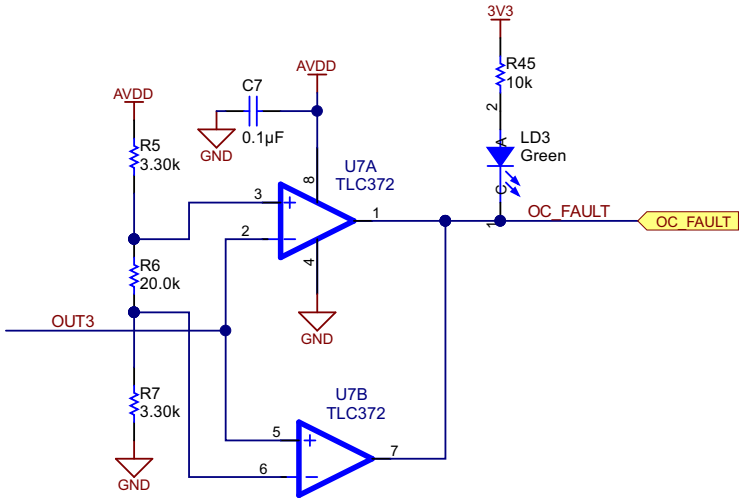


Figure 19. Overcurrent Protection Using TLC372

8.7.2 Earth Fault Protection

The earth fault protection is implemented as shown in Figure 20. The resistor dividers are calculated for VTH (pos) = 4.38 V and VTH (neg) = 0.62 V. The signals coming out from each channel are summed together with resistors. The indication of the overcurrent's condition is shown with an LED at the output. Both OC_FAULT and GND_FAULT are available on connector J17.

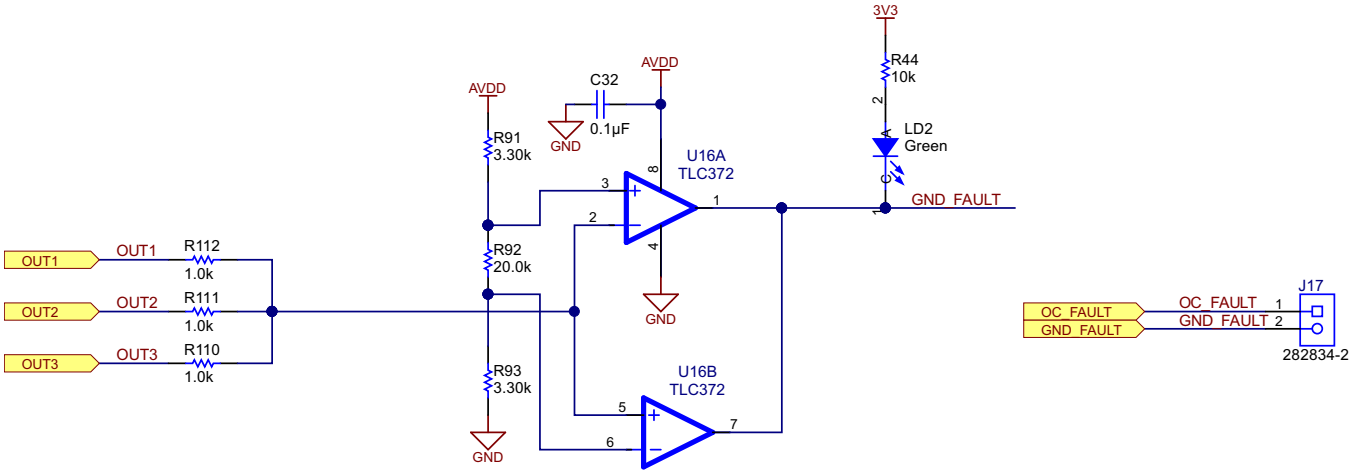


Figure 20. Earth Fault Protection Using TLC372

8.8 Connections to Onboard External ADCs: ADS7854

The ADS7854 belongs to a family of pin-compatible, dual, high-speed, simultaneous-sampling, ADCs that support fully-differential analog inputs. Each device includes two individually programmable reference sources that can be used for system-level gain calibration. Also, a flexible serial interface that can operate over a wide power-supply range enables easy communication with a large variety of host controllers. The interface is fully specified over the extended industrial temperature range (–40°C to 125°C). Figure 21 shows the schematic for the two ADS7854 devices available on board. The SPI outputs are available on a connector to interface with external motor controller (as shown in Figure 22).

Reference: Both ADCs can use either their internal references or an external reference coming from the REF5025 (VREF_BUF).

Power supply: Both ADCs are powered at AVDD with a 5-V supply voltage coming from the TPS7A4700 with a decoupling cap of 10 µF placed very close to the device. The DVDD supply is given from 3.3 V coming from the TLV70033. DVDD also has a decoupling capacitor of 10 µF placed very close to the device.

Simultaneous sampling of all four ADCs: All four ADCs can sample the input signals simultaneously by connecting the /CS pins together and giving one single /CS signal to the ADCs.

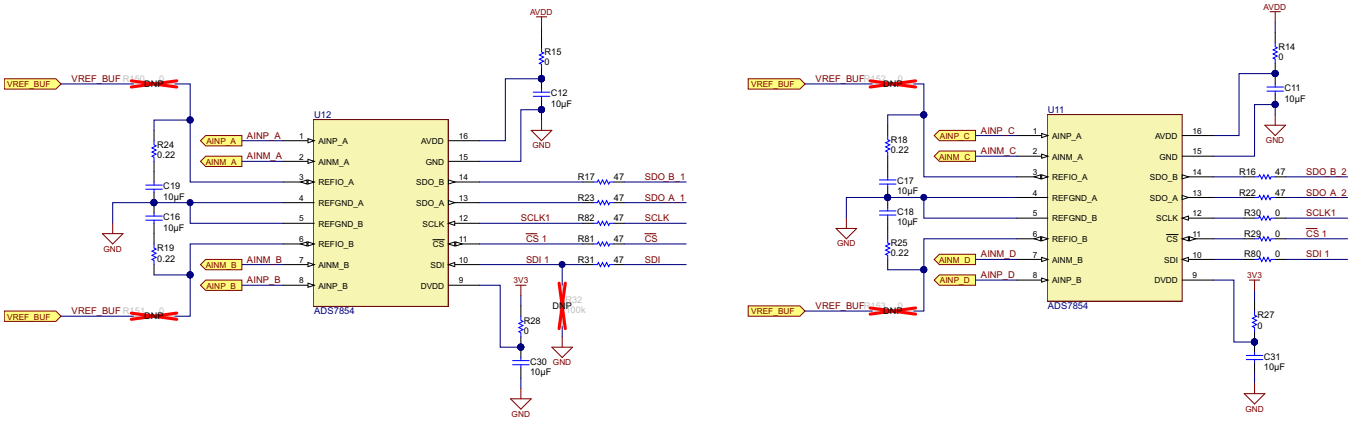


Figure 21. ADS7854 Circuit

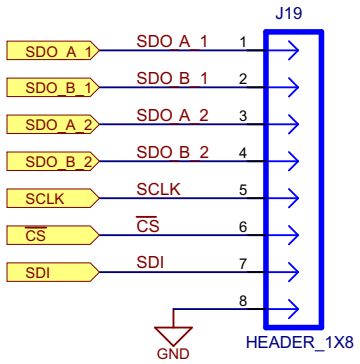


Figure 22. SPI Signals of External ADCs Taken Out on a Connector

8.9 Connections to Delfino F2837x Control Card

The Delfino F28377D Control Card (TMDSCNCD28377D) from TI provides a great way to learn and experiment with the F2837x device family within TI's C2000™ family of microcontrollers (MCUs). This 180-pin control card is intended to provide a well-filtered robust design capable of working in most industrial environments.

The F28377D Control Card features:

- Delfino F28377D MCU: A high performance C2000 MCU
- 180-pin HSEC8 edge card interface: Allows for compatibility with all of C2000's 180-pin control card application kits and control cards. Compatibility with 100-pin control cards can be accomplished using the TMDSADAP180TO100 adapter card (sold separately)
- Built-in isolated JTAG emulation: An XDS100v2 emulator that provides a convenient interface to Code Composer Studio (CCS) without additional hardware. Flipping a switch allows an external JTAG emulator to be used
- Connectivity: Contains connectors that allow the user to experiment with USB, a microSD card, and isolated UART/SCI with the F2837x MCU
- Key signal breakout: Most GPIOs, ADCs, and other key signals routed to hard gold connector fingers
- Robust power supply filtering: A single 5-V input supply that powers an on-CARD 3.3-V LDO. All MCU inputs are then decoupled using LC filters near the device
- ADC clamping: ADC inputs clamped by protection diodes

An image of the control card is shown in Figure 23:

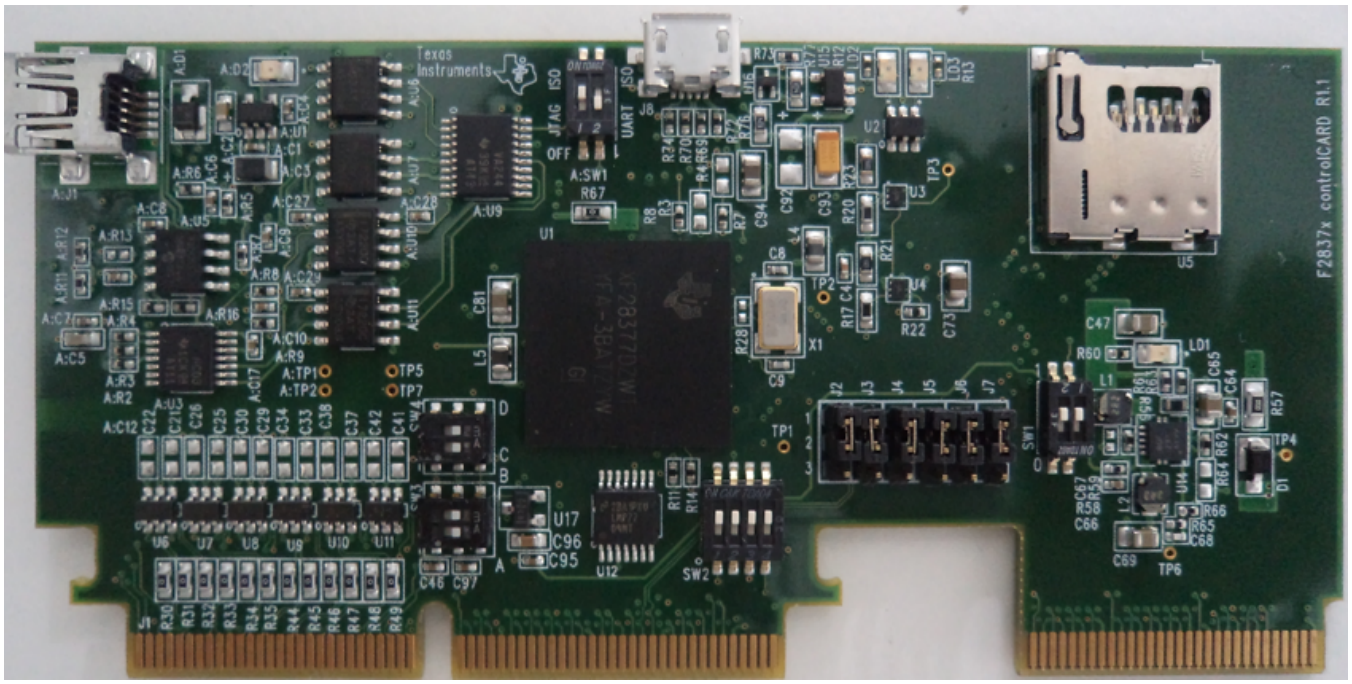


Figure 23. Image of Delfino F2837x Control Card

Figure 24 shows the pin-mapping for the 180-pin connector available on the Delfino F2837x Control Card. The signals are routed as shown in Table 6.

Date:				cCARD Pinout:		F28377D (180pin)				HSEC Pinout:
7-May-2014										2.10
		HSEC pin	MCU pin	HSEC function		HSEC function	MCU pin	HSEC pin		
		1	GPIO-71 **	JTAG-EMU1		JTAG-EMU0	GPIO-70 **	2		
		3	TMS	JTAG-TMS		JTAG-TRSTn	TRSTn	4		
		5	TCK	JTAG-TCK		JTAG-TDO	TDO	6		
		7		GND		JTAG-TDI	TDI	8		
		9	ADC-A0, DAC	ADC1 (and/or DACA)		GND		10		
		11	ADC-A1, DAC	ADC1 (and/or DACB)		ADC2	ADC-B0	12		
		13		Rsvd		ADC2	ADC-B1	14		
		15	ADC-A2, COMP+	ADC1 (and/or CMPIN+)		Rsvd		16		
		17	ADC-A3	ADC1		ADC2	ADC-B2, COMP+	18		
		19		GND		ADC2	ADC-B3	20		
		21	ADC-A4, COMP+	ADC1 (and/or CMPIN+)		GND		22		
		23	ADC-A5	ADC1		ADC2	ADC-B4, COMP+	24		
		25	ADCIN14, COMP+	ADC (and/or CMPIN+)		ADC2	ADC-B5	26		
		27	ADCIN15	ADC		ADC	ADC-D0, COMP+	28		
		29		Rsvd		ADC	ADC-D1	30		
		31	ADC-C2, COMP+	ADC		Rsvd		32		
		33	ADC-C3	ADC		ADC	ADC-D2, COMP+	34		
		35		GND		ADC	ADC-D3	36		
		37	ADC-C4	ADC		GND		38		
		39	ADC-C5	ADC		ADC	ADC-D4	40		
		41		Rsv		ADC	ADC-D5	42		
		43		A-GND (VREFLO on certain MCU)		Rsv		44		
		45	All VREFHIs *	Rsv (VREFHI on certain MCU)		GND		46		
		47		GND		5V0		48		
		49	GPIO-00	PWM1A		PWM3A	GPIO-04	50		
		51	GPIO-01	PWM1B		PWM3B	GPIO-05	52		
		53	GPIO-02	PWM2A		PWM4A	GPIO-06	54		
		55	GPIO-03	PWM2B		PWM4B	GPIO-07	56		
		57	GPIO-08	PWM5A		PWM7A or TZ1	GPIO-12	58		
		59	GPIO-09	PWM5B		PWM7B or TZ2	GPIO-13	60		
		61	GPIO-10	PWM6A		PWM8A or TZ3	GPIO-14	62		
		63	GPIO-11	PWM6B		PWM8B or TZ1/4	GPIO-15	64		
		65		GND		12V0?		66		
		67	GPIO-16	SPISIMOA		QEP1A (McBSP-MDXA)	GPIO-20	68		
		69	GPIO-17	SPISOMIA		QEP1B (McBSP-MDRA)	GPIO-21	70		
		71	GPIO-18	SPICLKA		QEP1S (McBSP-MFSXA)	GPIO-22	72		
		73	GPIO-19	SPISTEA		QEP1I (McBSP-MCLKXA)	GPIO-23	74		
		75	GPIO-24	ECAP1 or SPISIMOB		SCIRXA	GPIO-28	76		
		77	GPIO-25	ECAP2 or SPISOMIB		SCITXA	GPIO-29	78		
		79	GPIO-26	ECAP3 or SPICLKB		CANRXA	GPIO-30	80		
		81	GPIO-27	ECAP4 or SPISTEB		CANTXA	GPIO-31	82		
		83		GND		5V0		84		
		85	GPIO-32	I2CSDAA		GPIO	GPIO-34	86		
		87	GPIO-33	I2CSCLA		GPIO	GPIO-39	88		
		89	GPIO-40	GPIO		GPIO	GPIO-44	90		
		91	GPIO-41	GPIO		GPIO	GPIO-45	92		
		93	GPIO-42 ***	GPIO		GPIO	GPIO-46 ***	94		
		95	GPIO-43 ***	GPIO		GPIO	GPIO-47 ***	96		
		97		GND		5V0		98		
		99	GPIO-48	GPIO		QEP2A or GPIO	GPIO-54	100		
		101	GPIO-49	GPIO		QEP2B or GPIO	GPIO-55	102		
		103	GPIO-50	GPIO		QEP2S or GPIO	GPIO-56	104		
		105	GPIO-51	GPIO		QEP2I or GPIO	GPIO-57	106		
		107	GPIO-52	GPIO		GPIO (McBSP-MCLKRA)	GPIO-58	108		
		109	GPIO-53	GPIO		GPIO (McBSP-MFSRA)	GPIO-59	110		
		111		GND		5V0		112		
		113		Rsv		Rsv		114		
		115		Rsv		Rsv		116		
		117		Rsv		Rsv		118		
		119		Rsv		Device Reset (Active low)	XRSn	120		
		121	GPIO-35	GPIO		GPIO	GPIO-36	122		
		123	GPIO-37	GPIO		GPIO	GPIO-38	124		
		125	GPIO-60	GPIO		GPIO	GPIO-61	126		
		127	GPIO-62	GPIO		GPIO	GPIO-63	128		
		129	GPIO-64	GPIO		GPIO	GPIO-65	130		
		131	GPIO-66	GPIO		GPIO	GPIO-67	132		
		133	GPIO-68	GPIO		GPIO	GPIO-69	134		
		135		GND		12V0?		136		
		137	GPIO-70	GPIO		GPIO	GPIO-71	138		
		139	GPIO-72	GPIO		GPIO	GPIO-73	140		
		141	GPIO-74	GPIO		GPIO	GPIO-75	142		
		143	GPIO-76	GPIO		GPIO	GPIO-77	144		
		145	GPIO-78	GPIO		GPIO	GPIO-79	146		
		147	GPIO-80	GPIO		GPIO	GPIO-81	148		
		149	GPIO-82	GPIO		GPIO	GPIO-83	150		
		151	GPIO-84	GPIO		GPIO	GPIO-85	152		
		153	GPIO-86	GPIO		GPIO	GPIO-87	154		
		155	GPIO-88	GPIO		GPIO	GPIO-89	156		
		157		GND		5V0		158		
		159	GPIO-90	GPIO		GPIO	GPIO-91	160		
		161	GPIO-92	GPIO		GPIO	GPIO-93	162		
		163	GPIO-94	GPIO		GPIO	GPIO-133	164		
		165	GPIO-120 ***	GPIO		GPIO	GPIO-121 ***	166		
		167	GPIO-161	GPIO		GPIO	GPIO-162	168		
		169	GPIO-163	GPIO		GPIO	GPIO-164	170		
		171		Rsv		Rsv		172		
		173		Rsv		Rsv		174		
		175		Rsv		Rsv		176		
		177		Rsv		12V0?		178		
		179		GND		5V0		180		

Analog (HSEC pin 9 – 45)

Analog (HSEC pin 10 – 46)

Digital (HSEC pin 49 – 119)

Digital (HSEC pin 50 – 120)

* Switches may be altered to connect VREFHIs to the HSEC connector

** 0ohm resistors can be removed in order to tie GPIO-70 and 71 to EMU0 and EMU1

*** Can be dedicated to on-card USB or brought through the connector via jumpers on the cCARD

Figure 24. Pin-Mapping on Delfino F2837x Control Card (180-Pin Connector)

Table 6. Pin-Mapping Details

PIN NUMBER ON CONTROL CARD	PIN FUNCTIONALITY	MAPPING ON TIDA-00201 BOARD (J15 AND J16)
7, 10, 19, 22, 35, 46, 97, 111, 160, 161	GND	GND
15	ADC-A2, COMP+	AIN2P
17	ADC-A3	AIN2M
18	ADC-B2, COMP+	AIN1M
20	ADC-B3	AIN1P
21	ADC-A4, COMP+	AIN3P
23	ADC-A5	AIN3M
25	ADCIN14, COMP+	AIN4P
27	ADCIN15	AIN4M
39	ADC-C5	REF2025 REF/2
45	All VREFHIs	REF2025 REF
67, 77	SPISIMOA, SPISOMIB	SDI for onboard ADS7854
69, 75	SPISOMIA, SPISIMOB	SDOA and SDOB from onboard ADS7854
71, 79	SPICLKA	SCLK for onboard ADS7854
89	GPIO	/CS for onboard ADS7854
112, 180	AVDD	AVDD (5 V)

Figure 25 shows the schematic capture for the pin-mapping explained in Table 6. Although the control card has clamping diodes at each of the analog inputs, this design provides an option to mount external clamping diodes as well.

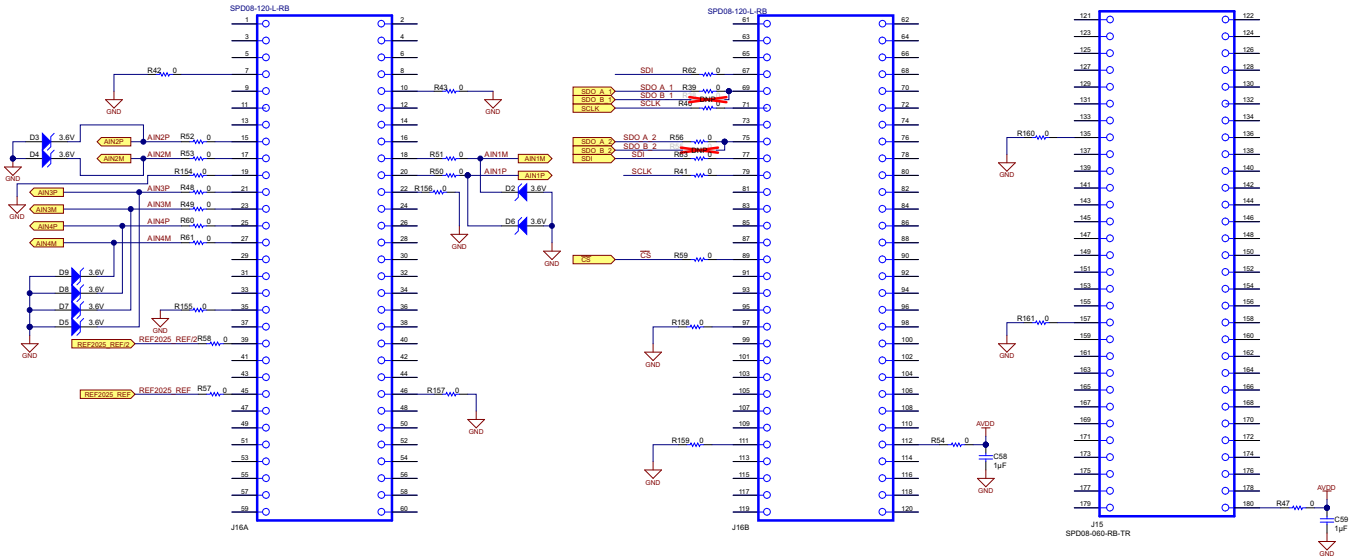


Figure 25. Schematic Capture for J15 and J16 (to Connect to 180-Pin Connector on Control Card)

9 Test Setup and Test Results

9.1 Noise Filtering for Fluxgate Current Sensor

As explained in Section 8.4, low-pass filters are used to filter out the 450-kHz / 900-kHz noise signal from fluxgate sensors. Figure 26 shows the waveforms before and after the filter. The noise signal on OUT pin of the fluxgate sensor is having frequency of 452.1 kHz, which is same as the internal fluxgate oscillator frequency.

NOTE: The signals captured in Figure 26 also include noise from the oscilloscope itself.

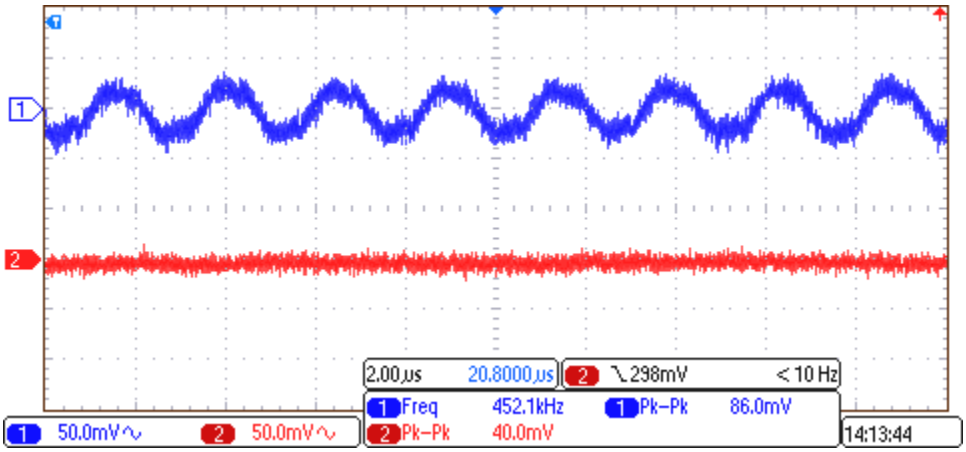


Figure 26. Noise Signal Before and After the Low-Pass Filter

9.2 DC (or Dynamic) Performance of the System Using External ADC ADS7254

All ADC circuits suffer from some amount of inherent broadband noise contributed by the internal resistors, capacitors, and other circuitry, which is referred to the inputs of the ADC. The front-end driver circuit also contributes some noise to the system, which can also be referred to the ADC inputs. The cumulative noise, often called as the input-referred noise of the ADC, has a significant impact on the overall system performance. The most common way to characterize this noise is by using a constant DC voltage as the input signal and collecting a large number of ADC output codes. A histogram can then be plotted to show the distribution of output codes, which can be used to illustrate the impact of noise on the overall system performance. For a theoretically perfect ADC system, the histogram of output codes is a single vertical bar because the ADC output is always the same for a DC input voltage. However, the noise contributions from the ADC and the front-end circuit lead to a distribution of output codes, which provides a measure of the overall system's DC noise. If the output code distribution has large peaks and valleys that make it distinctly non- Gaussian, then the histogram indicates significant DNL errors in the ADC or issues with the system design such as insufficient power supply decoupling, improper ground connections, or other poor PCB layout effects.

The noise-free resolution of an ADC is defined as the number of steady output bits from the converter beyond. The system performance is dominated by noise, and it is not possible to differentiate between individual code transitions. This resolution is an extremely conservative measurement of the ADC's performance because the formula for noise-free resolution is derived from the peak-to-peak code noise, which is extremely dependent on the total number of samples. Do not confuse the effective noise-free resolution and effective number of bits (ENOB) with each other as they are two completely different entities. The ENOB for an ADC is measured with an AC sinusoidal input signal and includes the effects due to quantization noise and distortion terms, which have no impact on a DC measurement.

Figure 27 and Figure 28 show the histogram, noise-free resolution, and the captured data for this design. With a 3-A DC current passing through the fluxgate sensor, the noise-free resolution is 11.55 bits for Channel A and 11.70 bits for Channel B.

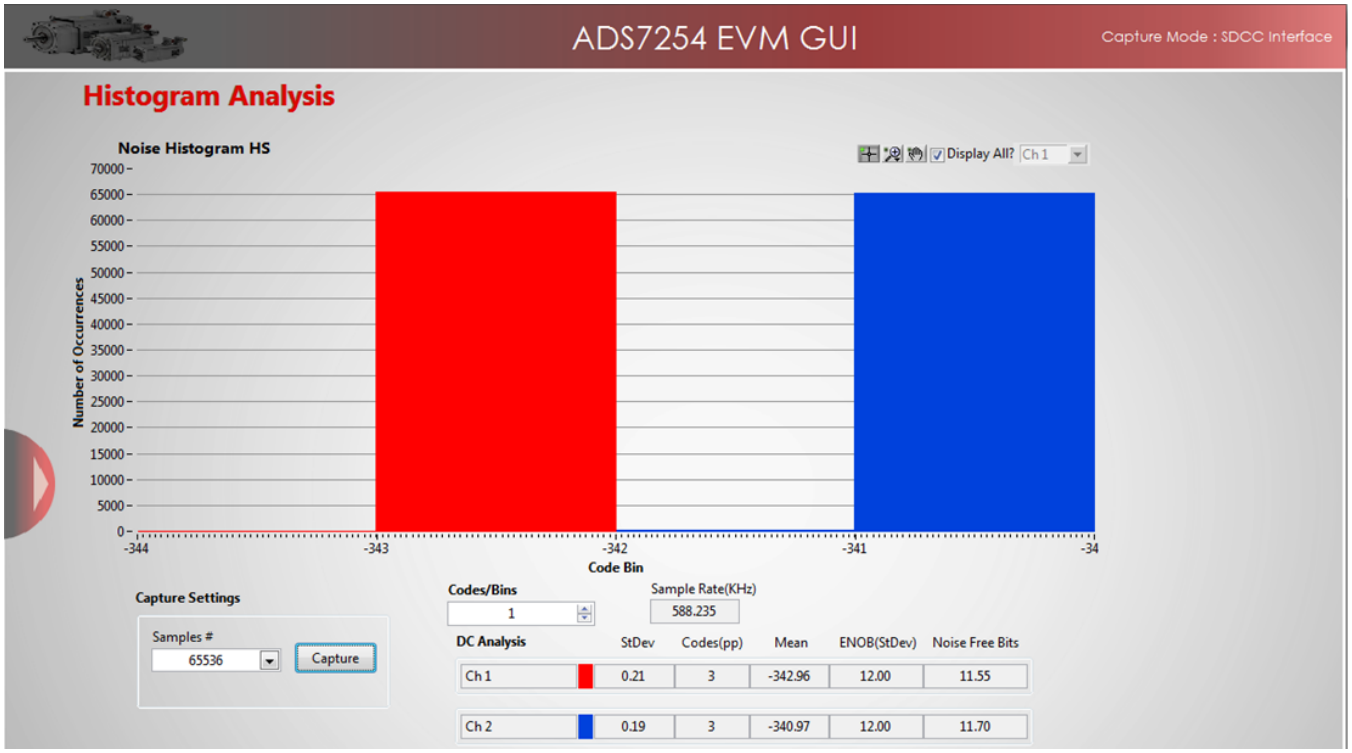


Figure 27. Histogram of Captures for Two Channels Using ADS7254 EVM GUI

Figure 28. Data Capture for Two Channels Using ADS7254 EVM GUI

9.3 AC (or Static) Performance of the System Using External ADC ADS7254

For any data acquisition system, an important focus is to achieve excellent dynamic performance while minimizing the total power consumption of the system. The main AC specifications to consider are THD, SNR, SINAD, and ENOB. Essentially, these parameters are different ways of quantifying the noise and distortion performance of an ADC based on a fast Fourier transform (FFT) analysis. A typical FFT plot for an ADC is shown in Figure 29.

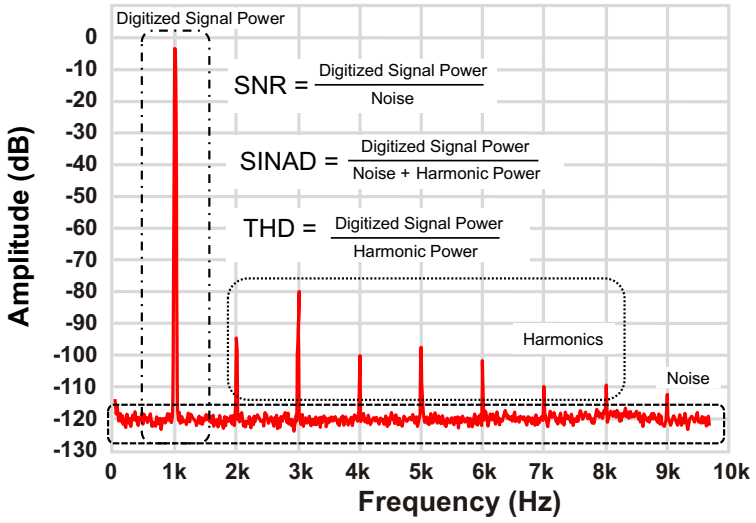


Figure 29. Typical FFT Plot Showing Different Dynamic Parameters

The SNR provides insight into the total noise of the system. The total noise of the data acquisition system is the RSS of the front-end amplifier noise ($V_{n\_AMP\_RMS}$) and the ADC noise ($V_{n\_ADC\_RMS}$). The ADC noise includes the quantization noise as well as the noise contributed by the ADC internal circuitry, or the input-referred noise of the ADC. The total noise contributions from all these sources, denoted as $V_{n\_TOT\_RMS}$, are referred to the input of the ADC to calculate the total SNR of the system (SNR_{SYS}).

$$V_{n\_TOT\_RMS} = \sqrt{V_{n\_AMP\_RMS}^2 + V_{n\_ADC\_RMS}^2}$$

$$SNR_{SYS} = \frac{V_{SIG\_RMS}}{V_{n\_TOT\_RMS}} \quad (5)$$

ENOB is an effective measurement of the quality of a digitized signal from an ADC by specifying the number of bits above the noise floor. For an ideal N-bit ADC with only quantization noise, the SNR (in dB) can be calculated as:

$$SNR = 6.02 \times N + 1.76$$

$$N = \frac{SNR - 1.76}{6.02} \quad (6)$$

While ENOB provides a good summary of the ADC dynamic performance, it does not describe the converter's entire performance over the operating frequency ranges and input signals. Additionally, ENOB does not include the ADC DC specifications such as offset and gain error. Therefore, pay attention to other converter specifications as well depending on the application using the ADC.

For an AC current of 4.5 V_{RMS} at a frequency of 50 Hz, the conditioned voltage signal (at the output of ADS7254) is captured, and the FFT of the system is also taken using the ADS7254EVM and SDCC board. As shown in Figure 30 and Figure 31, the GUI captures show the captured AC signal, the FFT, and other parameters.

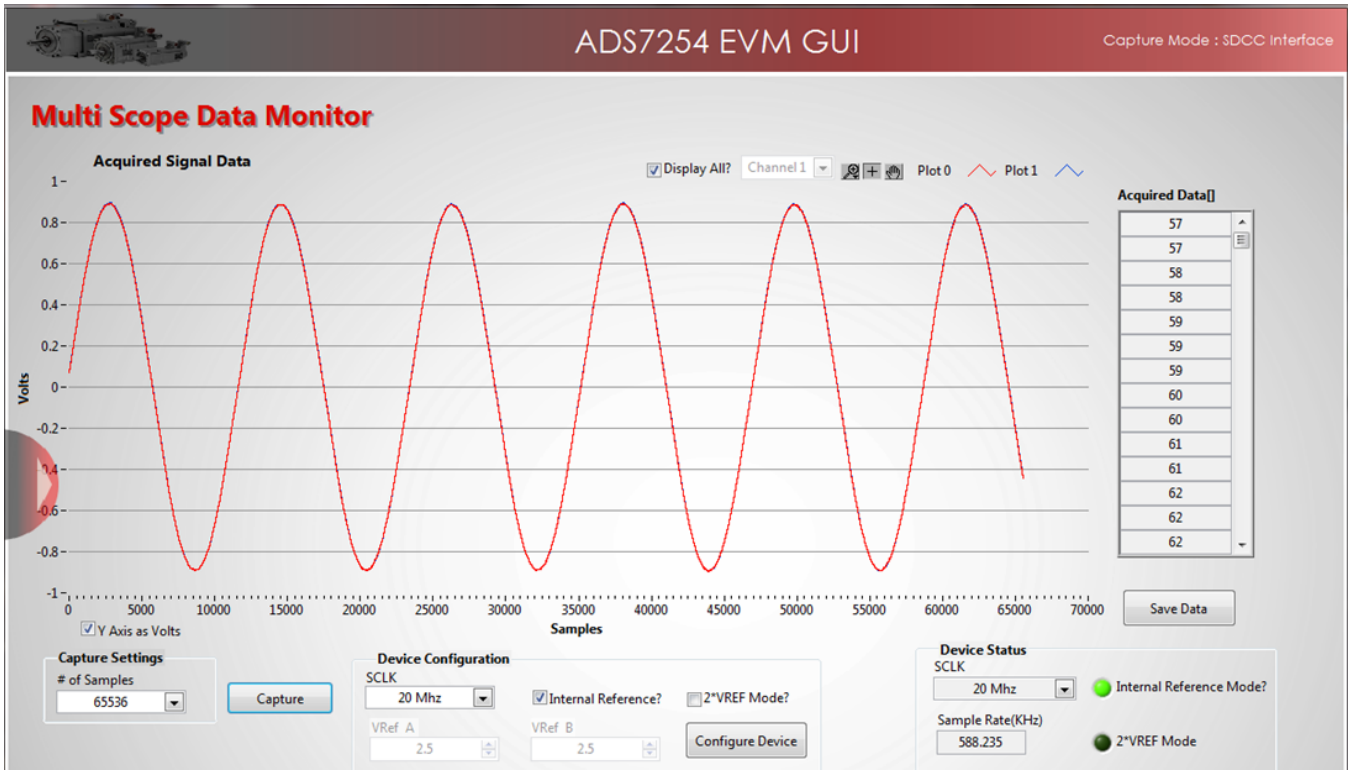


Figure 30. AC Signal Capture for Two Channels Using ADS7254 EVM GUI

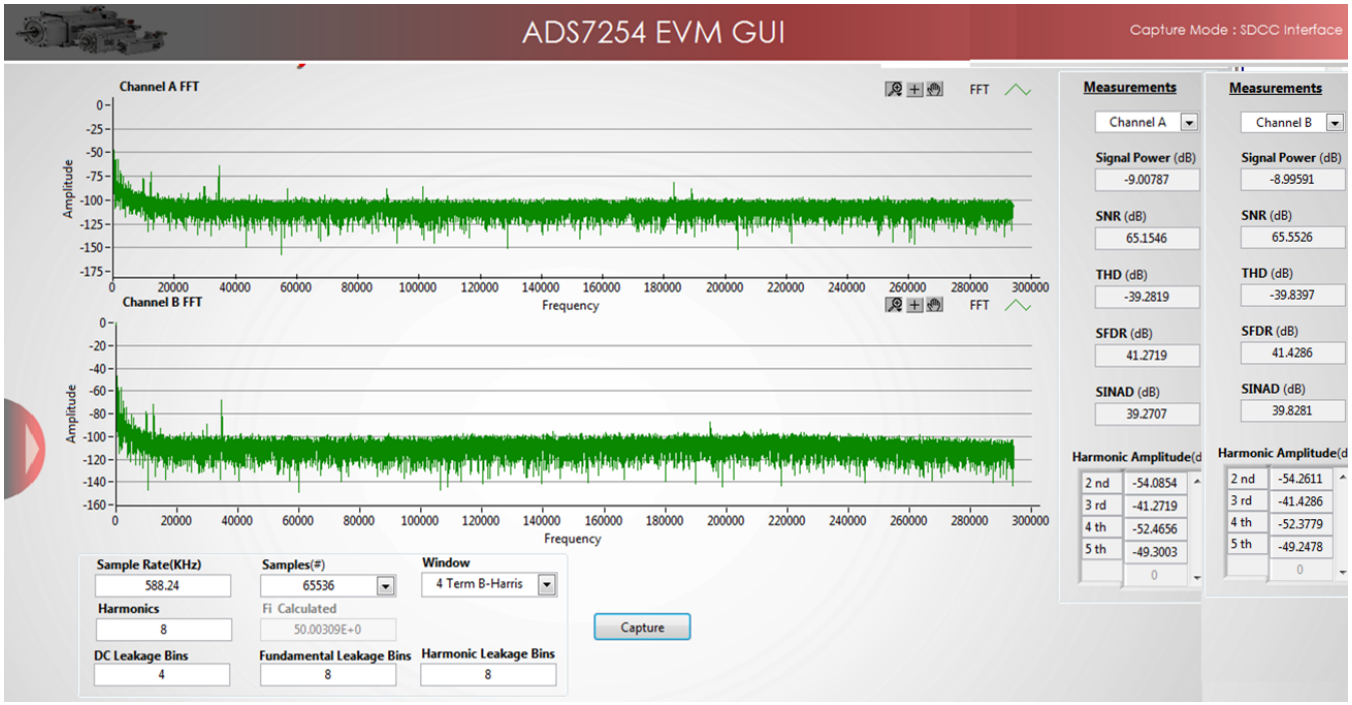


Figure 31. FFT and SNR for Two Channels Using ADS7254 EVM GUI

The FFT for both channels show an SNR of approximately 65 dB at a signal amplitude of –9 dBFS. This result is just an indication of performance, but the actual SNR can be measured when the device is operated with an input voltage that has reached the full-scale value of the ADC input range. Figure 32 is the setup used to measure the AC and DC performance for this reference design.

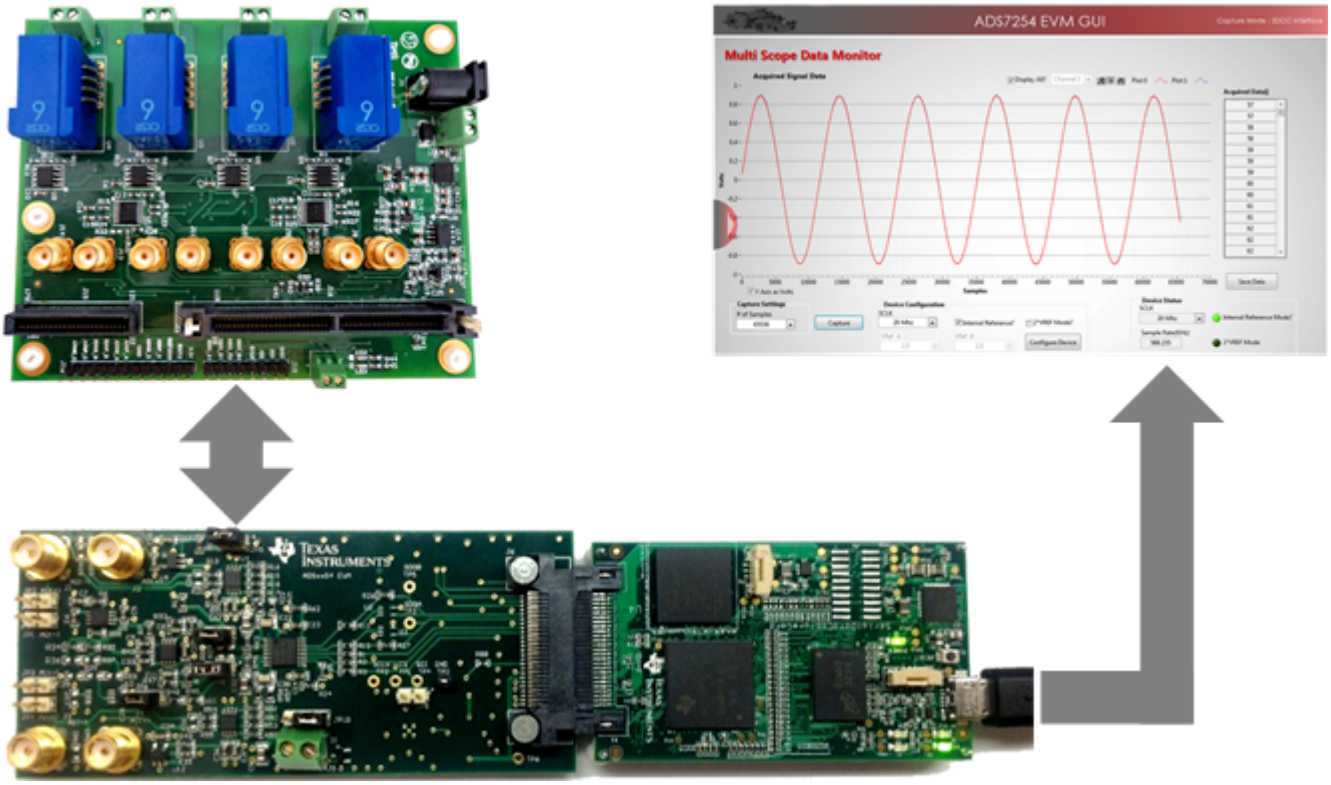


Figure 32. Test Setup for AC and DC Tests for ADS7254

9.4 DC Accuracy Tests (at 25°C and 75°C)

The following figures show the accuracy of the signal at each stage. Figure 33 shows accuracy of signal at the output of THS4531 at 25°C, and Figure 34 shows accuracy of signal at 75°C. The graphs include the offset and gain error compensation along with passive component mismatches in the feedback path of the THS4531.

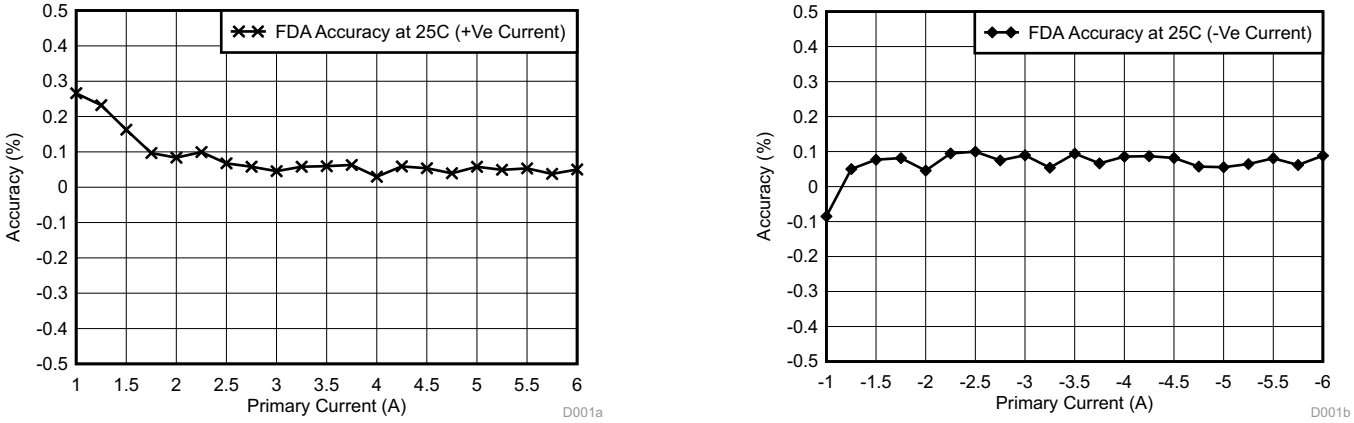


Figure 33. FDA Accuracy at 25°C for Positive Current (Left) for Negative Current (Right)

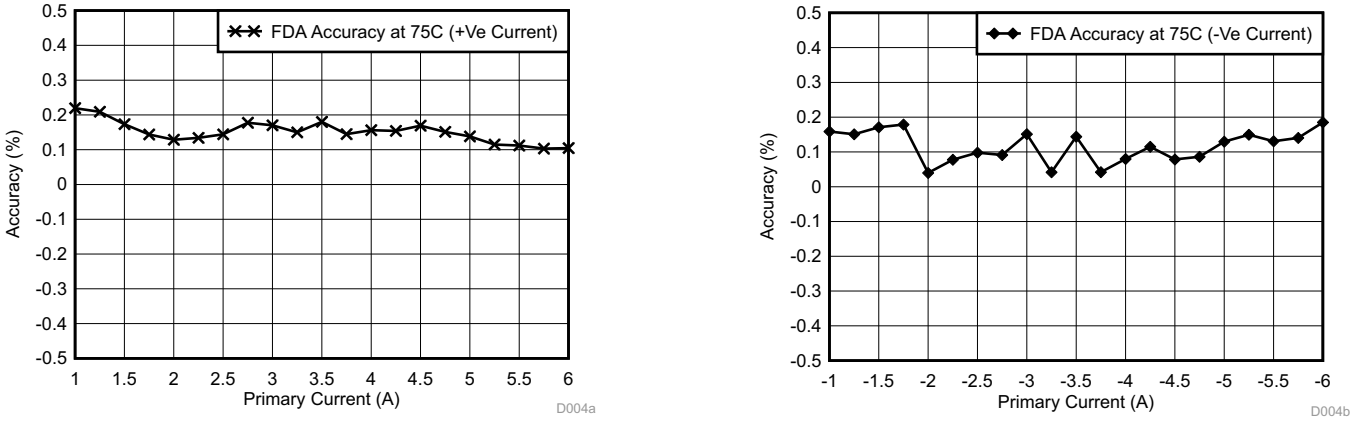


Figure 34. FDA Accuracy at 75°C for Positive Current (Left) for Negative Current (Right)

Figure 35 shows accuracy of the signal at the output of the ADS7254 at 25°C, and Figure 36 shows accuracy of ADC at 75°C. The graphs includes the linearity and gain error from the ADC itself.

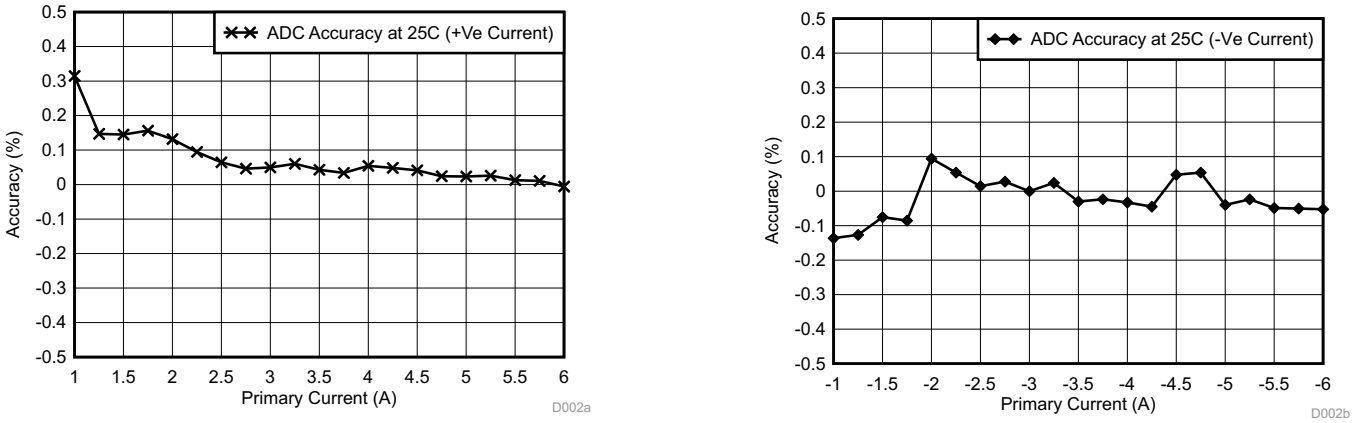


Figure 35. ADC Accuracy at 25°C for Positive Current (Left) for Negative Current (Right)

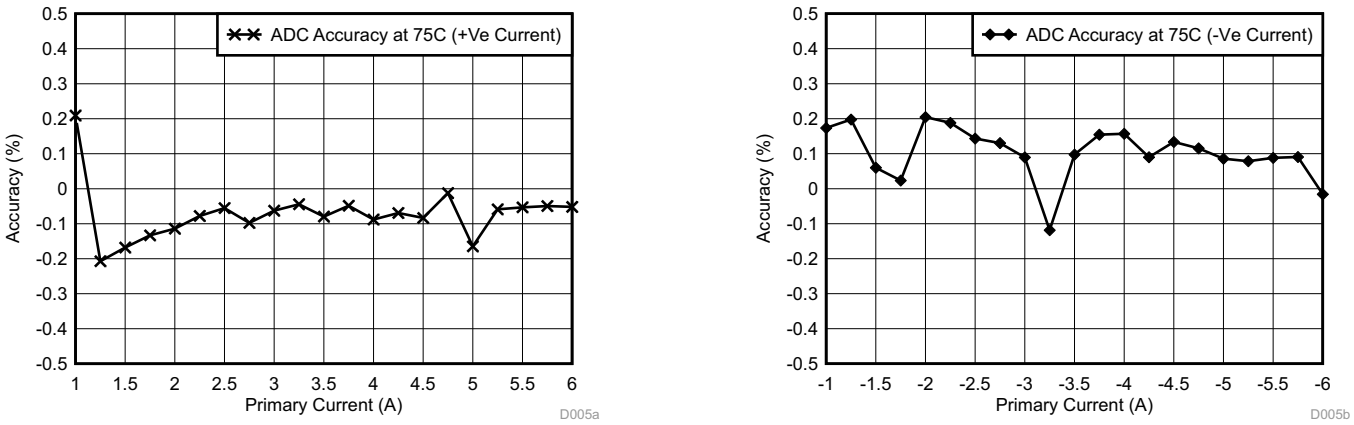


Figure 36. ADC Accuracy at 75°C for Positive Current (Left) for Negative Current (Right)

Figure 37 shows accuracy of signal for the entire signal chain (FDA + ADC) at 25°C, and Figure 38 shows the total accuracy at 75°C. Note that in a typical drive application, the current sensor would be used from 30% to 100% of its nominal current rating, so the accuracy should be considered for primary current from ±1.75 to ±6 A.

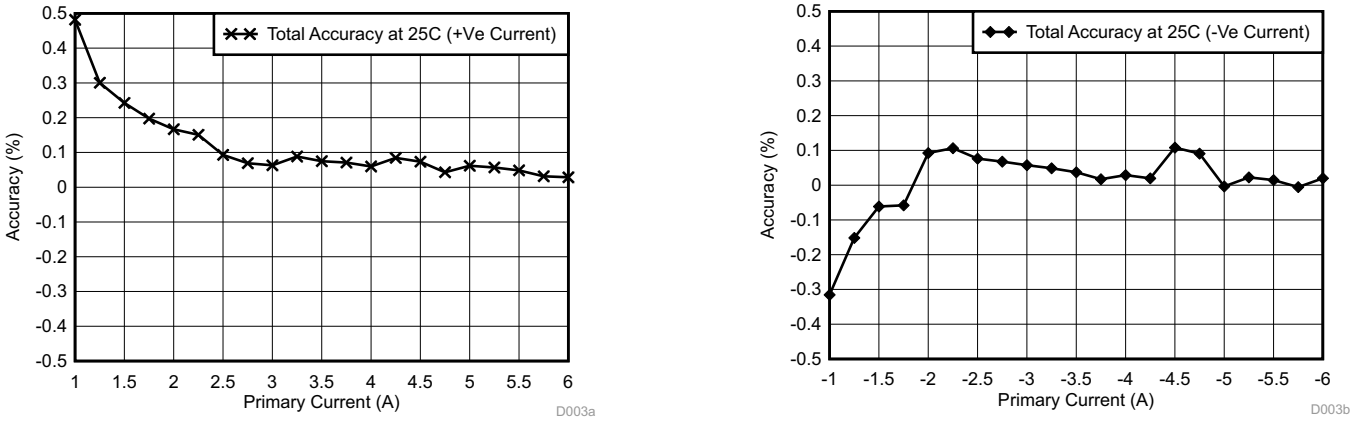


Figure 37. Total Accuracy at 25°C for Positive Current (Left) for Negative Current (Right)

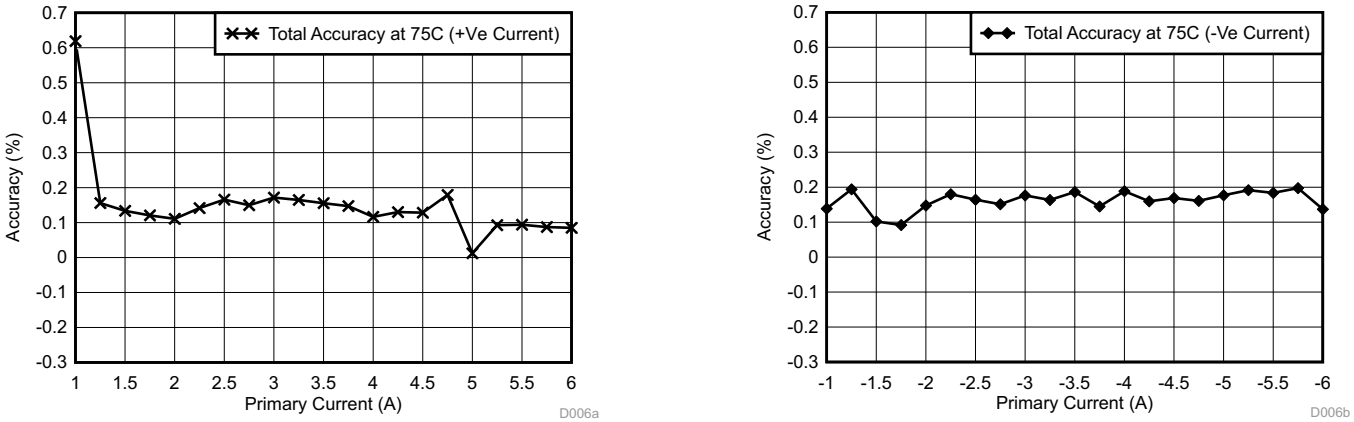


Figure 38. Total Accuracy at 75°C for Positive Current (Left) for Negative Current (Right)

9.5 DC Accuracy Tests Using Delfino F2837x Internal ADC (on Control Card)

The accuracy of the internal ADC of the Delfino F2837x is measured along with the fluxgate-based reference design. Figure 39 shows the screenshot capture of the ADC GUI. The total accuracy curve is as shown in Figure 40.

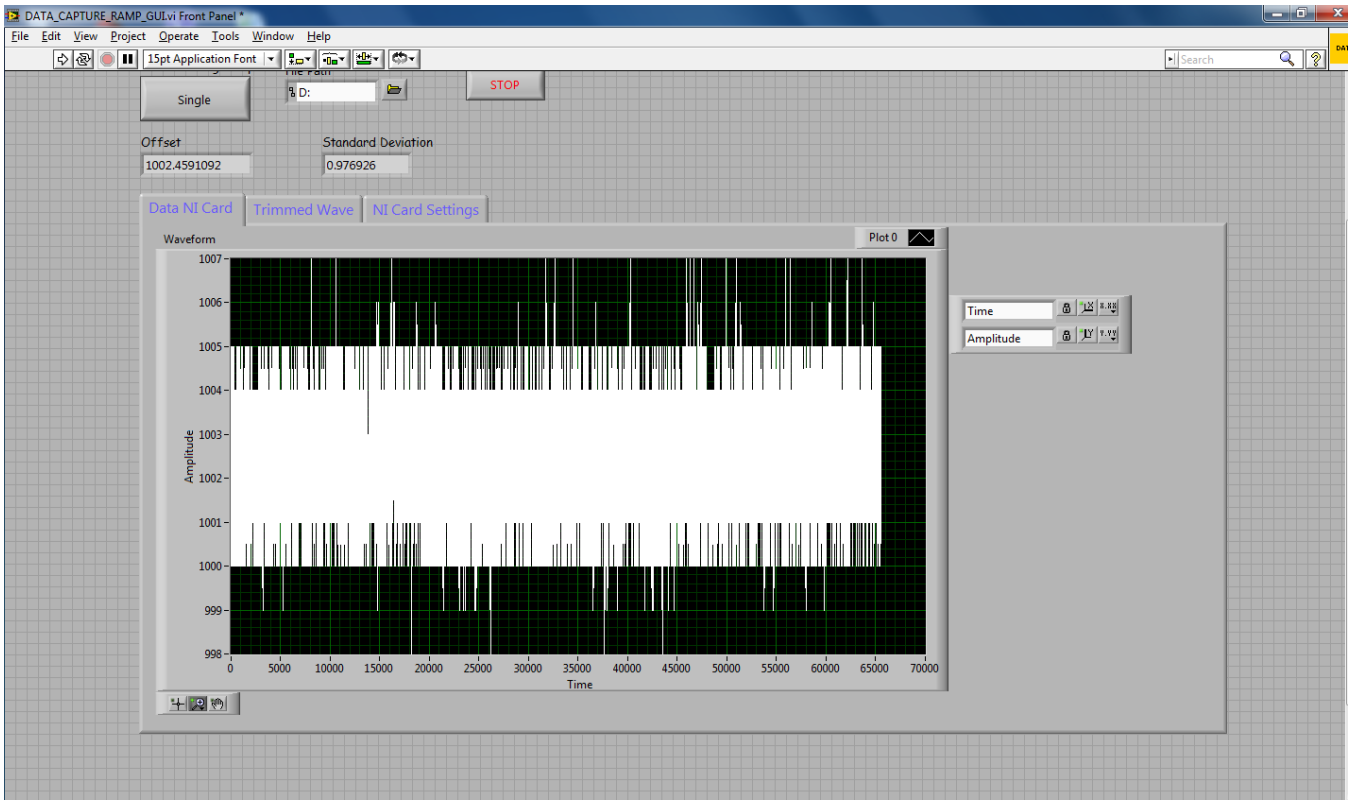


Figure 39. Screenshot of Internal ADC GUI for Delfino Controller

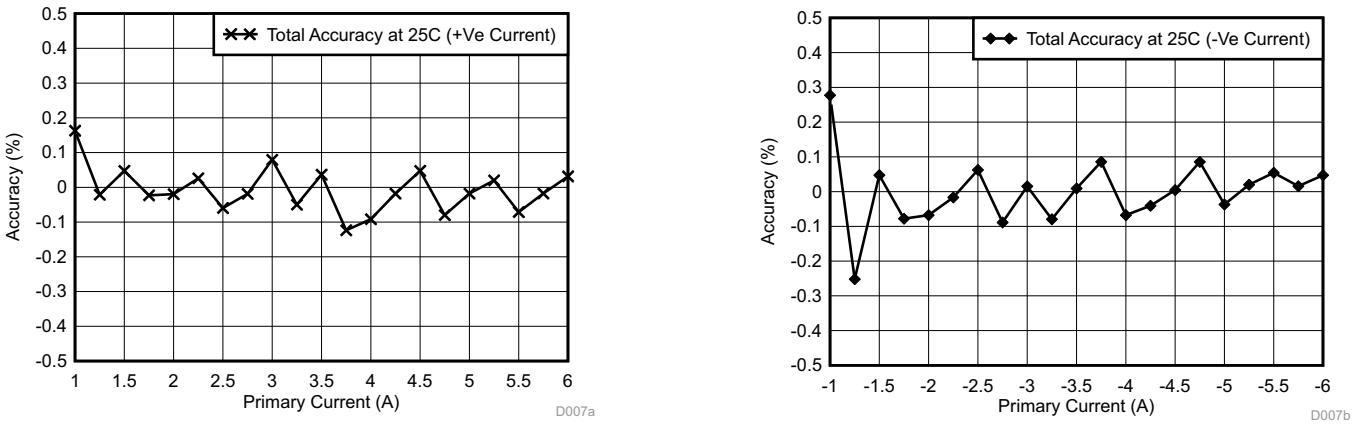


Figure 40. Total Accuracy Graph while Using Internal ADC of Delfino Controller for Positive Current (Left) for Negative Current (Right)

9.5.1 AC (or Dynamic) Performance Using Delfino F2837x Internal ADC

For an AC current of 4.5 V_{RMS} at a frequency of 50 Hz, the conditioned voltage signal (at the output of THS4531) is captured, and the FFT of the system is also taken using the Delfino F2837x Control Card. Figure 41 shows the captured signal. Note the time period X2-X1 (= 19.36507937 ms), which corresponds to the 51.6-Hz frequency.

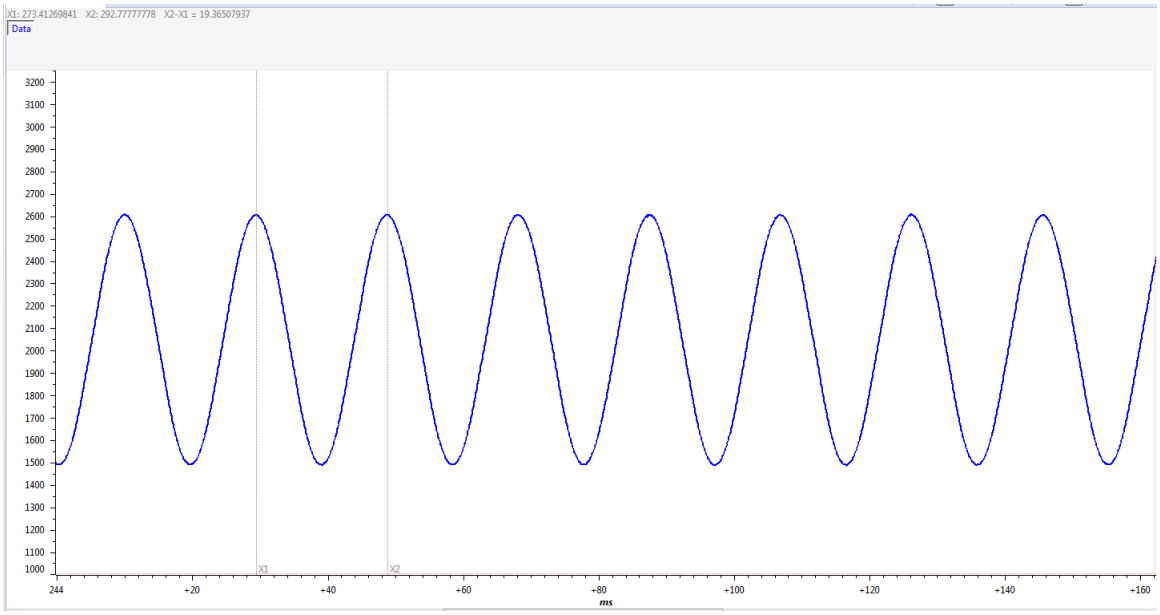


Figure 41. Signal Capture Using Delfino Control Card

9.6 THS4531A for Better DC Precision

Some highly accurate drive applications may ask for higher DC performance. In such cases, THS4531A can be used instead of THS4531 with no board changes. THS4531A has better DC precision compared to THS4531. For TIDA-00201, one channel is checked using THS4531A and THS4531. The graph in Figure 42 shows the DC accuracy for both the devices at 25°C.

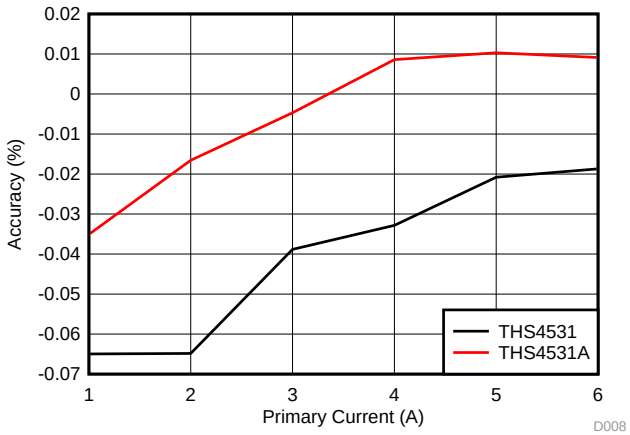


Figure 42. DC Accuracy Using THS4531 and THS4531A

9.7 Power Supply and Reference Circuit Functionality Tests

The power supply circuit is tested for functionality and ripple measurement. Figure 43 shows the output of the TPS7A4700 set at 5 V.

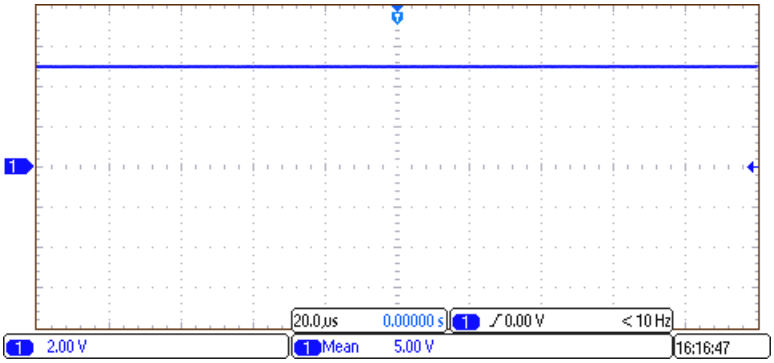


Figure 43. 5-V Signal from TPS7A4700

Figure 44 shows the 3.3-V digital supply voltage generated using the TLV70033.

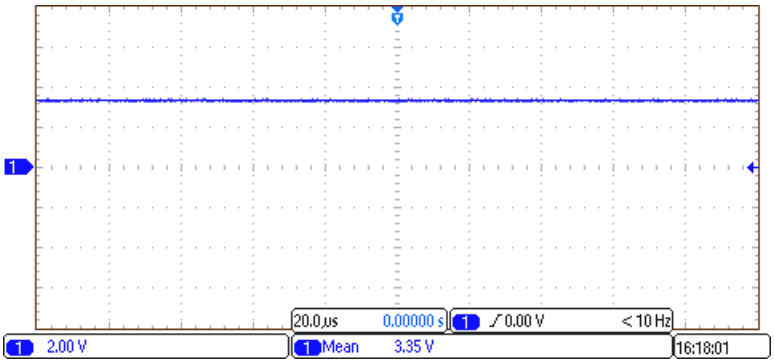


Figure 44. 3.3-V Reference Signal Generated by TLV70033

Figure 45 shows the output of the REF5025 set internally at 2.5 V.

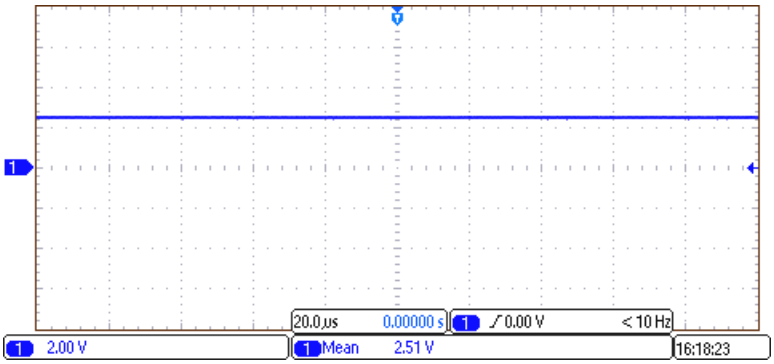


Figure 45. 2.5-V Reference Signal Generated by REF5025

Figure 46 and Figure 47 show the two outputs of the REF2025 set internally at 2.5 V and 1.25 V, respectively.

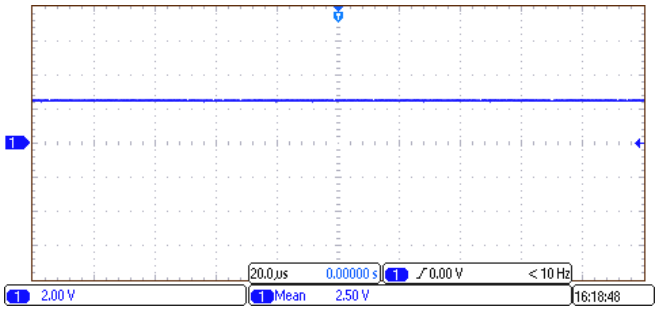


Figure 46. 2.5-V Reference Signal Generated by REF2025

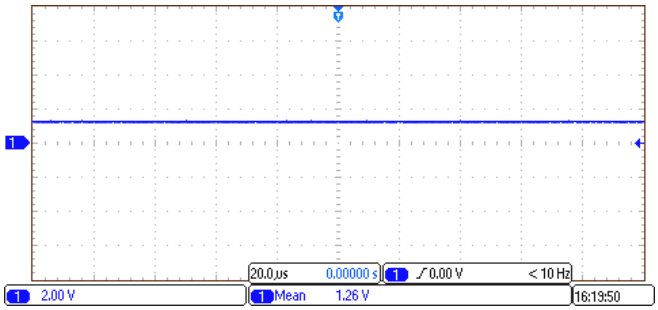


Figure 47. 1.25-V Reference Signal Generated by REF2025

9.8 Overcurrent and Earth Fault Detection Tests

The overcurrent and earth fault circuit are tested at 300% of the nominal current of the fluxgate sensors. The waveforms shown in Figure 48 and Figure 49 indicate the sensing of the overcurrent condition at VTH (pos), **which requires 98 nanoseconds to detect.**

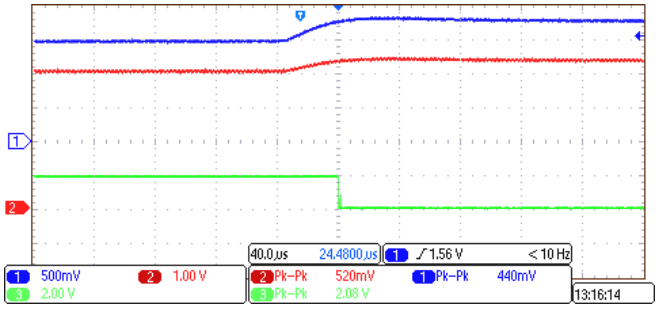


Figure 48. Overcurrent Detection at VTH (pos)

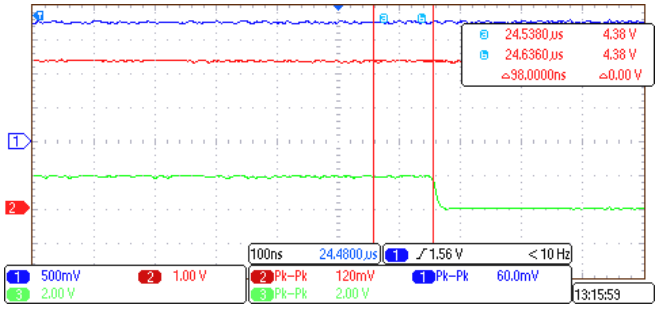


Figure 49. Overcurrent Detection at VTH (pos) — Zoomed

The waveforms shown in Figure 50 and Figure 51 indicate the sensing of the overcurrent condition at VTH (neg). The time required for the detection of the signal is 87.2 nanoseconds.

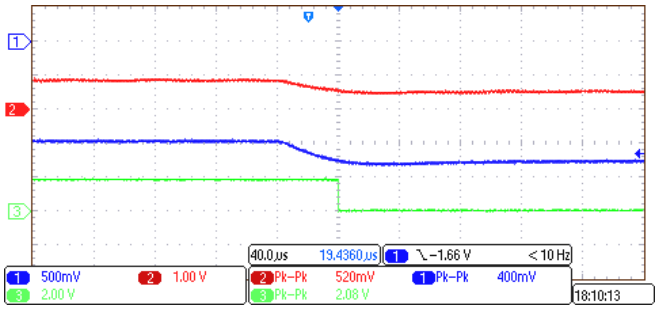


Figure 50. Overcurrent Detection at VTH (neg)

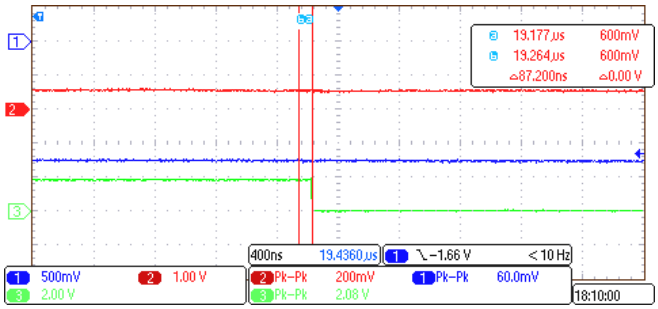


Figure 51. Overcurrent Detection at VTH (neg) — Zoomed

The waveforms shown in Figure 52 and Figure 53 indicate the sensing of earth fault condition at VTH (pos). The time required for the detection of the signal is 92 nanoseconds.

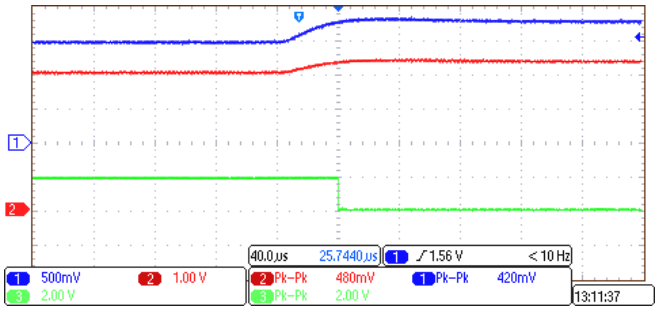


Figure 52. Earth Fault Detection at VTH (pos)

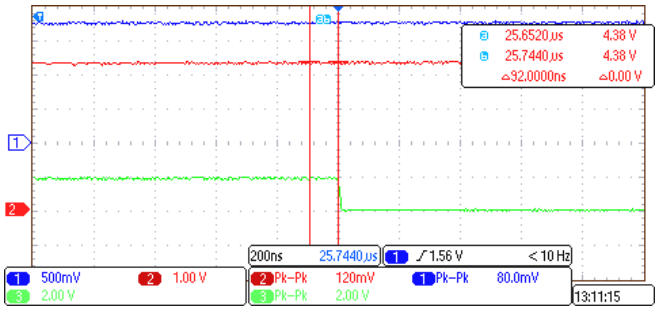


Figure 53. Earth Fault Detection at VTH (pos) — Zoomed

The waveforms shown in Figure 54 and Figure 55 indicate the sensing of the earth fault condition at VTH (neg). The time required for the detection of the signal is 98 nanoseconds.

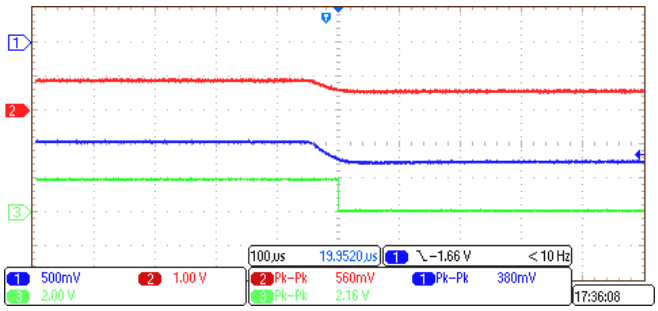


Figure 54. Earth Fault Detection at VTH (neg)

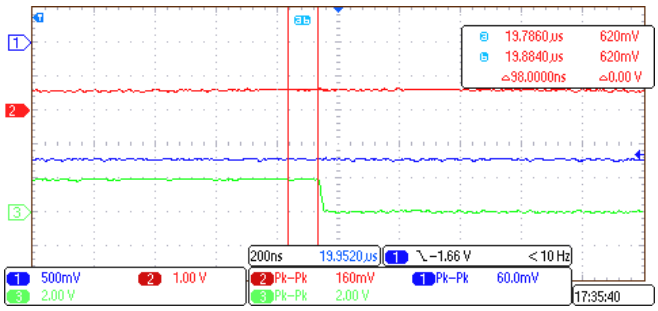


Figure 55. Earth Fault Detection at VTH (neg) — Zoomed

The comparators used in the protection circuits are open-drain outputs. The pull-up resistors are connected to 3.3 V (which is typically equal to digital supply of the MCU or FPGA) so that the high and low levels of the comparator outputs are within the sensing range of the MCU or FPGA.

10 Design Files

10.1 Schematics

To download the schematics, see the design files at TIDA-00201.

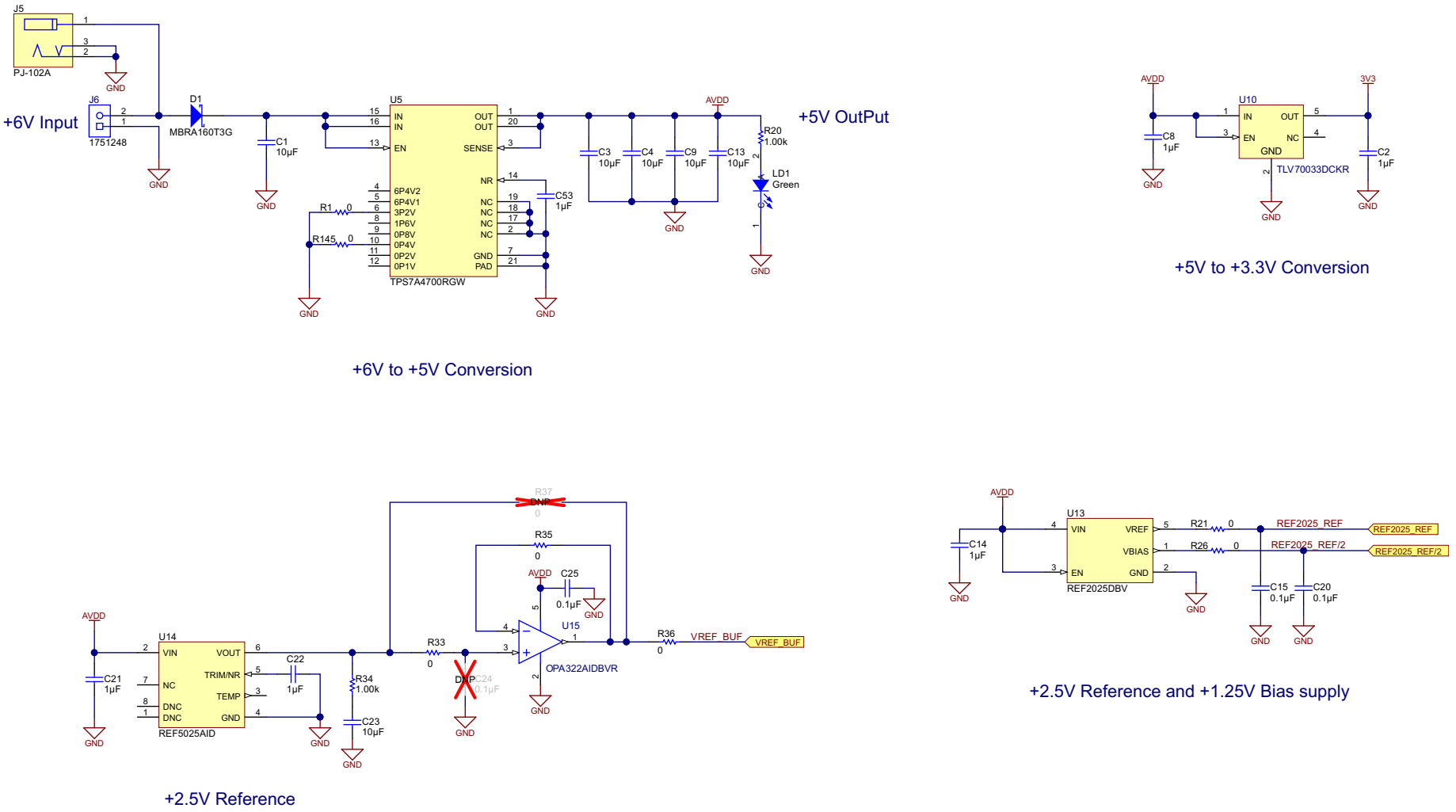
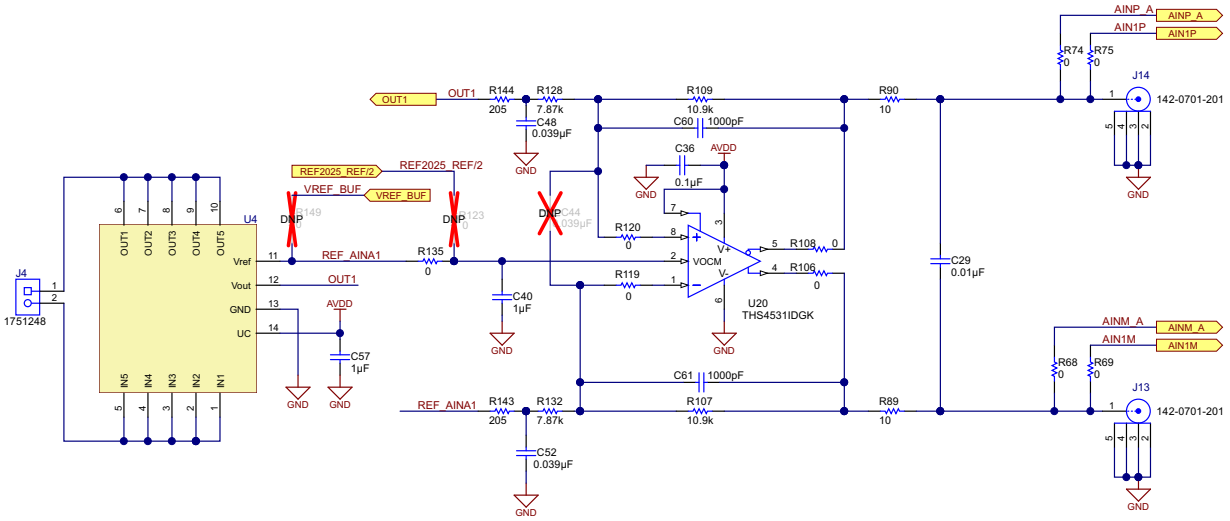
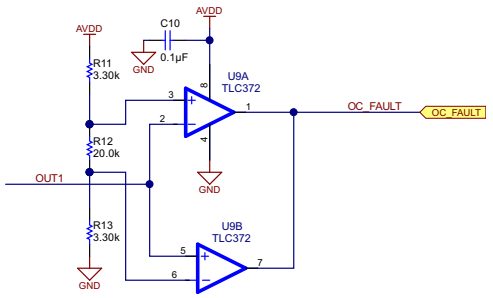
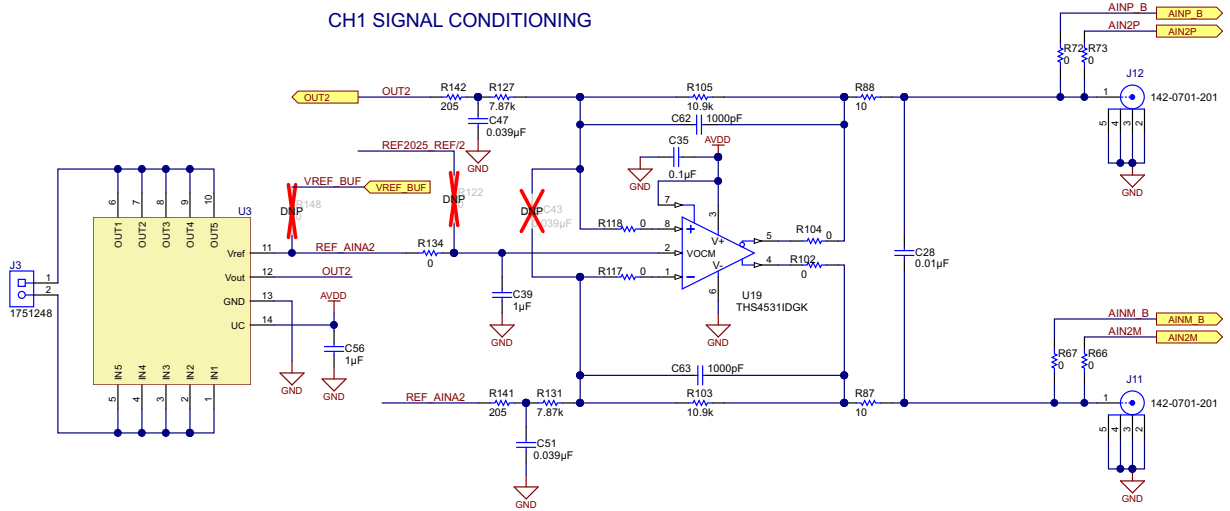


Figure 56. Power Schematic







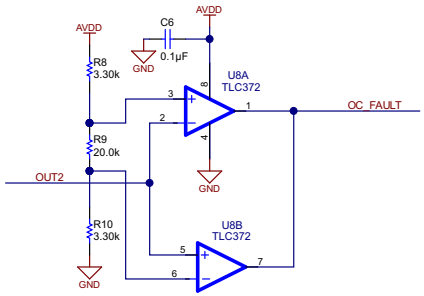
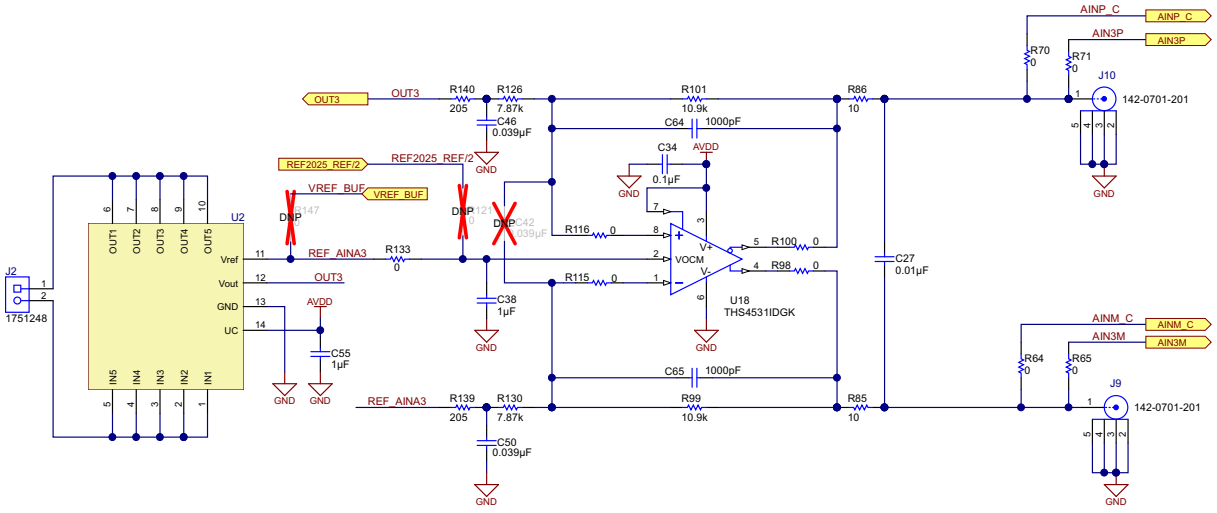
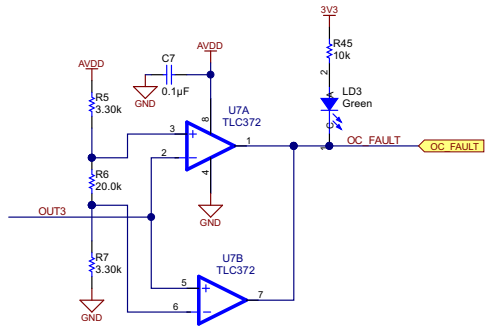
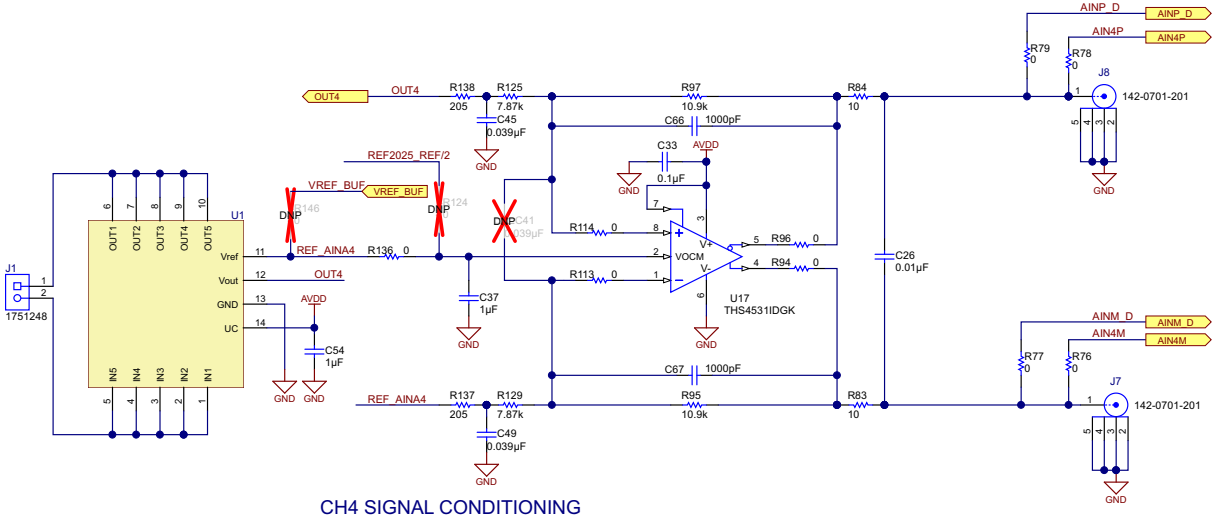


Figure 57. Channel 1 and 2 Schematic







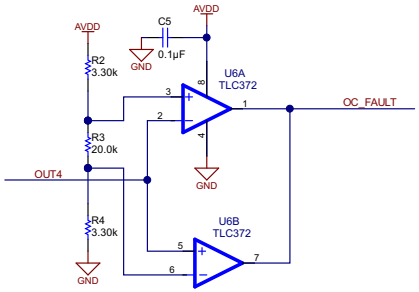
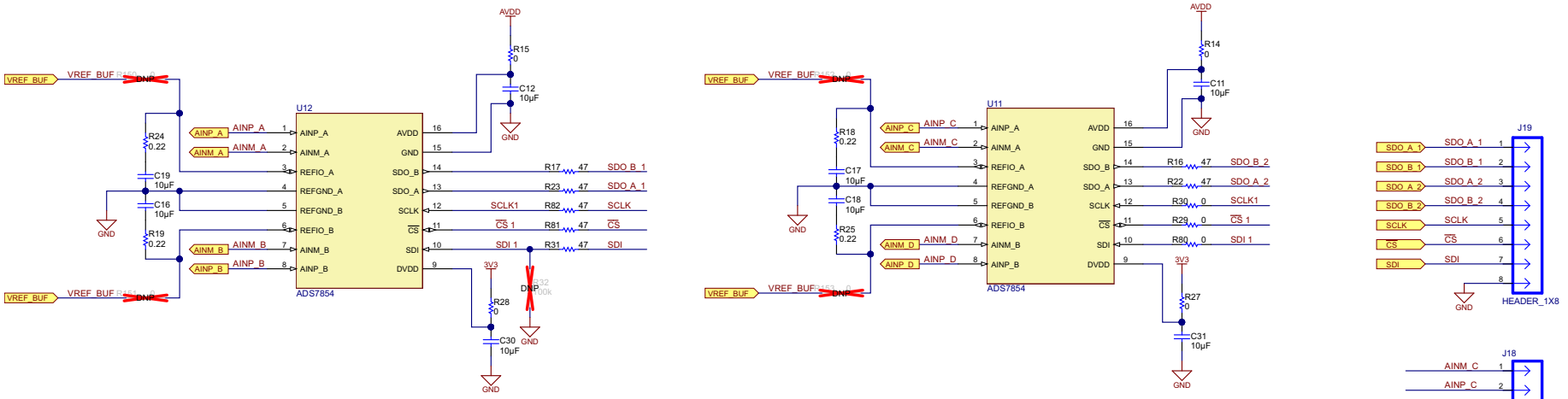
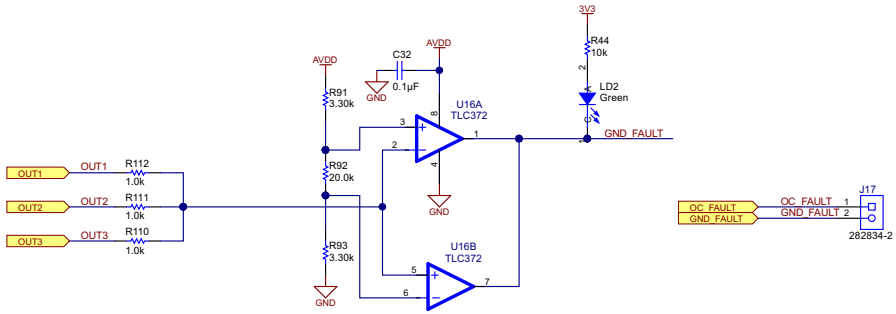


Figure 58. Channel 3 and 4 Schematic



TWO ADS7854s FOR INTERFACING WITH EX TERNAL MOTOR CONTROLLER



GROUND FAULT DETECTION

Figure 59. ADC Connectors Schematic

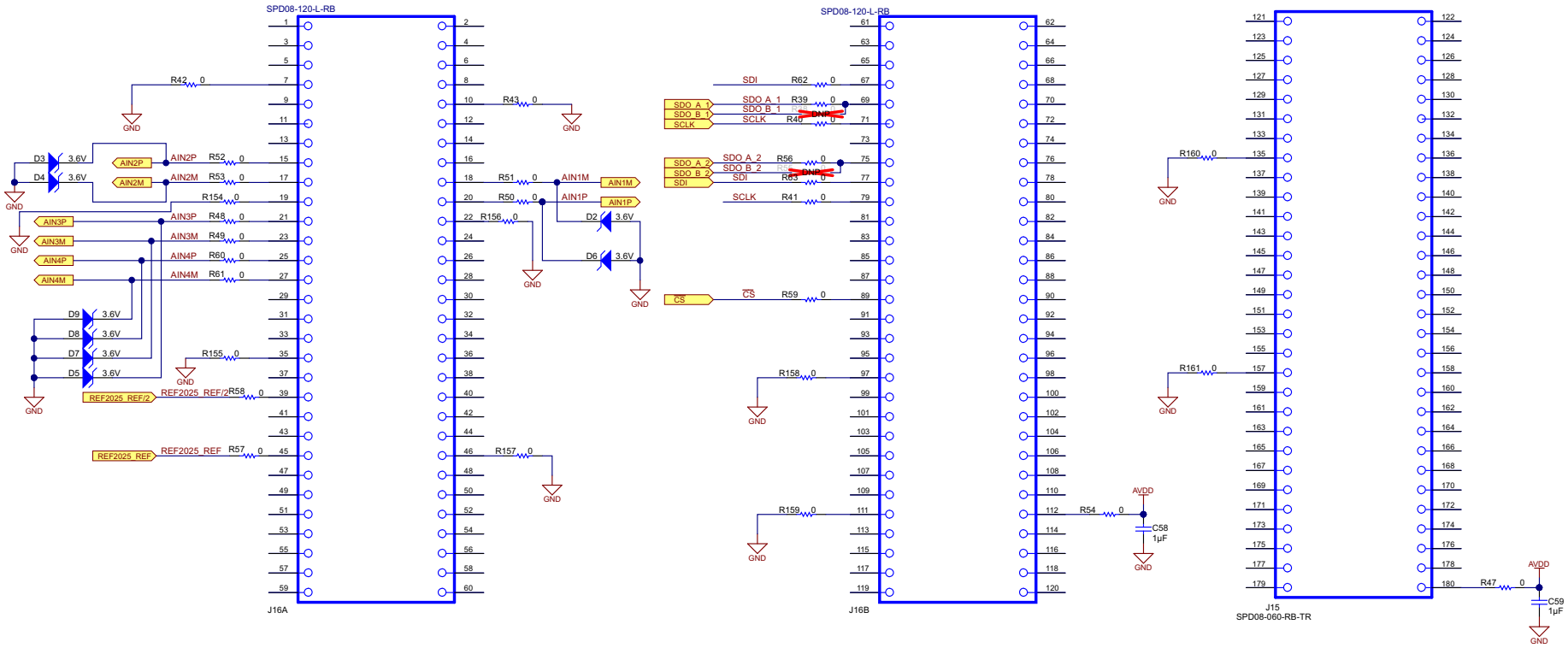


Figure 60. 180-Pin Connector Interface Schematic

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00201.

Table 7. BOM

FITTED	QTY	DESIGNATOR	DESCRIPTION	PARTNUMBER	MANUFACTURER	RoHS	PACKAGE REFERENCE	SUPPLIER	SUPPLIER PARTNUMBER
Fitted	1	!PCB1	Printed circuit board	TIDA-00201	Any	O			
Fitted	1	C23	CAP, CERM, 10 µF, 16 V, ±20%, X5R, 0603	EMK107BBJ106MA-T	Taiyo Yuden	Y	0603	Digi-Key	587-3238-1-ND
Fitted	1	D1	Diode, Schottky, 60 V, 1 A, SMA	MBRA160T3G	ON Semiconductor	Y	SMA	Digi-Key	MBRA160T3GOSCT-ND
Fitted	1	J15	Conn High SPD Card Edge 60 POS	SPD08-060-RB-TR	3M	Y	28.6 × 7 mm	Digi-Key	3M12039TR-ND
Fitted	1	J16	Conn High SPD Card Edge 120 POS	SPD08-120-L-RB	3M	Y	7 × 56 mm	Digi-Key	3M12042TR-ND
Fitted	1	J17	Terminal Block, 2×1, 2.54 mm, TH	282834-2	TE Connectivity	Y	Terminal Block, 2×1, 2.54 mm, TH	Digi-Key	A98333-ND
Fitted	1	J18	Header, Male 12-pin, 100-mil spacing	PEC12SAAN	Sullins		0.100 inch × 12		
Fitted	1	J19	Header, Male 8-pin, 100-mil spacing	PEC08SAAN	Sullins		0.100 inch × 8		
Fitted	1	J5	Connector, DC Jack 2.1×5.5 mm, TH	PJ-102A	CUI Inc.	Y	Power Jack, 14.4 × 11 × 9 mm	Digi-Key	CP-102A-ND
Fitted	1	LBL1	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	THT-14-423-10	Brady	Y	PCB Label 0.650"H × 0.200"W	Farnell	2065596
Fitted	1	R20	RES, 1.00 k, 1%, 0.1 W, 0603	CRCW06031K00FKEA	Vishay-Dale	Y	0603	Digi-Key	541-1.00KHCT-ND
Fitted	1	R34	RES, 1.00 kΩ, 1%, 0.1 W, 0603	RC0603FR-071KL	Yageo America	Y	0603	Digi-Key	311-1.00KHRCT-ND
Fitted	1	U10	Single Output LDO, 200 mA, Fixed 3.3-V output, 2- to 5.5-V Input, with Low IQ, 5-pin SC70 (DCK), –40°C to 125°C, Green (RoHS and no Sb/Br)	TLV70033DCKR	Texas Instruments		DCK0005A	Digi-Key	296-32413-2-ND
Fitted	1	U13	Dual Output Voltage Reference 2.5 V, DBV0005A	REF2025DBV	Texas Instruments	Y	DBV0005A		
Fitted	1	U14	Low-Noise, Very Low-Drift, Precision Voltage Reference, 2.5 V, D008A	REF5025AID	Texas Instruments	Y	D0008A		

Table 7. BOM (continued)

FITTED	QTY	DESIGNATOR	DESCRIPTION	PARTNUMBER	MANUFACTURER	RoHS	PACKAGE REFERENCE	SUPPLIER	SUPPLIER PARTNUMBER
Fitted	1	U15	20 MHz, Low Noise, RRIO, CMOS Operational Amplifier with Shutdown, 1.8 to 5.5 V, –40°C to 125°C, 5-pin SOT23 (DBV0005A), Green (RoHS & no Sb/Br)	OPA322AIDBVR	Texas Instruments		DBV0005A	Digi-Key	296-29488-2-ND
Fitted	1	U5	36-V, 1-A, 4.17-μV_{RMS}, RF LDO, RGW0020A	TPS7A4700RGW	Texas Instruments	Y	RGW0020A		
Fitted	10	C37, C38, C39, C40, C54, C55, C56, C57, C58, C59	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0603	GRM188R71E105 KA12D	MuRata	Y	0603	Digi-Key	490-5307-1-ND
Fitted	10	C5, C6, C7, C10, C25, C32, C33, C34, C35, C36	CAP, CERM, 0.1 µF, 16 V, ±5%, X7R, 0603	C0603C104J4RAC TU	Kemet	Y	0603	Digi-Key	399-1097-1-ND
Fitted	10	R2, R4, R5, R7, R8, R10, R11, R13, R91, R93	RES, 3.30 kΩ, 1%, 0.1 W, 0603	RC0603FR-073K3L	Yageo America	Y	0603	Digi-Key	311-3.30KHRCT-ND
Fitted	2	C15, C20	CAP, CERM, 0.1 µF, 10 V, ±10%, X7R, 0603	C0603C104K8RAC TU	Kemet	Y	0603	Digi-Key	399-1095-1-ND
Fitted	2	R44, R45	RES, 10 kΩ, 5%, 0.1 W, 0603	CRCW060310K0J NEA	Vishay-Dale	Y	0603	Digi-Key	541-10KGCT-ND
Fitted	2	U11, U12	IC ADC 12-BIT 1MSPS Dual 16TSSOP	ADS7854	Texas Instruments	Y	16TSSOP		
Fitted	3	LD1, LD2, LD3	LED SmartLED Green 570 NM	LG L29K-G2J1-24-Z	OSRAM		0603	Digi-Key	475-2709-2-ND
Fitted	3	R110, R111, R112	RES, 1.0 kΩ, 5%, 0.1 W, 0603	CRCW06031K00J NEA	Vishay-Dale	Y	0603	Mouser	71-CRCW0603J-1.0K-E3
Fitted	4	C26, C27, C28, C29	CAP, CERM, 0.01 µF, 16 V, ±10%, X7R, 0603	GRM188R71C103 KA01D	MuRata	Y	0603	Digi-Key	490-1525-1-ND
Fitted	4	H1, H2, H3, H4	Machine Screw, Round, #4–40 × 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	BandF Fastener Supply	Y	Screw	Digi-Key	H542-ND
Fitted	4	H5, H6, H7, H8	Standoff, Hex, 0.5"L #4–40 Nylon	1902C	Keystone	Y	Standoff	Digi-Key	1902CK-ND
Fitted	4	R18, R19, R24, R25	RES, 0.22 Ω, 1%, 0.1 W, 0603	ERJ-3RQFR22V	Panasonic	Y	0603	Digi-Key	P.22AJDKR-ND
Fitted	4	U1, U2, U3, U4	Sensor Current 50-A, 5-V MOD	CKSR X-NP	LEM USA Inc	Y	Module	Digi-Key	98-1098-5-ND

Table 7. BOM (continued)

FITTED	QTY	DESIGNATOR	DESCRIPTION	PARTNUMBER	MANUFACTURER	RoHS	PACKAGE REFERENCE	SUPPLIER	SUPPLIER PARTNUMBER
Fitted	4	U17, U18, U19, U20	Ultra Low Power, Rail-to-Rail Output, Fully-Differential Amplifier, DGK0008A	THS4531IDGK	Texas Instruments	Y	DGK0008A		
Fitted	5	C1, C3, C4, C9, C13	CAP, CERM, 10 µF, 16 V, ±10%, X5R, 0805	GRM21BR61C106KE15L	MuRata	Y	0805	Digi-Key	490-3886-1-ND
Fitted	5	J1, J2, J3, J4, J6	Conn Term Block, 2POS, 3.5 mm, TH	1751248	Phoenix Contact	Y	11 × 8.5 × 7.3 mm	Digi-Key	277-5719-ND
Fitted	5	R3, R6, R9, R12, R92	RES, 20.0 kΩ, 1%, 0.1 W, 0603	CRCW060320K0FKEA	Vishay-Dale	Y	0603	Digi-Key	541-20.0KHCT-ND
Fitted	5	U6, U7, U8, U9, U16	IC, Dual Differential Comparators, 2 to 36 Vin	TLC372	Texas Instruments		SO-8		
Fitted	6	C2, C8, C14, C21, C22, C53	CAP, CERM, 1 µF, 10 V, ±10%, X7R, 0805	C0805C105K8RACTU	Kemet	Y	0805	Digi-Key	399-1172-1-ND
Fitted	6	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A		Fiducial		
Fitted	7	R16, R17, R22, R23, R31, R81, R82	RES, 47 Ω, 5%, 0.1 W, 0603	CRCW060347R0JNEA	Vishay-Dale	Y	0603	Digi-Key	541-47GCT-ND
Fitted	8	C11, C12, C16, C17, C18, C19, C30, C31	CAP, CERM, 10 µF, 25 V, ±20%, X5R, 0603	C1608X5R1E106M080AC	TDK	Y	0603	Digi-Key	445-9015-1-ND
Fitted	8	C45, C46, C47, C48, C49, C50, C51, C52	CAP, CERM, 0.039 µF, 16 V, ±10%, X7R, 0603	GRM188R71C393KA01D	MuRata	Y	0603	Digi-Key	GRM188R71C393KA01D-ND
Fitted	8	C60, C61, C62, C63, C64, C65, C66, C67	CAP, CERM, 1000 pF, 16 V, ±10%, X7R, 0603	GRM188R71C102KA01D	MuRata	Y	0603	Digi-Key	GRM188R71C102KA01D-ND
Fitted	8	D2, D3, D4, D5, D6, D7, D8, D9	Diode, Zener, 3.6 V, 500 mW, SOD-123	MMSZ5227B-7-F	Diodes Inc.	Y	SOD-123	Digi-Key	MMSZ5227B-FDICT-ND
Fitted	8	J7, J8, J9, J10, J11, J12, J13, J14	Connector, TH, SMA	142-0701-201	Emerson Network Power	Y	SMA	Digi-Key	J500-ND
Fitted	8	R125, R126, R127, R128, R129, R130, R131, R132	RES, 7.87 k, 1%, 0.1 W, 0603	CRCW06037K87FKEA	Vishay-Dale	Y	0603	Digi-Key	541-7.87KHCT-ND
Fitted	8	R137, R138, R139, R140, R141, R142, R143, R144	RES, 205, 1%, 0.1 W, 0603	CRCW0603205RFKEA	Vishay-Dale	Y	0603	Digi-Key	541-205HCT-ND
Fitted	8	R83, R84, R85, R86, R87, R88, R89, R90	RES, 10 Ω, 5%, 0.1W, 0603	CRCW060310R0JNEA	Vishay-Dale	Y	0603	Digi-Key	541-10GCT-ND
Fitted	8	R95, R97, R99, R101, R103, R105, R107, R109	RES, 10.9 k, 0.5%, 0.1 W, 0603	RT0603DRE0710K9L	Yageo America	Y	0603		

Table 7. BOM (continued)

FITTED	QTY	DESIGNATOR	DESCRIPTION	PARTNUMBER	MANUFACTURER	RoHS	PACKAGE REFERENCE	SUPPLIER	SUPPLIER PARTNUMBER
Fitted	80	R1, R14, R15, R21, R26, R27, R28, R29, R30, R33, R35, R36, R39, R40, R41, R42, R43, R46, R47, R48, R49, R50, R51, R52, R53, R54, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R94, R96, R98, R100, R102, R104, R106, R108, R113, R114, R115, R116, R117, R118, R119, R120, R133, R134, R135, R136, R145, R154, R155, R156, R157, R158, R159, R160, R161	RES, 0 Ω, 5%, 0.1 W, 0603	CRCW06030000Z0EA	Vishay-Dale	Y	0603	Digi-Key	541-0.0GCT-ND
Not Fitted	0	C24	CAP, CERM, 0.1 µF, 10 V, ±10%, X7R, 0603	C0603C104K8RACTU	Kemet	Y	0603	Digi-Key	399-1095-1-ND
Not Fitted	0	C41, C42, C43, C44	CAP, CERM, 0.039 µF, 16 V, ±10%, X7R, 0603	GRM188R71C393KA01D	MuRata	Y	0603	Digi-Key	GRM188R71C393KA01D-ND
Not Fitted	0	R32	RES, 100 kΩ, 1%, 0.1 W, 0603	CRCW0603100KFKEA	Vishay-Dale	Y	0603	Digi-Key	541-100KHCT-ND
Not Fitted	0	R37, R38, R55, R121, R122, R123, R124, R146, R147, R148, R149, R150, R151, R152, R153	RES, 0 Ω, 5%, 0.1 W, 0603	CRCW06030000Z0EA	Vishay-Dale	Y	0603	Digi-Key	541-0.0GCT-ND

10.3 PCB Layout

NOTE: The total dimension of the board is 112 × 90 mm.

10.3.1 Layout Guidelines

Layout of Amplifier Section

The THS4531 datasheet provides some general guidelines for the layout of the external components near the amplifier, ground plane construction, and power routing:

1. Keep signal routing direct and as short as possible into and out of the op-amp.
2. Make the feedback path short and direct to avoid vias if possible.
3. Remove the ground or power planes from directly under the amplifier's input and output pins.
4. Place a series output resistor as near to the output pin as possible.
5. Place a power supply decoupling capacitor within 2 inches of the device and share with other op-amps. For a split supply, use a capacitor for both supplies.
6. Place a 0.1-µF power supply decoupling capacitor as near to the power supply pins as possible, preferably within 0.1 inch. For a split supply, use a capacitor for both supplies.
7. The PD pin uses TTL logic levels referenced to the negative supply voltage (VS–). When not used, tie the PD pin to the positive supply to enable the amplifier. When used, actively drive the pin high or low, and do not leave it in an indeterminate logic state. Although it is not required, use a bypass capacitor for robustness in noisy environments.

Layout of ADC Section

The most important considerations in designing the PCB layout are as follows:

1. Keep the length of traces from the reference buffer circuit (REF, THS, and OPA) to the REFP input pin of the ADC as small as possible to minimize the trace inductance that can lead to instability and potential issues with the accurate settling of the reference voltage.
2. Locate the input driver circuit, comprised of the THS4521, as close as possible to the inputs of the ADC to minimize loop area, making the layout more robust against EMI/RFI rejection. Similarly, keep the resistors and capacitor of the anti-aliasing filter at the inputs of the ADC close together and close to the inputs of the ADC to minimize the loop area.
3. Keep the traces feeding the differential input voltage from the source up to the differential inputs of the ADC symmetrical without any sharp turns.

10.3.2 Layer Plots

To download the layer plots, see the design files at TIDA-00201.

Figure 61. Top Overlay

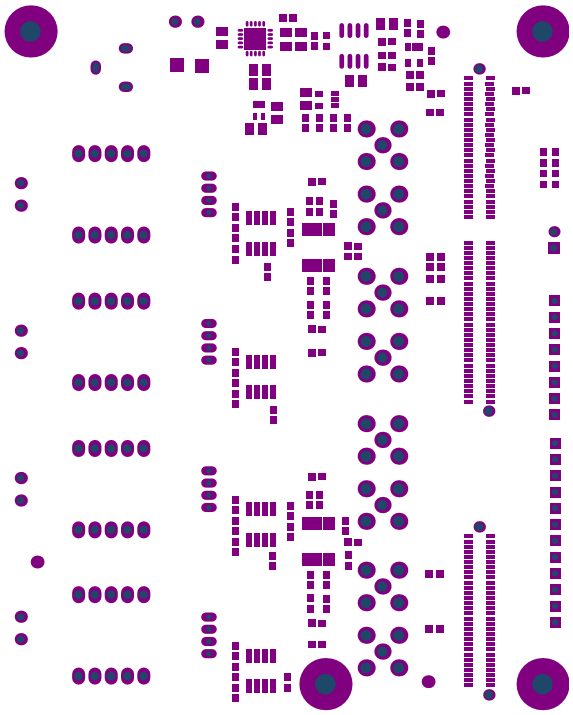


Figure 62. Top Solder

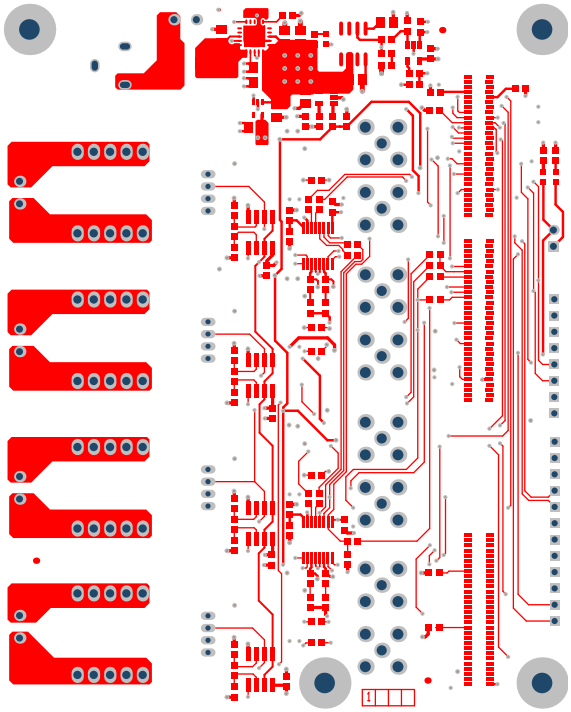


Figure 63. Top Layer

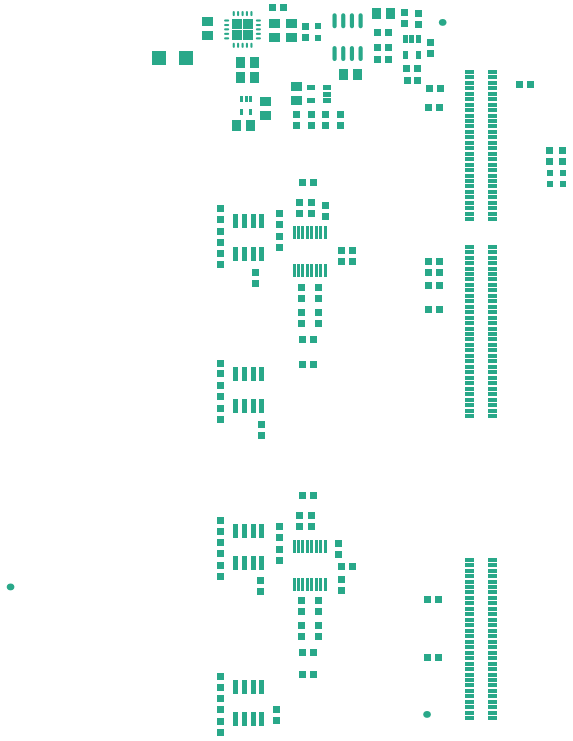


Figure 64. Top Paste

Figure 65. Bottom Paste

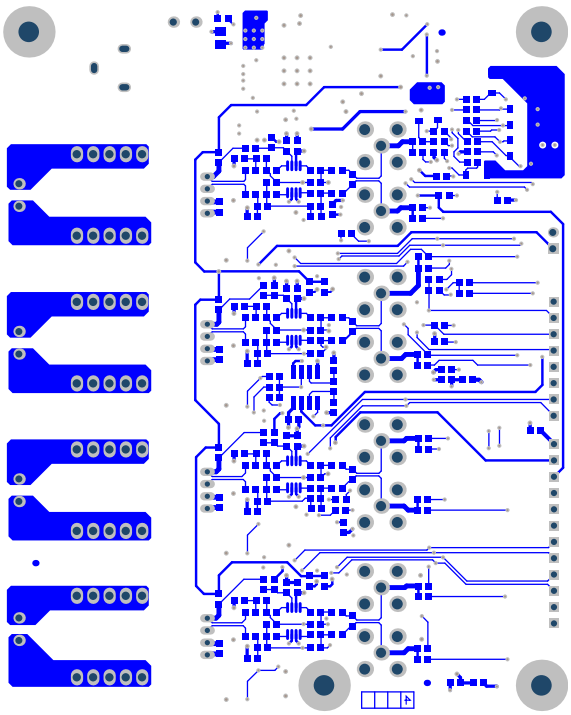


Figure 66. Bottom Layer

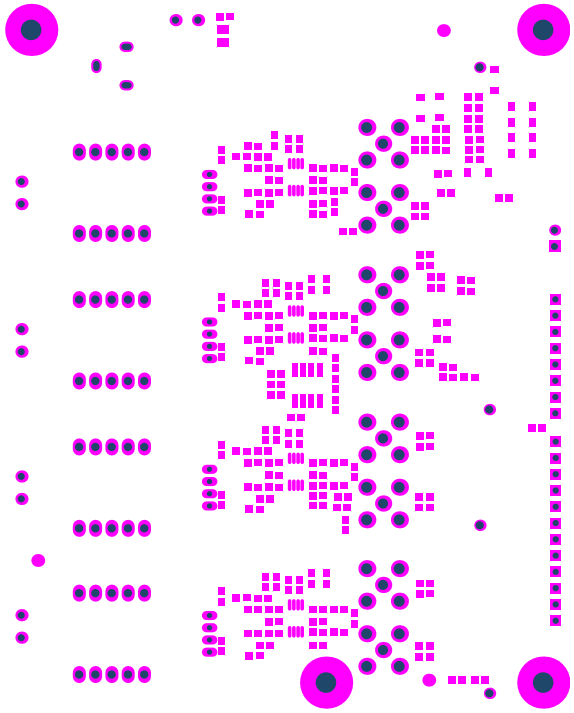


Figure 67. Bottom Solder

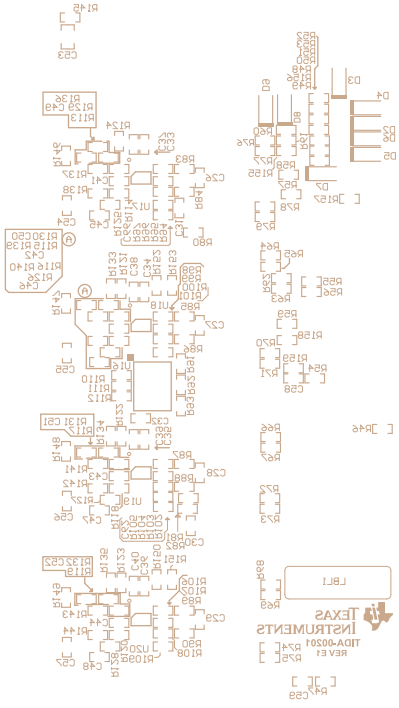


Figure 68. Bottom Overlay

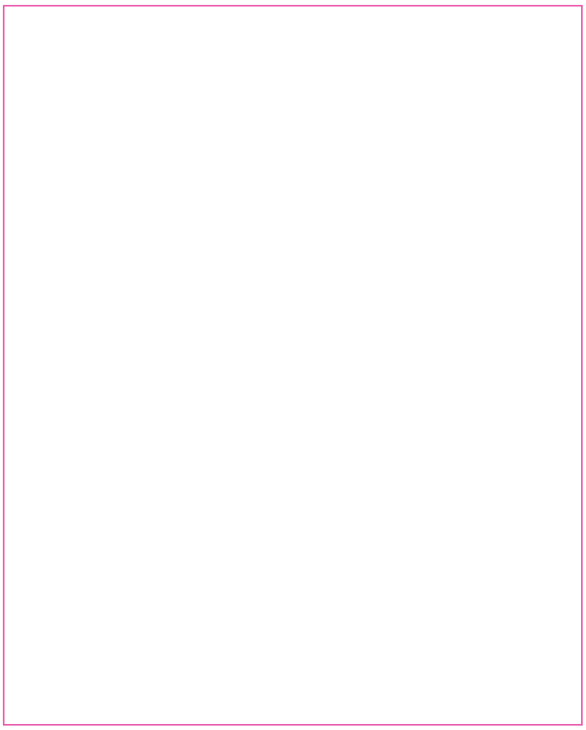


Figure 69. M1 Board Outline

10.4 Altium Project

To download the Altium project files, see the design files at TIDA-00201.

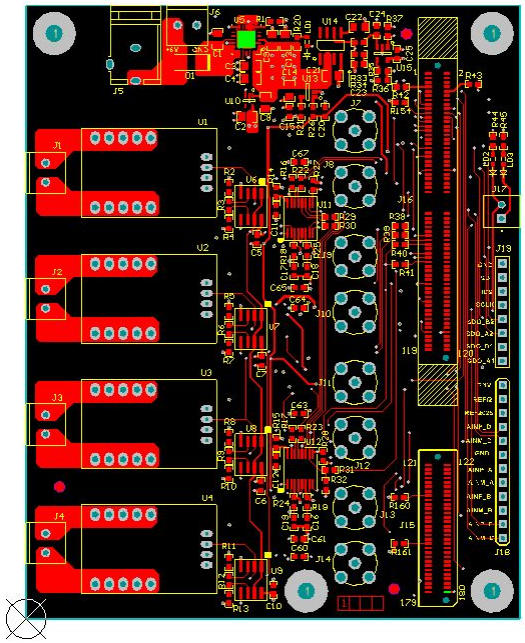


Figure 70. Top Layer

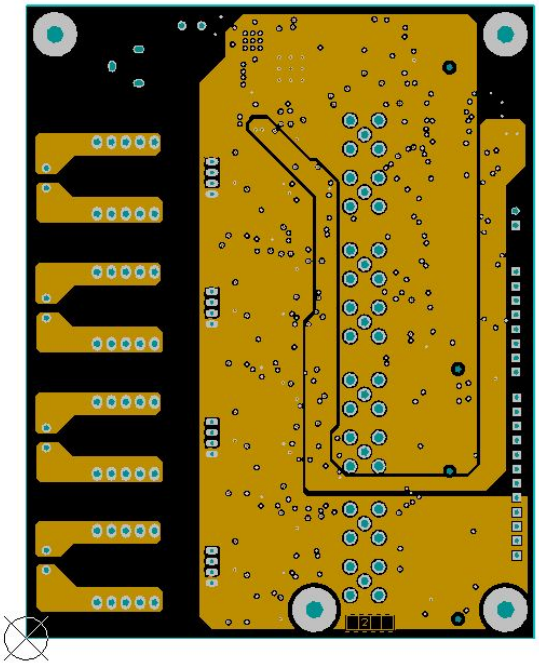


Figure 71. PWR Layer

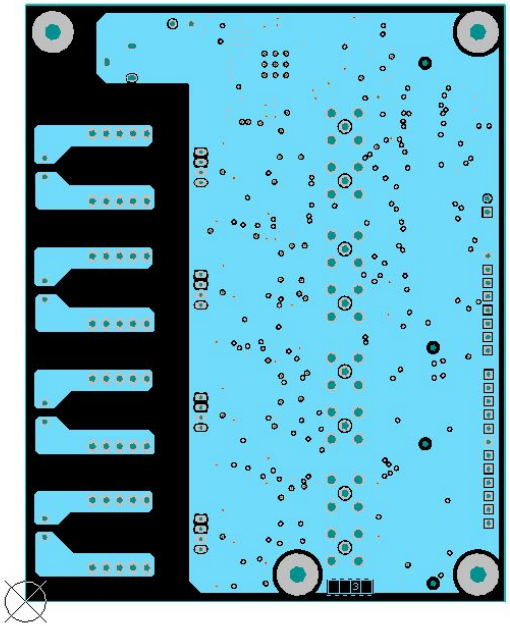


Figure 72. GND Layer

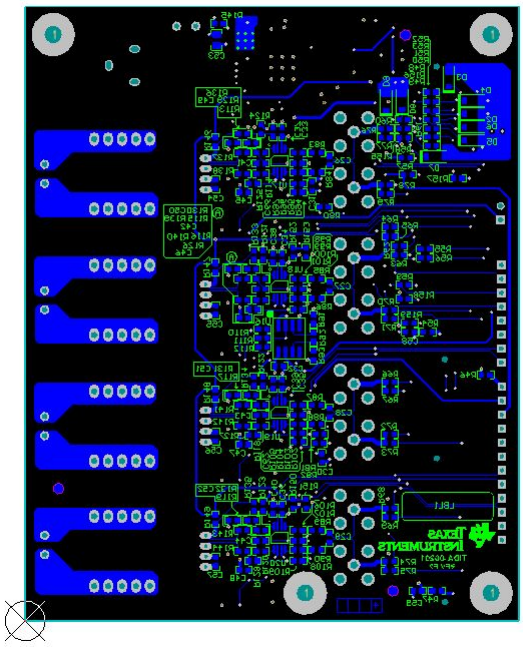


Figure 73. Bottom Layer

10.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00201.

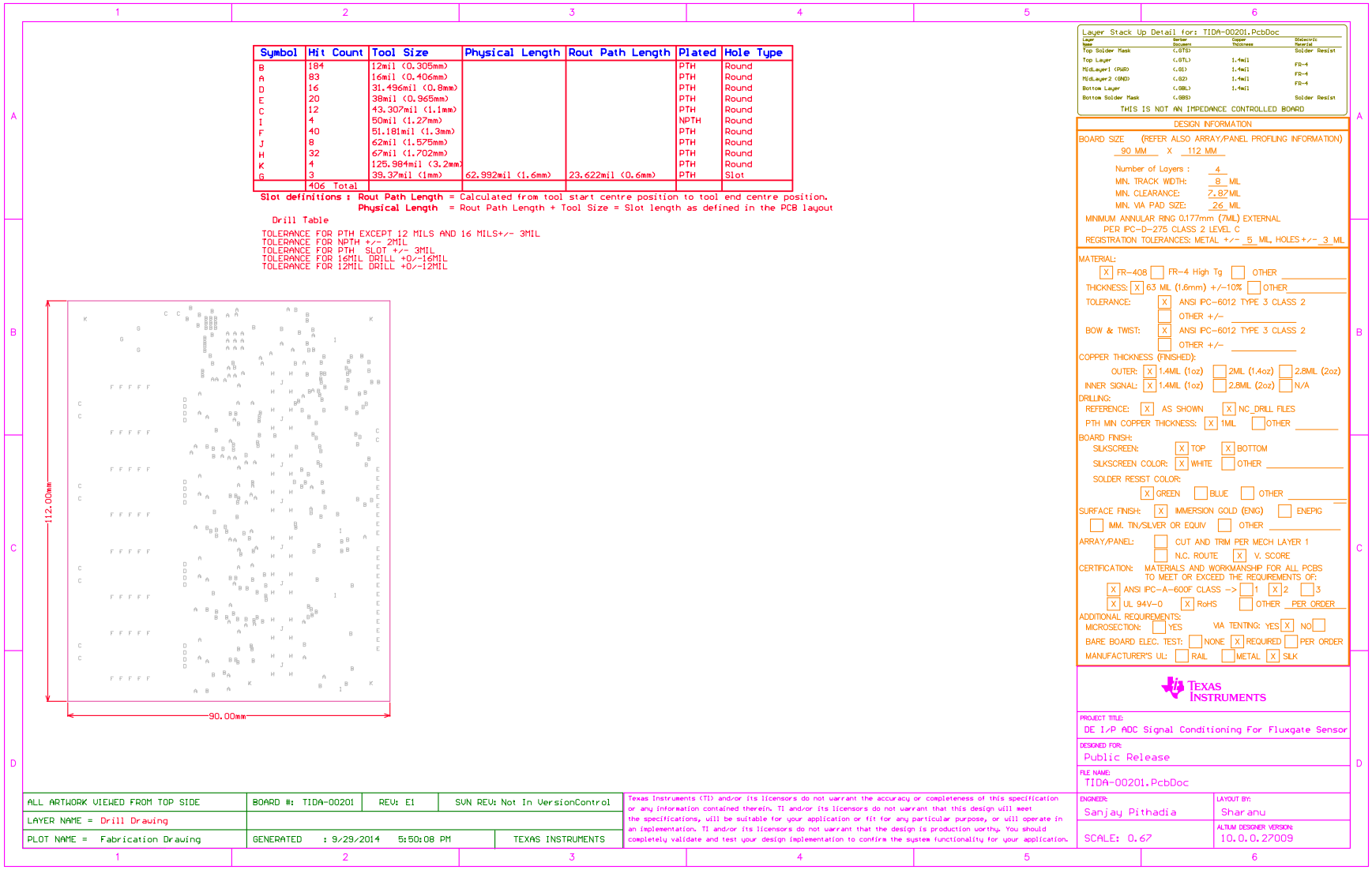


Figure 74. Fabrication Drawing

10.6 Assembly Drawings

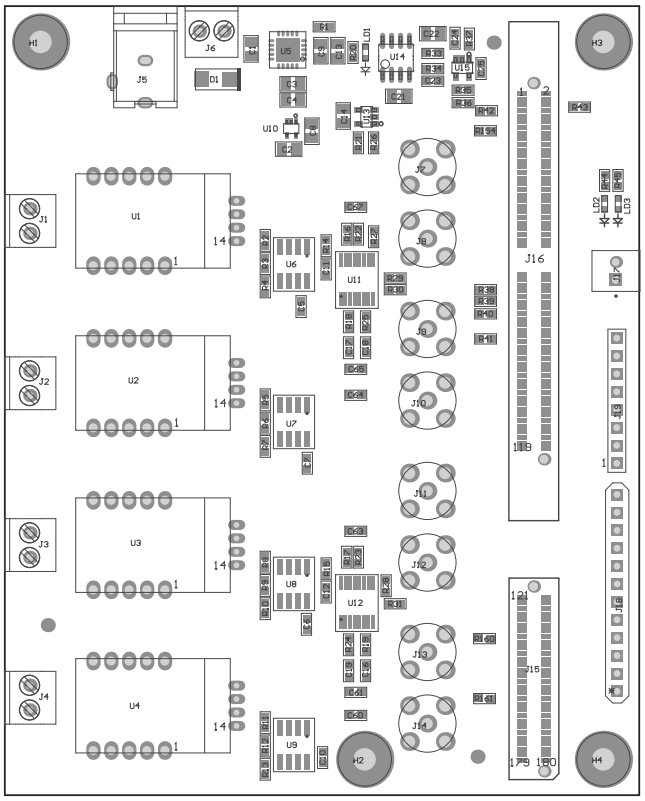


Figure 75. Top Assembly Drawing

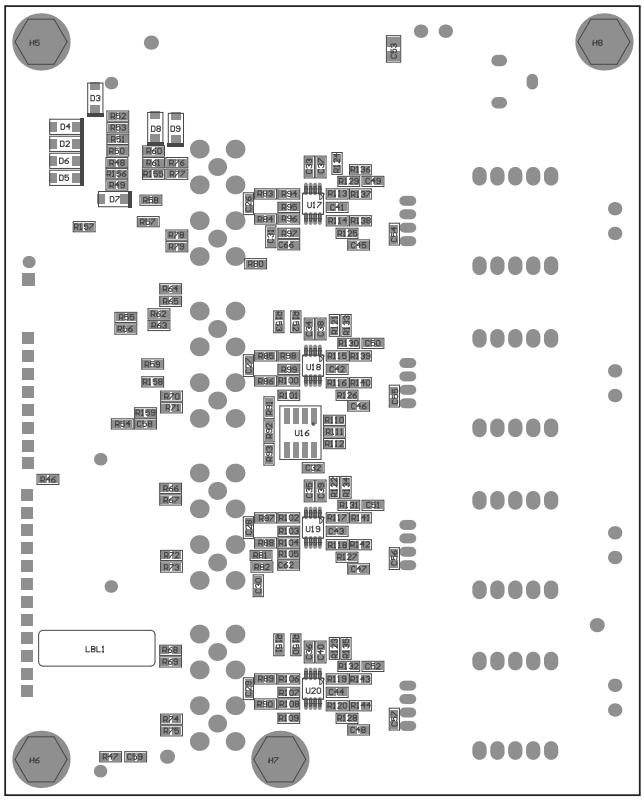


Figure 76. Bottom Assembly Drawing

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